

DUAL NON-INVERTING POWER DRIVER

FEATURES

- 3.0A Peak Current Totem Pole Output
- 5 to 35V Operation
- 25ns Rise and Fall Times
- 25ns Propagation Delays
- Thermal Shutdown and Under-Voltage Protection
- High-Speed, Power MOSFET Compatible
- Efficient High Frequency Operation
- Low Cross-Conduction Current Spike
- Enable and Shutdown Functions
- Wide Input Voltage Range
- ESD Protection to 2kV

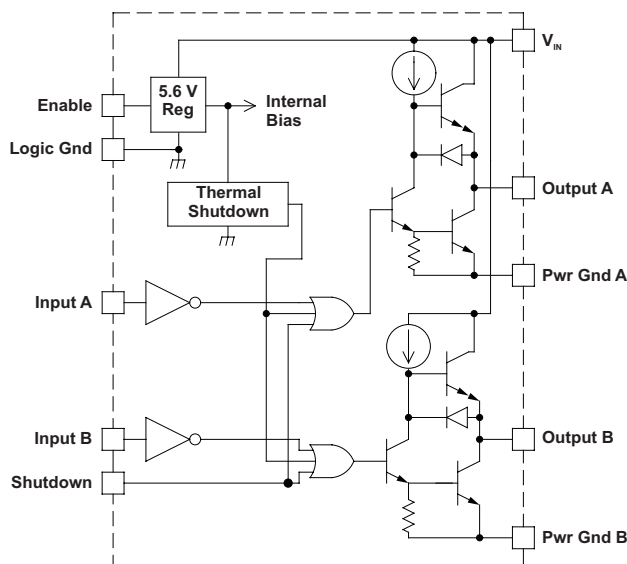
DESCRIPTION

The UC1708 family of power drivers is made with a high-speed, high-voltage, Schottky process to interface control functions and high-power switching devices – particularly power MOSFETs. Operating over a 5 V to 35 V supply range, these devices contain two independent channels. The A and B inputs are compatible with TTL and CMOS logic families, but can withstand input voltages as high as V_{IN} . Each output can source or sink up to 3 A as long as power dissipation limits are not exceeded.

Although each output can be activated independently with its own inputs, they can be forced low in common through the action of either a digital high signal at the Shutdown terminal or by forcing the Enable terminal low. The Shutdown terminal will only force the outputs low, it will not effect the behavior of the rest of the device. The Enable terminal effectively places the device in under-voltage lockout, reducing power consumption by as much as 90%. During under-voltage and disable (Enable terminal forced low) conditions, the outputs are held in a self-biasing, low-voltage, state.

The UC3708 and UC2708 are available in plastic 8-pin MINI DIP and 16-pin *bat-wing* DIP packages for commercial operation over a 0°C to 70°C temperature range and industrial temperature range of –25°C to 85°C respectively. For operation over a –55°C to 125°C temperature range, the UC1708 is available in hermetically sealed 8-pin MINI CDIP, 16 pin CDIP and 20 pin CLCC packages. Surface mount devices are also available.

BLOCK DIAGRAM



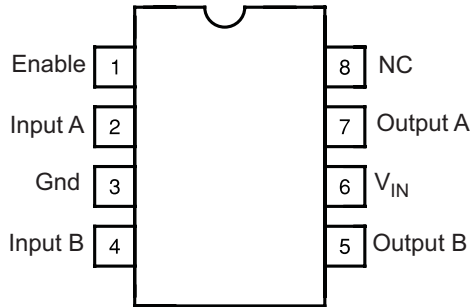
NOTE: Shutdown feature is not available in J or N packages only.



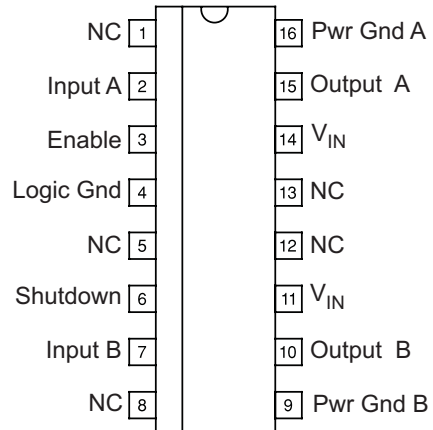
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

CONNECTION DIAGRAMS

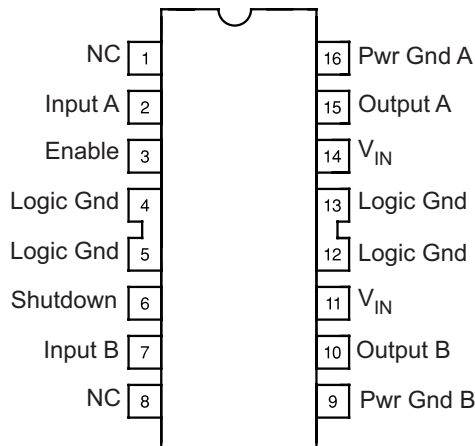
DIL-8 (Top View)
J Or N Package



SOIC-16 (Top View)
DW Package

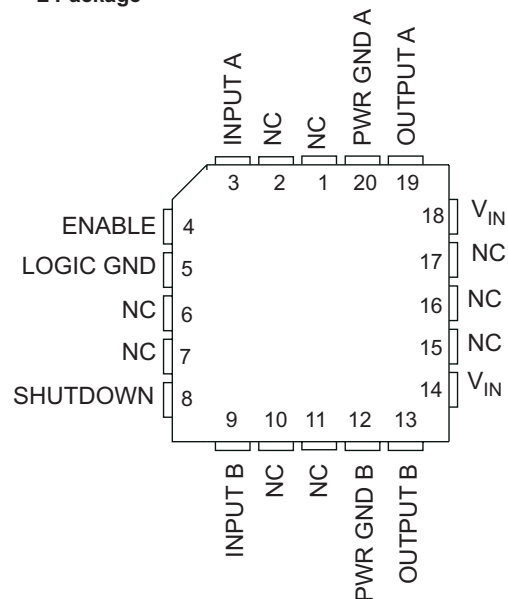


DIL-16 (Top View)
JE Or NE Package



Note: In JE package, Pin 4 is Logic Ground.
Pins 5, 12, and 13 are no connect.

CLCC-20 (Top View)
L Package



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| | VALUE | UNIT |
|---|----------------------------|------|
| Supply Voltage, V_{IN} | 35 | V |
| Output Current (Each Output, Source or Sink) | Steady-State | 0.5 |
| | Peak Transient | 3 |
| Output Voltage | -0.3 to ($V_{IN} + 0.3$) | V |
| Enable and Shutdown Inputs | -0.3 to 6.2 | V |
| A and B Inputs | -0.3 to ($V_{IN} + 0.3$) | V |
| Operating Junction Temperature ⁽²⁾ | 150 | °C |
| Storage Temperature Range | -65 to 150 | °C |
| Lead Temperature (Soldering, 10 Seconds) | 300 | °C |

(1) All voltages are with respect to Logic Gnd pin. All currents are positive into, negative out of, device terminals.

(2) Consult Unitorde Integrated Circuits databook for information regarding thermal specifications and limitations of packages.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated, $V_{IN}=10V$ to 35V, and these specifications apply for: $-55^{\circ}C < T_A < 125^{\circ}C$ for the UC1708,

$-25^{\circ}C < T_A < 85^{\circ}C$ for the UC2708, and $0^{\circ}C < T_A < 70^{\circ}C$ for the UC3708, $T_A = T_J$

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------|-------------------------------------|-----------------------|------|------|-----|------|
| V_{IN} | Supply current | Outputs low | | 18 | 26 | mA |
| | | Outputs high | | 14 | 18 | |
| | | Enable = 0 V | | 1 | 4 | |
| | A, B and shutdown inputs low level | | | | 0.8 | V |
| | A, B and shutdown inputs high level | | 2.0 | | | V |
| | A, B Input current low | $V_{A,B} = 0.4V$ | -1 | -0.6 | | mA |
| | A, B Input current high | $V_{A,B} = 2.4V$ | -200 | | 50 | A |
| | A, B Input leakage current high | $V_{A,B} = 35.3V$ | | | 200 | A |
| | Shutdown input current low | $V_{SHUTDOWN} = 0.4V$ | | 20 | 100 | A |
| | Shutdown input current high | $V_{SHUTDOWN} = 2.4V$ | | 170 | 500 | A |
| | | $V_{SHUTDOWN} = 6.2V$ | | 0.6 | 1.5 | mA |
| | Enable input current low | $V_{ENABLE} = 0V$ | -600 | -460 | 200 | A |
| | Enable input current high | $V_{ENABLE} = 6.2V$ | | | 200 | A |
| | Enable threshold rising | | | 2.8 | 3.6 | V |
| | Enable threshold falling | | 1.0 | 2.4 | 3.4 | V |
| $V_{IN} - V_{OUT}$ | Output High Saturation | $I_{OUT} = -50mA$ | | | 2.0 | V |
| | | $I_{OUT} = -500mA$ | | | 2.5 | V |
| V_{OUT} | Output Low Saturation | $I_{OUT} = 50mA$ | | | 0.5 | V |
| | | $I_{OUT} = 500mA$ | | | 2.5 | V |
| | Thermal Shutdown | | | 155 | | °C |

SWITCHING CHARACTERISTICS (see Figure 1)

(VIN = 20V, delays measured to 10% output change.)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------------------|----------------------------|---------------|-----|-----|-----|------|
| FROM A,B INPUT TO OUTPUT: | | | | | | |
| Rise Time Delay (TPLH) | CL = 0pF | | | 25 | 40 | ns |
| | CL = 1000pF | UC1708 | | 25 | 45 | ns |
| | | UC2708/UC3708 | | 25 | 40 | |
| | CL = 2200pF | UC1708 | | 25 | 50 | ns |
| | | UC2708/UC3708 | | 25 | 45 | |
| | 10% to 90% Rise (TTLH) | CL = 0pF | | | 55 | 75 |
| CL = 1000pF ⁽¹⁾ | | UC1708 | | 25 | 80 | ns |
| | | UC2708/UC3708 | | 25 | 50 | |
| CL = 2200pF | | UC1708 | | 40 | 85 | ns |
| | | UC2708/UC3708 | | 40 | 55 | |
| Fall Time Delay (TPHL) | | CL = 0pF | | | 25 | 40 |
| | CL = 1000pF ⁽¹⁾ | | | 25 | 45 | |
| | CL = 2200pF | | | 35 | 50 | |
| 90% to 10% Fall (TTHL) | CL = 0pF | | | 15 | 20 | ns |
| | CL = 1000pF ⁽¹⁾ | | | 25 | 45 | |
| | CL = 2200pF | | | 40 | 55 | |

(1) These parameters, specified at 1000pF, although ensured over recommended operating conditions, are not tested in production.

SWITCHING CHARACTERISTICS (see Figure 1)

(VIN = 20V, delays measured to 10% output change.)

| PARAMETER | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---------------------------------------|--|---------------|-----|-----|-----|------|
| FROM SHUTDOWN INPUT TO OUTPUT: | | | | | | |
| Rise Time Delay (TPLH) | CL = 0pF | | | 25 | 75 | ns |
| | CL = 1000pF ⁽¹⁾ | UC1708 | | 30 | 80 | ns |
| | | UC2708/UC3708 | | 30 | 75 | |
| | CL = 2200pF | UC1708 | | 35 | 85 | ns |
| | | UC2708/UC3708 | | 35 | 75 | |
| | 10% to 90% Rise (TTLH) | CL = 0pF | | | 50 | 75 |
| CL = 1000pF ⁽¹⁾ | | UC1708 | | 25 | 80 | ns |
| | | UC2708/UC3708 | | 25 | 50 | |
| CL = 2200pF | | UC1708 | | 40 | 85 | ns |
| | | UC2708/UC3708 | | 40 | 55 | |
| Fall Time Delay (TPHL) | | CL = 0pF | | | 25 | 45 |
| | CL = 1000pF ⁽¹⁾ | | | 30 | 50 | |
| | CL = 2200pF | | | 35 | 55 | |
| 90% to 10% Fall (TTHL) | CL = 0pF | | | 25 | 20 | ns |
| | CL = 1000pF ⁽¹⁾ | | | 25 | 45 | |
| | CL = 2200pF | | | 40 | 55 | |
| Total Supply Current | F = 200kHz, 50% duty cycle, both channels; CL = 0pF | | | 23 | 25 | mA |
| | F = 200kHz, 50% duty cycle, both channels; CL = 2200pF | | | 38 | 45 | |

(1) These parameters, specified at 1000pF, although ensured over recommended operating conditions, are not tested in production.

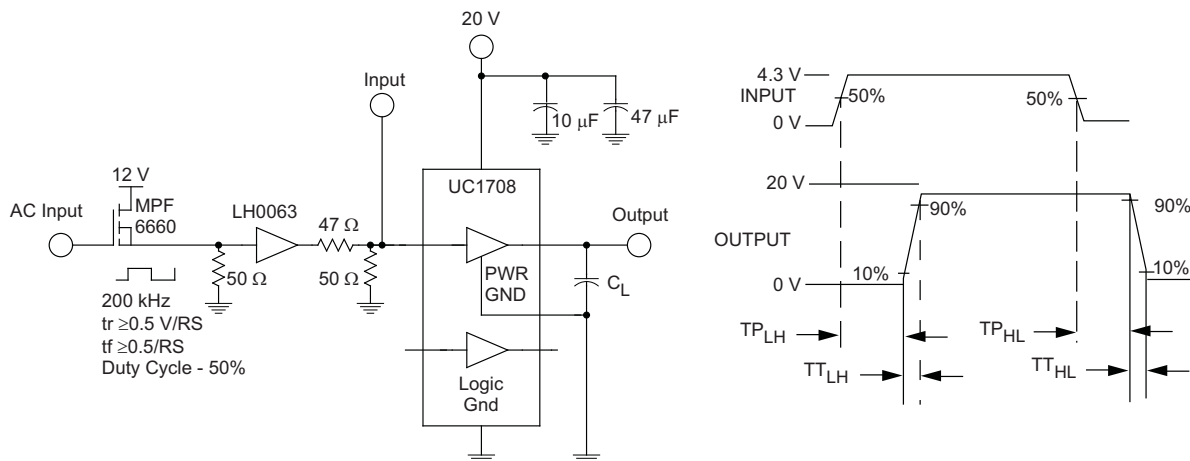
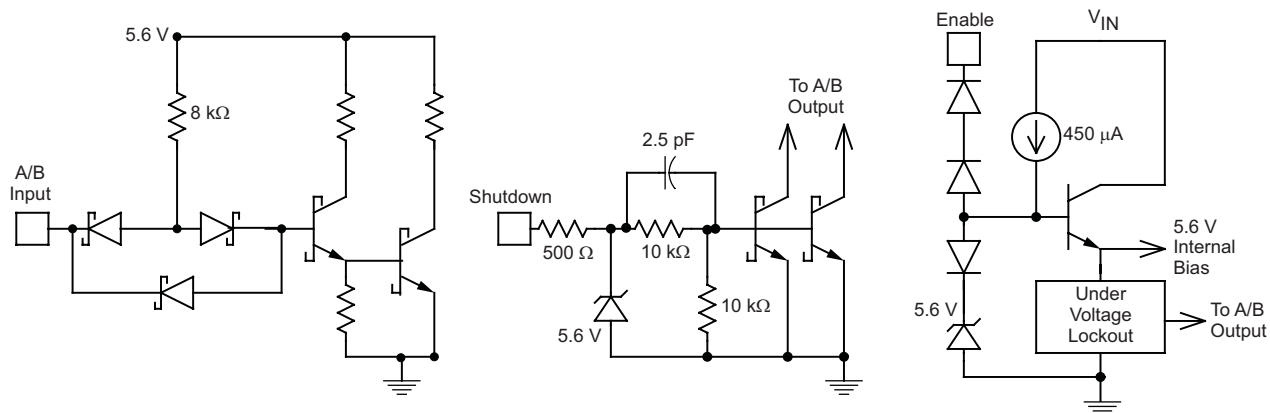


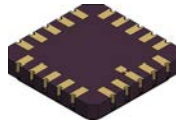
Figure 1. AC Test Circuit and Switching Time Waveforms



NOTE: Shutdown feature available only in JE, NE or DW Packages.

Figure 2. Equivalent Input Circuits

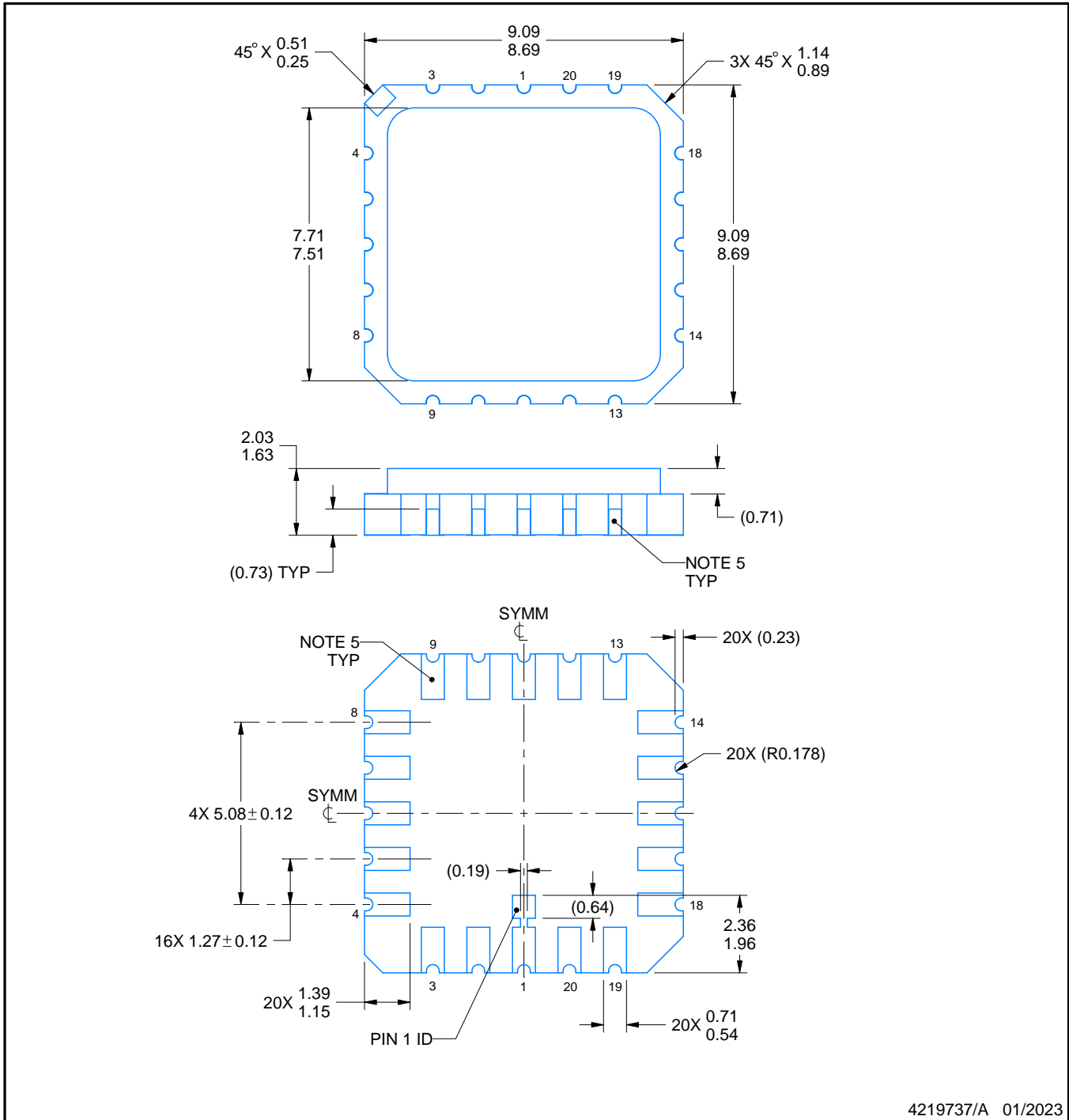
FK0020A



PACKAGE OUTLINE

LCCC - 2.03 mm max height

LEADLESS CERAMIC CHIP CARRIER



4219737/A 01/2023

NOTES:

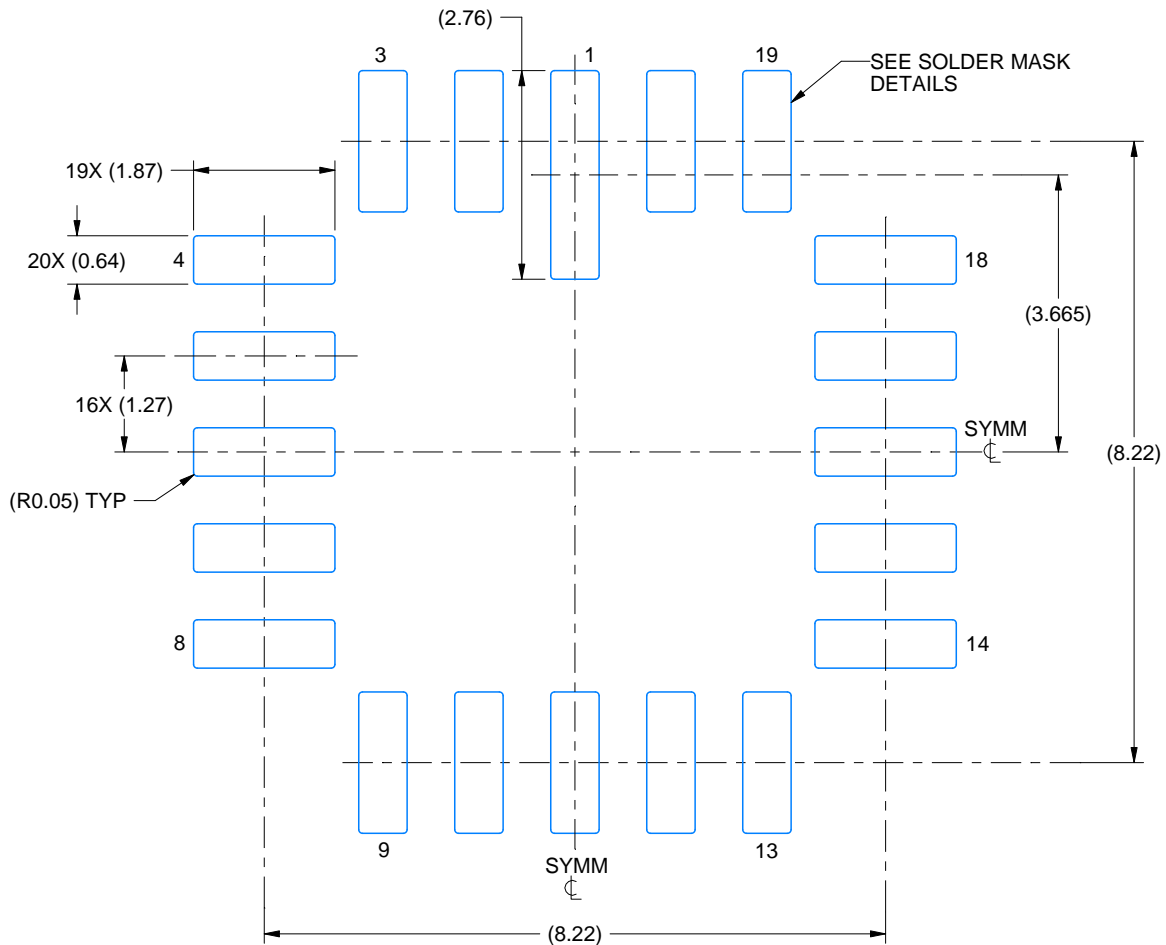
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a metal lid.
4. Reference JEDEC Registration MS-004.
5. The terminals are gold-plated.

EXAMPLE BOARD LAYOUT

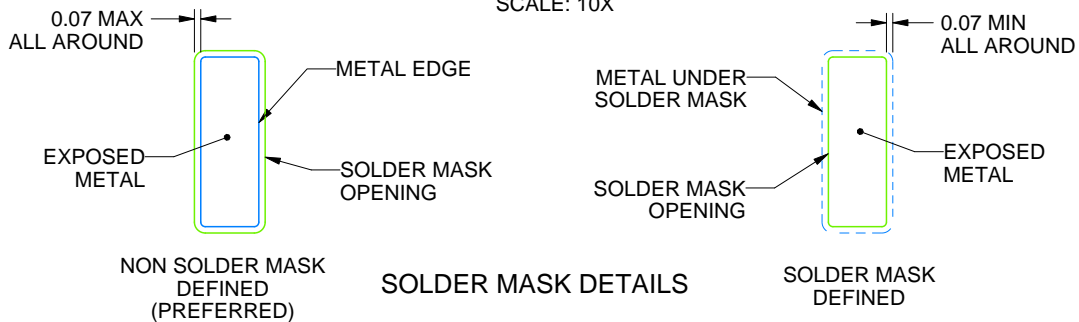
FK0020A

LCCC - 2.03 mm max height

LEADLESS CERAMIC CHIP CARRIER



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4219737/A 01/2023

NOTES: (continued)

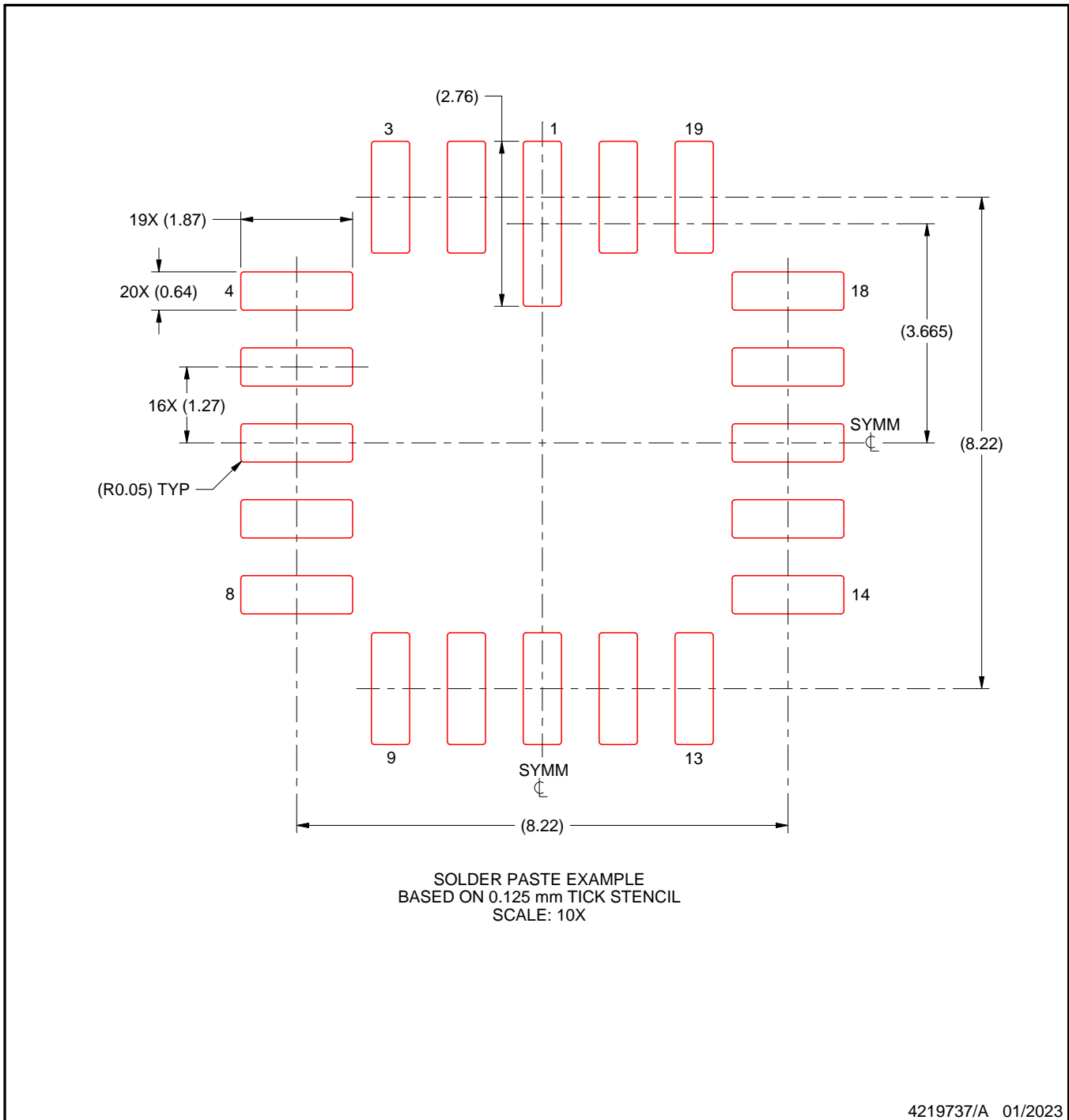
6. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

FK0020A

LCCC - 2.03 mm max height

LEADLESS CERAMIC CHIP CARRIER



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|--------------------------------------|-------------------------|
| 5962-0051401Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-0051401Q2A UC1708L/ 883B | Samples |
| 5962-0051401QEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-0051401QE A UC1708JE/883B | Samples |
| 5962-0051401QPA | ACTIVE | CDIP | JG | 8 | 50 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 0051401QPA UC1708 | Samples |
| 5962-0051401V2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-0051401V2A UC1708L QMLV | Samples |
| 5962-0051401VEA | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-0051401VE A UC1708JEQMLV | Samples |
| 5962-0051401VPA | ACTIVE | CDIP | JG | 8 | 50 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 0051401VPA UC1708 | Samples |
| UC1708J | ACTIVE | CDIP | JG | 8 | 50 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | UC1708J | Samples |
| UC1708J883B | ACTIVE | CDIP | JG | 8 | 50 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 0051401QPA UC1708 | Samples |
| UC1708JE | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | UC1708JE | Samples |
| UC1708JE883B | ACTIVE | CDIP | J | 16 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-0051401QE A UC1708JE/883B | Samples |
| UC1708L883B | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-0051401Q2A UC1708L/ 883B | Samples |
| UC2708DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2708DW | Samples |
| UC2708DWTR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | UC2708DW | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| UC2708N | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | UC2708N | Samples |
| UC3708DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3708DW | Samples |
| UC3708DWG4 | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3708DW | Samples |
| UC3708DWTR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | UC3708DW | Samples |
| UC3708N | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3708N | Samples |
| UC3708NE | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3708NE | Samples |
| UC3708NG4 | ACTIVE | PDIP | P | 8 | 50 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | UC3708N | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF UC1708, UC1708-SP, UC3708 :

- Catalog : [UC3708](#), [UC1708](#)
- Military : [UC1708](#)
- Space : [UC1708-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| UC2708DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| UC3708DWTR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| UC2708DWTR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| UC3708DWTR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-0051401Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-0051401V2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC1708L883B | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| UC2708DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC2708N | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| UC3708DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3708DWG4 | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| UC3708N | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |
| UC3708NE | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| UC3708NG4 | P | PDIP | 8 | 50 | 506 | 13.97 | 11230 | 4.32 |

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

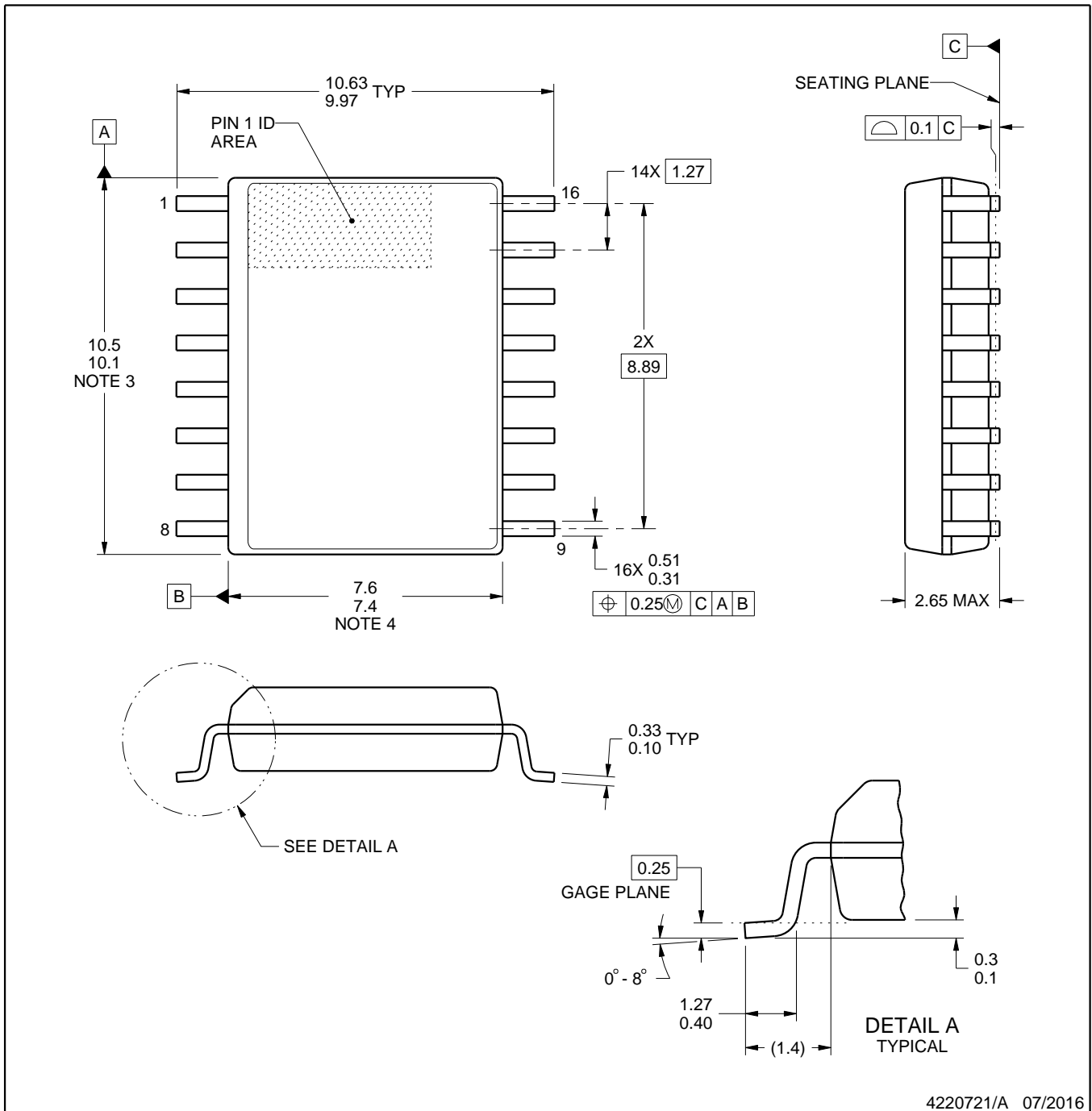


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

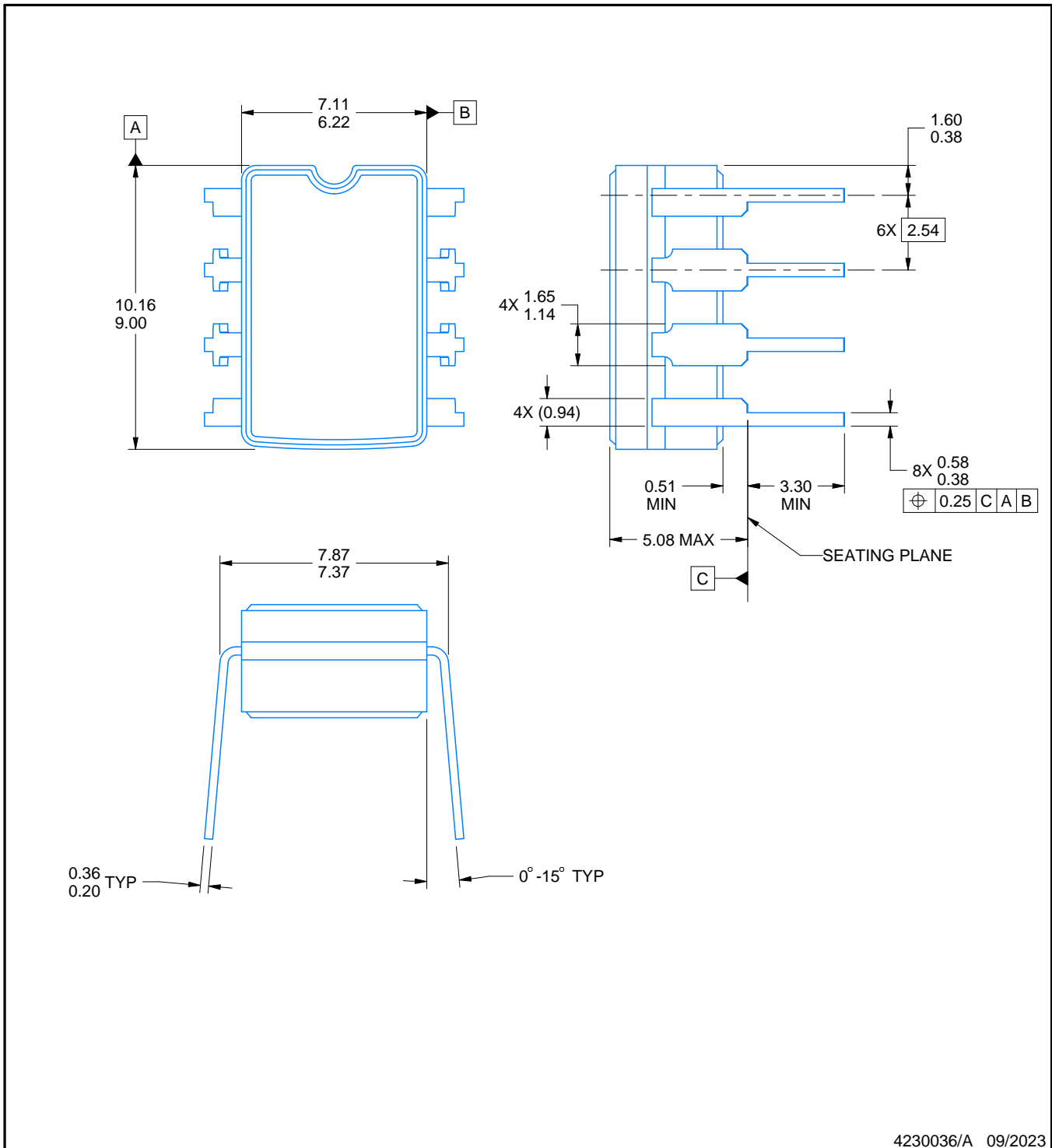
- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



NOTES:

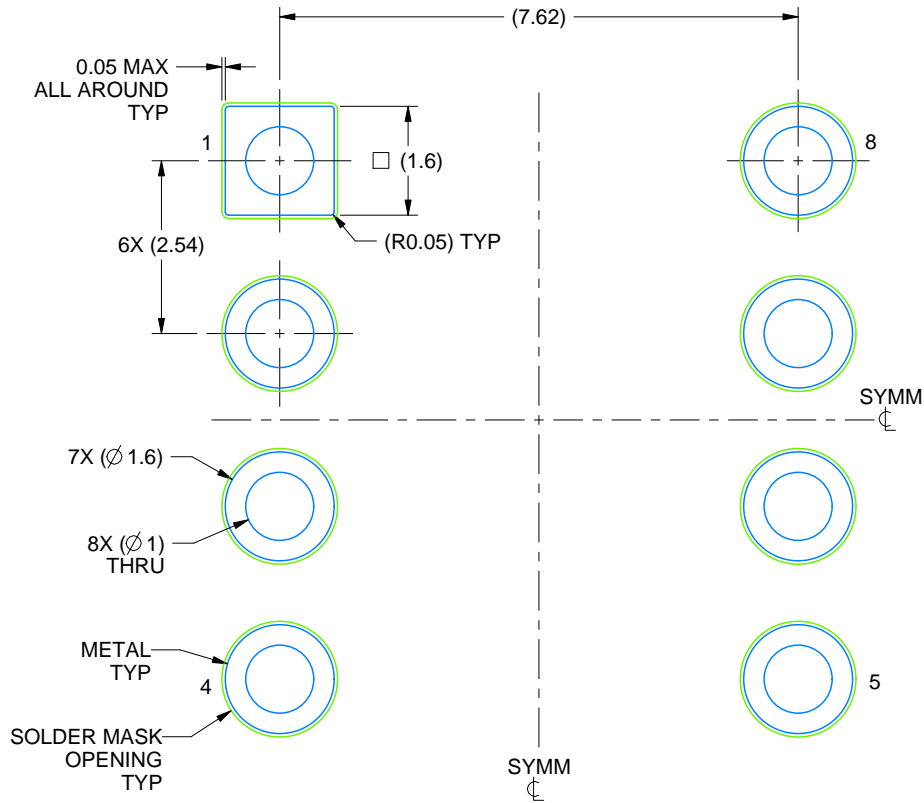
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package can be hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification.
5. Falls within MIL STD 1835 GDIP1-T8

EXAMPLE BOARD LAYOUT

JG0008A

CDIP - 5.08 mm max height

CERAMIC DUAL IN-LINE PACKAGE



LAND PATTERN EXAMPLE
NON SOLDER MASK DEFINED
SCALE: 9X

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