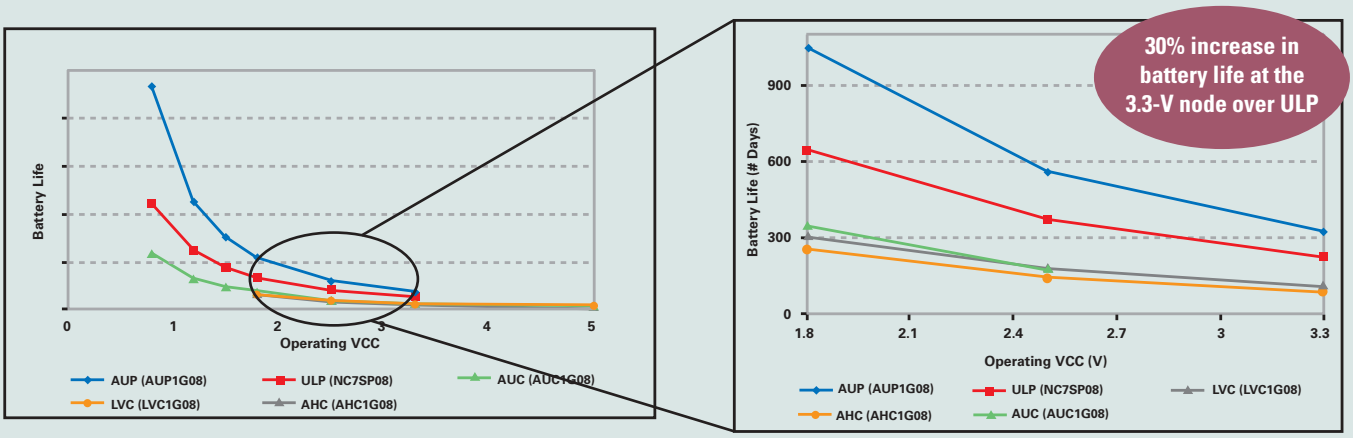
Advanced Ultra Low Power (AUP) Logic

Designed to help extend battery life in portable applications, Texas Instrument's (TI) new AUP family makes logic virtually unnoticeable in low voltage battery-powered system designs. AUP offers the industry's lowest power logic technology without sacrificing speed and signal integrity. Combined with TI's Wafer Chip Scale Package (WCSP), AUP holds the title as the world's smallest low power solution. This advantage also makes it the ideal logic technology for portable applications.

Benefits

- Lower Power: 91% less static power and 83% less dynamic power than industry standard 3.3-V logic
- Low EMI: Tightly controlled output-signal edge rates yield excellent signal integrity
- Wide V_{CC} Range: 0.8-V to 3.6-V V_{CC} range allows for interface with next-generation and legacy processors
- Fast T_{PD}: 2.0 ns (typ) at 3.3 V and 3.0 ns (typ) at 1.8 V
- Input hysteresis (150-mV typical @ 3.3-V V_{CC}) allows slow signal transitions and better noise immunity at the input

Increased Battery Life



Assumptions:

- 3.3-V lithium battery
- 850 mAH charge
- 90% efficiency
- Seven 1G08 functions:
  - Running at 10 MHz for 1 hour
  - Stand-by mode for 23 hours

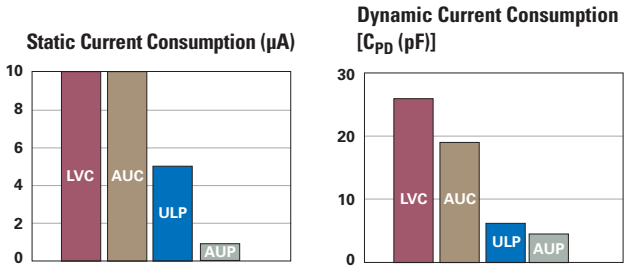
Assumptions:

- Battery Life (No. of Days) = 3.3 * 850 * 0.9/P_T
- P_T = 23 * Static Power + Dynamic Power = 23 * P_D + P_S
- P_D = (C_{PD}+C_L) * $V_{CC}2$ * f
- C_L = 5 pF, f =10 MHz
- P_S = V_{CC} * I_{CC}

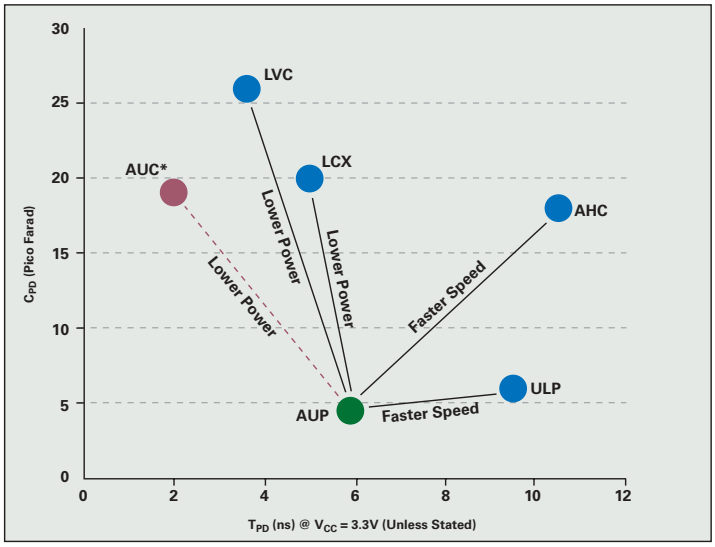
Figure 1. Battery life with 1-hr switching and 23-hr standby (5-pF load, 7 devices)

Decreased Power Consumption

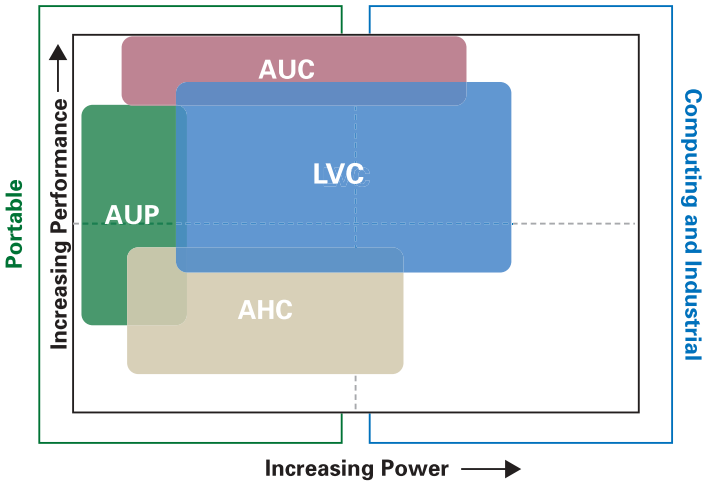
By using 91% less static power and 83% less dynamic power than the industry standard 3.3-V logic technology (LVC), AUP is able to increase battery life. As noted in Figure 1, AUP offers a 30% increase in battery life over ULP and 73% over 3.3-V logic technology.



AUP is particularly suitable to drive CMOS loads commonly found in portable applications. With the lowest static and dynamic power consumptions in the industry, AUP maintains the fastest speed of its class. Excellent speed-power performance makes it suitable for wide range operating frequencies. (See diagram below.)



*AUC is shown here for reference purpose only; AUC max V_{CC} is 2.7 V. The data for AUC represents 2.5V V_{CC} node.



TI's broad Little Logic portfolio offers designers a multitude of functions and technologies to meet their needs. AUP provides best-in-class power consumption without substantially sacrificing speed. AUP offers similar performance to LVC, but provides significant power savings. AUP Little Logic is complimented by AUC and LVC (see diagram above). Presently, LVC offers more single-, dual- and triple-gate functions to select from TI's broad Little Logic portfolio.

	AUP	ULP	LVC	AUC	AHC
V_{CC}	0.8 V to 3.6 V	0.9 V to 3.6 V	1.65 V to 5.5 V	0.8 V to 2.7 V	2.0 V to 5.5 V
I_{CC}	0.9 µA	5 µA	10 µA	10 µA	10 µA
I_I	0.5 µA	0.9 µA	5 µA	5 µA	1 µA
I_{OFF}	0.5 µA	5 µA	10 µA	10 µA	No I_{OFF}
I_{OZ}	0.5 µA	5 µA	5 µA	10 µA	5 µA
C_{PD}	4.5 pF	6 pF	26 pF	19 pF	18 pF
C_{IN}	1.5 pF	2 pF	4 pF	3 pF	4 pF
C_{OUT}	3 pF	4 pF	NS	NS	NS
T_{PD} (max)	4.3 ns (5 pF), 5.9 ns (15 pF)	9.5 ns (15 pF)	3.6 ns (15 pF)	2 ns (30 pF)	10.5 ns (15 pF)
I_{OH}/I_{OL}	4 mA	2.6 mA	24 mA	9 mA	4 mA

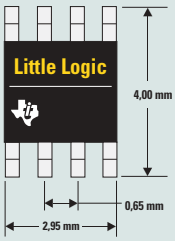
Note: The C_{PD}, I_{OH}, I_{OL} and T_{PD} data represent the 3.3-V V_{CC} node except for the AUC. The data for the AUC represents the 2.5-V V_{CC} node.

Packaging

Lead Frame

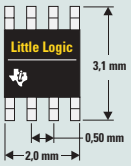
DCT (SM-8)

(Actual Size)



DCU (US-8)

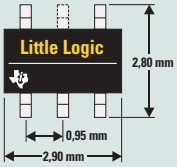
(Actual Size)



DBV (SOT-23)

5-pin or 6-pin

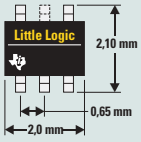
(Actual Size)



DCK (SC-70)

5-pin or 6-pin

(Actual Size)



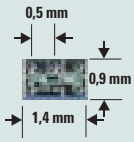
Wafer Chip-Scale

NanoStar™ (YEP)

5-pin or 6-pin

(Actual Size)

NanoFree™ (YZP)



Pb-FREE

TEXAS INSTRUMENTS