JESD204B
Physical Layer (PHY)

Texas Instruments High Speed Data Converter Training

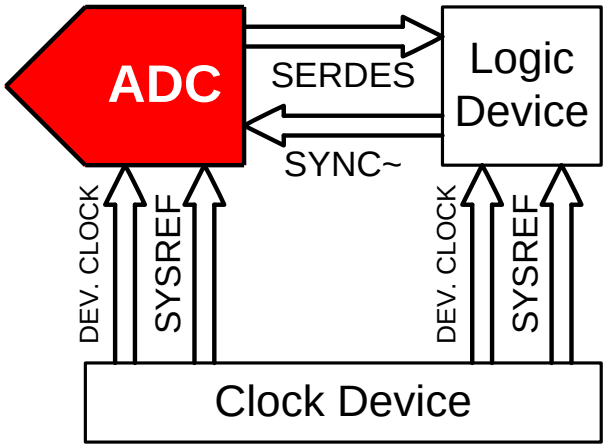
Overview

- What is the Physical Layer (PHY)?
- Speed Grades and Compliance Types
- SERDES Interface
- Solutions for Long/Lossy Channels
- Device Clock, SYSREF and SYNC~ Interfaces
- PCB Layout Recommendations

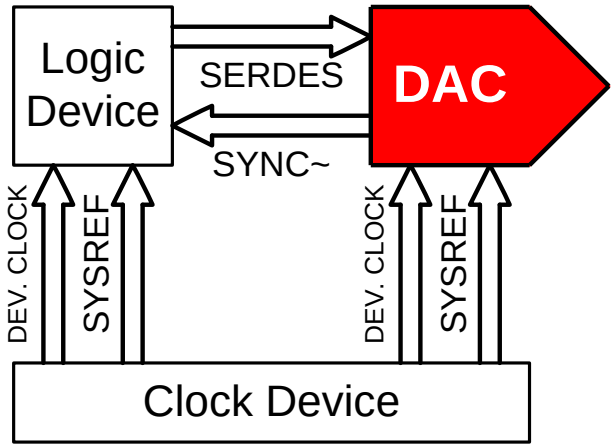
What is the Physical Layer (PHY)?

- The “Physical Layer” refers to the serial data transmitter and receiver of the JESD204B link
- Point-to-point, unidirectional serial interface
- Definition includes electrical and timing characteristics
- This presentation also considers the other signal interfaces

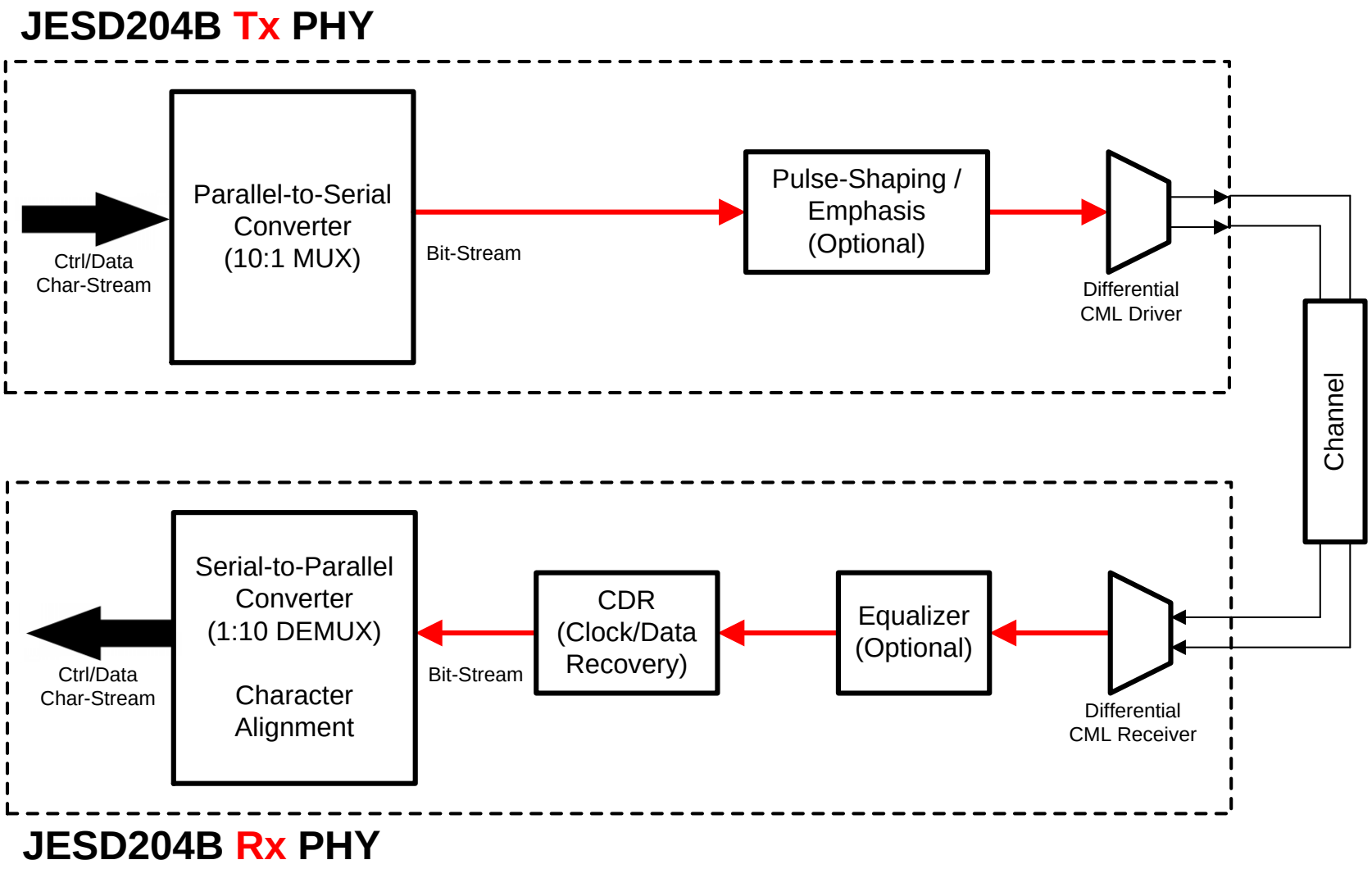
JESD204B Subclass 1
ADC Interfaces



JESD204B Subclass 1
DAC Interfaces



What is the Physical Layer (PHY)?



Speed Grades and Compliance

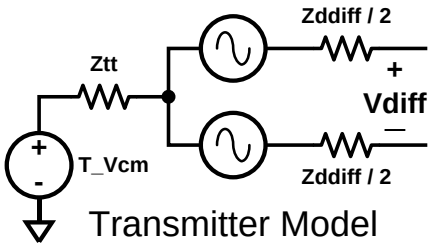
- The JESD204B standard defines 3 speed grade variants
- Based on OIF Optical standards (OIF-CEI-02.0)
- Variants differ most importantly in data rate, eye mask, and BER

Parameter	LV-OIF-Sx15	LV-OIF-6G-SR	LV-OIF-11G-SR
Data Rates	312.5Mbps – 3.125Gbps	312.5Mbps - 6.375Gbps	312.5Mbps – 12.5Gbps
Differential Output Voltage	500 – 1000 (mV)	400 – 750 (mV)	360 – 770 (mV)
Output Rise or Fall Time (20% - 80% into 100Ω load)	≥ 50 (ps)	≥ 30 (ps)	≥ 24 (ps)
Bit Error Rate (BER)	≤ 1e-12	≤ 1e-15	≤ 1e-15

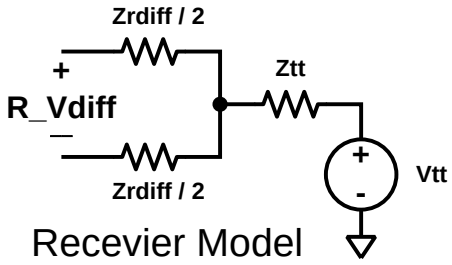
- Compliance refers to AC or DC coupling and impacts the electrical characteristics of the driver/receiver

PHY Electrical Requirements

- PHY defines the I/O electrical structure of the driver and receiver



Transmitter Model



Recevier Model

Common Mode Voltage Range

Signal Swing Range

Impedance and Return Losses

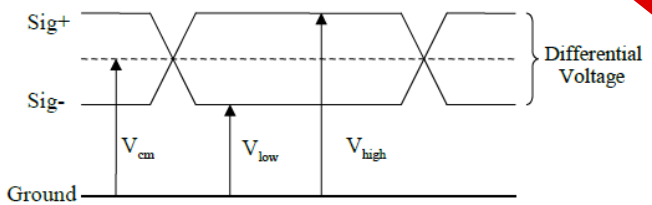
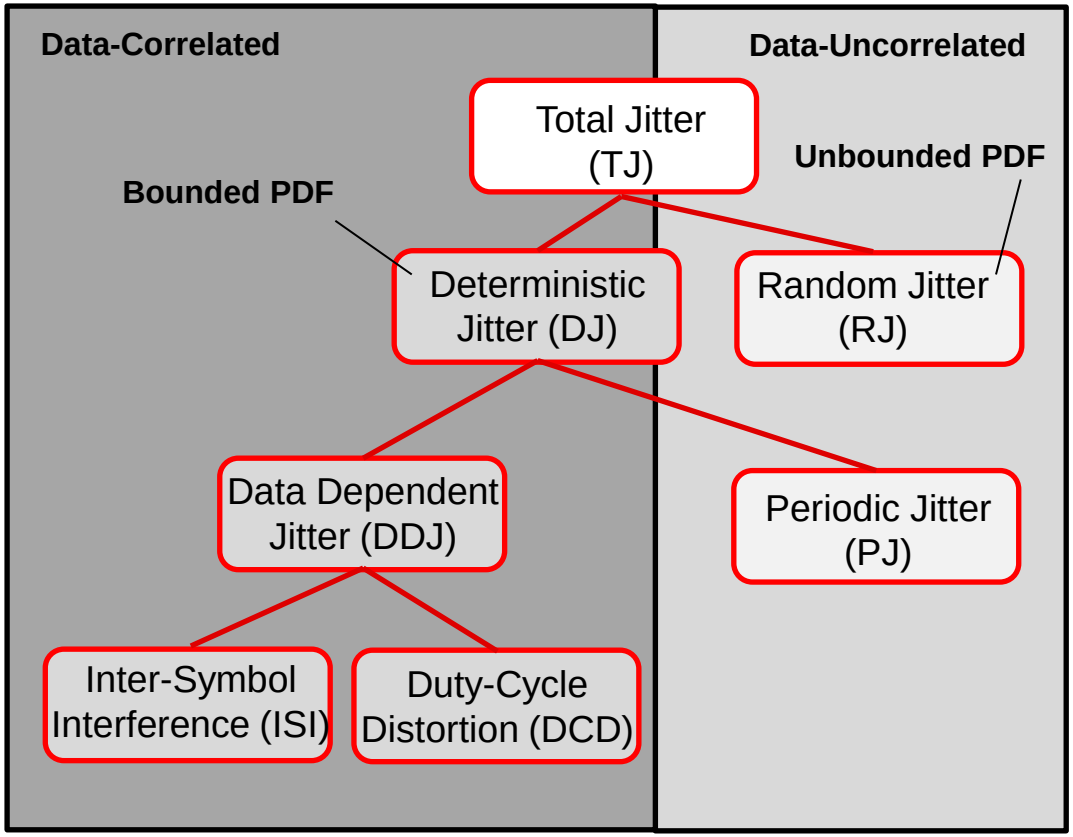


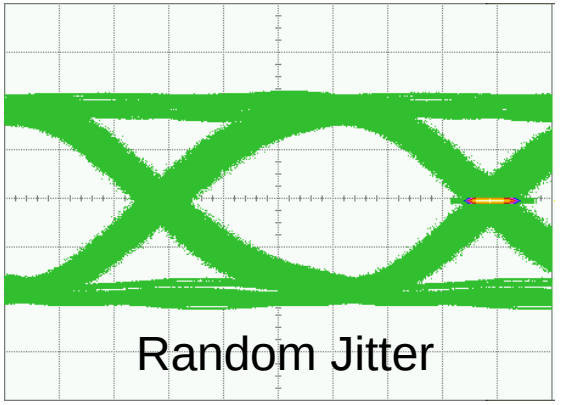
Figure 2 — Differential peak-to-peak Voltage = 2 * (V_{high} – V_{low})

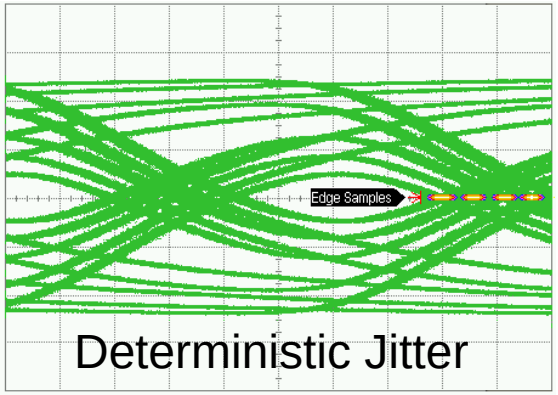
Symbol	Parameter	Conditions	Min	Max	Units
UI	Unit Interval	(Note 1)	80	156.9	ps
Trise/Tfall	Rise and Fall Times	20% - 80% into 100 Ω load	24	(Note 2)	ps
T_Vcm	Output Common Mode Voltage	Applies only to AC coupling. Termination circuit of Figure 5 applied at the Transmitter terminals and Transmitter Ground with parameters as per (Note 3).	0	1.8	V
		Required only if DC-Compliance is claimed. Termination circuit of Figure 5 applied at the Transmitter terminals and Transmitter Ground with parameters as per (Note 4).	735	1135	mV
		Required only if DC-Compliance is claimed. Termination circuit of Figure 5 applied at the Transmitter terminals and Transmitter Ground with parameters as per (Note 5).	550	1060	mV
		Required only if DC-Compliance is claimed. Termination circuit of Figure 5 applied at the Transmitter terminals and Transmitter Ground with parameters as per (Note 6).	490	850	mV
Vdiff	Transmitter Differential Voltage	Into floating 100 Ω load	360	770	mVppd
Idshort	Transmitter Short Circuit Current	Transmitter terminal(s) shorted to each other or ground, power on.	-100	+100	mA
Zddiff	Differential Impedance	At DC	80	120	Ω
RLddiff	Differential Output Return Loss	From 100MHz to 0.75*Baud Rate	8		dB
RLdcm	Common Mode	From 100MHz to 0.75*Baud Rate	6		dB

PHY Eye/Timing Requirements

- Total jitter is composed of both random and deterministic components
- JESD204B standard identifies requirements for different types of jitter







* “Analyzing Digital Jitter and its Components,” (Agilent Technologies)

PHY Eye/Timing Requirements

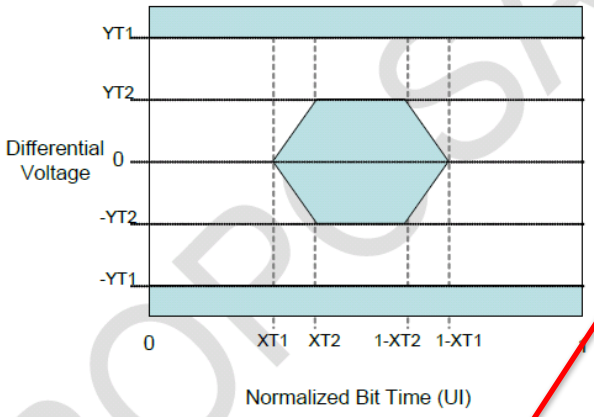
- Jitter Units
  - ‘peak-to-peak Unit Interval’ [p-p UI]:
    - 1 UI is equivalent to 1 bit period at the given transfer rate
  - ‘peak-to-peak seconds’ [p-p s]
  - ‘peak-to-peak Root-Mean-Square seconds’ [p-p rms]
    - Used to describe unbounded random jitter values
    - Must specify a BER to indicate probability density function (PDF) bounds for conversion to [p-p UI] (i.e. 1e-15)

- Combining Jitter Components
  - Random Jitter adds as sum of squares (un-correlated)
  - Deterministic Jitter sums directly (correlated)
  - Total Jitter is a direct sum of Random and Deterministic Components
    - TJ = RJ + DJ

PHY Eye/Timing Requirements

- TX and RX Eye Masks with amplitude, rise-time, and jitter requirements
- RX must recover signal after channel loss and ISI

Transmit Eye Mask

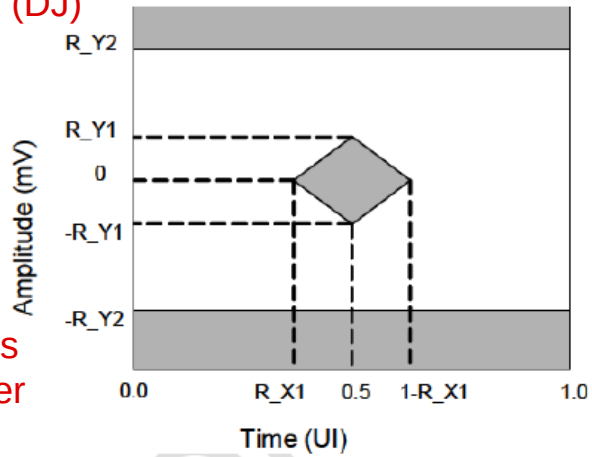


XT1 (UI)	XT2 (UI)	YT1 (V)	YT2 (V)	T_UBHPJ (p-p UI)	T_DCD (p-p UI)	TJ (p-p UI)
0.15	0.4	0.385	0.18	0.15	0.05	0.3

NOTE 1 T_UCHPJ = Transmit Uncorrelated Bounded High Probability Jitter
NOTE 2 T_DCD = Transmit Duty Cycle Distortion
NOTE 3 XT1 = TJ / 2.
NOTE 4 Unit Interval (UI) is specified in Table 6. However, for baud-rates greater than 11.1 Gsym/sec, UI shall be 90.09ps.
NOTE 5 The Gaussian Jitter (GJ) portion of the Total Jitter (TJ) is defined with respect to a BER of 1e-15 (Q=7.94).

Figure 9 Transmit Eye Mask for LV-OIF-11G-SR – based operation

Receive Eye Mask



R_X1 (UI)	1-R_X1 (UI)	R_Y1 (V)	R_Y2 (V)	R_SJ-hf (p-p UI)	R_SJ-max (p-p UI)	R_BHPJ (p-p UI)	TJ (p-p UI)
0.35	0.65	0.055	0. 525	0.05	5	0.45	0.70

NOTE 1 R_SJ-hf = Receive Sinusoidal Jitter, High Frequency
NOTE 2 R_SJ-max = Receive Sinusoidal Jitter, Maximum
NOTE 3 R_BHPJ = Receive Bounded High Probability Jitter – Breakdown is 0.25 UIpp Uncorrelated, 0.20 UIpp Correlated
NOTE 4 R_X1 = TJ / 2.
NOTE 5 Unit Interval (UI) is specified in Table 6. However, for baud-rates greater than 11.1 Gsym/sec, UI shall be 90.09ps.
NOTE 6 Total Jitter (TJ) includes high-frequency sinusoidal jitter (R_SJ-hf)
NOTE 7 The Gaussian Jitter (GJ) portion of the Total Jitter (TJ) is defined with respect to a BER of 1e-15 (Q=7.94).

Figure 10 — Receive Eye Mask for LV-OIF-11G-SR – based operation

Deterministic Jitter (DJ)

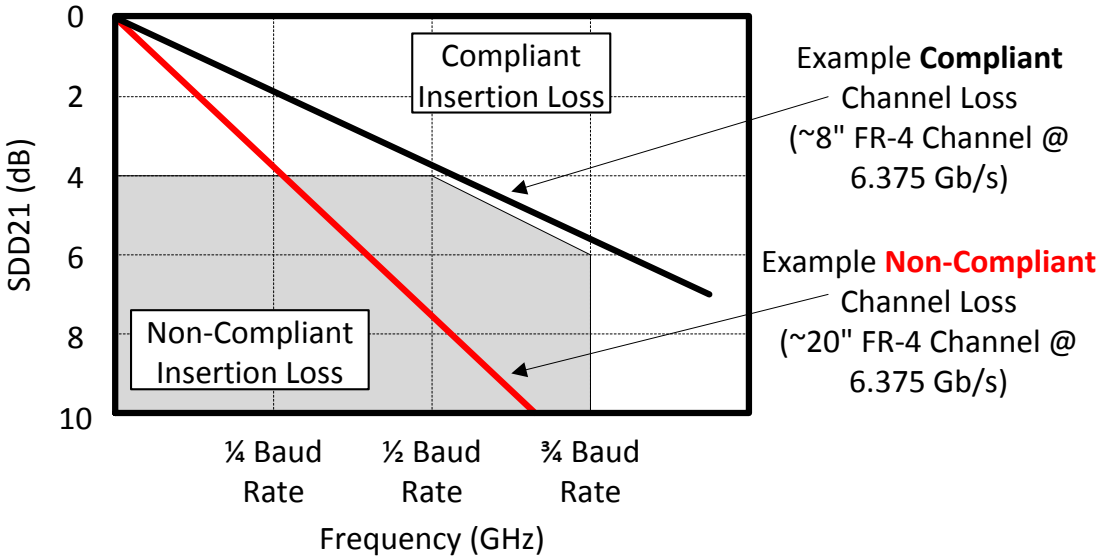
Random jitter plus Deterministic Jitter

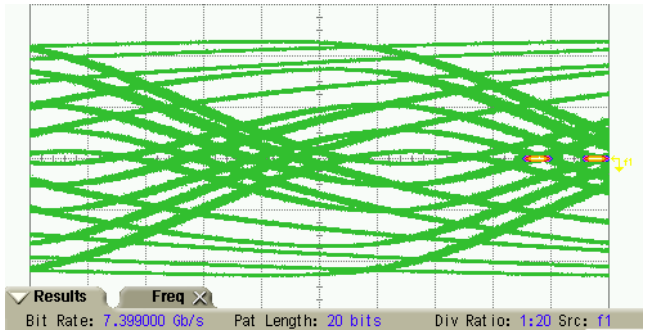
Bit-Error Rate

Solutions for Long/Lossy Channels

- Channel dielectric loss degrades the signal integrity of the signal
- Loss reduces the vertical/horizontal Eye opening and edge rate due to attenuation and inter-symbol interference (ISI)
- Loss Profile mask is specified in the JESD204B standard

JESD204B Acceptable Loss Profile

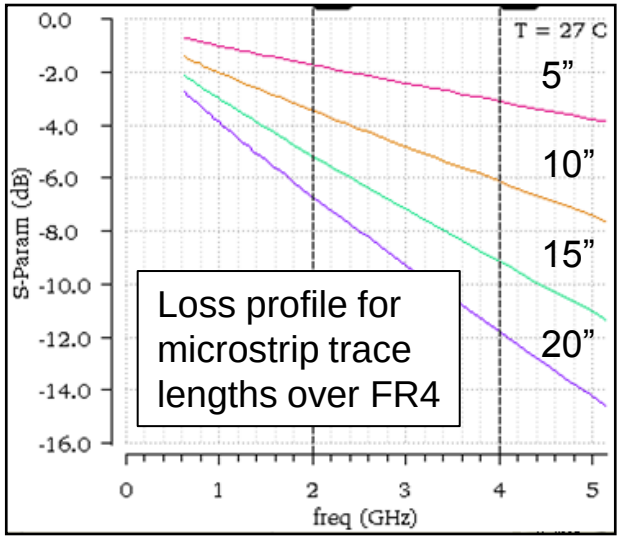


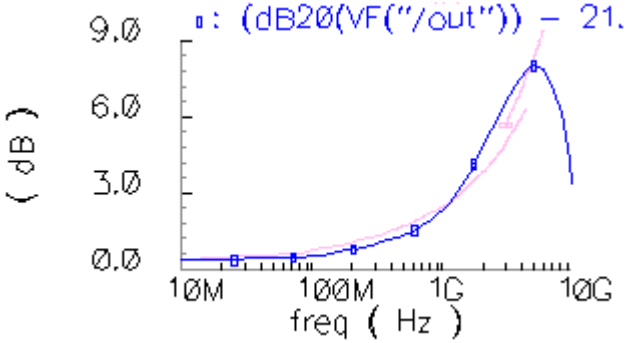


20in. FR4 channel @ 7.4Gb/s

Solutions for Long/Lossy Channels

- Equalization can be used to pulse-shape at TX or pulse-correct RX
- High-pass profile of equalization counteracts low-pass loss profile of channel
- Pre-emphasis
  - AMPLIFY HIGH frequencies to achieve high-pass profile
- De-emphasis
  - ATTENUATE LOW frequencies to achieve high-pass profile
  - May require broadband amplification to meet eye requirements at large de-emphasis

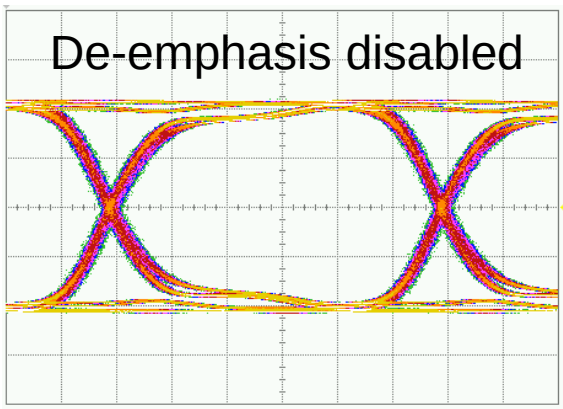


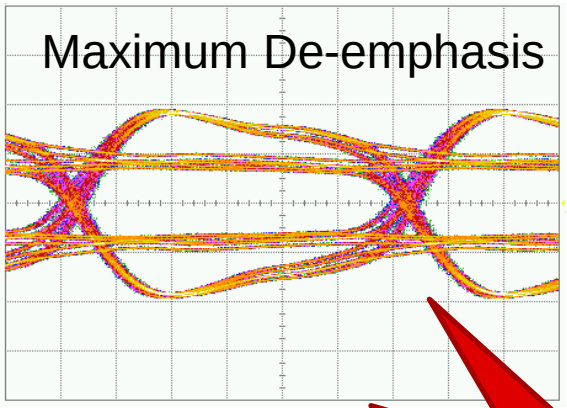


High-pass emphasis profile (blue) matches the inverse of the channel loss profile (pink)

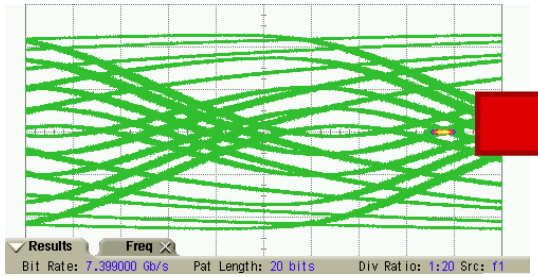
Solutions for Long/Lossy Channels

- **ADC16DX370** De-Emphasis Waveform @ 5 Gb/s at TX output

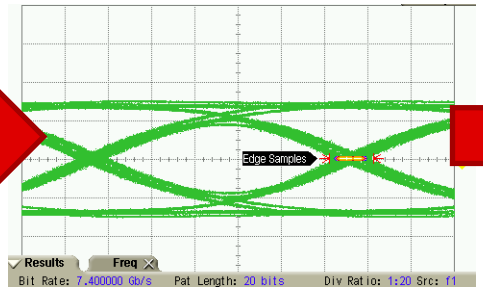




- Waveform @ 7.4 Gb/s at output of 20-inch FR4 channel



De-emphasis disabled



De-emphasis Optimized

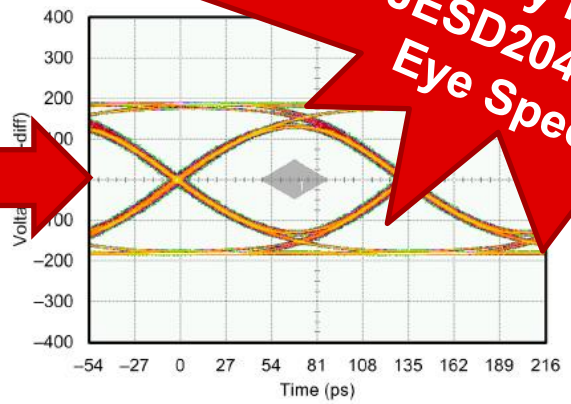
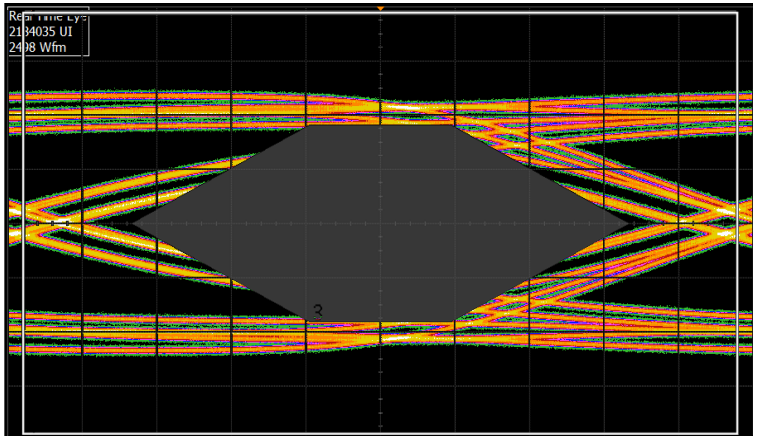


Figure 29. Transmitted Eye at Output of 20-inch, 5-mil. FR4 Microstrip at 7.4 Gb/s With Optimized De-Emphasis

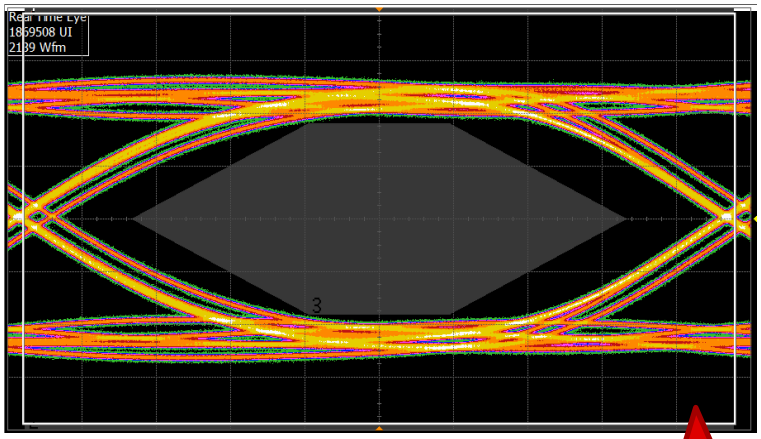
Easily Meets JESD204B RX Eye Spec!!!

Solutions for Long/Lossy Channels

- **ADC12J4000** Pre-Emphasis Waveform @ 7 Gb/s over 7 inches FR4



Pre-emphasis disabled

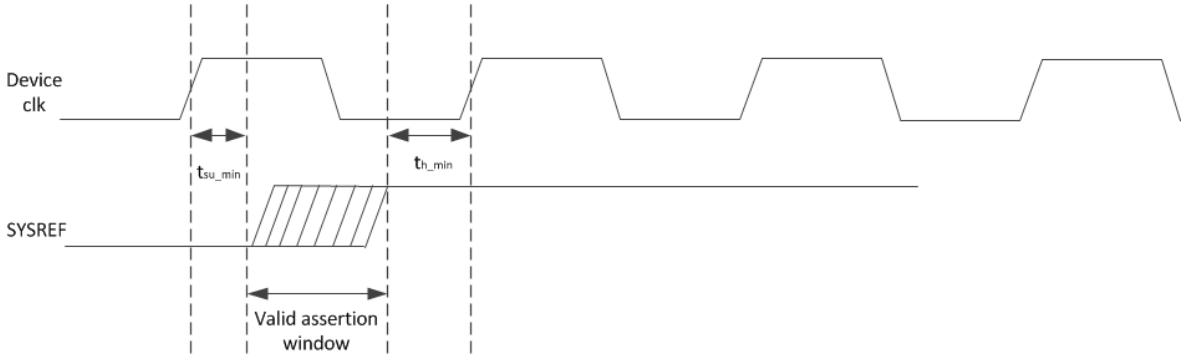


Pre-emphasis Optimized

Even Meets TX Eye Spec!!!

Device Clock and SYSREF Interfaces

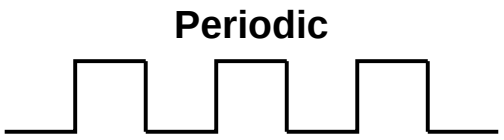
- No strict definition for electrical characteristics
  - LVDS, LVPECL are common solutions
- Device clock frequency may be equal to sampling rate or multiple
- Noise on device clock typically sets jitter performance of converter
- Attention required for DC-coupled common-mode compatibility of TX/RX
- Subclass 1
  - SYSREF must meet setup/hold relative to device clock
  - Electrical characteristics recommended to be consistent between device clock and SYSREF



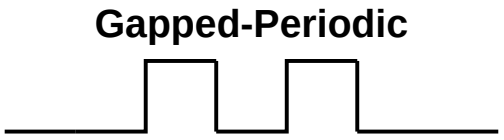
- Subclass 2: SYSREF not required

SYSREF Interface (Signal Types)

- Periodic
  - SYSREF always ON with periodic edges
  - Risk of interferer spurs near IF due to SYSREF



- Gapped-Periodic
  - Send periodic edges for a brief pulse of time
  - No spurs

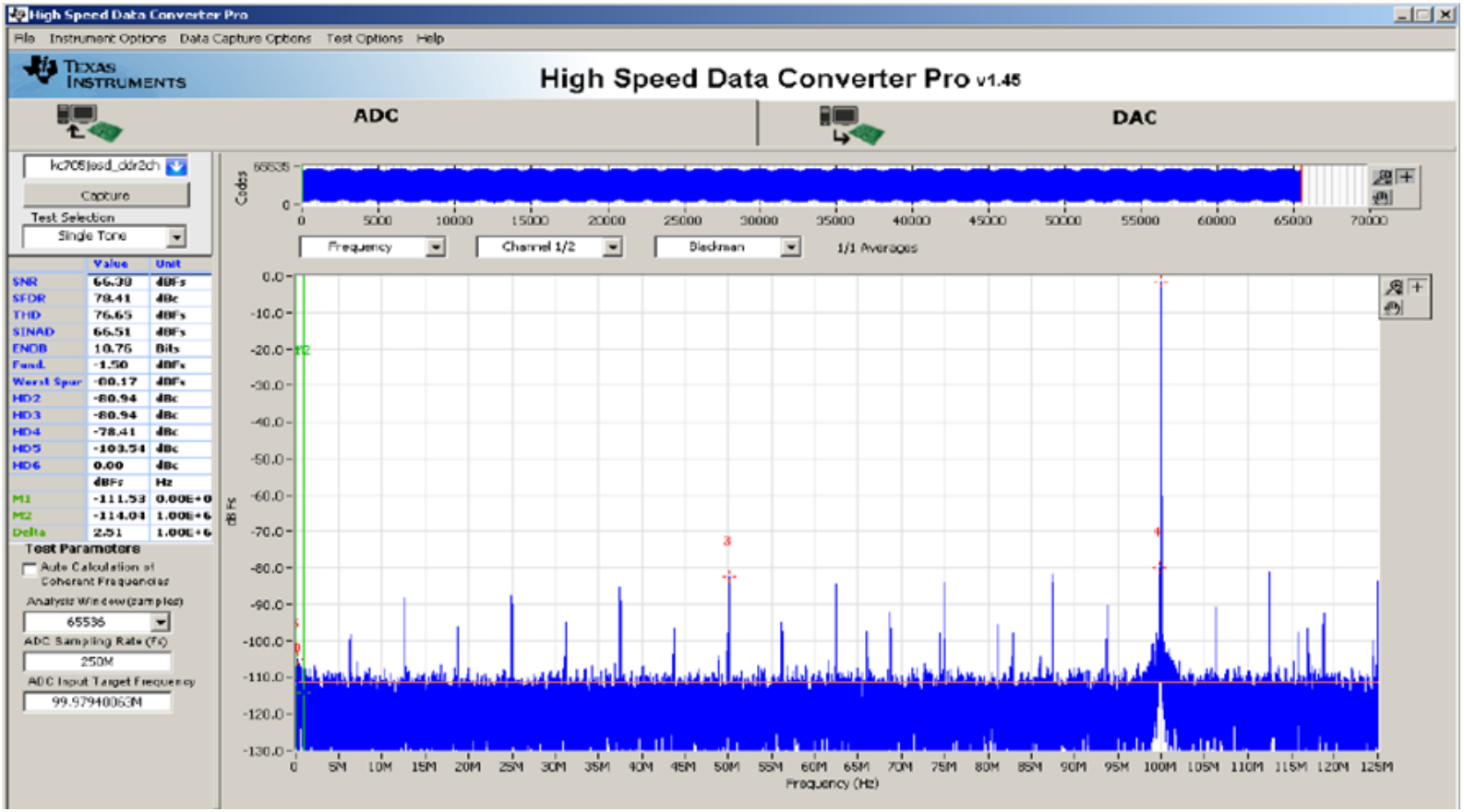


- One-Shot
  - Single SYSREF pulse and then leave in logic-low state
  - No spurs

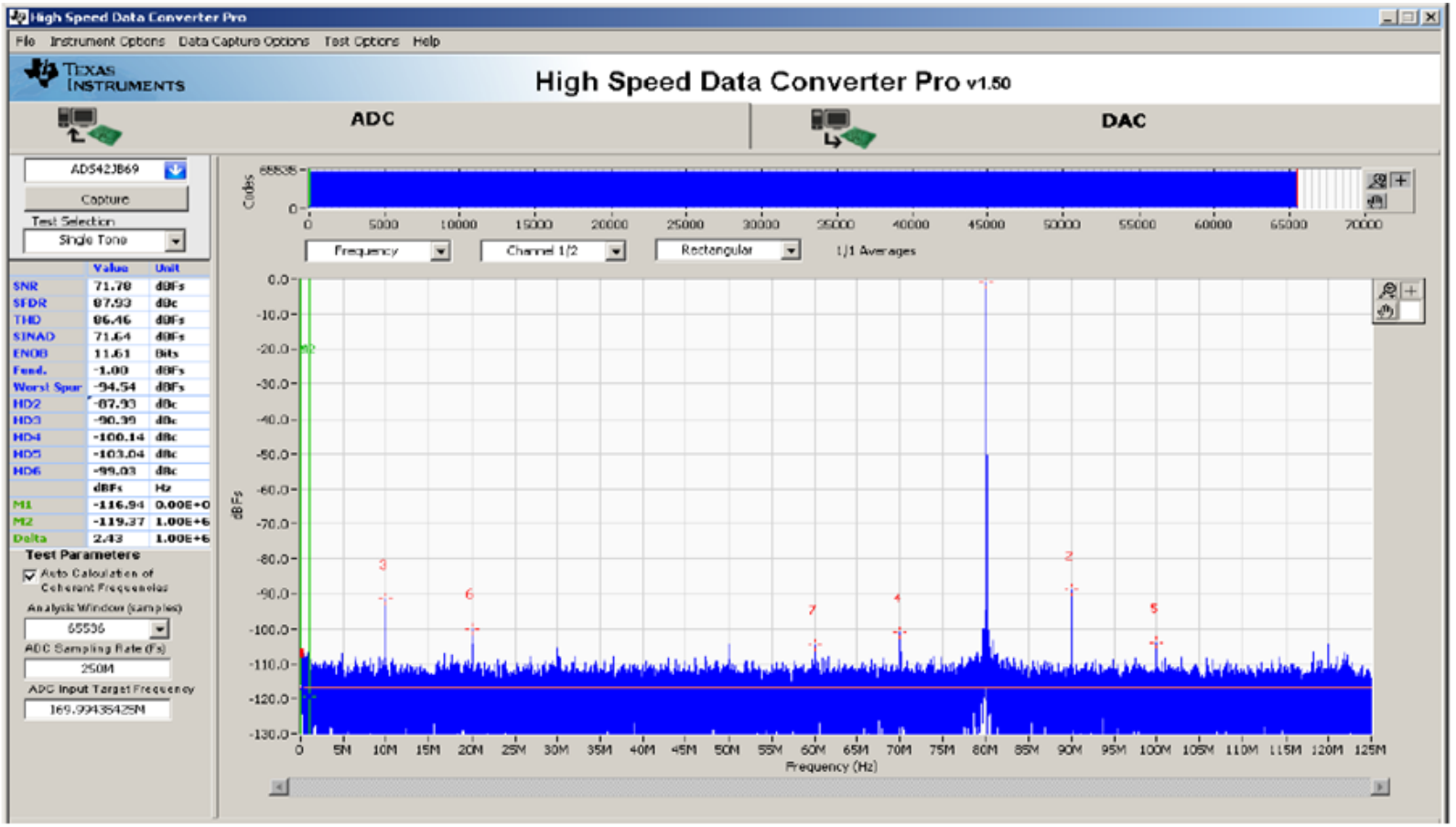
- SYSREF pulse period equal to integer multiple of multi-frame period
- Disabling and gating the SYSREF signal may be employed

TSW1400 Captured Data, SYSREF enabled

- Periodic SYSREF has sub-harmonic relationship to ADC sampling clock



TSW1400 Captured Data, SYSREF disabled



SYNC~ Interface

- No strict definition for electrical characteristics
  - LVDS, LVPECL, CMOS are common solutions
- DC coupling mandatory
- Subclass 1
  - SYNC~ does not have strict timing
- Subclass 2
  - SYNC~ must meet setup/hold relative to device clock
  - Timing requirements very difficult to meet for device clock rates > 250MHz

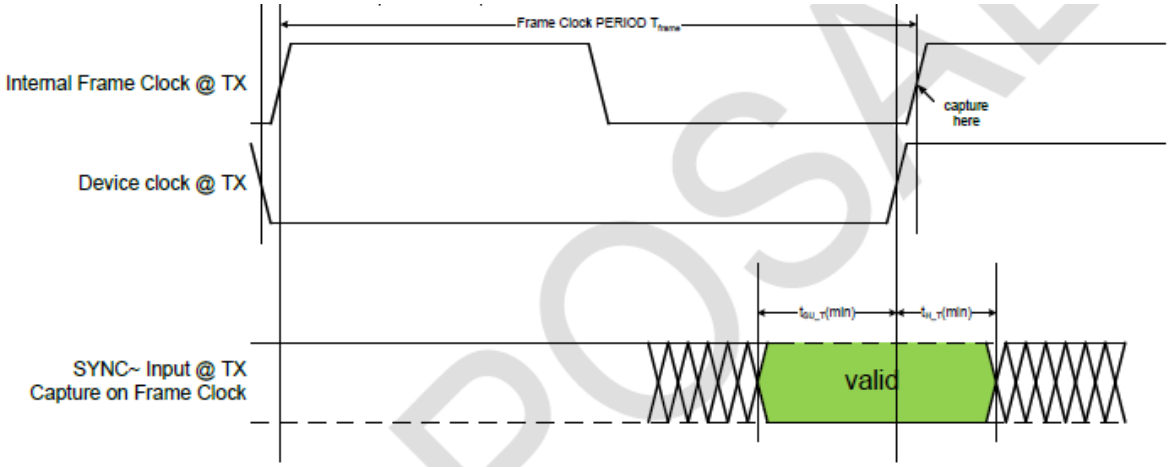
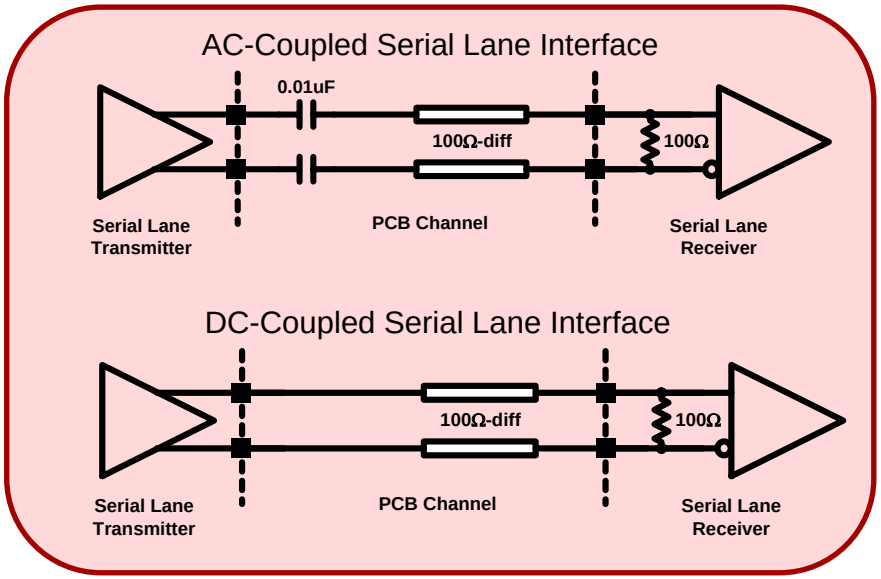


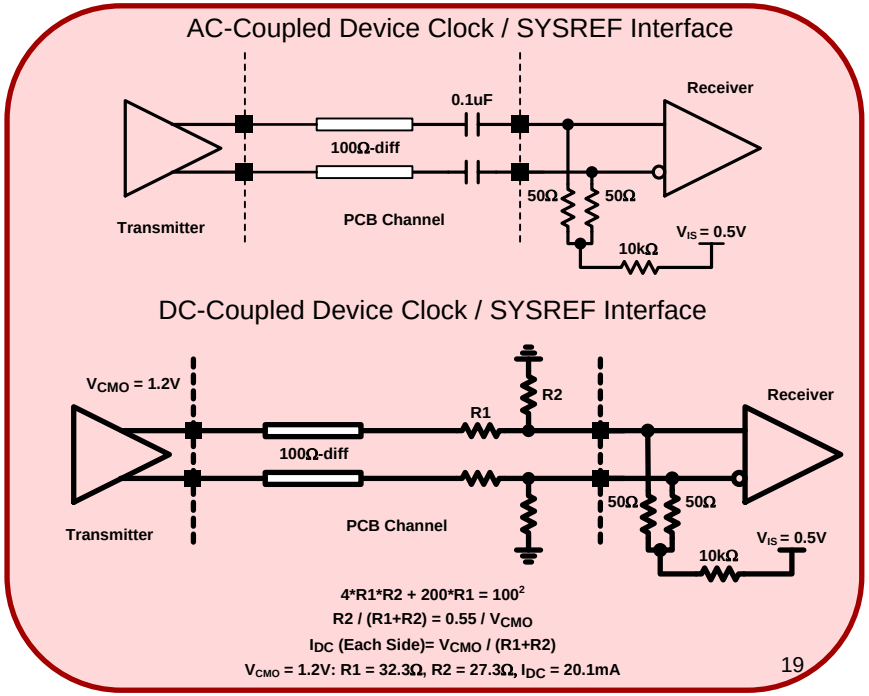
Figure 11 - SYNC~ signal timing for Subclass 0 and Subclass 2 Devices

Differential Interfaces (Example circuits)

- Serial Lane Interface
  - AC or DC Coupling
  - 100Ω differential channel
  - Routing signal integrity is MOST critical of all JESD204B interface signals

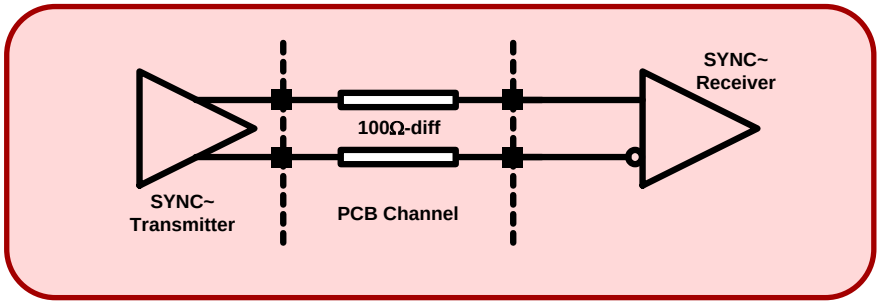
- Device Clock / SYSREF Interface
  - AC or DC Coupling
  - AC coupling SYSREF requires provision for DC balancing at receiver
  - 100Ω differential channel
  - Match device clock and SYSREF interface to meet setup/hold requirement





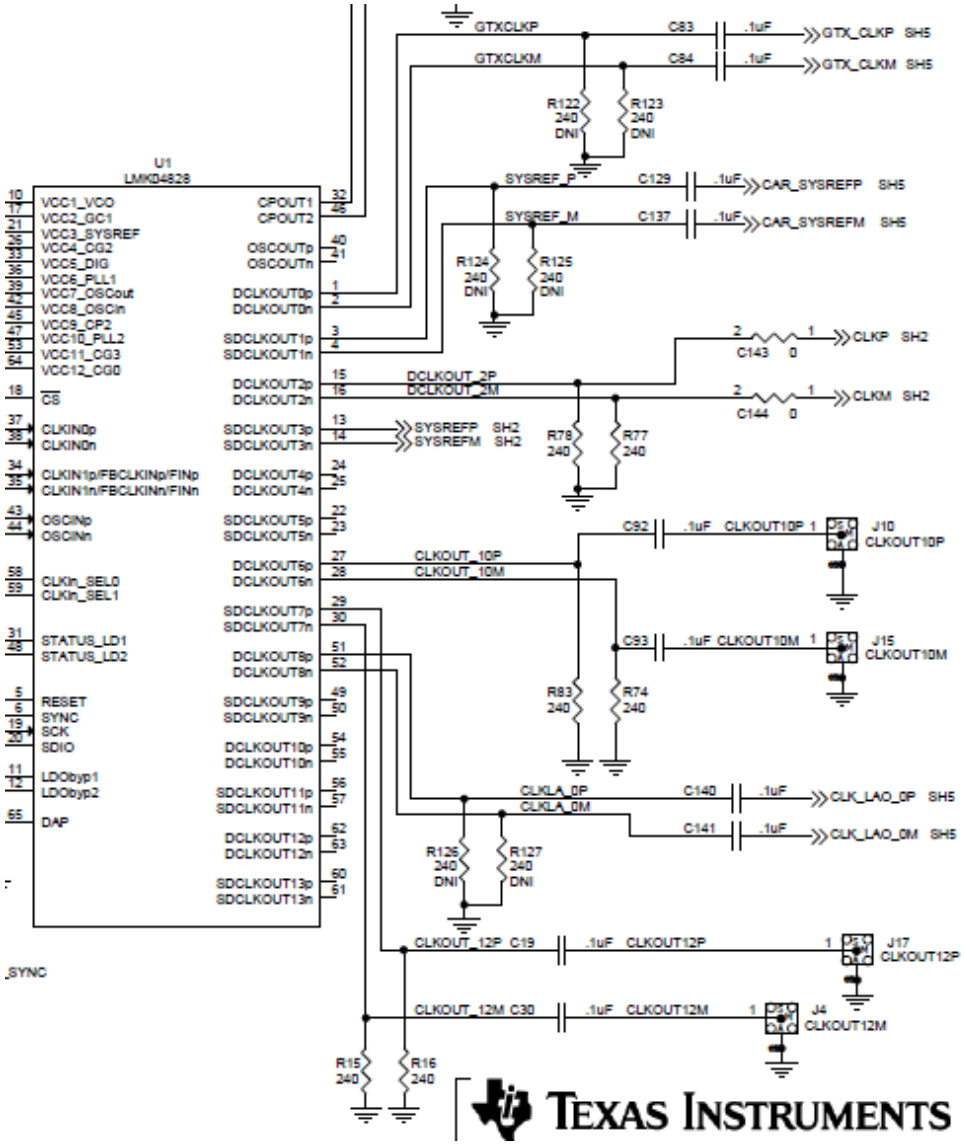
Differential Interfaces (Example Circuits)

- SYNC~ Interface
  - DC Coupling only
  - 100Ω differential channel
  - Routing VERY critical for subclass 2
  - Routing is LEAST critical for subclass 1



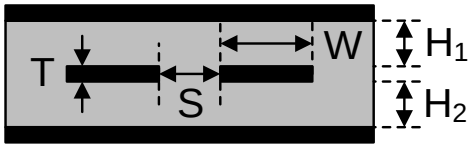
Generating Device Clocks and SYSREF

- Example: LMK04828
  - Subclass 1 capable
  - 7 Device CLK / SYSREF pairs
  - Low Jitter clock source
  - SYSREF Disable feature
  - Delay options
  - LVPECL, LVDS, HSDS outputs
  - Supports Clock Distribution mode using external clock source

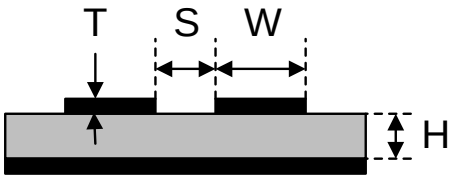


PCB Recommendations (Differential Pairs)

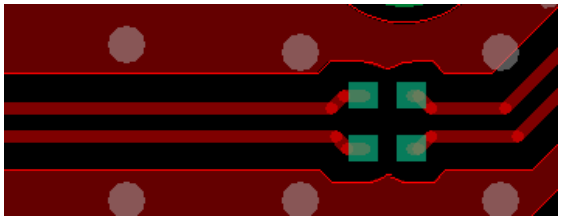
- Route differential signal as *tightly coupled* microstrip or stripline lanes (S<=W)
- 100 Ω differential impedance
- Avoid 90° turns
  - Reduces +/- trace mismatch
  - Reduces impedance discontinuity
- Recommend 0201 series components (AC coupling) to minimize impedance discontinuity of pads
- Routing on inner layers (stripline) has advantages:
  - Better impedance control
  - No speed issues with Nickel plating
  - Less interference/emissions



Differential Stripline



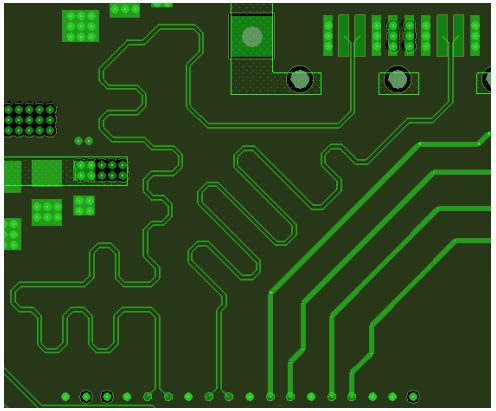
Differential Microstrip


0201 AC coupling capacitors

Via stitching

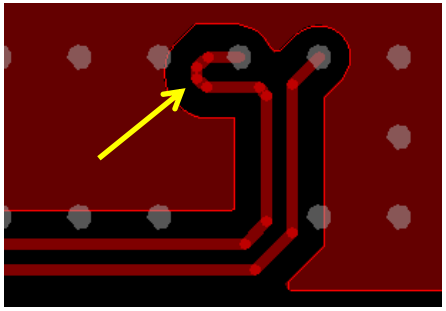
PCB Recommendations (Trace Matching)

- Device Clock, SYSREF, SYNC~, and serial lanes must be between matched +/- traces
- Device Clock and SYSREF pairs must be matched to each other
- Serial lanes need NOT match to each other
- Use wiggles to match the lengths of multiple differential pairs.
  - Keep radius of the wiggle > 3 times trace width
  - Use equal number of turns in each direction
- Use small jog-outs to correct +/- trace mismatch



Matched Dev. Clock and SYSREF pairs

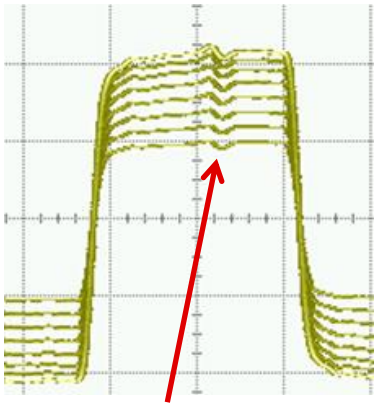
R > 3xW



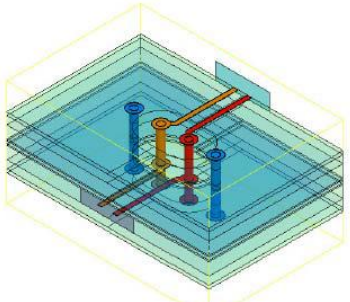
Jog-out matches +/- traces

PCB Recommendations (Vias)

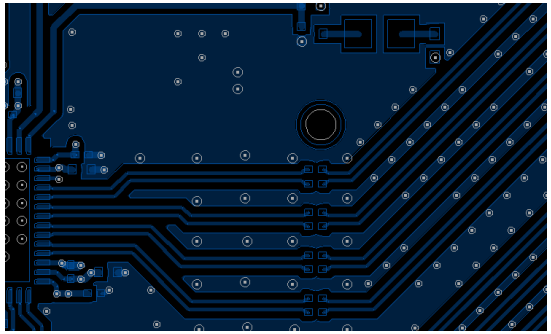
- Vias in the signal path create impedance discontinuities that result in signal reflections/degradation
- Simulate signal path with vias to determine signal integrity before manufacturing
- Avoid changing layers where possible, but use adjacent grounding vias where layer change is necessary to provide return current path
- Via stitch along sensitive differential signal paths
- Use blind vias or back-drilling to eliminate via stubs



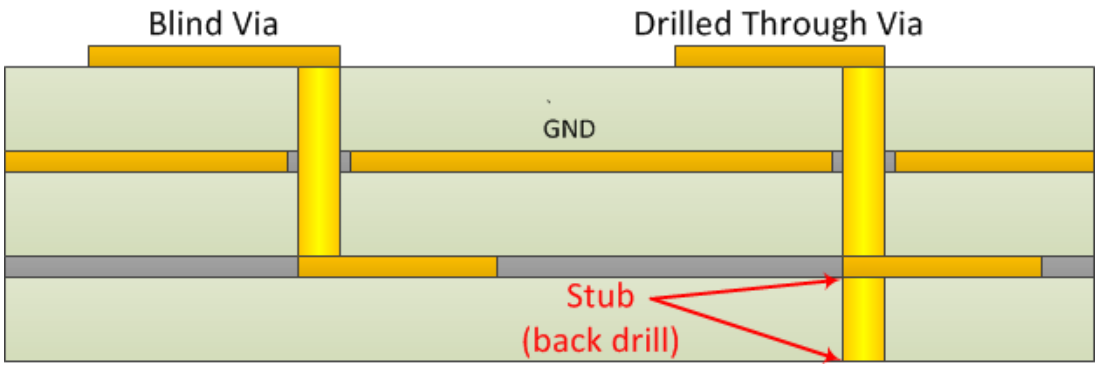
Waveform “blip” due to via in the signal path



Adjacent GND vias

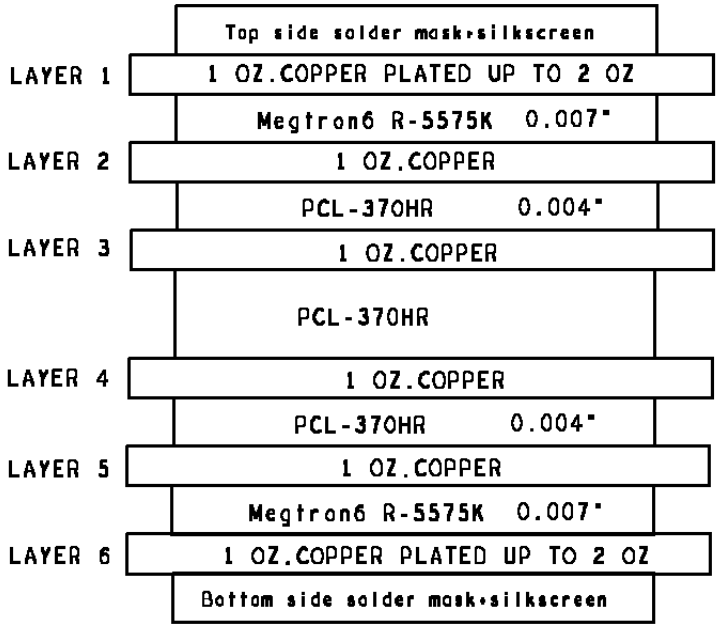


Via stitching



PCB Recommendations (Material/Stack-Up)

- Serial lane speeds **>** 3 Gb/s at length **>** 8”
  - Recommend low-loss, good impedance consistency dielectric material
  - Rogers-4350, Megtron-6.
  - Use premium dielectric only where needed
- Serial lane speeds **<** 3 Gb/s at length **<** 8”
  - Recommend low cost materials
  - FR4, 370HR
- Board shop reports that 370HR can be used up to 10 GHz with very short traces (1-3 inches)



Material	QTY	$/board
Megtron 6	50	$660
370HR	50	$350

PCB Recommendations (Reference Planes)

- Use a ground planes as the signal reference on adjacent layers
- Avoid splits in the reference plane underneath signals when possible
  - Return current for high-speed signals follows trace on the reference plane
  - Splits require the return current to travel around, increasing loop inductance, coupling, and interference
- When reference plane splits under differential signals are necessary:
  - Minimize split width
  - Ensure tight coupling of differential pair
  - Jump split at 90°
  - Good GND via stitching along channel
  - Avoid jumping split in vicinity of other noisy signals

PCB Recommendations (Reference Planes)

- Keep analog signals separate from digital signals
  - Single ground plane is recommended
  1. Split ground plane at DAC/ADC into analog and digital planes
  2. Route the signal traces in their respective domains
  3. Recombine the two ground planes into one after routing

PHY Debug (Test Patterns)

- Test patterns can verify the PHY layer signal integrity

Pattern	Use Test
PRBS7 /15 /23 /31	Long pattern performance Deterministic Jitter (ISI)
01010101010 (D21.5)	Random Noise

- PRBS and D21.5 patterns available on all TI JESD204B devices
- Most FPGA giga-bit transceivers have built-in PRBS generators/detectors

Handling Link Errors

Error Type	Effect on Serial Stream	Link Error Detection	Link Response
Jitter/ISI Single bit error	Single bit error	8b/10b decoding fails (not-in-table error)	- Output previous good frame - SYNC asserted for 2 frames
Jitter/ISI Multi-bit error	Multi-bit error, possibly across many frames	- Not-in-table error - Disparity error - Control Char error - Frame alignment error	- Depends on specific error - SYNC asserted >= 2 frames - Link re-initialization likely*
ADC Core Sample Error	None. Erroneous sample is encoded, transmitted, received as usual.	No error detected	No change

- The list of errors which require link re-initialization is implementation specific

TI Devices SERDES Summary

Device	Max Conversion Rate	Max Bit Rate	Min #Lane/Ch. (at full MSPS)	Emphasis / Equalization?
ADC16DX370	370 MSPS	7.4 Gb/s	1	TX De-emphasis
ADS42JB69	250 MSPS	3.125 Gb/s	2	Not needed
ADS42JB46	160 MSPS	3.125 Gb/s	1	Not needed
ADC3K Family (Preview)	160 MSPS	3.125 Gb/s	1	Not needed
ADC12J4000	4000 MSPS	8 Gb/s	*	TX Pre-Emphasis
ADC12J2700	2700 MSPS	10 Gb/s	*	TX Pre-Emphasis
DAC38J84	2500 MSPS	12.5 Gb/s	0.25	RX Adaptive Equalizer

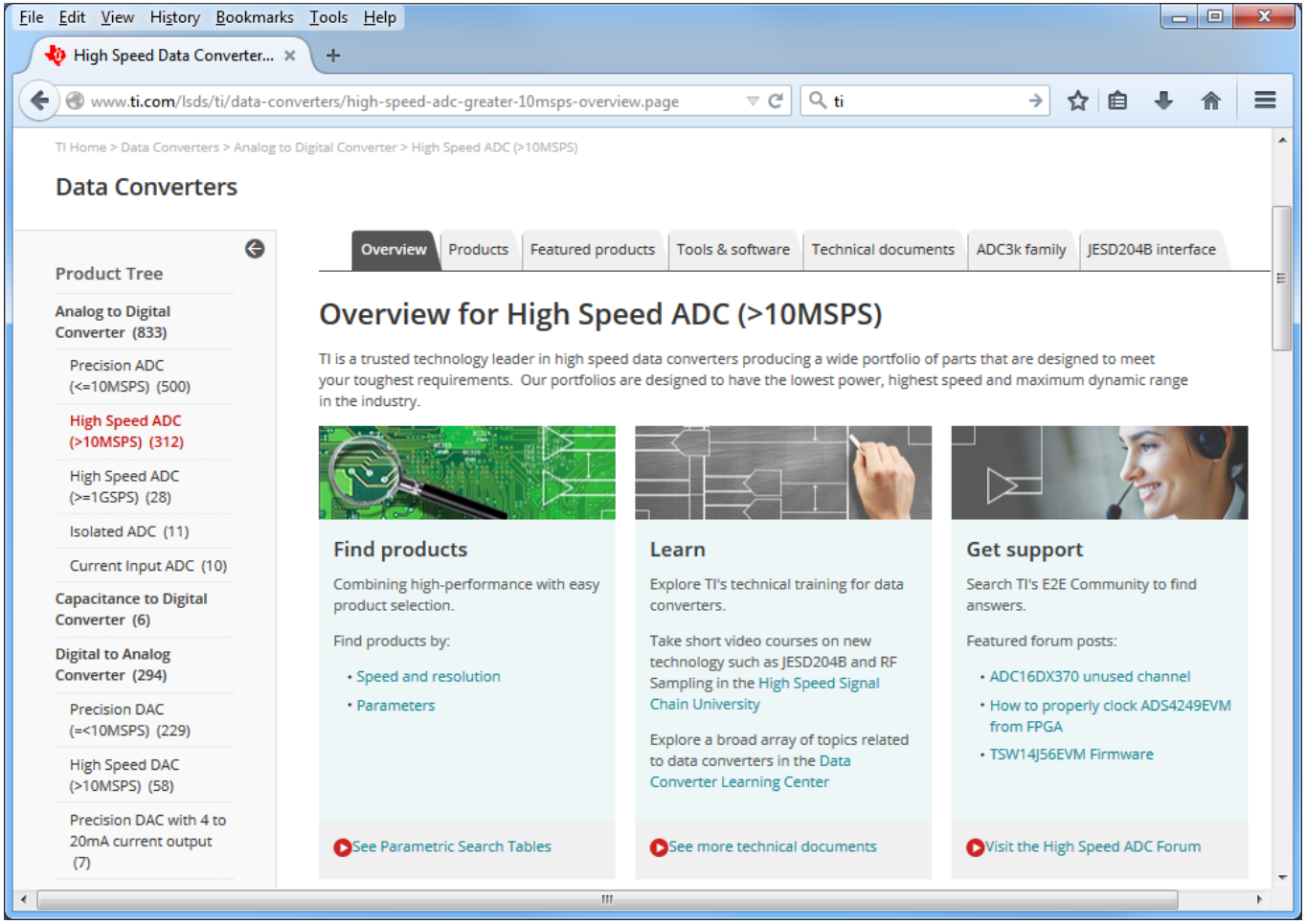
*Decimation Factor Dependent

Summary

- The Physical Layer refers to the electrical and timing characteristics of the TX and RX and their ability to send and recover data
- Equalization and (pre-/de-) emphasis can be used to enhance signal integrity of the link for longer lengths and higher bit rates
- Device Clock, SYSREF, and SYNCb interfaces and not strictly defined in the standard, but common guidelines are provided
- Very high speed layout techniques for the serial lanes are critical to ensure impedance matching and minimization of signal reflections
- Test patterns such as D21.5 and PRBS usually patterns are available for physical layer debug

More Educational Resources

www.ti.com/lsds/ti/data-converters/high-speed-adc-greater-10msps-jesd204b.page



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