Webinar

Today's solution for tomorrow's energy conversion systems

Olivier Monnier

Product marketing director, C2000 MCU portfolio

Agenda

- C2000™ real-time Microcontrollers portfolio
- New F28P65x and targeted applications
- F28P65x block diagram and new features
  - Analog
  - CPU
  - PWM
  - Communication
- Applications examples
- Getting started

C2000 MCUs | leading the way to energy efficiency

MOTOR DRIVES & APPLIANCE

SOLAR & EV CHARGING

POWER DELIVERY

TEST & MEASUREMENT

HEV, EV & POWERTRAIN SYSTEMS

BODY ELECTRONICS AND LIGHTING

C2000™ real-time microcontrollers | overview

Scalable, ultra-low latency, real-time controller platform designed for efficiency in power electronics, such as high power density, high switching frequencies, GaN and SiC technologies

C2000 Real-Time MCU

Highly accurate sensing:

- 12-/16-bit ADCs, up to 24 channels
- Full analog comparators with built-in DACs
- Quadrature Encoder and Capture Logic

Sense

Process

High performance processing:

Floating-point DSP C28x™ core + parallel multi-core architecture + instructions set optimized for control math, up to 925 MIPS

Highly flexible, High-resolution PWMs:

- Up to 32 outputs
- Tightly coupled with Sensing domain for fast response time
- Buffered Output DACs

Control

Interface

Integrated communications:

CAN, CAN-FD, LIN, UART, SPI, I2C, PMBus, USB, 10/100 Ethernet MAC, EtherCAT®, XEMIF

Expertise and support:

Software libraries, reference designs, and functional safety-compliant devices.

25 years expertise in real-time control systems

Leading innovation:

Configurable Logic Block for peripheral customization, Fast Serial Interface for high-speed communication, ERAD for enhanced diagnostics and profiling

Functional Safety:

All Safety integrity levels for Automotive and Industrial

Functional Safety Compliant

Functional Safety Support

Built-in HW features for safety

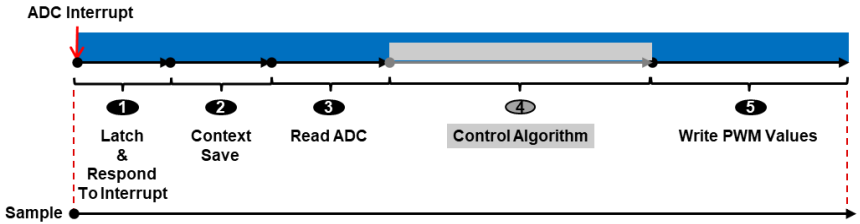
SW library and device drivers

Safety certification documentation

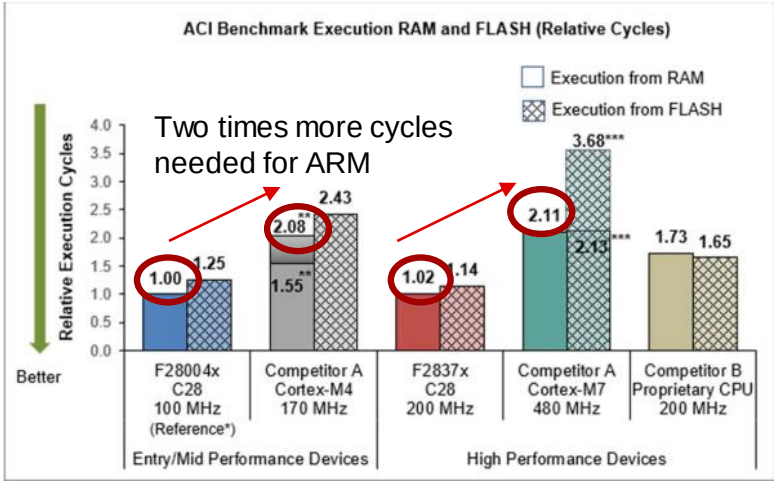
1.2-V core, 3.3-V I/O design | Up to 1.5 MB Flash, 256 kB RAM (ECC protected) | QFN, QFP, BGA package | -40 to 125C temperature range | Q100 automotive qualified options

Over 1 billion units shipped for industrial and automotive applications with compatible software

C2000 | Designed with real-time algorithms in mind



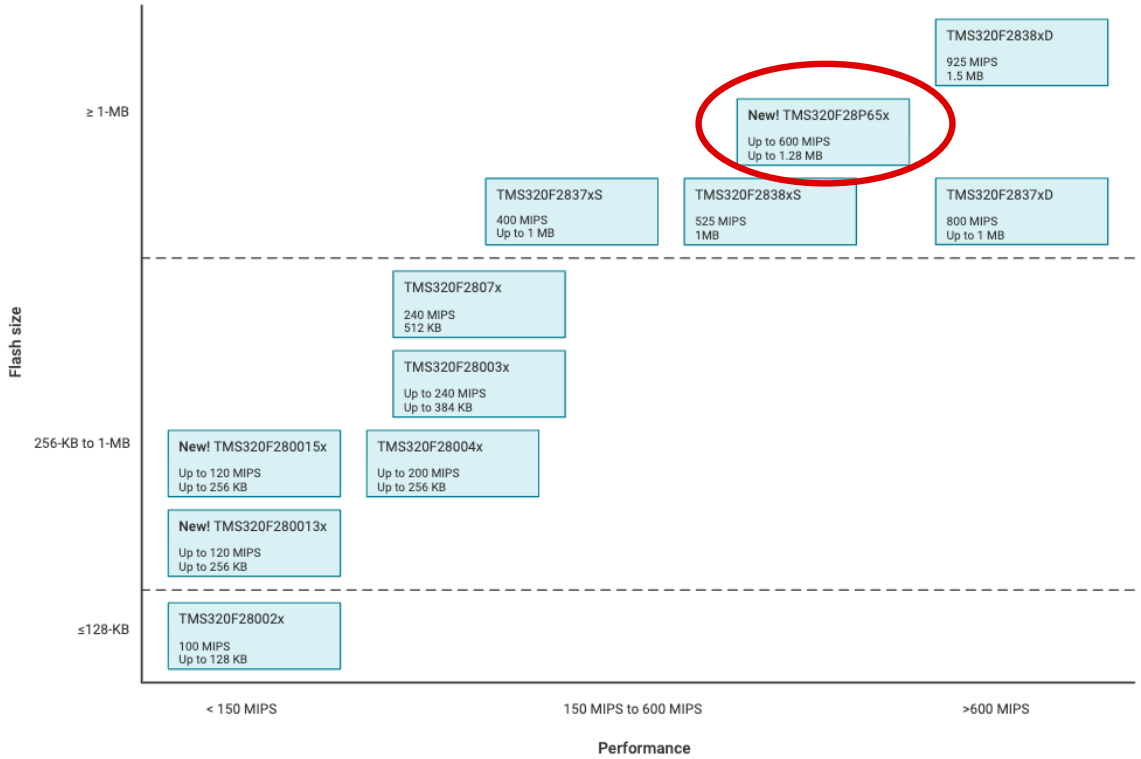
- Real-time is defined by the **latency** between the **Sample** and **output**
- Latency = time spent for Sensing + Processing + Control [1 to 5]
- C2000 did perform real-time application benchmarks (example: ACI – 3-phase electrical motors)



Number of cycles per function	F28004x (100MHz)	ARM M7 based device	Equivalent ARM M7 MHz (eMHZ) to achieve the same latency
Single PID	39	64	196 MHz
Dual PID	88	108	150 MHz
SV Gen	66	85	154 MHz
PARK + iPARK	26	50	230 MHz
Full ACI benchmark	**529**	**1100**	**200 MHz**

- **In order to achieve the same latency [ADC/CPU/PWM] (1 to 5),** a Cortex-M7 based device needs to run at 200MHz compared to a F28004x running at 100MHz (*200MHz equivalent M7 MHz (eMHZ)*)
- *C28x core: 2x times better then Cortex M7*
- *CLA core: 40% better than Cortex M7*

New F28P65x | PWM and Analog innovation, system cost reduction



Key points

- Up to 40 16/12-bit ADC channels
- New ADC HW oversampling feature
- 36 High Resolution (150ps) ePWM enabling advanced switching techniques, complex topologies & protection mechanisms for increased efficiency and power density
- Highly connected with ECAT, CAN-FD, USB, EMIF, CLB, FSI options
- Smallest real-time MCU with integrated EtherCat in a 9x9mm package
- Easier safety implementation with periodic HWBIST, ECC/ parity, CPU lock-step core
- Available in industrial and automotive qual
- 1KU price starting at $5.85 USD

Entry level to high-end software compatible, scalable platform

	28 VSSOP	32 QFN	48 QFN	48 QFP	56 QFN	64 QFP	80 QFP	100 QFP	169 BGA	176 QFP	256 BGA	337 BGA
1.5MB										F2838x		F2838x
1.28MB								F28P65x	F28P65x	F28P65x	F28P65x	
1MB								F2837x		F2838x F2837x		F2838x F2837x
768KB								F28P65x F28P65x	F28P65x F28P65x	F28P65x F28P65x	F28P65x F28P65x	
512kB								F2837x F2807x		F2837x F2807x		F2837x
384kB						F28003x	F28003x	F28003x				
				F28003x	F28004x	F28004x F28003x	F28003x	F28004x F28003x				
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64kB		F280015x F280013x	F280013x	F28002x F280015x F280013x		F28002x F280013x	F28002x					
32kB				F28002x								

Production

Sampling

F28P65x real-time control applications

Robotics

- Robot Servo Drive
- Robot sensing module
- Robot Comm Module
- AGV/ AMR Robots
- Encoders and Advanced Sensing
- Surgical Robots

Industrial Power

- Solar (String inverter)
- Energy storage systems
- EV charging Station
- UPS

Industrial Motor

- Single Axis Servo Drives (w and w/o FPGA, w and w/o Ethercat
- Dual Axis Servo Drives
- Single/ dual axis stepper closed loop

Automotive

- OBC + DC/DC single chip solution (11kW)
- High end HVAC pump
- High end Lighting

F28P65x | PWM and Analog innovation, system cost reduction

Analog

-3 x 12-bit or 16-bit ADC up to 3.5 MSPS

-Up to 40 ADC channels available

-HW post processing

-New HW ADC oversampling mechanism for better control and 54% improvement on code size and cycles

-11 comparators: protect more signals at the same time, Support for dual ramp generation (easier implementation of hysteretic, peak current mode control with lower latency) and more

Signal capture & generation:

-16x SDFM to support up to 3 axis

-6x Quadrature encoder interface;

-7x capture modules with 2 High Res

-Embedded pattern generator (EPG)

-6 Tiles CLB for encoder implementation, PWM protection, FPGA/ CPLD removal

Memory:

-248kB RAM with Parity

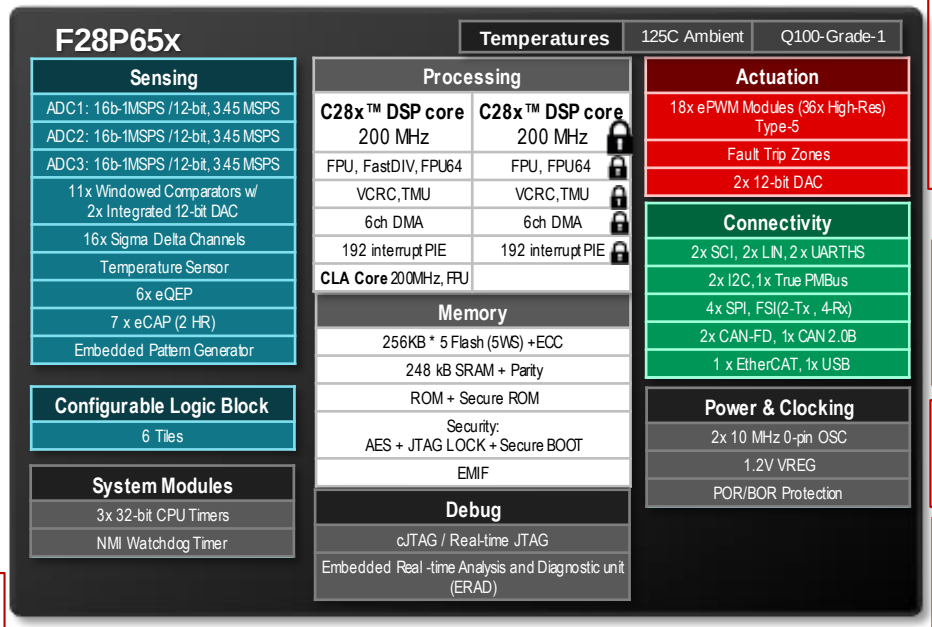
-1.25 MB Flash (ECC)

-Multi-bank support with banks allocable to either CPU statically optimizing mem usage and for easier Live Firmware Upgrade

Real-time Processing Performance:

2x 200 MHz F28x DSP core + FPU64 + TMU + 1x 200 MHz CLA CPU

Option for lock-step core, increased RAM support for CLA (64kB)



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100-pin LQFP/ 0.5mmp/ 16x16mm and 176-pin LQFP/ 0.5mmp/ 26x26mm

Actuation

-36 high resolution PWM channels

-Type 5 PWM support, Multi-threshold compare, PWM HW sync., diode emulation mode, Minimum Deadband, Illegal combo logic support, digital compare edge detection, Muti-compare operation within one period

-PWMs designed for future of power electronics with Matrix Converters, Multi Level Converters, Dual Active Bridge and Resonant Converters.

Connectivity

EtherCAT , CAN-FD, CAN, USB, 200 Mbps FSI, multiple serial ports, 25Mbps Hi-speed UART with DAM , EMIF, many I/Os and AGPIO

Security

Dual-zone code security, unique ID, secure boot, JTAG lock, HW AES

Safety (ASIL-B/ SIL-2)

Easier implementation with Reciprocal comparison, lock-step core, Periodic HWBIST, 2 DCSM zones, RAM with Parity, Flash all ECC, 2*APLL, BOR, Redundant interrupt vector RAM, better PWM safety with Minimum Deadband , Illegal combo logic support and digital edge detection

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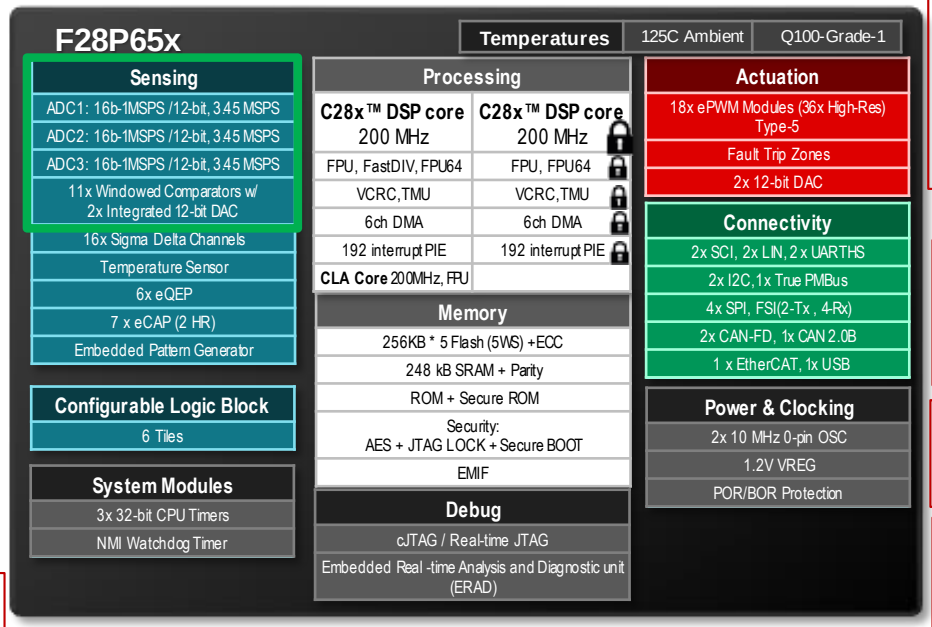

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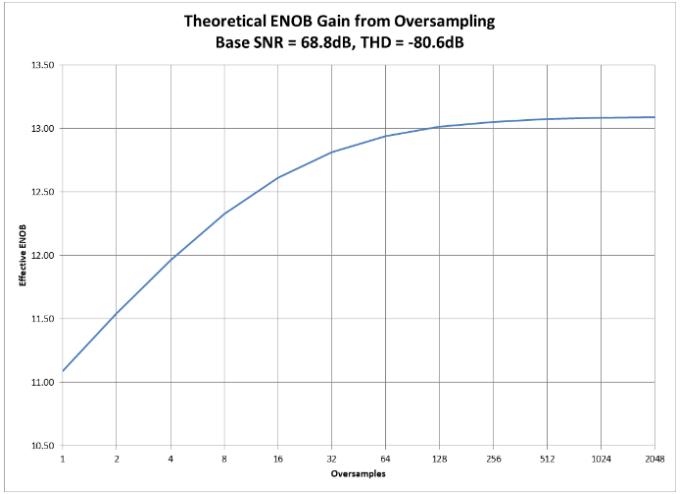
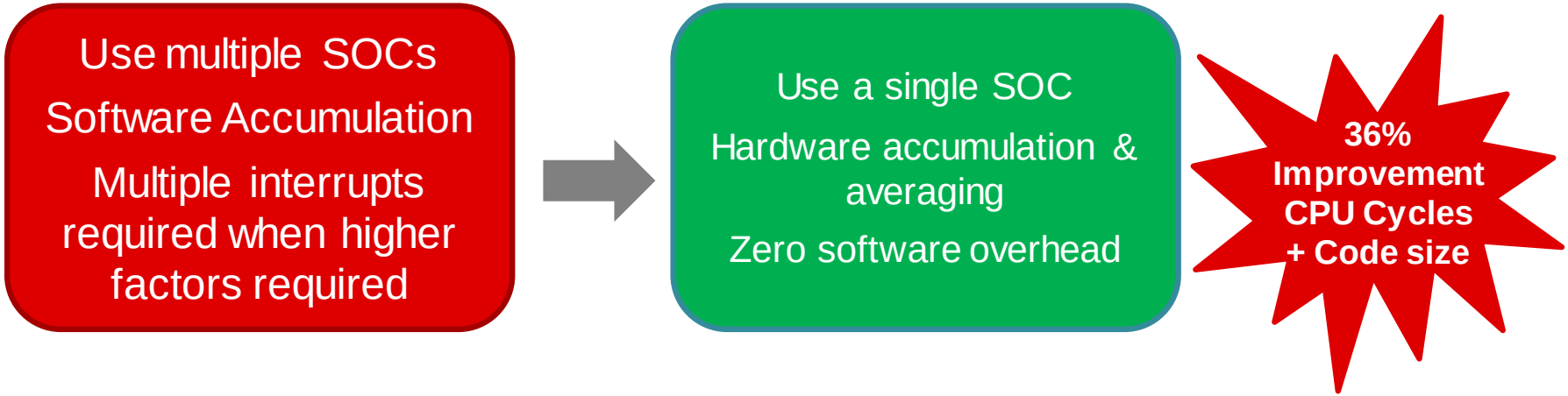
Oversampling overview

- Oversampling is a technique used to achieve higher effective number of bits (ENOB) than the base hardware provides, by performing multiple samples of the same signal back-to-back.
- Software oversampling requires use of redundant SOCs and post-conversion CPU processing to accumulate results
- The **new ADC** introduces a very flexible **hardware oversampling**
  - Up to 128x oversampling
  - Variable frequency oversampling
  - Period averaging
  - Undersampling/ trigger decimation
  - Precise trigger positioning
  - Trigger spread, multi-ADC interleaving



Hardware oversampling | Performance benefits



4x oversampling example (single channel)

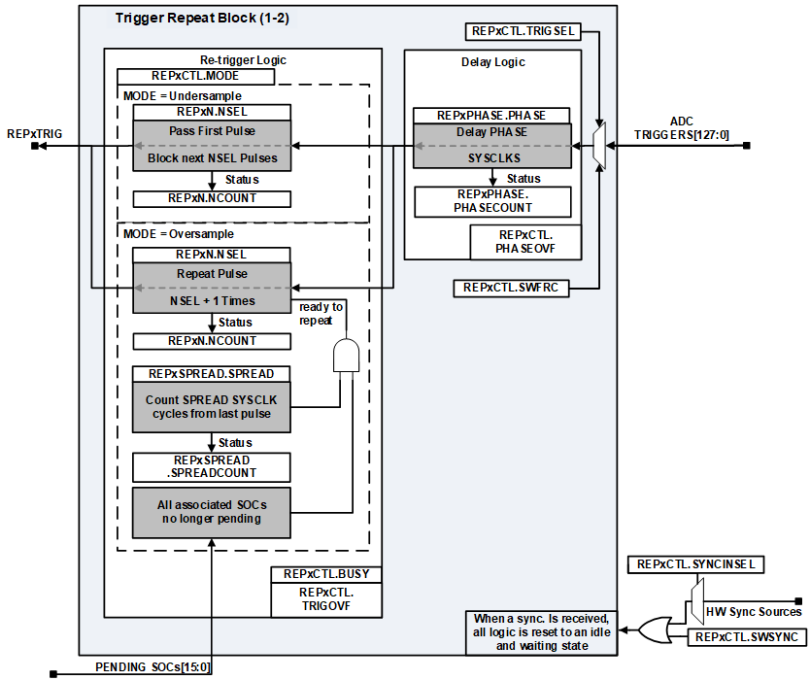
Existing: 605 cycles | **with New Method: 387 cycles**

ADC hardware oversampling

Oversampling can be used for noise rejection, increasing ENOB beyond the base capability of the ADC.

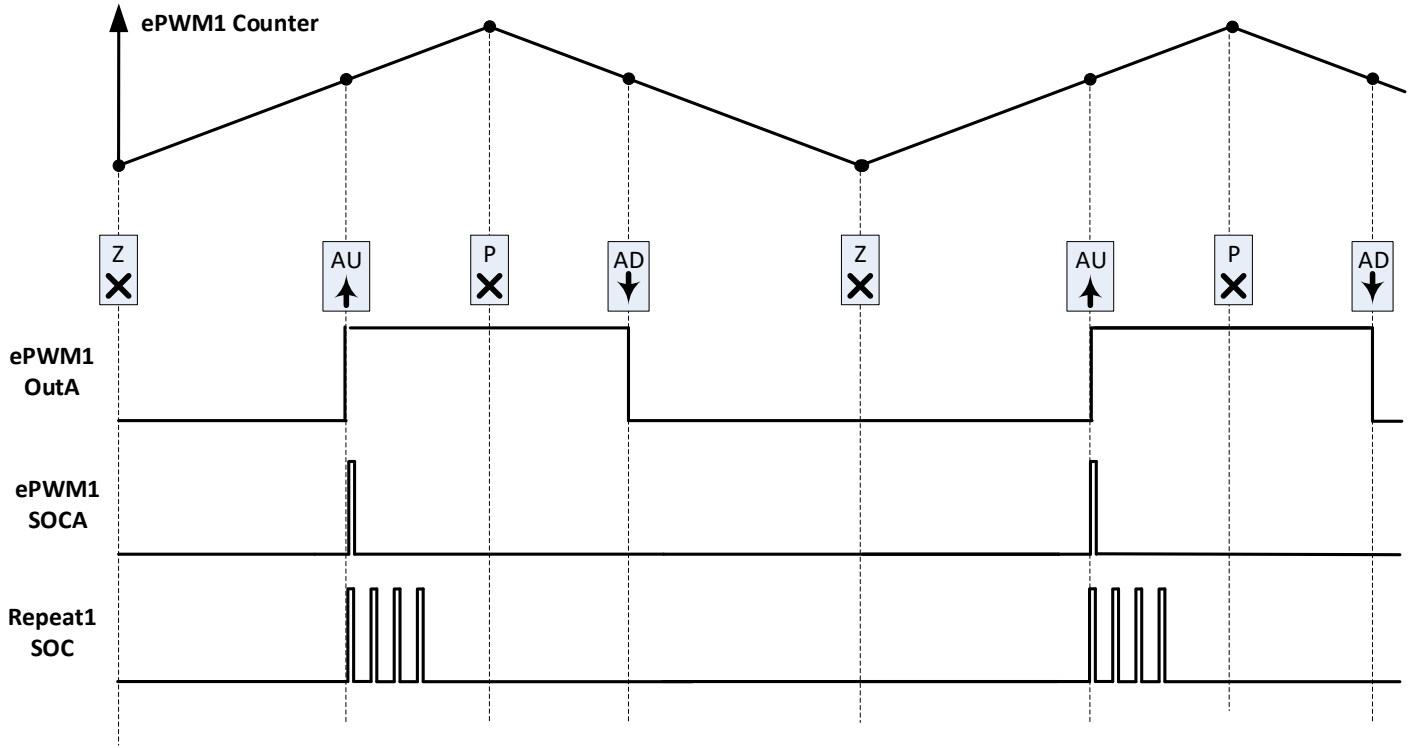
New ADC (Type 4) adds the following features to enable oversampling

- **Trigger repeater**: Generate up to 128 samples from a single trigger
- **Configurable trigger spread**: Add delays between retriggered samples if desired
- **Post Processing Block**
  - 24-bit hardware accumulator to automatically sum oversampled conversions
  - Shift function for averaging
  - Dedicated oversampling interrupt signal
  - Max/min sample calculation in hardware for outlier rejection
- **Shadow register** updates to reconfigure trigger repeater while current source trigger is still processing conversions.



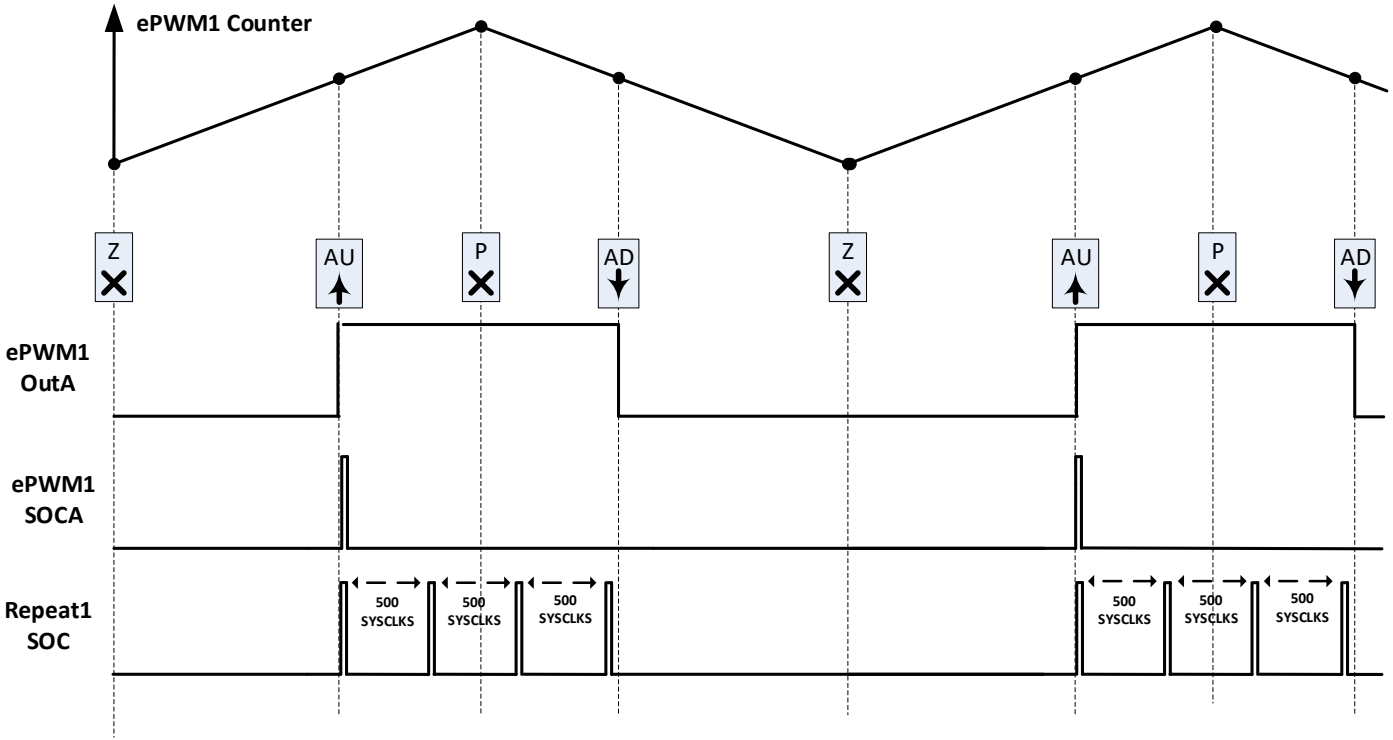
** ADC Post-Processing Block*

Oversampling | Example



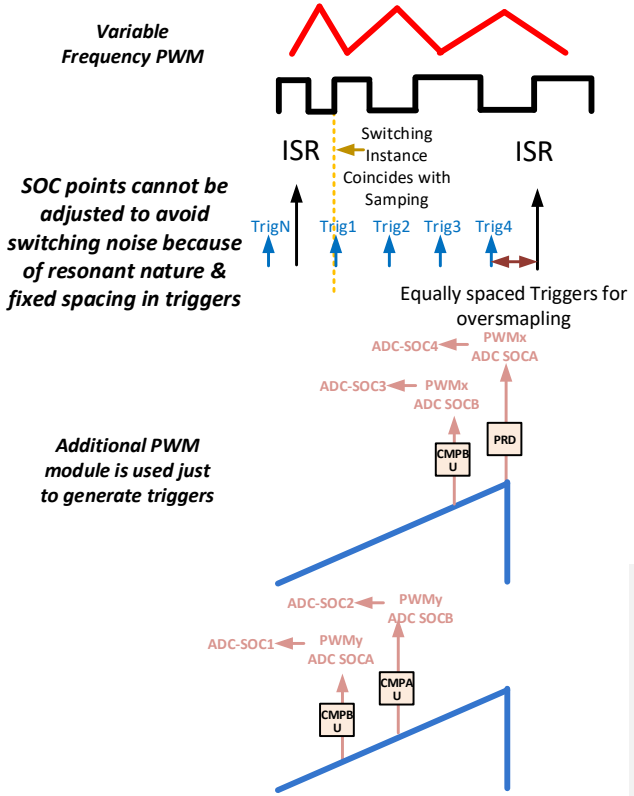
TRIGGER=ePWM SOCA, MODE=OVERSAMPLING, NSEL=3, PHASE=0, SPREAD=0

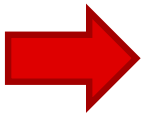
Oversampling spread | Example

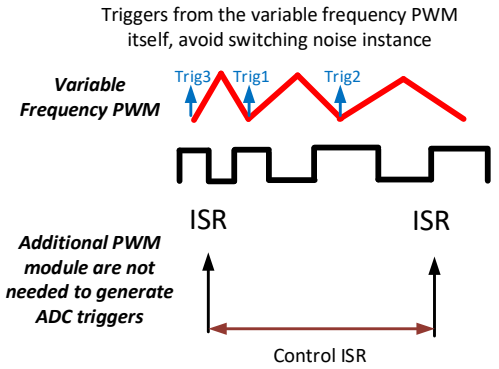


TRIGGER=ePWM SOCA, MODE=OVERSAMPLING, NSEL=3, PHASE=0, SPREAD=500

Avoid switching noise in variable frequency converters







Advantage with new method

1. Switching instances can be avoided when doing oversampling
2. Tunable method allows for the variable number of samples that one can get when avoiding switching instances

F28P65x | PWM and Analog innovation, system cost reduction

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-3 x 12-bit or 16-bit ADC up to 3.5 MSPS

-Up to 40 ADC channels available

-HW post processing

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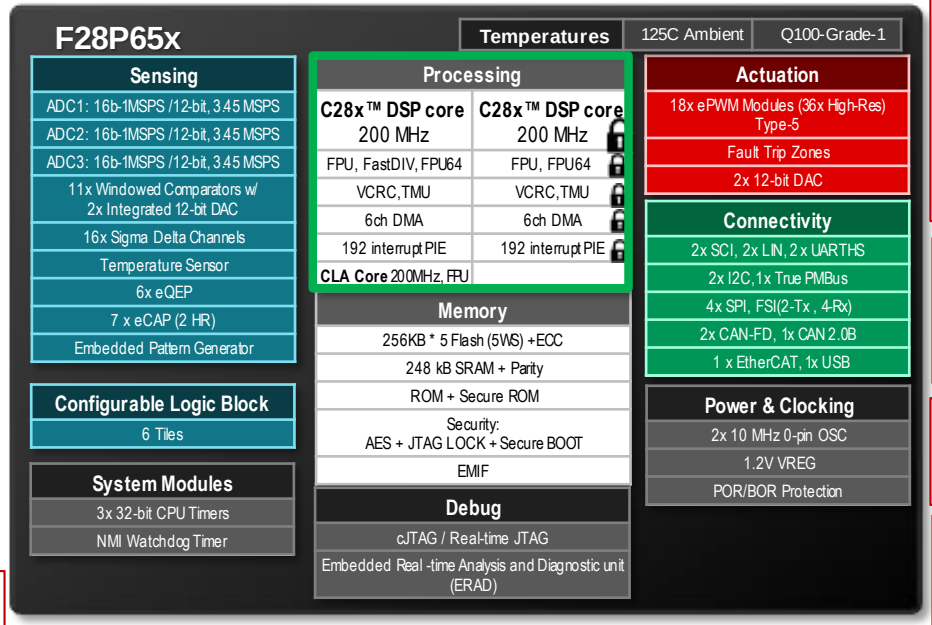

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Enhancing performance | Control Law Accelerator (CLA)

- Execute time-critical control loops *concurrently with the main CPU* and free it up to perform other required tasks.
- *Independent* access to peripheral registers
- Designed for math intensive computations.
- *Minimal latency* → where the time delay between sampling, processing, and outputting must fit within a tight time window in order to meet performance objectives.

CLA Math Library Functions	
Arc-Cosine	Exponential rasied to a Ratio
Arc-Sine	Exponential(Base 10)
Arc-Tangent of a ratio	Inverse Square Root
Arc-Tangent of a Ratio per Unit	Natural Logarithm
Arc-Tangent	Logarithm(Base 10)
Cosine	Sine
Cosine Per-Unit	Sine Per-Unit
Divide	Square Root
Exponential	

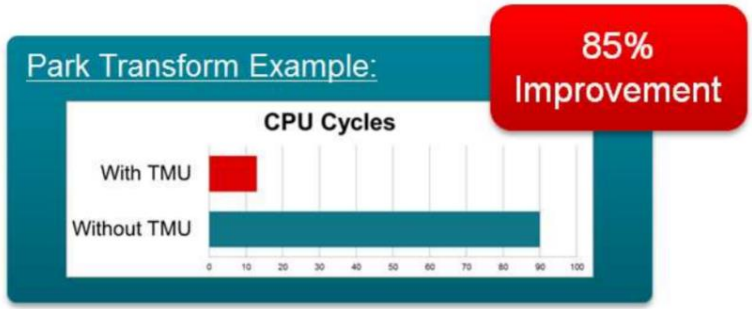
* fully software programmable solution-> CLA Math lib -> C2000ware

Application	Number of Execution Cycles		Improvement
	CPU	CLA	
	Min/Max	Min/Max	
Motor AC Induction	888/952	639/694	1.39x (vs CPU)
Power CNTL 2p2z	48	39	1.23x (vs CPU)
Power CNTL 3p3z	68	52	1.31x (vs CPU)

Enhancing performance | Trigonometric math unit

Key points

- **TMU:** Many common mathematical techniques in real-time control rely on the use of trigonometric functions: sine, cosine, and arc tangent are all examples
- Cycles taken for each instruction are listed below. The test showing 85% improvement is based on a simple Park Transform



Operation	C Equivalent Operation	C28x Pipeline Cycles
Multiply by 2*pi	a = b * 2pi	2 cycles + Sine/Cosine function
Divide by 2*pi	a = b / 2pi	2 cycles + Sine/Cosine function
Divide	a = b / c	5 cycles
Square Root	a = sqrt(b)	5 cycles
Sin Per Unit	a = sin(b*2pi)	4 cycles
Cos Per Unit	a = cos(b*2pi)	4 cycles
Arc Tangent Per Unit	a = atan(b)/2pi	4 cycles
Arc Tangent 2 and Quadrant Operation	Operation to assist in calculating ATANPU2	5 cycles

Equation in Floating-Point C: PARK Transform

```
#include "math.h"
#define  TWO_PI   6.28318530717959
 void park_calc(PARK *v)
{
     float cos_ang , sin_ang;
     sin_ang = sin(TWO_PI * v->ang);
     cos_ang = cos(TWO_PI * v->ang);

     v->de = (v->ds * cos_ang) + (v->qs * sin_ang);
     v->qe = (v->qs * cos_ang) - (v->ds * sin_ang);
}
```

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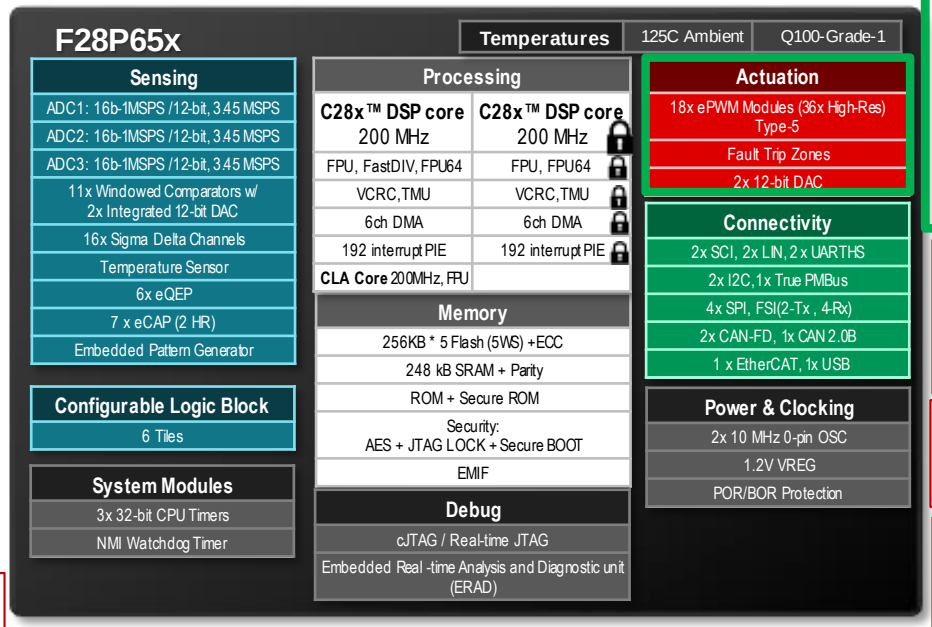

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PWM new feature set

- XCMP Complex Waveform Generator
- Diode Emulation Submodule
- Minimum Dead-Band & Illegal Combo Logic Submodule
- Digital Compare – Event Detection

XCMP complex waveform generator | Overview

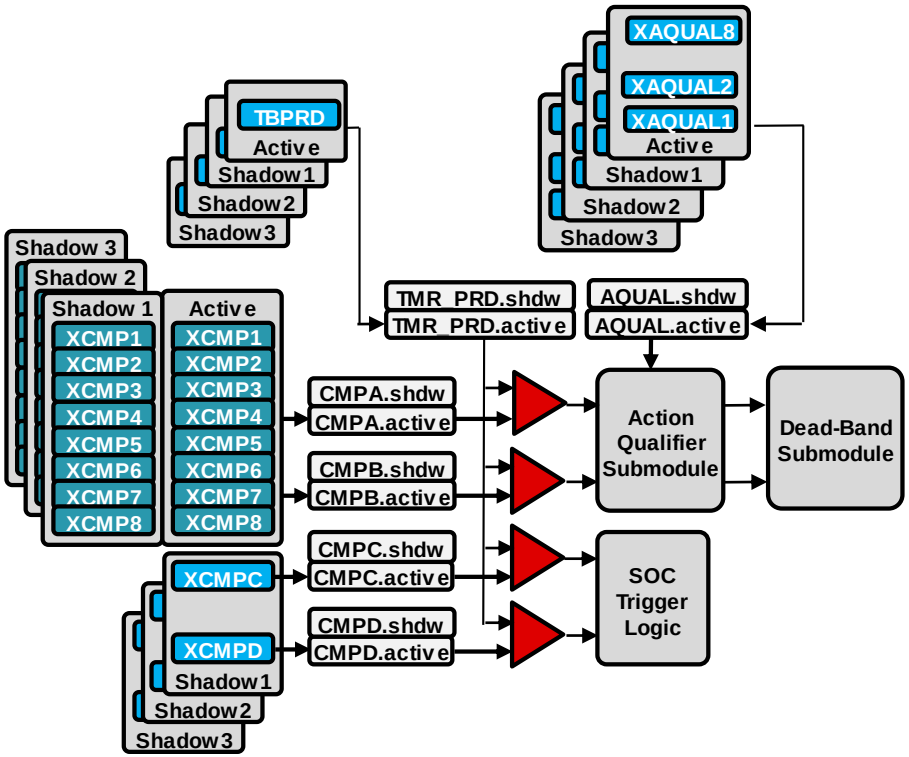
Generate up to four pulses within one EPWM period

Benefits

- ✓ Generate complex waveforms without the need of complex logic within code
- ✓ Useful for High Frequency Resonant Topologies

Highlights

- 8 Comparator values (XCMP1-8)
- 3 sets of shadows for each XCMP value
  - Action qualifier event for each XCMP value, same shadow scheme
- 8 XCMP values can be allocated to CMPA or 4 to CMPA and 4 to CMPB
- XTBPRD, XCMPC, and XCMPD have 3 sets of shadows

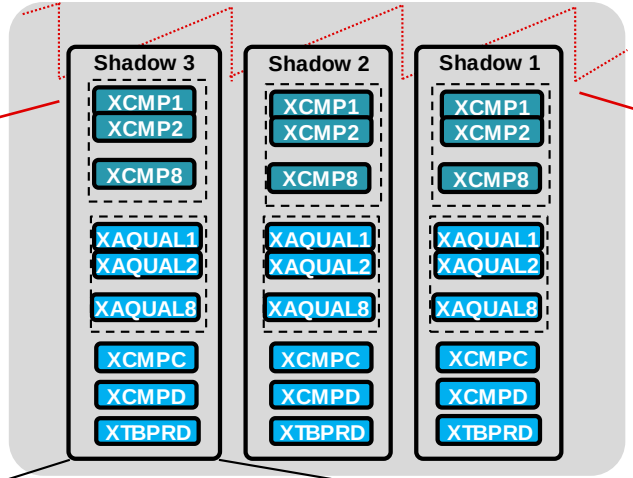


* XCMP Mode can only be used in up-count mode

XCMP complex waveform generator | Example

Shadows 3 and 2 can repeat for up to a total of 8 times

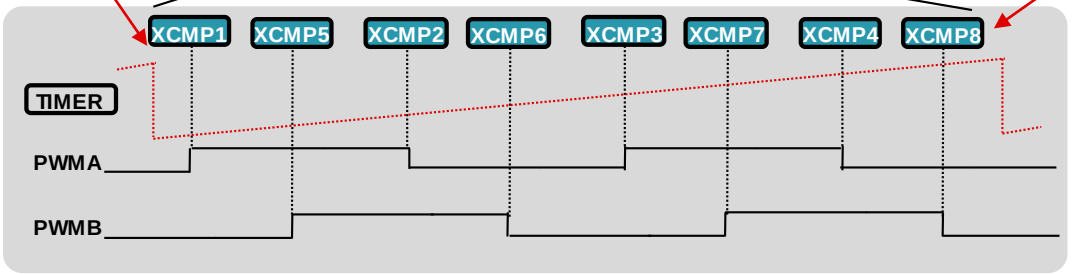
Ex. SHDW3, SHDW3, SHDW2, SHDW2, SHDW2, SHDW1



The amount of shadow sets is configurable as well. No shadow sets, one shadow set… up to 3 shadow sets

Shadow sets get loaded when time base counter equals 0

All 8 or a subset of XCMP values can be used within one period



Minimum dead-band & illegal combo logic | Overview

- **Insert a configurable amount of minimum delay between EPWM modules**
- **Set output low or high if undesired output state across modules occurs**

Benefits:

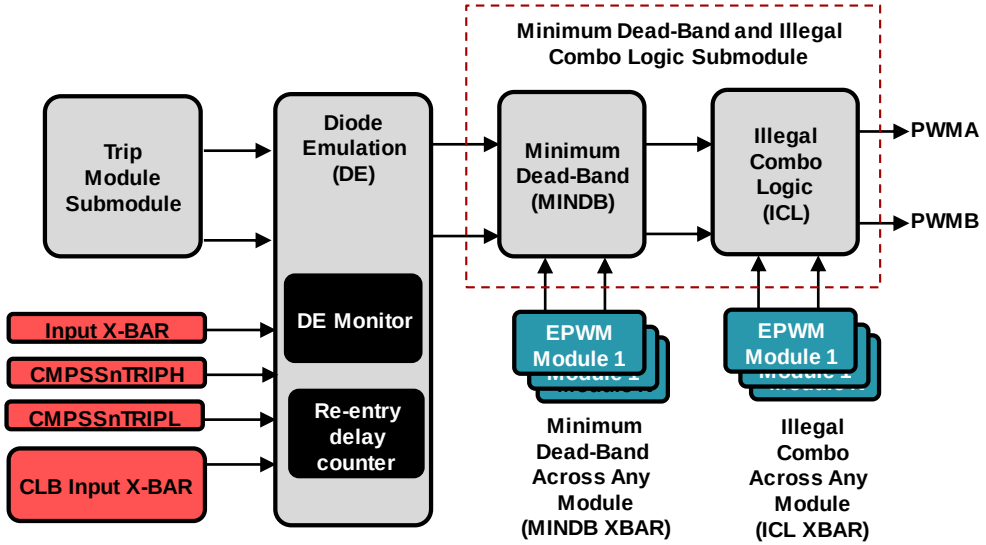
- ✓ Safety feature from power topology perspective to prevent short from supply to ground
- ✓ Prevent unwanted output combinations

Functionality (MINDB)

A blocking signal is generated to prevent both EPWM outputs switching at the same time

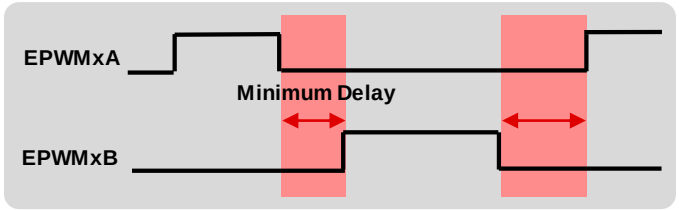
Functionality (ICL)

Logic table based on EPWM outputs is configured to setup “illegal” combos



Minimum dead-band & illegal combo logic | Example

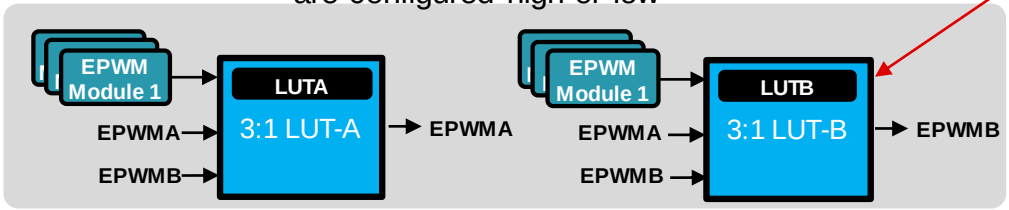
Minimum Dead-Band



Programmable delay (DelayA and Delay B in sysclk cycles) is added to ensure there is always a minimum amount of delay between outputs

Illegal Combo Logic

Based on the truth table, output of EPWMA/EPWMB are configured high or low



Input 1	Input2	Input3	Output
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

Digital compare | Event capture

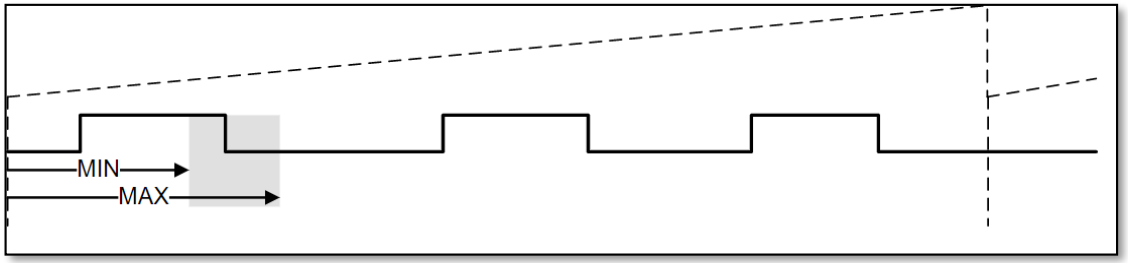
Detect a missing edge event in a configured time window

Benefit:

✓ Generate a trip or interrupt if edge is not detected

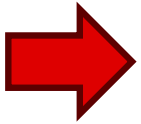
Functionality:

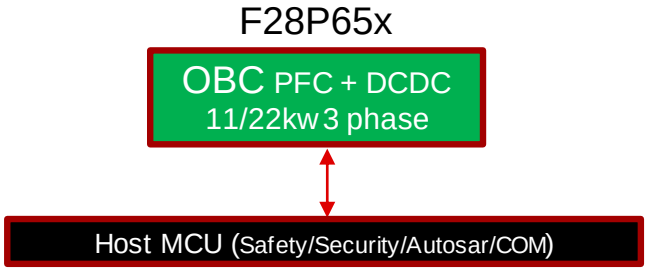
1. Define Min value
2. Define Max value
3. Select *CAPEVT* as trip or interrupt source

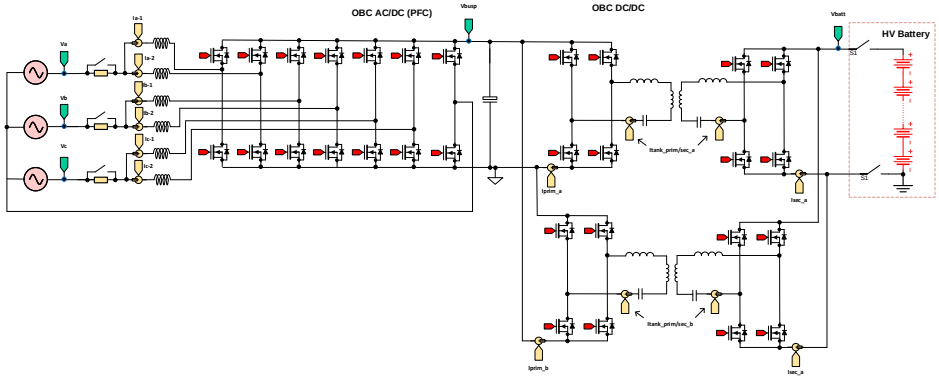


*Min and Max values are also shadowed (3 sets)

F28P65x | On-board charger integration capabilities example







Power stage Topology (up to 22kW, 3Ph)

- PFC: 2-Ph Totempole per phase
- DCDC: 2xCLLLC

F28P65x - PWM and Analog resources

	Power Stage Requirements	F28P65x
PWM Channels	30	Up to 36
ADC Instances	3	3
ADC Channels	23	Up to 40
Comparators	8-11	11

F28P65x - CPU resources

CPU1-C28	CPU1.CLA	CPU2-C28 (Lock Step)
PFC	2xCLLLC	House keeping Safety function

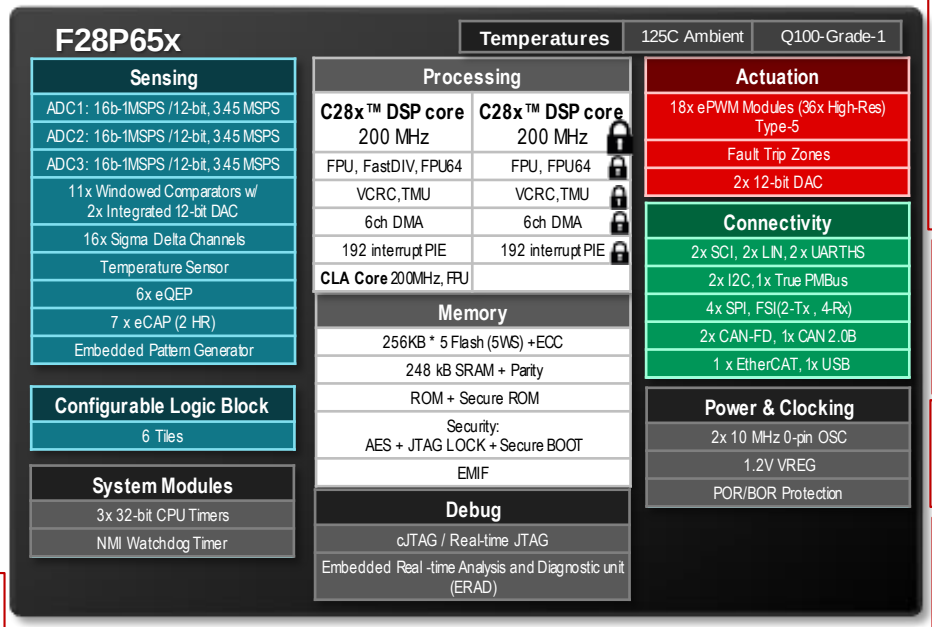
F28P65x | PWM and Analog innovation, system cost reduction

Analog
-3 x 12-bit or 16-bit ADC up to 3.5 MSPS
-Up to 40 ADC channels available
-HW post processing
-New HW ADC oversampling mechanism for better control and 54% improvement on code size and cycles
-11 comparators: protect more signals at the same time, Support for dual ramp generation (easier implementation of hysteretic, peak current mode control with lower latency) and more

Signal capture & generation:
-16xSDFM to support up to 3 axis
-6x Quadrature encoder interface;
-7x capture modules with 2 High Res
-Embedded pattern generator (EPG)
-6 Tiles CLB for encoder implementation, PWM protection, FPGA/ CPLD removal

Memory:
-248kB RAM with Parity
-1.25 MB Flash (ECC)
-Multi-bank support with banks allocable to either CPU statically optimizing mem usage and for easier Live Firmware Upgrade

Real-time Processing Performance:
2x 200 MHz F28x DSP core + FPU64 + TMU + 1x 200 MHz CLA CPU
Option for lock-step core, increased RAM support for CLA (64kB)



Package & Pin Information:
New small 169-pin BGA/ 0.65mmp 9x9mm for space constrained applications
New 256-pin BGA/ 0.8mmp/ 13x13mm supporting 40 ADC channels and many GPIO/ APGIO leading to similar count as 337 BGA from F2837x/ F2828x
100-pin LQFP/ 0.5mmp/ 16x16mm and 176-pin LQFP/ 0.5mmp/ 26x26mm

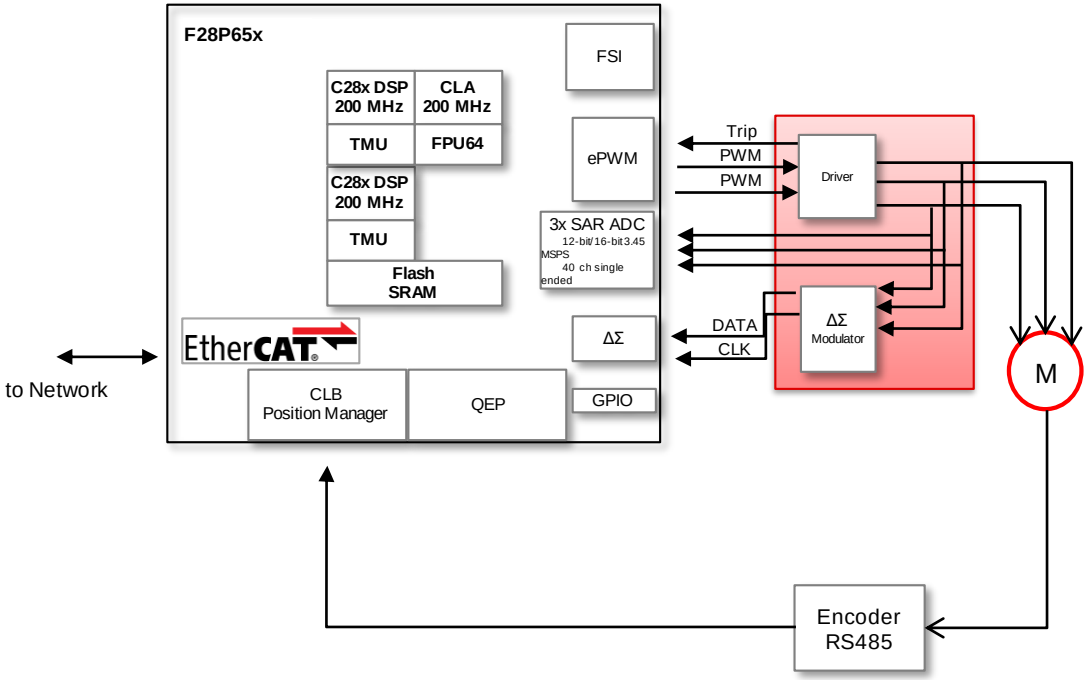
Actuation
-36 high resolution PWM channels
-Type 5 PWM support, Multi-threshold compare, PWM HW sync., diode emulation mode, Minimum Deadband, Illegal combo logic support, digital compare edge detection, Muti-compare operation within one period
-PWMs designed for future of power electronics with Matrix Converters, Multi Level Converters, Dual Active Bridge and Resonant Converters.

Connectivity
EtherCAT, CAN-FD, CAN, USB, 200 Mbps FSI, multiple serial ports, 25Mbps Hi- speed UART with DAM , EMIF, many I/Os and AGPIO

Security
Dual-zone code security, unique ID, secure boot, JTAG lock, HW AES

Safety (ASIL-B/ SIL-2)
Easier implementation with Reciprocal comparison, lock-step core, Periodic HWBIST, 2 DCSM zones, RAM with Parity, Flash all ECC, 2*APLL, BOR, Redundant interrupt vector RAM, better PWM safety with Minimum Deadband , Illegal combo logic support and digital edge detection

F28P65x single chip servo drive + EtherCat



EtherCAT Training: https://training.ti.com/ethercat-protocol-c2000-real-time-controller-training-series

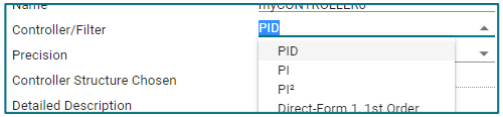
Development | Rapid start – developer zone (dev.ti.com)

Pick a Device

- Search using TI.com
- Preview in SysConfig

Try Tools + Examples in the Cloud

Run examples quickly and easily on real hardware, no SW installations needed



Add Libraries with a Click

One click to add FREERTOS, optimized PID Control Algorithms, CPU accelerators and more!

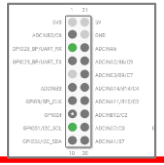
Learn with Academy

Follow along with labs and videos to learn quickly!

1 2 3 4 5 6 7

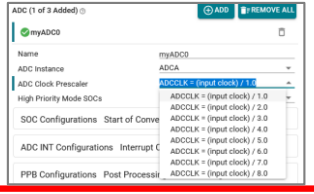
Pick a Board

- Preview EVMs in SysConfig
- Use later in reference designs



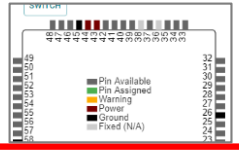
Configuring Examples

Begin configuring peripherals and code for your system needs



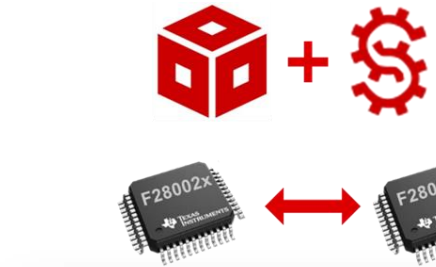
Download for Free

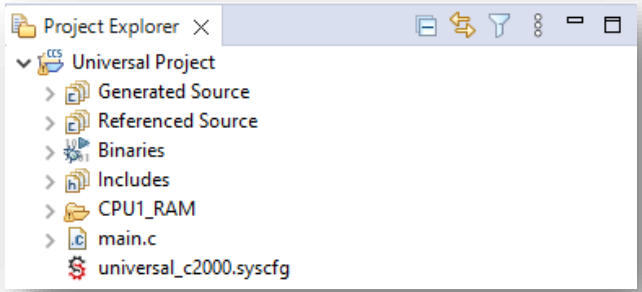
CCStudio IDE, SysConfig, Software Development Kits to begin development



C2000 | Easy migration across devices with One-Click

- C2000 Universal Project Structure with Advanced Migration Support
- **One-Click & In-Place** (within the same CCS project/no copy needed) migration of the **Code Composer Studio properties and SysConfig** from one C2000 device family to another
- Identify the changes introduced by the migration including:
  - Changes in the generated code
  - Changes in the GUI device configuration (PinMux, Resource Management, etc.)
- Customers who utilize this new project structure can migrate across device families at any point in their development with **one-click**
- Errors and warnings are generated for unsupported features, unavailable resources
- Automatic SW diff generation for the device configuration changes caused by the migration





✓ This project can be migrated across C2000 device families with JUST one click

Development resources

You can start evaluating this device leveraging the following:

Content type	Content title	Link to content or more details
Product information	Data-sheet, migration guide, pin-mux, tools	TMS320F28P65DK Product Page TMS320F28P65DK-Auto Product Page F28P65x product brief Technical blog
Training	New to C2000? On-demand training, examples, and videos	C2000 Five Minute Overview C2000 Academy
Development tools to be aware of	C2000Ware Motor Control SDK Digital Power SDK Universal Motor Control Project Guide One-click set-up, pin-mux, device configuration Both Control Card and LaunchPad™ development kit will be supported	www.ti.com/tool/c2000ware www.ti.com/tool/c2000ware-motorcontrol-sdk www.ti.com/tool/c2000ware-digitalpower-sdk www.ti.com/lit/spruj26 C2000 SysConfig F28P65x ControlCard F28P65x LaunchPad

New F28P65x recap

- New PWM generation
- New ADC features
- More integration
- System cost reduction

www.ti.com/c2000

Questions?

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