Adaptive Voltage Scaling Technology

Up to 60% Energy Savings for Digital Core Operation

Texas Instruments

With the emphasis on lowering power consumption a concern for system designers, Texas Instruments pioneered ground-breaking technology for reducing the energy consumed by large-scale CMOS ASICs and other digital systems on a chip (SoCs). This technology is called Adaptive Voltage Scaling (AVS) which can reduce overall energy consumption by up to 60%.* Unlike other methods, AVS is a closed-loop control system that not only handles process variation between devices, but also shifts in temperature, digital load, and process aging.

Modern CMOS processes vary in performance from die to die and wafer to wafer. The extent of the variation is not always known

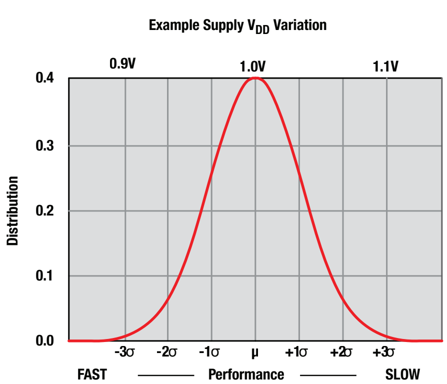

Figure 1. CMOS Processing and Distribution

*Actual power savings will vary by process, temperature, aging, and other factors.

since designers are provided a worse case set of parameters to use for timing closure simulation. The parameters also provide the operating voltage which takes into account the slowest silicon (see ***Figure 1***). Dynamic losses increase exponentially with supply voltage and static losses (i.e. gate and sub-threshold leakage) are increasing with smaller geometries.

$$E = \underbrace{(\alpha + C + f_{CLK} + V^2}_{\text{Dynamic}} + \underbrace{V + I_{LEAK})t_{TASK}}_{\text{Leakage}}$$

By accurately controlling the supply voltage for the actual requirements of each device, large power savings can be realized – but the system needs to know the current performance level of every device. The use of simple, standard hardware interfaces and TI's collaboration with other industry leaders ensures that AVS technology can be used on any CMOS process with standard design tools and flows. Additionally, it can be integrated with any operating system or application, resulting in exceptional energy efficiency.

Technology Features:

- Closed loop real-time adaptive power optimization
- Delivers accurate voltage to each individual processor across temperature, process corner, and frequency variations
- Up to 60% typical power savings over fixed-voltage implementations
- Processor and architecture independent

AVS technology achieves this efficiency by placing fully synthesizable hardware performance monitors or HPMs into the ASIC or SoC (see ***Figure 2***).

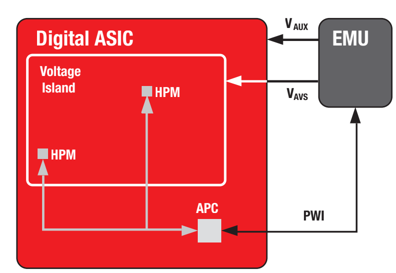

Figure 2. AVS Implementation

National Products
from Texas Instruments

These circuits monitor the device's process and temperature profile and report the information to an embedded controller called the Advanced Power Controller (APC). The APC determines whether a voltage optimization should be made and, if required, sends a command to an external Energy Management Unit (EMU) via an open-standard PowerWise® Interface (PWI) to adjust the voltage supplied to the digital core. AVS runs in real-time, continuous closed-loop operation and therefore maintains the minimum energy required to meet the performance level of the overall system.

AVS technology minimizes system energy consumption and improves reliability by impacting both dynamic and static (leakage) energy consumption. The energy savings from an AVS implementation can be seen in ***Figure 3***.

This portable system example consists of the ARM CPU running with a variable frequency of 60, 120, 180, or 240 MHz. With AVS, 64% energy saving is achieved compared to the fixed-voltage scheme. AVS also demonstrates 28% energy saving over Dynamic Voltage Scaling (DVS) because it compensates for process and temperature variation where DVS frequency-to-voltage look-up tables do not.

TI developed Adaptive Voltage Scaling technology specifically to address tomorrow's energy-saving requirements. It is ideally suited to high volume systems such as data centers and wireless base stations, as well as power constrained applications such as portable devices, USB powered peripherals, and consumer electronics. Anywhere that an ASIC, processor, or SoC is used, AVS can be implemented.

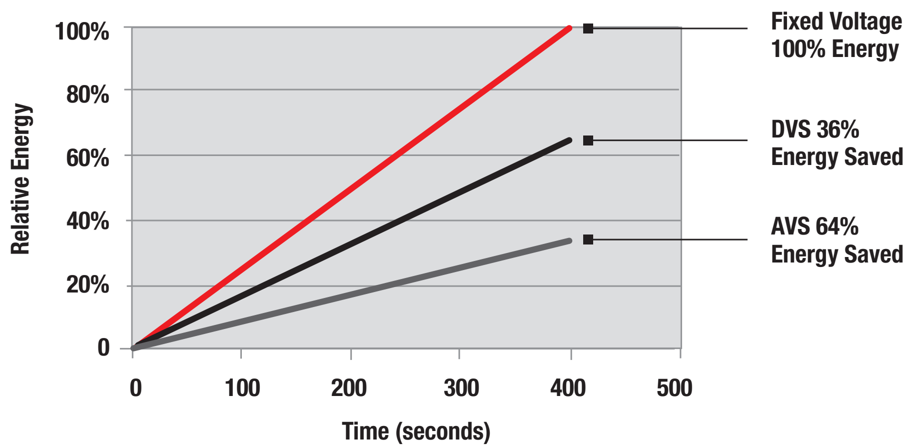

Figure 3. Energy savings with PowerWise AVS

AVS Products

Product Type	Product ID	Topology	V_{IN} (V)	Outputs	Bus
Multi-Output EMU	**LP5550**	PMIC	2.7 – 5.5	1 x 300 mA switcher, 3 LDOs 50 – 250 mA	PWI 1.0
	LP5551	PMIC	2.7 – 5.5	2 x 300 mA switchers, 4 LDOs 25 – 250 mA	PWI 2.0
	LP5552	PMIC	2.7 – 4.8	2 x 800 mA switchers, 5 LDOs 25 – 250 mA	PWI 2.0
	LP5553	PMIC	2.7 – 4.8	2 x 800 mA switchers, 5 LDOs 25 – 250 mA	SPMI
	LM10503	PMIC	3 – 5.5	2A AVS switcher, 2 x 1A switchers	PWI 2.0
Single Output EMU	**LM10500**	Switcher	3 – 18	5A AVS switcher	PWI 1.0 / 2.0
	LM10520	Controller	3 – 18	20A AVS controller	PWI 2.0
	LM10540	Controller	3 – 42	20A AVS controller	PWI 2.0
AVS System Controller / Bridge Chip	**LM10000**	AVS bridge chip	N/A	Bridge chip enables AVS in power solutions	PWI 2.0

Visit **www.ti.com/avs** to learn more about PowerWise AVS technology.

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