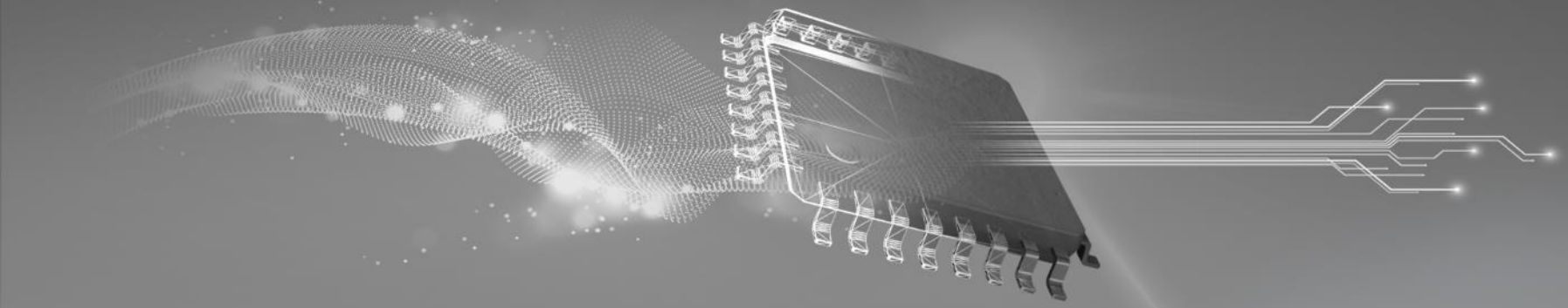
TI TECH DAYS



Solving Common Buck Converter Design Challenges

Rich Nowakowski

Texas Instruments

Texas Instruments

Agenda

1. Reducing voltage ripple for signal chain power.
2. Achieving high output voltage accuracy for FPGA power.
3. Understanding impact of thermal SOA.
4. Smaller size with faster switching frequencies.
5. Control mode types.
6. Using WEBENCH® to address the latest buck converter design challenges.

Challenge #1: low noise for signal chain power

Achieving low-ripple output voltage noise without a linear regulator, using higher current DC/DC converters.

LDO drawbacks compound at higher currents:

- Cost penalty, but some designers may not care.
- Thermal penalty.
- Efficiency penalty.
- Size penalty.
- Paralleling LDOs is possible, but complicated.

Attribute	400-kHz Design with LDO	4-MHz Design	Advantage
Size	640 mm^2	195 mm^2	4-MHz design
Full-load efficiency	77.2%	86.8%	4-MHz design
Power loss	2.06 W	1.1 W	4-MHz design
IC temperature	57.8°C + 51.6°C	37.1°C	4-MHz design
Transient over-shoot	146 mV	35.5 mV	4-MHz design
Ripple voltage	11.5 mV	6.7 mV	4-MHz design
Output voltage noise	14.9 µV	135 µV	400-kHz design
Solution cost	$9.55 at 1 Ku	$7.50 at 1 Ku	4-MHz design

- 12V to 1.8V @ 4A
- No additional noise reduction techniques employed

Low noise means different things to different designers

Low noise problem	Specific need	Market	IC solution	Package solution	PC board solution	System solution
Low output voltage ripple (μV_{PP})	High speed ADC and AFE systems need to reduce the output ripple to ~200µV to maintain high ENOB (effective number of bits).	Wireless Infrastructure, Test and Measurement	2nd loop compensation, Higher Fsw (reduced inductor ripple), Spread Spectrum	Hotrod packaging, RLF with integrated input cap	Ferrite output filter, post regulate with LDO, multiple caps to reduce ESL	
Phase noise (μV_{RMS})	Clocking systems need low phase noise from from 100Hz to 100kHz 20uV_{RMS} or less output noise voltage	Wireless Infrastructure, Test and Measurement	optimize bandgap and optimize error amplifier design for low intrinsic device noise			
1/f noise	Thermal and flicker noise can cause errors in low frequency bands	Test and Measurement	Reduce bandgap noise			
Power supply rejection	ADC requires ~40dB of input power supply rejection to minimize cross coupling noise from the input rails	Test and Measurement	IC may meet the spec		Additional input filtering	
Electromagnetic interference (EMI)	Meet FCC Unintentional Radiator Limits	Radio and TV receivers, PE		Hotrod packaging		
	Meet FCC Intentional Radiator Limits	Wireless (WLAN and BT, etc) devices	Adjustable slew rate and/or optimized gate drive, Spread Spectrum	Hotrod packaging, RLF with integrated input cap	Good board layout to minimize coupling power supply noise	Metal shielding
	Meet CISPR 25 Class 5	Automotive applications	Adjustable slew rate and/or optimized gate drive, Spread Spectrum, allow SYNC to external clock with Spread Spectrum	Hotrod packaging, RLF with integrated input cap	Chokes to the power supply input	Metal shielding

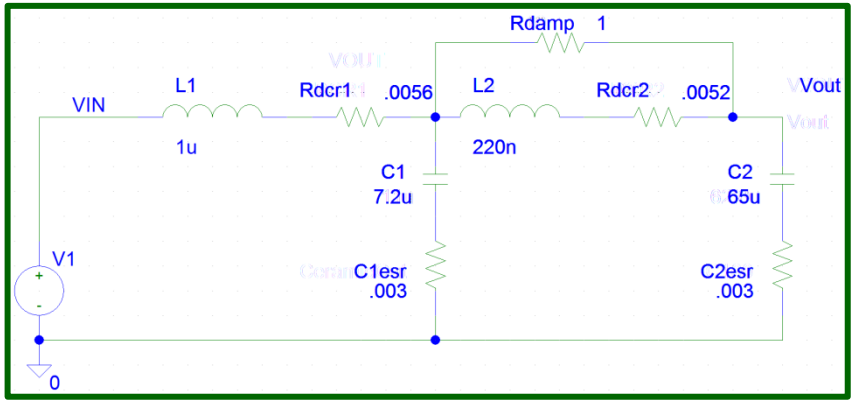
Low noise: tips to reduce noise conduction to the load

- High self-resonant frequency for inductor.
- Place vias for bypass capacitors between terminals.
- Keep non-ground vias spaced wide enough to allow ground planes to flow between vias
- Ramp capacitors up and down from inductor to load: 1.0uF, 2.2uF, 4.7uF, 10uF, 22uF, 47uF, 100uF, 47uF, 22uF, 10uF, 4.7uF, 2.2uF, 1.0uF.
- Mix capacitor values with 2:1 or 3:1 values and different packages.
- Use Multi-phase converter.
  - Synchronized and phase-shifted multi-phase architecture increase ripple frequency and reduce ripple currents.
  - Use different boot resistors and snubbers on each phase to spread noise spike frequencies.
- Use Second-stage Output Filter.
  - Ferrite Bead or soft-resonating inductor between first and second stage.
  - DC regulation feedback after second filter, with feed-forward capacitor from first stage to minimize loop impact of 2-stage filter.

Low noise: two-stage output filter example

TPS54618-Q1 example:

- 5 V_{IN} to 3.3 V_{OUT} @ 5 A
- Fsw = 750 kHz
- Cout = 22 uF 6.3 V X5R ceramic
- L = 1 uF
- Ripple is 39 mV (~1%)
- Target ripple: 1 mV ripple



Step #1:

- Make the second-stage capacitor 4x to 10x bigger than the first-stage capacitor. Choose 100 uF X5R.

Step#2

- Choose new resonant frequency – 150 kHz. Rule of thumb (3-5x higher than loop cross-over frequency).
- Calculate second stage inductor value (L2) using equation. Choose 220 nH.

Step #3

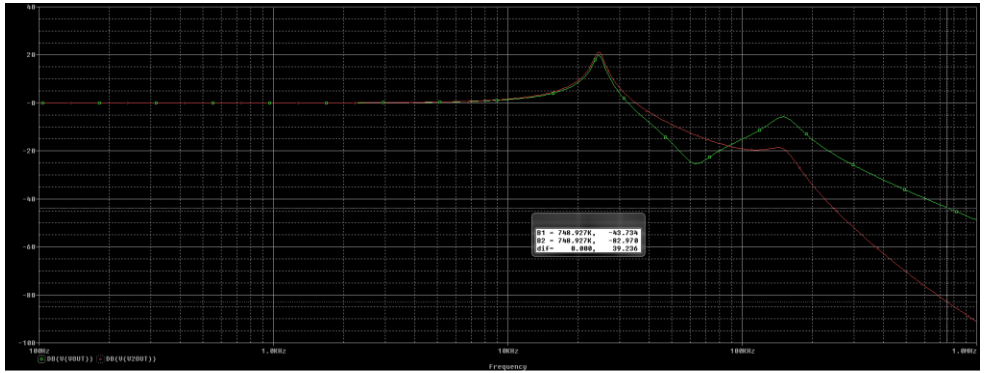
- Damp the second filter resonance properly. That means carefully choosing the ESR of the second inductor.

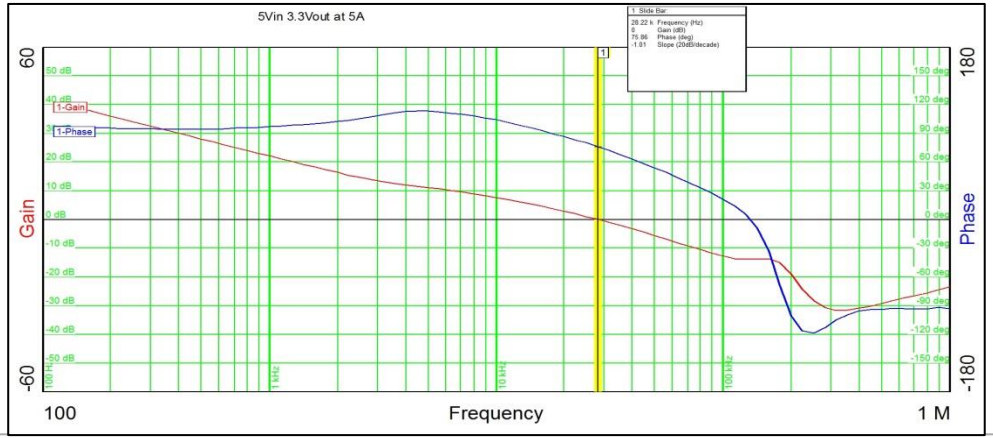
Step #4

- Re-compensate the loop.

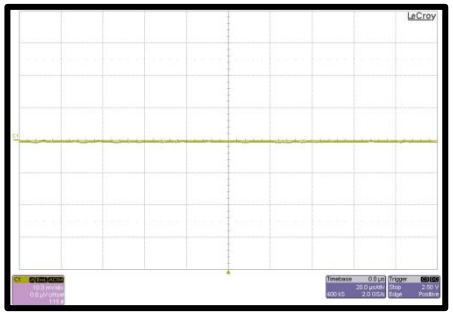
$$F,res2 = \frac{1}{(2\pi*\sqrt{L2*Cs})}, \text{ where } Cs = \frac{1}{\frac{1}{C_1}+\frac{1}{C_2}}$$

Two-stage filter waveform results



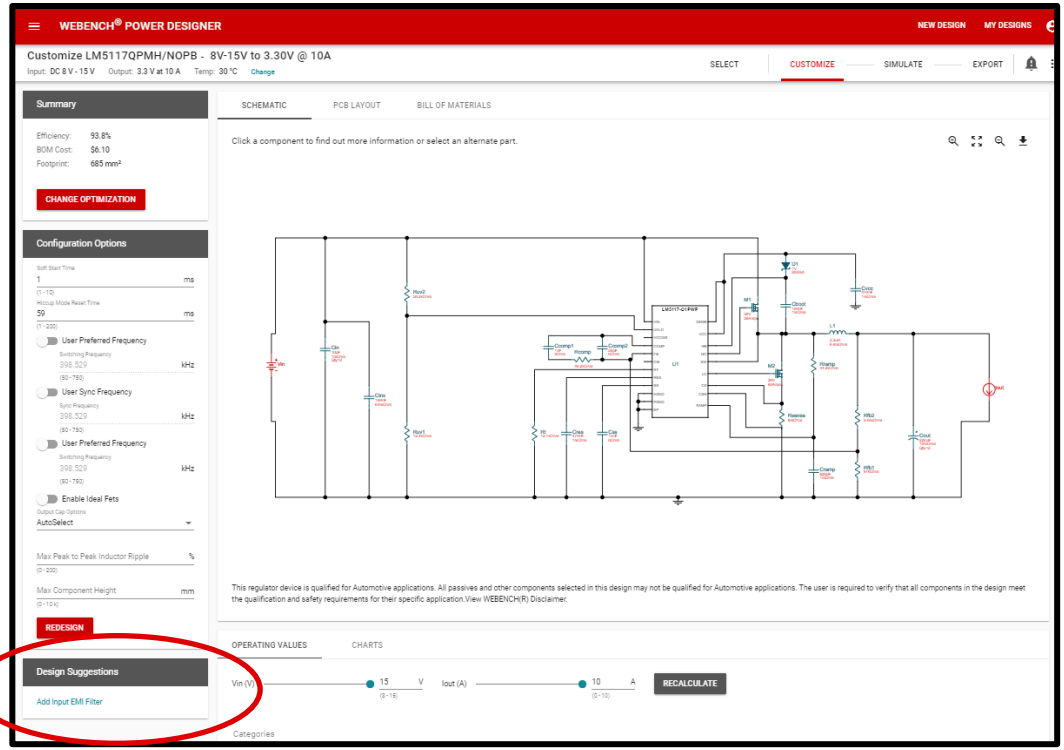


- Transfer function before and after the second LC shown. There are two resonances: 25 kHz and 150 kHz.
- Simulating the power-stage gain and phase shows the output pole at 6.5 kHz.
- Measured loop response is also shown.
- <1mV ripple achieved.



Low noise: WEBENCH example

- Create design.
- Click on “Add Input EMI Filter” from design suggestions.
- Choose “Noise Standard” and “Noise Class”.



Low noise: resources

Application reports:

- Reducing output ripple and noise with the TPS84259 module.
- Not all jitter is created equal
- Reduce buck-converter EMI and voltage stress by minimizing inductive parasitics.
- Reducing noise on the output of a switching regulator.
- Understanding and managing buck regulator output ripple

Technical articles:

- Power tips: Designing a two-stage LC filter TPS54678 (TPS54618-Q1).
- Design a second-stage filter for sensitive applications LMZ23601.

White papers:

- Simplify low-EMI design with power modules.

Reference designs:

- Paralleling multiple LDOs (14A) reference design.

Challenge #2: voltage regulation accuracy

As process technology advances, processor voltage requirements are lower and require high accuracy.

More Expensive Virtex Ultrascale+

Recommended Operating Conditions (16 nm)

Symbol	Description[1, 2]	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}	Internal supply voltage	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage	0.698	0.720	0.742	V
	For -3E devices: internal supply voltage	0.873	0.900	0.927	V
V_{CCINT_IO}[3]	Internal supply voltage for the I/O banks	0.825	0.850	0.876	V
	For -2LE (V_{CCINT} = 0.72V) devices: internal supply voltage for the I/O banks	0.825	0.850	0.876	V
	For -3E devices: internal supply voltage for the I/O banks	0.873	0.900	0.927	V
V_{CCBRAM}	Block RAM supply voltage	0.825	0.850	0.876	V
	For -3E devices: block RAM supply voltage	0.873	0.900	0.927	V
V_{CCAUX}	Auxiliary supply voltage	1.746	1.800	1.854	V

DS923 - Virtex UltraScale+ FPGA Data Sheet: DC and AC Switching Characteristics (v1.15)

VCCINT	±3%
VCCBRAM	±3%
VCCAUX	±3%

Cheaper Spartan 7

Recommended Operating Conditions (28 nm)

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
V_{CCINT}[3]	For -2 and -1 (1.0V) devices: internal supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: internal supply voltage.	0.92	0.95	0.98	V
V_{CCAUX}	Auxiliary supply voltage.	1.71	1.80	1.89	V
V_{CCBRAM}[3]	For -2 and -1 (1.0V) devices: block RAM supply voltage.	0.95	1.00	1.05	V
	For -1L (0.95V) devices: block RAM supply voltage.	0.92	0.95	0.98	V
V_{CCO}[4][5]	Supply voltage for HR I/O banks.	1.14	–	3.465	V

DS189 - Spartan-7 FPGAs Data Sheet: DC and AC Switching Characteristics (v1.9)

VCCINT	±3%, ±5%
VCCBRAM	±3%, ±5%
VCCAUX	±5%

Voltage regulation accuracy: sources of error

Sources of output voltage error:

- Routing distance and trace losses of the circuit board.
- DC/DC converter:
  - Temperature swings.
  - Input voltage variations.
  - Feedback voltage accuracy.
- Ratio of the resistor divider & tolerance of resistors.
- Voltage ripple.
- Load transients.

Voltage regulation accuracy: DC/DC converter datasheet

Choose DC/DC with V_{FB} <= 1% accuracy

Cheaper TPS568230 17 V / 8 A

T_J =-40°C to 125°C, V_{VIN} = 12 V, unless otherwise noted

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	594	600	606	mV
		T_J = -40°C to 125°C	592	600	611	mV

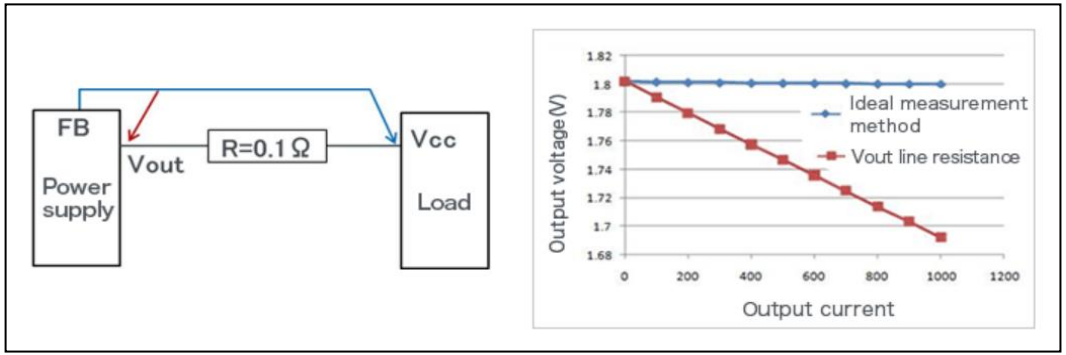
More expensive TPS54824 17 V / 8 A

T_J = -40°C to 150°C, VIN = 4.5 V to 17 V (unless otherwise noted)

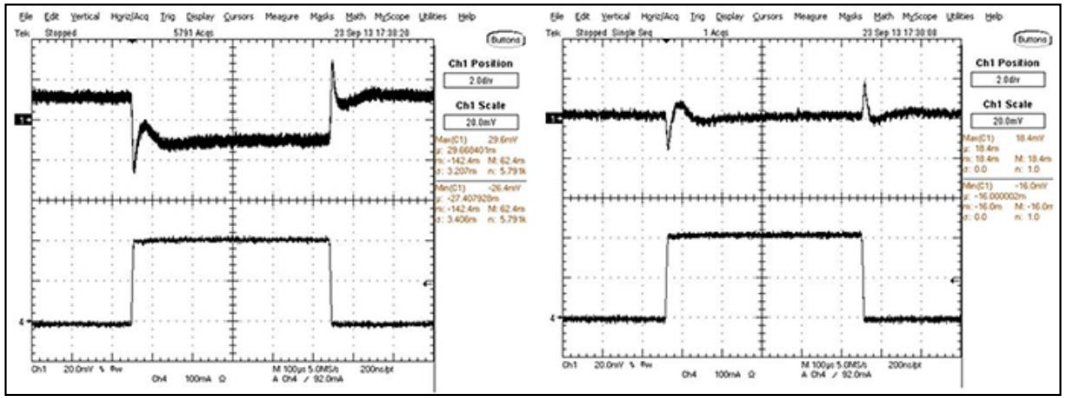
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FB						
V_{FB}	Regulated FB voltage	T_J = 25°C	596	600	604	mV
		T_J = -40°C to 150°C	595	600	605	mV

- Consider line and temperature changes.
- Avoid the ‘front page’ accuracy number.

Voltage regulation accuracy: remote sense

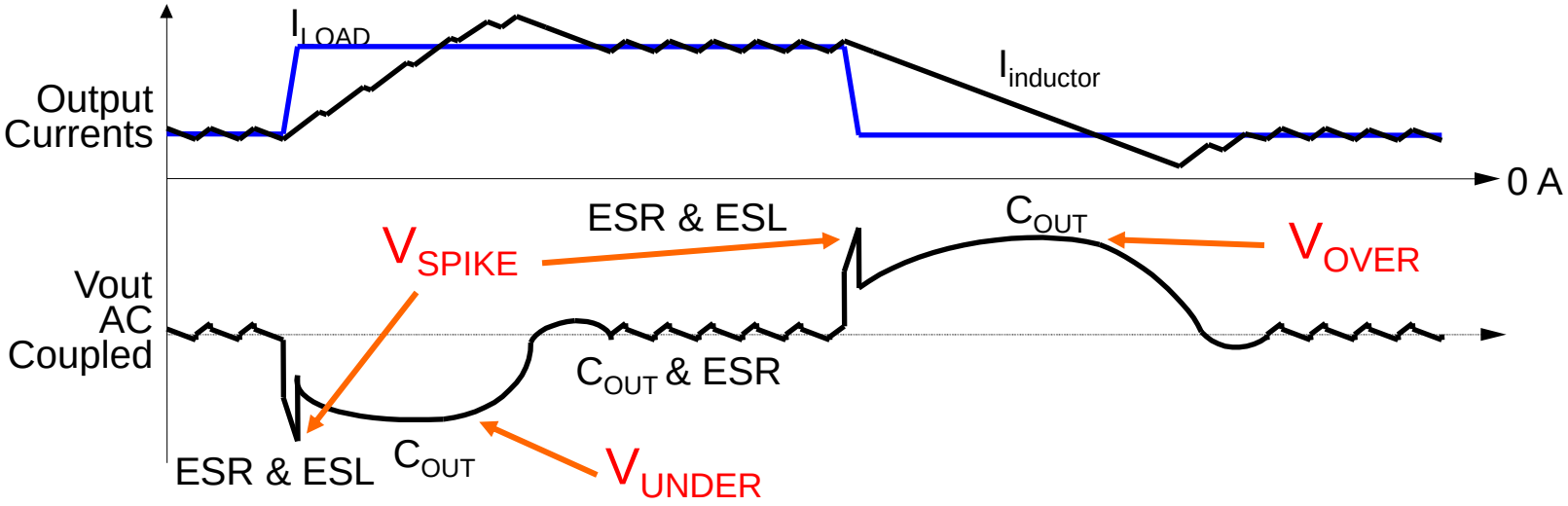


- Ohm's Law: V = I x R
- Line resistance cannot be eliminated, only reduced or managed.



- Waveforms with and without remote sensing.
- Notice voltage drop during load transient w/o remote sense.

Maintaining voltage accuracy during load transient



- Transient from light load to heavy load creates an under shoot.
- PWM delivers maximum duty until the control loop catches up.
- Output capacitor supplies load until inductor catches up.
- Similarly when load changes from heavy load to light load, output will overshoot.
- Duty cycle goes to zero, $V_L = V_O$.

Voltage regulation accuracy: ±3% & ±5% example

$$V_{UNDER} = \frac{I \times dt}{C} \quad \text{where} \quad I = \frac{I_{STEP}}{2} \quad \text{(Avg. current)}$$

$$dt = \frac{L \times dI}{D_{MAX} \times V_L} \quad \text{where} \quad dI = I_{STEP}, V_L = V_{IN} - V_O$$

$$V_{OVER} = \frac{L \times I_{STEP}^2}{2 \times C_O \times V_O} \ (V_L \text{ is Vout}) \quad V_{UNDER} = \frac{L \times I_{STEP}^2}{2 \times C_O \times D_{max} \times (V_{IN} - V_O)}$$

$$C_O > \frac{L \times I_{STEP}^2}{2 \times V_{OVER} \times V_{OUT}} \qquad C_O > \frac{L \times I_{STEP}^2}{2 \times V_{UNDER} \times D_{max} \times (V_{IN} - V_{OUT})}$$

Example: 4-A TPS62136

- Transient: 0.8-A to 3.2-A load step
- Input voltage: 12 V
- Output voltage: 1.8 V
- Inductor: 1.5 uH
- V_{under}: 1.746 V, 1.71 V
- V_{over}: 1.854 V, 1.89 V

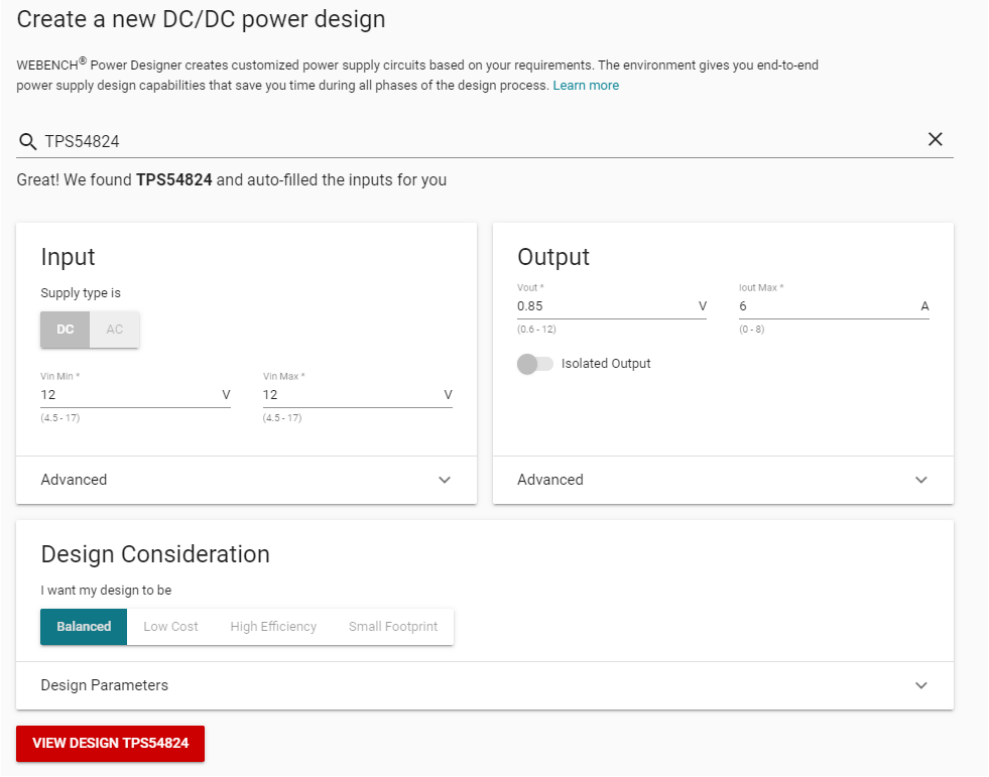
Co for ±5% is 26 uF
Co for ±3% is 44 uF

Voltage regulation accuracy: WEBENCH example

- Transient: 1-A to 6-A load step @ 1A/us
- Input voltage: 12 V
- Output voltage: 0.85 V
- Inductor: 470 nH

	3%	**5%**
• V_{under}:	0.825 V,	0.808 V
• V_{over}:	0.876 V,	0.893 V

Use WEBENCH to get 1% ripple and 3% transient with TPS54824.



Voltage regulation accuracy: resources

Application Reports:

- Achieving Better than 1% Output Voltage Accuracy with 40A TPS546D24A, 20A TPS546B24A, & 10A TPS546A24A
- Remote Sensing for Power Supplies
- Power Supply Design Considerations for Modern FPGAs
- Calculating Output Capacitance to Meet Transient and Ripple Requirements of Integrated POL

Technical Articles:

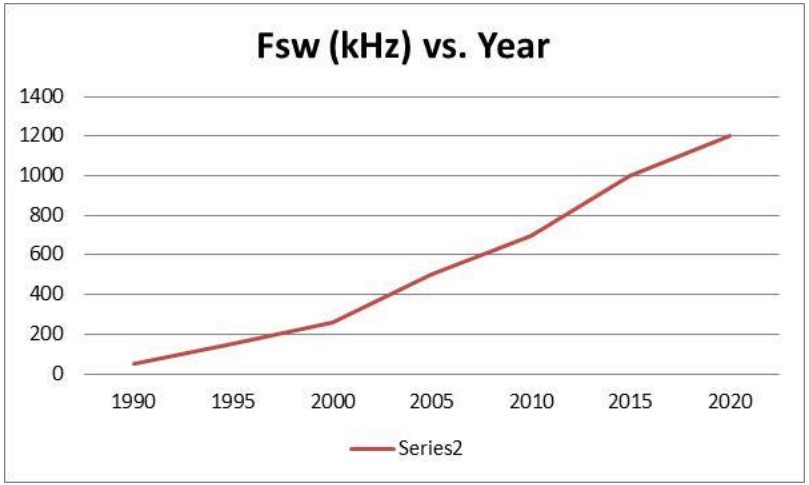
- “Kollman Power Tip #18” voltage dividers and Vout accuracy

On-line training:

- How to meet FPGA's DC voltage accuracy and AC load transient specification

Challenge #3: higher switching frequency to reduce area

Achieve higher power density by increasing the DC/DC converter's switching frequency.



- Board space is valuable.
- Suppliers are releasing faster DC/DC converters that claim to save space.
  - How much space is really saved?
  - What are the trade-offs?

Higher switching frequency: considerations

Switching frequency considerations:

- Minimum on-time.
- Pulse-skipping.
- Efficiency and power losses.
- LC filter area.
- Voltage ripple.
- Transient response.
- Component cost.

Higher switching frequency: minimum on-time

Check the minimum controllable on-time in the datasheet, not the maximum oscillator frequency!

100-V synchronous buck DC/DC controller with wide duty cycle

LM5146-Q1 PWM Control		Min	Typ	Max	unit
$t_{ON(MIN)}$	Minimum controllable on-time		40	60	ns
$t_{OFF(MIN)}$	Minimum off-time		140	200	ns
DC_{100kHz}	Maximum duty cycle	98%	99%		
DC_{400kHz}		90%	94%		

Min. Duty Cycle = Min. On time x Switching Frequency
0.06 = 60 ns x 1 MHz

Examples at 1 MHz:
0.8 V_{OUT} = V_{INMAX} x 0.06; V_{INMAX} = 13 V
3.3 V_{OUT} = V_{INMAX} x 0.06; V_{INMAX} = 55 V

Pulse-skipping happens when the DC/DC converter cannot extinguish the gate drive pulses fast enough to maintain the desired duty cycle.

- Converter will still regulate, but:
- Ripple voltage increases due to the pulses being further apart.
- Frequency is no longer predictable.
- Current limit may no longer work since the IC cannot respond in time.
- Control loop may be unstable. Transient response is also affected.
- Reduce Fsw, lower the input voltage, or pick a different part.

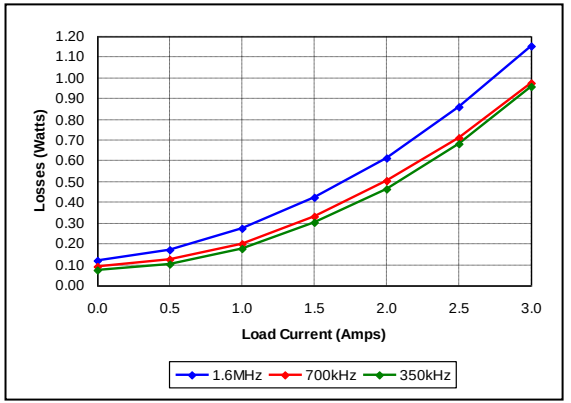
Higher switching frequency: power loss & efficiency

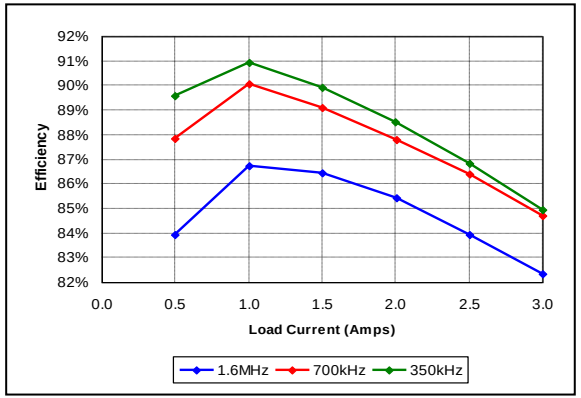
Design example (TPS54388C-Q1):

- 5 V_{IN}, 1.8 V_{OUT}, 3 A, 20-mV ripple, $1A_{p-p}$
- Total power loss 350 kHz: 0.95 W
- Total power loss 1.6 MHz: 1.15 W

Power losses:

- FET driving loss (Qg * V * Fsw)
- FET switching loss f(Vin, Iout, Ton/off, Fsw)
- FET resistance (I^2 * Rds(on))
- Inductor loss (I^2 * DCR + Core losses):
- Capacitor loss (I_{RMS}^2 * ESR)
- IC loss (Iq)





Higher switching frequency: transient & ripple

L = V * ΔI / Δt
L ≥ Vout * (1-D)/(ΔI x Fs)
ΔI = 1-A peak to peak

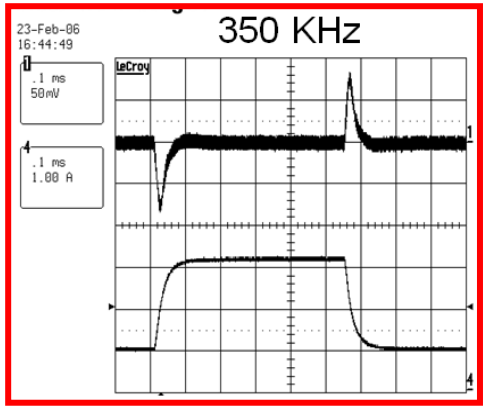
- 350 kHz: L ≥ 3.3 uH → Choose 3.5 uH (84mm²)
- 1.6 MHz: L ≥ 0.7 uH → Choose 1.0 uH (41mm²)

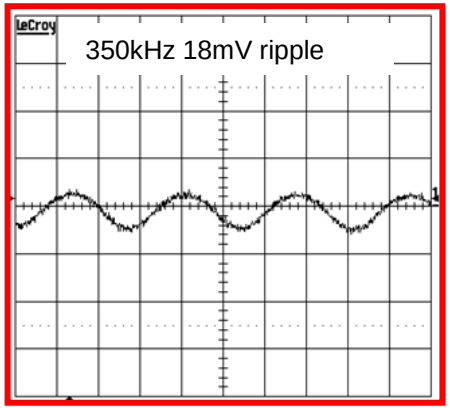
R = V/I → ESR ≤ ΔV/ ΔI; use 0 mΩ for ceramic
I = C * dv/dt → C ≥ ΔI /(8 * Fs * ΔV)
Total ΔV = ΔI / (8 * C * Fs) * 2 (to account for DC bias)

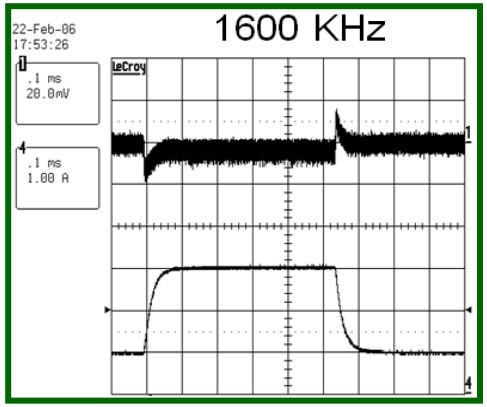
- 350 kHz: C ≥ 36 uF → Choose 47 uF 1206 (5mm²)
- 1.6M Hz: C ≥ 7.9 uF → Choose 10 uF 0603 (1.4mm²)

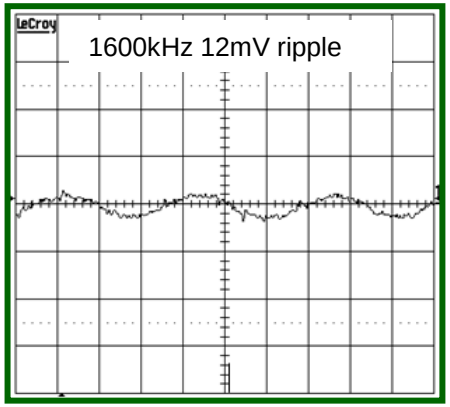
Space savings: 45 mm²

Not counting keep-out





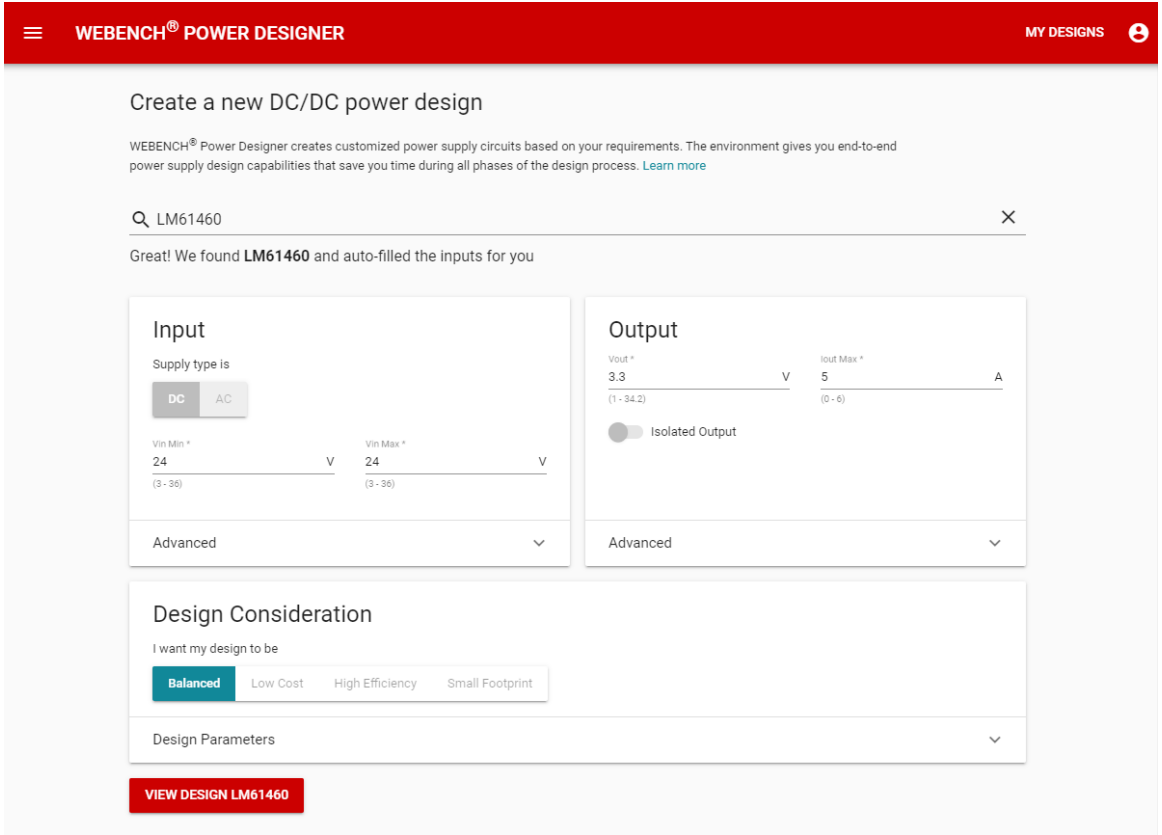




Higher switching frequency: WEBENCH example

- Customer using LM61460
- V_{IN}=24, V_{OUT}=3.3 I_{OUT} = 5 A

- What are some of the ways we can use WEBENCH to reduce the overall size of our design?



Higher switching frequency: WEBENCH example

- Beginning size with ”balanced” design=146 mm^2
- Efficiency 85.7%
- Now let’s click “Change Optimization”

Optimization options

	Small Footprint Design	Low Cost Design	Balanced Design	High Efficiency Design
Efficiency	81.2 %	84.1 %	85.7 %	88.4 %
Bom Cost	$3.74	$4.74	$3.82	$4.72
Footprint	130 mm²	138 mm²	146 mm²	181 mm²
	SELECT	SELECT	SELECT	SELECT

Higher switching frequency: resources

Application Notes:

- Benefits of a Multiphase Buck Converter

Technical Articles:

- Trade-Offs In Switching High-Input-Voltage Step-Down Converters at High Frequencies
- Choosing the optimum switching frequency of your DC/DC converter

Challenge #4: safe operating area

Will the small QFN package of the DC/DC converter or the power module handle the rated high current?

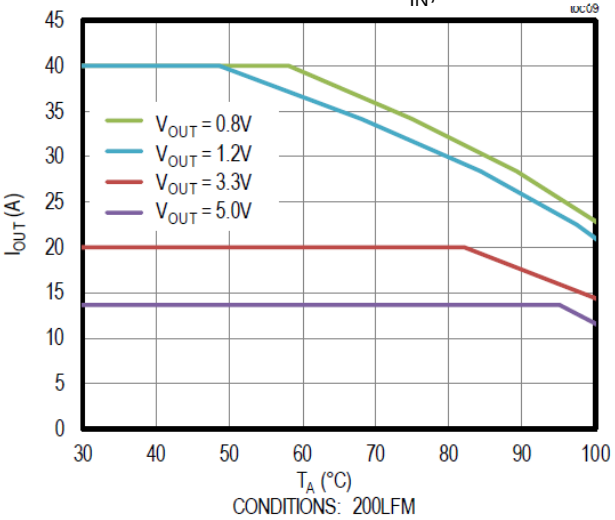
- Safe Operating Area (SOA) represents operating conditions where the maximum electrical and thermal rating of the component will not be exceeded.
- Recommended operating points are always less than the SOA limits.
- Cooler is always better for reliability.

SOA: using SOA curves

- SOA curves tell the designer:
  - Desired current at the desired Ta.
  - Airflow is needed.
  - How much margin or reserve is available.
- The farther the operating point is from the SOA boundary, the cooler the supply will operate.
- SOA curves do *not* represent thermal shutdown points. Some products will not reach shutdown until pushed past SOA limits.
- Catalog current rating may be rated under different conventions.

SOA: comparison

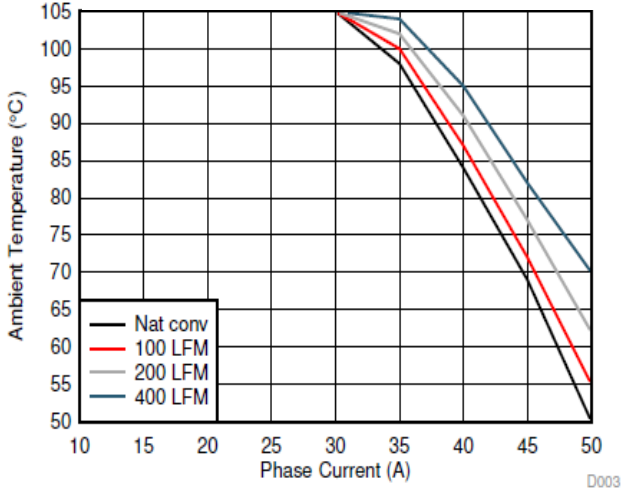
40 A MAX20734 12 V_{IN}, 400 kHz



- 22A @ 84C Ta, no airflow, 30A @ 84C, 200LFM
- EVM board results shown with 4 layers of 2 oz copper

4.15x9 mm QFN
JEDEC θ_{JA} = N/A °C/W
EVM θ_{JA} = 12°C/W

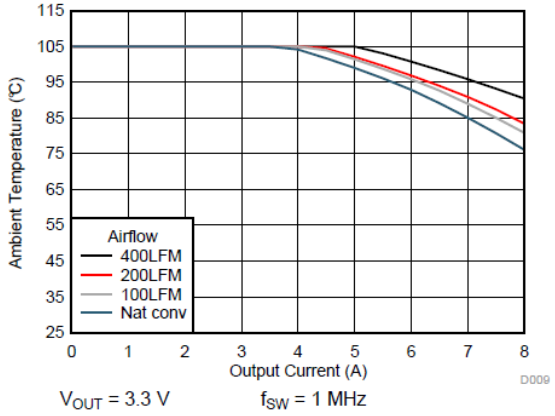
40-A TPS546D24A 12 V_{IN}, 325 kHz



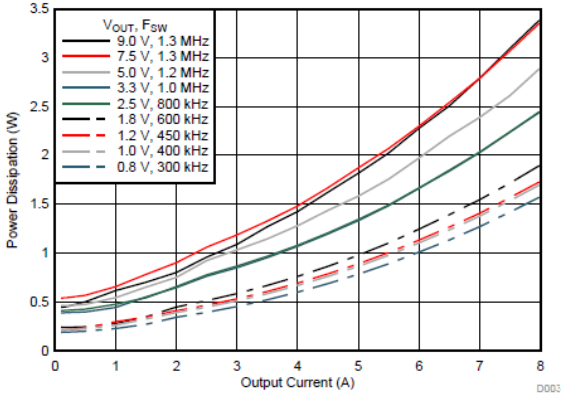
- 40A @ 84C Ta, no airflow
- EVM board results shown with 4 layer, 2 oz copper

5x7 mm Clip QFN
JEDEC θ_{JA} = 28.9°C/W
EVM θ_{JA} = 8.1°C/W

SOA: rough estimation using SOA and θ_{JA}



V_{OUT} = 3.3 V f_{SW} = 1 MHz



TPSM84824 example:

- 12 V_{IN}, 3.3V_{OUT}, 8A, 1 MHz
- T_A = 70°C, no airflow
- θ_{JA} = 12°C/W (4 layer, 2 oz copper-100 mmx100 mm)

Will it work?

- SOA curve inspection passes 70°C T_A with 5°C margin

What temperature will the module heat up to?

- 8 A @ 3.3 V dissipates 2.7W
- 2.7 W x 12°C/W = 32°C temp rise above ambient
- Module junction temperature will be ~102°C

SOA: what does WEBENCH say?

TPSM84824 example:

- $12V_{IN}$, 3.3 V_{OUT}, 8A, 1 MHz
- T_A = 70°C, no airflow
- θ_{JA} = 12°C/W (4 layer, 2 oz copper-100 mmx100 mm)

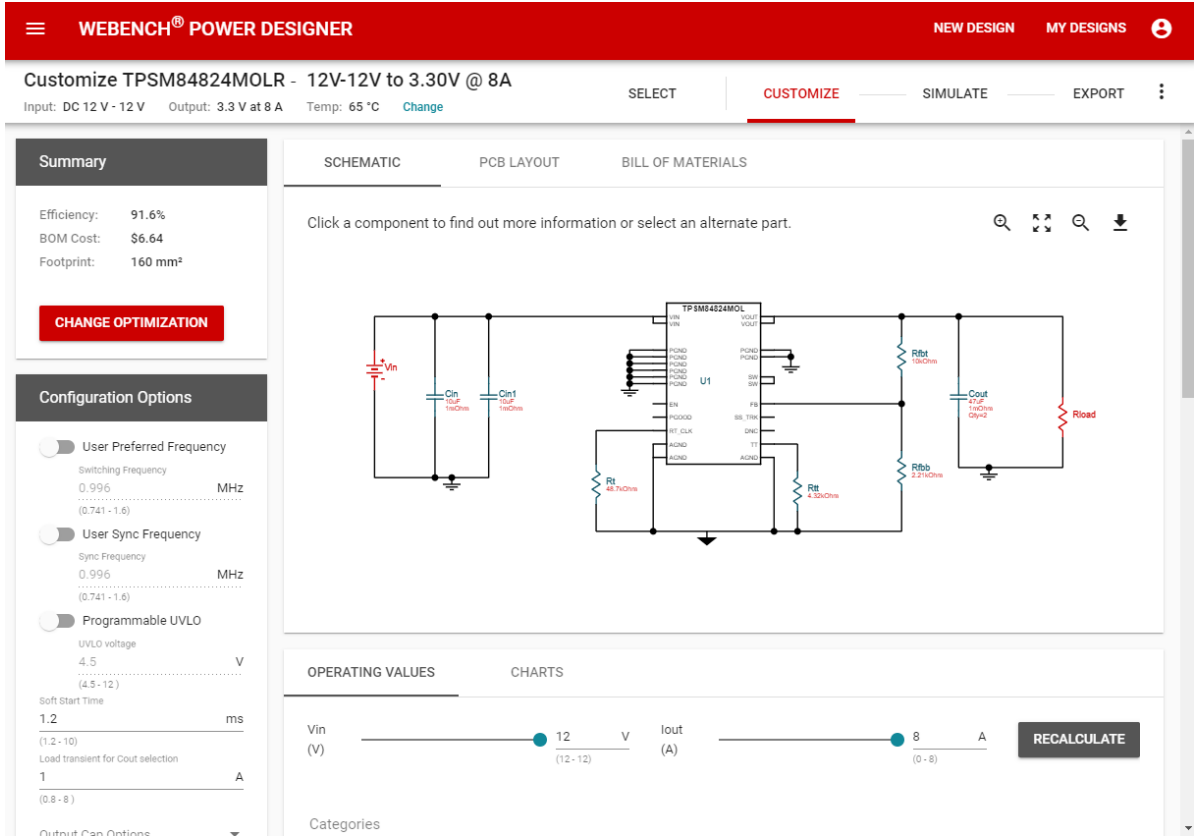
Will it work?

Oh NO!

Let's try 65°C

SUCCESS!

Takeaway, We are very close to the edge with this design.



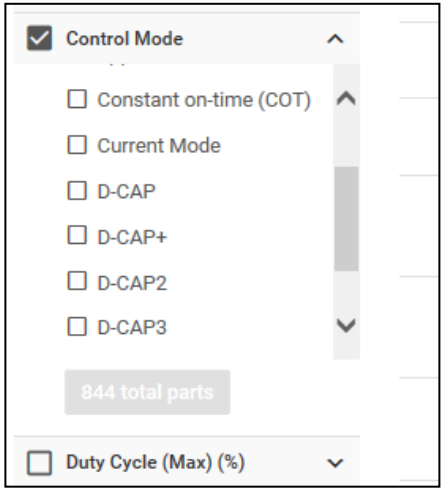
SOA: resources

Application Reports:

- Method of Graphing Safe Operating Area (SOA) Curves for DC-DC Converters
- Understanding the thermal-resistance specification of DC/DC converters with integrated power MOSFETs
- How to Evaluate Junction Temperature Properly with Thermal Metrics
- Improving the Thermal Performance of a MicroSiP™ Power Module

Challenge #5: control mode confusion

There are a lot of control mode architectures to chose!
Which one is best for my application?



2300	0.6	Dynamic Voltage Scaling, Enable, Frequency Synchronization, Light Load Efficiency, Phase Interleaving, Power Good, Synchronous Rectification, UVLO Adjustable	Current Mode
580	0.4	Enable, Synchronous Rectification	D-CAP2
580	0.4	Enable, Light Load Efficiency, Synchronous Rectification	D-CAP2
2000	4.3	Adjustable Current Limit, Enable, Frequency Synchronization, N/A, Over Current Protection, Phase Interleaving, Power Good, Pre-Bias Start-Up, Remote Sense, Synchronous Rectification	Current Mode

Control mode information located in the parametric search.

Control mode: history – buck converters and controllers

Linear control

Voltage mode

- Good noise margin with fixed ramp amplitude
- Higher component count for compensation

Current mode

- Fast response to output current changes
- Fewer components than VM
- Sensitive to current noise

Voltage mode w/ feed forward

- Ramp slope varies with input voltage
- Fast change to input voltage variation
- Higher component count for compensation

Emulated current mode

- Ramp current estimated with sample and hold circuit
- Very small duty cycles w/o current noise susceptibility
- High duty cycles difficult due to S&H blanking time

Internally compensated advanced current mode

- Internally generated ramp to represent inductor current
- No loop compensation required
- Allows wide output capacitance range
- Higher frequency, faster min on-time

Non-linear control

Constant on-time

- Fast transient response
- On-time proportional to input voltage
- No loop compensation
- Jitter. Frequency not fixed

D-CAP

- Fast transient response
- On-time proportional to input and output voltage
- No loop compensation
- Needs ESR capacitance
- Frequency not fixed

D-CAP+

- Fast transient with single Vout multiphase (load line)
- On pulse issued when summed inductor current is lower than desired target
- No loop compensation

D-CAP2

- Fast transient response
- Same as D-CAP but with ripple injection circuit for ceramic output caps
- No loop compensation
- Frequency not fixed
- Offset voltage affects Vref

D-CAP3

- Fast transient response
- Same as D-CAP2 but with sample and hold circuit to reduce injection circuit offset voltage for higher Vref accuracy
- No loop compensation

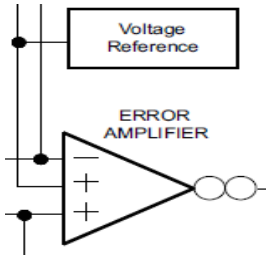
Synchronizable constant on-time

- Fast transient response
- Same as COT, but sync's to external clock during steady state
- Uses Ceramic capacitance
- Low duty cycle, fast minimum on-time
- No loop compensation

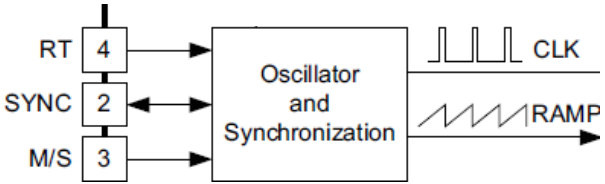
Timeline

Control mode: basic circuit block elements

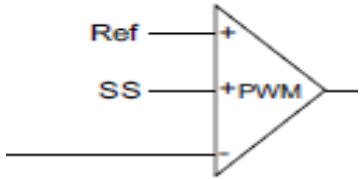
Error amplifier



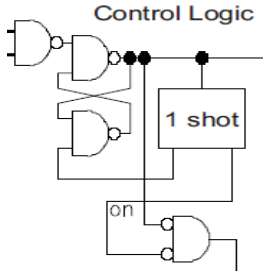
Oscillator



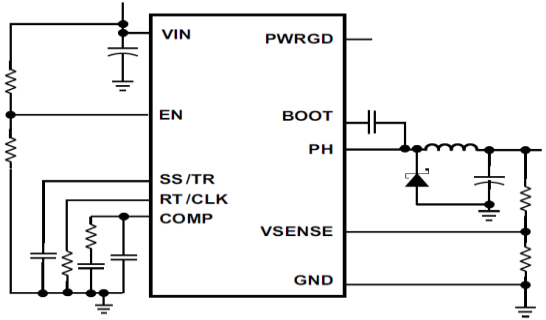
PWM comparator

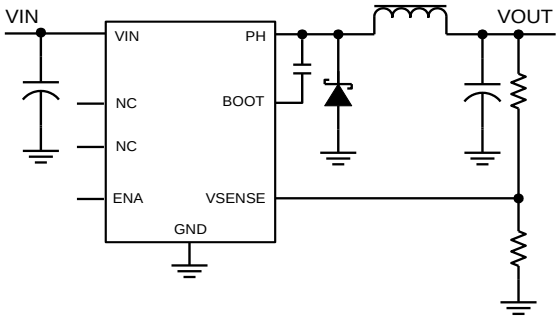


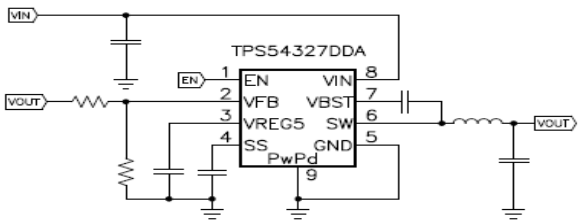
One shot timer



Control mode: internal, external, or no compensation







External compensation

- Control over gain and phase margin.
- Wide selection of filter components.
- Flexible switching frequency.
- Complex small-signal feedback network.

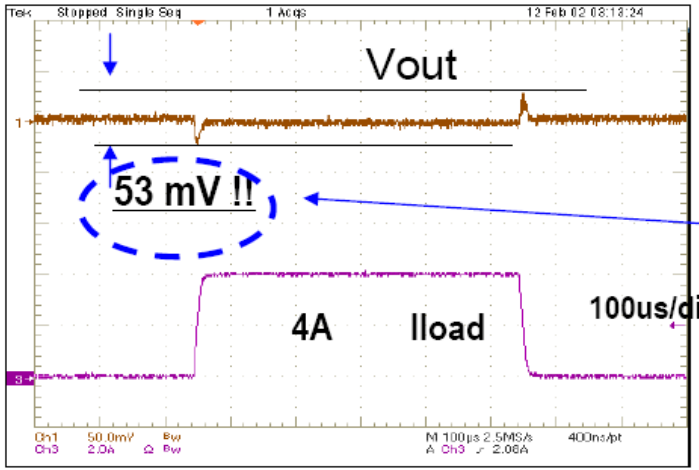
Internal compensation

- Fewer external components.
- Easy design & less verification.
- Limited L & C components.
- Be careful with large number bypass capacitance.

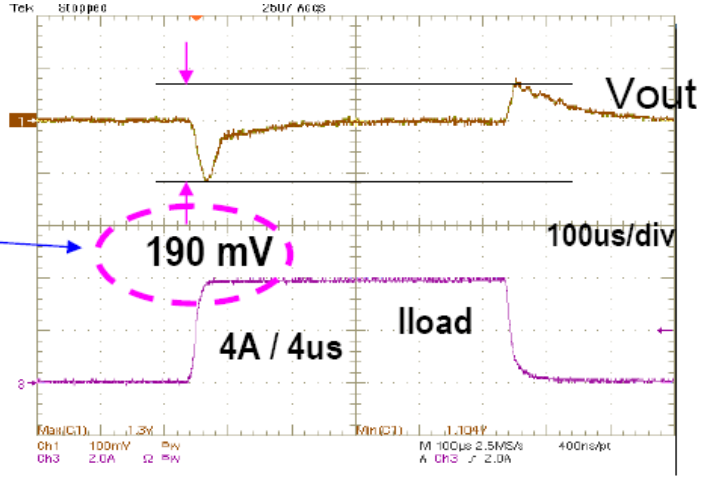
No compensation

- D-CAP versions, DCS or Constant On Time (COT).
- Fast transient response.
- Easy design & less verification.
- Limited L & C components.

Control mode: linear and non-linear transient response



Non-linear D-CAP mode transient response



Linear voltage mode transient response

Cout=22uFx3 ⟷ Cout=100uFx4

Control mode: rules of thumb

Concern	Linear control	Non-linear control
Frequency behavior	Predictable	Not so predictable
Synchronization	With Frequency Sync pin	Not possible over dynamic load condition
Transient response	Typically slower. Needs to wait for clock pulse	Typically faster. No internal clock circuit
Load profile	Signal chain power, noise sensitive PCB area, static load behavior	Higher current, dynamic load conditions. “Moving data around”
Typical market segment	Industrial, Communications, Automotive	Enterprise, Personal Electronics
Customer effort	External compensation needs customer validation effort. Internal compensation limits components	Less customer validation effort. Limits external capacitance selection
External components	Most flexibility with output capacitance with external compensation	Limited flexibility with output capacitance, fewer Cout to meet overshoot/undershoot
Models	Average, Transient	Transient. Average models are difficult
WEBENCH support	Yes. WEBENCH can help compensate	Yes

In some cases, customers don’t understand control mode nuances, but want “easy, or “fewer caps”

Control mode: WEBENCH example

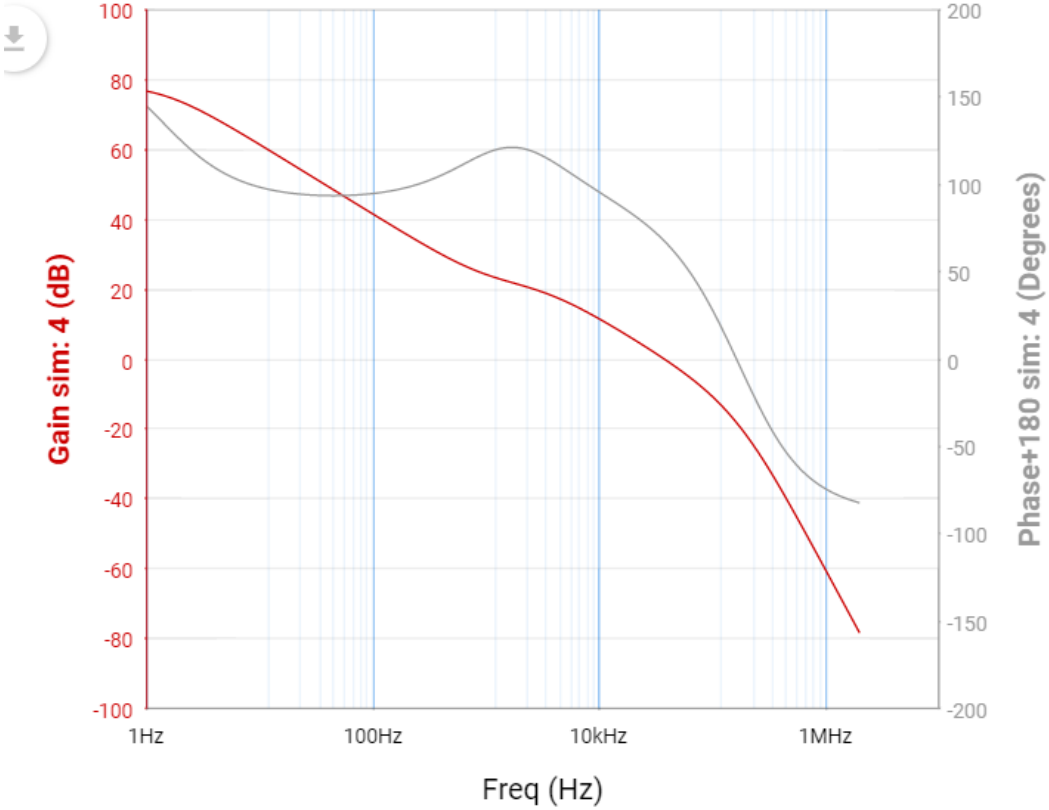
TPS54824 example:

- 12-14 V_{IN}, 1.2 V_{OUT}, 8 A
- Required Inductor from Customer AVL:
  - Coilcraft
  - XAL1010-822MEB
  - 8.2 uH

Original WEBENCH design:

- 1.2 uH Coilcraft
- Switching Freq: 374.6 kHz
- Crossover Freq: 37.5 kHz
- Phase Margin: 67.8 Deg
- Gain Margin: -18.2 dB

All point to good stability.



Control mode: resources

Reference Guides:

- Control-Mode Quick Reference Guide

Application Reports:

- Choosing the Right Fixed-Frequency Buck-Regulator Control Strategy
- Choosing the Right Variable-Frequency Buck-Regulator Control Strategy
- How to Measure the Loop Transfer Function of Power Supplies
- Understanding Frequency Variation in the DCS-Control™ Topology

White Papers:

- Internally Compensated Advanced Current Mode (ACM)

Technical Articles:

- Comparing Internally-compensated Advanced Current Mode (ACM) with D-CAP3™ Control

Remember!

- TI DC/DC solutions and content help customers solve their problems.
- When using Embedded Processing and Signal-Chain products, remember TI DC/DC conversion products address both processor and signal-chain power concerns.
- Use WEBENCH to help understand the trade-offs as well as find working solutions.
- Our factory applications engineers are here to help.
- Check out: The Essential Collection of DC/DC Buck Switching Regulator Technical Documentation.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265