Welcome! Texas Instruments New Product Update

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- Phone lines are muted
- Please post questions in the chat or contact your TI sales contact or field applications engineer



LEARN ABOUT TI'S LEADING POWER DENSITY ICS FOR SPACE GRADE POWER MANAGEMENT

New Product Update

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- Product Marketing Engineer

Agenda

- Space grade product flows
 - Radiation tolerant space enhanced plastic and radiation hardened QML Class V
- Buck converter overview
 - Power density
 - FPGA core rail challenge and paralleling
 - Ease of layout
- LDO regulator overview
 - General purpose LDOs
 - DDR Termination Regulators
 - High performance RF LDO





Space product grades

	Rad Tolerant Plastic	Rad Hard Plastic QML Class P Precursor	Rad Hard Hermetic QML Class V
Packaging	Plastic	Plastic	Ceramic / Metal Can
Mil. Spec	VID	VID/SMD*	SMD
Burnin	No	Yes	Yes
TID Char	30 – 50 krad(Si)	<>	
TID RLAT	20, 30, or 50 krad(Si)	<> Non-RHA, 50, 100, or 300 krad(Si)>	
SEL	43 MeV⋅cm²/mg	l <> <>	



TI's space-grade manufacturing flows

	TI defined Space Enhanced Product (-SEP) flow	MIL-SPEC-38535 defined QML Class-P (-SP) flow	MIL-SPEC-38535 defined QML Class-V (-SP) flow
Part Number	TI defined TPS7HxxxxSEP	5962xxxxxPxx	5962xxxxxVxx
Packaging	Plastic	Plastic	Ceramic-Hermetic
Single Controlled Baseline	Yes	Yes	Yes
Bond Wires	Au	Au	AI
Meets DLA spec for less than 2% Sn	Yes	Yes	Yes
Production Burn-in	No	Yes	Yes
Typical Temperature Range	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
Characterized Radiation Performance	Yes	Yes	Yes
Per lot TID Radiation Lot Acceptance Testing (RLAT)	Yes	Yes	Yes
Outgassing tested per ASTM E595	Yes	Yes	N/A
Lot Level Temp Cycle	Yes	Yes	Yes
Per tube, tray or reel single lot date code	Yes	Yes	Yes
Life Test Per Wafer Lot	No	Yes	Yes
Group reports	Basic PCR report & Group E & P reports	PCR report & Group B, C, D, E, WLA reports	PCR report & Group B, C, D, E, WLA reports



Full space-grade power management solution



Rad-hard hermetically sealed QMLV solution

Rad-tolerant space enhanced plastic solution





Plastic pkg option

Radiation qualified switching regulators





TI Key Benefits | Buck Converters





Power Density (considering pin layout)

(19.3)



TPS7H4001-SP

Package Size with 2.5mm leads: 12.4mm x 12.7mm = 157.5mm²

Power density: 1V_{out} @ Max I_{out} TPS50601A-SP: 38mW/mm² TPS7H4002-SP: 19mW/mm² Package Size with 2.5mm leads: 12.6mm x 21.6mm = 272.2mm²

Power density: $1V_{out} @ Max I_{out}$ 66.1mW/mm² TPS7H4003-SEP



Package Size with leads: 8.1mm x 14mm = 113.4mm²

Power density: $1V_{out}$ @ Max I_{out} 158.7mW/mm²

TPS7H4010-SEP

Package Size (leadless): 4mm x 6mm = 24mm²

Power density: $1V_{out} @ Max I_{out}$ 250mW/mm²



Evolution of Core Power Rails





Achieving higher current





Ease of Layout with example

Ease of Layout (Bucks)

- Designed with flow through in mind
- Smaller loops to minimize switching noise and parasitics
- Power node (PH) grouped together on one side (ideal layout to LC filter)







Released

Plastic pkg option

Space qualified linear regulators



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TI Key Benefits | LDO

Existing Solutions

General Purpose / High current

TPS7H1111-SP/-SEP

Made for noise sensitive applications (DACs, ADCs, Clock)



TPS7H3302-SEP

Power Dissipation and Data Integrity via DDR termination



Existing solutions for noise sensitive rails





Double Data Rate (DDR) Termination LDO

TPS7H3302-SEP

Summary: Radiation-tolerant 3 A source-sink DDR termination regulator in a plastic package

Use Case:

- VLDO input down to 0.8 V
- •10 mA Buffered VTTREF
- Source/Sink VTT voltage output with drop compensation

Design Benefits:

- Compact Power solution: no inductor \ nor compensation needed
- Only a few passives are required for operation





Powering DDR1 – DDR4

- VDDQ supplied externally by buck regulator
- TPS7H3302-SEP VTT output able to sink and source current
- Supports the multiple spec differences to power DDR, DDR2, DDR3, DDR3L, and DDR4
- VTTSNS pin for remote sensing and more accurate regulation
- Internal resistor dividers to generate VTTREF







Noise sensitive application LDO

TPS7H1111-SEP

Summary: 0.85 V – 7 V VIN, 2.2 V – 14 V VBIAS, 1.5 A, RF, LDO

Use Case: Low Noise and High PSSR

-VCOs (voltage controlled oscillators)

-Data Converters: ADCs and DACs (analog-to digital and digital-to-analog converters)

-PLLs (phase-lock-loops), SerDes (serializer and deserializers), Imaging sensors

-Accurate supply for precision ASIC and FPGA supply rails

Design Benefits:

Highly integrated features (programable soft start) Low output voltage Enhanced Noise and PSRR performance (helping eliminate need for external filters)





Comparison performance over frequency for leading LP-SP LDOs



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Example of creating an ultra-clean rail





Getting started

You can start evaluating this device leveraging the following:

Content type	Content title	Link to content or more details
Selection Guide	TI Space Products Guide	https://www.ti.com/lit/sg/slyt532i/slyt532i.pdf
Application Note	Reduce the Risk in Low-Earth Orbit Missions with Space Enhanced Plastic Products	https://www.ti.com/lit/an/sboa344a/sboa344a.pdf
Whitepaper	Powering a New Era of High-Performance Space-Grade Xilinx FGPAs	https://www.ti.com/lit/wp/slvaf47/slvaf47.pdf
Application Note	TI Space Rated Power Solution for Microsemi® RTG4™ FPGA	https://www.ti.com/lit/an/slva857b/slva857b.pdf



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