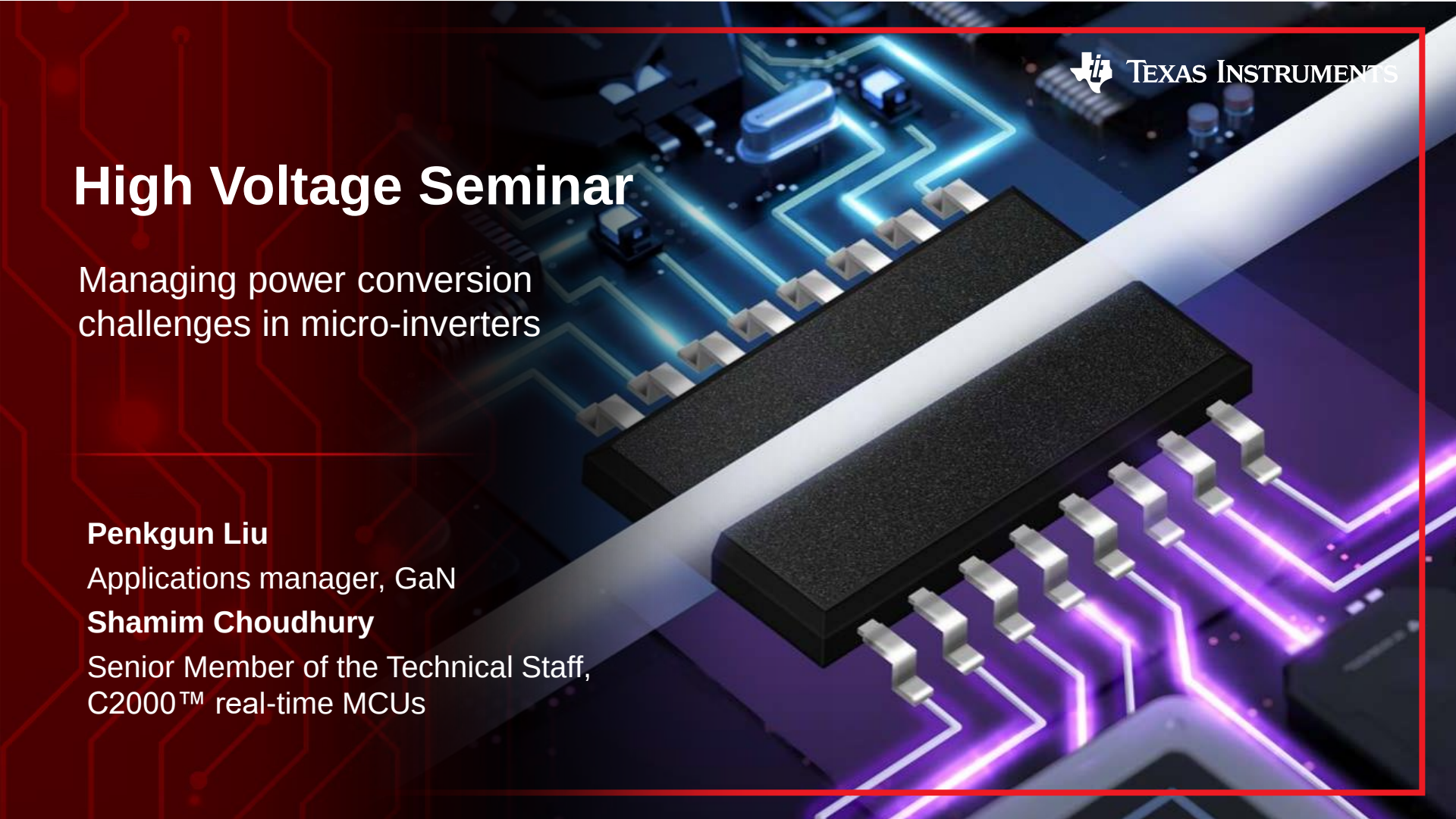
High Voltage Seminar

Managing power conversion challenges in micro-inverters



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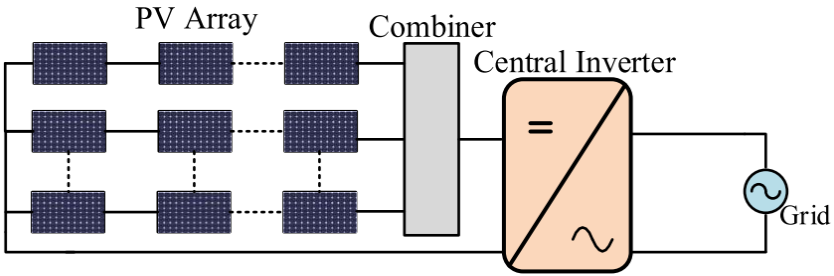
Agenda

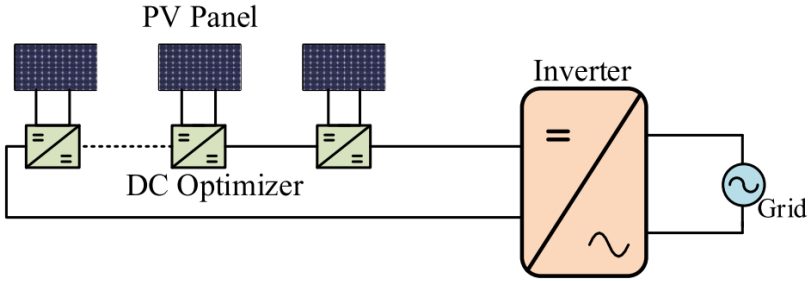
- Introduction: Micro inverters
- GaN in micro inverters:
  - Benefits of GaN in H-bridges
  - Comparisons between AC/DC in PV applications
- Challenges in micro inverter control:
  - MPPT stage
  - Inverter stage
  - Power line communication

Solar energy system

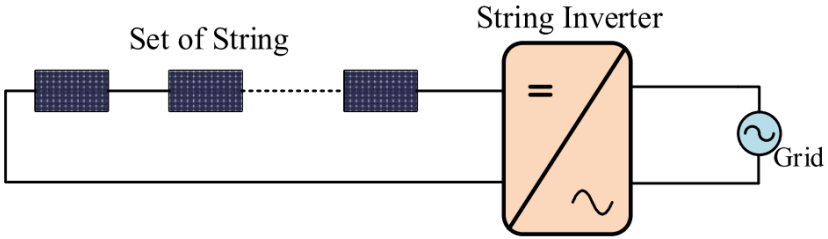
- Central inverter system



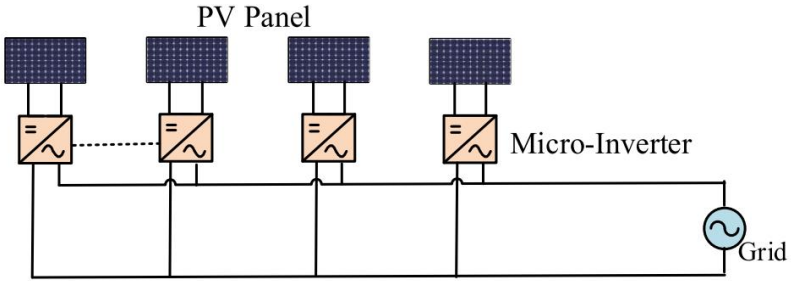
- DC optimizer system



- String inverter system

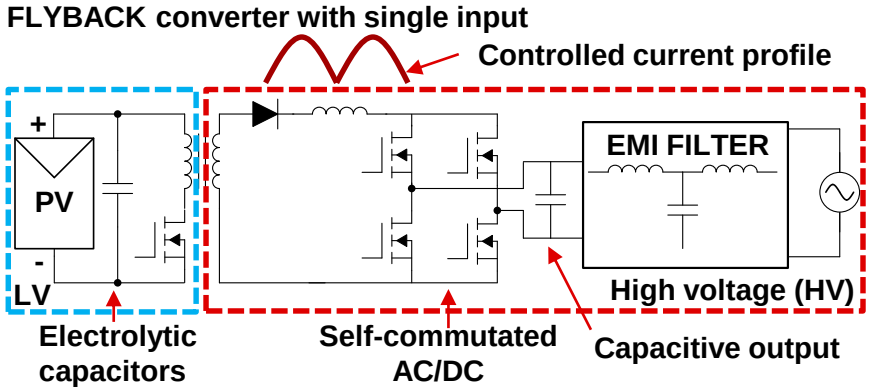


- Microinverter system



Overview | Micro inverter

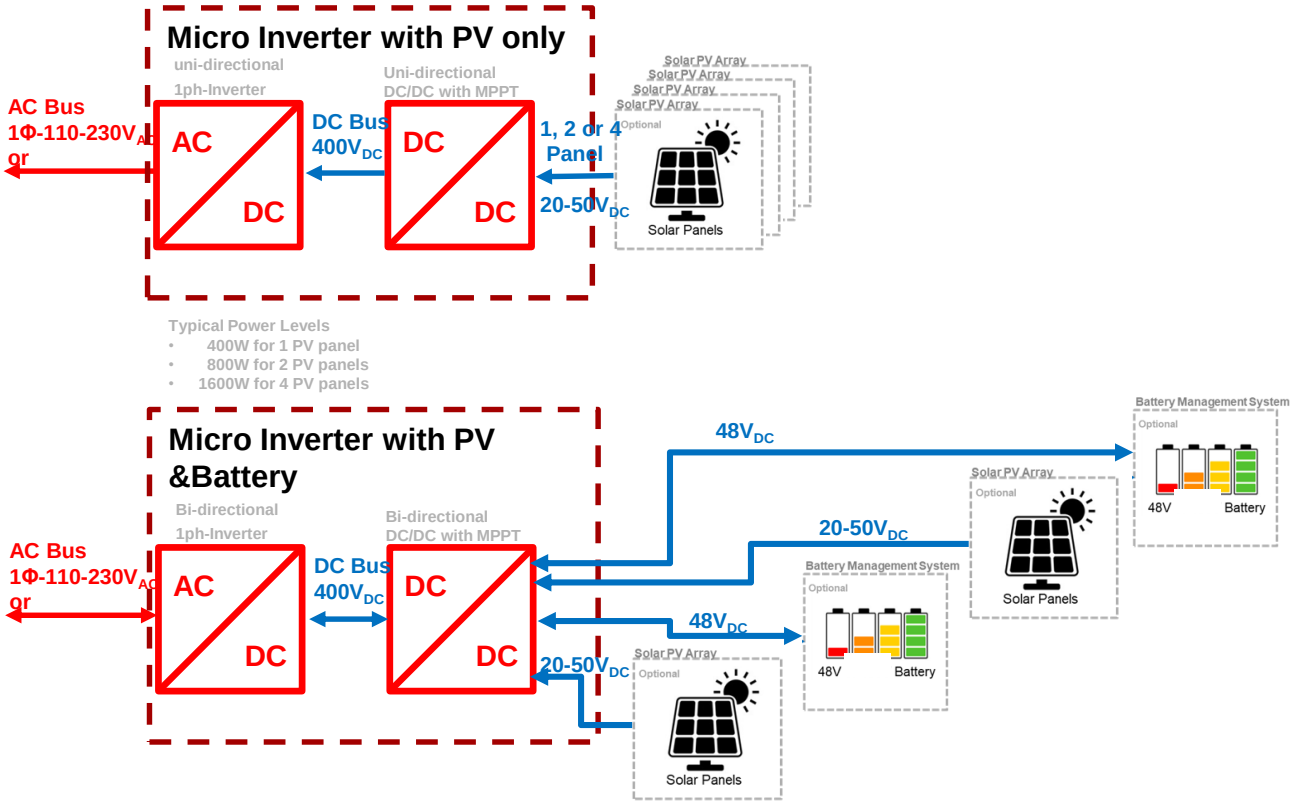
- Micro inverters are in general able to target powers up to **2 kW** by connecting up to 4 PV panels per EE.
- Reasons to use a **transformer**:
  - Galvanic isolation;
  - no Residual Current Detection (RCD);
  - Transformer on the DCDC cheaper and smaller with respect to AC/DC;
  - Parasitic capacitances of PVs are complete decoupled from the grid;
- Pros and cons of a micro inverter:
  - MPPT per panel
  - Higher total cost per kW.



- Self-commutating AC/DC composed of low-speed devices.
- Ripple power compensated at the low voltage side.
- MCU ground referred to PV (-).

[1] Design and Control of an Inverter for Photovoltaic Applications "Kjær, Søren Bækhøj"

Overview | Micro inverter configurations

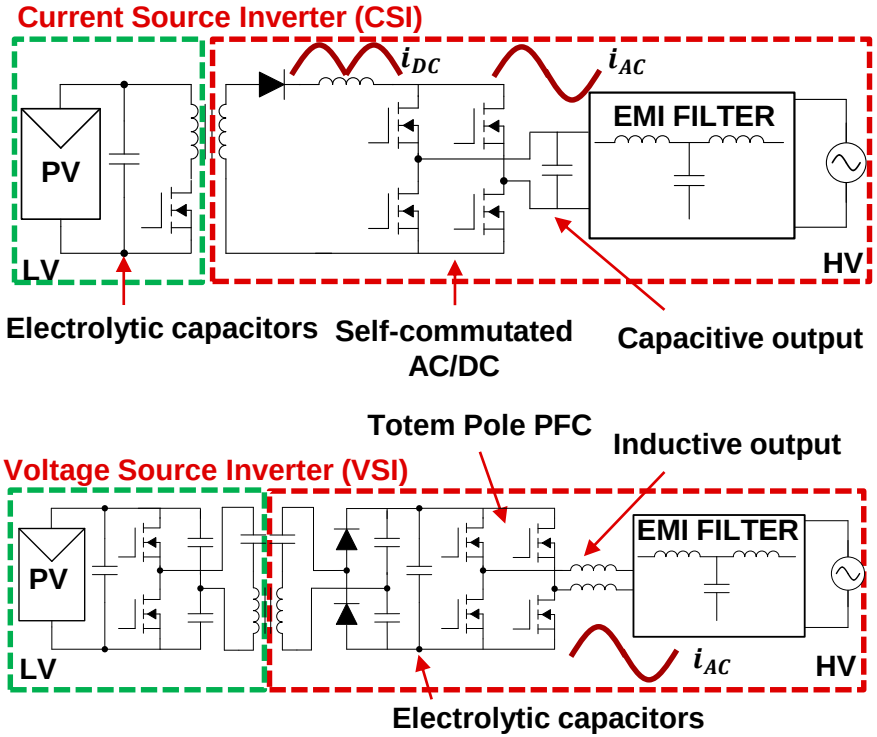


Overview | Micro inverter topologies

Micro inverter can be found as current source inverter (CSI) or voltage source inverter (VSI)

- AC/DC converter:
  - When used with a DC/DC controller as a current source inverter **(CSI)** is a self commutated AC/DC.
  - When used with a system having a DC link a standard bidirectional AC/DC converter **(VSI).**
- DC/DC converter:
  - Flyback, active flyback, Push-pull transformer, LLC converter.

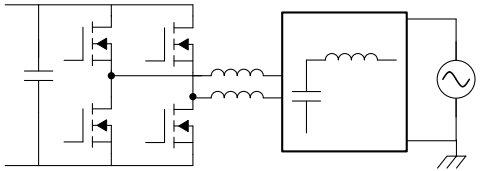
VSI enables the addition of energy storage.



AC/DC topologies in PV applications

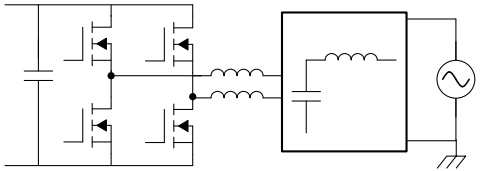
- Most common topologies used in voltage source inverters are the following:

H-Bridge



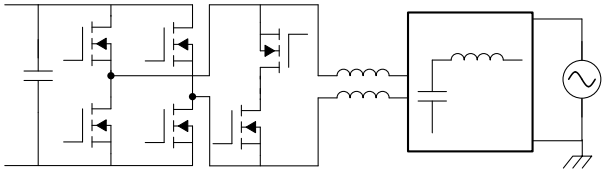
- Switches of the same family:
  - UNIPOLAR Switching technique
  - BIPOLAR Switching technique

Totem Pole AC/DC



- Hybrid topology, where Si and WBG technologies can be adopted.

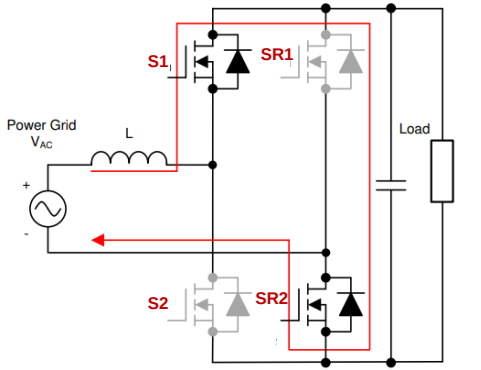
Highly Efficient and Reliable Inverter Concept (HERIC)



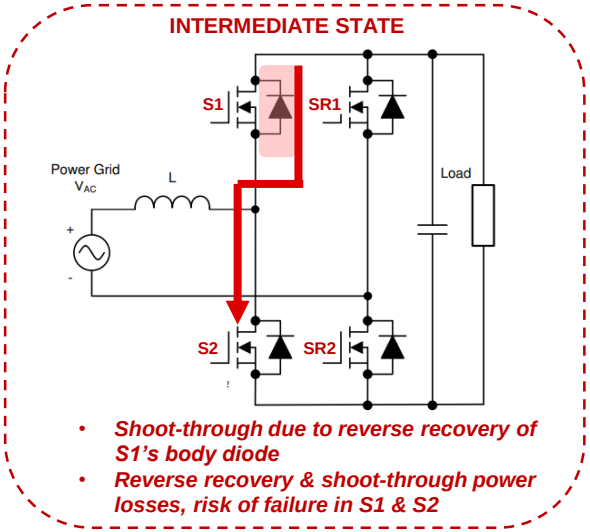
- Two additional switches;
- Converter still not adopt widely due to IP royalties;
- Patent going to expire in 2026 for US and 2030 for EU.

[4] HERIC Patent Infos

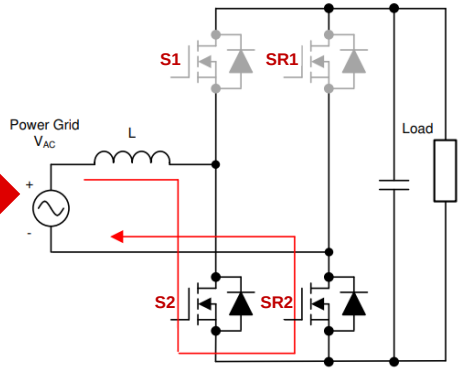
Why Si MOSFETs are not suitable for H-Bridge



- *S1 – on, reverse conduction*
- *S2 – off*



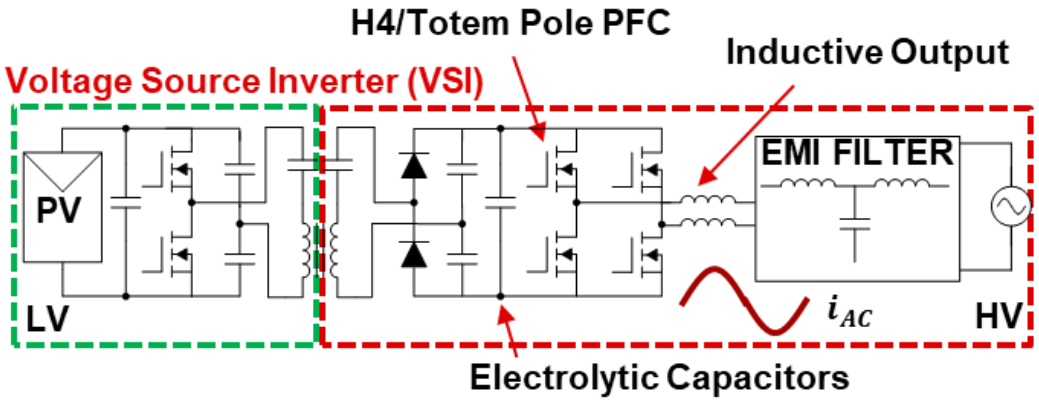
- *Shoot-through due to reverse recovery of S1's body diode*
- *Reverse recovery & shoot-through power losses, risk of failure in S1 & S2*



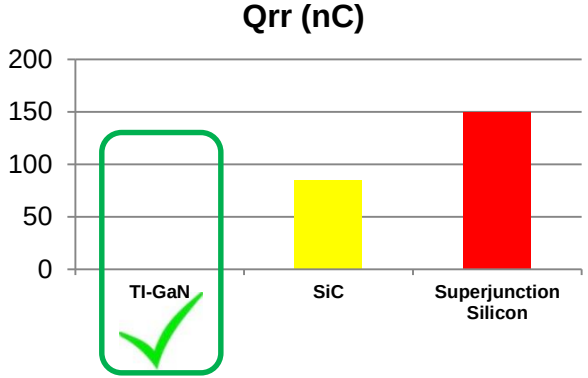
- *S1 – off*
- *S2 – on, forward conduction*

- CCM symmetrical bridge FETs ➔ Must have zero or very low reverse recovery.
- If using Si MOSFETs/IGBTs, the switching frequency is limited (< 20kHz) or use CRM operation instead.

Why GaN is the best power FET for H-Bridge

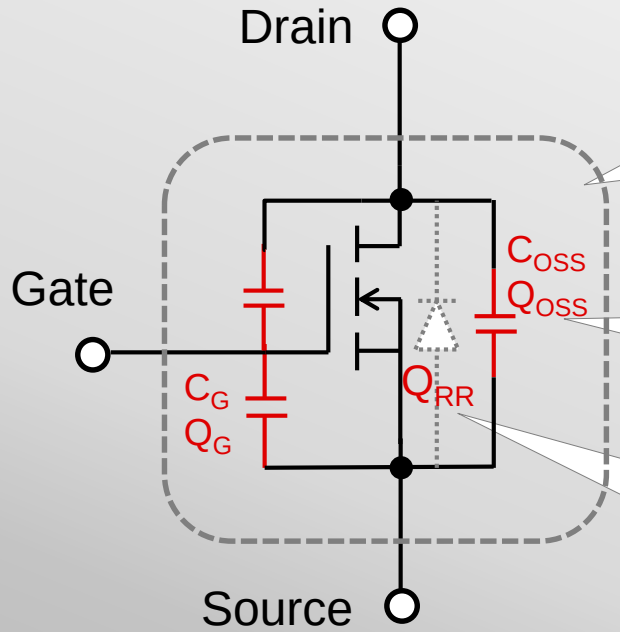


Zero reverse recovery in **Direct-drive** TI GaN



- CCM symmetrical bridge FETs ➔ Must have zero or very low reverse recovery
- Best power switch in high-power (CCM) H-bridge/totem-pole inverter
  - GaN FETs = no body diode, zero reverse recovery, zero power loss ➔ Best fit
  - Si MOSFETs = body diode has high reverse recovery, high power loss ➔ Not suitable
  - SiC MOSFETs = body diode has some reverse recovery, some power loss ➔ Acceptable

GaN devices | Key advantages



Low C_G,Q_G gate capacitance/charge (1 nC-Ω vs Si 4 nC-Ω)

- ✓ faster turn-on and turn-off, higher switching speed
- ✓ reduced gate drive losses

Low C_{OSS},Q_{OSS} output capacitance/charge (5 nC-Ω vs Si 25 nC-Ω)

- ✓ faster switching, high switching frequencies
- ✓ reduced switching losses

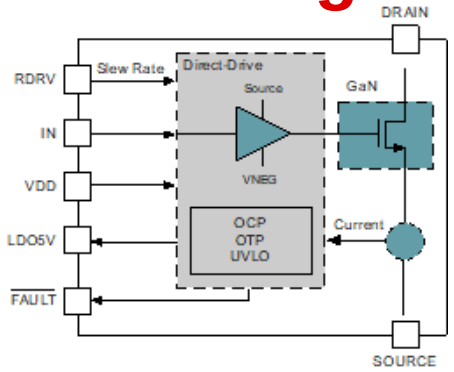
Low R_{DSON} (5 mΩ-cm^2 vs Si >10 mΩ-cm^2)

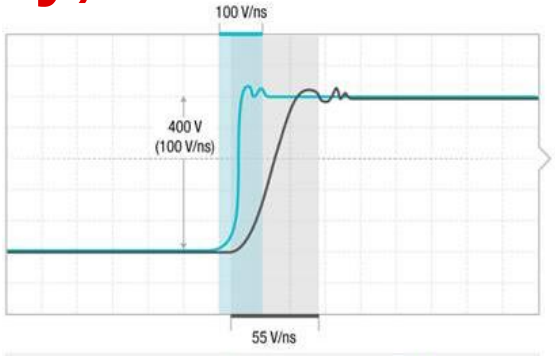
- ✓ lower conduction losses

Zero Q_{RR} No ‘body diode’

- ✓ No reverse recovery losses
- ✓ Reduces ringing on switch node and EMI

TI GaN engineered for high-frequency, robustness





Integrated GaN FET, gate driver & more

- <1 nH common source inductance, <4 nH gate loop inductance
- on-chip V/I/T sensing, protections & reporting
- advanced power management features

+

Compact SMD package

- low parasitic lead inductance
- enhanced thermal management with top/bottom-side cooling

=

Design simplicity & confidence

- demonstrated dV_{DS}/dt capability of 150 V/ns
- dV_{DS}/dt adjustable between 30-150 V/ns for EMI vs efficiency
- compact PCB footprint

Comparisons between AC/DC in PV applications

- Topology comparison between:
  - H-Bridge Unipolar, H-Bridge Bipolar, Totem-Pole and HERIC.
- GaN vs. SiC vs. IGBT Technologies;
- 3.6 kW power limit coming from GaN TI Portfolio.

Allowable Power Dissipation 68 W

- **4 W → housekeeping (MCU, DCDCs)**
- **7 W → Power Ripple (electrolytic, caps)**
- **16 W → Passive Components (Inductors, etc.)**
- **40 W → Power Components (Switches)**

	Value
Maximum input DC voltage	500 V
Nominal DC input voltage	400 V
Nominal DC Current	9 A
Rated output voltage	230 V
Rated output power	3.6 kW
Efficiency at Peak Power	98.2 %
Power factor	± Active ± Reactive
Ambient Temperature Range	-40~+60°C
Cooling	Static Cooling
Heatsink Thermal Resistance	0.6 °C/W
THD	< 5%
DC link voltage ripple	+- 20 V
DC link capacitance value	720 uF

Comparisons between AC/DC in PV applications

IGBT:
(650 V, Ic = 40 A)
TO-247-3

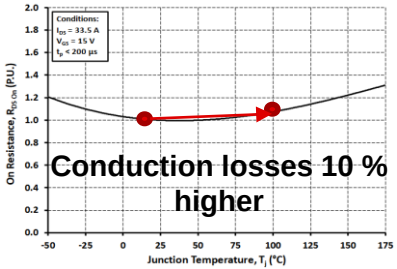
$R_{OFF} = R_{ON} = 7\ \Omega$
$t_r = 15\ ns\ ;\ t_f = 70\ ns\ ;$

- Cheap IGBT but external diode required;
- Important variation of switching and conduction losses vs. temperature due to reverse recovery and tail current;

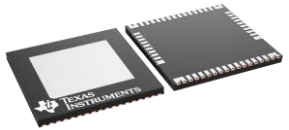
SiC:
(650 V, 25 mΩ)
TO-247-4

$R_{OFF} = 5\ \Omega\ R_{ON} = 7\ \Omega$
$t_r = 30\ ns\ ;\ t_f = 12\ ns;$

- When temperature of the SiC device changes there is no important variation in Rds.

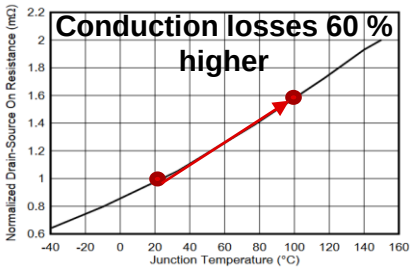


GaN: LMG3522R030
(650 V, 30 mΩ)
Top Side Cooled Devices

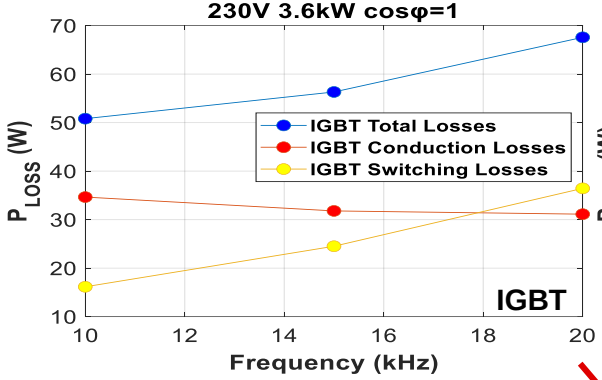


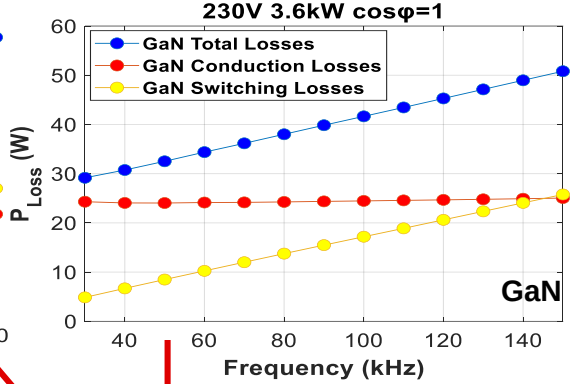
$dV/dT = 100\ V/ns$
$t_r = 4\ ns\ ;\ t_f = 12\ ns;$

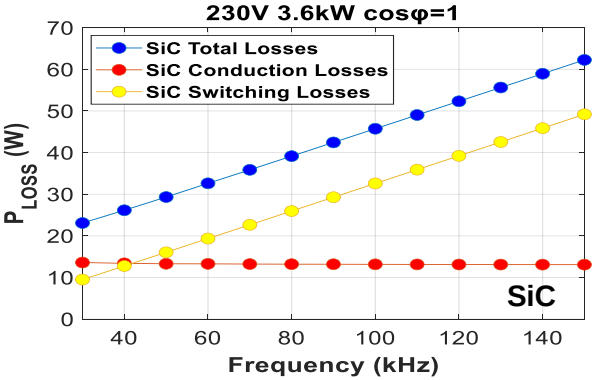
- When temperature of the GaN device changes there is important variation in Rds.

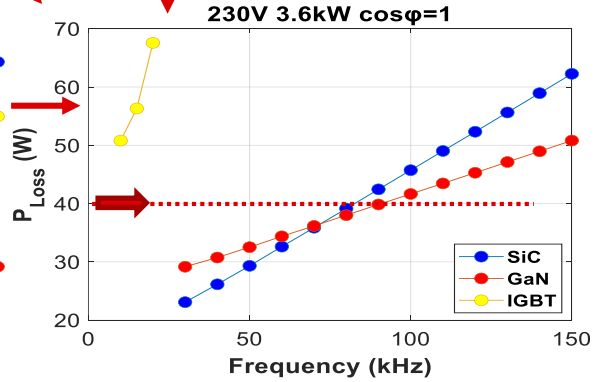


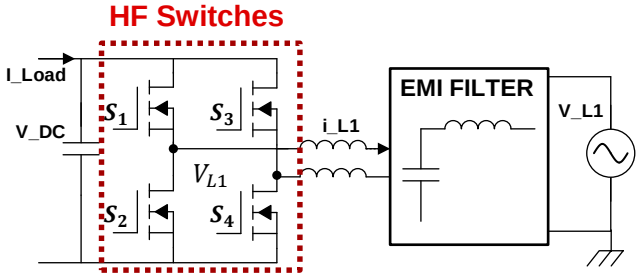
H-Bridge unipolar PWM | Losses





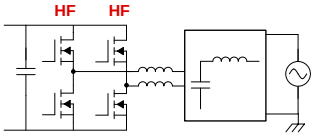


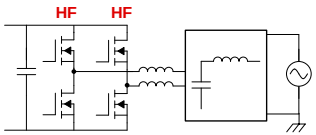


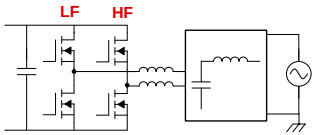


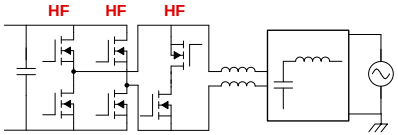
- Switching frequency sweep in order to find out the right switching frequency;
- Higher conduction losses of GaN with respect to SiC;
- **40 W** total power for targe η:
  - IGBT $f_{sw} < 10\ kHz$;
  - SiC $f_{sw} < 82\ kHz$;
  - GaN $f_{sw} < 90\ kHz$.

Topology comparisons









		Unipolar H-Bridge (3-Level)	Bipolar H-Bridge (2-Level)	Totem-Pole (3-Level)	HERIC (3-Level)
SiC	f_{sw}	70 kHz	78 kHz	100 kHz	80 kHz
	η_{CEC}	98.1 %	98 %	98.4 %	98.2 %
	ΔL	- 72 %	**1 P.U.***	- 61 %	- 51 %
GaN	f_{sw}	70 kHz	95 kHz	120 kHz	90 kHz
	η_{CEC}	98.44 %	98.54 %	98.6 %	98.5 %
	ΔL	- 72 %	- 18 %	- 68 %	- 57 %

$$\eta_{CEC} = 0.03 * \eta_{5\%} + 0.06 * \eta_{10\%} + 0.13 * \eta_{20\%} + 0.1 * \eta_{30\%} + 0.48 * \eta_{50\%} + 0.2 * \eta_{100\%}$$

*** Inductance needed with respect to the reference point, e.g. In this case, the needed inductance is 72 % smaller;**

Thermal difference with PSU

- PSU market
  - Fan

- Micro inverter
  - No Fan
  - TIM + heatsink + GEL

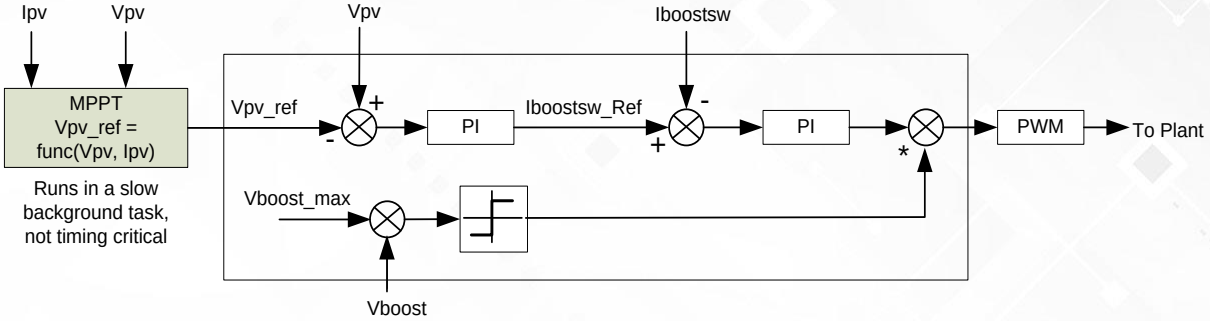
Constant
Input
Output

	Configuration 1	Configuration 2		
Configuration	CCM Totem Pole	CCM Totem Pole		
Select FET	LMG3422R050	LMG3411R070		
Select # of phase legs	1	1		
$R_{DS,ON}$	55	90	mΩ	(maximum)
$R_{th,\ junction\ to\ case}$	0.4	0.5	C/W	
E_{on}	41	24	uJ	(at zero current)
E_{off}	0.05	7.00	uJ	
AC $V_{IN,\ RMS}$	220	220	V	*min: 50, max: 350*
DC V_{OUT}	400	400	V	*min: 300, max: 450*
Switching Frequency	100	100	kHz	*max: 2,200*
Deadtime	100	100	ns	*min: 50*
Ambient Temperature	55	55	C	*min: 25, max: 100*
Junction Temperature (T_j)	125	125	C	min: T_{amb}
Slew Rate	100	50	V/ns	*min: 30, max: 100, 150*
Max Output Power	600	600	W	*min: 300, max: 7000*
$R_{th,\ case\ to\ ambient}$	26.918	32.108	C/W	
$R_{th,\ junction\ to\ ambient}$	**27.318**	**32.608**	C/W	
R_{DS,ON_temp}	0.099	0.144	Ω	
Device Conduction Power Loss	0.383	0.558	W	(per device)
Device Coss Power Loss	1.932	1.100	W	(per device)
Overlap Power Loss	0.136	0.379	W	(per device)
Deadtime Loss	0.055	0.084	W	(per device)
Driver Loss	0.056	0.026	W	(per device)
Total Loss per Device	**2.562**	**2.147**	W	
Input RMS Current	2.783	2.783	A	
Device Average Current	1.253	1.253	A	

Challenges in micro inverter control

- **Grid current with low THD** – high bandwidth control loop – fast digital control loop
- **High efficiency and high power density** - advanced power topologies - flexible PWM generation**,** high frequency PWM, low latency fast and high frequency digital control loop.
- **Maximum Power Point Tracking (MPPT)** from the panel - maximizes the returns from installation. Requires small ripple across PV module(s) to operate around MPP without fluctuation.
- **Accurate estimation of grid phase** - Inverter output current (phase & frequency) locked to fundamental grid voltage – allows low THD, high PF current injection into grid. Also enables reactive power control (power factor -0.9 to +0.9).
- **Decouple Power -** Driving AC load from PV (DC) source causes power ripple. For PV to operate at MPP it must be free from this ripple. A decoupling capacitor is, therefore, used as power storage element. Electrolyte free decoupling is desired for higher reliability.
- **Power Line Communication** - Microinverters and gateway communication via AC lines.

DC/DC MPPT boost control

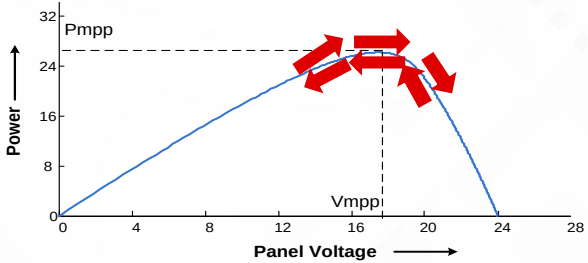


- Input panel current I_{pv} & panel voltage V_{pv} are sensed to estimate the power. Sensed signals are fed to the MPPT algorithm which provides a reference for the panel voltage.
- Input voltage regulation is achieved using two control loops:
    1. **Outer loop for input voltage regulation**: MPP provides a reference for the panel voltage. This outer loop modulates the current reference, thus modulating the current through the boost stage. The PV voltage changes according to the current drawn. Boost stage maintains the panel volt at the reference MPP level.
    2. **Inner current loop**: Controls the closed loop current for the boost stage to maintain the loading of the panel.
- The output voltage of the boost stage is not controlled – however OVP is implemented using an internal comparator and cycle-by-cycle trip feature of the control MCU. The downstream inverter is operated to transfer all the energy from the boost output to the grid and prevent any overvoltage.

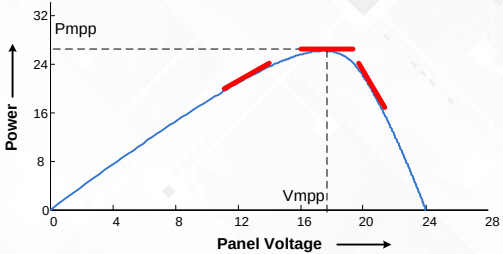
MPPT algorithms

Perturb & Observe (PnO)

- Panel volt ref is continually perturbed and the change in power observed. Perturbation that leads to increase in power is rewarded, otherwise the direction is reversed.
- Under stable condition, the panel voltage will oscillate slightly about the MPP point.



Perturb & Observe (PnO)



Incremental Conductance (INCC)

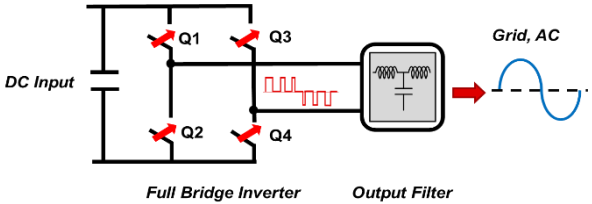
Incremental Conductance (INCC)

- The slope of PV panel power curve is zero at the MPP, positive on the left of the MPP, and negative on the right of the MPP. The incremental conductance algorithm works by moving the operating point to the right or left depending on the measured slope.
- The control MCU implementing the INCC algorithm smoothly maintains the operation at MPP unless a change in ΔI occurs (e.g. a change in atmospheric conditions).

$$\frac{dP}{dV} = \frac{d(IV)}{dV} = I + V\frac{dI}{dV} \cong I + V\frac{\Delta I}{\Delta V}$$

Inverter stage

- The inverter stage generates a clean sinusoidal waveform and connects to the grid.
- The full bridge inverter generates a high frequency sinusoidal waveform which is then filtered by the output filter to generate the 60/50Hz AC waveform.



- LCL filter is commonly used to attenuate the harmonics in grid connected application
- One way to solve the LCL resonance issue is to use an adaptive 4th order notch filter
- Tuning and connecting to the grid remains challenging issue. A software based integrated frequency response analyzer (SFRA) greatly simplifies the process of tuning.

PWM configuration in micro inverter

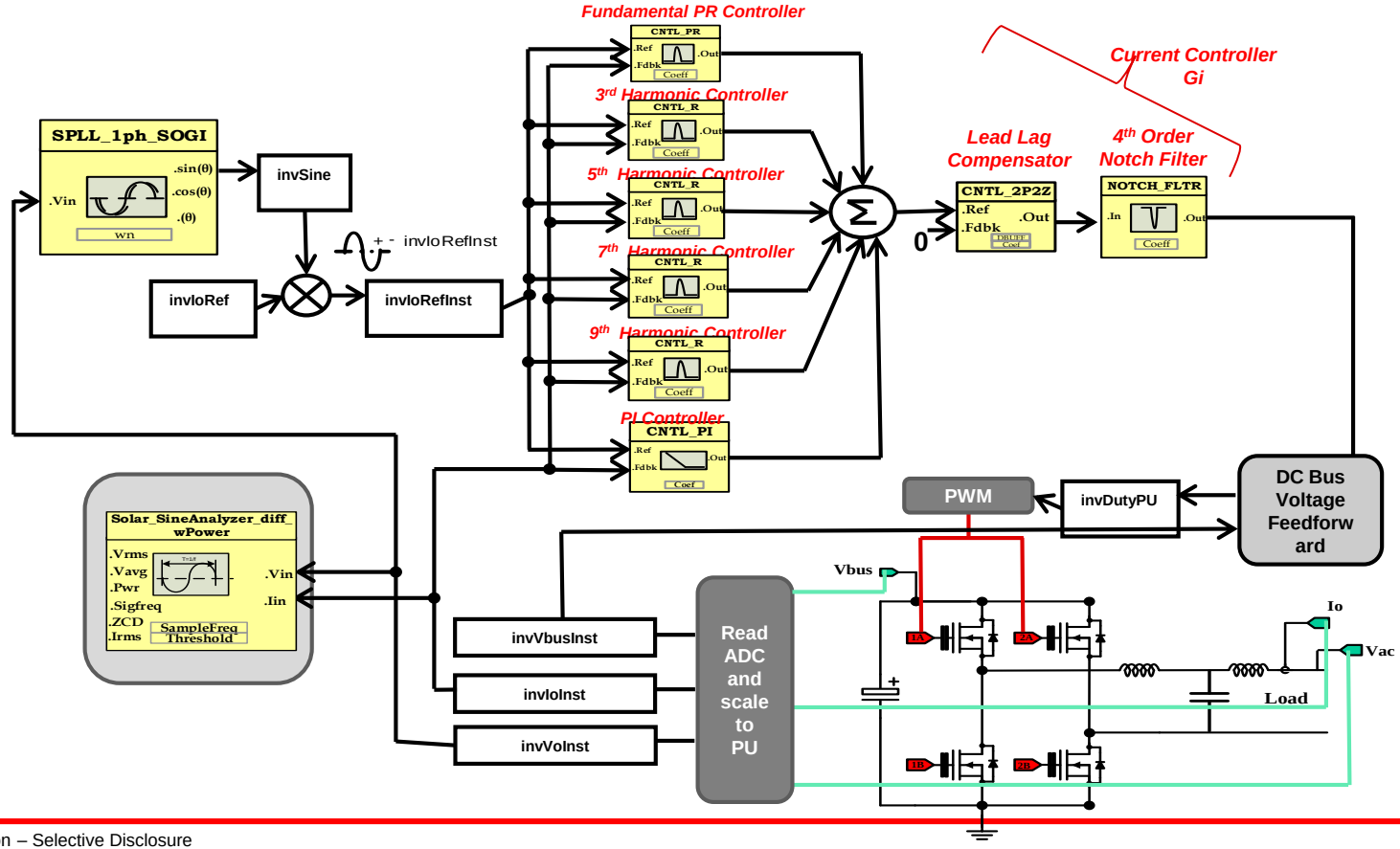
PWM techniques used in PV microinverter - two major categories.

In the first, PWM control is applied to both dc–dc and inverter stage. A constant voltage dc link decouples the power flow in the two stages such that the dc input is not affected by the double-line-frequency power ripple appearing at the ac side.

The second PWM configuration utilizes a quasi-sinusoidal PWM method to control the dc–dc, generates a rectified sine current (or voltage) at the inverter dc link. Then, a line-frequency-commutated inverter unfolds the rectified current (or voltage) to obtain the sinusoidal signal synchronized with grid.

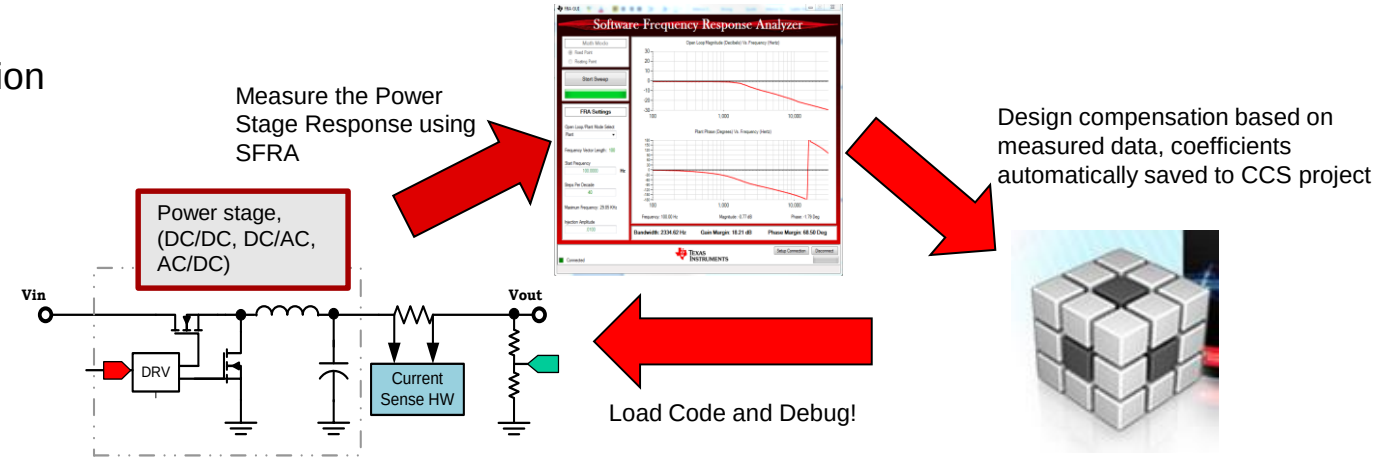
The latter has no HF switching losses and so higher conversion efficiency. However, the double line-frequency power ripple must be all absorbed by the dc input capacitor, making the MPPT efficiency (ratio of energy drawn by inverter within a certain period at steady state to the theoretical available energy from the panel) compromised unless a very large capacitance is used. Moreover, the inverter requires challenging control techniques to meet grid current requirements.
Therefore, in terms of the MPPT performance and current quality, the first category is more appropriate.

Inverter stage control | Example one



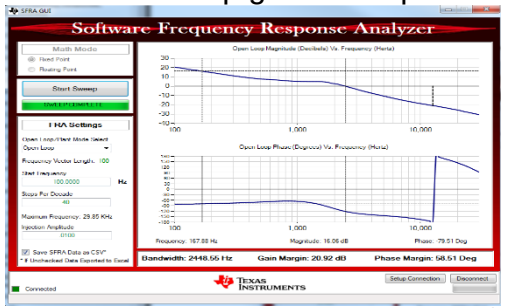
Control loop design verification with SFRA

Tune the solution

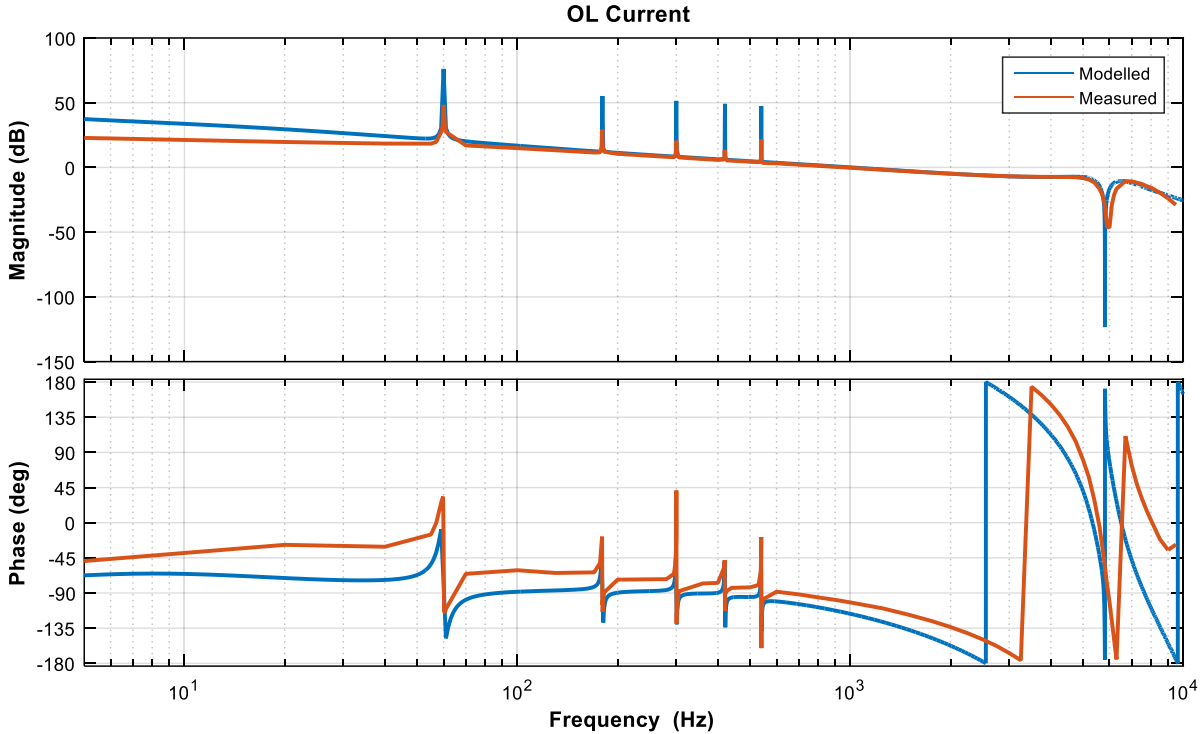


- Eliminates external frequency response analyzer and uses software frequency response analyzer (SFRA) integrated with the power converter control code.
- Requires fast MCU and accelerators, such as, Trigonometric Math Unit (TMU).
- Tune control loop parameters in software while running the application.
- Faster design of stable controller/compensator based on measured response.

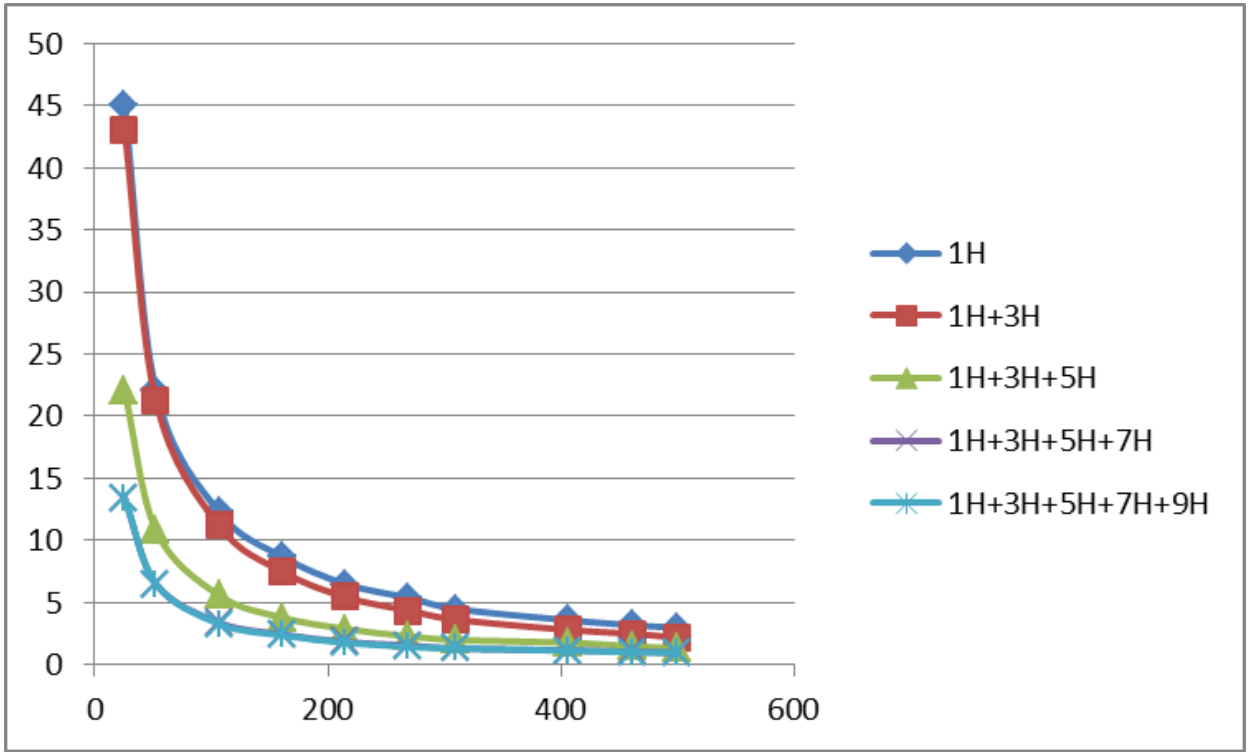
Loop gain Bode plot



Measured Vs modelled frequency response for grid connected operation

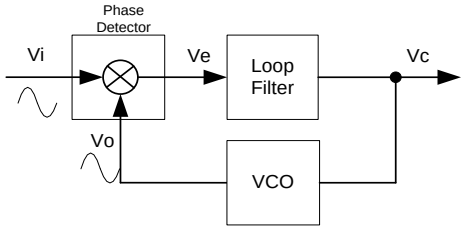


THD vs power with different harmonic controllers

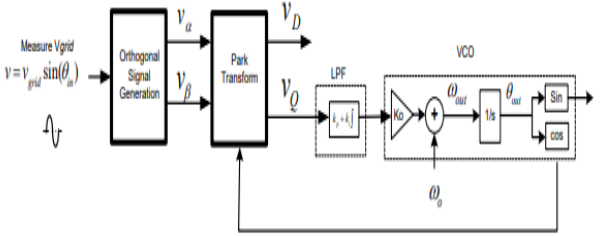


Inverter phase locked loop

- A grid-connected solar inverter must work in harmony with the grid. Inverter internal oscillator is phase and frequency locked to fundamental grid voltage for maximum power transfer.
- For C2000 MCU, eCAP module can be used for grid frequency detection (line volt zero cross detect).

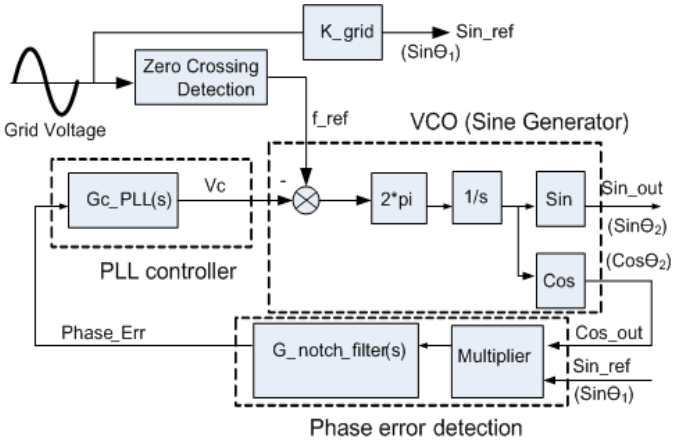


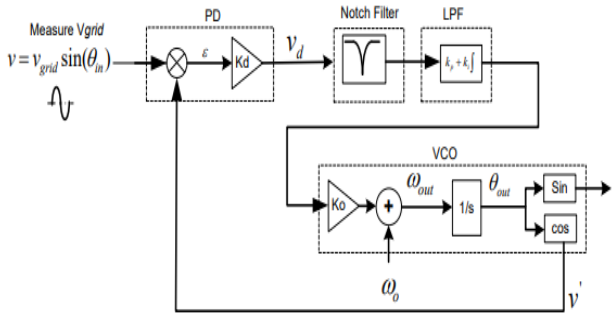
Grid volt Vi is sensed to extract the instantaneous sin angle θg , which is known as the phase lock loop.



- Phase Detector (PD) - output (Ve) proportional to phase difference between its two inputs (Vi & Vo).
- Loop Filter(LPF) - filters high frequency AC from PD. Typically this is a 1st order LPF or PI controller.
- Voltage Controlled Oscillator(VCO) - generates AC signal, frequency varies with output of loop filter.
- Other type of PLL uses orthogonal signal generator and then park transform to use synchronous reference frame for single phase application. Such PLL consists of a PD using orthogonal signal generator and park transform, a LPF and a VCO.

PLL equations





Multiplier output: $\cos(\omega_2 t+\varphi_2)\sin(\omega_1 t+\varphi_1)\approx\frac{1}{2}\sin[2\omega_2 t+(\varphi_1+\varphi_2)]+\frac{1}{2}(\varphi_1-\varphi_2)$

Using ω1= ω2 ,
and Sinβ≈β when β is small

Phase error: $\Delta\theta=(\omega_1 t+\varphi_1)-(\omega_2 t+\varphi_2)=(\omega_1-\omega_2)t+(\varphi_1-\varphi_2)\approx\Delta\varphi_0$

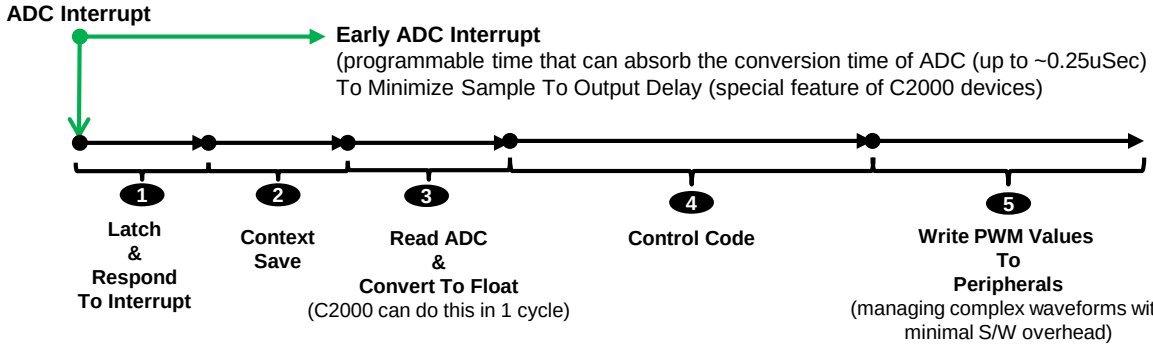
Small signal change in phase: $\tilde{\theta}(t)=\tilde{\omega}t+\Delta\varphi_0$

$$\frac{d\tilde{\theta}(t)}{dt}=\tilde{\omega}\qquad\frac{\tilde{\theta}(s)}{\tilde{f}(s)}=\frac{2\pi}{s}$$

MCU resource usage & digital control performance

- **50KHz Interrupt** runs
  - 7 Compensators, 1 Notch Filter 4th Order and Software PLL for Grid Sync,
  - ADC and PWM software driver routines, SFRA and SineAnalyzer
- Cycles use for control loop :1500 cycles i.e. **35%** CPU utilization on **200MHz** TMS320F28377S MCU **when control ISR runs at 50kHz**

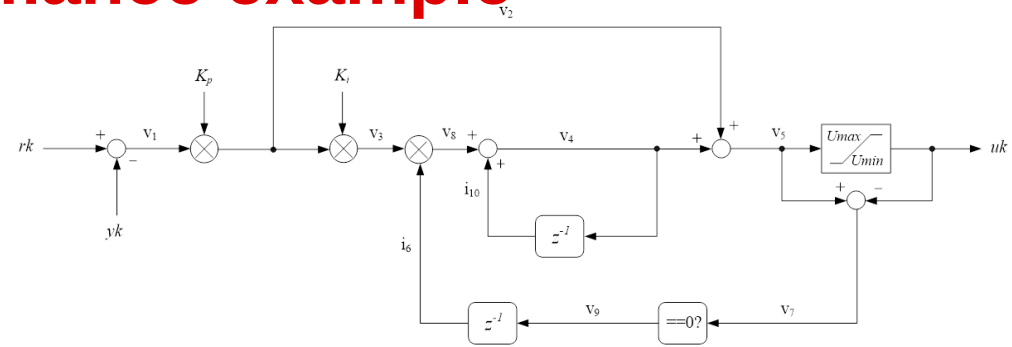
Signal chain performance



Benchmark	C28 execution @200MHz	R5F/M7 execution @400MHz	R5F/M7 execution @800MHz
Phase 4	Reference (1.0)	~2.2x	~4.4x
Signal Chain (Phase 1 to 5)	Reference (1.0)	~1.0x	~1.7x

The True Performance Takes Into Account The Whole Signal Chain.

PID performance example

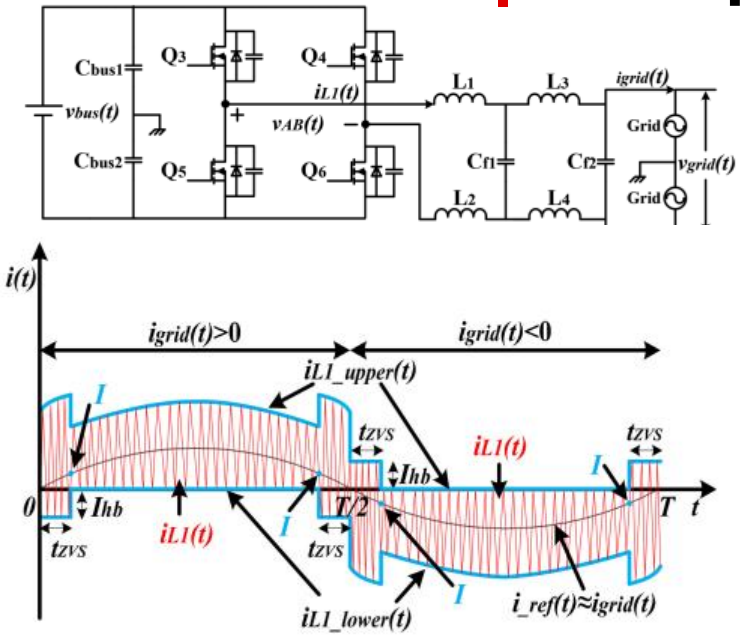


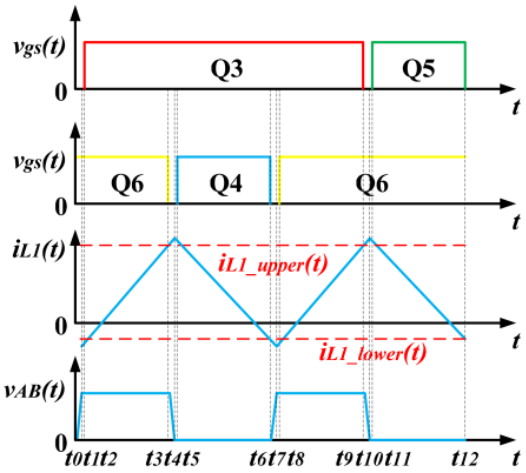
PID Benchmark	C28 Cycles	M7 Cycles
Cycles	39	64
Execute (uS)	0.195	0.160
	@200MHz	@400MHz

C28 Bytes	M7 Bytes
132	172

Device	CPU Clock (MHz)	ADC Clock (MHz)	CPU HW INT (cycles)	ADC with DMA	ADC INT Response [ADC sampling + CPU HW INT + Compiler context save] (cycles)
TI C2000 C28	200	50	14	No (INT – 1st chan sampling complete)	**57** (10.6% of total cycles 537) (57 cycles = 0.285 usec at 200MHz)
Cortex-M7	480	50	12	Yes (INT – DMA half full)	**198** (17.3% of total cycles 1143) (198 cycles = 0.412 usec at 480MHz)

Solar micro inverter | Example 2

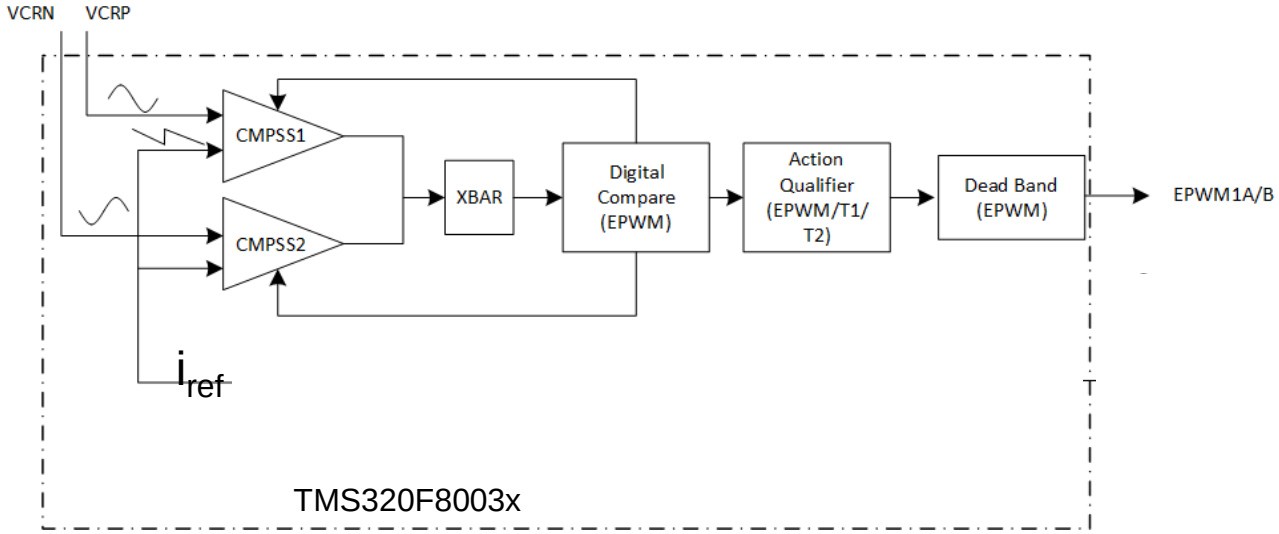




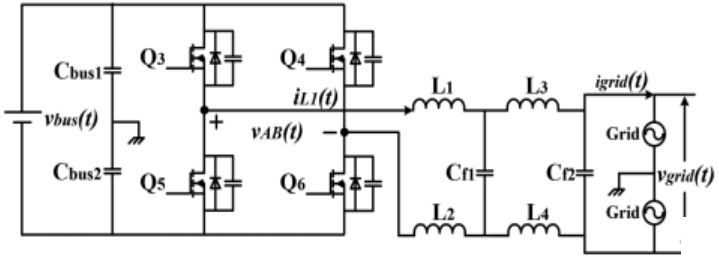
"Hybrid hysteresis current control and low frequency current harmonics mitigation based on proportional resonant in dc/ac inverter" – H. Zhang, X. Li, S. Xiao, R. Balog, Texas A&M University, College Station, USA

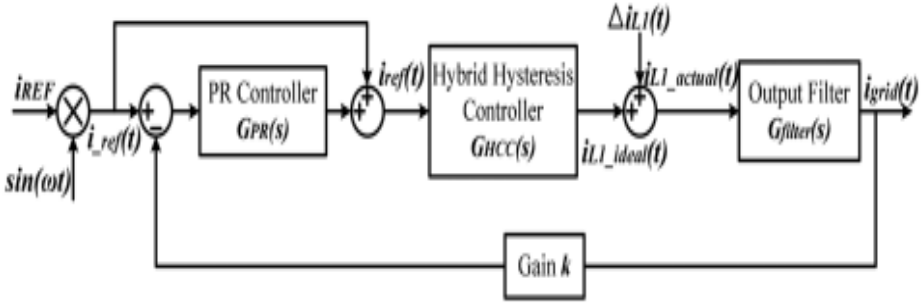
- Hysteresis current control with soft switching achieves fast dynamic response, robust current regulation and high efficiency even with higher switching frequency;
- Hybrid modulation (bipolar modulation around zero-crossing points and unipolar modulation in other moments during the AC line period) minimizes the zero-crossing distortion, reduces switching frequency by 50% without increasing the output inductance;
- PR control minimizes the steady-state error at low frequency and mitigate the low-frequency harmonics

Hybrid Hysteretic Control (HHC) using C2000 MCU



Solar micro inverter | Example 2 cont

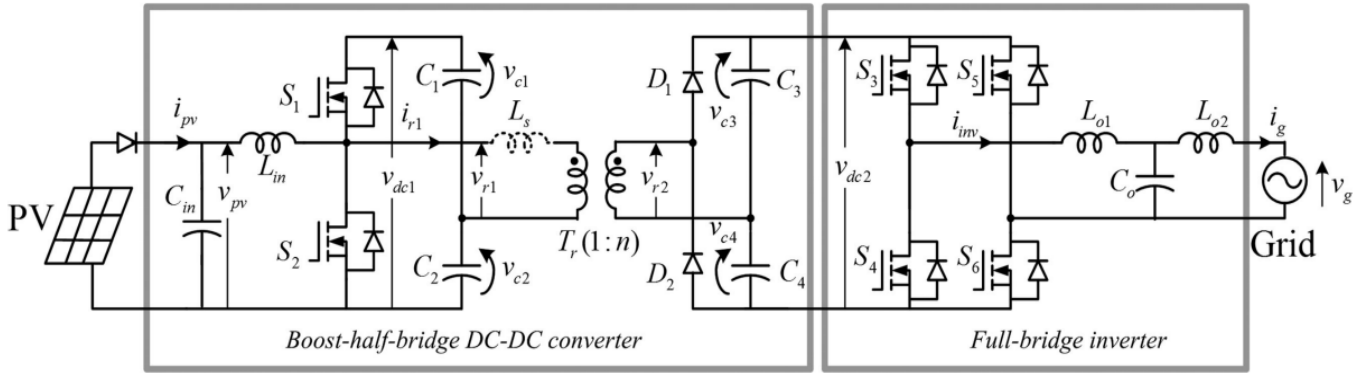


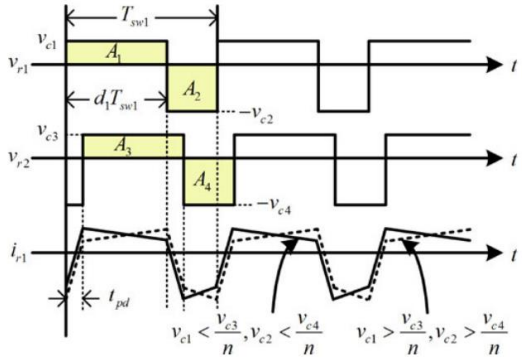


Hybrid hysteresis current control and PR control

"Hybrid hysteresis current control and low frequency current harmonics mitigation based on proportional resonant in dc/ac inverter" - Haiyu Zhang , Xiao Li , Shunlong Xiao , Robert S. Balog, Department of Electrical & Computer Engineering, Texas A&M University, College Station, USA

Solar micro inverter | Example 3





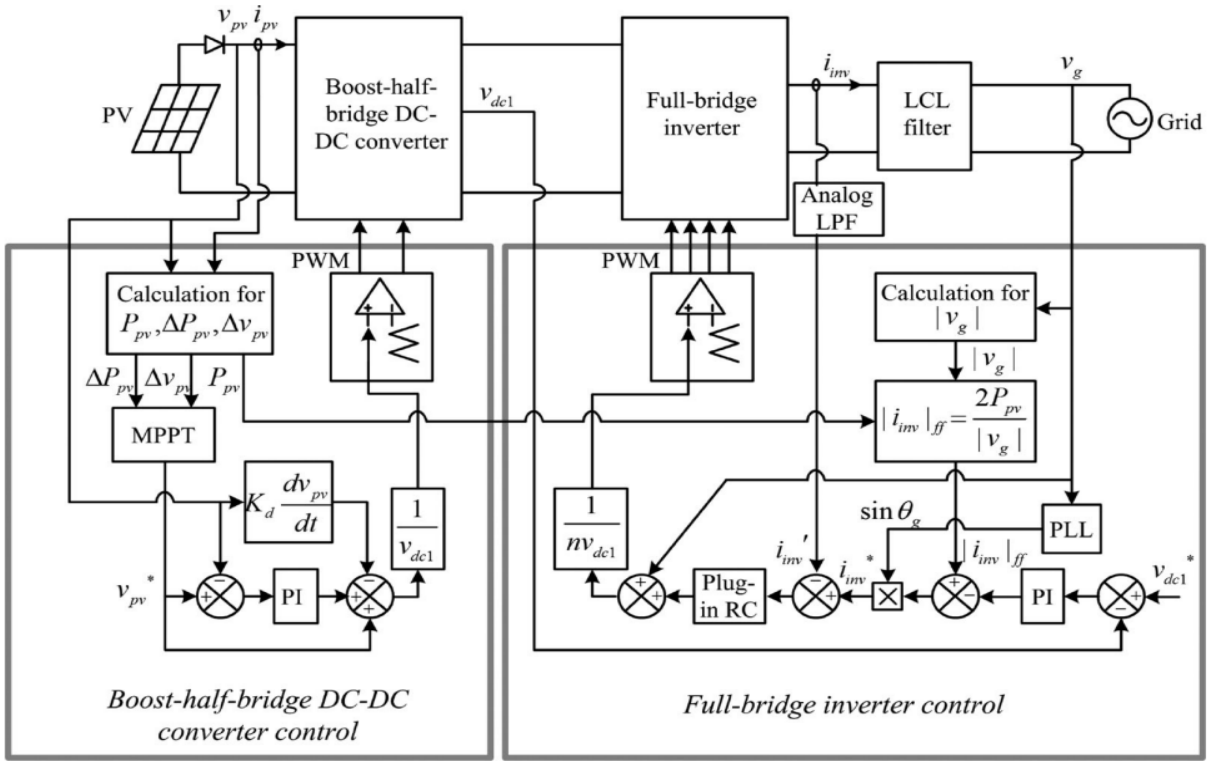
Boost-half-bridge converter used as the MPPT dc–dc stage.

Benefits - circuit simplicity, ease of control, and minimal semiconductor devices.

Low cost, high efficiency, and high reliability.

"Grid-Connected Boost-Half-Bridge Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking" - Shuai Jiang, Student Member, IEEE, Dong Cao, Student Member, IEEE, Yuan Li, Member, IEEE, and Fang Zheng Peng, Fellow, IEEE

Solar micro inverter | Example 3 cont



Current reference feedforward, based on input PV power P_{PV} is added for fast dynamic responses of the grid current as well as the dc-link voltage,

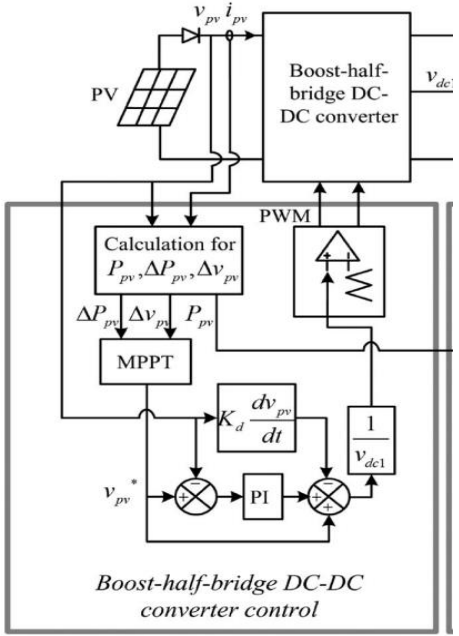
"Grid-Connected Boost-Half-Bridge Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking" - Shuai Jiang, Dong Cao, Yuan Li and Fang Zheng Peng.

Solar micro inverter | Example 3 – MPPT stage control

Different techniques have shown different steady-state MPPT efficiency and transient tracking speed.

High bandwidth PI control is adopted to track the voltage reference v^*_{PV} and to minimize the double-line-frequency disturbance from the LVS dc link.

The capacitor voltage differential feedback is introduced for active damping of the input LC resonance



"Grid-Connected Boost-Half-Bridge Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking" - Shuai Jiang, Dong Cao, Yuan Li and Fang Zheng Peng.

Solar micro inverter | Example 3 – MPPT stage control cont

Dynamics of MPPT converter influences the converter efficiency and functioning.
For ex, MPPT using step-changed perturbations may cause inrush current, LC oscillation, magnetic saturation, etc - result in higher power losses, circuit malfunctioning.

MPPT producing a ramp-changed PV volt performs well considering the dynamics of boost-HB converter.
Also, for the purpose of fast tracking and high MPPT efficiency, the power–voltage (P–V) curve is divided into three different zones, where the MPPT step size is varied accordingly.

MPPT using Step-changed volt ref and ramp-changed volt ref are implemented and compared (Figure). Transformer dc flux linkage (λm) averages to zero with 2x line-frequency ripple for constant PV volt.

Oscillation of λm occurs when PV voltage is perturbed by the MPPT.

For MPPT step size of 0.3 V and voltage ramp time of 75 ms (trp), the ramp-changed volt reference help reduces λm oscillation.

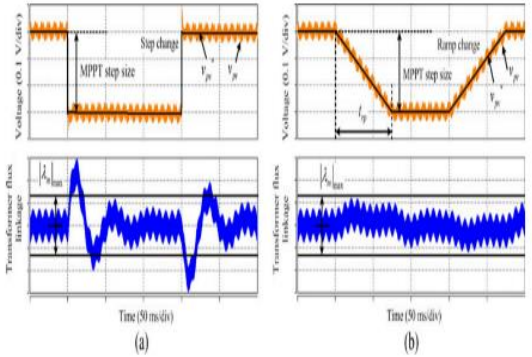
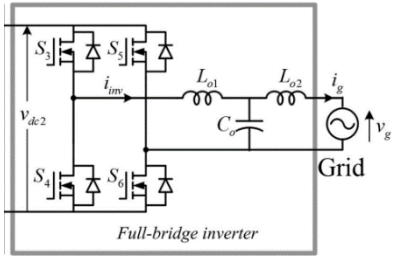
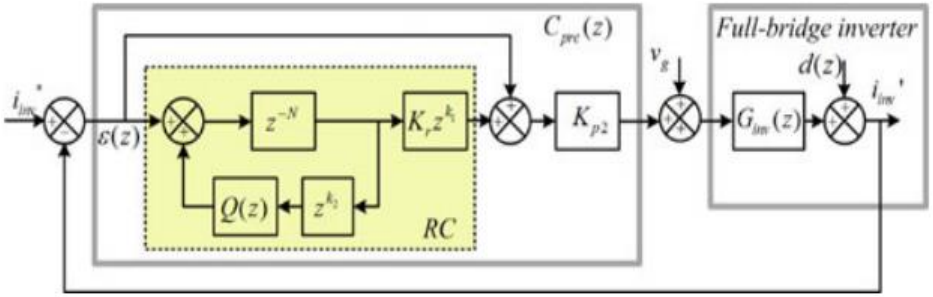


Fig. 10. Dynamic responses corresponding to the different voltage reference generation methods in the MPPT. (a) Using a step-changed voltage reference. (b) Using a ramp-changed voltage reference.

"Grid-Connected Boost-Half-Bridge Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking" - Shuai Jiang, Dong Cao, Yuan Li and Fang Zheng Peng.

Solar micro inverter | Example 3 – inverter stage control





Block diagram of the proposed plug-in repetitive controller.

d(z) is the repetitive disturbances.

phase lead compensators zk1, zk2

Full-bridge PWM inverter with LCL output filter.

Repetitive control (RC) is an effective solution for elimination of periodic harmonic errors.
A RC control with 4th order linear-phase IIR filter Q(z) has been implemented to obtain very high loop gains at a large number of harmonics for enhanced harmonic rejection. Linear-phase FIR filter achieves higher performance, but requires higher filter order and, so, a faster MCU.

This paper uses a plug-in repetitive current controller consisting of a proportional part (Kp2) and a RC part.
The current controller implements 1) high PF; 2) low current THD (up to the 13th-order); 3) outstanding current regulation within a wide range of load conditions; 4) and fast dynamic response during load transients and/or solar irradiance change.

"Grid-Connected Boost-HB Photovoltaic Microinverter System Using Repetitive Current Control and Maximum Power Point Tracking" - Shuai Jiang, Dong Cao, Yuan Li and Fang Z Peng.

Power decoupling

- AC side load power has DC and AC components.

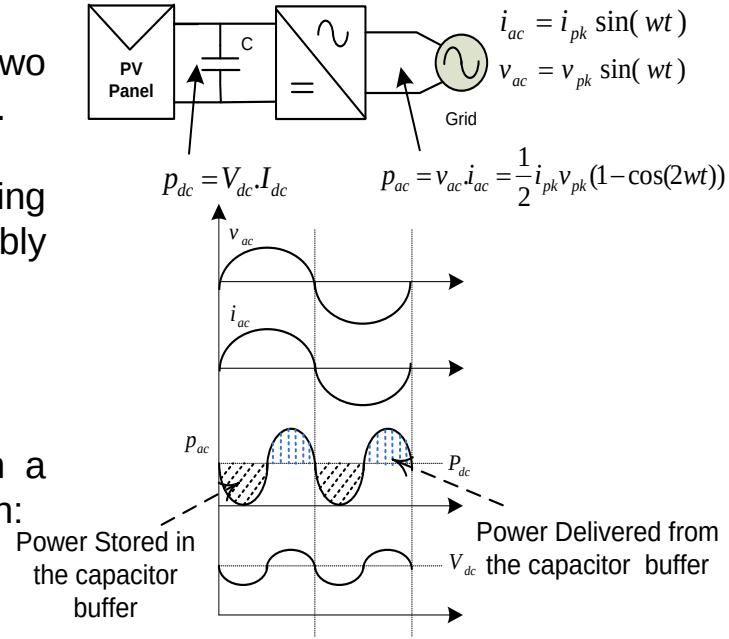
- A constant voltage dc link decouples the power flow in the two stages such that the dc input is not affected by ac side power ripple.

- Power decoupling achieved with electrolytic capacitor - main limiting factor of the lifetime - should be as small as possible and preferably substituted with film capacitors.

- The capacitor in parallel with PV modules or in the dc link.

- Capacitance designed such that the voltage ripple remains in a given range. Minimum capacitance required is given by the equation:

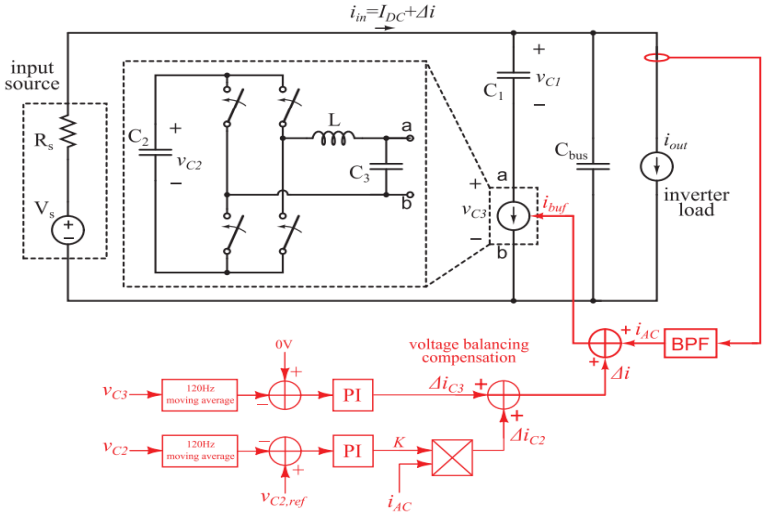
$$C = \frac{P_{\mathrm{PV}}}{2 \cdot \omega_{\mathrm{grid}} \cdot U_C \cdot \hat{u}_C}$$



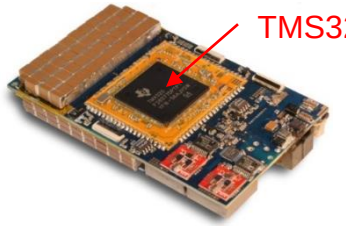
For Ppv= 600W, fgrid=60, Uc=300 and uc = 3%, Cmin=294.7uF

Power decoupling with active buffer

- Active buffer reduces the size of the capacitor and allows use of high reliability film capacitor
- Active buffer with GaN significantly reduces the overall size
- Requires additional converter control



Series stacked energy buffer



"Architecture and Control of a High Energy Density Buffer for Power Pulsation Decoupling in Grid-Interfaced Applications" - Shibin Qin, Yutian Lei, Christopher Barth, Wen-Chuen Liu and Robert C.N. Pilawa-Podgurski

Power line communication (PLC)

- In Micro-inverter applications, there is a gateway that communicates with the microinverters via AC lines. The gateway than communicates via wireless internet connection. Some appliances produce electrical noise at similar frequencies on the same AC lines as the PLC. This can disrupt communication between the gateway and microinverters. Therefore robust performance PLC is needed in noisy environments.
- Also fast data rates (21 kbps+) is needed across AC or DC power lines with low-cost PLC solution
- Single MCU based design supporting PLC and Microinverter
- Operation in frequency bands up to 150 KHz with bandwidth of 24 KHz (CENELEC-A/BCD).
- Industrial standard CSMA/CA MAC protocol supporting point-to-point, point-to-multipoint environments suitable for industrial applications

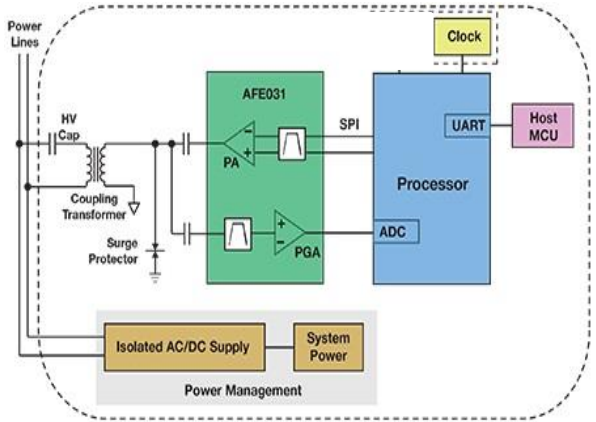
F28035, 60MHz, CPU without VCU accelerator

	RAM (kWord)	FLASH (kWord)	MIPS/RX (PEAK)	MIPS/TX (PEAK)
Half-A, B/C/D (500 KHz Sampling)	8.9	24.6	45	58

F28069, 90MHz, CPU with VCU accelerator

	RAM (kWord)	FLASH (kWord)	MIPS/RX (PEAK)	MIPS/TX (PEAK)
Half-A, B/C/D (500 KHz Sampling)	13	26.4	21	27

PLC Block Diagram



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