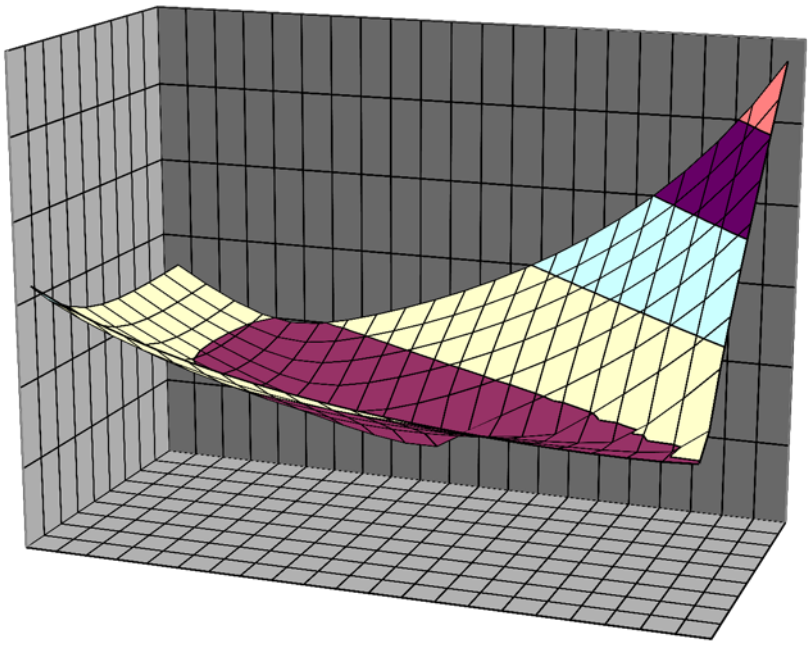
PLL Performance, Simulation, and Design

5th Edition

Dean Banerjee



"Make Everything as Simple as Possible, but not Simpler."
Albert Einstein

To my wife, Nancy, and my children, Caleb, Olivia, and Anabelle

Preface

I first became familiar with PLLs by working for National Semiconductor (now acquired by Texas Instruments) as an applications engineer. While supporting customers, I noticed that there were many repeat questions. Instead of creating the same response over and over, it made more sense to create a document, worksheet, or program to address these recurring questions in greater detail and just re-send the file. From all of these documents, worksheets, and programs, this book was born.

Many questions concerning PLLs can be answered through a greater understanding of the underlying concepts and the mathematics involved. By approaching problems in a rigorous mathematical way one gains a greater level of understanding, a greater level of satisfaction, and the ability to extend the learnings to other problems.

Many of the formulas that are commonly used for PLL design and simulation contain gross approximations with no or little justification of how they were derived. Others may be rigorously derived, but are from outdated concepts or are not compared to measured results to ensure they account for all relevant factors. It is therefore no surprise that there are so many rules of thumb which yield unreliable results.

There is also the approach of not trusting formulas enough and relying on only measured results. The fault with this is that many great insights are lost and it is difficult to learn and grow in PLL knowledge this way. By knowing what a result should theoretically be, it makes it easier to spot and diagnose problems with a PLL circuit. This book takes a unique approach to PLL design by combining rigorous mathematical derivations for formulas with actual measured data. When there is agreement between these two, then one can feel much more confident with the results.

Although PLL technology is evolving, many concepts are timeless and will never become outdated. The fifth edition adds substantial content from the fourth edition regarding many topics including fractional spurs, VCO calibration, delta sigma PLLs, and many other topics.

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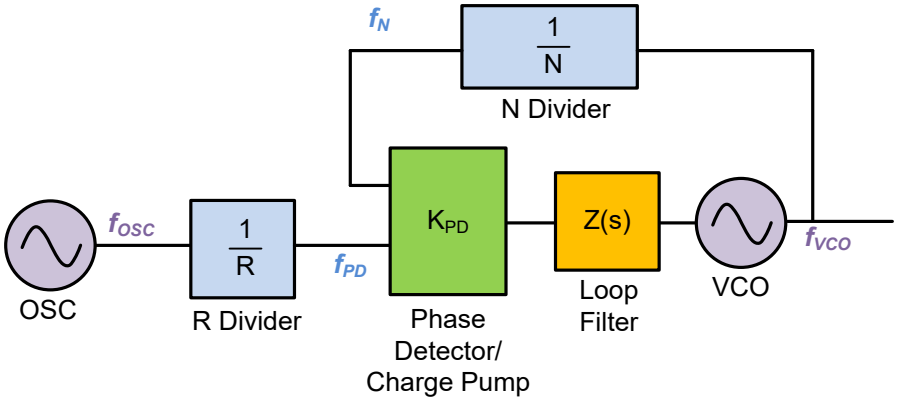
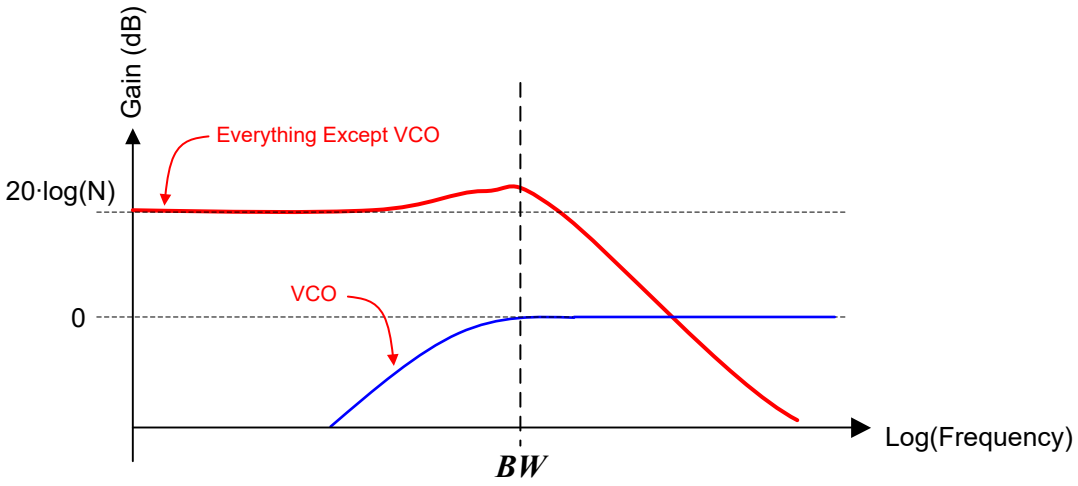
PLL Basics


f_N
1
N
N Divider
f_{OSC}
1
R
f_{PD}
K_{PD}
Z(s)
f_{VCO}
OSC
R Divider
Phase
Detector/
Charge Pump
Loop
Filter
VCO


Gain (dB)
Everything Except VCO
20·log(N)
VCO
0
Log(Frequency)
BW

Chapter 1 Basic PLL Overview

Introduction

The *PLL* (Phased Locked Loop) has been around for many decades. Some of its earliest applications included keeping power generators in phase and synchronizing to the sync pulse in a TV set. Other applications include recovering a clock from asynchronous data and demodulating an FM modulated signal. Although these are legitimate applications of the PLL, this book focuses mainly on the use of a PLL to generate a stable output frequency. In this situation, the PLL starts with a fixed and stable input frequency and this is used to generate one or more output frequencies. Components that generate a tunable output frequency directly typically are not as stable or low noise as a fixed frequency input, so by using negative feedback as is employed in a PLL, it is possible to get a tunable frequency that has both good accuracy and good noise performance.

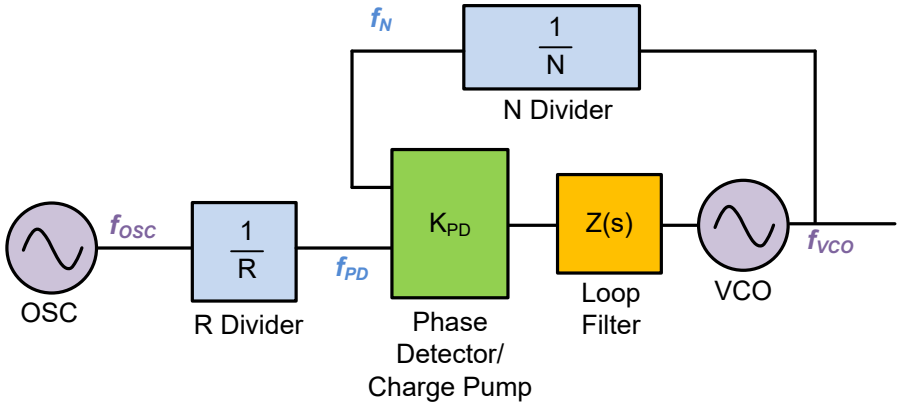


Figure 1.1 *The Basic PLL*

PLL Structure and Frequencies

The PLL starts with a stable input frequency (f_{OSC}). This frequency is typically fixed and very stable over temperature and process. The *R divider* reduces this frequency to the phase detector frequency (f_{PD}). The phase-frequency detector then compares the phase of the R divider (f_{PD}) with the phase of the *N divider* (f_N) and produces current correction pulses that have a duty cycle that is proportional to the phase error between the two inputs to the phase detector. These pulses can be sourcing K_{PD} current, sinking K_{PD} current, or off (tri-state). In later chapters, the charge pump is discussed in more depth, but for most practical purposes, it can be treated as an analog current source that outputs a current of magnitude K_{PD} times the phase error as presented to the phase detector. These current correction pulses then go through a low pass filter called the loop filter, which has a current to voltage transfer function *Z(s)*. The loop filter is typically implemented with discrete components, but can also be integrated on silicon or in the digital domain. The loop filter is application specific and much of this book is devoted to the art of loop filter design. The output voltage of the

loop filter then is used to steer the output frequency of the *VCO* (Voltage Controlled Oscillator). The VCO is a voltage to frequency converter and has a proportionality constant of K_{VCO}. The output of the VCO then goes through the N divider and is divided down to an input of the phase detector, f_N. The phase detector compares the input phases and will cause both inputs to be the same frequency and phase in the steady state and the VCO frequency will be as follows:

$$f_{VCO} = \frac{N}{R} \cdot f_{osc} \tag{1.1}$$

The N divider value can be changed in order to produce a range of VCO frequencies that have the same frequency accuracy as the crystal. In some applications, there is no need for a VCO divider and one can use the direct VCO output. When a range is specified, one typically specifies a channel spacing f_{CH} for the spacing between the frequencies. It is usually desirable to maximize the phase detector frequency, which means that it would be chosen equal to the channel spacing in this case, unless there were some other restrictions with the device that would cause it to be chosen to be lower.

In the case that the output frequency of the PLL is to be fixed, the choice of the N divider value may not be intuitively obvious as there are many choices. In this case, it is typically best to choose the N divider as small as possible to maximize the phase detector frequency in order get the best noise performance.

$$\frac{N}{R} = \frac{f_{VCO}}{f_{osc}} \tag{1.2}$$

Since the output frequency and input frequency are both known quantities, the right hand side of this equation is known and can be reduced to a lowest terms fraction. Once this lowest terms fraction is known, the numerator is the ***N*** value and the denominator is the ***R*** value. If this solution results in an ***N*** divider ratio that the PLL cannot do or phase detector frequency that is too high for the PLL to handle, then multiply both N and R by some integer until it is not an issue. In the case where there is freedom to choose the input reference frequency, it is best to choose it so that it has a lot of common factors with the output frequency so that the ***N*** value is as small as possible.

It is also possible for the dividers to be fractional. Fractional N dividers are somewhat common and fractional values for the R and D divider could arise in a situation if there was a frequency doubler at the input or output. In general, the output frequency is as follows.

$$f_{OUT} = \frac{f_{VCO}}{D} = \frac{N}{R \cdot D} \cdot f_{osc} \tag{1.3}$$

Using an Output Divider to Extend the Frequency Range

Fractional synthesizers with output dividers are commonplace in today's market. The broad host of applications for PLLs makes it desirable for the VCO to be able to tune over a wide frequency. However, there is a trade-off for VCOs between tuning range and noise performance. A common technique used is to combine the VCO with the output divider to produce this wide range.

For instance, one can combine an octave VCO with a divider that does powers of 2 to cover a continuous range. For instance, consider a VCO that can tune 2-4 GHz combined with a divider that can divide by 1, 2, 4, 8, 16, and 32. The divide by 1 can create 2-4 GHz, the divide by 2 can create 1-2 GHz, and the divide by 4 can create 0.5-1 GHz, and so on until the entire range of 62.5 – 4000 MHz is covered.

An alternative approach is to use a higher frequency divider of lesser tuning range and accept a small frequency hole to get continuous coverage. For instance, one could take a divider that can do 1, 2, 3, 4, 5, ... 20 and combine with a VCO that tunes from 4-5 GHz to get frequency coverage from 200 MHz – 1 GHz, then with a divide by one and divide by 2, this can be extended to 0.5 – 2 GHz. Extending on this concept, one could take a programmable divider of 1, 2, 4, 8, 16, and 32 to extend this tuning range to 31.25 – 2000 MHz with no gaps in coverage for VCO.

Fractional PLL N Example with VCO Divider

The model in Figure 1.3 is sufficient for understanding the fundamentals of PLLs, but for a more complete model, one also needs to allow for a VCO divider as shown in Figure 1.2. The VCO divider is often used in cases where it is easier to integrate a higher frequency VCO and then divide down the frequency.

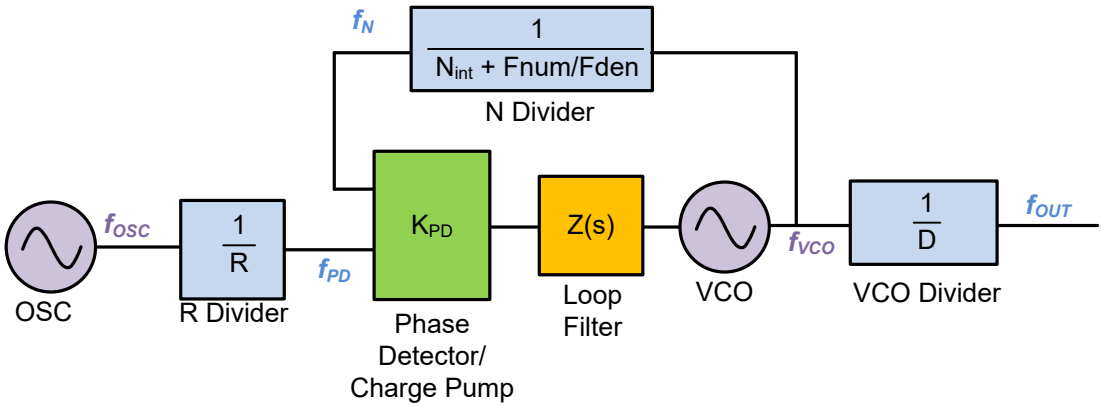


Figure 1.2 *Fractional N PLL with VCO Divider*

Industry Impact on PLL Terminology

The term PLL technically refers to the entire system shown in Figure 1.1; however, challenges with integrating the VCO and input signal have caused industry to redefine the term. In industry, often times when one buys a "PLL" chip from semiconductor manufacturers, it only includes the dividers and charge pump. When capability to integrate VCOs came along, semiconductor vendors did not want to call this a PLL because they wanted it clear that the VCO was also included, so this is often called a *frequency synthesizer*. Integration of the input reference is less common at the time of writing this book and is assumed that this is supplied external to the PLL chip.

PLL Applications

Integer PLL FM Radio

Starting with a more basic example, consider an FM radio receiver where we want to generate a range of frequencies of 88, 88.1, 88.2, … to 108 MHz. Assume that this is done by down converting the received signal to 10.7 MHz. This means that the PLL frequency would be 77.3 to 97.3 MHz with a channel spacing of 0.1 MHz.

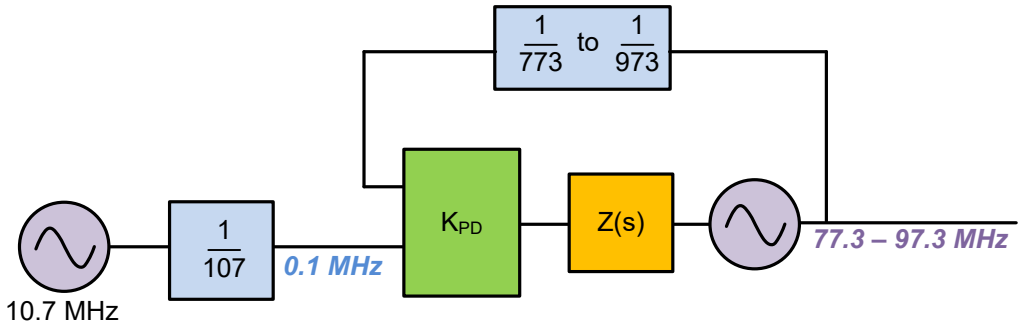


Figure 1.3 *Integer PLL Example*

Clock Recovery Applications

One variation of a jitter cleaning application is a clock recovery application. In wired communications, a clock is typically used to send data. It is undesirable to require an extra wire to just send the clock. In addition to this, skew between the data and clock wires becomes a concern. One approach that can be used is to embed the clock with the data and then use a PLL to recover the clock. The data should have a sufficient number of transitions in order to get the PLL to lock to the clock frequency and there are encoding methods that are designed to do this. This also may put some special requirements on the phase detector. The approach is to feed the data with embedded clock into the input reference of the PLL and then the recovered clock is attained at the VCO output.

Fractional PLL Two Way Radio

One example of a PLL synthesizer in fractional mode using the VCO divider could be a two way radio that generates 430 – 480 MHz with a channel spacing of 10 kHz from a 20 MHz input frequency. Assume that the device chosen has an input multiplier of four and an integrated VCO that tunes from 4300-5300 MHz. Also assume that this VCO has a divider of ten after it. Figure 1.4 shows how this can be done.

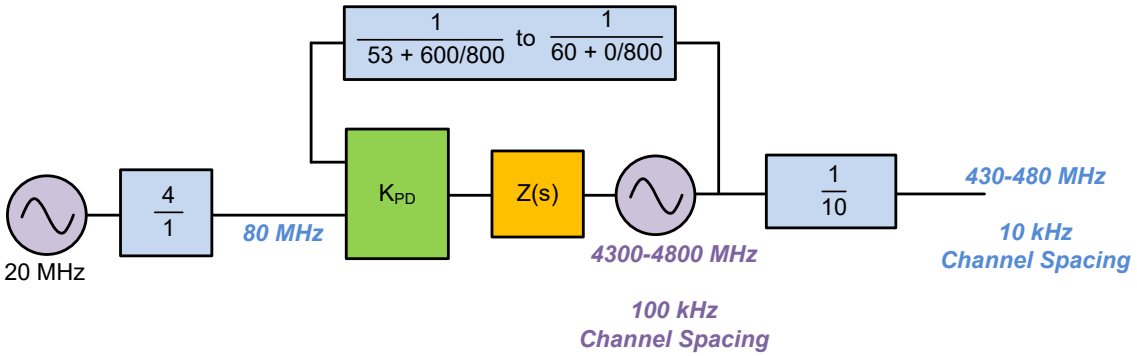


Figure 1.4 *Two Way Radio Example*

Jitter Cleaner Applications

In this type of applications, the PLL can be used to improve the noise of a noisy input signal. This clock may be noisy for intentional reasons or for non-intentional reasons. For instance, sometimes the clock is intentionally made noisy in order to reduce the radiated energy for EMI requirements.

For whatever reason that the clock is dirty, the idea is to use this as the input reference for the PLL and configure the PLL such that it filters out this noise and replaces it with just the noise of the PLL. The PLL can be used to scale the input frequency as well.

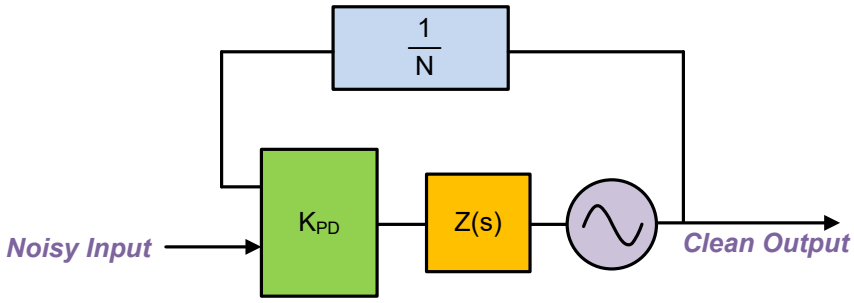


Figure 1.5 *Example of a PLL used to clean a Noisy Input*

Clocking Applications

In some cases, all that is required is a fixed output frequency, such as the case of clocking an A/D converter. Even though there might be fixed crystal frequencies that have pretty good performance, they tend to be at lower frequency. By using a PLL, one can generate much higher fixed frequencies.

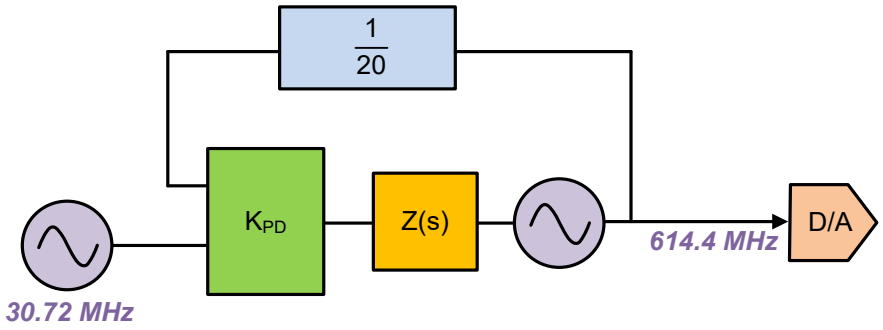


Figure 1.6 *Example of PLL Clocking an A/D Converter*

Conclusion

The PLL can be used to generate a stable output frequency from a fixed input frequency using a phase detector, charge pump, VCO, and dividers. The output frequency can be adjusted by changing the divider values. The output frequency can be a fixed frequency or a tunable range of frequencies. There is a broad range of applications for the PLL.

Chapter 2 A Brief Overview of PLL Performance Characteristics

Introduction

The performance characteristics of the PLL are involved and optimizing them involves many trade-offs. This chapter is intended to give the reader a simplified high level overview of some of these key concepts. Among these concepts are the loop characteristics, phase noise, spurs, and transient response.

Loop Characteristics

The closed loop transfer function from the input of the phase detector to the VCO output is determined by the N divider, VCO gain, charge pump gain, and the loop filter. This is a low pass function with a cutoff frequency called the loop bandwidth (*BW*). The choice of the loop bandwidth is the most critical design parameter and has a significant impact on phase noise, spurs, and the switching speed of a PLL. For all noise and spurs not coming from the VCO, this transfer function multiplies up the phase noise within the loop bandwidth and then suppresses then the filter attenuation begins to kick in after the loop bandwidth. For the VCO, the noise is suppressed below the loop bandwidth frequency and unshaped above the loop bandwidth frequency.

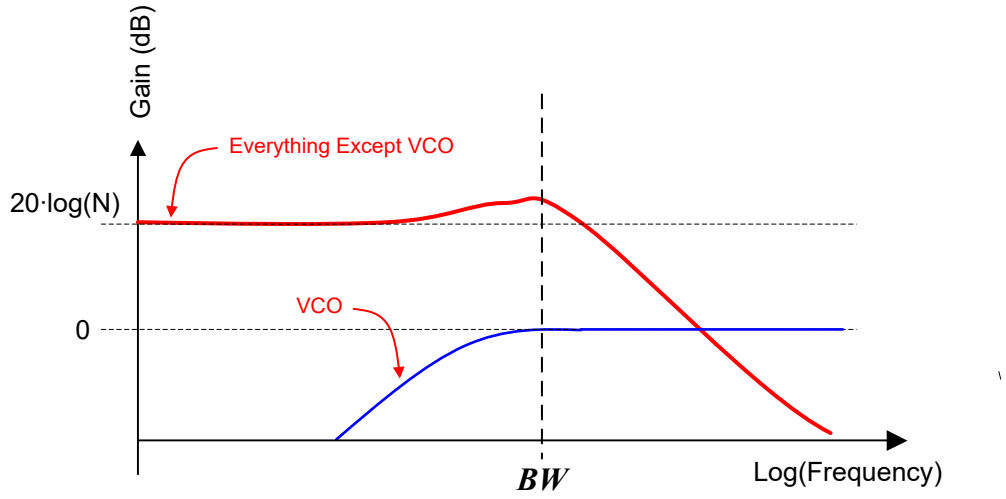


Figure 2.1 *PLL Noise Transfer Functions*

PLL Phase Noise

In addition to the desired signal, a PLL will also produce undesired noise. This noise can be thought of as noise on the phase of the output and is therefore called *phase noise*. In the frequency domain, this is more commonly thought of as the density of the noise power relative to the carrier power and measured in dBc/Hz.

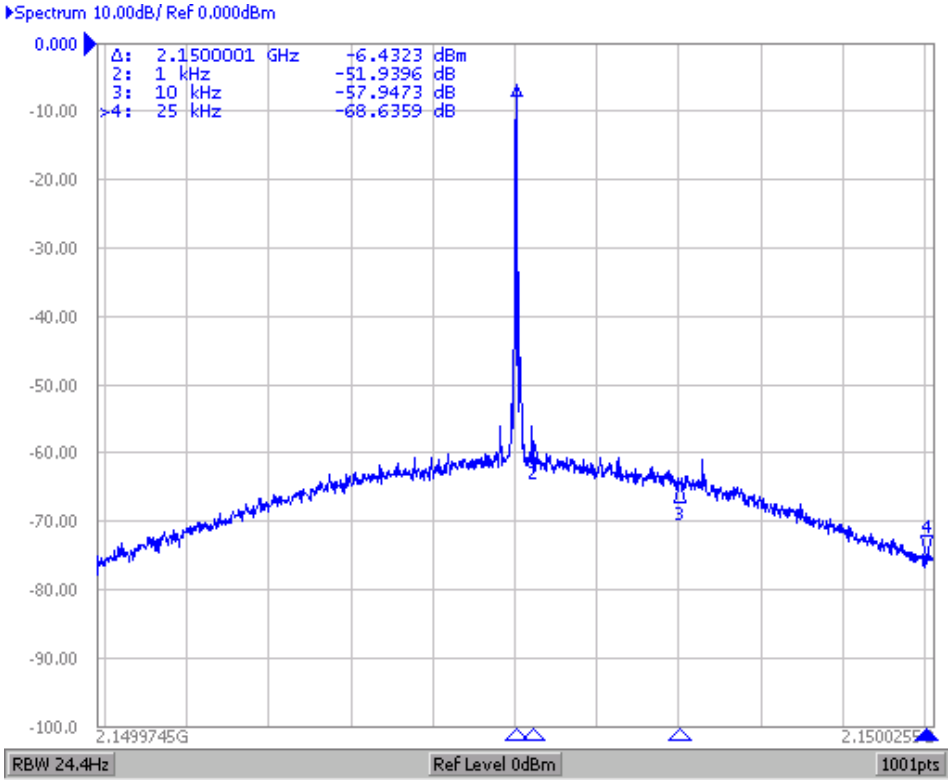


Figure 2.2 *Phase Noise as seen on a Spectrum Analyzer*

A *spectrum analyzer* is a piece of test equipment that can be used to measure phase noise and displays noise power vs. frequency as shown in Figure 2.2. In this case, the measurement needs to be adjusted by 10·log(*Resolution Bandwidth*), which would be 10·log(24.4) = 13.8 dB. For instance, the phase noise at 10 kHz would be -57.9 – 13.8 = -71.7 dBc/Hz. Sometimes spectrum analyzers have correction factors that can account for a few dB. Sometimes there is a marker noise function to help account for this.

The *phase noise analyzer* tracks the VCO frequency and then plots the phase noise as a function of offset. Figure 2.3 shows the same frequency and setup condition as shown in Figure 2.2 with the exception that the instrument was switched from spectrum analyzer mode to phase noise analyzer mode. Note that the phase noise at 10 kHz is -74.1 dBc/Hz, which is better and more accurate than the measurement in spectrum analyzer mode. Part of this reason could be due to the spectrum analyzer correction factor.

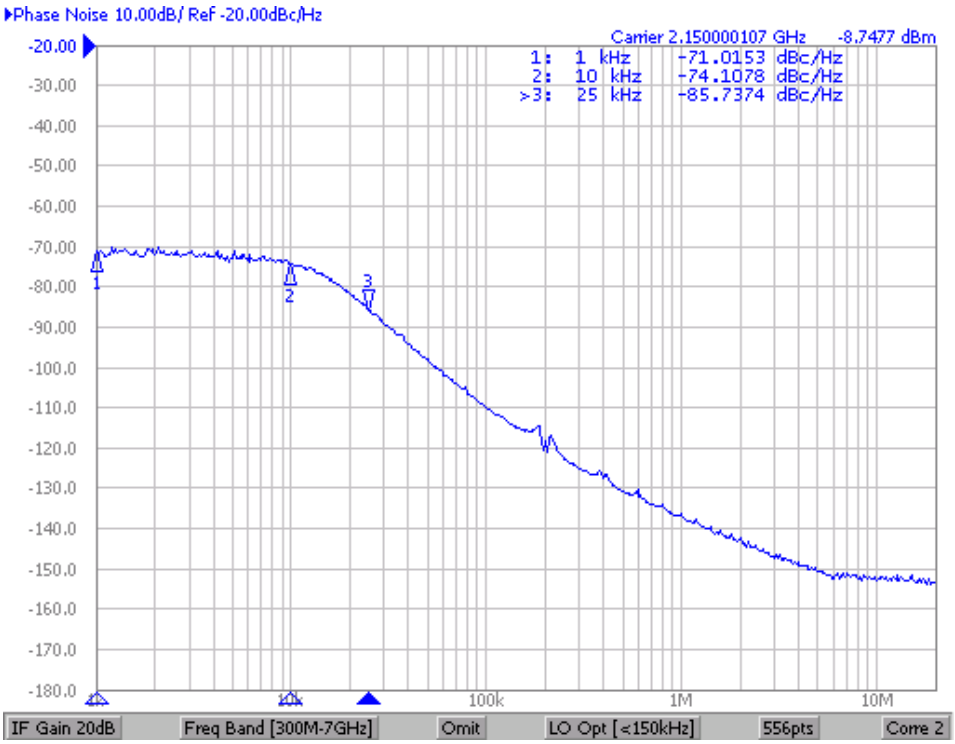


Figure 2.3 *Phase Noise as Seen on a Phase Noise Analyzer*

Spurs

Spurs can be thought of as noise that is concentrated at a specific offset from the carrier as shown in Figure 2.4. These are typically measured in dBc with a spectrum analyzer. There are many kinds of spurs and they can have multiple causes, but most of them occur at very predictable offsets. Spurs have a tendency to occur at multiples of the phase detector frequency, input reference frequency, channel spacing, and fractions of the channel spacing.

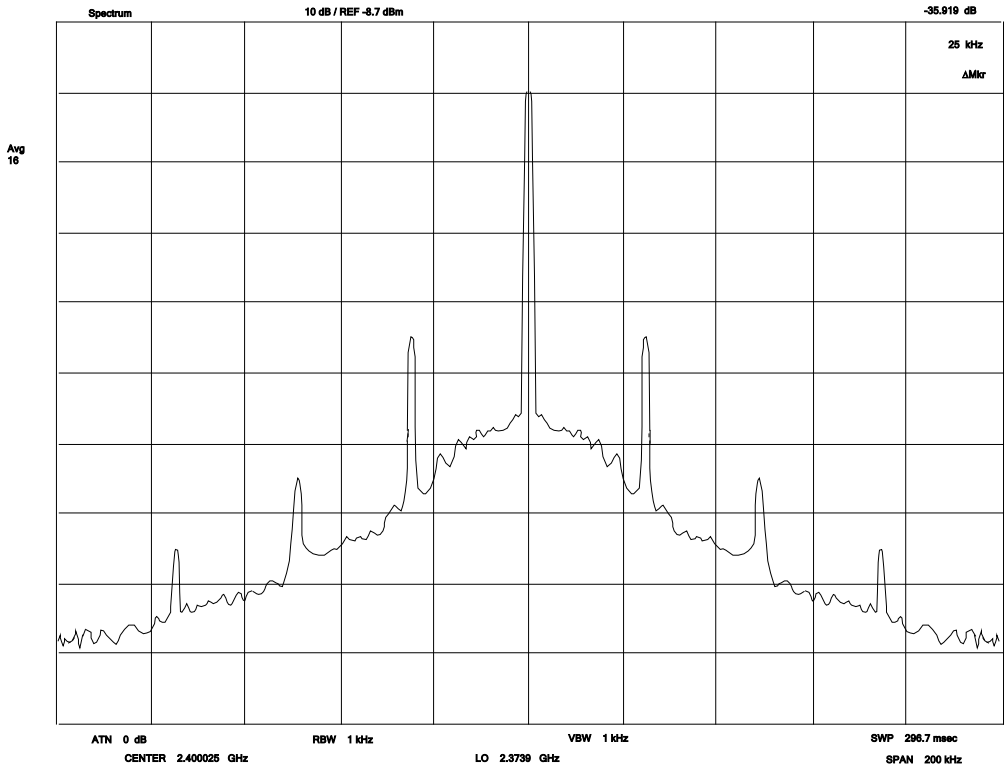


Figure 2.4 *Spurs as seen on a Spectrum Analyzer*

Impact of Dividers on Phase Noise and Spurs

It is getting more common, especially with devices that include the integrated VCO, to have a divider after the VCO to extend the frequency range. This divider has a significant impact on the phase noise and spurs. For the phase noise going through a divider of value *D*, the phase noise is reduced by 20·log(D). So a divide by two translates to a theoretical 6 dB improvement in phase noise. In practice, this 6 dB is typically realized for closer in offsets, but at farther out offsets, the noise improvement may be less due to the divider noise and the fact that some of the noise far-out might not be correlated to the carrier frequency. In regards to spurs, a divider does not change the offset frequency and theoretically reduces the magnitude by 20·log(*D*). Furthermore, because the offset frequency is not changed, this often allows the user to increase the channel spacing at the VCO by a factor of *D* to achieve the same channel spacing, which theoretically pushes the spurs to farther offsets, making them easier to filter. This benefit is seen in practice, although there are certain spurs that are not improved as much as theoretically predicted due to crosstalk.

Transient Response and Lock Time

The *lock time* is typically thought of as the amount of time it takes the PLL to settle to a given *frequency tolerance* after the N divider value is changed. The lock time definition can be expanded to included cases where there is a phase disturbance or when the tolerance is expressed as a phase error instead of a frequency error.

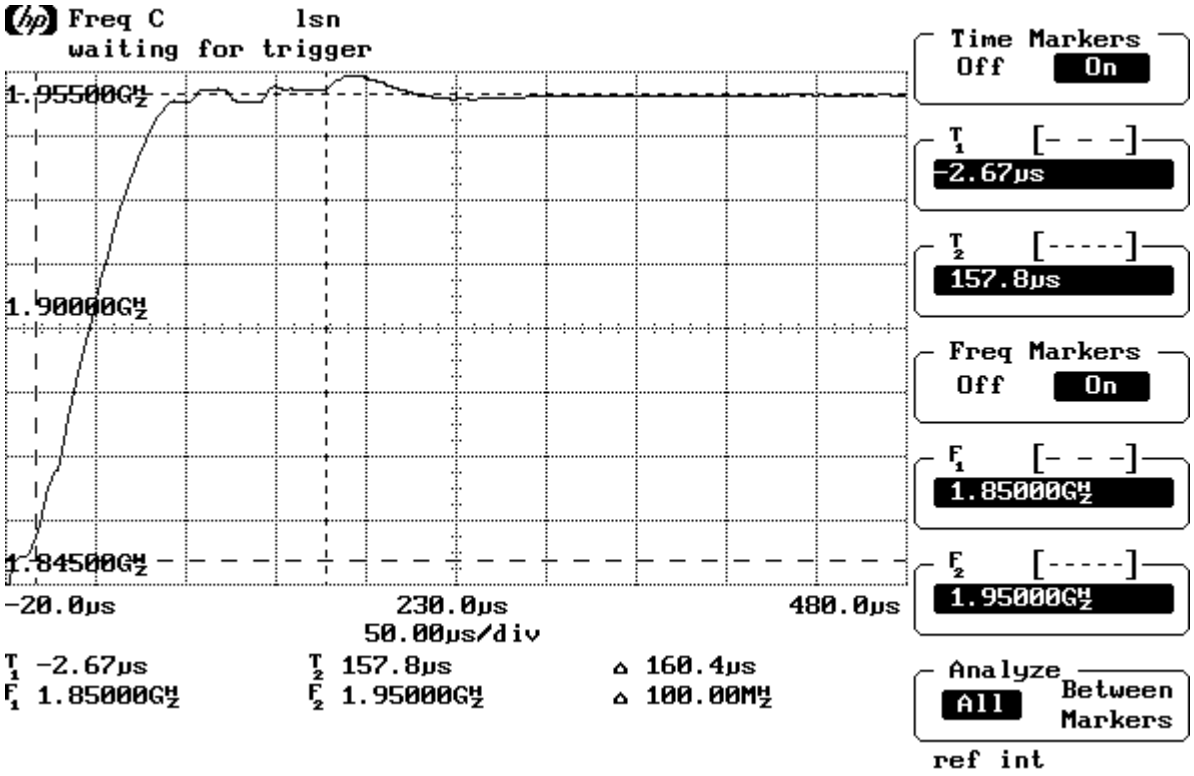


Figure 2.5 *PLL Transient Response*

Conclusion

Phase noise, spurs, and lock time are key performance characteristics and are all impacted dramatically by the loop characteristics, especially the loop bandwidth. A lower loop bandwidth tends to improve spurs and far out phase noise, but degrades the lock time, and the opposite is true of a wide loop bandwidth, although it may improve close-in phase noise depending on the noise quality of the input reference. Different applications may have different requirements, so there is no single PLL design that is optimal for every application.

Chapter 3 Impact of the PLL Performance on the System

Introduction

Phase noise, spurs, and lock time are critical performance characteristics of a PLL. This chapter discusses the impact of these on the performance of a typical system.

Typical Wireless Receiver Application

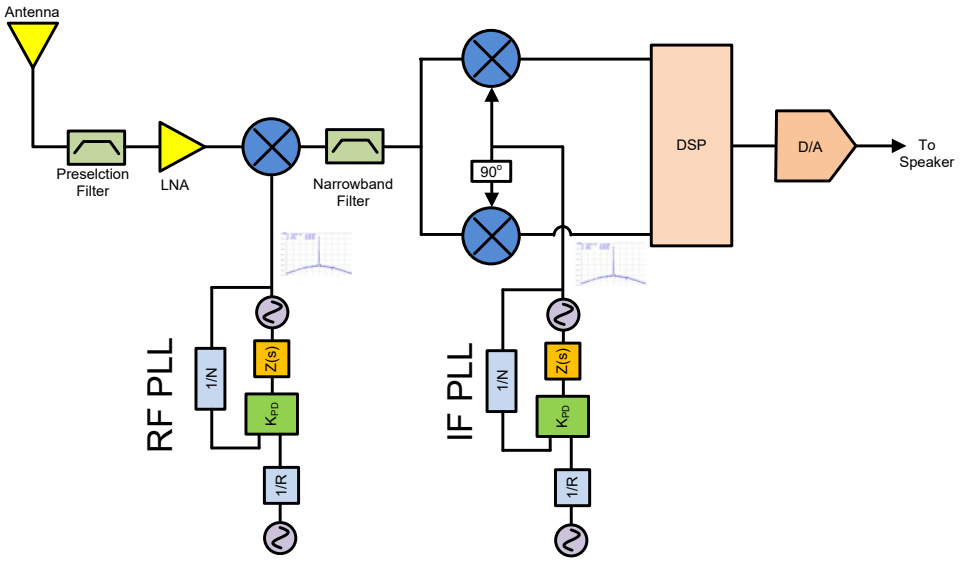


Figure 3.1 *Typical PLL Receiver Application*

General Receiver Description

Figure 3.1 shows a typical receiver application using a PLL. Several different channels, each with a unique frequency, are received by the antenna and allowed to pass through the preselection filter. The signal is them amplified with a *low noise amplifier (LNA)* and downconverter with the *RF (Radio Frequency)* PLL to a fixed *IF (Intermediate Frequency)* signal. In other words, the frequency of the RF PLL is adjusted such that the difference of the desired channel frequency and the RF PLL frequency is always the same. This signal then goes through the narrow filter that is at this fixed value in order to remove the unwanted mixer image as well as mixing products formed by undesired channels that pass through the preselection filter. The IF PLL mixes this frequency down to baseband so that the information on the signal can be attained.

Other than the obvious parameters of a PLL such as cost, size, and current consumption, the phase noise, reference spurs, and lock time are important to the performance of the system and will be discussed in more detail.

Phase Noise, Spurs, and Lock Time as They Relate to This System

Phase noise at lower offsets from the carrier has a tendency to increase bit error rates and degrade the signal to noise ratio of the system. Many systems that care about integrated phase noise that can be impacted heavily by the lower offset phase noise. Phase noise at farther offsets can mix with other signals from other users in the system in order to create undesired noise products.

Spurs are noise concentrated at discrete offset frequencies from the carrier. These offset frequencies are typically multiples of the channel spacing. These offset frequencies are typically exactly at frequencies where an adjacent user of the system can be and can mix down to create undesired noise products that fall on the desired carrier frequency.

Lock time is the time that it takes for the PLL to change frequencies. This can be for applications that scan over a frequency band or do frequency hopping. When the PLL is switching frequencies, no data can be transmitted, so lock time of the PLL must lock fast enough as to not slow the data rate. Lock time can also be related to power consumption. In some systems, the PLL only needs to be powered up when data is transmitted or received. During other times, the PLL and many other RF components can be off. If the PLL lock time is less, then that allows systems like this to spend more time with the PLL powered down and therefore current consumption is reduced. For other systems, the PLL need to scan over a range of frequencies and these applications tend to need faster PLL lock times.

Analysis of Receiver System

For the receiver shown in Figure 3.1, the PLL that is closest to the antenna is typically the most challenging from a design perspective, due to the fact that it is tunable and higher frequency. Since this PLL is tunable, there is typically a more difficult lock time requirement, which in turn makes it more challenging to meet spur requirements as well. In addition to this, the requirements on this PLL are also typically stricter because the undesired channels are not yet filtered out from the antenna.

The IF PLL has less stringent requirements, because it is lower frequency and also it is often fixed frequency. This makes lock time requirements easier to meet. There is also a tradeoff between lower spur levels and faster lock times for any PLL. So if the lock time requirements are relaxed, then the spur requirements are also easier to meet. The signal path coming to the second PLL has already been filtered, so typically the lock time and spur requirements are often less difficult to meet.

Example of an Ideal System with an Ideal PLL

For this example, assume all the system components are ideal. All mixers, LNAs and filters have 0 dB gain and noise figure. All filters are assumed to have an idea “brick wall” response. The PLL is assumed to put out a pure signal and have zero lock time.

Parameter	Value	Units
Receive Frequency	869.03 – 893.96	MHz
RF PLL Frequency	783.03 – 807.96	MHz
IF PLL Frequency	86	MHz
Channel Spacing	30	kHz
Number of Channels	831	n/a
IF PLL Frequency	240	MHz

Table 3.1 *RF System Parameters*

The received channel will be one of the 831 channels. The channels will be designated 0 to 830, where channel 0 is at 869.03 MHz and channel 830 is at 893.96 MHz. Now suppose one wants to receive channel 453 at 888.62 MHz. This frequency comes in through the antenna, filter, and LNA and is presented to the first mixer. The RF PLL frequency is then programmed to 802.62 MHz. The output of the mixer is therefore the sum and difference of these two frequencies, which would be 1691.24 MHz and 86 MHz. The filter afterwards filters out the high frequency signal so that only the 86 MHz signal passes through. This 86 MHz signal is then down converted to baseband with the IF PLL frequency, which is a fixed 86 MHz.

Ideal System with a Non-Ideal PLL

Consider the effects of a non-zero lock time. Suppose that the RF PLL takes 1 ms to change frequencies and the IF PLL takes 10 ms to change channels. For this application, the fact that the IF PLL takes 10 ms to change channels really does not have any impact on system performance. What this means is that once the receiver is turned on, it takes an extra 10 ms to power up. Because the IF PLL never changes frequency, this is the only time this lock time comes into play. Now the 1 ms lock time on the RF PLL has a greater impact. If a person was using their cell phone and it was necessary to change the channel, then this lock time would matter. This might happen if the user was leaving a cell and entering another cell and the channel they were on was in use. Also, sometimes there is a supervisory channel that the cell phone needs to periodically switch to in order to receive and transmit information to the network. This is the factor that drives the lock time requirement for the PLL in the IS-54 standard, after which this example was modeled. The time needed to switch back and forth to do this needs to be transparent to the user and no data can be transmitted or received when the PLL is switching frequencies.

Now consider the impact of phase noise and spurs of the PLL. Suppose two signals, the desired channel to be received at 888.62 MHz, and an undesired channel at 888.65 MHz, as shown in Figure 3.2.

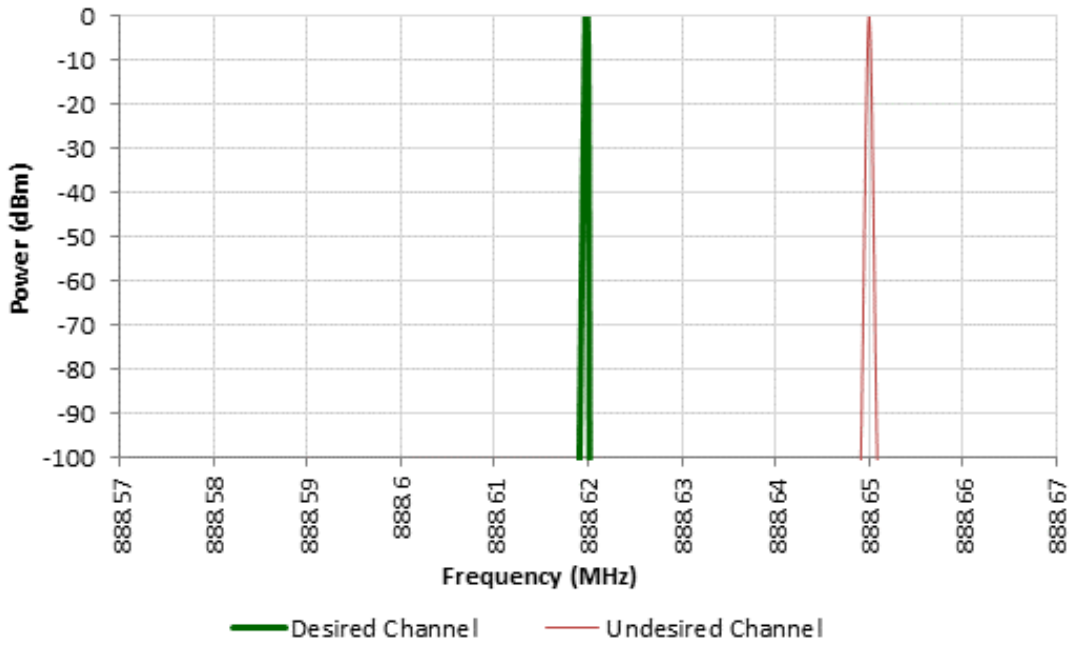


Figure 3.2 *Output of the Preselection Filter*

Assume that the RF PLL output has an output at 802.62 MHz with noise and spurs as shown in Figure 3.3.

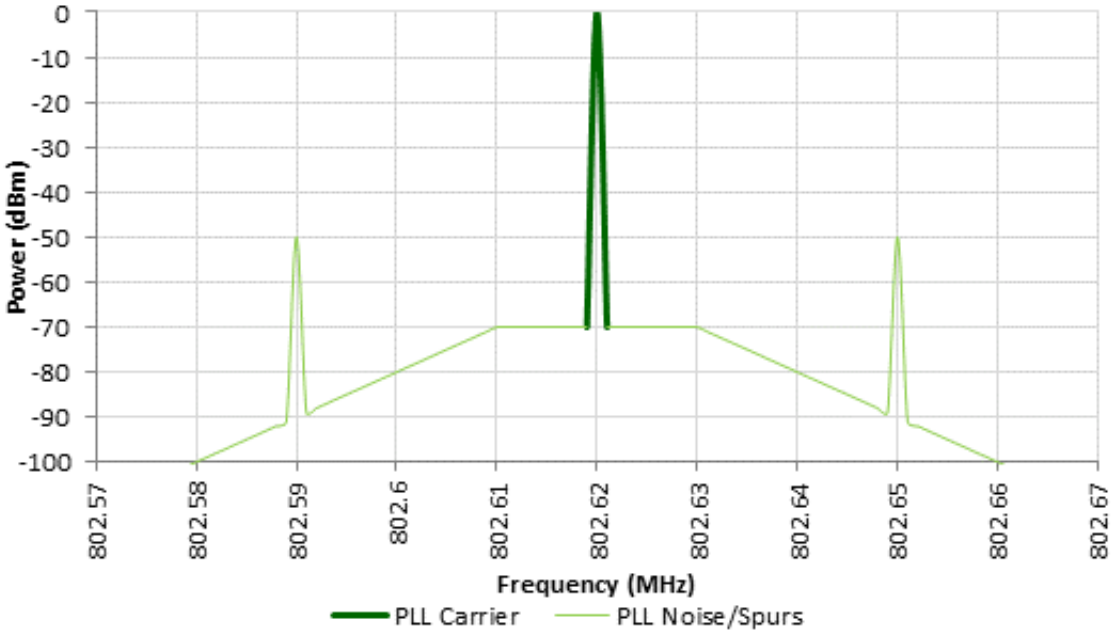


Figure 3.3 *Signal with Noise from RF PLL*

The desired output would be a pure 86 MHz tone, but the noise and spurs of the RF PLL mix with both the desired and undesired channels. One of the purposes of the narrowband filter is to remove noise and spurs, but the spur caused by the mixing of the 888.65 MHz undesired channel and the spur at 802.65 MHz lands exactly at 86 MHz and cannot be filtered as shown in Figure 3.4. Also, as no filter is perfect, some of the phase noise close to this 86 MHz signal will also pass through the narrowband filter.

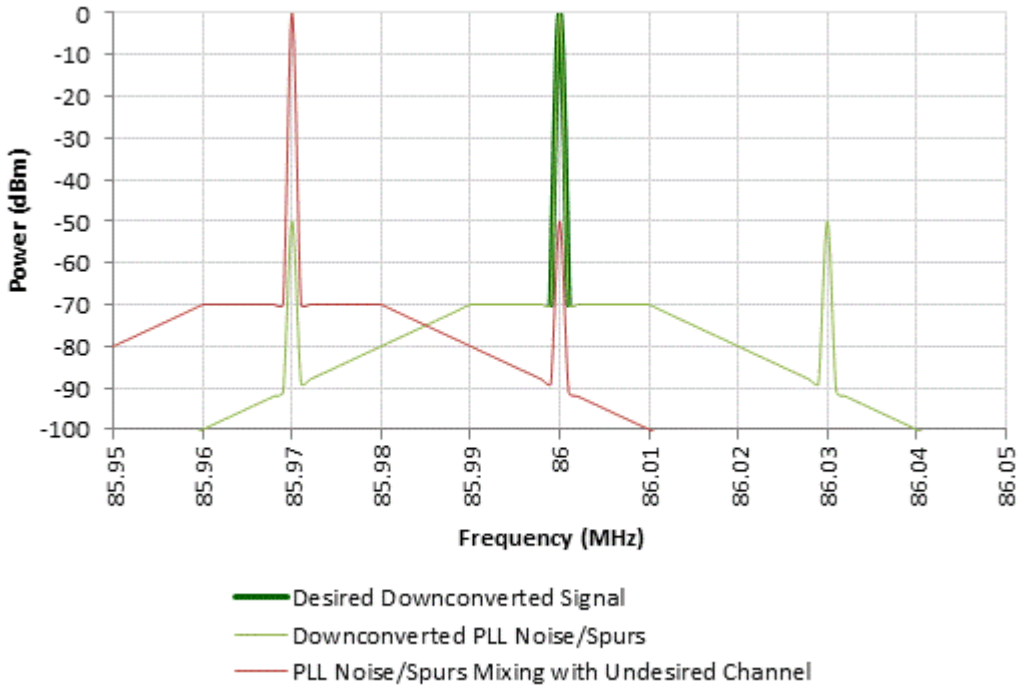
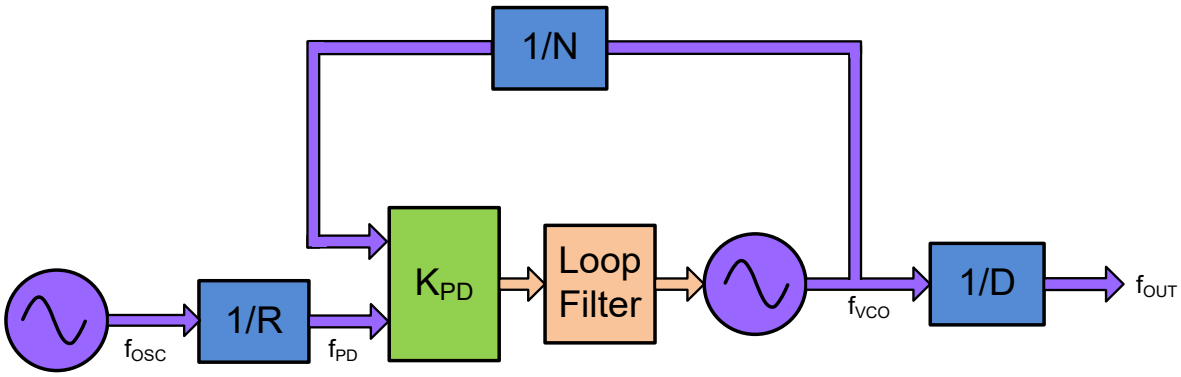


Figure 3.4 *Output Signal from Mixer*

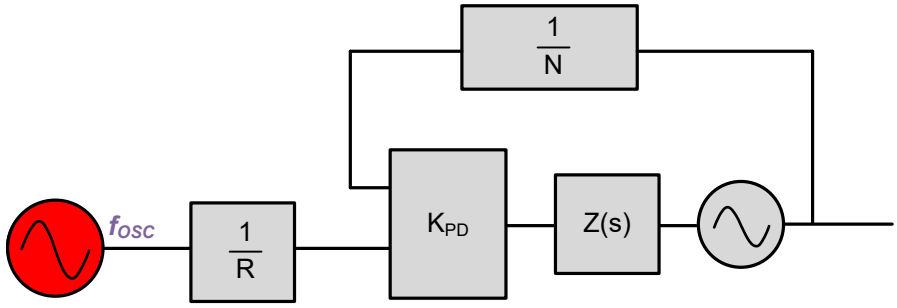
Conclusion

This chapter has investigated the impacts of phase noise, spurs, and lock time on system performance. These three performance parameters are greatly influenced by many factors including the VCO, loop filter, and ***N*** divider value. Of course it is desirable to minimize all three of these parameters simultaneously, but there are important trade-offs that need to be made. Applications where the PLL only has to tune to fixed frequency tend to be less demanding on the PLL because the lock time requirements tend to be very relaxed, allowing one to optimize more for spur levels. There is no one PLL design that is optimal for every application.

PLL Building Blocks



Chapter 4 Input Sources, Crystals, and Principles of Oscillation



Introduction

The PLL starts with the assumption that there is an input signal. This should be very accurate in frequency as any error is translated directly to the VCO. This signal can be a recovered clock, a frequency generated from another chip, or a signal generated by a crystal /crystal oscillator. Aside from the frequency of the input signal, characteristics such as phase noise, amplitude, and slew rate are also critical. This chapter discusses some important properties of recovered clocks, crystals, and crystal oscillators.

Recovered Clocks

When data is transmitted over a long distance, one technique is to serialize the data and embed the clock. By doing this, fewer wires are needed for transmission and issues with skew between the lines are eliminated. The deserializer then recovers the clock from the data and interprets the signal sent. Often times, recovered clocks do not have very good noise performance, but a PLL can be used to clean up the signal.

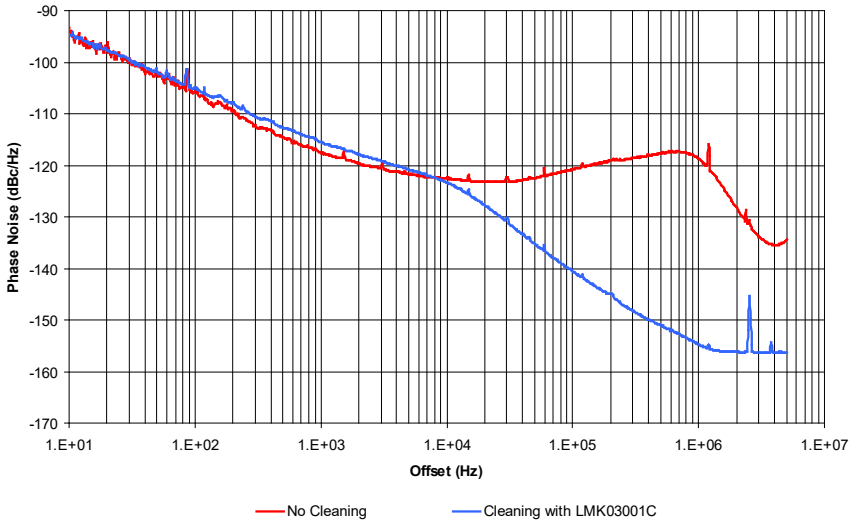


Figure 4.1 *Recovered Clock Before and After Being Cleaned by a PLL*

Crystals and Crystal Oscillators

Principles of Oscillation

The general idea for an oscillator is to have an inverter with the output fed back to the input through a filter. Since it is not possible to filter without delay, this filter can also be thought of as a delay. In order for a circuit to oscillate, it must satisfy the following conditions known as the *Barkhausen criterion*.

1. The open loop gain at the oscillation frequency must be 1.

2. The phase of the open loop gain at the oscillation frequency, including the phase shift of the inverter must be a zero or some other multiple of 360 degrees.

The most basic oscillator is called the *ring oscillator*. This is basically a series of inverter with the output fed back to the input. A delay is added to set the frequency. If the gate delay of the inverter is significant, it adds to this delay. This delay can also be thought of as a filter. The only difference is that a filter produces a sine wave instead of a square wave. This circuit model works especially well for crystal oscillators and is very intuitive. The fundamental frequency of oscillation, f_{osc}, is easy to calculate once the delay, τ is known.

$$f_{osc} = \frac{1}{\tau} \qquad \textbf{(4.1)}$$

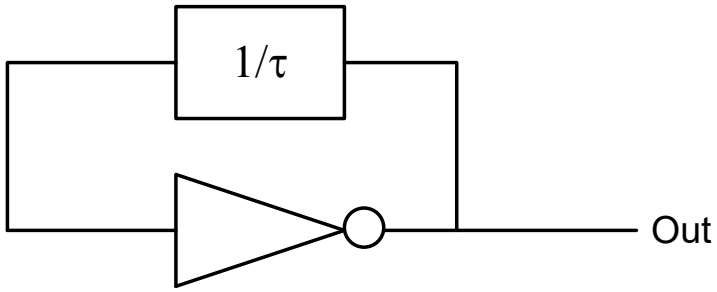


Figure 4.2 *A Typical Crystal Oscillator Diagram*

Note that there is no input and the oscillator relies on noise to get it started. Once it does, the inverter sustains the oscillations. The startup time is governed by the gain of the inverter and the external components around it. One way to implement the delay is with a crystal.

Crystal Element for Used in Oscillators

The crystal can be viewed as a filter with a very low bandwidth and high frequency accuracy with an equivalent circuit in Figure 4.3 with ***Lm*** (motional inductance), ***Cm*** (motional capacitance), ***Rs*** (series resistance), and ***Cp*** (parallel capacitance).

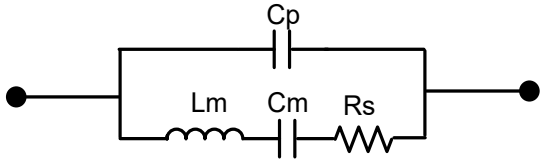


Figure 4.3 *A Typical Crystal Oscillator Circuit*

The impedance of the crystal is given by:

$$Z(s) = \frac{s^2 + s \cdot \left(\frac{Rs}{Lm}\right) + \left(\frac{1}{Lm \cdot Cm}\right)}{s \cdot Cp \cdot \left(s^2 + s \cdot \left(\frac{Rs}{Lm}\right) + \left(\frac{Cm + Cp}{Cm \cdot Lm \cdot Cp}\right)\right)} \tag{4.2}$$

The imaginary part of the numerator will never be zero ***Rs***, but satisfying the following equation for series resonance will minimize the impedance.

$$s^2 + \left(\frac{1}{Lm \cdot Cm}\right) = 0 \tag{4.3}$$

$$\omega_{Series} = \sqrt{\frac{1}{Lm \cdot Cm}} \tag{4.4}$$

If we set the real part of the portion of the denominator in parenthesis equal to zero, we get the frequency for parallel resonance.

$$s^2 + \left(\frac{Cm + Cp}{Lm \cdot Cm \cdot Cp}\right) = 0 \tag{4.5}$$

$$\omega_{Parallel} = \sqrt{\frac{Cm + Cp}{Lm \cdot Cm \cdot Cp}} = \frac{1}{\sqrt{Lm \cdot Cm}} \cdot \sqrt{1 + \frac{Cm}{Cp}} = \omega_{Series} \cdot \sqrt{1 + \frac{Cm}{Cp}} \tag{4.6}$$

The series and parallel resonant frequencies correspond to totally different values for the crystal impedance, but these frequencies are typically very close because ***Cm*** is typically very small compared to ***Cp***. All crystals have a series and parallel resonant mode and the mode of oscillation depends how the crystal is hooked up in the circuit.
The value of ***Rs*** has only a very slight impact on the oscillation frequency. However, it does impact how sharp the cutoff is, which corresponds to the noise. Below is an example of a 20 MHz parallel resonance shown for ***Cp***=5.4 pF, ***Cm*** = 0.02545 pF, ***Lm*** = 2.5 mH, and ***Rs*** at various values.

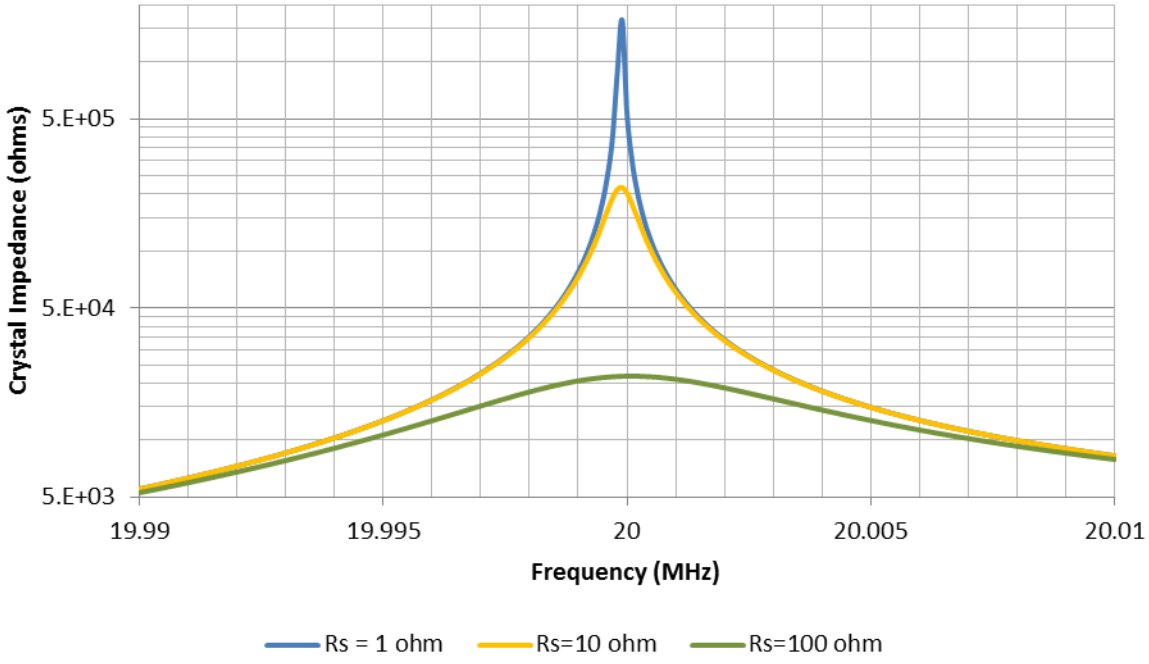


Figure 4.4 *Crystal Resonance*

Typical Parallel Crystal Circuit

For parallel resonant of the circuit, the crystal, the output of the inverter is what is used to drive the rest of the circuit. Load capacitors of ***C1*** and ***C2*** are the load capacitors, which are supplied externally to help stabilize the frequency and improve spurious emissions. These values effective are in parallel with ***Cp***. The series resonant frequency is not shifted, but the parallel resonant frequency is shifted closer to the resonant frequency as follows:

$$\omega_{Parallel} = \omega_{Series} \cdot \sqrt{1 + \frac{Cm}{Cp + \left(\frac{C1 \cdot C2}{C1 + C2}\right)}} \qquad (4.7)$$

The load capacitors can also be used to slightly "pull" the crystal. The capacitors can reduce harmonics and sometimes making ***C2*** > ***C1*** can help reduce them even further. If harmonics are still an issue, the resistor, ***R***, can optionally be added.

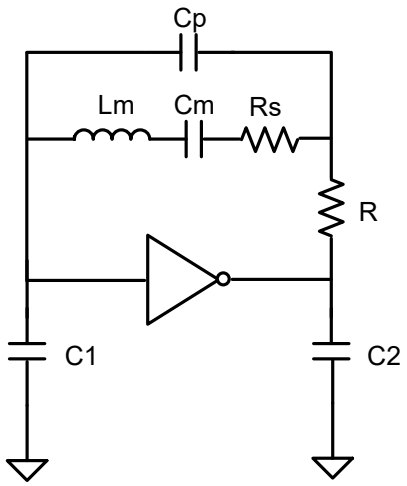


Figure 4.5 *Parallel Crystal Oscillator*

Common Types of Crystal Oscillators

Frequency accuracies of ten parts in one million are not uncommon for crystal oscillators. The main cause of frequency error in these oscillators is drift over temperature. The *Temperature Compensated Crystal Oscillator* (TCXO) has a temperature sensor and compensation to correct the crystal frequency over temperature. This improves the frequency accuracy by about a factor of ten. The *Oven Controlled Crystal Oscillator* (OCXO) improves the performance by approximately another factor of ten by having an oven heat the crystal to a constant temperature.

Acronym	Oscillator Type	Accuracy	Comments
XO	Crystal Oscillator	10 ppm	This is a crystal plus the inverter.
TCXO	Temperature compensated crystal oscillator	1 ppm	Uses circuitry to compensate frequency over temperature, but sometimes this circuitry can add noise.
VCXO	Voltage compensated crystal oscillator	10 ppm	Like a crystal oscillator, but a voltage can be used to tune the frequency
OCXO	Oven controlled crystal oscillator	0.1 ppm	Uses an oven to maintain constant temperature

Table 4.1 *Common Types of Crystal Oscillators*

Conclusion

The input source to the PLL can come from many sources such as another device or a crystal oscillator. It typically needs to be clean and highly accurate in order to generate a good frequency at the output. Aside from the noise and accuracy of the signal, one does need to be also mindful of the output format and slew rate. In general, PLLs like to have a higher slew rate for the best phase noise and spur performance. Differential inputs typically can have better phase noise as well.

References

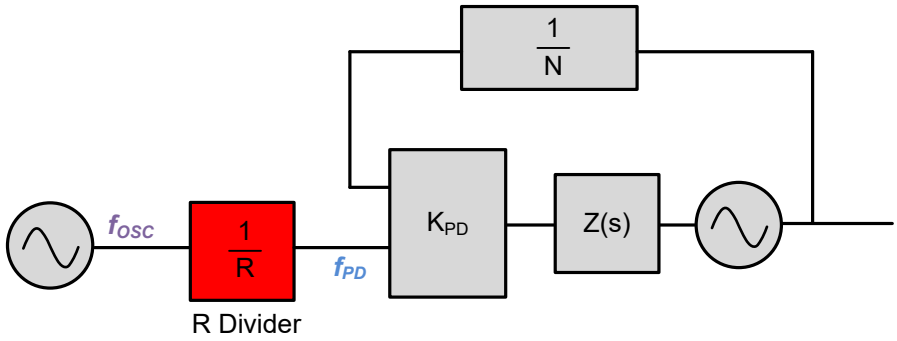
[1] Gardner, F.M. *Phaselock Techniques*, 2nd ed., John Wiley & Sons, 1980

[2] Massovich, Vadim *Frequency Synthesis: Theory and Design*, 3rd ed., John Wiley & Sons 1987

[3] *1997 ARRL Handbook*, 74th ed. The American Radio Relay League, 1996

[4] Rohde, Ulrich L. *Microwave and Wireless Synthesizers: Theory and Design*, John Wiley & ,1997

Chapter 5 The Input Path and R Divider



Introduction

Although the input path and R divider might not seem be the most complicated blocks of the PLL, they are still worthy of some discussion because the output of this block gets multiplied by the N divider to the output of the VCO. If this block is noisy or if the input signal does not have a sufficient slew rate, then there can be degradations in the spurs and phase noise. When input frequency (f_{OSC}) is a low frequency sine wave, this tends to lead to slower slew rates on the signal that can impact the performance of the PLL. The input path can also be more sophisticated and include doublers and multipliers.

Connecting to the Input (OSCin) Pin

General Properties of the Input Pin

The input pin to a PLL often has its own bias level and requires the signal to be AC coupled. The input pin to the PLL can be either differential or single-ended.

PLLs with Differential OSCin Input

Many PLLs offer a differential OSCin input. If this is offered, the ideal way to drive this is differentially with a signal of high slew rate. In the case that the input source is single-ended, one can either use a balun or AC couple the unused input to ground. For optimal performance, some devices get better spurs if the impedance as seen looking from the OSCin pin is the same as looking outward from the OSCin* pin as shown in Figure 5.1. The likely reason for this is that any spurious noise on the ground gets tracked out better by the pins.

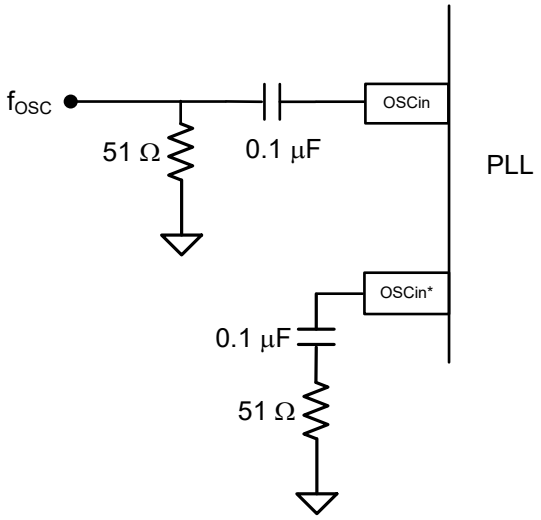


Figure 5.1 *Driving a differential input as single-ended*

PLLs with Single Ended OSCin Pin

For the case of a single-ended OSCin input and a single-ended source, it is typical to just a shunt 50 ohm resistor to ground. This works if we assume that the driving source has 50 ohm output impedance, the amplitude is not too high, and the input impedance of the PLL is not too high. If this is not the case, one can either use a series resistor or a resistive pad to correct for this.

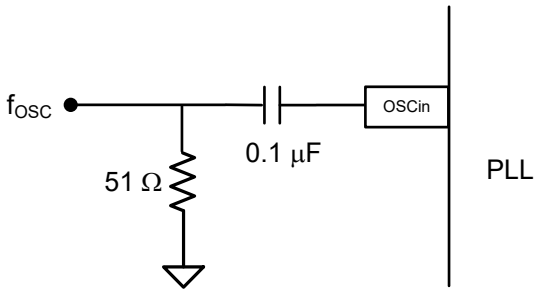


Figure 5.2 *Driving a PLL Single-ended*

Another situation that might come up is if the input signal is differential, but the input pin is only single-ended. One way to resolve this is to use a balun, but if this is undesired it is possible to just use one side of the differential output. If the impedance presented to the OSCin pin is important, it is allowable to ground just one side of the differential output if it is AC coupled to the driver as shown in Figure 5.3. However, do not ground both sides as this will interfere with the differential termination.

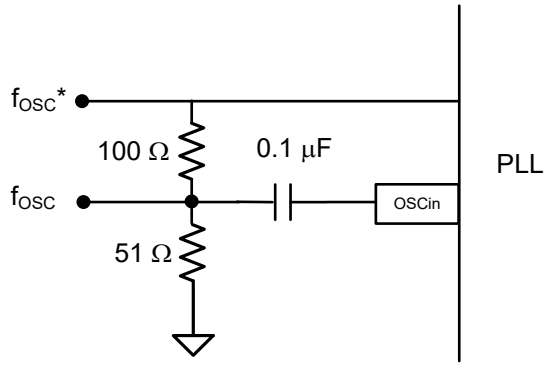


Figure 5.3 *Driving a PLL Single-ended with a Differential Input*

R Divider Structure

The R divider is typically done in a lower frequency process and is often differentially done in CMOS or CML. It is typically done with a series of flip-flops.

Doublers and Input Multipliers

Some devices offer programmable input multipliers to allow improvement to PLL phase noise or spurs. However, one has to be aware that these blocks can add noise. Doublers are easier to implement, so they often do not add noticeable noise. Multipliers greater than two can add a significant amount of noise and the amount of added noise is device specific.

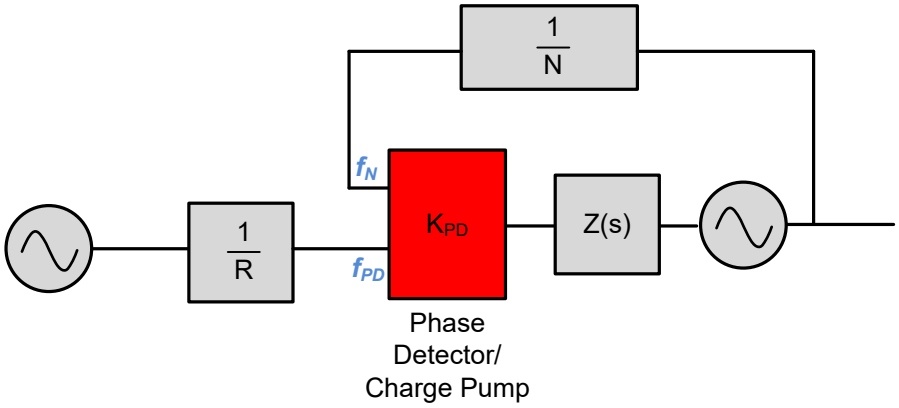
The Importance of Slew Rate

It is often the case that slew rate is important to the OSCin input pin. The reason for this is that this gives the input signal greater noise immunity. This noise can come in the form of phase noise or spurs. It is also the case that sometimes this noise and spurious might come from inside the PLL. In any case, the higher slew rate almost always is a benefit. For a sine wave, higher slew rates come with higher amplitude and frequency. At some point, the faster slew rate does not help, and a typical LVPECL, LVDS, or LVPECL signal has a sufficient slew rate.

Conclusion

The input path to the PLL is an important part to the PLL because if this is not connected correctly, it can lead to performance degradations in phase noise and spurs.

Chapter 6 The Phase Detector and Charge Pump



Introduction

The phase detector is a device that converts the differences in the two phases from the N counter and the R counter into an output voltage. This output voltage can either be applied directly to the loop filter or converted to a current by the charge pump. The voltage phase detector is presented to support legacy literature, but the main focus of this book is charge pump PLLs.

The Modern Charge Pump vs. the Voltage Phase Detector

The Voltage Phase Detector

The voltage phase detector was the approach that was commonly used before the introduction of the charge pump and outputs a voltage proportional to the phase error between the outputs of the N and R dividers. It can be implemented with a mixer, XOR gate, or JK flip flop. Perhaps the reason why the voltage phase detector lost popularity compared to the charge pump was that it was unable to attain and hold lock if the VCO frequency/phase was too far off from the target value, unless acquisition aids or an active filter is used. Floyd Gardner's classical book, *Phaselock Techniques*, goes into great detail about all the details and pitfalls of this sort of phase detector and presents the following topology for active filters.

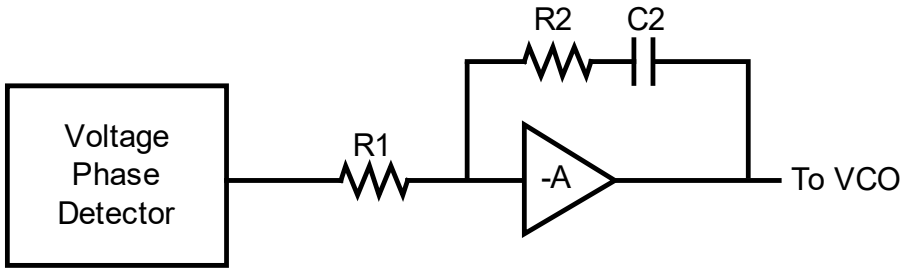


Figure 6.1 *Classical Active Loop Filter Topology for a Voltage Phase Detector*

Active filters require an op amp, which add cost, area, current, and noise, and tend to be less popular unless the op-amp is necessary for some other purposes, such as providing a larger tuning voltage range to the VCO. Although the voltage phase detector might have applications where it may be superior to the charge pump, it is far less common and therefore not discussed in much depth in this book.

The Introduction of the Phase/Frequency Detector (PFD) and Charge Pump

The phase/frequency detector (***PFD***) and charge pump combination has replaced the voltage detector in many designs because it has no issues with attaining and maintaining lock and requires no active components. Referring to Figure 6.2, the charge pump architecture may be different, but it mathematically achieves the same functionality as integrating an ideal op amp for the voltage phase detector. The current can be thought of as the output voltage in Figure 6.1 divided by R1. The charge pump PLL requires the additional component C1 in order to help filter the current pulses it outputs, but this component also provides additional filtering for spurs, which makes it a good idea to have anyways.

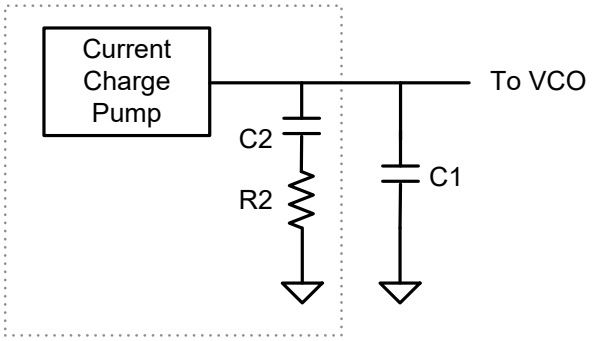


Figure 6.2 *Passive Loop Filter with PFD and Charge Pump*

Phase Frequency Detector High Level Description

The PFD compares the outputs of the N and R counters in order to generate a correction voltage, which is converted to a current by the charge pump. This book will treat the charge pump and PFD as one block because they are typically integrated together.

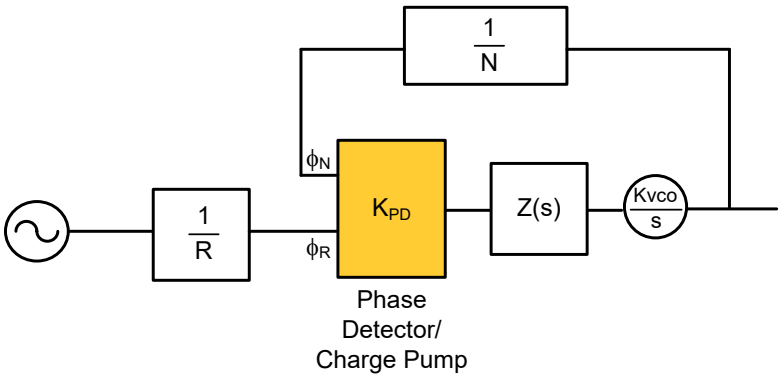


Figure 6.3 *Phase/Frequency Detector with Charge Pump*

Looking carefully at Figure 6.3, observe the VCO gain is divided by a factor of ***s*** in order to convert the VCO output from frequency to phase. The reason that this is done is that it makes more sense to model the PLL in terms of phases and not frequencies to help model the phase detector. If the frequency output is sought, then it is only necessary to multiply the transfer function by a factor of ***s***, which corresponds to differentiation. So the phase-frequency detector not only causes the input phases to be equal, but also the input frequencies, since they are related.

Phase Frequency Detector Structure and Theoretical Operation

Simplified Structure of the PFD and Charge Pump

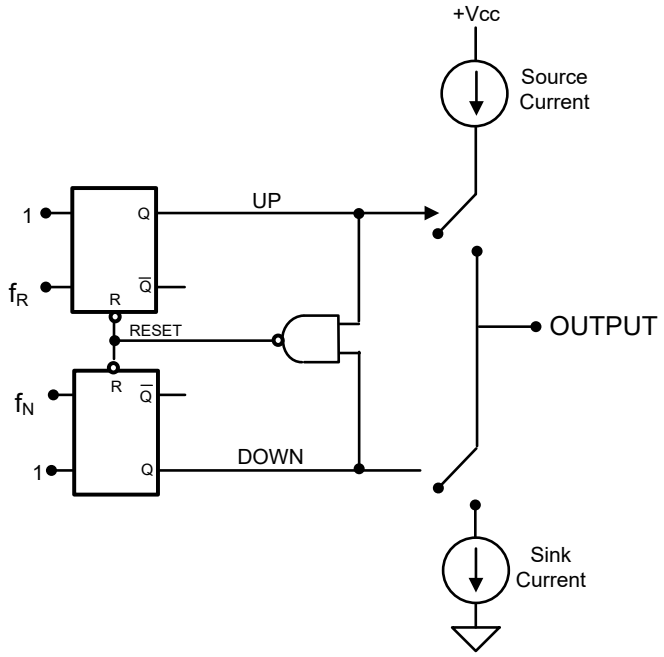


Figure 6.4 *Phase/Frequency Detector and Charge Pump*

An implementation of the PFD and charge pump is shown in Figure 6.4 with f_N representing the signal from the N divider and f_R the signal of the *R* divider. The circuit has the three possible states of the source current enabled, the sink current enabled, or both currents disabled. However, the state of both currents enabled is not allowed because if both the UP and DOWN signals were high, it would reset the flip-flops and causing both switches to be open.

The circuit in Figure 6.4 is said to have positive *phase detector polarity* because a positive phase error leads to a positive correction current. On many PLLs, it is possible to invert the polarity of the phase detector so that the behavior between the sink and source currents is reversed. When this is done, the phase detector is said to have a negative phase detector polarity. This feature is often useful when using active filters.

Simplified Operation of the PFD

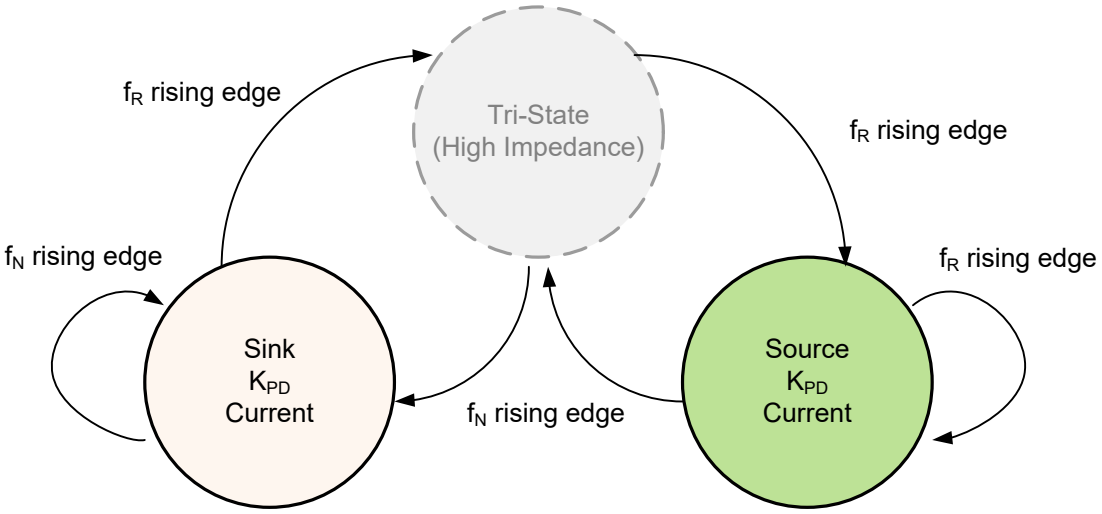


Figure 6.5 *States Diagram of the Phase Frequency Detector*

A simplified time-averaged output of the PFD with respect to phase error between the N and R divider outputs $\Delta\phi$ is shown below.

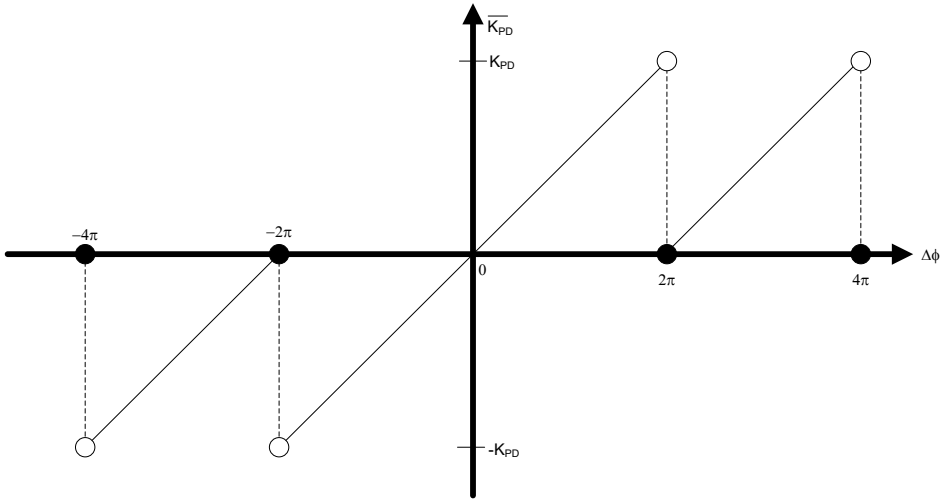


Figure 6.6 *Simplified Time-Averaged Output of the Phase Detector*

The PFD can lock to any phase error, but there are some performance considerations if the phase error is very small or if the phase error exceeds 2π. These cases are discussed now.

Operation in the Linear Region -2π < | Δϕ | < 2π

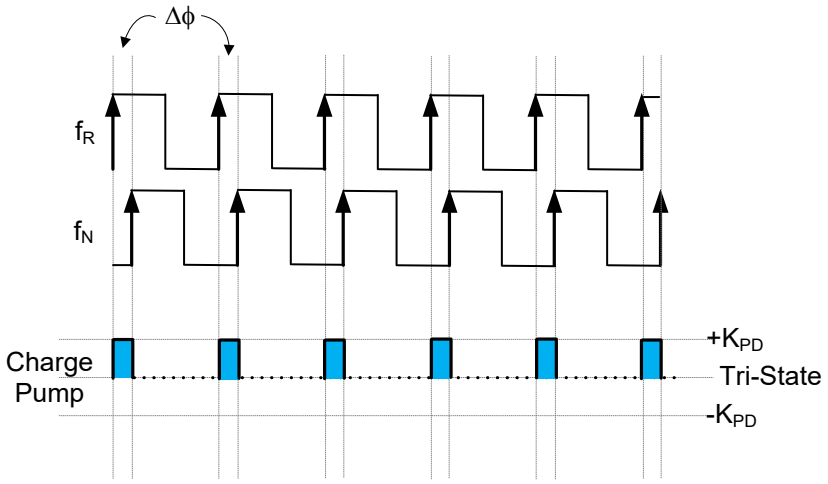


Figure 6.7 *PFD Output for an Error Less than 2π*

Figure 6.6 shows the time averaged output of the phase detector. The slope of this line, $\overline{K_{PD}}$, corresponds to the time-averaged charge pump gain and can be calculated as follows:

$$\overline{K_{PD}} = \frac{K_{PD} - (-K_{PD})}{2\pi - (-2\pi)} = \frac{K_{PD}}{2\pi} \qquad \textbf{(6.1)}$$

For this equation, there is debate over the division by a factor of 2π. Although it is technically correct to include this factor, it is typically left out because most calculations involve multiplying it by the VCO gain, which contains a factor of 2π to convert it from MHz/volt to MRad/volt. Knowing that these will cancel, this book will use the practical definition of disregarding this factor rather than the academic version of this formula in order to simplify calculations and reduce the possibility for round off errors.

$$\overline{K_{PD}} = K_{PD} \cdot \Delta\phi \qquad \textbf{(6.2)}$$

Operation near the Dead Zone of the Linear Region

When operating near zero phase error, the structure of the phase detector becomes more relevant and there is more interest in real-world features such unequal sink and source currents as well as the unequal turn on times of the sink and source currents. To discuss this, Figure 6.8 shows a more detailed diagram of the phase detector.

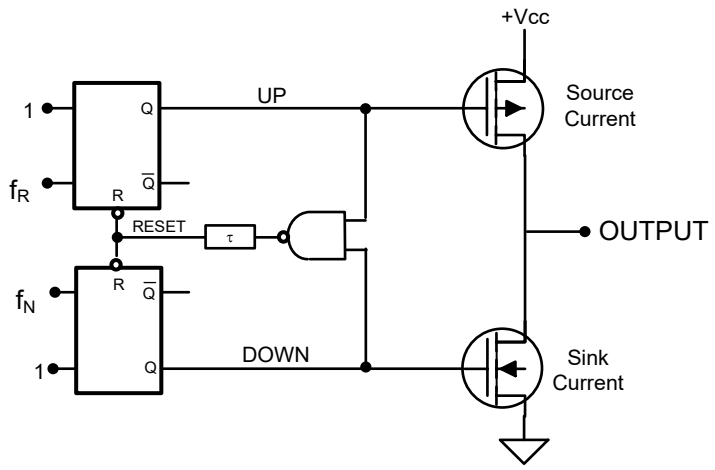


Figure 6.8 *Detailed Phase Detector Drawing*

Figure 6.9 shows the impact of the non-zero turn on times of the sink and source currents as well as their mismatch.

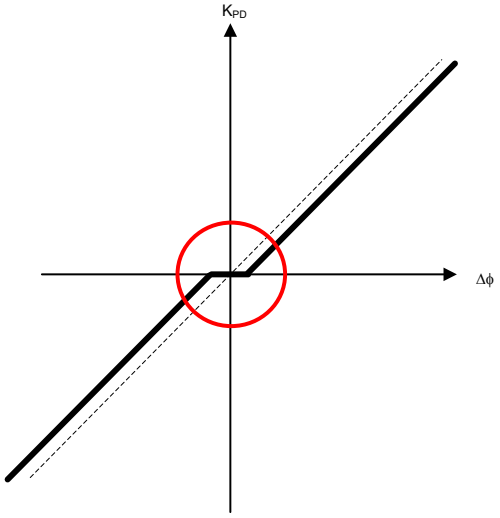


Figure 6.9 *Non-Ideal Charge Pump Operating Near Zero Phase Error*

Near zero phase error the nonzero turn on times of sink and source MOS devices significantly reduces the gain from the ideal value. This area of operation of the phase is known as the *dead zone*. In this region, the charge pump gain tends to be very low which makes the loop unable to suppress the VCO noise. Furthermore, the phase detector can look nonlinear and lead to high phase noise and fractional spurs. The strategy in most PFD designs is to avoid this dead zone.

There are some common strategies to deal with the dead zone. One method is to introduce a bleed current that pulls the phase detector away from operating with zero phase error. Another is to introduce a minimum on time for the phase detector to ensure that it operates away from a phase error that is too small, and a third is to introduce a small delay τ, to de-emphasize nonzero turn on times for the sink and source devices in the charge pump as shown in Figure 6.10.

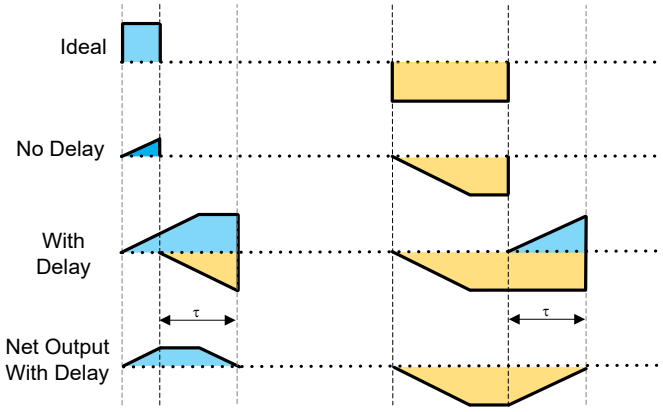


Figure 6.10 *PFD with Delay to Reduce Dead Zone*

If the rise and fall times of the MOS devices are identical, then the total area under the curve will be identical to the ideal area provided the delay is longer than the turn on time of these MOS devices and that the phase error in question is greater than the rise time. For purposes of comparing the phase error, express in terms of absolute time, not a phase error.

$$\Delta t = K_{PD} \cdot \frac{\Delta\phi}{2\pi \cdot f_{PD}} \tag{6.3}$$

Phase Error	***Ideal***	***No Delay***	***With Delay***
$\lvert\Delta t\rvert < t_R$	$K_{PD} \cdot \Delta t$	$K_{PD} \cdot \frac{\Delta t^2}{2 \cdot t_R}$	$K_{PD} \cdot \frac{\Delta t^2}{t_R}$
$\lvert\Delta t\rvert \geq t_R$		$K_{PD} \cdot \Delta t - K_{PD} \cdot t_R / 2 \cdot sgn(\Delta t)$	$K_{PD} \cdot \Delta t$

Table 6.1 *Charge Injected for Phase Error of Δt*

Operation Out of the Linear Region, $|\Delta t| \geq t_R$:

At first glance, it may seem absurd to talk about a phase greater than 2π, but what this really means is that one counter is having more rising edges than another, which typically implies that the inputs to the phase detector are not the same frequency and the PLL is not in lock. In this case, the PFD does put current in the correct direction, but the magnitude does not track the phase error. Two phenomenon of interest in this situation are cycle slipping and the time-averaged duty cycle of the phase detector.

Cycle Slipping

When one of the rising edges of one of the inputs to the phase detector does not get counted, this is known as a cycle slip. One situation where this comes up is if the N divider is changed abruptly to change the VCO frequency and the input frequencies to the phase detector are therefore different. This causes degradation in the lock time.

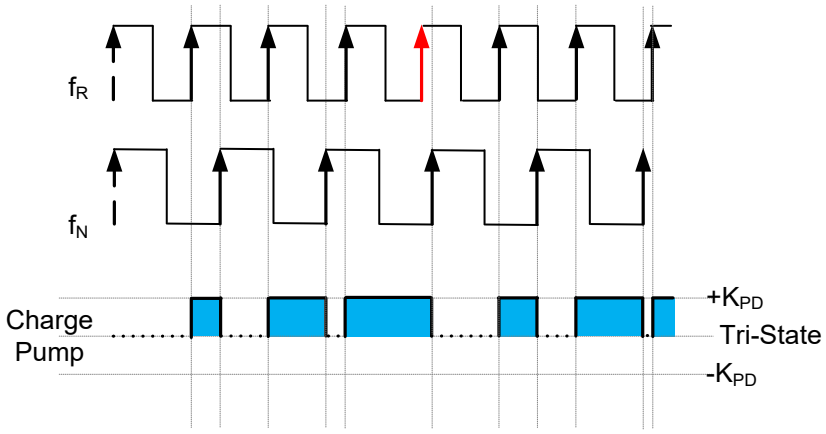


Figure 6.11 *Cycle Slip Example Assuming 0 Hz Loop Bandwidth*

Figure 6.11 shows situation when the N divider is abruptly changed to a higher value in order to direct the VCO to a higher frequency. As the duty cycle increases, eventually one cycle of the R divider is not counted, which causes the duty cycle of the charge pump to go back to a lower state. This is known as a *cycle slip*. The PFD does recover, but this increase the lock time. If the loop bandwidth is wide enough, the PLL can track this before the cycle slip happens, but this depends on the ratio of the phase detector frequency to the loop bandwidth.

In order to calculate the time to the first cycle slip, it is necessary to find the time when the faster counter will get one cycle ahead of the slower divider. For instance, if the N divider output was faster than the R divider output, the equation would be as follows.

$$(t + 1) \cdot f_R = t \cdot f_N \qquad \textbf{(6.4)}$$

If it was the case that the R divider output frequency was higher, then just switch the frequencies around. Solving these equations gives the following conditions for the first cycle slip.

$$t \geq \begin{cases} \infty & f_N = f_R \\ \dfrac{f_R}{f_N - f_R} & f_R < f_N \\ \dfrac{f_N}{f_R - f_N} & f_R > f_N \end{cases} \quad \textbf{(6.5)}$$

Calculation of Duty Cycle When Inputs Differ in Frequency

If two inputs to the phase detector differ in frequency, there are situations when the duty cycle of the phase detector would be of interest. One such situation would be if one was to construct a lock detect circuit. In order to calculate the duty cycle, make the simplifying assumption that loop bandwidth is wide enough to avoid cycle slipping. Also, without loss of generality, one can assume that the R divider output is greater than the N divider. If not, then swap the names and do the same analysis. Finally, assume that both the R and N dividers start off in phase. Under these assumptions, the phase at the output of the R divider after one cycle would be:

$$\phi_R = f_R \cdot \left(1/f_R\right) = 1 \quad \textbf{(6.6)}$$

The phase at the output of the N divider after this same period of time can also be calculated.

$$\phi_N = f_N \cdot \left(1/f_R\right) = f_N/f_R \quad \textbf{(6.7)}$$

Assuming the magnitude of the phase error does not exceed 2π, the time-averaged phase error of the PFD, expressed in cycles (not radians), can be calculated as:

$$\overline{\Delta\phi} = \begin{cases} 1 - f_N/f_R & f_N \leq f_R \\ 1 - f_R/f_N & f_N > f_R \end{cases} \quad \textbf{(6.8)}$$

As the ratio becomes infinite, the duty cycle approaches 100%. If the ratio of the input frequencies is two, then the duty cycle is 50%. For ratios above 2, it makes no difference if we assume there is cycle slipping or not. However, for ratios below two, assuming a 0 Hz bandwidth as opposed to no cycle slipping does make a difference.

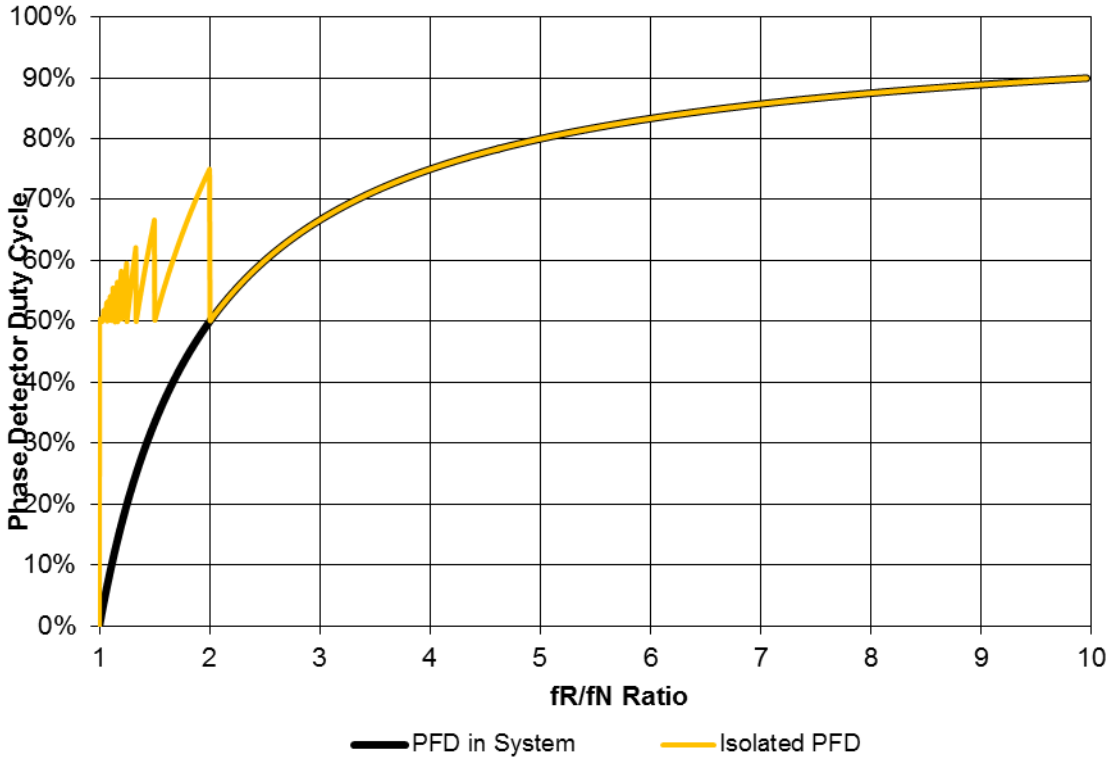


Figure 6.12 *Duty Cycle of the PFD for Inputs of Unequal Frequency*

For purposes of measuring the charge pump current, it is important to be aware of this duty cycle. Even if the ratio of these frequencies is ten, still the duty cycle of the charge pump is only 90%. The best way to do this is to actually remove the input to the N counter completely and set the N counter value to the maximum value. Theoretically, the N counter value should not matter, but if there is no signal there, there could be some self-oscillation at this pin. To see the sink current, invert the polarity of the phase detector.

The Continuous Time Approximation

It greatly simplifies calculations to model the charge pump current as a continuous current with a magnitude equal to the time-averaged value of these currents from the charge pump. However, the phase/frequency detector technically puts out a pulse width modulated signal and not a continuous current. This approximation is referred to as the *continuous time approximation* and is a valid provided that the loop bandwidth is no more than about one-

tenth of the phase detector frequency. Reference [2] goes into the justification for this result. In practice, one will start to see the loop go unstable when the loop bandwidth reaches about one-third of the phase detector frequency and would probably never want to exceed one-fifth the phase detector frequency to avoid any issues. Between one-tenth and one-fifth, the PLL will probably still lock, but the performance may be degraded. Specifically, increasing the loop bandwidth beyond one-tenth of the phase detector frequency might not yield the expected improvement in lock time. Also, spurs might have a cusping effect due to this sampling. If the loop bandwidth is less than about $1/100^{th}$ of the phase detector frequency, then the lock time could be degraded due to cycle slipping, which will be discussed in a later chapter. It will also be shown in a later chapter why the discrete sampling action of the phase detector causes the phase detector to get noisier at higher phase detector frequencies.

Conclusion

This chapter has discussed the PFD (Phase Frequency Detector) and has given some characterization on how it performs for different types of inputs. It is important to also remember that most of the time that this book refers to the PFD, it is meant to also include the charge pump. When charge pump is referred to, it is just the devices sinking or sourcing the current. Also, the gain of the PFD in this book will be defined as the charge pump gain. Other references may divide by a factor of 2π, but it is commonly done so in industry as this factor gets cancelled out by another factor of 2π in the VCO gain.

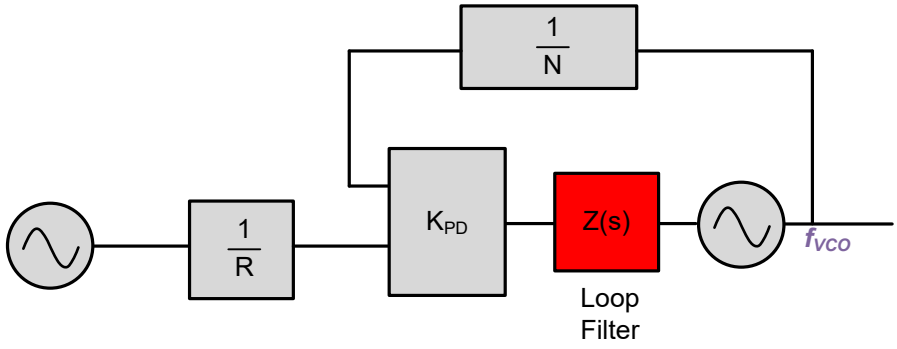
References

[1] Best, Roland E.,*Phase-Lock Loop Theory, Design, Applications*, 3rd. ed, McGraw-Hill 1995

[2] Gardner, F.M., *Charge-Pump Phase-Lock Loops*, IEEE Trans. Commun. vol. COM-28, pp. 1849 – 1858, Nov 1980

[3] Gardner, F.M. *Phaselock Techniques*, 2nd ed., John Wiley & Sons, 1980

Chapter 7 The Loop Filter



Introduction

The loop filter is a low pass filter that translates the charge pump output current into a tuning voltage for the VCO. However, not just any old low pass filter will do. The loop filter transfer function is actually a part of the entire closed loop PLL which also includes the N divider value, charge pump gain, and VCO gain. This closed loop transfer function has a profound impact on PLL switching speed, spurs, phase noise, and stability. There are many chapters in this book devoted to just loop filter design, so this chapter gives just a brief overview of loop filters.

Loop Filter Structure

A loop filter can be implemented with resistors and capacitors and a simple one is shown in the following figure.

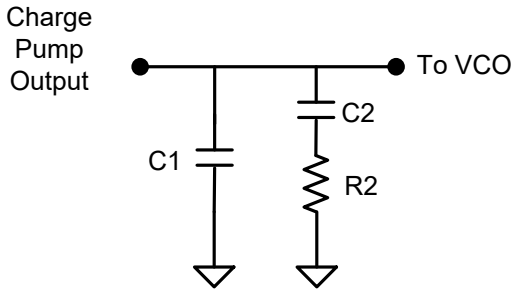


Figure 7.1 *Typical Loop Filter*

The transfer function for this loop filter in this case is simply the impedance of the loop filter which can be written as follows:

$$Z(s) = \frac{1 + s \cdot C2 \cdot R2}{(C1 + C2) \cdot s \cdot \left(1 + s \cdot \frac{C1 \cdot C2 \cdot R2}{C1 + C2}\right)} = \frac{1 + s \cdot T2}{A0 \cdot s \cdot (1 + s \cdot T1)} \qquad (7.1)$$

The zero, T2, is always necessary for stability of the system and there are also poles at zero and T1. In the case of a charge pump PLL, the pole T1 is necessary. Without this pole, the sharp corrections of the charge pump would be theoretically be directly converted to a voltage by the resistor R2 and cause huge voltage swings to the VCO input, which would lead to high phase noise and spurs. In reality, the VCO has an input capacitance that would act as capacitor C1 to lessen this effect, although it is not good practice to depend on it. Additional poles may be added to improve the ability to filter noise at farther offsets. The *loop filter order* is defined by the number of poles in the loop filter.

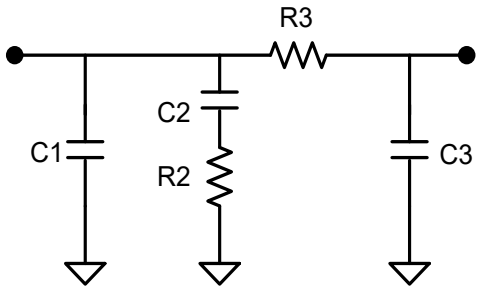


Figure 7.2 *A Third Order Loop Filter*

The Loop Filter Transfer Function

The generalized loop filter transfer function is defined as the output voltage at the VCO divided by current injected by the PLL charge pump and is shown by the following expression.

$$Z(s) = \frac{1 + s \cdot T2}{A0 \cdot s \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)} \qquad \textbf{(7.2)}$$

The pole, *T2*, and the zero, *T1*, are required. The poles *T3* and *T4* are optional and can be set to zero if they are not used. The order of the loop filter is defined by the number of poles it has, including the pole at zero. So the loop filter in Figure 7.2 is considered a third order loop filter, since it has a pole at zero, *T1*, and *T3*.

Passive and Active Loop Filters

In general, it is ideal to implement the loop filter with just resistors and capacitors for the reasons of cost and noise. However, in some situations, there may be reasons to use an active device such as an op-amp. The most common reason for this is when the charge pump cannot put out a high enough voltage. In either case, the analysis for such filter is the same using the poles and zeros of the transfer function.

Degenerate Loop Filters

Degenerate loop filters are ones that have zero valued components. This can be unintentional or intentional. One common situation when they may unintentionally arise is with partially integrated loop filters. One occurrence of this is when the filter has fixed component values for the higher poles formed by C3, C4, R3, or R4 and one tries to design for a loop bandwidth that is wider than possible. In this case, it can sometimes lead to a case where the capacitor C1 is zero.

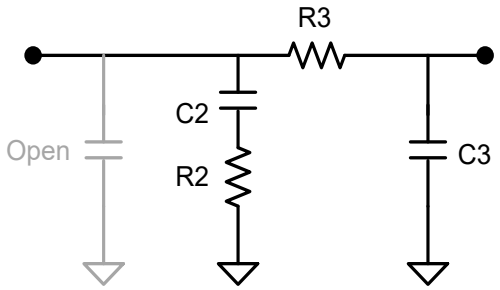


Figure 7.3 *Degenerate 3nd Order Loop Filter*

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In other situations, degenerate filters are intentionally created. One good reason for this is when one wants the board layout to accommodate different possibilities by putting a fourth order filter layout and then using zero value components if the extra poles are not needed. In Figure 7.4, the capacitance for C1 has been distributed between its normal spot and also a spot closer to the VCO. In some situations, this could yield better performance if the footprint on the PCB for C4 is much closer to the VCO than the footprint for C1.

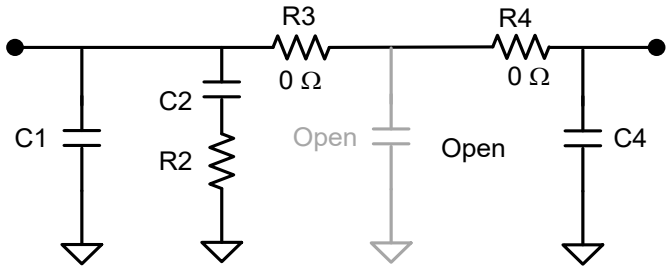


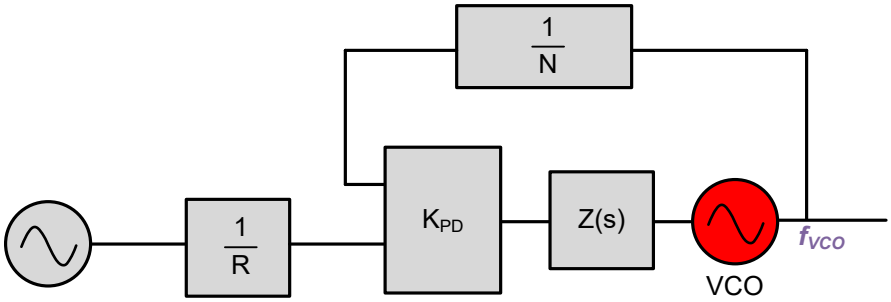
Figure 7.4 *Degenerate 4th Order Loop Filter*

For the purposes of defining these filters, they will be named based on the number of poles that they have, including the one at zero. For instance, Figure 7.3 is considered a 2nd order filter because it has two poles, but will be called a degenerate 3rd order filter because this is what it would be if the components were not all non-zero. Figure 7.4 is considered a 2nd order filter, but a degenerate 4th order filter.

Conclusion

The loop filter is key the performance of the PLL system and has a lot of degrees of flexibility for one to design. The loop filter can have different orders; this book assumes that it can be of order two, three, or four. There is no one loop filter that is right for every application as it involves performance trade-offs. Later chapters will cover the characteristics of the loop filter in much greater depth.

Chapter 8 Voltage Controlled Oscillators



Introduction

The voltage controlled oscillator (VCO) generates a frequency based on the input voltage; it can be thought of as a voltage to frequency converter. Although the principles of oscillators have already been covered and apply to voltage controlled oscillators, there are more details specific to VCOs that are worthy of study. This chapter discusses the performance characteristics of the VCO and then follows it up with the structure and implementation.

VCO Performance Characteristics

Frequency and Tuning Range

The range of frequencies that a VCO can produce is perhaps the most critical and relevant parameter for the VCO. A wider frequency range is always desirable, but this comes at the expense of phase noise. The minimum frequency is defined to be f_{VCOmin} and is produced by an input voltage of $V_{TuneMin}$. The maximum frequency is defined to be f_{VCOmax} and is produced by an input voltage of $V_{TuneMax}$. For some VCOs, going below the minimum tuning voltage can degrade the performance, or cause the VCO to not oscillate at all. The VCO frequency changes as a function of supply voltage, process, and temperature, so the guaranteed frequency range that is typically specified in a manufacturer's datasheet will typically be narrower than the actual range of the VCO.

VCO Gain

The gain of the VCO, K_{VCO}, is expressed in MHz/V and is how much the output frequency changes for a change in the input voltage. It is desirable for this to be constant over the VCO tuning range and if this is assumed this can be calculated as follows:

$$K_{VCO} = \frac{df_{VCO}}{dV_{Tune}} \approx \frac{f_{VCOmax} - f_{VCOmin}}{V_{TuneMax} - V_{TuneMin}} \quad \textbf{(8.1)}$$

The VCO gain can be calculated from measured by taking the slope of the tuning curve. If it is constant, then it can be calculated for the whole range. If not, it can be calculated by calculating the slope of the tuning curve in a small range about each V_{Tune} voltage or by breaking up the VCO tuning range can be broken up into several regions. The VCO gain has a significant impact on the closed loop transfer. If this gain changes significantly, by say a factor of 1.5 or more, it can throw the loop dynamics off. It is often possible to compensate for this with the charge pump gain.

Supply Voltage, Pushing, and Power Supply Noise Rejection

The supply can impact the performance of the VCO. *Pushing* refers to how much a change in voltage at the power supply pins of the VCO impact the output frequency and is typically measured in MHz/V. It is generally desirable to have this pushing to be lower. The first reason is that if there is an abrupt change in voltage, it could cause a glitch in the VCO frequency which would then need to settle out. The other reason is that any noise voltage on the power supply pins gets multiplied by the pushing goes to the output of the VCO. If the gain at this pin is high, then the noise at the output of the VCO will be worse.

Pulling

Pulling refers to how much the VCO frequency will shift when a load is placed on the output. One example of where this can be an issue is in a circuit when the power amplifier is first turned on. This changes the load presented to the VCO and can cause a frequency disturbance that needs to settle out.

Harmonics

VCOs generate harmonics, which occur at a multiple of the out frequency. In general, these are considered undesirable. The first exception to this is if the desired output is a square wave, which is very rich in odd harmonics. The other exception is when one wants to intentionally lock the PLL to one of these harmonics in order to get a higher frequency. In this case, a higher harmonic of the VCO is intentionally used as the intended signal. The drawback of this approach is that a lot of power is sacrificed.

Other Issues with VCOs

- Output power can vary with frequency, voltage, and temperature.
- VCO gain can vary with frequency, voltage, and temperature.
- VCO tank circuit can interact with loop filter if there is insufficient isolation
- Some VCOs may have high leakage currents, especially if their minimum tuning voltage is violated.
- Some VCOs may not oscillate if the tuning voltage is 0 V.
- VCOs typically have an input capacitance, which adds in to the loop filter. Typically this is the varactor diode and whatever is in parallel with this.

Relating the VCO to a Pendulum

Although the concept of an amplifier with a filter in the feedback path does apply to a VCO, this is a hard way to visualize the VCO. This is because transistors and FETs do not deal strictly with voltage gains. In order to understand VCOs, it is easier to understand them as a tank circuit and amplification circuitry.

VCO Tank Circuits

The tank circuit consists of an inductor and a capacitor and has many analogies to the pendulum. In the pendulum, the energy changes from potential to kinetic. For the tank circuit, the energy changes from the magnetic field in the inductor to the magnetic field in the capacitor plates. This can be thought of as an electronic spring, or others compare it to a pendulum.

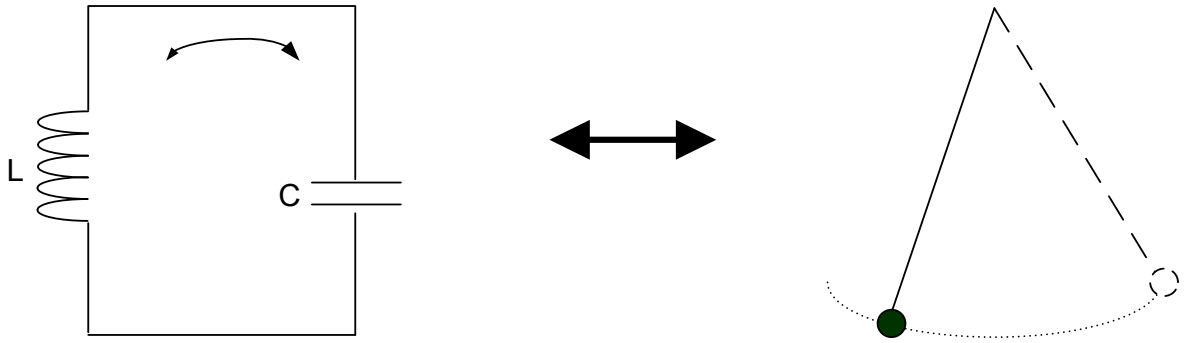


Figure 8.1 *Comparison of a VCO Tank Circuit to a Pendulum*

Characteristic	Conservation of Energy	Frequency
Pendulum	$m \cdot g \cdot l \cdot sin\theta + \frac{1}{2} \cdot m \cdot \left({}^{d\theta}/_{dt}\right)^2 = E$	$\sqrt{\frac{g}{l}}$
Tank Circuit	$\frac{1}{2} \cdot C \cdot V^2 + \frac{1}{2} \cdot L \cdot C^2 \cdot \left({}^{dV}/_{dT}\right)^2 = E$	$\frac{1}{\sqrt{L \cdot C}}$

Figure 8.2 *Tank Circuit and Pendulum Equations Assuming no Losses*

When the voltage is maximized in the tank circuit, the energy stored in the capacitor is maximized and the energy stored in the inductor is zero. When the voltage is minimized, the capacitor has no energy and the inductor has a maximum amount of energy in its magnetic field. The reason that this is called a tank circuit is that the energy inside sloshes between the inductor and the capacitor. If there were no parasitic resistances, this circuit could continue forever. This is very similar to the pendulum, where the potential energy is maximized and the kinetic energy is zero when the pendulum is at its highest position.

Likewise, when the pendulum is at its lowest position, the potential energy is minimized and the kinetic energy is maximized; the pendulum is moving at maximum speed at this time. However, there are resistances, so amplification is needed to sustain the oscillation.

Implementation of Amplifier

The traditional oscillator model of an amplifier and a delay in the feedback path is intuitive and easy to understand. However, a typical high frequency VCO does not typically use a voltage amplifier, but rather uses transistors devices with current gains. It is easier to visualize the principles of operation of this sort of oscillator as a tank circuit with some active circuit to sustain the oscillation. The basic idea is that the full voltage of the tank circuit drives the amplifier, but the output of the amplifier is lightly coupled to the tank circuit so as not to disturb the natural oscillations of the circuit. Aside from coupling in the amplified signal to the tank, the coupling network is also actually part of the tank as well. In Figure 8.3, capacitors C1 and C2 form the coupling network.

VCO Structure

Oscillator Topologies

The common types of VCOs are Colpitts, Clapp, and Hartley. The thing that makes them different is how the output of the amplifying device is applied to the tank circuit.

In the Colpitts design, there is a capacitive divider that forms part of the resonant capacitance to which this is applied.

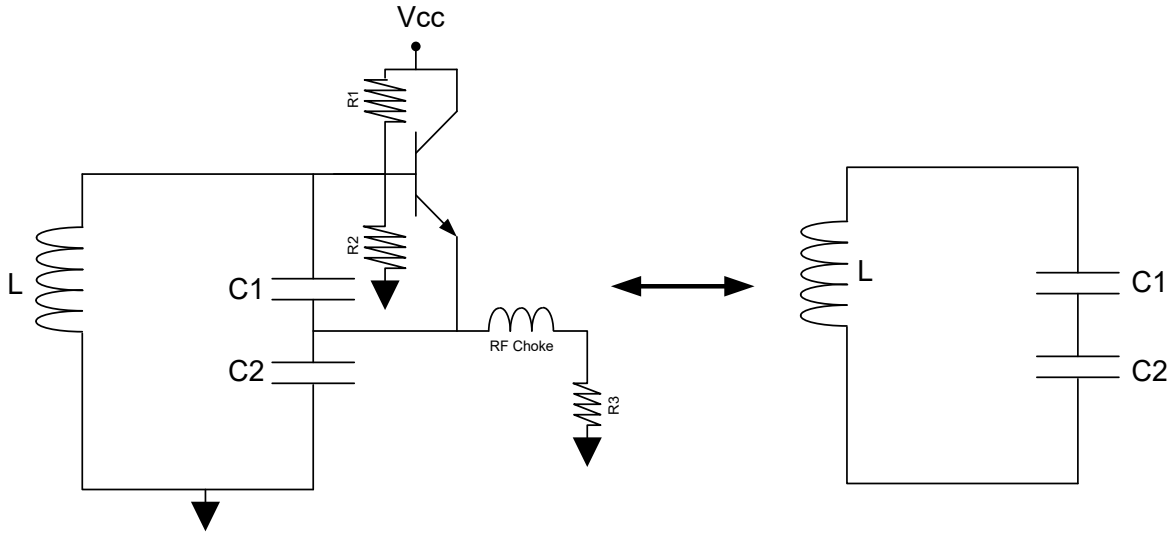


Figure 8.3 *Colpitts Oscillator and Its Tank Circuit*

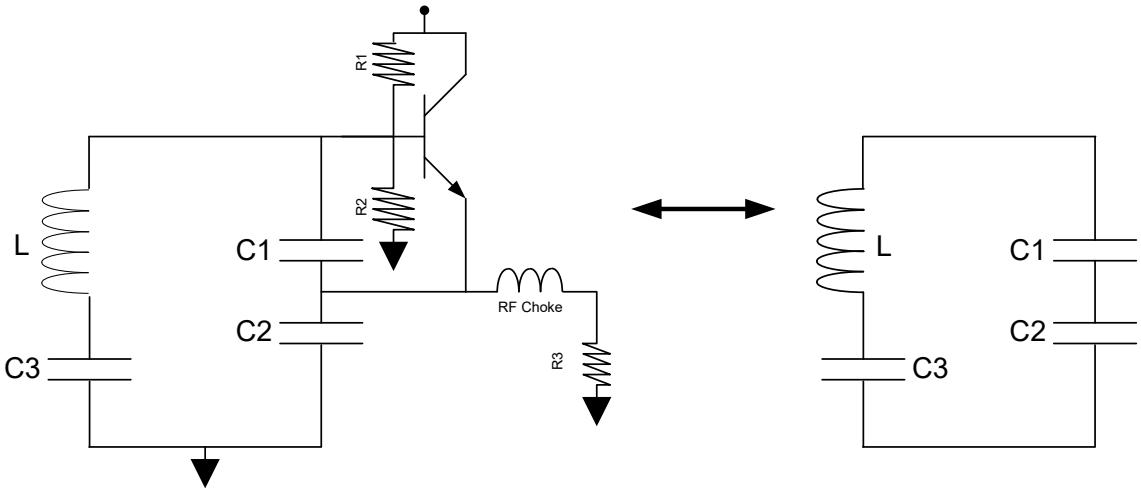


Figure 8.4 *Clapp Oscillator and its Tank Circuit*

The Clapp oscillator is very similar to the Colpitts oscillator, except for the fact that there is a series capacitor, C3 in this case, added in series with the inductor. It also goes by the name of Clapp-Gouriet and Series Tuned Colpitts Oscillator.

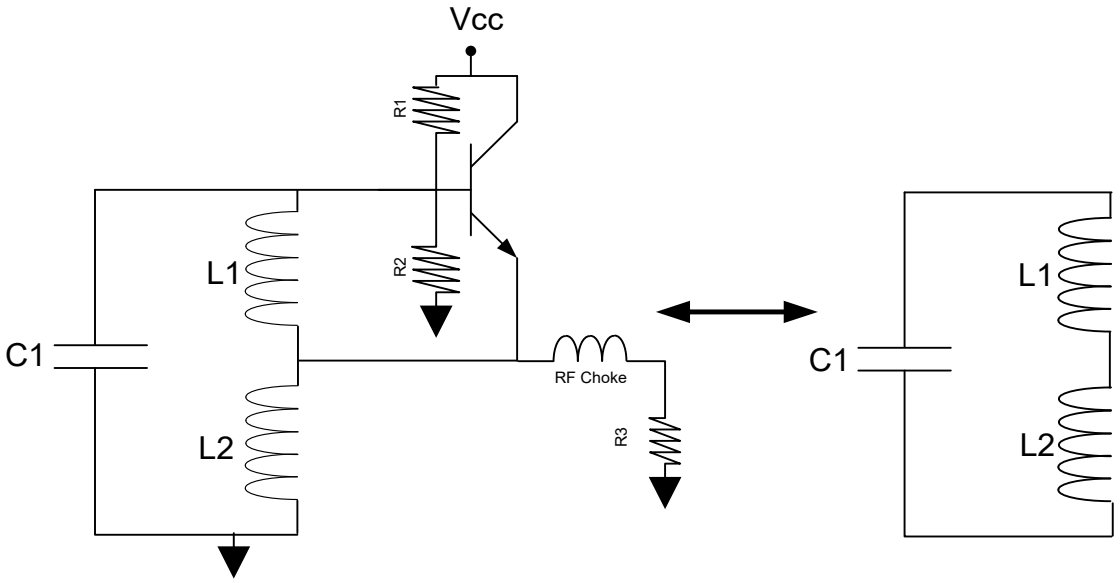


Figure 8.5 *Hartley Oscillator and its Tank Circuit*

In the Hartley oscillator, the feedback from the amplifier is applied to the inductor. To implement this, there are two inductors, and the voltage is applied between them. The sum of the two inductors forms the total inductance.

The Varactor Diode

The concept of the tank circuit has been discussed, but the circuits are only designed to operate at a single frequency; no mention has been made of what makes it possible to adjust the frequency. For the VCO, the varactor diode is the component that does this. It is a reverse biased diode that has a junction capacitance between the P and N junctions. Between these two junctions, there is a depletion layer. The width of this depletion layer widens as the reverse voltage across the diode is increases. Recall that for two parallel plates, the capacitance is inversely proportional to the distance between the plates. This situation applies to the varactor diode. As the voltage is increased, the capacitance becomes less in accordance with the following equation.

$$C_{Varactor}(V) = \frac{C_{Varactor}(0)}{(\alpha + V)^{\gamma}} \tag{8.2}$$

$\boldsymbol{C_{Varactor}(V)}$ is the capacitance of the varactor diode, $\boldsymbol{C_{Varactor}(0)}$ is the diode capacitance specified at a zero volts. $\boldsymbol{\alpha}$ is the diode potential voltage, $\boldsymbol{V}$ is the voltage applied, and $\boldsymbol{\gamma}$ is an exponent that is typically on the order of 0.5. For instance, here is some data for the 1SV229 varactor diode as modeled from the datasheet with $\boldsymbol{C_{Varactor}(0)}$ = 24 pF, $\boldsymbol{\alpha}$=2.8, and $\boldsymbol{\gamma}$=0.9.

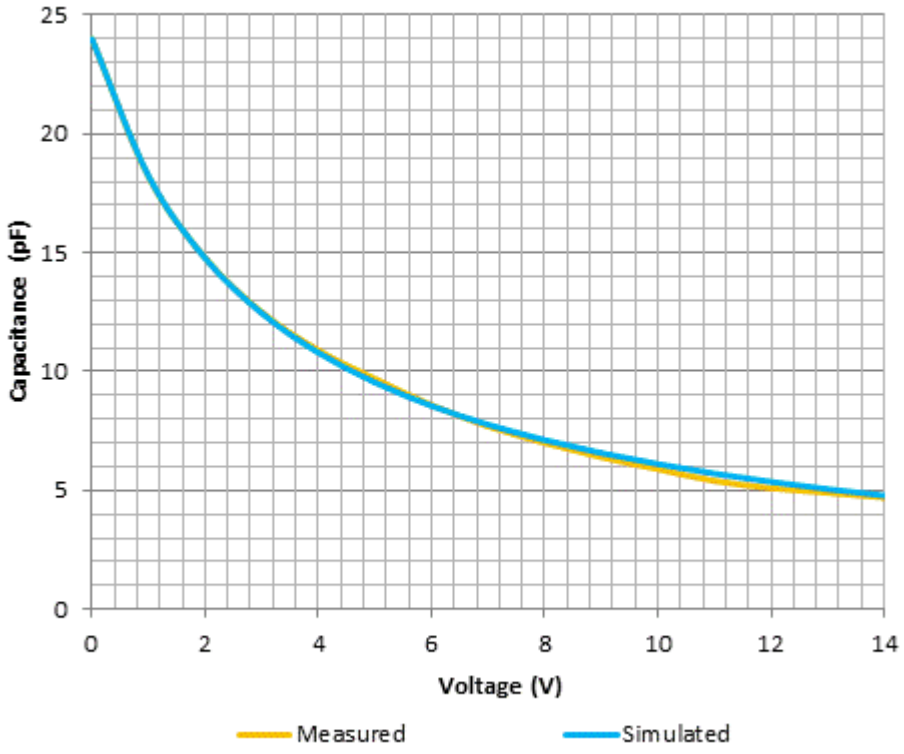


Figure 8.6 *Varactor Diode Capacitance for 1SV229 Diode*

The varactor diode typically is placed in parallel with one of the capacitors in the tank circuit. Maximum tuning range is attained if the varactor diode completely replaces a capacitor, however the phase noise is typically better there is some capacitance in parallel with the varactor diode. This is because the quality factor of a fixed value capacitor is typically higher than that for the varactor. There are many techniques for reducing the noise due to the varactor diode, such as putting multiple ones in parallel, which divides their noise resistance.

Oscillation Frequency Calculation

The theoretical oscillation frequency can be found once circuit inductance and capacitance are found. The value for the circuit inductance, ***L***, is straightforward to calculate. The capacitance, $\boldsymbol{C_{Equivalent}}$, is easier to find if one first simplifies the circuit by removing the amplifier and bias circuitry. The grounds can also be removed because the frequency is the same everywhere in the tank, so the placement of the ground can be ignored. This is done in Figure 8.3, Figure 8.4, and Figure 8.5.

Oscillator Type	Equivalent Inductance	Equivalent Capacitance
Colpitts	***L***	$\frac{1}{\frac{1}{C1} + \frac{1}{C2 + C_{Varactor}}}$
Clapp	***L***	$\frac{1}{\frac{1}{C1} + \frac{1}{C2} + \frac{1}{C3 + C_{Varactor}}}$
Hartley	***L1 + L2***	$C1 + C_{Varactor}$

Table 8.1 *Resonant Component Calculations*

The varactor diode capacitance typically adds to one of the capacitances, ***C1***, ***C2***, or ***C3***. Be aware that there are many different oscillator topologies and this formula for the equivalent capacitance is only good for the topologies shown in the examples.

The theoretical oscillation frequency is given by:

$$f_{VCO} = \frac{1}{2\pi\sqrt{L \cdot C_{Equivalent}}} \qquad \textbf{(8.3)}$$

Due to parasitic capacitances on the order of a few pF from the board and the transistor, the oscillation frequency can be lower than theoretically predicted.

VCO Example

For an example, consider the following VCO circuit, which is a Colpitts style oscillator. The only thing different is the series 1000 pF capacitor to keep the bias voltage of the transistor and VCO tuning voltage from fighting.

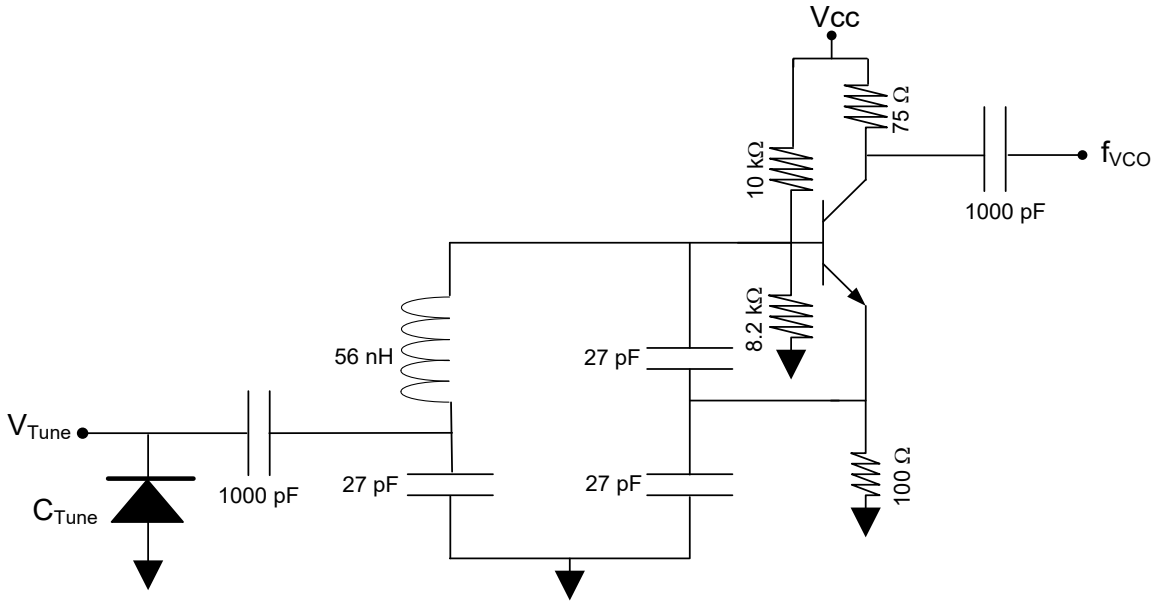


Figure 8.7 *VCO Circuit Example*

Using the analysis for frequency and comparing this to an actual measurement, we see that the measure frequency is lower than the simulated frequency as shown in Figure 8.8. The most likely explanation is parasitics. For instance, if one adds 2.5 pF to the equivalent capacitance, then there is a much better agreement between the measured and simulated frequencies. However, this shifts the VCO gain simulation a little off from the measurement. The best match between simulation and measured result is obtained by modeling this with an inductance value of 73 nH instead of 56 nH which matches the VCO frequency and gain very nicely. It may be hard to justify doing this although this VCO was done discretely on a PCB and perhaps some of the inductance could be due to the PCB trace length.

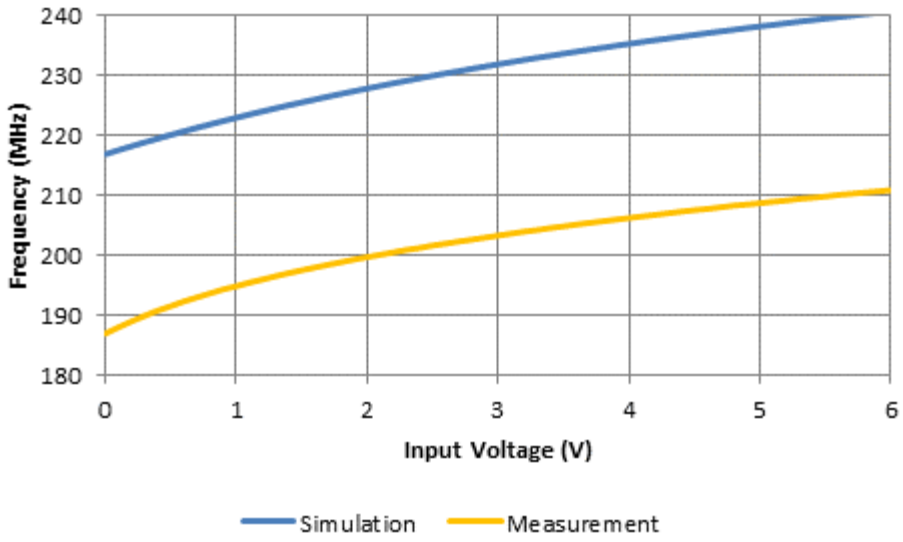


Figure 8.8 *VCO Frequency Simulation*

The gain can also be calculated. Note that at higher frequencies, the VCO gain drops off. This is typical of VCOs because the varactor diode capacitance changes tends to be overwhelmed by other capacitances when it is lower, which is the result of a higher tuning voltage.

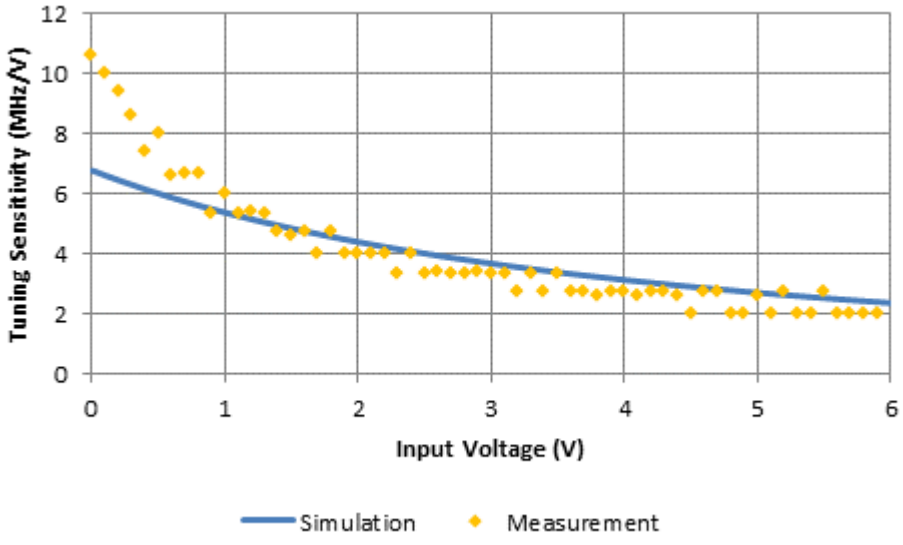


Figure 8.9 *VCO Gain Simulation*

Types of VCOs

So far, the resonant circuit of the oscillator was implemented with an inductor(s) and capacitors. However, there are actually many ways that resonant circuits can be implemented.

Circuit Type	Resonant Circuit	Tuning Range	Phase Noise
RC Oscillator	Resistor and Capacitor	Wide	Poor
Standard LC VCO	Inductor(s) and Capacitor(s)	Wide	Fair
Stripline VCO	Microstrip	Wide	Fair
SAW (Surface Acoustic Wave) Oscillator	SAW Filter	Narrow	Excellent
VCXO (Voltage Controlled Crystal Oscillator)	Crystal	Very Narrow	Best
CRO (Ceramic Resonator Oscillator)	Ceramic	Wide	Excellent
DRO (Dielectric Resonator Oscillator)	Dielectric	Wide	Excellent
YIG Oscillator	YIG Sphere	Very Wide	Good
Silicon VCO	Bond Wires, Internal Spiral Inductor, or External	Very Wide	Fair

Table 8.2 *Different Types of Oscillators*

Silicon VCOs

"I bought my last canned VCO." – Anonymous

Introduction

One VCO type that is worth special attention is the silicon VCO. VCOs integrated on semiconductor chips can have the advantages lower cost, smaller area, wider tuning range, programmable output dividers, and programmable output power. Silicon VCOs are able to achieve good phase noise and wide tuning range by switching in different resonant elements for different frequencies. This allows the frequency band to be broken up into smaller sub-bands, therefore reducing the VCO gain which in turn leads to better phase noise. The key elements of silicon VCOs are an inductive element, capacitor bank, and calibration circuitry.

Creating the Inductive Element

Silicon VCOs are typically LC oscillators and the inductance needs to be formed some way. The three common methods are to allow the user to use an external inductor, use the bond wires of the package, or use spiral inductors on the silicon die. External inductors give good flexibility to the user, but tend to be more limited in frequency since the bond wires also add inductance, that can be on the order of 1 nH. Bond wire inductors give flexibility to the manufacturer to tune the frequency, but also need to be tightly controlled in process or the VCO will have to tune much wider than is guaranteed in the datasheet. Spiral inductors are a popular method used and lend themselves well to allowing multiple inductor values which will be called *cores* to be selected between. If the element is bond wire or spiral inductor on silicon, the VCO frequency tends to be higher because it is harder to get larger inductor values on silicon or with bond wires. In some VCOs, it is necessary to use multiple inductors to get the required tuning range. In this case, multiple VCO cores can be created by having several different inductors switched in

Capacitor Bank

The capacitance of the resonant circuit for the silicon VCO is typically formed with a varactor diode, fixed capacitance, and a bank of switchable capacitors. The switched capacitor bank allows the VCO to divide the total bandwidth into several smaller bands, thus effectively reducing the VCO gain and improving phase noise. In the switched capacitor bank, the switch resistance may add some noise, so sometimes a fixed capacitance is used to improve the phase noise, although it sacrifices some VCO tuning range.

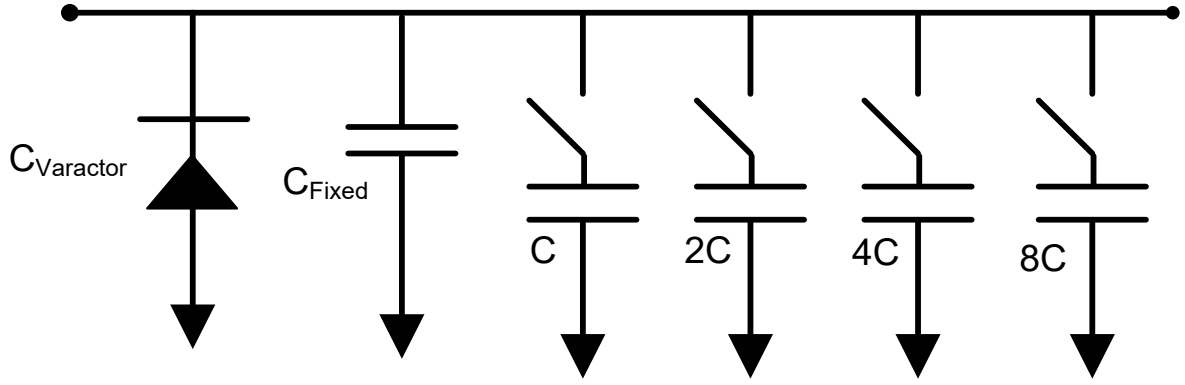


Figure 8.10 *Typical Switched Capacitor Bank for a VCO*

VCO Digital Frequency Calibration

Silicon VCOs that divide the frequency range into several different bands need a method to determine which frequency band to use. This sometimes is done manually by the user pulling pins high or low, but this does not work well for a large number of bands. It is more common for this calibration to be done automatically by the PLL device when the frequency

is changed. Automatic calibration is often typically transparent to the user and runs through various combinations of the capacitors and inductor cores to determine the combination that best centers the VCO frequency. The most fundamental method is to internally force the VCO tuning voltage to a fixed voltage and then search through the different capacitor combinations to find the most optimal one. The method to find the most optimal capacitor bank combination can be just a linear search that increments or decrements the capacitor bank value by one at each step, or a divide and conquer approach. For the divide and conquer approach, the capacitors are in the relative values of 1, 2, 4, 8, 16, and so on. Initially, the largest capacitor is switched in. If the achieved frequency of the VCO is higher than the target frequency, then the next largest capacitor is switched in. Otherwise, the largest capacitor is switched out, and the second largest capacitor is switched in. The frequency error in each step is half of what it was in the previous step. This process is repeated until the value of the smallest capacitor is set. Sometimes another calibration is run after the frequency calibration to optimize the phase noise.

Aside from finding the best frequency band, some silicon VCOs also use digital techniques to optimize phase noise. These routines are often run after the frequency calibration in order to get the best settings for the particular frequency band of interest. This phase noise calibration has the advantage that the settings can be optimized to account for changes in process, temperature, and frequency.

The circuitry that runs the calibration circuitry is typically run by a state machine clock that is derived by the OSCin frequency. If this frequency is too fast for the circuitry to run reliably, it is divided down. If it is too slow, it typically slows down the time it takes for the VCO to calibrate, that may or may not be an issue for the application. Figure 8.11 shows a divide and conquer frequency calibration followed by another phase noise calibration.

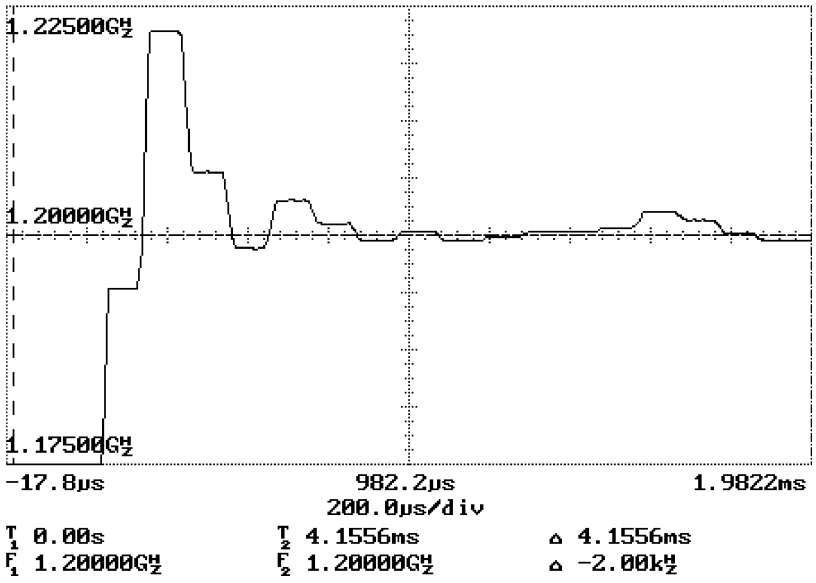


Figure 8.11 *Silicon VCO Using a Divide and Conquer Approach*

After the VCO calibration is done, the VCO is allowed to settle to the final frequency in analog mode. The challenge with the divide and conquer approach happens when the target frequency lies close to the border frequency between two capacitor codes. For this reason, and also to allow for temperature drift, the frequency ranges covered by each capacitor code must have some overlapping with the others. There are also other methods of dealing with this issue as well.

Output Dividers

One very common practice with integrating VCOs on silicon is to follow it up with a divider. This also greatly extends the frequency range of the device and also is done because on-chip inductors tend to be smaller, which implies higher VCO frequencies.

Conclusion

This chapter has discussed the architecture and common types of VCOs and has gone over some of fundamental concepts to understand how the VCO work. Many VCOs are commercially available and can be bought in a module. In general, higher frequency VCOs are more challenging and it is more common practice to buy these in module or integrated form.

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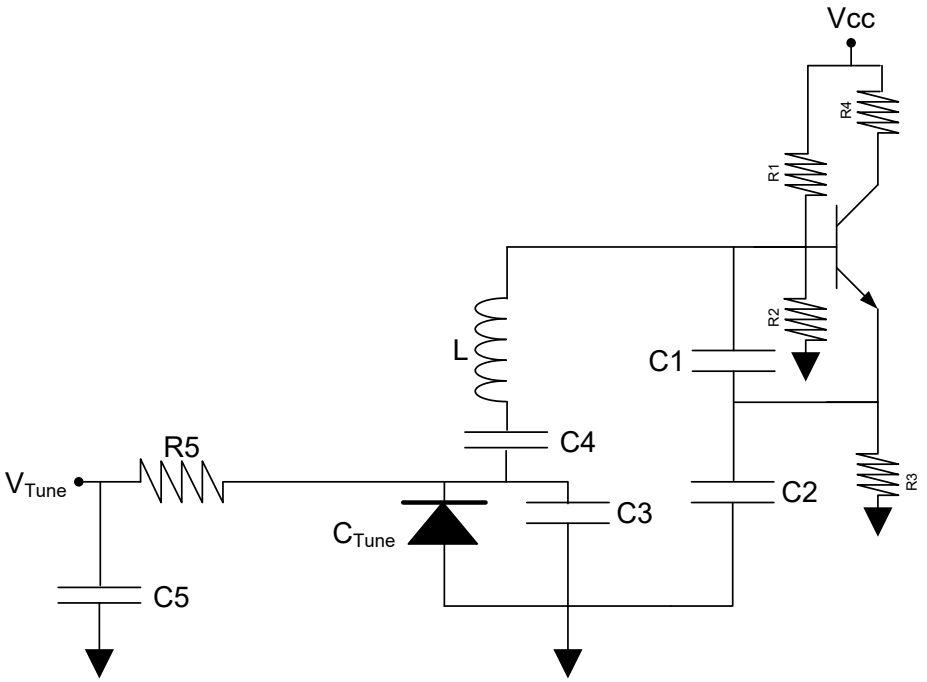
[6] Special Thanks to Thomas Mathews for informative conversations pertaining to VCOs.

Appendix A: A Closer Look at a Clapp Oscillator



Component	Primary Purpose	Value
C_{Vtune}	Varactor Diode, which is a voltage variable capacitance	32 pF (@ 0 V) 15 pF (@ 2 V) 12.5pF (@ 3V)
L	Inductor for the Tank	56 nH
C1	Couples Output into Tank and forms part of resonant tank.	27 pF
C2		27 pF
C3	Helps improve phase noise due to varactor diode resistance by adding in parallel to varactor.	Open
C4	Forms a DC block, so the tuning voltage does not fight the transistor bias level.	100 pF
C5	Works with R5 to prevent noise from VCO from exiting out through the tuning voltage. Especially important for a VCO module.	Open
R1	Transistor Biasing	10 kΩ
R2		8.2 kΩ
R3		10 kΩ
R4		75 Ω
R5	Isolates VCO tank circuit from the loop filter so that the loop filter capacitance will not shift the VCO frequency.	10 kΩ

Impact of Components on VCO Frequency

For this tank circuit, there are two additional components; the varactor diode and ***C4***. The simplified tank circuit is shown below.

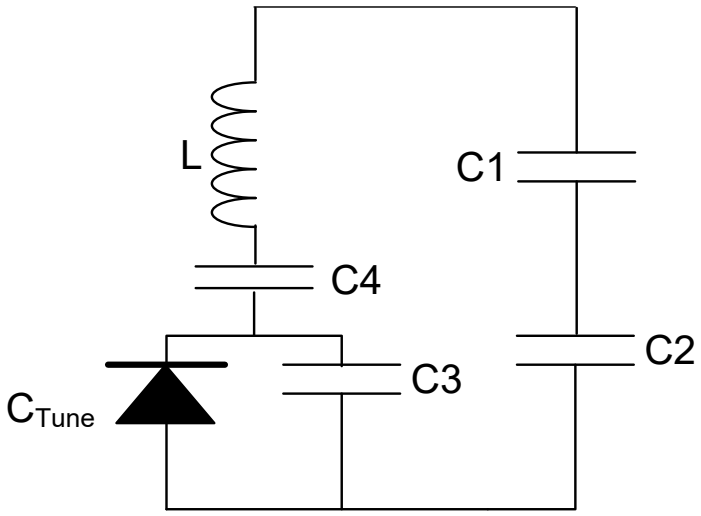


Figure 8.12 *Simplified Tank Circuit*

In order to better understand the impact of the components on this VCO Frequency, it was theoretically calculated assuming that the parasitic capacitance was zero. Then components were changed and the parasitic capacitance was calculated under these different circumstances to see how much it changed. The theoretical VCO frequency was calculated from the following formulae:

$$f_{VCO} = \frac{1}{2\pi\sqrt{L \cdot C_{Equivalent}}} \quad \textbf{(8.4)}$$

$$C_{Equivalent} = \frac{1}{\frac{1}{C1} + \frac{1}{C2} + \frac{1}{C3 + C_{tune}} + \frac{1}{C4}} \quad \textbf{(8.5)}$$

The impact of ***C4*** on frequency is very small, but it is easy to account for it, since it is just in series with the other capacitors. Note that in a string of series capacitors, the smallest capacitor value dominates.

Table 8.3 shows the result of changing the capacitors and inductor for the VCO and comparing the theoretical and actual results.

	C1	C2	C3	L	Measured Frequency			Theoretical Frequency (C_{Par}=0)	C_{Par}
	pF	pF	pF	nH	Min	V_{Tune}=2V	Max	V_{Tune}=2V	pF
#1	27	27	Open	12	385.3	430.3	445.3	564.1	4.8
#2	27	27	Open	56	204.8	227.8	235.2	261.1	2.1
#3	27	27	Open	120	139.8	155.1	160.0	178.4	2.1
#4	27	27	10	56	194.1	205.4	208.5	230.5	2.2
#5	15	150	Open	56	204.7	226.2	233.3	260.5	2.2
#6	18	56	Open	56	203.3	226.3	233.7	260.5	2.2

Table 8.3 *Actual vs. Theoretical VCO Frequencies*

The value for the parasitic capacitance, C_{Par}, can be extrapolated by comparing the theoretical and measured operating frequencies via the formula:

$$C_{Parasitic} = \frac{1}{(2\pi \cdot f_{Measured})^2 \cdot L} - C_{Equivalent} \qquad \textbf{(8.6)}$$

Once the parasitic capacitance was extrapolated when the varactor was at a fixed frequency of 2 volts, then the frequency range of the VCO could be calculated. In order to measure the extreme frequencies of the VCO, it was tuned to frequencies far above and below its tuning capabilities, and the actual frequency achieved was noted.

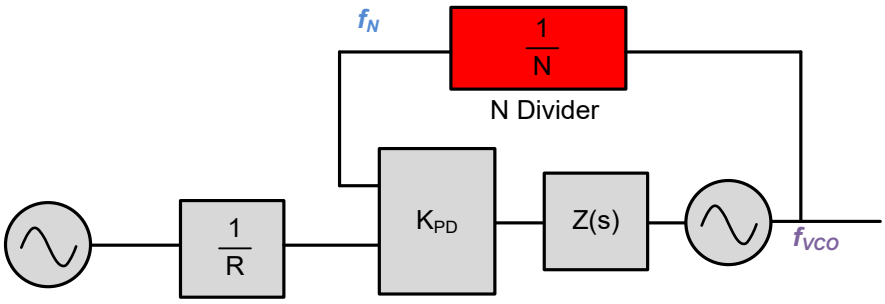
The first thing to note is that the calculated value for the parasitic capacitance is very constant, except for the first row, where this is higher frequency, but there could be other factors such as the inductor value changing. It is not shown in the table, but the minimum and maximum frequencies can also be predicted with textbook accuracy.

The first three lines of the table show the impact of changing the inductor value. Note that the absolute tuning range goes up with frequency, but remains roughly constant as a percentage. Comparing the fourth line to the third line, we see the impact of adding a capacitance in parallel with the varactor. This greatly reduces the tuning range, but will be shown later to improve phase noise slightly in the $1/f^2$ region, as Lesson's equation would theoretically predict.

The last two lines are dealing with the coupling capacitors in the tank. They were chosen to keep their series value roughly constant, and the frequency does not shift as one would theoretically expect.

When the output frequency is high, then there are other effects that cause the calculated parasitic capacitance to be higher. For the second and third lines, and for the rest of the table, there is textbook agreement. This shows how powerful this parasitic capacitance can be as a modeling tool. Note also that when the inductor is changed, this could be changing parasitics as well.

Chapter 9 Prescalers and High Frequency Dividers



Introduction

Until now, the ***N*** counter has been treated as some sort of black box that divides the VCO frequency and phase by ***N***. If the output frequency of the VCO is low, it can be implemented with a digital counter fabricated with a low frequency process, such as CMOS. This is ideal for low current and cost. However, a pure CMOS counter is not going to be operating at higher frequencies. To resolve this dilemma, fixed high frequency dividers called *prescalers* are often used to divide down the VCO frequency to a range that can be handled with a lower frequency process. These prescalers are typically implemented as a power of two divider followed with some additional circuitry. The most common implementations of prescalers are single modulus, dual modulus, and quadruple modulus.

Single Modulus Prescaler

For this approach, a single high frequency divider placed in front of a counter. The divider can either be integrated on the PLL chip or implemented with an external divide. This approach tends to be more popular in high frequencies where it is more difficult to implement more intricate approaches as well as older PLLs and low cost PLLs.

For notation purposes, upper case letters will be used to name counters and lower case letters will be used to denote the actual value of that counter, if it is programmable. For instance, ***b*** represents the actual value that the physical ***B*** counter is programmed to. If the counter value is fixed, then the upper case letter will denote the name and the value for that counter.

In this case, $\boldsymbol{N} = b \cdot P$, where ***b*** can be changed and ***P*** is fixed, typically to some power of two. This approach is straightforward and simple, but has the disadvantage that only ***N*** values that are an integer multiple of ***P*** can be synthesized. The channel spacing can be reduced to compensate for this, doing so degrades phase noise and spurs.

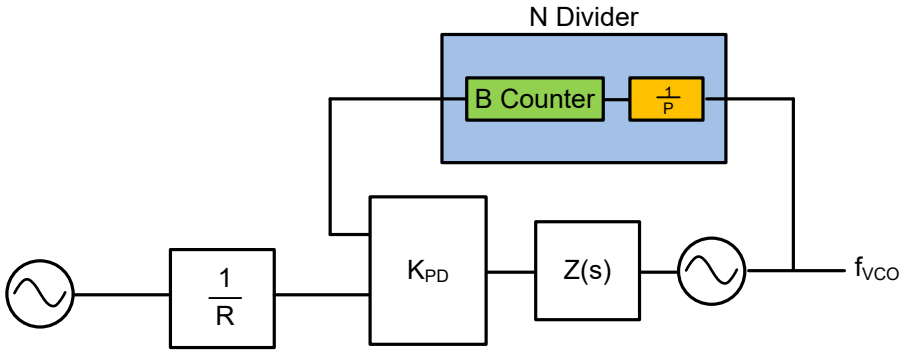


Figure 9.1 *Single Modulus Prescaler*

Dual Modulus Prescaler

In order not to sacrifice frequency resolution, a dual modulus prescaler is often used. These come in the form ***P/(P+1)***. For instance, a ***32/33*** prescaler has ***P = 32***. In actuality, there is really only one prescaler of size ***P***, and the ***P+1*** value is implemented by putting a pulse swallow function before the prescaler. Since the A counter controls whether or not the pulse swallow circuitry is active or not, it is often referred to as the swallow counter.

Operation begins with the ***P+1*** prescaler being engaged for a total of ***a*** cycles. It takes a total of *a·(P+1)* cycles for the A counter to count down to zero. There is also a B counter that also counts down at the same time as the A counter. After the A counter reaches a value of zero, the pulse swallow function is deactivated and the A counter stops counting. Since the B counter was counting down with the A counter, it has a remaining count of ***(b – a)***.

Now the B counter starts counting down with the prescaler value of ***P***. This takes *(b-a)·P* counts to finish up the count, at which time, all of the counters are reset, and the process is repeated. From this the fundamental equations can be derived:

$$N = (P + 1) \cdot a + P \cdot (b - a) = P \cdot b + a \qquad \textbf{(9.1)}$$

$$b = Floor(N/P) \qquad \textbf{(9.2)}$$

$$a = N \bmod P \qquad \textbf{(9.3)}$$

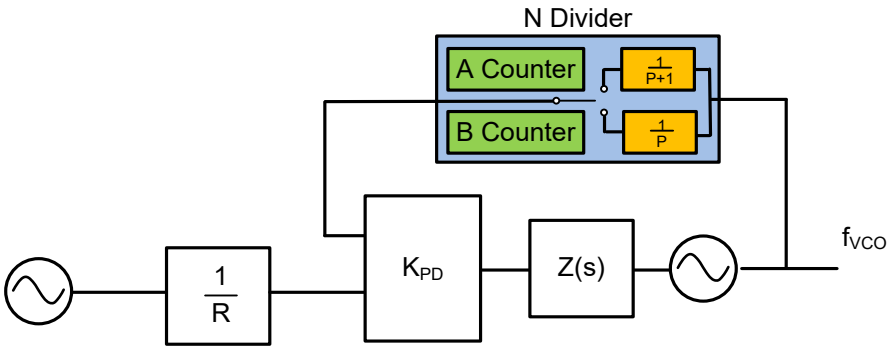


Figure 9.2 *Dual Modulus Prescaler*

The restriction that **b≥a** is required for proper operation. If this constraint is not satisfied, the counters reset prematurely before the A counter reaches zero and the wrong N value is achieved. ***N*** values for which ***b<a*** do not satisfy this criteria are referred to as illegal divide ratios. It turns out that if N is greater than a limit called the minimum continuous divide ratio, then it will not be an illegal divide ratio.

Quadruple Modulus Prescalers

In order to achieve a lower minimum continuous divide ratio, the quadruple modulus prescaler is often used. In the case of a quadruple modulus prescaler, there are four prescalers, but only three are used to produce any given ***N*** value. Commonly, but not always, these four prescalers are of values ***P***, ***P+1***, ***P+4***, and ***P+5***, and are implemented with a single prescaler, a pulse swallow circuit, and a four-pulse swallow circuit.

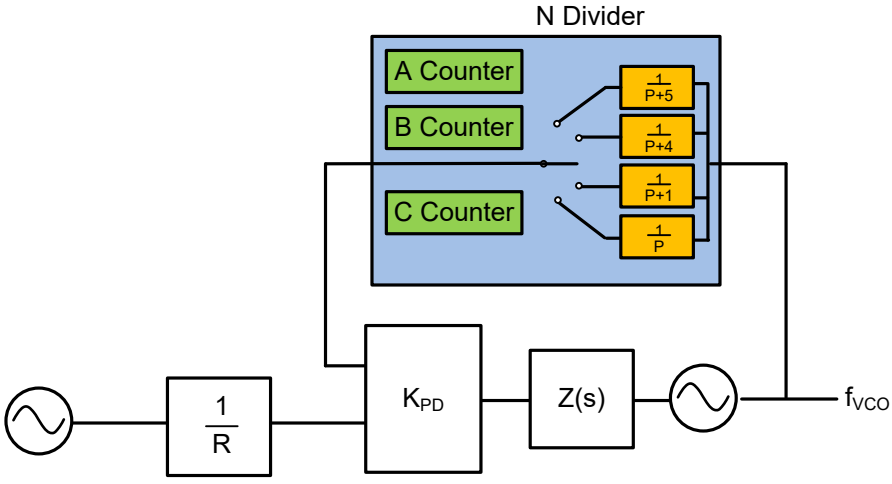


Figure 9.3 *Quadruple Modulus Prescaler*

The following table shows the three steps and how the prescalers are used in conjunction to produce the required ***N*** value. Regardless of whether or not ***b>=a***, the resulting ***N*** value is the same.

Step	If $b \geq a$		If b<a	
	Description	**Counts Required**	**Description**	**Counts Required**
1	The P+5 prescaler is engaged in order to decrement the A counter until a=0.	$a \cdot (P+5)$	The P+5 prescaler is engaged in order to decrement the B counter until b=0.	$b \cdot (P+5)$
2	The P+4 prescaler is engaged in order to decrement the B counter until b=0.	$(b-a) \cdot (P+4)$	The P+1 prescaler is engaged in order to decrement the A counter until a=0.	$(a-b) \cdot (P+1)$
3	The P prescaler is engaged in order to decrement the C counter until c=0.	$(c-b) \cdot P$	The P prescaler is engaged in order to decrement the C counter until c=0.	$(c-a) \cdot P$
	Total Counts	$P \cdot c + 4 \cdot b + a$	Total Counts	$P \cdot c + 4 \cdot b + a$

Table 9.1 *Typical Operation of a Quadruple Modulus Prescaler*

Observe that unlike the dual modulus prescaler, the quadruple modulus prescaler does not have the restriction that ***b≥a***. The restriction for the quadruple modulus prescaler is ***c >= max{a, b}***. ***N*** values that violate this rule are called illegal divide ratios. Even though the quadruple modulus prescaler has four potential values, only three of them will be used for any particular N value. The fundamental equation relating the *a*, *b*, and *c* values to the N counter value is:

$$b = Floor(N/P) \tag{9.4}$$

The values to be programmed into the A counter, B counter, and C counter can be found as follows:

$$a = N \bmod P \tag{9.5}$$

$$c = Floor(N/P) \tag{9.6}$$

$$b = \frac{N - c \cdot P - a}{4} \tag{9.7}$$

Minimum Continuous Divide Ratio

It turns out that for the dual modulus and quadruple modulus prescaler that all N values that are above a particular value, called the minimum continuous divide ratio, will be legal divide ratios. For the dual modulus prescaler, this is easy to calculate. Because ***a*** is the result of taking a number modulus ***P***, the maximum this number can be is ***P-1***. It therefore follows that if $b \geq P - 1$, the N value is legal. For the quadruple modulus prescaler, the maximum ***a*** can be is 3. By doing some numerical examples, the maximum that ***b*** can be is $max\{ P/4 - 1, 3 \}$. From this, the minimum continuous divide ratio for the quadruple modulus prescaler can be calculated.

Prescaler Type	Prescaler	Minimum Continuous Divide Ratio
Dual Modulus	4/5	12
	8/9	56
	16/17	240
	32/33	992
	64/65	4032
	128/129	16256
	P/(P+1)	P × (P-1)
Quadruple Modulus	4/5/8/9	12
	8/9/12/13	24
	16/17/20/21	48
	32/33/35/56	224
	64/65/68/69	960
	128/129/132/133	3968
	P/(P+1)/(P+4)/(P+5)	max{ P/4 - 1, 3 } × P

Table 9.2 *Minimum Continuous Divide Ratios*

Adjustments to Minimum Continuous Divide Ratio for Fractional Dividers

Fractional PLLs can introduce exceptions for both the dual modulus prescaler and the quadruple modulus prescaler. This is for several reasons. One reason for this is that fractional PLLs achieve an N value that is fractional by alternating the N counter value between two or more values. The sequence and different values that the fractional part goes through can change with the design of the part. For the desired fractional N counter to be legal, all of the values that the N counter switches between must also be legal. In addition to requirements brought on by the use of additional N counter values, there are additional intricacies of the fractional N architecture that can put additional requirements. In general, when dealing with fractional parts, there can be many exceptions, which often reduce the number of legal N counter values and raise the minimum continuous divide ratio.

Issues and Pitfalls with High Frequency Dividers

On the Pitfalls of Sensitivity

For PLLs that allow an external VCO, sensitivity of the N divider is a real world concern. The divider can miscount the power level of the input signal is too low or too high. The limit at which the device fails is referred to as *sensitivity*. Sensitivity changes as a function of process, temperature, voltage, and frequency and is typically displayed in curves in the datasheet. At the higher frequencies, the curve degrades due to process limitations. At lower frequencies, the curve can also degrade because of problems with the dividers making thresholding decisions due to the edge rate of the input signal being too low. At the lower frequencies, this limitation can sometimes be addressed by running a square wave instead of a sine wave into the high frequency input of the PLL. Sensitivity can vary considerably over process, voltage, and temperature, so it is best to operate far away from the typical operating curves. In other words, design to the datasheet limits and stay in the safe operating range.

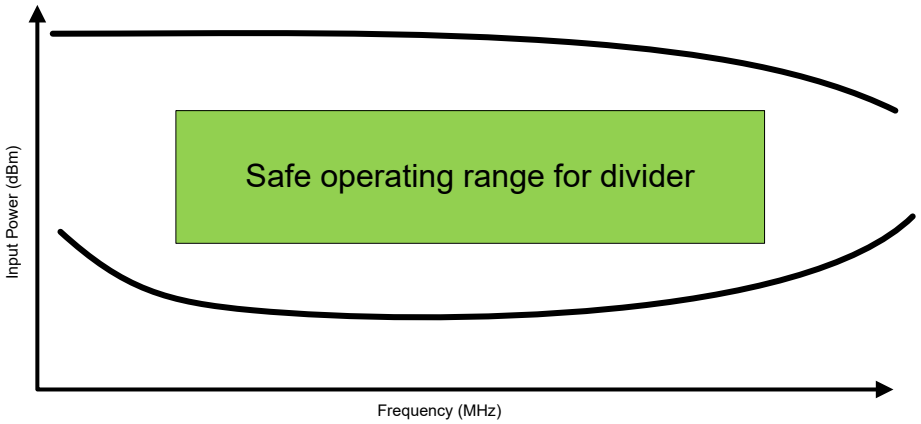


Figure 9.4 *Typical Sensitivity Curve for a PLL*

The sensitivity curve applies to both the desired signal from the VCO and all of its harmonics. VCO harmonics can especially be troublesome when a part designed for a very high operating frequency is used at a very low operating frequency. Unexpected sensitivity problems can also be agitated by poor matching between the VCO output and the high frequency input of the PLL. Although sensitivity issues are most common with the ***N*** counter, because it usually involves the higher frequency input, these same concepts apply to the ***R*** counter as well.

There are a few approaches to debugging sensitivity issues. Many devices have a way to access the output of the ***R*** and ***N*** dividers, which is excellent way of diagnosing and debugging sensitivity problems. Sensitivity related problems also tend to show a strong dependence on the Vcc voltage and temperature. If poor impedance matching is causing the sensitivity problem, then sometimes pressing one's finger on the part will temporarily make the problem go away. This is because the input impedance of the part is being impacted.

Sensitivity problems with either the ***N*** or ***R*** can cause spurs to appear, increase phase noise, or cause the PLL to tune to a different frequency than it is programmed to. In more severe cases, they can cause the PLL to steer the VCO to one of the power supply rails. ***N*** counter sensitivity problems usually cause the VCO to go higher than it should. ***R*** counter sensitivity problems usually cause the PLL to tune lower than it should. In either case, the VCO output is typically very noisy. Figure 9.5 shows a PLL locking much lower than it is programmed to lock due to an ***R*** counter sensitivity problem. It is also possible for the ***N*** counter to track a higher harmonic of the VCO signal, which causes the PLL to tune the VCO lower than it should. This problem is most common when parts are operated at frequencies much lower than they are designed to run at. One should be aware that it is possible to be operating within the datasheet specifications for sensitivity with a few dB of margin, and still have degraded phase noise as a result of a sensitivity problem. This is because the datasheet specification for sensitivity is a measurement of when the counters actually miscount, not when they become noisy.

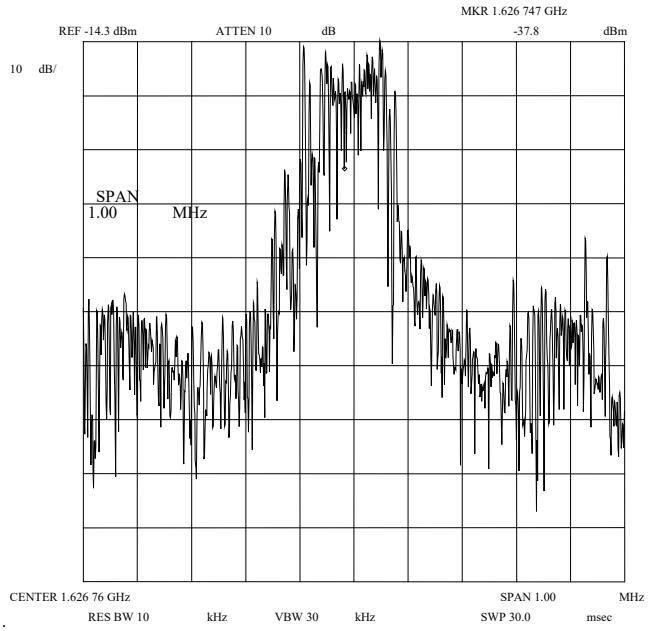


Figure 9.5 *PLL Locking to Wrong Frequency Due to R Counter Sensitivity Problem*

PLL Accidentally Locking to VCO Harmonics

All VCOs put out harmonics. If the harmonic levels are too high, the PLL may lock to them instead of the intended signal. But what is too high? The theoretical result can be found by looking at the sum of two sine waves and inspecting what amplitude of a harmonic causes a miscount. For instance, when considering the second harmonic, it is found that if the voltage level is exactly one-half of the fundamental, which is 6 dB down, the PLL would theoretically be just about to miscount.

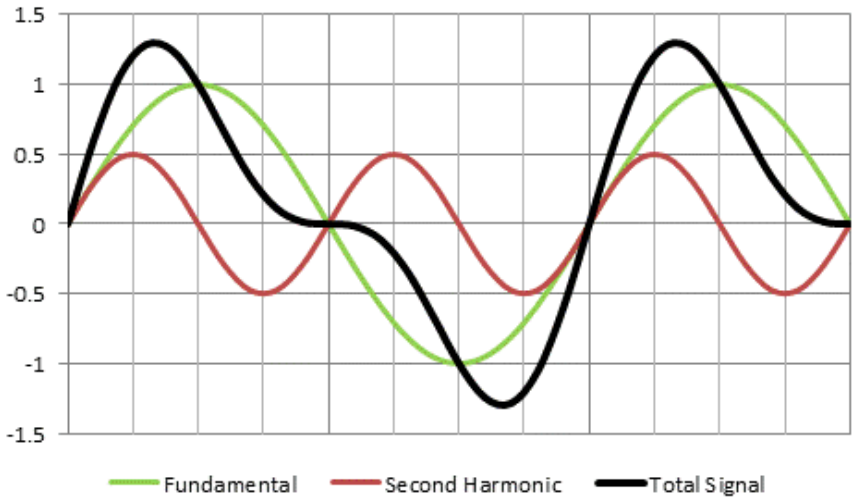


Figure 9.6 *Second Harmonic Illustration*

Assuming that these signals are in phase, the maximum tolerable harmonic for the higher order harmonics can also be calculated. Note that the even harmonics are much more of a problem than the odd harmonics. In fact, if the odd harmonics are in just the right mixture to make a square wave, the sensitivity is actually theoretically improved.

Harmonic	Maximum Tolerable Level (*dBc*)
2^{nd}	-6.0
3^{rd}	0.0
4^{th}	-12.0
5^{th}	-1.9
6^{th}	-15.6
7^{th}	-4.3
8^{th}	-5.3
9^{th}	-6.2
10^{th}	-7.0

Table 9.3 *Theoretical Maximum Tolerable Harmonics*

There are other factors that can influence the maximum tolerable levels for the harmonics. As the harmonics approach the maximum tolerable levels, it becomes easier for any noise riding on the signal to cause the counters to miscount. Furthermore, PLL sensitivity varies as a function of frequency and will probably be different for the fundamental and harmonic. The normalized sensitivity harmonic ($H_{SensNorm}$) gives a better indication of if the divider is going to be fooled into counting the harmonic instead of the carrier. It is found from the harmonic power ($P_{Harmonic}$), carrier power ($P_{Carrier}$), sensitivity to the carrier ($S_{Carrier}$) and sensitivity to the harmonic ($S_{Harmonic}$).

$$H_{SensNorm} = (P_{Harmonic} - P_{Carrier}) + (S_{Carrier} - S_{Harmonic}) \quad \textbf{(9.8)}$$

To test this concept, the VCO input of a LMX2326 PLL was driven with two signal generators. One signal generator simulated the fundamental frequency, where the second signal generator was used to simulate the second harmonic. It was found that the closer that the main signal was to the sensitivity limits, the more sensitive it was to the second harmonic. The sensitivity numbers used for the calculations here are actual measured data, not the datasheet limits, which tend to be much more conservative to accommodate for voltage, temperature, and process.

Sensitivity Margin	Max Tolerable Normalized Harmonic
1 dB	-12 dBc
5 dB	-5 dBc
10 dB	-2 dBc
20 dB	0 dBc

Table 9.4 *Maximum Tolerable Normalized Second Harmonic*

For instance, consider an application where the user is operating at 400 MHz output with a +2.0 dBm signal. Further suppose that the sensitivity limit on this part is measured to be –8 dBm at 400 MHz and –20 dBm at 800 MHz. This means that this application has 10 dB margin on the sensitivity and can tolerate a normalized harmonic of –2 dBc, which translates to a harmonic level of –12 dBc after the sensitivity difference is considered. However, this does not have any margin. If one was to add 5 dB margin, this would work out to –17 dBc. Note that this table is empirical and not exact, but does serve as a rough guideline as to what harmonic levels are tolerable.

Note that there is a discrepancy between the theoretical and measured results. Theoretically, a second harmonic of greater than –6 dBc would cause a miscount, yet this case was measured and it was found that 0 dBc was tolerable before considering sensitivity. The true answer probably lies somewhere between the theoretical and measured results, but is not critical to be exact because the whole goal is to stay away from these marginal designs.

The VCO Divider

Aside from the N divider, some PLLs will also have another divider after the VCO to extend the frequency range. Unlike the N divider, the duty cycle output on this matters a little more as this goes straight to the output; it is more than just rising edges of the output that matter. If the duty cycle is not 50%, this leads to a higher second harmonic. This is one reason why it is common for these dividers to be restricted to powers or multiples of two, so that a nice 50% duty cycle output can be obtained. There are some devices with VCO dividers that can do odd divides that have a 50% duty cycle, but these are less common.

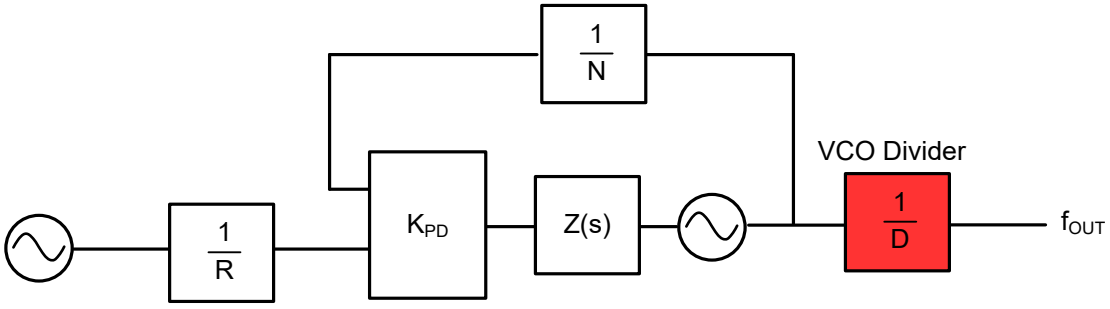
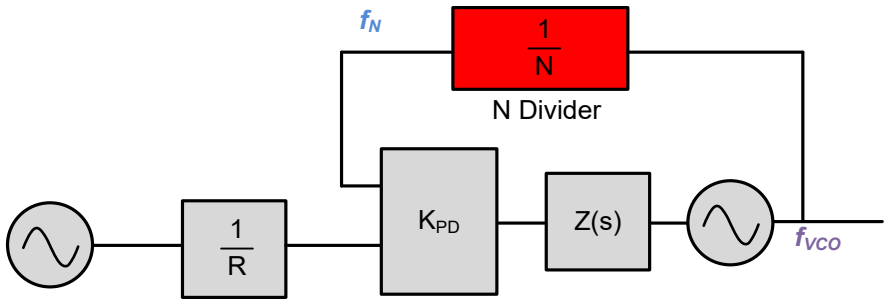


Figure 9.7 *The VCO Divider*

Conclusion

For PLLs that operate at higher frequencies, prescalers are necessary to overcome process limitations. The basic operation of the single, dual, and quadruple modulus prescaler has been presented. Prescalers combine with the A, B, and C counters in order to synthesize the desired ***N*** value. Because of this architecture, not all ***N*** values are possible there will be ***N*** values that are unachievable. These values that are unachievable are called illegal divide ratios. If one attempts to program a PLL to use an illegal divide ratio, then the usual result is that the PLL will lock to the wrong frequency. The advantage of using higher modulus prescalers is that a greater range of ***N*** values can be achieved, particularly the lower ***N*** values. Many PLLs allow the designer more than one choice of prescaler to use. In the case of an integer PLL, the prescaler used typically has no impact on the phase noise, phase detector spurs, or lock time, provided that the N divide value is the same.

Chapter 10 Fundamentals of Fractional Dividers



Introduction

The feedback (N) divider sets the VCO frequency. If this divider value is restricted to integer values only, then this implies that that the VCO frequency is restricted integer multiples of the phase detector frequency. This implies that the phase detector frequency must be lowered to accommodate the tuning resolution. When the tuning resolution is not large, this typically leads to a degradation in phase noise and spurs. A more popular approach is to create fractional N dividers to allow a finer tuning increment at the VCO without sacrificing performance. Fractional ***N*** PLLs differ from integer ***N*** PLLs in that some fractional N values are permitted. In general, a modulo ***Fden*** fractional N PLL allows ***N*** values in the form of:

$$N = N_{integer} + \frac{Fnum}{Fden} \qquad \textbf{(10.1)}$$

For most modern fractional PLLs, Fden is typically a very large number and is even programmable in many devices. This means that the phase detector frequency can be increased to the f_{OSC} frequency without sacrificing resolution. Because the ***N*** value can now be a fraction, the phase detector frequency can now be increased. This results in a lower N divider noise, which theoretically leads to lower phase noise and spurs. Figure 10.1 shows an example of a fractional N PLL generating 903 MHz with ***Fden=10***. This PLL has a channel spacing of 1 MHz, but the phase detector frequency is 10 MHz.

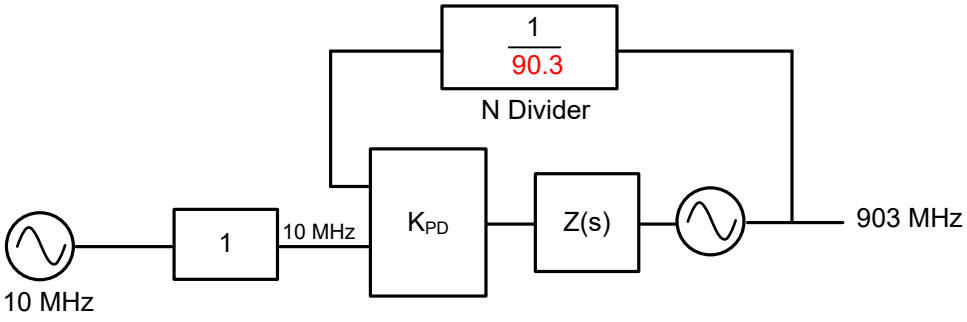


Figure 10.1 *Fractional N PLL Example*

Fractional N Architectures

The First Order Modulator

The simplest way to generate fractional N values is to toggle the N divider output between two values such that the average is the desired value. For instance, to achieve a fractional value of 100 1/3, the ***N*** counter can be made 100, then 100 again, then 101. The cycle repeats.

An accumulator is used to keep track of the instantaneous phase error, so that the proper ***N*** value can be used and the instantaneous phase error can be compensated for (Best 1995). Although the average ***N*** value is correct, the instantaneous value is not correct, and this causes high fractional spurs. In order to deal with the spur levels, a current can be injected into the loop filter to cancel these. The disadvantage of this current compensation technique is that it is difficult to get the correct timing and pulse width for this correction pulse, especially over temperature. Another approach is to introduce a phase delay at the phase detector. This approach yields more stable spurs over temperature, but sometimes adds phase noise. In some parts that use the phase delay compensation technique, it is possible to shut off the compensation circuitry in order to sacrifice reference spur level in order to improve the phase noise. For the Texas Instruments LMX2364, the fractional compensation circuitry can be disabled in order to gain about a 5 dB improvement in phase noise at the expense of 15 dB degradation in fractional spurs. The nature of added phase noise and spurs for fractional parts is very part specific.

Figure 10.2 shows how a fractional N PLL can be used to generate a 900.2 MHz signal from a 1 MHz phase detector frequency, using the phase delay technique. This corresponds to an ***N*** value of 900.2. Be aware that a 900.2 MHz signal has a period of 1.111 ps, and a 1 MHz signal has a period of 1000 ns. ε represents the difference in these periods.

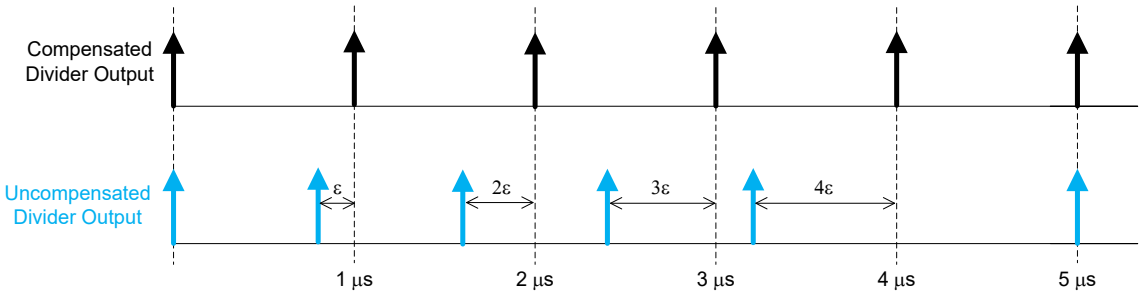


Figure 10.2 *Timing Diagram for Fractional Compensation*

Phase Detector Cycle	Accumulator (Cycles)	Overflow (Cycles)	Time for Rising Edge for Dividers (ns)		Phase Delay (ns)	Phase Delay (ns)
			Uncompensated	Compensated		
0	0.0	0	999.7778	0	0.222	0.222
1	0.2	0	1999.556	2000	0.444	0.444
2	0.4	0	2999.333	3000	0.667	0.667
3	0.5	0	3999.111	4000	0.889	0.889
4	0.8	0	4998.889	5000	1.111	1.111
5	0.0	1	999.7778	6000	0.222	0.222

Table 10.1 *Fractional **N** Phase Delay Compensation Example*

In Table 5.2, only the VCO cycles that produce a signal out of the ***N*** counter are accounted for. The phase delay is calculated as follows:

$$Phase\ Delay = \frac{1}{f_{VCO}} \cdot (Accumulator - Overflow) \qquad \textbf{(10.2)}$$

When the accumulator value exceeds one, then an overflow count of one is produced, the accumulator value is decreased by one, and the next VCO cycle is swallowed (Best 1995). Note that in Table 10.1, this whole procedure repeats every 5 phase comparator cycles, which corresponds to 4501 VCO cycles.

Higher Order Delta Sigma Modulators

Delta sigma PLLs have no analog compensation and reduce fractional spurs using digital techniques in order to try to bypass a lot of the issues with using traditional analog compensation. The delta sigma PLL reduces spurs by alternating the ***N*** counter between more than two values. The impact that this has on the frequency spectrum is that it pushes the fractional spurs to higher frequencies that can be filtered more by the loop filter.

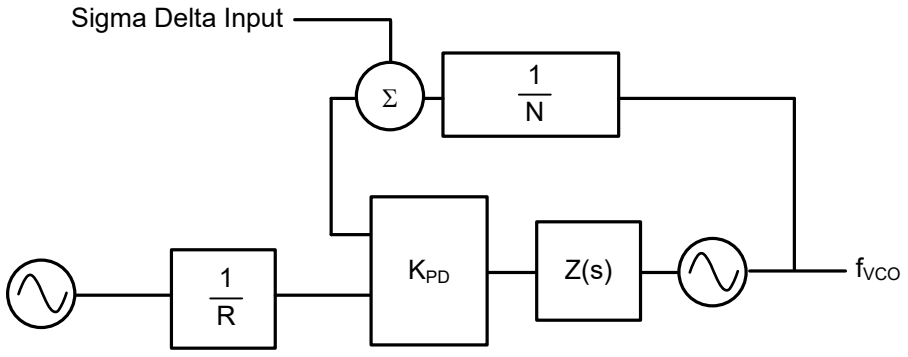


Figure 10.3 *Delta Sigma PLL Architecture*

Delta Sigma Order	Delta Sigma Input
1 (Traditional Fractional PLL without Compensation)	0, 1
2^{nd}	-2, -1, 0, 1
3^{rd}	-4, -3, -2, -1, 0, 1, 2, 3
4^{th}	-8, ... +7
k^{th}	-2^k ... 2^k-1

Table 10.2 *Delta Sigma Modulator Example*

For example, consider a PLL with an ***N*** value of 100.25 and a phase detector frequency of 1 MHz. A traditional fractional N PLL would achieve this by alternating the ***N*** counter values between 100 and 101. A 2^{nd} order delta sigma PLL would achieve this by alternating the ***N*** counter values between 98, 99, 100, and 101. A 3^{rd} order delta sigma PLL would achieve this by alternating the ***N*** counter values between 96, 97, 98, 99, 100, 101, 102, and 103. In all cases, the average ***N*** counter value would be 100.25. Note that in all cases, all of the N counter values must be legal divide ratios. The first fractional spur would be at 250 kHz, but the 3^{rd} order delta sigma PLL would theoretically have lower spurs than the 2^{nd} order delta sigma PLL. This would also have better spurs than the traditional fractional N PLL, although the traditional PLL could have analog compensation to impact the comparison.

Generation of the Delta Sigma Modulation Sequence

First Order Modulator

The sequence generated by the delta sigma modulator is dependent on the structure and the order of the modulator. For this case, the problem is modeled as having an ideal divider with some unwanted quantization noise. In this case, the quantization noise represents the instantaneous phase error of an uncompensated fractional divider. Figure 10.4 contains expressions involving the Z transform, which is the discrete equivalent of the Laplace transform. The expression in the forward loop representations a summation of the accumulator, and the z^{-1} in the feedback path represent a 1 clock cycle delay.

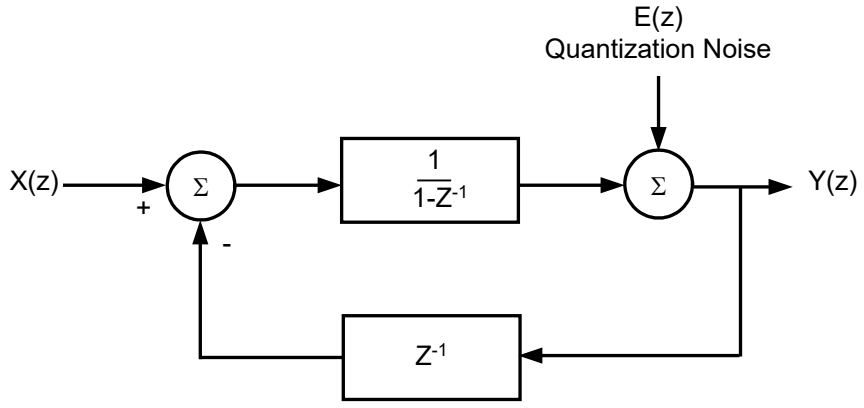


Figure 10.4 *The First Order Delta Sigma Modulator*

The transfer function for the above system is a follows:

$$Y(z) = X(z) + E(z) \cdot (1 - z^{-1}) \quad \textbf{(10.3)}$$

Note that the error term transfer function means to take the present value and subtract away what the value was in the previous clock cycle. In other words, this is a form of digital high pass filtering. The following table shows what the values of this first order modulator would be for an ***N*** value of 900.2.

x[n]	Accumulator	e[n]	y[n]	N Value
0.2	0.2	-0.2	0	900
0.2	0.4	-0.4	0	900
0.2	0.6	-0.6	0	900
0.2	0.8	-0.8	0	900
0.2	1.0	-0.0	1	901
0.2	0.2	-0.2	0	900
0.2	0.4	-0.4	0	900
0.2	0.6	-0.6	0	900
0.2	0.8	-0.8	0	900
0.2	1.0	-0.0	1	901

Table 10.3 *Values for a First Order Modulator for N=900.2*

Higher Order Modulators

In general, the first order modulator is considered a trivial case and delta sigma PLLs are usually meant to mean higher than first order. Although there are differences in the architectures, the general form of the transfer function for an $\boldsymbol{n^{th}}$ order delta sigma modulator is:

$$Y(z) = X(z) + E(z) \cdot (1 - z^{-1})^n \quad \textbf{(10.4)}$$

As a general rule of thumb, the lower offset spur/phase noise energy is pushed out to half of the phase detector frequency, where it should be easier to filter with the loop filter. The peaks are at odd multiples of the $\boldsymbol{f_{PD}/2}$ and the point where all the modulators are the same is theoretically $\boldsymbol{f_{PD}/6}$. This result is derived in a later chapter, but illustrated in Figure 10.5.

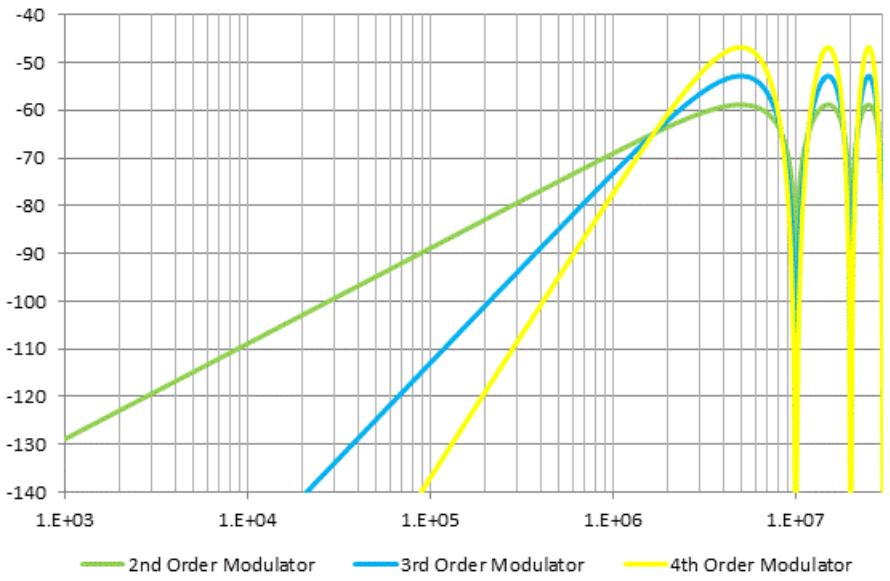


Figure 10.5 *Theoretical Delta Sigma Noise for a 10 MHz Phase Detector Frequency*

Example with Spurs

Consider the generation of a fraction of 1/10 with a first, second, third, and fourth order modulator. The theoretical sequence is shown in Table 10.4.

Modulator Order	Sequence
First	0,0,0,0,0,0,0,0,0,1, (repeats) …
Second	0,0,0,1,-1,1,-1,1,0,0,0,0,1,-1,1,-1,1,0,0,0, (repeats) …
Third	0,0,1,-1,0,1,0,0,-1,2,-2,2,-1,1,-1,0,1,1,-2,1, (repeats) …
Fourth	0,0,1,-1,1,-2,4,-4,2,1,-1,-1,3,-3,2,-1,2,-2,1,0,0,1,-2,2,-1,2,-3,3,-1,-1,1,2,-4,4,-2,1,-1,1,0,0, (repeats) ...

Table 10.4 *Delta Sigma Modulator Sequence for a Fraction of 1/10*

We see that the sequence repeats every 10 times for the first order modulator, every 20 times for the second and third order modulators, and every 40 times for the fourth order modulator.

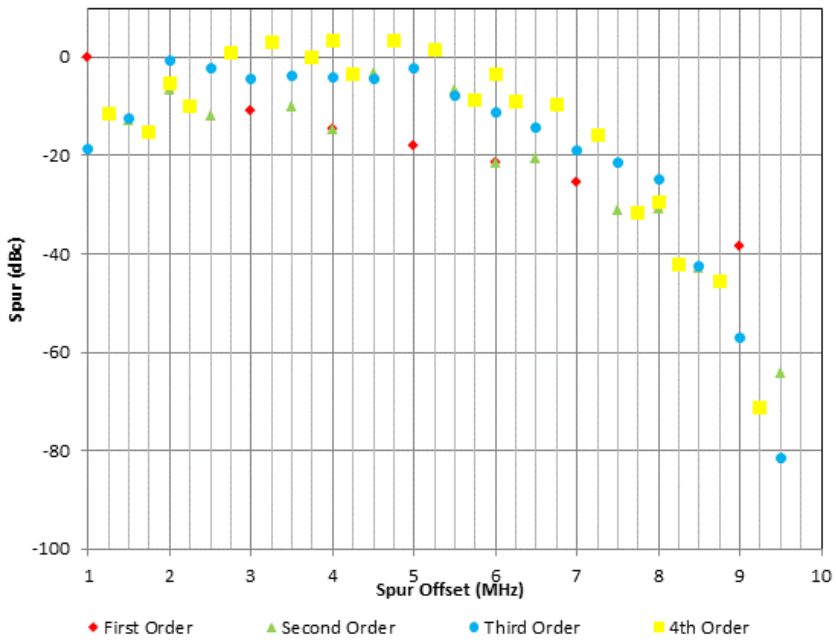


Figure 10.6 *Spur Comparison for Different Modulators for Fraction of 1/10*

Looking at 1 MHz, we see that the higher order modulators improve the spurious performance at 1 MHz and the lower offsets. Note that the fact that the spur at 1 MHz is completely eliminated for the 2nd order modulator is a lucky coincidence for this fraction, but the general pattern is that the higher order modulators push out the spurs to higher offsets, that can be easier filtered by the loop filter. This will be discussed in depth in a later chapter.

Concept of Dithering

In addition to using more than two ***N*** counter values, delta sigma PLLs may also use dithering to reduce the spur levels. Dithering is a technique of adding randomness to the sequence. For example, an ***N*** divide value of 99.5 can be achieved with the following sequence:

98, 99, 100, 101, ... (pattern repeats)

This sequence is periodic, which may lead to higher fractional spurs. Another sequence that could be used is:

99, 100, 98, 101, 98, 99, 100, 101, 98, 101, 99, 100 ... (pattern repeats)

Both sequences achieve an average ***N*** value of 99.5, but the second one has less periodicity, which theoretically implies that more of the lower frequency fractional spur energy is pushed to higher frequencies.

Dithering is typically implemented in the PLL chip, but it can also be manually implemented by the user. The general concept is to make the fraction to look like something that is much more complicated. For instance, consider the fraction of 17/1536. This fraction can also be expressed as 17000 / 1536000. If dithering is not used, the fractional accumulators start at zero, and modulator order is the same, then this larger equivalent fraction would yield the same sequence as the simplified fraction. However, there are ways to make this not the case. For instance, one could use a fraction of 17000 / 1536001. In this case the fraction does not reduce, but some of the sub-fractional spurs can be lower at the expense of increasing the close-in fractional noise. In this case, there might be some concern that the frequency is off, but there are now fractional PLLs with much larger denominators where this is much less of an issue. Another approach that does not introduce any frequency error is to put a non-zero starting value in one of the fractional accumulators. If this initial start value is relatively prime with the fractional denominator, then the sequence would be as it would be for the larger denominator.

The impact of dithering is different for every application. It tends to have a minimal impact on the main fractional spurs, but delta-sigma PLLs can have sub-fractional spurs that occur at a fraction of the channel spacing. Dithering tends to have the most impact on these spurs. In some cases, it can improve sub-fractional spur levels, while in other cases, it can make these spurs worse. One example where dithering can degrade spur performance is in the case where the fractional numerator is zero.

Conclusion

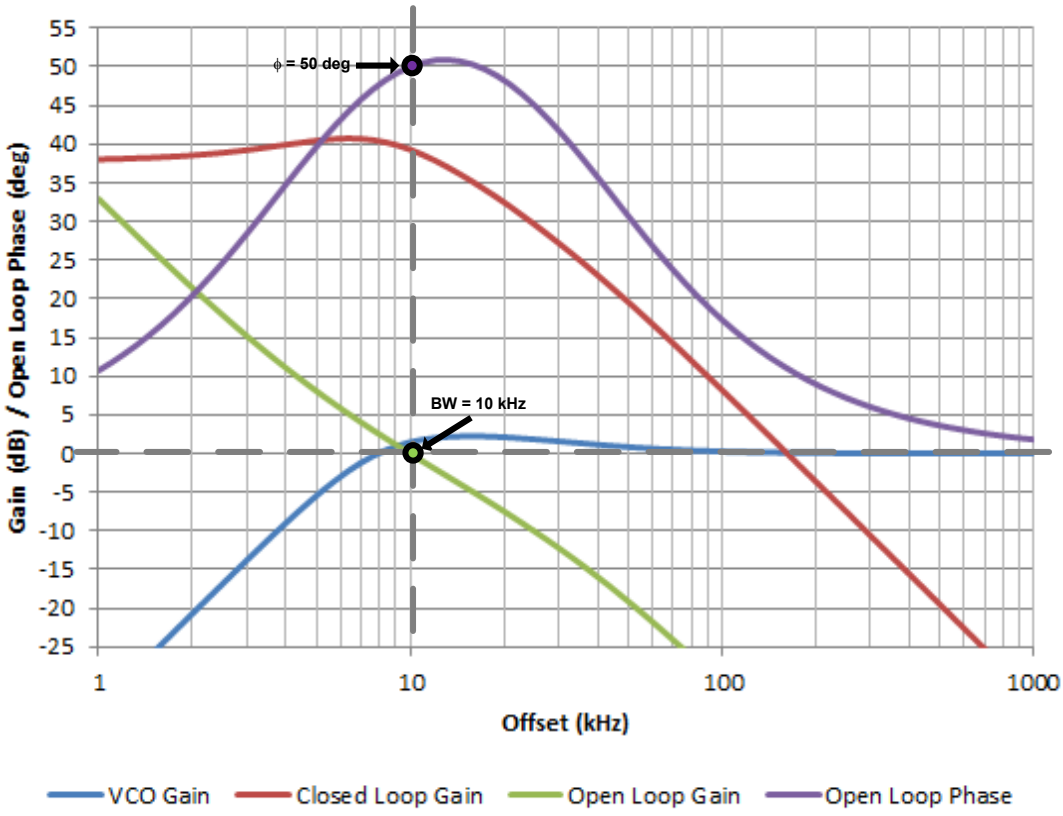
The delta sigma architecture can be used in fractional PLLs to reduce the fractional spurs. In practice, delta-sigma fractional PLLs do have much lower fractional spurs than traditional fractional PLLs with analog compensation. In addition to this, the digital compensation of delta-sigma PLLs tends to add less phase noise than the analog compensation used for the traditional first order fractional engine. Higher order modulators theoretically allow more reduction in fractional spurs, but do not always give the best results; this is application specific. One might think that because the compensation is based on digital techniques, the delta-sigma fractional spurs would be very predictable from pure mathematical models. However, calculated spur levels due to these factors tend to be very low, so other contributing factors can easily dominate the spur level. The modulator order and dithering are two things that can be chosen. In actuality, there can be many kinds of dithering, and many hidden test bits that can impact performance. In truth, delta-sigma PLLs can be very complex, although the part presented to the end user may seem much less complex because many test bits will be defined to default values after evaluation.

References

[1] Connexant Application Note Delta Sigma Fractional N Synthesizers Enable Low Cost, Low Power, Frequency Agile Software Radio

[2] Best, Roland E.,*Phase-Locked Loop Theory, Design, and Applications,* 3rd ed, McGraw-Hill, 1995

PLL Loop Theory



Chapter 11 Introduction to Loop Filter Coefficients

Introduction

This chapter introduces notation used to describe loop filter behavior throughout this book. The loop filter transfer function is defined as the change in voltage at the tuning port of the VCO divided by the current at the charge pump that caused it. In the case of a second order loop filter, it is simply the impedance. In general, the transfer function of the PLL loop filter can be described as follows:

$$Z(s) = \frac{1 + s \cdot T2}{s \cdot (A3 \cdot s^3 + A2 \cdot s^2 + A1 \cdot s + A0)} \quad \textbf{(11.1)}$$

$$T2 = R2 \cdot C2 \quad \textbf{(11.2)}$$

A0, ***A1***, ***A2***, and ***A3*** are the *loop filter coefficients* of the filter. In the case of a second order loop filter, ***A2*** and ***A3*** are zero. In the case of a third order loop filter, ***A3*** is zero. If the loop filter is passive, then ***A0*** is the sum of the capacitor values in the loop filter. In this book, there are two basic classes of loop filter that will be presented, passive and active. Although, there are multiple topologies presented for the active filter, only one is shown here, since this is the preferred approach.

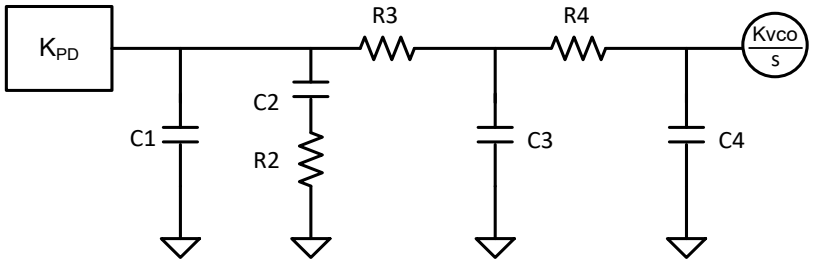


Figure 11.1 *Passive Loop Filter*

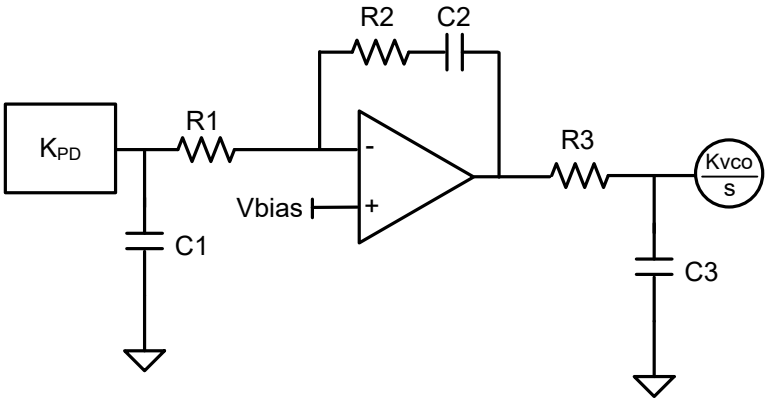


Figure 11.2 *Active Loop Filter (Active A)*

Calculation of Filter Coefficients

The equations for the 2nd and 3rd order filters are redundant as they can be easily derived from the 4th order equations by setting the unused component values to zero. In order to simplify calculations later on, the filter coefficients will be referred to many times, so it is important to be very familiar how to calculate them.

Filter Order	Symbol	Filter Coefficient Calculation
2	***A0***	*C1 + C2*
	A1	*C1·C2·R2*
	A2	*0*
	A3	*0*
3	***A0***	*C1 + C2 + C3*
	A1	*C2·R2·(C1+C3) + C3·R3·(C1+C2)*
	A2	*C1·C2·C3·R2·R3*
	A3	*0*
4	***A0***	*C1 + C2 + C3 + C4*
	A1	*C2·R2·(C1+C3+C4) + R3·(C1+C2)·(C3+C4)+C4·R4·(C1+C2+C3)*
	A2	*C1·C2·R2·R3·(C3+C4)* *+ C4·R4·(C2·C3·R3+C1·C3·R3+C1·C2·R2+C2·C3·R2)*
	A3	*C1·C2·C3·C4·R2·R3·R4*

Table 11.1 *Filter Coefficients for Passive Loop Filters*

Filter Order	Symbol	Filter Coefficient Calculation
2	***A0***	*C2*
	A1	*C1·C2·R1*
	A2	*0*
	A3	*0*
3	***A0***	*C2*
	A1	*C2·(C1·R1+C3·R3)*
	A2	*C1·C2·C3·R1·R3*
	A3	*0*
4	***A0***	*C2*
	A1	*C2·(C1·R1 + C3·R3 + C4·R4 + C4·R3)*
	A2	*C1·C2·R1·(C3·R3 + C4·R4 + C4·R3)+ C2·C3·C4·R3·R4*
	A3	*C1·C2·C3·C4·R1·R3·R4*

Table 11.2 *Filter Coefficients for an Active Type A Filter*

Filter Order	Symbol	Filter Coefficient Calculation
2	***A0***	*C1 + C2*
	A1	*C1·C2·R2*
	A2	*0*
	A3	*0*
3	***A0***	*C1 + C2*
	A1	*C1·C2·R2+(C1+C2)·C3·R3*
	A2	*C1·C2·C3·C4·R2·R3*
	A3	*0*
4	***A0***	*C1 + C2*
	A1	*C1·C2·R2+(C1+C2)·(C3·R3+C4·R4+C4·R3)*
	A2	*(C1+C2)·C3·C4·R3·R4* *C1·C2·R2·(C3·R3+C4·R4+C1·C2·R2+C4·R3)*
	A3	*C1·C2·C3·C4·R2·R3·R4*

Table 11.3 *Filter Coefficients for Active Type B and C Filters*

The calculation of the zero, ***T2***, is the same for active and passive filters and independent of loop filter order:

$$T2 = R2 \cdot C2 \qquad \textbf{(11.3)}$$

Relation between the Loop Filter Coefficients and Loop Filter Poles

In order to get a more intuitive feel of the loop filter transfer function, it is often popular to express this in terms of poles and zeroes. If one takes the reciprocal of the poles or zero values, then they get the corresponding frequency in radians. In the case of a fourth order passive loop filter, it is possible to get complex poles.

$$Z(s) = \frac{1 + s \cdot T2}{s \cdot A0 \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)} \qquad \textbf{(11.4)}$$

Once the loop filter time constants are known, it is easy to calculate the loop filter coefficients. The time constants and filter coefficients are related as follows:

$$\frac{A1}{A0} = T1 + T3 + T4 \qquad \textbf{(11.5)}$$

$$\frac{A2}{A0} = T1 \cdot T3 + T1 \cdot T4 + T3 \cdot T4 \quad \textbf{(11.6)}$$

$$\frac{A3}{A0} = T1 \cdot T3 \cdot T4 \quad \textbf{(11.7)}$$

Calculation of Poles for Passive Filters

Calculation of Pole for Second Order Filter

The calculation of the pole in the case of a second order filter, ***T1*** is trivial in this case.

$$T1 = \frac{A1}{A0} = \frac{C1 \cdot C2 \cdot R2}{C1 + C2} \quad \textbf{(11.8)}$$

Calculation of Poles for Third Order Filter

It is common to approximate the passive third order poles with the active third order poles. In order to solve exactly, it is necessary to solve a system of two equations and two unknowns.

$$T1 + T3 = \frac{A1}{A0} \quad \textbf{(11.9)}$$

$$T1 \cdot T3 = \frac{A2}{A0} \quad \textbf{(11.10)}$$

$$T1, T3 = \frac{A1 \pm \sqrt{A1^2 - 4 \cdot A0 \cdot A2}}{2 \cdot A0} \quad \textbf{(11.11)}$$

Calculation of Poles for Fourth Order Filter

For the passive fourth order loop filter, the time constants satisfy the following system of equations:

$$T1 + T3 + T4 = \frac{A1}{A0} \quad \textbf{(11.12)}$$

$$T1 \cdot T3 + T1 \cdot T4 + T3 \cdot T4 = \frac{A2}{A0} \quad \textbf{(11.13)}$$

$$T1 \cdot T3 \cdot T4 = \frac{A3}{A0} \quad \textbf{(11.14)}$$

If one uses the first equation to eliminate the variable ***T1***, the result is as follows:

$$y = x^2 - \frac{A1}{A0} \cdot x + \frac{A2}{A0} \tag{11.15}$$

$$y \cdot \left(x - \frac{A1}{A0}\right) = \frac{A3}{A0} \tag{11.16}$$

$$x = T3 + T4 \tag{11.17}$$

$$y = T3 \cdot T4 \tag{11.18}$$

Solving (11.15) into (11.16) yields the following cubic equation.

$$x^3 - 2 \cdot \frac{A1}{A0} \cdot x^2 + \left(\frac{A1^2}{A0^2} + \frac{A2}{A0}\right) \cdot x + \left(\frac{A3}{A0} - \frac{A1 \cdot A2}{A0^2}\right) = 0 \tag{11.19}$$

There will be at least one real root to this equation that can be found using numerical methods or the closed form solution presented in a later chapter. After ***x*** is chosen to be a real root of (11.19), then (11.15) can be used to find ***y***. From this the poles can be found.

$$T3, T4 = \frac{x \pm \sqrt{x^2 - 4 \cdot y}}{2} \tag{11.20}$$

$$T1 = \frac{A3}{A0 \cdot y} \tag{11.21}$$

One rather odd artifact of the fourth order passive filter is that it is possible for the poles ***T3*** and ***T4*** to be complex and yet still have a real-world working loop filter. Although this can happen, it is not very common.

Calculation of Poles for Active Filters

For active filters, it is perfectly legitimate to calculate the poles from the loop filter coefficients just as done in a passive filter. However, the addition of the op-amp adds isolation that simplifies the mathematics by separating out poles ***T3*** and ***T4***. The calculation of the pole T1 is the same for the second, third, and fourth order filters and only differs on the filter type.

For an Active Type A Filter:

$$T1 = \frac{A1}{A0} = C1 \cdot R1 \tag{11.22}$$

For passive type B and type C filters.

$$T1 = \frac{A1}{A0} = \frac{C1 \cdot C2 \cdot R2}{C1 + C2} \tag{11.23}$$

In the case of an active third order loop filter, the calculation of the pole, ***T3***, is rather simple:

$$T3 = C3 \cdot R3 \tag{11.24}$$

In the case of an active fourth order loop filter, ***T3*** and ***T4*** satisfy the following equations:

$$T3, T4 = \frac{x \pm y}{2} \tag{11.25}$$

$$x = C3 \cdot R3 + C4 \cdot R4 + C4 \cdot R3 \tag{11.26}$$

$$y = \sqrt{x^2 - 4 \cdot C3 \cdot C4 \cdot R3 \cdot R4} \tag{11.27}$$

Conclusion

It is common to discuss a loop filter in terms of poles and zeros. The zero, ***T2***, is always calculated the same way, but the calculations for the poles depends on the loop filter order and whether or not the loop filter is active or passive. However, filter coefficients are easier to calculate, simplify further calculations, and make it easier to generalize many results. The purpose of this chapter was to make the reader familiar with the filter coefficients, ***A0***, ***A1***, ***A2***, and ***A3***, since they will be used extensively throughout this book.

Chapter 12 Introduction to PLL Transfer Functions and Notation

Introduction

This chapter introduces fundamental transfer functions and notation for the PLL that will be used throughout this book. A clear understanding of these transfer functions is critical in order to understand spurs, phase noise, lock time, and PLL loop filter design.

PLL Basic Structure

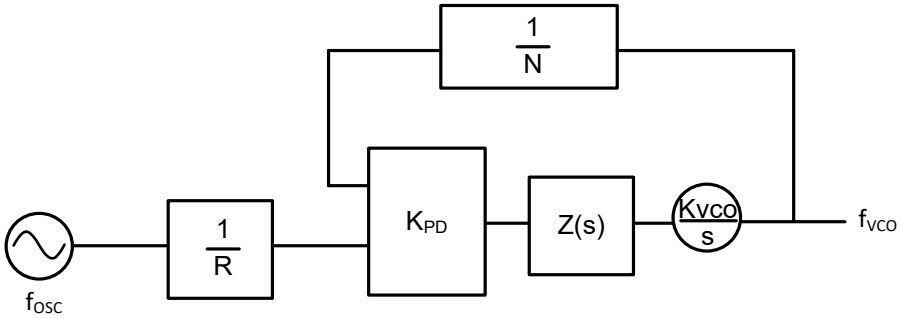


Figure 12.1 *Basic PLL Structure*

Introduction of Transfer Functions

The open loop transfer function is defined as the transfer function from the phase detector input to the output of the PLL. Note that the VCO gain is divided by a factor of ***s***. This is to convert output frequency of the VCO into a phase. Technically, this transfer function is the phase of the PLL output divided by the phase presented to the phase detector, assuming the other input, ϕ_R, is a constant zero phase. The open loop transfer function is shown below:

$$G(s) = \frac{K_{PD} \cdot K_{VCO} \cdot Z(s)}{s} \quad \textbf{(12.1)}$$

$$s = 2\pi \cdot j \cdot f \quad \textbf{(12.2)}$$

The ***N*** counter value is the output frequency divided by the phase detector frequency. Although the mathematics involved in defining ***H*** as the reciprocal of ***N*** may not be very impressive, it does make the equations look more consistent with notation used in classical control theory textbooks.

$$H = \frac{1}{N} \quad \textbf{(12.3)}$$

The closed loop transfer function takes into account the whole closed loop response including the phase frequency detector, feedback divider, and VCO.

$$CL(s) = \frac{G(s)}{1 + G(s) \cdot H} \tag{12.4}$$

This transfer function involves an output phase divided by an input phase. In other words, it is a phase transfer function. However, the frequency transfer function would be exactly the same. If one is considering an input frequency, this could be converted to a phase by dividing by a factor of ***s***, then it is converted to a phase. At the output, one would multiply by a factor of ***s*** to convert the output phase to a frequency. So both of these factors cancel out, which proves that the phase transfer functions and frequency transfer functions are the same. By considering the change in output frequency produced by introducing a test frequency at various points in the PLL loops, all of the transfer functions can be derived.

Source	Transfer Function
Input Reference	$\frac{1}{R} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
R Divider	$\frac{G(s)}{1 + G(s) \cdot H}$
N Divider	$\frac{G(s)}{1 + G(s) \cdot H}$
Phase Detector/Charge Pump	$\frac{1}{K_{PD}} \cdot \frac{G(s)}{1 + G(s) \cdot H}$
VCO	$\frac{G(s)}{1 + G(s) \cdot H}$

Table 12.1 *Transfer functions for various parts of the PLL*

Analysis of Transfer Functions

Note that the input reference transfer function has a factor of ***1/R*** and the phase detector transfer function has a factor of $\boldsymbol{1/K_{PD}}$ It is also true that the phase detector noise, ***N*** divider noise, ***R*** divider noise, and the input reference noise all contain a common factor in their transfer functions. All of these noise sources will be referred to as in-band noise sources and have the common factor given below.

$$\frac{G(s)}{1 + G(s) \cdot H} \tag{12.5}$$

The loop bandwidth is defined as the frequency that forward loop transfer function to have a gain of one.

$$\|G(j \cdot \omega c \cdot H)\| = 1 \tag{12.6}$$

ωc is used to express loop bandwidth in radians and ***BW*** is used to express this in Hz.

$$\omega c = 2\pi \cdot BW \tag{12.7}$$

Phase margin is defined as one hundred eighty degrees minus the phase of the forward loop transfer function at the loop bandwidth frequency.

$$\phi = 180 - \angle G(j \cdot \omega c) \cdot H \tag{12.8}$$

Phase margin relates to the stability. If the phase margin is low, there tends to be peaking in the closed loop transfer function and ringing in the PLL transient response. Higher phase margin gives a flatter closed loop transfer function, but excessively high phase margin can sacrifice switching speed of the PLL.

A third parameter of interest is the gamma optimization factor, which is defined as follows:

$$\gamma = \frac{T2}{\omega c^2 \cdot A0} \tag{12.9}$$

The gamma optimization relates maximizing the phase margin at the loop bandwidth frequency. For a gamma of one and a second order filter, the phase margin is maximized at the loop bandwidth frequency. If gamma is less than one, this maximum point is higher than the loop bandwidth frequency and if gamma is greater than one, this maximum point is lower than the loop bandwidth frequency.

Using these definitions, and equations (9.1) and (9.2), and the fact that ***G(s)*** is monotonically decreasing in ***s*** allows the following approximation.

$$\frac{G(s)}{1 + G(s) \cdot H} \approx \begin{cases} N & for\ f \ll BW \\ G(s) & for\ f \gg BW \end{cases} \tag{12.10}$$

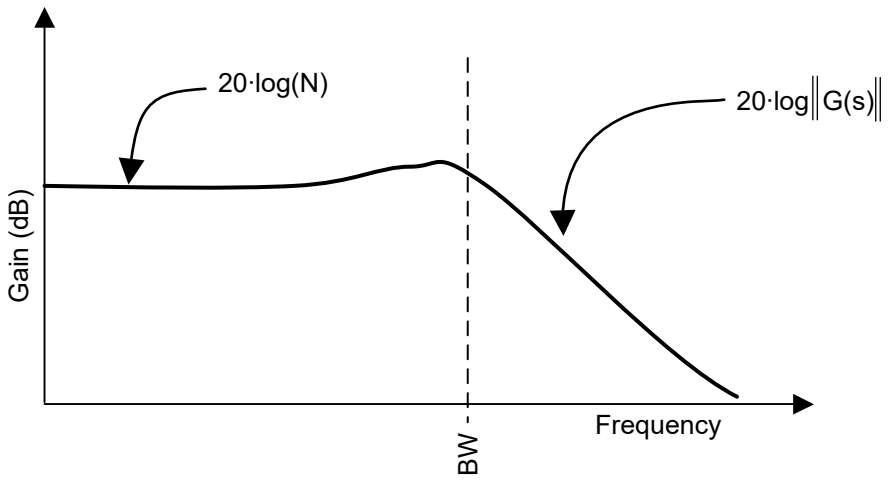


Figure 12.2 *Transfer Function that Multiplies all Sources except the VCO*

The VCO has a different transfer function:

$$\left\| \frac{1}{1 + G(s) \cdot H} \right\| \tag{12.11}$$

Note that this transfer function can be approximated by:

$$\left\| \frac{1}{1 + G(s) \cdot H} \right\| = \begin{cases} \dfrac{N}{\|G(s)\|} & for\ f \ll BW \\ 1 & for\ f \gg BW \end{cases} \tag{12.12}$$

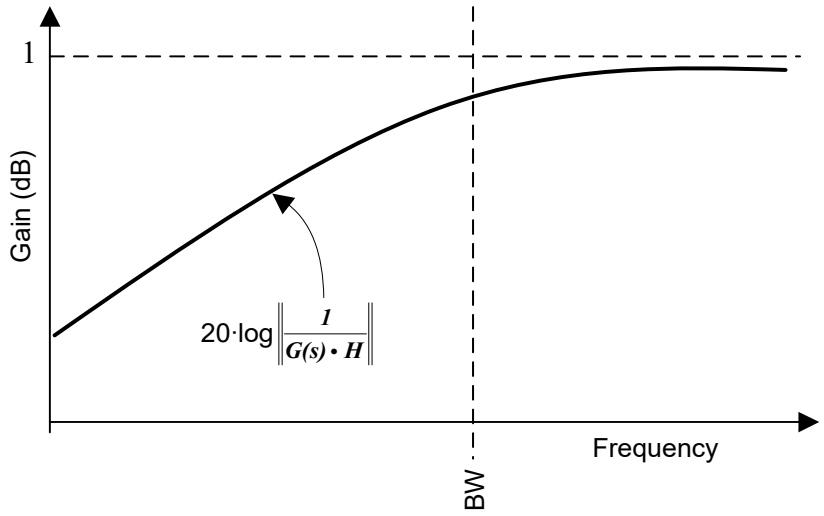


Figure 12.3 *Transfer Function for the VCO*

Scaling Properties of PLL Loop Filters

Loop Gain Constant

In order to discover these properties, it is easier to expand the expression for the closed loop transfer function and introduce a new variable, ***K***.

$$K = \frac{K_{PD} \cdot K_{VCO}}{N} \tag{12.13}$$

The loop gain constant, ***K***, is dependent on the charge pump gain, VCO gain, and ***N*** counter value. From the above equation, one can see that these three parameters can be changed without impacting the transfer functions, provided that the loop gain constant is held constant. For instance, if the charge pump gain and ***N*** divider value are doubled, yet the VCO gain is held constant, the closed loop transfer function remains unchanged. Using this new definition for loop gain constant, the closed loop transfer function can be simplified.

$$\frac{G(s)}{1 + {G(s)}/{N}} = \frac{K \cdot N \cdot (1 + s \cdot T2)}{s^5 \cdot A3 + s^4 \cdot A2 + s^3 \cdot A1 + s^2 \cdot A0 + s \cdot K \cdot T2 + K} \tag{12.14}$$

Scaling Property of Components

Even though loop filter design has not been discussed yet, it is not premature to show how to scale loop filter components. The first step involves understanding how the loop filter coefficients change with the loop filter values. If one was to change all capacitors by a factor of ***x*** and all resistors by a factor of ***y***, then the impact on the loop filter coefficients can be found.

Loop Filter Coefficient	Proportionality ($\propto$) to x and y
A0	$\propto x$
A1	$\propto x \cdot (x \cdot y)$
A2	$\propto x \cdot (x \cdot y)^2$
A3	$\propto x \cdot (x \cdot y)^3$

Table 12.2 *Relationship of Loop Filter Coefficients to Component Scaling Factors*

Equation	Implication
$x \propto \frac{K}{BW^2}$	The loop filter capacitors should be chosen proportional to the loop gain divided by the loop bandwidth squared.
$y \propto \frac{BW}{K}$	The loop filter resistors should be chosen proportional to the loop bandwidth over the loop gain.

Table 12.3 *The Rule for Scaling Components*

Table 12.3 shows the fundamental rule for scaling components. There are several ways this can be applied. Consider the case where the loop gain constant, ***K***, is changed. An example of this is if one were to inherit a PLL design done by someone else who has since left the company. Suppose in this case, the original design was done with a PLL with a charge pump gain of 1 mA, and now the PLL is being replaced with a newer one with a charge pump gain of 4 mA. Because the loop gain changes by a factor of 4, all the capacitors should be made four times larger and all the resistors should be made to one-fourth of their original value. Consider a second case where one designed a loop filter for a loop bandwidth of 10 kHz, but now wants to increase the loop bandwidth to 20 kHz. In this case, the loop bandwidth is changing by a factor of two, so the capacitors should be one-fourth of their original value, and the resistors should be twice their original value.

Scaling Rule of Thumb for the Loop Bandwidth

This rule deals with the case when the gain constant is changed, but the loop filter components are not changed and the impact on loop bandwidth is desired. Even though the loop filter is not optimized in this case, it still makes sense to understand how it behaves. An example of this could be where the loop filter is designed for a particular VCO gain, but the actual VCO has a gain that varies considerably.

To derive this rule, recall that the loop bandwidth is the frequency for which the magnitude of the open loop transfer function is unity. It is easier to see this relationship if the open loop transfer function is expressed in the following form.

$$G(s) = \frac{K}{s} \cdot \frac{1 + s \cdot T2}{s \cdot A0 \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)} \qquad \textbf{(12.15)}$$

Although a coarse approximation, if one neglects all the poles and zeros, one can derive the fundamental result.

$$BW \propto \sqrt{K} \qquad \textbf{(12.16)}$$

This rule assumes that the loop filter is not changed. For example, suppose that it is known that a PLL has a loop bandwidth of 10 kHz when the VCO gain is 20 MHz/V. Suppose the VCO gain is actually 40 MHz/V. In this case, the loop bandwidth should be about 1.4 times larger. This rule of thumb is not exact and the loop filter may not be perfectly optimized, but it is useful in many situations.

Applying the Scaling Factor for Re-Use of a Loop Filter

When the loop bandwidth, charge pump gain, N divider value, or VCO frequency of a loop filter is changed significantly, then the loop dynamics are changed as well. Although it is possible to re-design the loop filter, often times it is desirable to use the same loop filter. In other situations, this might not be practical, such is the case for a wideband tuning application where the N divider and VCO gain varies. In this situation, a good strategy is to keep the loop gain constant from changing too much.

$$\frac{K_{PD_1} \cdot K_{VCO_1}}{N_1} \sim \frac{K_{PD_2} \cdot K_{VCO_2}}{N_2} \qquad \textbf{(12.17)}$$

For most modern PLLs, the easiest way to do this is to adjust the charge pump gain. In other words, if the VCO gain was to double the charge pump gain could be made half to compensate.

Conclusion

This chapter has discussed the fundamental concept of PLL transfer functions. The reader should familiarize themselves with the notation in this chapter, since it will be used throughout the book. Although the PLL transfer functions are derived as phase transfer functions, the frequency transfer functions are identical.

Chapter 13 PLL Modulation, Demodulation, and Clock Cleaning

Introduction

In many applications, one may be interested in how a PLL reacts to signals at the input reference, N divider, or VCO tuning voltage. In the case of PLL modulation, this signal is intentionally created and applied at some point in the loop so that the carrier is modulated. In demodulation applications, the signal is applied at some point in the loop and information from the signal is obtained at some other point in the PLL loop. In the case of clock cleaning, the PLL is used to suppress unwanted noise on the input reference signal. This chapter discusses general principles and techniques for PLL modulation and demodulation.

General Modulation Principles

Relationship between Phase and Frequency

Modulation can be viewed a phase or frequency; it can be shown that both of these are related. Let the voltage output of the VCO be defined as follows:

$$V(t) = A \cdot cos\big(\omega_0 \cdot t + \phi(t)\big) \tag{13.1}$$

In this equation, A is the amplitude of the signal, ω_0 is the unmodulated carrier frequency, $\phi(t)$ is the phase modulation, and $\omega_0 + \phi(t)$ is the instantaneous phase.

The instantaneous frequency of the signal is the time derivative of the instantaneous phase.

$$\frac{d}{dt}[\omega_0 \cdot t + \phi(t)] = \omega_0 + \frac{d\phi}{dt} \tag{13.2}$$

The frequency modulation can be thought of as the difference of the actual frequency and the unmodulated frequency of the signal.

$$f(t) = \frac{d\phi}{dt} \tag{13.3}$$

It follows from this that:

$$\phi(t) = \int_0^t f(x) \cdot dx \tag{13.4}$$

Since frequency is the derivative of phase, it follows that frequency and phase modulation are really two different ways of looking at the same thing. It is therefore sufficient to focus the study on phase modulation. The only difference is that in traditional frequency modulation, one would not expect the phase to change abruptly because this would not be possible if the modulation function for the frequency was continuous. To account for this subtle point, frequency modulation and phase modulation will be generalized as angle modulation. It therefore follows that (13.1) can be re-stated as:

$$V(t) = A \cdot cos[\omega_0 \cdot t + \phi(t)] = A \cdot cos\left[\omega_0 \cdot t + \int_0^t f(x) \cdot dx\right] \quad \textbf{(13.5)}$$

When modulation is applied to a PLL in various forms, sometimes an integral or derivative finds its way worked in to the formula. This is why it is useful to understand this relationship between frequency and phase.

Sinusoidal Tone Modulation

The most basic form of modulation is a sinusoidal tone. Define $\boldsymbol{f_{MOD}}$ as the modulation frequency in Hz. For this type of modulation:

$$\phi(t) = \beta \cdot sin[2\pi \cdot f_{MOD} \cdot t] \quad \textbf{(13.6)}$$

It is easier to think of this in terms of frequency modulation and to define the deviation from center frequency in Hz as $\boldsymbol{f_{DEV}}$. Now take the derivative of (13.6) to find frequency deviation from center frequency in Hz.

$$2\pi \cdot f_{DEV} \cdot cos(2\pi \cdot f_{MOD} \cdot t) = \frac{d\phi}{dt} = \beta \cdot 2\pi \cdot f_{MOD} \cdot cos(2\pi \cdot f_{MOD} \cdot t) \quad \textbf{(13.7)}$$

By equating the two expressions in (13.7), the equation for the modulation index can be expressed in terms of the frequency deviation and the modulation frequency

$$\beta = \frac{f_{DEV}}{f_{MOD}} \quad \textbf{(13.8)}$$

The modulation index, $\boldsymbol{\beta}$, is of particular interest in FM modulation, since it determines the sideband levels. Figure 13.1 gives a visual representation of how sinusoidal tone modulation would look as a function of frequency vs. time and voltage vs. time.

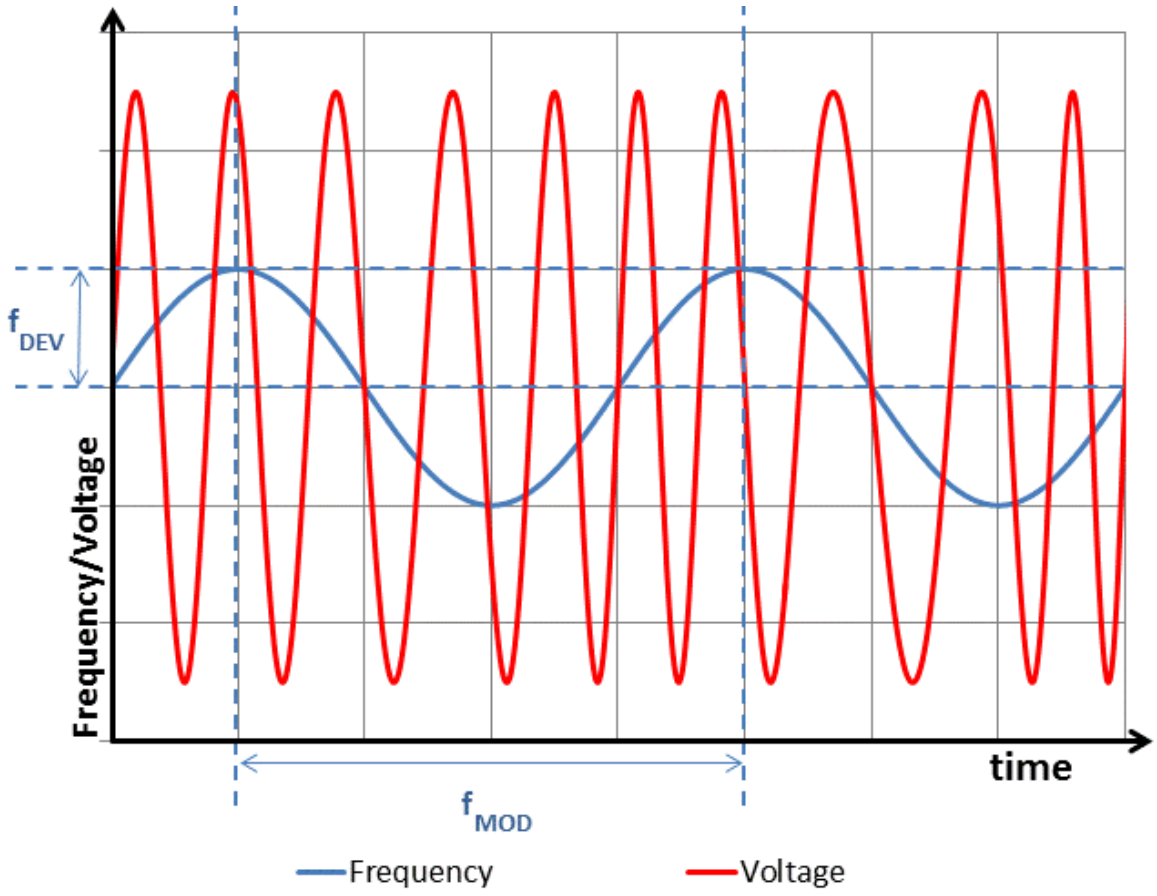


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Figure 13.1 *Sinusoidal FM Modulation*

This concept of modulation index proves to be a fundamental cornerstone in understanding FM modulation and is useful to remember. Continuing on to calculate the spectrum from the modulation index, the next step is to write down the complex Fourier series for $e^{j\cdot\beta\cdot sin(\omega_m\cdot t)}$ (Tranter 1985).

$$e^{j\cdot\beta\cdot sin(\omega_m\cdot t)} = \sum_{n=-\infty}^{\infty} c_n \cdot e^{j\cdot n\cdot\omega_m\cdot t} \qquad \textbf{(13.9)}$$

The calculation of the c_n coefficient is as follows

$$c_n = \frac{\omega_n}{2\pi}\cdot\int_{-\pi/\omega_m}^{\pi/\omega_m} e^{j\cdot\beta\cdot sin(\omega_m\cdot t)}\cdot e^{j\cdot n\cdot\omega_m\cdot t}\cdot dt \qquad \textbf{(13.10)}$$

The next is to introduce the substitution $x \rightarrow \omega_m \cdot t$ which also means that we have to substitute $\rightarrow \omega_m \cdot dt$. Performing this substitution yields the following.

$$c_n = \frac{1}{2\pi} \cdot \int_{-\pi}^{\pi} e^{j \cdot [n \cdot x - \beta \cdot sin(x)]} \cdot dx = J_n(\beta) \tag{13.11}$$

The above expression is the integrated form of the Bessel function of the first kind of order *n* (Tranter 1985). Therefore, (13.9) can be written as follows.

$$e^{j \cdot \beta \cdot sin(\omega_m \cdot t)} = \sum_{n=-\infty}^{\infty} J_n(\beta) \cdot e^{j \cdot n \cdot \omega_m \cdot t} \tag{13.12}$$

This allows power spectral density to be simplified as follows (Tranter 1985):

$$\begin{aligned} V(t) &= A \cdot cos[\omega_0 \cdot t + \beta \cdot sin(\omega_m \cdot t)] \\ & A \cdot Real\left\{e^{j \cdot \omega_0 \cdot t} \cdot \sum_{n=-\infty}^{\infty} J_n(\beta) \cdot e^{j \cdot n \cdot \omega_m \cdot t}\right\} \\ &= A \cdot \sum_{n=-\infty}^{\infty} J_n(\beta) \cdot cos(\omega_0 \cdot t + n \cdot \omega_n \cdot t) \end{aligned} \tag{13.13}$$

From this expression, the sideband levels can be found by each of the coefficients.

$$Carrier: \quad J_0(\beta) \approx 1 \tag{13.14}$$

$$First\ Sideband: \quad J_1(\beta) \approx \frac{\beta}{2} \tag{13.15}$$

$$Second\ Sideband: \quad J_2(\beta) \approx \frac{\beta^2}{8} \tag{13.16}$$

$$n^{th}\ Sideband: \quad J_n(\beta) \tag{13.17}$$

Modulation Techniques

Modulation of the Input Reference

When the input reference is modulated, all modulation within the loop bandwidth is passed. The general rule of thumb is that the loop bandwidth should be twice of the information bandwidth of the modulating signal. Note the frequency deviation of the modulation is not changed at the output of the VCO. This is for the same reason why the spurs of a signal after a divider have the same offset. The modulation can be either phase or frequency, and the output modulation is of the same type. This type of modulation is typically easy to implement. The transfer function for phase or frequency modulation is as follows:

$$T_{Input}(s) = \frac{1}{R} \cdot \frac{G(s)}{1 + G(s)/N} \quad \textbf{(13.18)}$$

Provided that the modulation frequency is less than about two times loop bandwidth, this can be approximated by:

$$T_{Input}(s) \approx \frac{N}{R} \quad \textbf{(13.19)}$$

For example, if the modulating signal was a sinusoidal tone, then the output at the VCO would be a similar sinusoidal tone with the same modulation frequency, $\boldsymbol{\omega_m}$, and with the frequency deviation, $\boldsymbol{\Delta F}$, multiplied by $\boldsymbol{N/R}$.

Modulation of the Tuning Voltage or VCO

The VCO can be thought of as a voltage to frequency converter. It therefore follows that FM modulation can be achieved by modulating this tuning voltage. This can be done by adding a summing op-amp before the VCO or using a separate VCO modulation pin, if it has one. K_{MOD} has units of MHz/V and represents the modulation constant, which is the amount the VCO frequency changes per a given voltage change on the modulation port. Using this method, the transfer function for voltage to frequency is as follows:

$$T_{VCO}(s) = \frac{K_{MOD}}{1 + G(s)/N} \quad \textbf{(13.20)}$$

For this situation, modulation below the loop bandwidth frequency is attenuated, so the loop bandwidth of the PLL is typically chosen narrow relative to the modulation frequency. In this case, the transfer function can be approximated as follows:

$$T_{VCO}(s) \approx K_{MOD} \quad \textbf{(13.21)}$$

VCO Open Loop Modulation

This is a special type of VCO modulation where the charge pump is disabled during the time of modulation. The reason for doing this is to prevent the PLL from fighting the modulation. A drawback of this method is that the loop filter voltage will drift when the charge pump is off, so the time that the VCO can be modulated is limited by how fast the VCO drifts off frequency. The charge pump leakage of the PLL is typically the dominant source of leakage, and the sum of the capacitors in the loop filter is a rough approximation for the effective capacitance that this leakage acts on for purposes of frequency drift calculations. Because of this fact, designs with narrower loop bandwidth, higher charge pump currents, or higher comparison frequencies (as in Fractional N PLLs) tend to be more resistant to leakage due to the larger capacitor sizes. There is typically a phase disturbance when the charge pump is engaged or disengaged, which needs to be taken into consideration. The transfer function for open loop modulation is as follows:

$$T_{VCO}(s) \approx K_{MOD} \qquad \textbf{(13.22)}$$

Dual Port Modulation

With the exception of open loop modulation, the PLL fights the modulation inside or outside the loop bandwidth. In dual port modulation, both the input reference and the VCO are modulated at the same time. In this way, the modulations added together give the desired modulation without any distortion from the PLL. If ***m(s)*** represents the desired modulation, then this modulation needs to be pre-distorted. The modulation frequency (or phase) applied to the input reference needs to be multiplied by a factor of ***R/N*** and the modulation presented to the VCO needs to be divided by a factor of $\boldsymbol{K_{MOD}}$. Applying this result to (13.19) and (13.20) shows that the modulation theoretically has an all pass response.

$$\left[\frac{R}{N}\cdot m(s)\right]\cdot\left[\frac{1}{R}\cdot\frac{G(s)}{1+\frac{G(s)}{N}}\right]+\left[\frac{m(s)}{K_{MOD}}\right]\cdot\left[\frac{K_{MOD}}{1+\frac{G(s)}{N}}\right] = \text{m(s)} \qquad \textbf{(13.23)}$$

There is theoretically no distortion. However, due to delays in the phase detector, there may be some. If a voltage phase detector is being used, instead of a charge pump, the modulation can be injected after this charge pump before and after the loop filter.

Modulation of the N Counter

For this modulation technique, the N counter value is modulated with information in order to produce a waveform. The simplest example of this modulation is binary FSK that toggles the output between two frequencies, $\boldsymbol{f_1}$ and $\boldsymbol{f_2}$, which represent the two states of 0 and 1. If these frequencies are farther apart, it is easier to discern the difference between them, but separating these frequencies more consumes more spectrum. The rate at which one toggles between the two frequencies is the transmission rate. If more frequencies are used, as is the case in 4-FSK or 8-PSK, then the spectrum required can be reduced.

A fractional PLL can be used to further enhance this method. For instance, it can be used to approximate a Gaussian shaping for the transmitted signal in order to reduce intersymbol interference and reduce the bandwidth of the signal. If there is sufficient resolution, this waveform can be digitally programmed in the PLL. One consideration with this technique is that it is limited by the write speed to the PLL and is therefore best for lower data rate applications.

For this application, data inside the loop bandwidth of the system is passed, and that outside of the loop bandwidth is attenuated. As a rule of thumb, the loop bandwidth should be about twice of the bandwidth of the modulated signal to avoid distorting the signal. The transfer function is shown below:

$$T_N(s) = \frac{G(s)}{1 + G(s)/N} \tag{13.24}$$

Provided that the loop bandwidth is wide relative to the modulation frequency, the transfer function can be approximated as follows:

$$T_N(s) \approx N \tag{13.25}$$

Another application where the N divider can be modulated is to create a ramp and chirp waveforms that are often used in radar applications. In this sort of application, the fractional value in the N divider is dynamically adjusted. The loop bandwidth needs to be wide enough to follow the slew rate of the desired waveform.

Pre-Emphasis/Pre-Distortion

In many types of PLL modulation, the PLL fights the modulation and the loop filter dynamics. The first way to compensate for this is to simply make the loop bandwidth sufficiently wide such that this is not an issue. However, the loop bandwidth may be limited by spur requirements, phase noise requirements, or the phase detector frequency. Aside from dual-port modulation, another technique that can be used to overcome this is pre-emphasis, also called pre-distortion. In this technique, the signal is intentionally distorted before it is sent to the PLL in such a way that the distortion due to the loop bandwidth of the PLL cancels out this distortion, and the recovered signal is the intended one with no distortion. For example, if the input reference is modulated, the Laplace transform of the pre-distortion function would be:

$$P(s) = R \cdot \frac{1 + G(s)/N}{G(s)} \tag{13.26}$$

Another trivial type of pre-emphasis was already described in dual-port modulation, where the frequency deviation, $\boldsymbol{\Delta f}$, presented to the R counter was multiplied by a factor of $\boldsymbol{R}$.

Demodulation Techniques

All the demodulation techniques discussed in this chapter involve using the carrier with modulation as an input reference to the PLL. Whether phase demodulation or frequency demodulation is desired determines where the demodulated signal is monitored.

Demodulation at the Tuning Voltage of the VCO

If the modulation to be recovered is frequency modulation, then the voltage presented to the VCO has the following transfer function.

$$T(s) = \frac{1}{R} \cdot \frac{G(s)}{1 + G(s)/N} \cdot \frac{s}{K_{VCO}} \quad \textbf{(13.27)}$$

If the loop bandwidth is made wide, then this can be approximated as:

$$T(s) \approx \frac{N}{R} \cdot \frac{s}{K_{VCO}} \quad \textbf{(13.28)}$$

Note that all of the factors are constant, except for the factor of ***s***, which indicates differentiation. So whatever modulation is input into the input reference, the tuning voltage will have the derivative of the input signal. For this reason, the modulation signal at the input is first integrated (and possibly multiplied by a scaling factor), so that when it is differentiated, the intended signal is obtained. Since frequency is the derivative of phase, this is why this modulation is regarded as frequency modulation.

Demodulation at the Output of the Phase Detector

Although the tuning voltage is easily accessible, it may require the extra step of the modulating signal be first integrated before it is sent. If the modulation is retrieved at the output of the phase detector or the phase detector is a voltage phase detector, then this signal is easy to retrieve. However, charge pump PLLs have mostly replaced voltage phase detectors, which complicates things, since this current output needs to be converted to a voltage. One method is to put a small series sense resistor that develops a voltage that is proportional to the charge pump current. If it is acceptable to lose polarity information, another method is to use the an analog lock detect mode, as this puts out negative pulses corresponding to when the charge pump turns on and is therefore proportional to the phase error. For this method of demodulation, the transfer function is as follows:

$$T(s) = \frac{1}{R} \cdot \frac{K_D}{1 + G(s)/N} \quad \textbf{(13.29)}$$

The loop bandwidth is typically made narrow, and the transfer function can be approximated as:

$$T(s) = \frac{K_D}{R} \qquad \textbf{(13.30)}$$

$\boldsymbol{K_D}$ is the voltage gain of the phase detector, neglecting the impact of the charge pump. In the case that a charge pump PLL is being used and this is being extracted from the lock detect output or from a sense resistor, this would be the voltage produced divided by 2π.

AM Demodulation

AM modulation is typically not possible with a PLL alone. However, there is an architecture known as the Costas Loop which can demodulate an AM signal. In general, AM can be demodulated in other ways, but the Costas Loop is good when the carrier itself is weak. This involves squaring the signal and using some dividers and is beyond the scope of this book.

Conclusion

Aside from providing a stable signal source, the PLL can also be used to modulate or demodulate data. As discussed above, there are many approaches to this, each with their advantages and disadvantages. Just because the PLL can be modulated with information does not mean that this is the only way to modulate or demodulate data. It is very common in modern digital communications to not modulate the PLL and simply use it as a signal source.

References

[1] Tranter, W.H. and R.E. Ziemer *Principles of Communications Systems, Modulation, and Noise*, 2nd Ed, Houghton Mifflin Company, 1985

Chapter 14 Stability of PLL Loop Filters

Introduction

Although there are many potential causes for a PLL to be unlocked, stability typically refers to issues with the causes that are evident from the closed loop analysis of the PLL. The most common symptom of instability is for the VCO have very strong FM modulation that smears across the entire frequency range of the VCO. In the frequency domain, it looks like the frequency is smearing over the spectrum.

Some practical situations that can lead to instability could be a large change in the loop gain (K_{VCO}, K_{PD}, or N) from the intended design value, an unaccounted for VCO input capacitance, or accidental misplacements of components (such as swapping of loop filter capacitors C1 and C2).

The first kind of stability discussed will be called *discrete sampling stability*, which is a requirement related to the discrete sampling action of the phase detector. The second kind of stability will be called *transfer function stability*, which requires that the poles of the closed loop transfer function are in the right hand plane. For this kind of stability, Routh's Stability Criteria, is the most complete test for this, but there also exist the criteria of phase margin and gain margin that can be used as indicators as well.

Discrete Sampling Stability

The PLL charge pump is often modeled as having a continuous analog current that is proportional to the phase error at the phase detector. However, the charge pump output is actually a pulse width modulated signal that has an average current proportional to the error at the phase detector. The true criterion for the second order filter is discussed in reference [1] in depth, although the derivations are rather involved and there exists an easy to use rule of thumb. When the loop bandwidth is less than about one-tenth of the phase detector frequency, approximating the charge pump output as an analog current is pretty accurate. Typically when the loop bandwidth is between one-tenth and one-fifth of the phase detector frequency, the PLL will lock with some distortions in behavior. These distortions can include an increase the in lock time and a "cusping" effect on the phase noise near the phase detector offset frequency. When the loop bandwidth approaches 28% of the phase detector frequency (which varies slightly with phase margin, gamma, and filter order), the loop filter will go unstable due to the discrete sampling action of the phase detector.

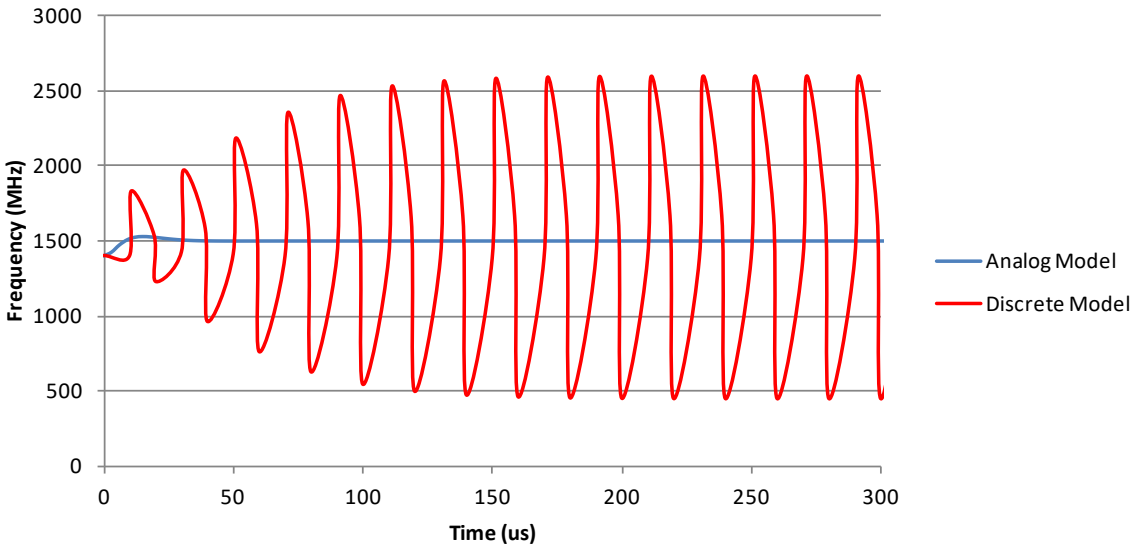


Figure 14.1 *Example of Discrete Sampling Instability*

Figure 14.1 shows the transient response of a PLL that is unstable due to the discrete sampling effects of the phase detector. The analog model approximates the output as a continuous current and misses the instability, but the discrete model shows it.

Transfer Function Stability

The transfer function will be stable if the poles of the closed loop transfer function have all negative real parts. The poles show up as exponents in the time domain response and a negative real part of each pole means that the time domain response will converge to a final value over time. There are methods, such as *Routh's Stability Criteria*, that can be used to determine if the poles all have all negative real parts without explicitly calculating them.

Phase Margin

Phase margin is commonly used that gives useful insight both the transient behavior, the peaking in the loop filter response, and stability. However, it is not a perfect metric for stability. Loop filters that have unstable transfer functions tend to have lower phase margin less than 20 degrees and filters with lower phase margin also tend to have more peaking in the closed loop response. For this reason, low phase margin or large peaking in the closed loop response is often related to a filter being unstable, or close to that point. This being said, it is possible to have very low phase margin (even 5 degrees) and have a loop filter that is perfectly stable. So therefore, there is value introducing other metrics of stability that are more reliable and also that give a better indication of how far a filter is from the point of becoming instability.

Gain Margin

Gain margin is defined as the gain of the open loop transfer function at the frequency where the open loop phase is equal to 180 degrees. Another way to view this is if one graphs 180 degrees minus the open loop phase and calls this phase margin, then the gain margin would be the frequency where the phase margin is zero. In the following figure at 100 kHz, the phase margin is 0 degrees and the open loop gain is about -31 dB. So the gain margin would be 31 dB in this case. This theoretically means that the loop filter could tolerate a gain of 31 dB which would mean that the VCO gain, charge pump gain, or phase detector could increase by a factor of about 1259 times before the loop filter would have an unstable transfer function. In other words, this loop filter is very stable.

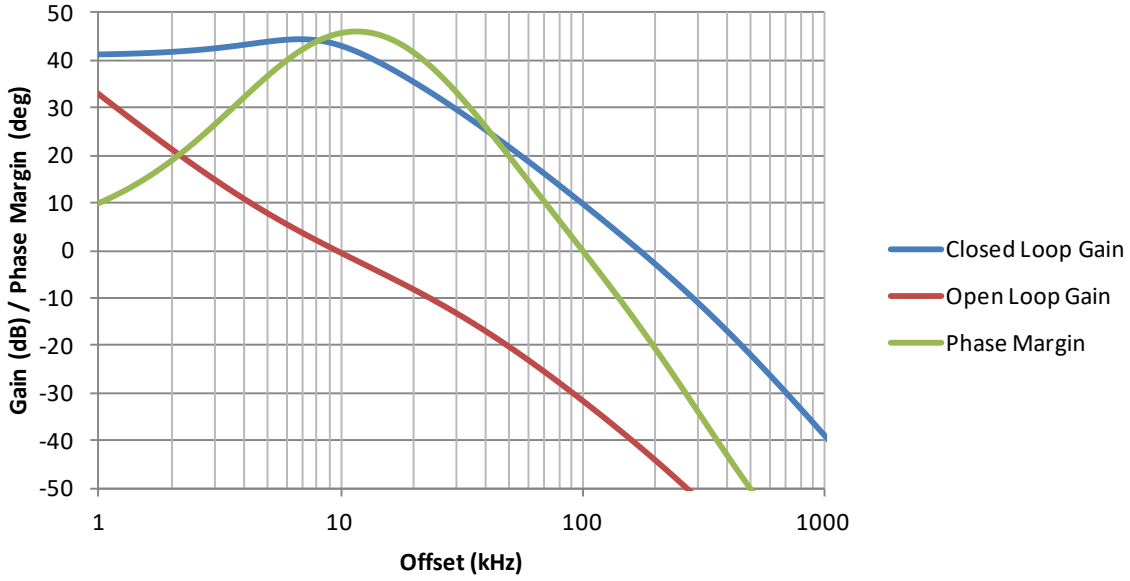


Figure 14.2 *Gain Margin Example*

Gain margin is can be observed from a graph, but it can also be calculated with a closed form solution. To do this, the first step is to find the frequency, ω_{GM}, where the phase margin is zero degrees.

$$tan^{-1}(T2 \cdot \omega_{GM}) + tan^{-1}(T1 \cdot \omega_{GM}) + tan^{-1}(T3 \cdot \omega_{GM}) + tan^{-1}(T4 \cdot \omega_{GM}) = \pi \quad \textbf{(14.1)}$$

Taking the tangent function of both sides and solving for the gain margin frequency yields the following result:

$$\omega_{GM} = \sqrt{\frac{T2 - T1 - T3 - T4}{T1 \cdot T2 \cdot T3 + T1 \cdot T2 \cdot T4 + T2 \cdot T3 \cdot T4 - T1 \cdot T3 \cdot T4}} \quad \textbf{(14.2)}$$

For the purposes of simplifying calculations and also to resolve any concerns that one may have about the pathological case of a fourth order filter with complex poles, one can also express this in terms of the filter constants.

$$\omega_{GM} = \sqrt{\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}} \quad \textbf{(14.3)}$$

Provided that this frequency is greater than the loop bandwidth, the gain margin will be greater than zero. It turns out that for the second order loop filter, the gain margin is infinite. Later on, it will be shown that the gain margin in combination with a requirement of poles is a necessary and sufficient requirement for Pole Stability.

Routh's Stability Criteria

This method allows one to check if all the poles of the PLL closed loop transfer function are in the left hand plane without having to explicitly calculate them. It involves creation of a Routh table from coefficients to determine stability. The system is stable if and only if all the elements in the first column of this array are positive.

The first step is to get the coefficients for this table. The open loop transfer function for a loop filter up to 4th order can be expressed as follows:

$$T(s) = \frac{N \cdot K \cdot (1 + s \cdot T2)}{s^2 \cdot (A3 \cdot s^3 + A2 \cdot s^2 + A1 \cdot s + A0)} \quad \textbf{(14.4)}$$

$$K = \frac{K_{PD} \cdot K_{VCO}}{N} \quad \textbf{(14.5)}$$

The closed loop transfer function is as follows:

$$\frac{G(s)}{1+{}^{G(s)}/_{N}} = \frac{N \cdot K \cdot (1 + s \cdot T2)}{A3 \cdot s^5 + A2 \cdot s^4 + A1 \cdot s^3 + A0 \cdot s^2 + T2 \cdot K \cdot s + K} \qquad \textbf{(14.6)}$$

The Routh table is formed by forming the first row with the highest order term, then third highest order term, and so on. The second row starts with the second highest order term, fourth highest order term, and so on. The rows starting with row three and higher are formed by taking the negative of the determinant of the 2 X 2 matrix formed by eliminating the column that the entry of interest is in, and dividing by the first entry in the row above the entry of interest. Any row can be multiplied by a positive constant without affecting stability. Since all the filter coefficients are positive, this means that the denominator portions of the formulas may be disregarded.

$\mathbf{s^n}$	d_n	d_{n-2}	d_{n-4}	...
$\mathbf{s^{n-1}}$	d_{n-1}	d_{n-3}	d_{n-5}	...
	$b_1 = \frac{d_{n-1} \cdot d_{n-2} - d_n \cdot d_{n-3}}{d_{n-1}}$	$b_2 = \frac{d_{n-1} \cdot d_{n-4} - d_n \cdot d_{n-5}}{d_{n-1}}$	...	...
	$c_1 = \frac{b_1 \cdot d_{n-3} - b_2 \cdot d_{n-1}}{b_1}$	...	...	...

Table 14.1 *A Generic Routh Table*

Key Results Regarding Pole Stability

Summarizing results, we see that Routh's stability criteria implies that a gain margin greater than one with a pole constraint is a necessary and sufficient condition for pole stability.

Filter Order	ω_{GM}	***Gain Margin***	***Pole Constraint***
2	Infinite	Infinite	*T2 > T1*
3	$\sqrt{\frac{T2 \cdot A0 - A1}{T2 \cdot A2}}$	$\frac{A1 \cdot \lvert T2 \cdot A0 - A1 \rvert}{K \cdot T2^2 \cdot A2}$	*T2 > T1+T3*
4	$\sqrt{\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}}$	$\frac{\lvert (T2 \cdot A0 - A1) \cdot (A2 \cdot A1 - A0 \cdot A3) \rvert}{K \cdot (T2 \cdot A2 - A3)^2}$	*T2 > T1+T3+T4*

Table 14.2 *Gain Margin Calculations*

Conclusion

The types of stability for loop filters have been investigated. Discrete sampling instability occurs when the loop bandwidth is not sufficiently narrow relative to the phase detector frequency. Transfer function instability will result the poles of the closed loop transfer function do not all have negative real parts. It can be shown that this requirement is equivalent to the zero in the loop filter being greater than the sum of the poles of the filter and the gain margin being greater than one.

With the gain margin constraint, this can be met if the loop gain is reduced sufficiently, which can be done if one can sufficiently reduce the charge pump gain, VCO gain, or increase the N divider value. The pole constraint gain is independent of the loop gain and if this is not satisfied, then the filter will always be unstable. However, if the R2 or C2 component is made sufficiently large, eventually the pole constraint will be met as well.

From a stability standpoint, the second order filter is the most stable as there is no gain margin constraint and the pole constraint is always met, except for when the Active A filter is used. For the third and fourth order filter, one common diagnostic is to lower the charge pump gain. Not always, but often this will fix stability issues as it fixes the gain margin constraint.

The most common causes for pole stability are not accounting for a large VCO input capacitance, having too large of a higher order pole, or accidentally swapping C1 and C2 in the loop filter when soldering.

References

[1] Franklin, G., et. al. *Feedback Control of Dynamic Systems* Addison Wesley

[2] Gardner, Floyd *Charge-Pump Phase-Lock Loops IEEE Transactions on Communications*, Vol. COM-28, No. 11, November 1980

Appendix: Key Results from Routh's Stability Criteria

Proof of Routh Stability for a Second Order Filter

The second order loop filter is a special case where ***A3 = A2 = 0***.

s^3	$A1 = T1 \cdot A0$	$T2 \cdot K$
s^2	A0	K
	$K \cdot A0 \cdot (T2 - T1)$	***0***
	K	***0***

Table 14.3 *Routh Table for Second Order Loop Filter*

Now from the definition of ***K***, it is clear that ***K>0***. From the third row, this puts the restriction that ***T2 > T1***. For a second order (except for the Active A), this is always the case because:

$$T2 = C2 \cdot R2 \qquad \textbf{(14.7)}$$

$$T1 = T2 \cdot \frac{C1}{C1 + C2} \qquad \textbf{(14.8)}$$

Appendix B: Derivations for the Third Order Filter

Calculation of Gain Margin

The gain margin frequency is simply found by setting ***A3=0***.

$$\omega_{GM} = \sqrt{\frac{T2 \cdot A0 - A1}{T2 \cdot A2}} \tag{14.9}$$

To find the actual gain margin, plug this in the closed loop expression:

$$|G(j \cdot \omega_{GM})| = \frac{K}{(\omega_{GM})^2} \cdot \left| \frac{1 + (j \cdot \omega_{GM}) \cdot T2}{A2 \cdot (j \cdot \omega_{GM})^2 + A1 \cdot (j \cdot \omega_{GM}) + A0} \right| \tag{14.10}$$

Now substitute the expression for the gain margin frequency

$$|G(j \cdot \omega_{GM})| = \frac{K}{\left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2}\right)} \cdot \sqrt{\frac{1 + \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2}\right) \cdot T2^2}{\left(A0 - A2 \cdot \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2}\right)\right)^2 + A1^2 \cdot \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2}\right)}} \tag{14.11}$$

Now do some simplifications:

$$|G(j \cdot \omega_{GM})| = \frac{K \cdot A2 \cdot T2}{|T2 \cdot A0 - A1|} \cdot \sqrt{\frac{1 + \frac{A0 \cdot T2^2}{A2} - \frac{A1 \cdot T2}{A2}}{\frac{A1^2}{T2^2} \cdot \left(1 + \frac{A0 \cdot T2^2}{A2} - \frac{A1 \cdot T2}{A2}\right)}} \tag{14.12}$$

Gain Margin is the reciprocal of this gain, so the final result after simplifications is:

$$Gain\ Margin = \frac{A1 \cdot |T2 \cdot A0 - A1|}{K \cdot A2 \cdot T2^2} \tag{14.13}$$

Analysis Using Routh's Stability Criteria

For the third order filter, the Routh Table is as follows.

s^4	*A2*	*A0*	*K*
s^3	*A1*	$T2 \cdot K$	*0*
	$A1 \cdot A0 - K \cdot A2 \cdot T2 = x$	$A1 \cdot K$	*0*
	$K \cdot (T2 \cdot x - A1^2)$	*0*	*0*
	$K^2 \cdot A1 \cdot (T2 \cdot x - A1^2)$	*0*	*0*

Table 14.4 *Third Order Routh Stability Table*

The elements in the third, fourth, and fifth rows will all be positive provided that:

$$T2 \cdot x - A1^2 > 0 \tag{14.14}$$

If this is expressed in terms of filter coefficients, then the following rule can be derived:

$$\frac{A1}{K} \cdot \frac{T2 \cdot A0 - A1}{T2^2 \cdot A2} > 1 \tag{14.15}$$

Comparing this expression to the one for gain margin, it is very similar except that we need to ensure that the expression T2·A0 - A1 is not negative. To see the conditions required to make this true, substitute in the poles of the filter to find an additional constraint.

$$\frac{T1 + T3}{K \cdot T2^2} \cdot A0 \cdot (T2 - T1 - T3) > 1 \tag{14.16}$$

This constraint will be met provided the following condition is met.

$$T2 > T1 + T3 \tag{14.17}$$

From these rules, the practical learning is that the gain margin is a measure of the stability. The simple rule regarding the poles is sometimes a useful check because gain margin is often expressed in terms of dB and this gives clarity to the case where it is negative.

Derivations for the Fourth Order Loop Filter

Calculation of Gain Margin

The gain margin frequency has been found.

$$\omega_{GM} = \sqrt{\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}} \tag{14.18}$$

To find the actual gain margin, plug this in the closed loop expression:

$$|G(j \cdot \omega_{GM})| = \frac{K}{(\omega_{GM})^2} \cdot \left| \frac{1 + (j \cdot \omega_{GM}) \cdot T2}{A3 \cdot (j \cdot \omega_{GM})^2 + A2 \cdot (j \cdot \omega_{GM})^2 + A1 \cdot (j \cdot \omega_{GM}) + A0} \right| \tag{14.19}$$

Now substitute the expression for the gain margin Frequency

$$|G(j \cdot \omega_{GM})| = \frac{K}{\left|\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}\right|} \cdot \sqrt{\frac{1 + \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}\right) \cdot T2^2}{\left(A0 - A2 \cdot \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}\right)\right)^2 + \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}\right) \cdot \left(A1 - A3 \cdot \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}\right)\right)}} \tag{14.20}$$

Now do some simplifications

$$|G(j \cdot \omega_{GM})| = \frac{K \cdot |T2 \cdot A2 - A3|}{|T2 \cdot A0 - A1|} \cdot \sqrt{\frac{1 + \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}\right) \cdot T2^2}{\frac{(A1 \cdot A2 - A0 \cdot A3)^2}{(T2 \cdot A3 - A3)^2}\left[1 + \left(\frac{T2 \cdot A0 - A1}{T2 \cdot A2 - A3}\right) \cdot T2^2\right]}} \tag{14.21}$$

Gain Margin is the reciprocal of this gain, so the final result after simplifications is:

$$Gain\ Margin = \frac{|(T2 \cdot A0 - A1) \cdot (A2 \cdot A1 - A0 \cdot A3)|}{K \cdot (T2 \cdot A2 - A3)^2} \tag{14.22}$$

Conditions for Fourth Order Loop Filter Routh Stability

For the fourth order filter, there is some added complexity, but the general rule remains the same. There is a restriction on high the loop gain, ***K***, can be, and also there is a restriction that ***T2 > T1 + T3 + T4***. Table 14.5 shows the coefficients for a fourth order loop filter.

s^5	$A3$	$A1$	$T2 \cdot K$
s^4	$A2$	$A0$	K
s^3	$A2 \cdot A1 - A0 \cdot A3 = x$	$K \cdot (A2 \cdot T2 - A3) = K \cdot y$	0
	$A0 \cdot x - A2 \cdot K \cdot y$	$K \cdot x$	0
	$K \cdot y \cdot (A0 \cdot x - A2 \cdot K \cdot y) - K \cdot x^2$	0	0
	$K \cdot x \cdot [y \cdot (A0 \cdot x - A2 \cdot K \cdot y) - K \cdot x^2]$	0	0

Table 14.5 *Fourth Order Routh Stability Table*

This imposes three constraints:

$$A2 \cdot A1 - A0 \cdot A3 > 0 \qquad \textbf{(14.23)}$$

$$A0 \cdot x - A2 \cdot K \cdot y > 0 \qquad \textbf{(14.24)}$$

$$y \cdot (A0 \cdot x - A2 \cdot K \cdot y) - \mathrm{x}^2 > 0 \qquad \textbf{(14.25)}$$

If one substitutes in the time constants in place of the filter coefficients, we find easily find that the first constraint is always satisfied provided restriction (14.31) is assumed.

The third constraint implies that

$$x \cdot y \cdot A0 - A2 \cdot y^2 \cdot \mathrm{K} - \mathrm{x}^2 > 0 \qquad \textbf{(14.26)}$$

This can be rearranged to say the following:

$$\frac{(A2 \cdot A1 - A0 \cdot A3) \cdot (A2 \cdot T2 - A3) - (A2 \cdot A1 - A0 \cdot A3)^2}{K \cdot (A2 \cdot T2 - A3)^2 \cdot A2} > 1 \qquad \textbf{(14.27)}$$

After some labor, we get the following:

$$\frac{(T2 \cdot A0 - A1) \cdot (A2 \cdot A1 - A0 \cdot A3)}{K \cdot (A2 \cdot T2 - A3)^2} > 1 \qquad \textbf{(14.28)}$$

This simplifies to the constraint of:

$$\frac{(T2 \cdot A0 - A1) \cdot (A2 \cdot A1 - A0 \cdot A3)}{K \cdot (A2 \cdot T2 - A3)^2} > 1 \qquad \textbf{(14.29)}$$

This constraint looks almost identical to the gain margin without the absolute value signs. The denominator is always positive and the right side term on the numerator is positive. This leaves a constraint on the other side to be positive. In other words

$$T2 \cdot A0 - A1 > 0 \qquad \textbf{(14.30)}$$

This simplifies to the expected constraint of

$$T2 > T1 + T3 + T4 \qquad \textbf{(14.31)}$$

Just as in the third order case, Routh's stability criteria imply that the gain margin is greater than zero and ***T2*** is greater than the sum of the poles.

Chapter 15 A Sample Loop Filter Analysis

Introduction

This chapter is an example of a PLL analysis that applies many of the formulas and concepts that were derived in previous chapters.

Symbol	Description	Value	Units
K_{PD}	Charge Pump Gain	5	mA
K_{VCO}	VCO Gain	30	MHz/V
f_{VCO}	Output Frequency	900	MHz
f_{PD}	Phase detector frequency	200	kHz
C1	Loop Filter Capacitor	5.600	nF
C2	Loop Filter Capacitor	100.00	nF
C3	Loop Filter Capacitor	0.330	nF
*C4**	Loop Filter Capacitor *(Not Accounting For VCO input Capacitance)	0.082	nF
C_{VCO}	VCO Input Capacitance	0.022	nF
R2	Loop Filter Resistor	1.0	kΩ
R3	Loop Filter Resistor	6.8	kΩ
R4	Loop Filter Resistor	33.0	kΩ

Table 15.1 *Sample Loop Filter*

Calculate Basic Parameters

$$N = \frac{f_{PD}}{f_{VCO}} \tag{15.1}$$

$$C4 = C4^{*} + C_{VCO} \tag{15.2}$$

$$A0 = C1 + C2 + C3 + C4 \tag{15.3}$$

$$A1 = C2 \cdot R2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) + C4 \cdot R4 \cdot (C1 + C2 + C3) \tag{15.4}$$

$$A2 = C1 \cdot C2 \cdot R2 \cdot R3 \cdot (C3 + C4) + C4 \cdot R4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2 + C2 \cdot C3 \cdot R2) \tag{15.5}$$

$$A3 = C1 \cdot C2 \cdot C3 \cdot C4 \cdot R2 \cdot R3 \cdot R4 \tag{15.6}$$

Start with the loop filter transfer function.

$$Z(s) = \frac{1 + s \cdot C2 \cdot R2}{s \cdot (A3 \cdot s^3 + A2 \cdot s^2 + A1 \cdot s + A0)} \quad \textbf{(15.7)}$$

$$G(s) = \frac{K_{PD} \cdot K_{VCO} \cdot Z(s)}{s} \quad \textbf{(15.8)}$$

BW, the loop bandwidth can be found by numerically solving the following equation.

$$\|G(BW \cdot 2\pi \cdot i)\| = N \quad \textbf{(15.9)}$$

Once ***BW*** is known, the phase margin and gamma optimization parameter can also be calculated.

$$\phi = \angle G(BW \cdot 2\pi \cdot j) + 180° \quad \textbf{(15.10)}$$

$$\gamma = \frac{(BW \cdot 2\pi)^2 \cdot C2 \cdot R1 \cdot A1}{A0} \quad \textbf{(15.11)}$$

Symbol	Description	Value	Units
N	N Counter Value	4500	none
C4	Loop Filter Capacitor accounting for VCO input Capacitance	0.104	nF
A0	Total Capacitance	106.0340	nF
A1	First order loop filter coefficient	1.2786×10^{-3}	nF·s
A2	Second Order loop filter coefficient	4.5011×10^{-9}	$nF \cdot s^2$
A3	Third Order loop filter coefficient	4.3128×10^{-15}	$nF \cdot s^3$
BW	Loop Bandwidth	5.0857	kHz
ϕ	Phase Margin	50.7527	degrees
γ	Gamma Optimization Parameter	1.2313	none

Table 15.2 *Calculated Filter Coefficients and Parameters*

Finding the Poles and Zero

Solving for ***T1*** is the hard part. First a cubic polynomial must be solved, and the results need to be manipulated in order to obtain ***T1***. Once ***T1*** is known, the other poles are easy to find. The following cubic polynomial needs to be solved for ***x***, and then ***y*** can be calculated.

$$x^3 - 2 \cdot \frac{A1}{A0} \cdot x^2 + \left(\frac{A1^2}{A0^2} + \frac{A2}{A0}\right) \cdot x + \left(\frac{A3}{A0} - \frac{A1 \cdot A2}{A0^2}\right) = 0 \quad \textbf{(15.12)}$$

$$y = \mathrm{x}^2 - \frac{A1}{A0} \cdot x + \frac{A2}{A0} \quad \textbf{(15.13)}$$

$$T3, T4 = \frac{\mathrm{x} \pm \sqrt{x^2 - 4 \cdot y}}{2} \quad \textbf{(15.14)}$$

$$T1 = \frac{\mathrm{A3}}{A0 \cdot y} \quad \textbf{(15.15)}$$

Now that the poles are known, reorder them such that:

$$T1 \geq T3 \geq T4 \quad \textbf{(15.16)}$$

Calculate the zero.

$$T2 = C2 \cdot R2 \quad \textbf{(15.17)}$$

Symbol	Description	Value	Units
x	Intermediate Calculation	1.0498×10^{-5}	s
y	Intermediate Calculation	2.6072×10^{-11}	s^2
$T1$	Loop Filter Pole	6.4665×10^{-6}	s
$T2$	Loop Filter Zero	1.0000×10^{-4}	s
$T3$	Loop Filter Pole	4.0318×10^{-6}	s
$T4$	Loop Filter Pole	1.5601×10^{-6}	s
$\frac{T3}{T1}$	Pole Ratio	62.3481	%
$\frac{T4}{T3}$	Pole Ratio	38.6947	%
$\frac{1}{2\pi \cdot \lvert T1 \rvert}$	Frequency of Loop Filter Pole	24.6121	kHz
$\frac{1}{2\pi \cdot T2}$	Frequency of Loop Filter Zero	1.5915	kHz
$\frac{1}{2\pi \cdot \lvert T3 \rvert}$	Frequency of Loop Filter Pole	39.4753	kHz
$\frac{1}{2\pi \cdot \lvert T4 \rvert}$	Frequency of Loop Filter Pole	102.0173	kHz

Table 15.3 *Calculated Filter Poles*

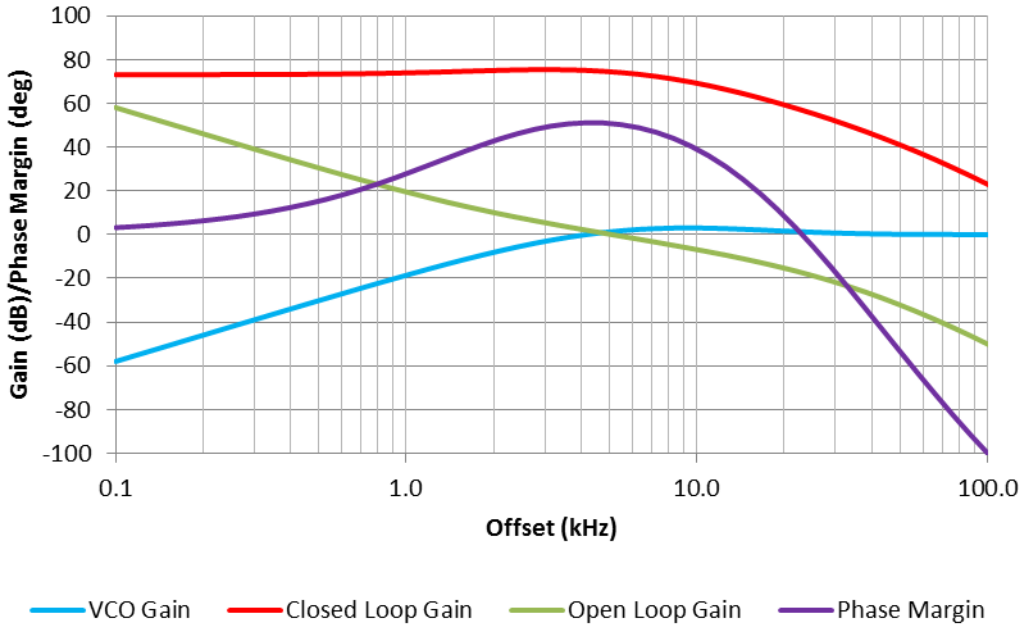
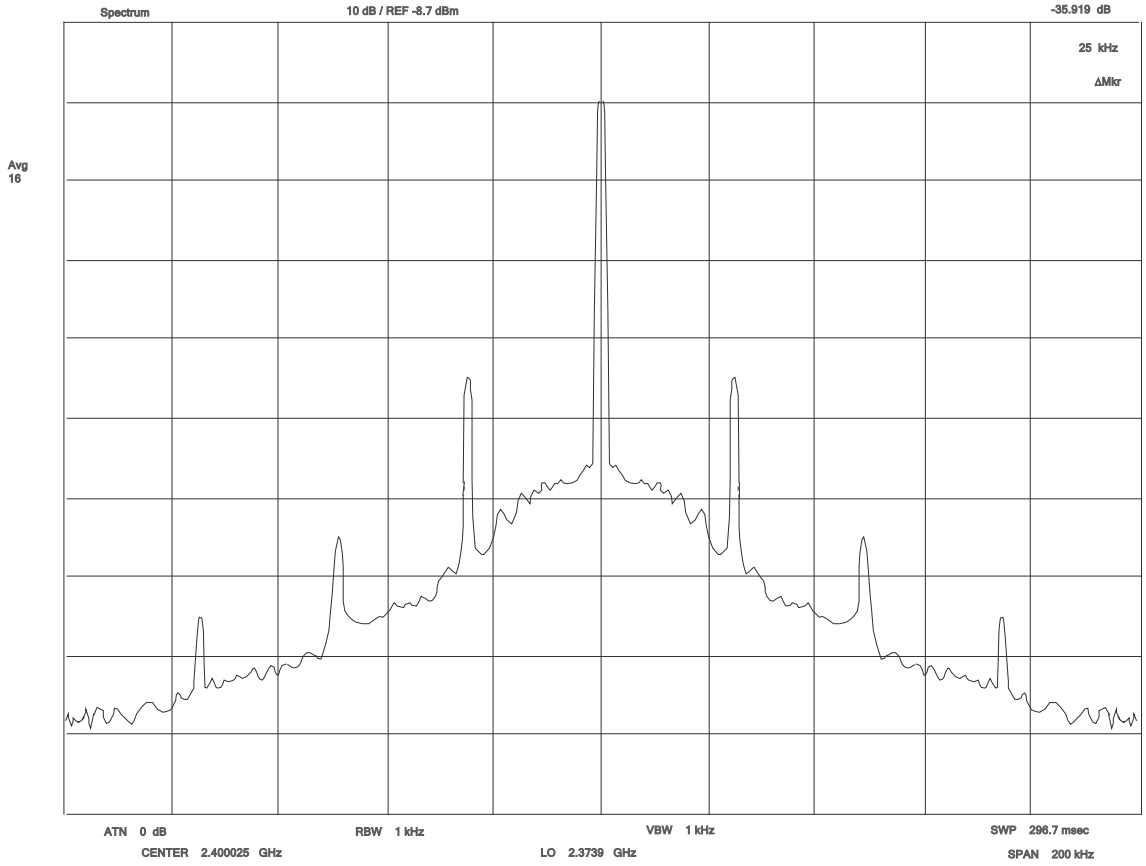


Figure 15.1 *Loop Filter Transfer Functions*

Spurs


Spectrum
10 dB / REF -8.7 dBm
-35.919 dB
25 kHz
ΔMkr
Avg
16
ATN 0 dB
RBW 1 kHz
VBW 1 kHz
SWP 296.7 msec
CENTER 2.400025 GHz
LO 2.3739 GHz
SPAN 200 kHz

Chapter 16 Direct Spurs

Introduction

Modulated Spurs vs. Direct Spurs

The two broad classes that spurs can be divided into are *Modulated Spurs* and *Direct Spurs.* Modulated spurs occur at equal offset from the right and left of the carrier and are the result of the carrier being modulated; these will be discussed later. Direct PLL spurs are those that appear at the output and are not the result of the VCO or the output buffer being modulated.

Spur Type	Direct	Modulated
Intended Signal	$A \cdot sin(2\pi \cdot f_{out} \cdot t)$	
Unintended Signal	$B \cdot sin(2\pi \cdot f_{Spur} \cdot t)$	
Total Signal	$A \cdot sin(2\pi \cdot f_{out} \cdot t) + B \cdot sin(2\pi \cdot f_{Spur} \cdot t)$	$A \cdot B \cdot sin(2\pi \cdot f_{out} \cdot t) \cdot sin(2\pi \cdot f_{Spur} \cdot t) = \frac{A \cdot B}{2} \cdot sin(2\pi \cdot (f_{out} - f_{Spur}) \cdot t) - \frac{A \cdot B}{2} \cdot sin(2\pi \cdot (f_{out} + f_{Spur}) \cdot t)$
Spur Frequencies	f_{Spur}	$f_{Spur} \pm f_{out}$

Table 16.1 *Comparison between Direct and Modulated Spurs*

Direct PLL spurs tend to involve much less PLL theory and loop dynamics then their counterparts, but nonetheless are important to understand.

Common Direct Spur Types

The following table gives some of the more common types of direct PLL spurs

Spur Type	Frequency	Comment
External Crosstalk	*Varies*	These spurs tend to be not by sources external to the PLL, such as power supply.
Output and VCO Harmonics	$k \cdot f_{VCO}$ $k=2,3,4,\ldots$	Occur at multiples of the VCO frequency with odd harmonics tending to be stronger.
Output ½ Harmonic	$f_{OUT}/2$	Occurs when there is a doubler after the VCO and the fundamental VCO frequency leaks through.
OSCin Harmonics	$k \cdot f_{OSC}$ $k>2,3,4,\ldots$	Occur at multiples of the OSCin frequency, in a similar way to VCO harmonics.
Phase Detector Harmonics	$k \cdot f_{PD}$ $k=2,3,4,\ldots$	Occur at multiples of the phase detector frequency. For PLLs used in fractional mode there can also be a collection of spurs near this frequency.
MASH Engine Spurs	*Near* f_{PD} *and* $f_{PD}/2$	This tends to be a family of spurs that only happens for delta sigma fractional PLLs due to noise from the MASH engine.
Output to Output Spurs	f_{OUT} *from another output*	These spurs are the direct output from another PLL or output. For instance, if a clocking device was to have an output of 200 and 300 MHz, then there would be a 200 MHz spur on the 300 MHz output

Table 16.2 *Types of Direct Spurs*

External Crosstalk Spur

Description and Diagnosis

The external crosstalk spur is a generic term for any spur that occurs that is not related to the PLL. When the PLL is powered down with the rest of the circuit running, this spur persists.

Cause and Mitigation

This spur could be the result of power supplies, lights, computer screens, other devices on the PCB, a spur riding on the input signal, or even something being produced by the spectrum analyzer itself. The general way to approach this spur is start systematically eliminating causes until it is found. If nothing seems to make it go away, try driving the spectrum analyzer directly with a signal generator to ensure that the spur is not inherent to the test setup.

Output and VCO Harmonics

Description and Diagnosis

These spurs appear at the VCO frequency and multiples thereof and change with the VCO frequency. All VCOs put out harmonics of some kind that occur at multiples of the desired frequency. Sometimes odd harmonics may actually be desired if in the right proportions, such as the case for the odd harmonics of a square wave. However, the even harmonics are never desirable and the odd harmonics in the wrong proportions are also not good. Harmonics can be a concern if they trick the PLL input pin to count them instead of the fundamental signal. As a rule of thumb, it is good to have the second harmonic 20 dB down if possible, but that is very dependent on the matching and the sensitivity of the PLL.

Cause and Mitigation

VCOs are part specific in what level of harmonics they produce, but they all produce undesired harmonics of the fundamental frequency. For a differential output, unequal termination of the unused side can cause high harmonics. If the VCO harmonics cause a problem there are several things that can be done to reduce their impact. They can be low pass filtered with LC or RC filters. A resistor or inductor can be placed in series at the fin pin to prevent them from causing the prescaler to miscount. Matching is also important and having short traces and good matching can stop the harmonic from causing the prescaler to miscount. Note also that the many PLLs do not have 50 Ω input impedance and treating it as such often can cause matching issues.

Output ½ Harmonic

Description and Diagnosis

This spur occurs at a frequency equal to ½ of the output frequency. When the VCO frequency is changed, this spur will stay at half of the output frequency

Cause and Mitigation

The most common cause of this spur is when a doubler is used after a VCO to get a higher frequency. In this case, the fundamental VCO frequency leaks to the output and the spur occurs. This spur is PLL specific, so one solution is to choose another device, perhaps one that does not use a doubler. Aside from that, this spur can also be removed by an external filter on the output.

OSCin Harmonics

Description and Diagnosis

This spur is visible at an offset from the carrier equal to some multiple of the input frequency. It is very common for this to be a whole family of harmonics, with the odd harmonics being stronger than the even harmonics. This spur sometimes is reduced if the power supply to the input buffer is reduced and sometimes goes away of the PLL is driven with an external signal generator.

Cause and Mitigation

In the case that source of the OSCin signal is completely external to the PLL, this spur is often impacted by the format of this signal, in particular if the amplitude is higher. As a general recommendation, lower amplitude and higher slew rate input signals are desired. Sometimes putting filters to reduce the harmonics of the input signal can also be helpful in this case.

In the case that the source of the OSCin signal includes a crystal that uses an inverter on the PLL chip, this spur is often the result of excessive gain of this inverter. Some mitigation techniques may include reducing the input voltage to the inverting buffer, putting a series resistor at the output of the inverter, or putting a slightly larger load capacitor at the output of the inverter. The only caution with these approaches is to ensure that these changes are not too drastic as they can impact the oscillation of the crystal circuit.

Phase Detector Harmonics

Description and Diagnosis

This spur appears at multiples of the phase detector frequency. Sometimes, it goes away or is reduced when the charge pump is powered down.

Cause and Mitigation

Phase detector harmonics are typically caused by the phase detector noise getting to the output. Often a supply pin to the charge pump can inject spur energy onto the ground plane or power supply. For diagnostic purposes, try lowering the charge pump gain to see if it has an impact on this spur. If the charge pump is suspected to be the cause, sometimes this spur can be reduced by isolating the charge pump supply pin with series resistance or inductance.

MASH Engine Spurs

Description and Diagnosis

This is actually a collection of spurs at a frequency around $f_{PD/}$ and $f_{PD/}2$. They only occur in fractional PLLs. When the fractional part of the PLL is powered down, or the fractional numerator is set to zero with dithering disabled, the spur goes away

Cause and Mitigation

When the MASH engine is running, it creates a lot of fractional noise that may find its way to the output. If the crosstalk is internal to the chip, then the only mitigation is to tinker with the fractional settings. However, in many cases, it can be caused by board crosstalk and isolating the power supply pin to the MASH engine may help. Also realize that if one puts a shunt capacitor on the power supply pin to the MASH engine or the charge pump supply, it can transfer spur energy to the ground plane that can later show up at the output.

Output to Output Spurs

Description and Diagnosis

This spur occurs when there are two outputs running at different frequencies. For instance, if one output is 400 MHz and one output is 500 MHz, then one can observe a 400 MHz spur on the 500 MHz output. When the output not being observed is powered down, the spur goes away. The spur tends to be more of an issue for outputs that are closer together or ones that share dividers or buffers internal to the chip.

Cause and Mitigation

This spur is caused by crosstalk between outputs. This crosstalk can be on the die of the chip, across bond wires, or on the board. When there is some flexibility of choice, planning which frequency goes on which output has a large impact on this spur. For instance, put the same frequencies on outputs that are known to have lots of interaction. Output format can also have a large impact. Lower amplitude differential outputs like LVDS tend to be the best. If using differential output programmed to a CMOS format, it is best to have each side programmed to opposite polarity, even if only one side is used. Power supply decoupling can also have an impact. Bypass capacitors for the output power supply pins can actually be hurtful as they can couple spur energy direct to the ground plane that shows up by other outputs. If this is the case, isolating these power supplies by removing these capacitors or placing series ferrite beads tends to be very effective.

Conclusion

Direct spurs are those that occur at the output without causing double-sideband modulation. The spurs discussed in this chapter are measured directly at the frequency stated, as opposed to modulated spurs that are measured at an offset from the carrier, which is the next chapter.

Chapter 17 Modulated Spurs

Introduction

Modulated spurs are the result of a spur source directly modulating the VCO or the output. One of the telltale signs that distinguish them from direct spurs is that they occur in pairs at equal offset from the carrier of equal amplitude. Many noise sources modulate the carrier frequency and these spurs are measured at an offset from the carrier. For instance, if one has a 900 MHz signal and spurs at +/- 1 MHz offset, the actual spur frequencies would be 899 and 901 MHz. The spurs that modulate the carrier will be discussed in greater depth in other chapters, but this chapter will give an overview of the most common types, with a focus on being to identify these spurs by offset. For some of these spurs, all the details are in this chapter, and for others, other chapters go into much greater depth.

The first step in dealing with these spurs is to identify them by offset frequency and then do some verification to find the correct mechanism that causes them. Once this is done, then one can do optimizations around the spur.

Relationship between Frequency Modulation and Spurs

Modulated spurs can be viewed as FM modulation on the VCO frequency. The principles of sinusoidal modulation have been discussed, but this modulation is generally not a sine wave. However, it is fair to assume it is periodic on the interval 0 to L. Under this assumption, the modulating waveform can be represented by a Fourier series which can be in either the form of sine and cosine functions or complex exponential functions.

$$m(t) = \sum_{n=0}^{\infty} a_n \cdot cos\left(\frac{n \cdot \pi \cdot t}{L}\right) + b_n \cdot sin\left(\frac{n \cdot \pi \cdot t}{L}\right) = \sum_{n=-\infty}^{\infty} c_n \cdot \exp\left(j \cdot \frac{n \cdot \pi \cdot t}{L}\right) \quad \textit{(17.1)}$$

The Fourier coefficients can be calculated as follows:

$$a_n = \frac{2}{L} \cdot \int_0^L m(t) \cdot cos\left(\frac{n \cdot \pi \cdot t}{L}\right) \cdot \mathrm{dt} \quad \textit{(17.2)}$$

$$b_n = \frac{2}{L} \cdot \int_0^L m(t) \cdot sin\left(\frac{n \cdot \pi \cdot t}{L}\right) \cdot \mathrm{dt} \quad \textit{(17.3)}$$

$$c_n = \frac{2}{L} \cdot \int_{-L}^L m(t) \cdot exp\left(j \cdot \frac{n \cdot \pi \cdot t}{L}\right) \cdot \mathrm{dt} \quad \textit{(17.4)}$$

From the Fourier series, the component for ***n=0*** represents the carrier. For the other spurs, we see that the lowest frequency spur occurs at an offset frequency that is equal to the repeat frequency of the modulating waveform, 1/L. The offset frequency of the ***n^th^*** spur is given by:

$$f_{Spur} = \frac{n}{L} \tag{17.5}$$

The amplitude of these spurs can be calculated from the Fourier coefficients as follows:

$$f_{dev} = \|c_n\| = \sqrt{(a_n)^2 + (b_n)^2} \tag{17.6}$$

As the frequency deviation and modulation frequency are known, the modulation index of the spur can be calculated.

$$\beta = \frac{f_{dev}}{f_{Spur}} \tag{17.7}$$

It is a fair assumption to assume that the modulation is fairly small and therefore the Bessel function (J_0) and spur level can be approximated as follows:

$$Spur\ Level = 20 \cdot log[J_0(\beta)] \cong 20 \cdot \log\left({}^{\beta}/_{2}\right) \tag{17.8}$$

To test the accuracy of this approximation, Figure 17.1 compares the true spur level to the approximated spur level. In the case that the spur is less than -10 dBc, the approximation introduces less than a 0.1 dB error and if the spur was to be greater than -10 dBc, one probably has bigger issues to worry about than the accuracy of a theoretical model for the spur. Based on this and the fact that it greatly simplifies the math going forward, it will be assumed that the Bessel function can be approximated with good accuracy.

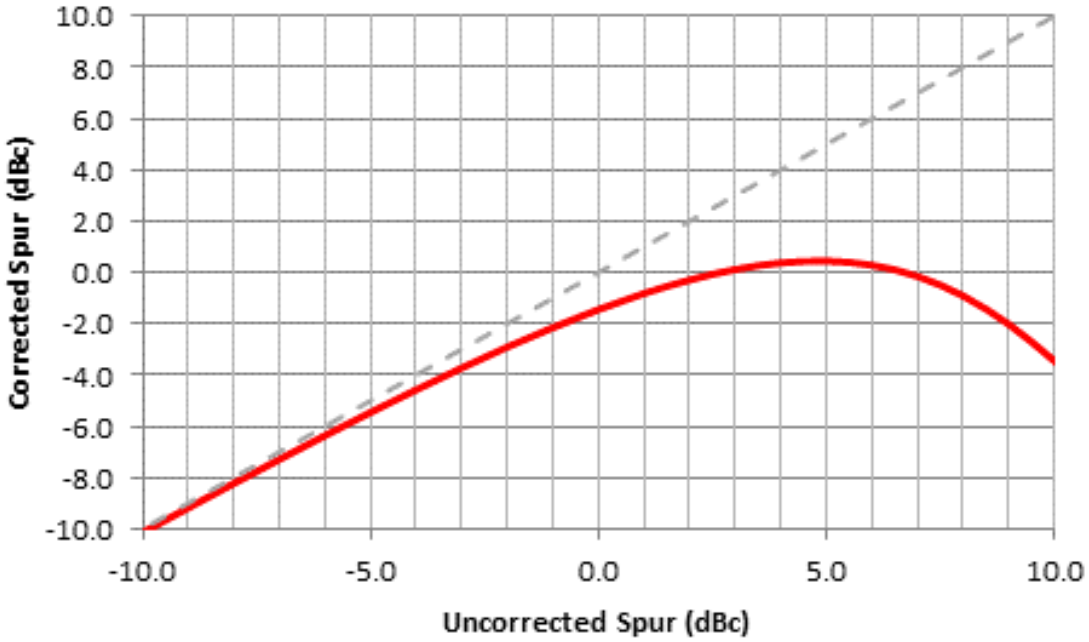


Figure 17.1 *Impact of Approximating the Bessel Function for Spur Level Calculations*

		Modulation Index (β)	Frequency Deviation (Hz)					
			f_{PD} = 10 kHz	f_{PD} = 30 kHz	f_{PD} = 50 kHz	f_{PD} = 100 kHz	f_{PD} = 200 kHz	f_{PD} = 1 MHz
Spur Level (dBc)	-30	6.32e-2	632	1900	3160	6320	12600	63200
	-40	2.00e-2	200	600	1000	2000	4000	20000
	-50	6.32e-3	63	190	316	632	1260	6320
	-55	3.56e-3	36	107	178	356	712	3560
	-60	2.00e-3	20	60	100	200	400	2000
	-65	1.12e-3	11	34	56	112	224	1120
	-70	6.32e-4	6	19	32	63	126	632
	-75	3.56e-4	4	11	18	36	71	356
	-80	2.00e-4	2	6	10	20	40	200
	-85	1.12e-4	1	3	6	11	22	112
	-90	6.32e-5	0.6	2	3	6	13	63

Table 17.1 *Relationship between Spur Level, Modulation Index, and Frequency Variation*

Impact of Division on Spurs

Many synthesizers have a divider after the VCO and it is good to understand the general principle that when one divides by ***D***, the spur offset is unaffected, but the spur magnitude is theoretically decreased by ***20·log(D)***. To demonstrate this principle, consider the following illustration:

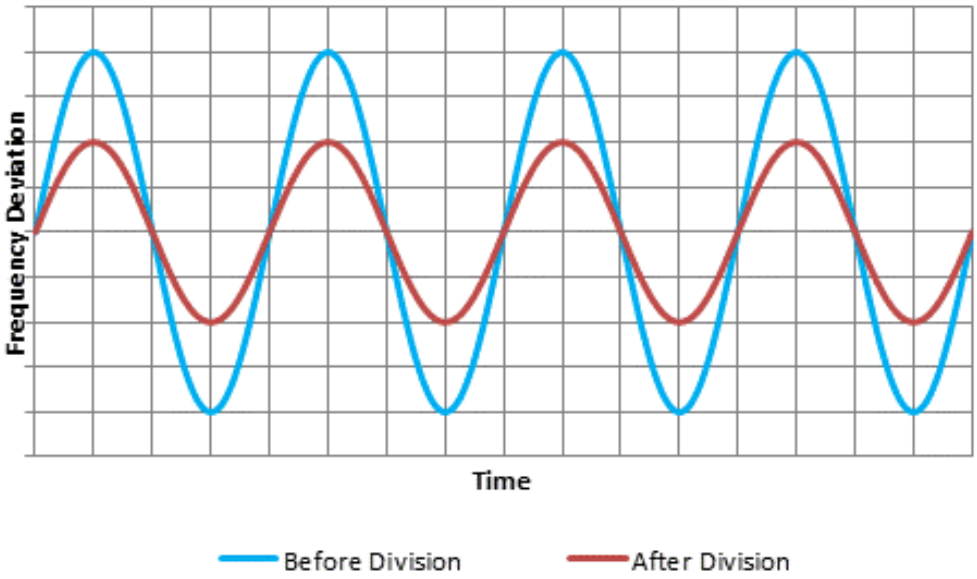


Figure 17.2 *Example with Divide by 2*

The figure shows that dividing by two changes the frequency deviation, f_{DEV}, but does not change the modulation frequency, f_{MOD}. So therefore the spur amplitude is decreased by 6 dB and the spur offset is unchanged. The real-world occurrence that might cause confusion is that when the divide by 2 is employed after a VCO, a spur at ½ the offset can be created. However, this spur is typically the result of coupling between the OSCin path and the VCO and not a result of the division.

Impact of the Loop Filter on Spurs

Inband and Outband Spur Mechanisms

The possible impact that the loop bandwidth can have on spurs can be low pass, high pass, or all pass. *Inband* mechanisms are those that go through the loop and are low pass filtered by it. *Outband* mechanisms are high pass filtered and crosstalk directly to the VCO and follow the VCO transfer function. Some spurs can be completely unaffected by the loop filter and these are all pass filtered.

Spur Gain and Rolloff

Inband spur mechanisms are low pass filtered by the loop filter. The *Spur Gain* is defined as the gain of the closed loop transfer function at spur frequency of interest.

$$SpurGain(f_{Spur}) = 20 \cdot log\left\|CL(2\pi \cdot j \cdot f_{Spur})\right\| \quad \textbf{(17.9)}$$

In cases where the spur frequency of interest is far outside the loop bandwidth, the spur gain can be approximated using the open loop transfer function instead of the closed loop transfer function. This greatly simplifies some of the mathematical analysis done later on.

Assuming that the dominant spur mechanism is in band, the level of the spur is directly related to the spur gain. In other words, if the spur gain decreases 1 dB, one would expect the spur at that frequency as well to decrease by 1 dB. The derivation of this is given in the Appendix and the approximations used hold very well provided that the spur level that is predicted is –10 dBc or lower.

Rolloff is how much the loop filter rolls off the spur from inside the loop bandwidth and is given by:

$$Rolloff(f_{Spur}) = SpurGain(f_{Spur}) - 20 \cdot log(N) \quad \textbf{(17.10)}$$

VCOGain

Outband spur mechanisms that crosstalk directly onto the VCO are filtered by the high pass VCO transfer function. *VCOGain* is the value of the VCO transfer function at the spur frequency of interest.

Identification of Modulated Spurs

Introducing the Modulus Operator

The modulus operator "%" is often used to denote remainder. In reference to spurs, "A % B" can be thought of as the distance of *A* to the closest integer multiple of *B*. Some examples would be 1503.7 % 100 = 3.7, 3999.7 % 100 = 0.3, and (9.7 MHz) % (2 MHz) = 300 kHz.

Identification of Spur Type by Offset

The process of identifying a spur first starts by determining the offset it is from the carrier. Then one goes through a list of potential spur types until one reaches a potential cause. It is possible, and usually the case, that there could be multiple spur names for a potential spur and in this case, one could use any of the names. If the dominant mechanism is known, then this is probably the best name

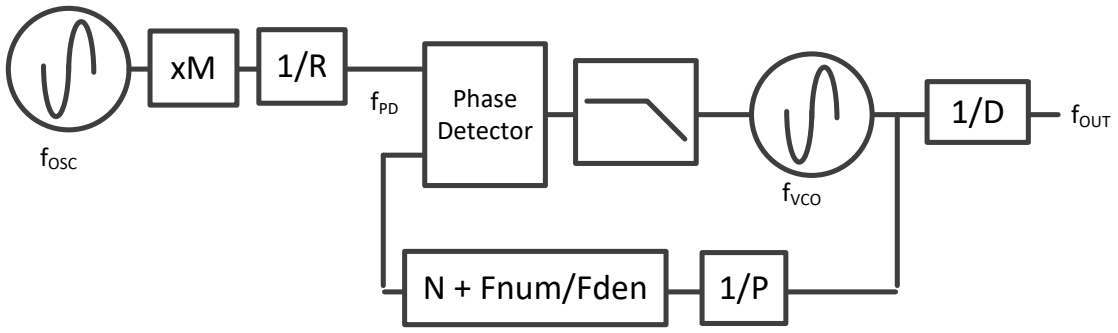


Figure 17.3 *PLL Diagram*

Common Modulated Spur Types

Spur Type	f_{VCO} +/- Offset
f_{OSC}	f_{OSC}
f_{PD}	f_{PD}
f_{VCO}% f_{OSC}	f_{VCO} % f_{OSC}
Integer Boundary	$(f_{PD}/Fden)\cdot(Fnum\%Fden)$
Primary Fractional	$f_{PD}/Fden$
Sub-Fractional	$f_{PD}/Fden/k$ $k=2,3,\ldots$

Table 17.2 *Common Types of VCO Modulated Spurs*

Table 17.2 gives a brief overview of some of the most modulated spur types. Table 17.3 gives an example for identifying modulated spurs by their offset. For the fractional spurs, the fraction is simplified, so the fraction used is 249/500, not 502/1000.

Name	+/- Offset From Carrier	Offset for This Example
f_{OSC}	f_{OSC}	50 MHz
f_{PD}	f_{PD}	75 MHz
f_{VCO}% f_{OSC}	f_{VCO}% f_{OSC}	24.7 MHz
f_{VCO} % f_{PD}	f_{VCO} % f_{PD}	300 kHz
f_{OUT}% f_{OSC}	f_{OUT}% f_{OSC}	7.53 MHz
Integer Boundary	$f_{PD}\cdot(Fnum\%Fden)/Fden$	37.35 MHz
Primary Fractional	$f_{PD}/Fden$	150 kHz
Sub-Fractional	$f_{PD}/Fden/k$	75 kHz

Table 17.3 *Spur Type Identification Example*

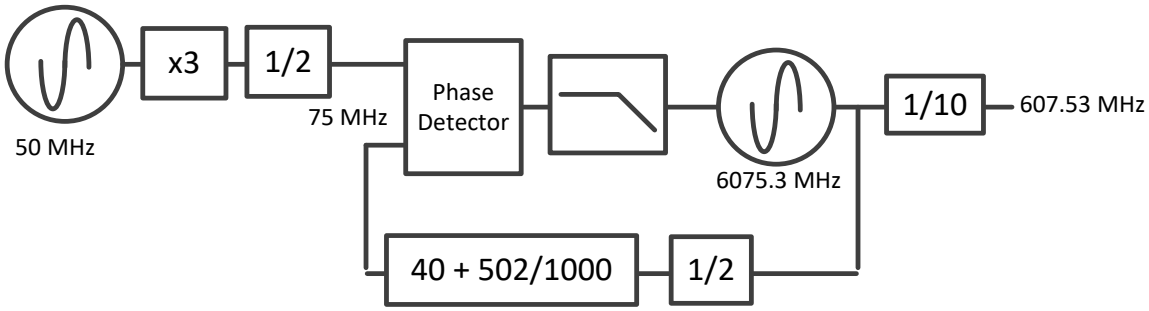


Figure 17.4 *PLL Diagram*

Auxiliary PLL Cross Talk Spur

Description

This spur only occurs in dual PLLs and is seen at a frequency offset from the carrier equal to the difference of the frequencies of the main and auxiliary PLL (or sometimes a higher harmonic of the auxiliary PLL). This spur is most likely to occur if the main and auxiliary sides of a dual PLL are close in frequency. If the auxiliary PLL is powered down, but the auxiliary VCO is running, then this spur can dance around the spectrum as the auxiliary frequency VCO drifts around.

Cause

Parasitic capacitances on the board allow high frequency signals to travel from one PCB trace to another, especially for higher frequencies and longer traces. There can also be cross talk within the chip. The charge pump supply pins are vulnerable to high frequency noise.

Diagnosis

One of the best ways to diagnose this spur is to tune the auxiliary side of the PLL while observing the main side. If the spur moves around, that is a good indication that the spur being observed is of this type. Once this type of spur is diagnosed, then it needs to be determined if the spur is related to cross talk on the board, or cross talk in the PLL. Most PLLs have a power down function that allow one to power down the auxiliary side of a PLL, while keeping the main side running. If the auxiliary side of the PLL is powered down, and the spur reduces in size substantially, this indicates cross talk in the PLL chip. If the spur stays about the same magnitude, then this indicates that there is cross talk in the board.

Cure

Aside from powering down the unused PLL, isolation of the power supply pins can also have an impact on this kind of spur.

Less Common Spur Types

Greatest Common Multiple Spur

This spur occurs in a dual PLL at the greatest common multiple of the two phase detector frequencies. For example, if one side was running with a 25 kHz phase detector frequency, and the other side was running with a 30 kHz phase detector frequency, then this spur would appear at 5 kHz. In some cases, this spur can be larger on certain output frequencies.

The reason that this spur occurs is that the greatest common multiple of the two phase detector frequencies corresponds to the event that both charge pumps come on at the same time. This result can be derived by considering the periods of the two comparison frequencies. When both charge pumps come on at the same time, they produce noise at the charge pump supply pins, which gives birth to this spur.

A couple telltale signs of this type of spur are it is always spaced the same distance from the carrier, regardless of output frequency. However, keeping the output frequency the same, but changing the phase detector frequency causes this spur to move around. Just be sure that when changing the comparison frequencies for diagnostic purposes, you are also changing the greatest common multiple of the two comparison frequencies.

This spur can be treated effectively by putting more capacitors on the Vcc and charge pump supply lines. Be sure that there is good layout and decoupling around these pins. Also consider changing the phase detector frequency of the auxiliary PLL.

Prescaler Miscounting Spur

This spur typically occurs at half the phase detector frequency. On more rare occasions, it can be at one-third, two-thirds, or some fractional multiple of the phase detector frequency. It can have mysterious attributes, such only occurring on odd channels.

This spur is caused by the prescaler miscounting. Things that cause the prescaler to miscount include poor matching to the high frequency input pin, violation of sensitivity specifications for the PLL, and VCO harmonics. Be very aware that although it may seem that the sensitivity requirement for the PLL is being met, poor matching can still agitate sensitivity problems and VCO harmonic problems. Note also that there is an upper sensitivity limitation on the part.

To understand why the prescaler miscounting causes spurs, consider fractional N averaging. Since the prescaler is skipping counts on some occasions and not skipping counts on another, it produces spurs similar to fractional spurs.

Since miscounting ties in one way or another to sensitivity, try varying the voltage and/or temperature conditions for the PLL. Since sensitivity is dependent on these parameters, any dependency to supply voltage or temperature point to prescaler miscounting as the cause of the spur. Changing the ***N*** counter between even and odd values can also sometimes have an impact on this type of spur caused by the ***N*** counter miscounting, and can be used as a diagnostic tool.

Also be aware that ***R*** counter sensitivity problems can cause this spur as well. One way to diagnose the ***R*** counter miscounting is to change the ***R*** counter value just slightly. If the spur seems sensitive to this, then this may be the cause. If a signal generator is connected to the input reference, and the spur mysteriously disappears, then this suggests that the ***R*** counter miscounting is the cause of the spur.

To cure this problem, it is necessary to fix whatever problem is causing the prescaler to miscount. The first thing to check is that the power level is within the specifications of the part. After that, consider the input impedance of the PLL. For many PLLs, this tends to be capacitive. Putting an inductor to match the imaginary part of the PLL input impedance at the operating frequency can usually fix impedance matching issues. Also be aware of the sensitivity and matching to the VCO harmonics, since they can also cause a miscount. Try to keep the VCO harmonics –20 dBm or lower in order to reduce the chance of the PLL miscounting the VCO harmonic.

Prescaler Oscillation Spur

This spur typically occurs far away from the carrier at an offset frequency of approximately the output frequency divided by the prescaler value. In most applications, it is not a concern because it is out of band.

The prescaler oscillation spur is caused internally by the output frequency being divided by the prescaler. It comes out through the high frequency input pin.

This spur is sensitive to isolation between the VCO and the PLL. The frequency offset is a good indicator that the spur may be due to prescaler oscillation. Be sure to power down the PLL and make sure the spur goes away to verify it is not a cross talk issue.

Providing greater isolation for the high frequency input pin of the PLL can be effective in reducing the prescaler oscillation spur. The most basic way is to put a pad with sufficient attenuation. The issue with this is that the attenuation of the pad may be limited by the sensitivity limits of the PLL. Another approach is to put an amplifier, which increases isolation. Yet a third approach is to use a directional coupler, but this is frequency specific and costs layout area.

Conclusion

In this chapter, some of the types of modulated spurs have been discussed. Modulated spurs are those that occur as sidebands of equal amplitude and offset from the carrier, as opposed to direct spurs that occur as just a single spur. In some cases, there can be both direct and modulated spur mechanisms contribute to the same spur. In this case, it is possible to get unequal sidebands as could happen for the f_{VCO} % f_{PD}, f_{VCO} % f_{OSC}, or f_{OUT} % f_{OSC} spur.

Chapter 18 Modulated Crosstalk Spurs

Introduction

Crosstalk can be caused my many factors such as the board layout, but can also be internal to the PLL chip. This can especially be a concern when the VCO is integrated on the chip. In many cases, these spurs might even occur at the same offset and often coincide with the integer boundary spur. These spurs can behave differently for different PLLs and situations and this is why it is good to try to isolate these spurs to understand them. These spurs can be InBand and filtered by the loop filter, or OutBand, which are not filtered by the loop filter. This chapter discusses the three main versions of the modulated crosstalk spur, which would be the f_{VCO}%f_{PD} spur, f_{VCO}%f_{OSC} spur, and the f_{OUT}%f_{OSC} spur.

General Crosstalk Model

The Board for Crosstalk Parasitic Capacitance and Crosstalk Model

The following model is sometimes useful in visualizing how crosstalk can occur.

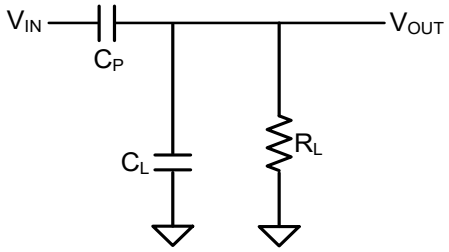


Figure 18.1 *Basic Crosstalk Model*

For lower frequencies, the transfer function increases as 20 dB/decade and then approaches a final value for higher frequencies. In general, this pattern might be seen with several of the crosstalk spurs discussed in this chapter.

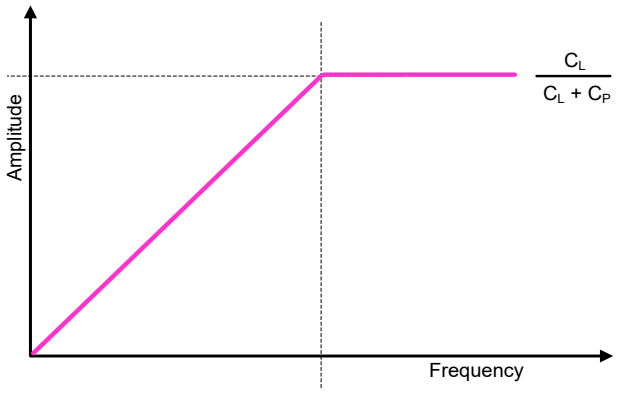


Table 18.1 *Frequency Transfer Function for Crosstalk Model*

Crosstalk Spur Summary

The following table gives some of the more common crosstalk spurs, their suspected causes, and their common behaviors. The mechanisms and trends stated are highly speculative and could vary between applications. Use this table as a general guideline for trends to be watchful of.

Spur Type	InBand or OutBand	Mechanism	General (Not Always) Trends
f_{OSC}	Always OutBand	Stimulus: OSCin Victim: VCO or Output	• Degrades for higher f_{OSC} • Degrades for higher p_{OSC} • Impacted by VCO Core • Improves with VCO Divide
f_{PD}	Always OutBand	Stimulus: R Divider Victim: VCO or Output	• Degrades with f_{PD} • Impacted by VCO Core • Improves with VCO Divide
f_{VCO}%f_{PD}	InBand	Stimulus: R Divider Mixing with N divider Victim: R Divider	• Improves with f_{OSC} • Improves with p_{OSC} • Improves with OSCin Slew Rate • Impacted by VCO Core • Improves with VCO Divide
	OutBand	Stimulus: R Divider Mixing with N divider Victim: VCO	• Degrades with f_{PD} • Impacted by VCO Core • Improves with VCO Divide
f_{VCO}%f_{OSC}	InBand	Stimulus: OSCin Path Victim: VCO	• Impacted by VCO Core • Improves with VCO Divide
	OutBand	Stimulus: OSCin Path Victim: VCO	• Impacted by VCO Core • Improves with VCO Divide
f_{OUT}%f_{OSC}	InBand and OutBand	Stimulus: OSCin Path Victim: Output Power Supply	• Decrease with f_{OSC}
f_{OUT}%f_{PD}	This spur is typically not a high as the other ones and dominated by other mechanisms		

Table 18.2 *Common Crosstalk Spurs*

Input Path Coupling Mechanisms

OSCin Noise Coupling from the N Divider Input

One mechanism for spurs to couple is for the high N divider input to generate noise that can couple to the VCO. The noise generated by this pin can contain the phase detector frequency or MASH spur energy. In the case of an external VCO, one way to mitigate this spur is to add more resistance between the N counter input pin, f_{IN}, and the VCO output.

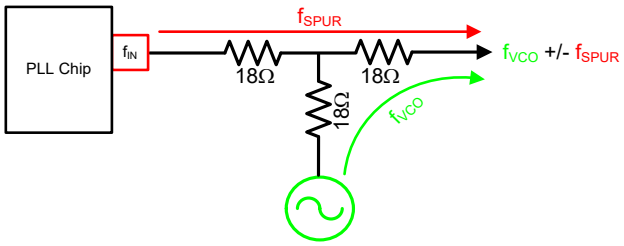


Table 18.3 *Crosstalk Produced by the VCO input Path*

f_{OSC} Spurs

Description and Diagnosis

These occur at an offset that is equal to f_{OSC} or some multiple thereof. They can have the tendency to be worse for higher OSCin power levels, but better for OSCin slew rates. It is best to make the OSCin frequency different than the phase detector frequency to better diagnose this spur.

Cause and Mitigation

These spurs are typically caused by the signal from the OSCin input mixing with the output frequency. This mixing could be internal to the PLL chip or through the board. Optimize the input format for the best spurs. Often the best results are when the OSCin signal is low amplitude but high slew rate. As slew rate is impacted by frequency, changing the input frequency can sometimes help as well. The PCB board can have an impact on this spur, so isolation of supplies from OSCin may be useful. Also, sometimes noise from the OSCin source can corrupt the ground plane, which can later enter to the power and ground supplies of the PLL. So isolating this can sometimes help.

f_{VCO} % f_{OSC} Spurs

Description

These spurs occur at an offset of f_{VCO} % f_{OSC} for synthesizers that integrate the VCO on chip. There should be caution with diagnosing with this spur is that there are several other spurs that can also occur at this offset, so some diagnosis is required. There tend to be both in-band and out-band mechanisms for this spur and for synthesizers that integrate multiple VCO cores, it could be different for each core.

Cause

This spur is caused by crosstalk between the OSCin and VCO paths.

Diagnosis

The first step to diagnose this spur is to distinguish it from the f_{OUT}%f_{OSC}, f_{OUT}%f_{PD}, f_{VCO}%f_{PD}, and IBS spurs. Depending on what multipliers and dividers are on the chip, this might not always be possible. However, to whatever means is possible, shift f_{PD}, f_{OSC}, f_{OUT}, and the PLL fraction to try to isolate this spur. This spur can also be impacted by OSCin slew rate, power, and frequency. If there is any way to better isolate the input path by doing something like enabling a doubler and dividing by two, then this can also can also help isolate this as the spur. For devices with multiple programmable VCO cores, try to find a frequency at the boundary of two VCO cores that has this frequency and see if changing the VCO core, but keeping the same frequency has any impact.

Cure

Optimize the input format, frequency, and power for the best spurs. Often the best results are when the OSCin signal is low amplitude but high slew rate. Sometimes also for devices, this spur is better if you enable the input doubler and divide by two. Although less common, isolation of the VCO power supply from any OSCin signals can help.

f_{OUT} % f_{OSC} Spurs

This spur has many similarities to the f_{VCO} % f_{OSC} spur, except the interaction is with the output instead of the VCO. This spur can only be distinguished from the f_{VCO} % f_{OSC} spur in the case that there is a VCO divider that is not one ($D \neq 1$).

Description

These spurs occur at an offset of f_{OUT} % f_{OSC}. There should be caution with diagnosing with this spur is that there are several other spurs that can also occur at this offset, so some diagnosis is required. Mathematically, this spur offset can be interpreted as a sub-multiple of the f_{VCO} % f_{OSC} spur if an output divider is used. For instance, for an input frequency of 100 MHz, VCO frequency of 2002 MHz and output divide of 2, then this spur would be at 1 MHz output. Some incorrectly assume the 1 MHz offset it is the VCO spur offset (2 MHz) divided by 2, but it is actually because the output is 1001 MHz % 100 MHz = 1 MHz.

Cause

This spur is caused by crosstalk between the OSCin and output buffer.

Diagnosis

The first step to diagnose this spur is to distinguish it from the f_{VCO}%f_{OSC}, f_{OUT}%f_{PD}, f_{VCO}%f_{PD}, and IBS spurs. Depending on what multipliers and dividers are on the chip, this might not always be possible. However, to whatever means is possible, shift f_{PD}, f_{OSC}, f_{VCO}, and the PLL fraction to try to isolate this spur. This spur can also be impacted by OSCin slew rate, power, and frequency. If there is any way to better isolate the input path by doing something like enabling a doubler and dividing by two, then this can also can also help isolate this as the spur.

Cure

Optimize the input format, frequency, and power for the best spurs. Often the best results are when the OSCin signal is low amplitude but high slew rate. Sometimes also for devices, this spur is better if you enable the input doubler and divide by two. Isolation of the supply to the output buffer can sometimes be helpful in improving this spur.

f_{PD} Spurs

The phase detector spur has already been discussed. As the phase detector frequency is always much higher than the loop bandwidth, there is only an out-band version of this crosstalk spur.

f_{VCO} % f_{PD} Spurs

Description

These spurs occur at an offset of f_{VCO}% f_{PD}, especially in cases where the VCO is integrated on chip. There should be caution with diagnosing with this spur as there are several other spurs that can also occur at this offset, so some diagnosis is required. This spur can change for different VCO cores for an integrated VCO. For example, with a phase detector frequency and a VCO frequency of 5000.1 MHz, one would see these spurs at 5000 and 5000.2 MHz. If these were pure modulated spurs, theses should be both the same amplitude, but sometimes it can be the case that the spur at 5000 MHz would be higher amplitude because it is a direct harmonic of 100 MHz. Other times, the spurs are exactly the same.

Cause

This spur is caused by crosstalk between the f_{PD} and f_{VCO} signals.

Diagnosis

Change the phase detector frequency to isolate this spur from the f_{VCO}% f_{OSC} spur. Sometimes also, if you see that raising the phase detector frequency increases this spur, then this is a giveaway that it is this spur.

Cure

If the spur is on-chip, then sometimes reducing the phase detector frequency can help. This spur tends to be better for low amplitude, high slew rate OSCin signals. If the phase detector or charge pump has any programmable settings, sometimes this can help. Also better isolation of the charge pump supply pin can be helpful.

f_{OUT} % f_{PD} Spurs

For the sake of completeness, this spur is included in the descriptions, but the truth is that the mechanism of the phase detector frequency mixing with the output frequency is much less than other mechanisms that would cause a spur at this same offset.

f_{VCO} % f_{PD} Spur

This spur only occurs in fractional PLLs and will occur at the same offset as the integer boundary spur unless there is a pre-N divider in the loop.

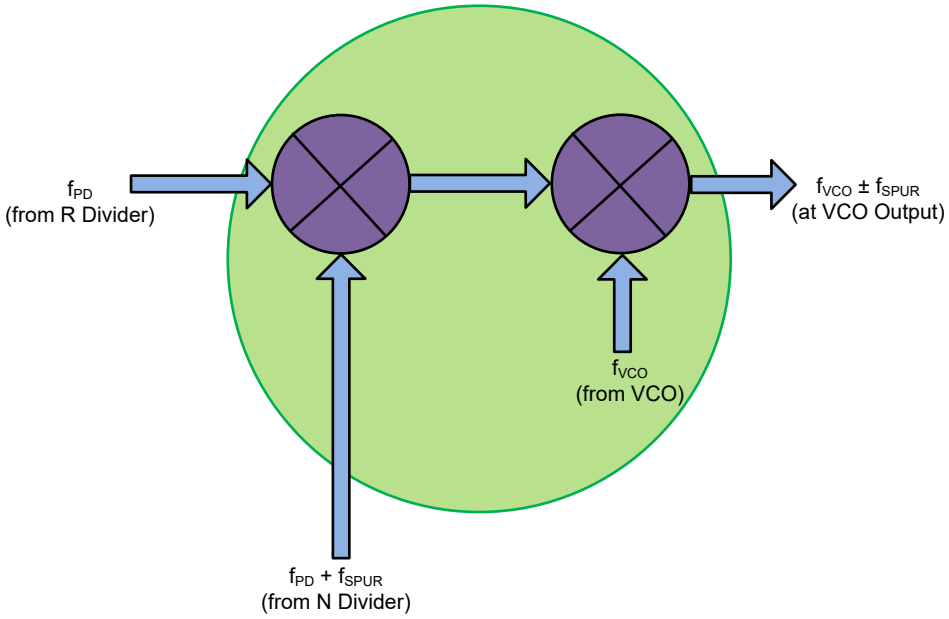


Figure 18.2 *Spur Coupling Mechanism or the f_{VCO} % f_{PD} Spur*

Conclusion

One common, but often ignored mechanism for spurs is crosstalk. This crosstalk is often between VCO and input, VCO and phase detector, or divided VCO frequency and input. The spurs produced by these mechanisms are often at the same offset as one would expect from fractional spurs, so it is good practice to be systematic in determining where these spurs come from so that they can be better mitigated.

Chapter 19 Phase Detector Spurs and their Causes

Introduction

Phase detector spurs occur at an offset from the carrier equal to the phase detector frequency (f_{PD}). The three mechanisms that generally cause this spur are charge pump leakage, charge pump on time (pulse), and crosstalk. Charge pump leakage occurs when the charge pump is intended to be off, but leakage introduces AC modulation on the VCO tuning line. Pulse effects are referring to time that the charge pump comes on and this can be impacted by other factors, such as charge pump mismatch. Crosstalk can come in many forms, but the one discussed in this chapter is that from the phase detector to the VCO that goes around the loop filter. This chapter discusses these three mechanisms and gives some models for them.

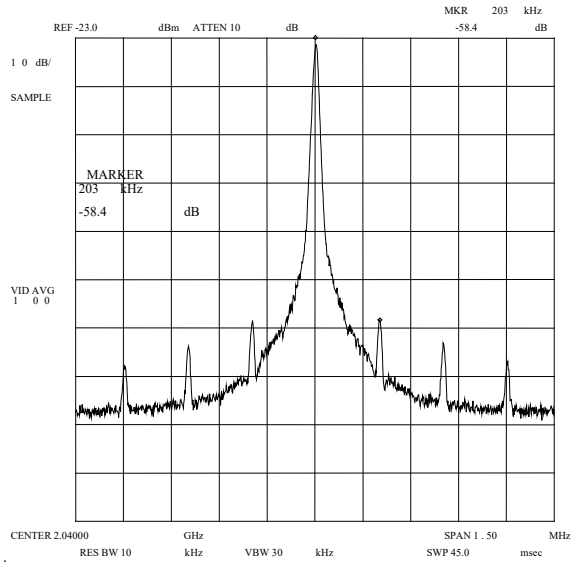


Figure 19.1 *Typical Phase Detector Spur Plot*

Understanding how Charge Pump Leakage Causes Spurs

When the PLL is in the locked condition, the charge pump will generate short correction currents with long periods in between in which the charge pump is supposed to be high impedance (tri-state). However, during the tri-state period there will be some parasitic leakage through the charge pump, VCO, and loop filter capacitors. Of these leakage sources, the charge pump is often, but not always, the dominant one. If the leakage is sufficiently large, it can cause the charge pump to only source current and can be modeled in the following figure. Theoretically, the on time of the charge pump will be such that the total charge delivered is equal to the total charge lost through leakage when the charge pump is supposed to be high impedance.

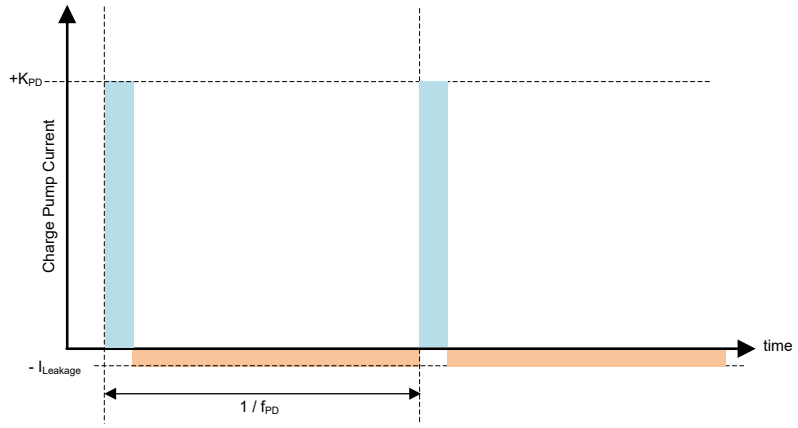


Figure 19.2 *Output of the Charge Pump in Locked Condition with High Leakage*

The leakage causes FM modulation on the VCO tuning line as shown in Figure 19.3.

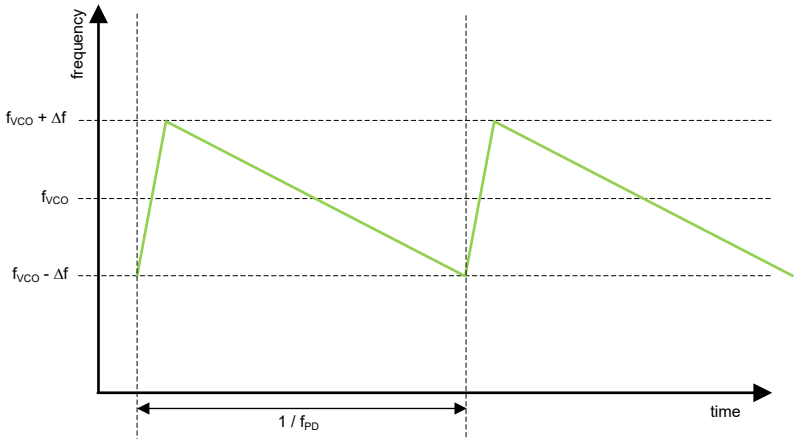


Figure 19.3 *Modulation on VCO Tuning Line Caused by Leakage Currents*

This modulation results in spurs that are at an offset of f_{PD} from the carrier and with an amplitude that is correlated to the magnitude of the leakage. To predict the phase detector spur levels based on leakage, use the following general rule that works for both the fundamental spur and its higher harmonics:

$$Leakage\ Spur\ =\ BaseLeakageSpur + \ 20 \cdot log\left|\frac{I_{Leakage}}{K_{PD}}\right| + \mathrm{SpurGain}(f_{PD}) \qquad \textbf{(19.1)}$$

BaseLeakageSpur is calculated in the appendix and is given by:

$$BaseLeakageSpur\ \approx 16.0 \qquad \textbf{(19.2)}$$

BaseLeakageSpur is a universal constant for any integer PLL and is not device specific. It is not measured directly, but rather it can be extrapolated from measured data. Appendix A goes in to greater detail as to how this model and constant were derived. $I_{Leakage}$ is the leakage current when the charge pump is supposed to be high impedance. This can be temperature dependent with a tendency to increase at higher temperatures and higher charge pump voltages, so spurs caused by leakage of the charge pump tend to increase when the PLL is heated. To demonstrate this model for leakage induced spurs matches reality, various leakage currents were induced at different phase detector frequencies and the first three harmonics of the phase detector spur was measured. This experiment was tried for three different loop filters. Although the phase detector frequencies, VCO frequencies, and measured spurs vary considerably, the BaseLeakageSpur is fairly consistent.

I_{leak} (nA)	20· Log ($I_{leakage}$ /K_{PD}) (dB)	f_{PD} (kHz)	Filter	Spur Levels (dBc)			Spur Gain (dB)			Implied BaseLeakage Spur (dBc)		
				1st	2nd	3rd	1st	2nd	3rd	1st	2nd	3rd
200	-86.0	50	A	-28.3	-40.5	-47.3	41.7	29.7	22.7	16.0	15.8	16.0
100	-92.0	50	A	-33.8	-45.7	-52.7	41.7	29.7	22.7	16.5	16.6	16.6
100	-80.0	100	B	-24.3	-40.5	-51.5	38.8	21.9	11.6	16.9	17.6	16.9
100	-80.0	200	B	-43.5	-61.5	-72.0	21.9	4.2	-6.3	14.6	14.3	14.3
500	-46.0	400	C	-32.7	X	X	-2.4	X	X	15.7	X	X
200	-54.0	400	C	-40.5	X	X	-2.4	X	X	15.9	X	X
Average Base Leakage spur										**15.9**	**16.1**	**16.0**

Filter	K_{PD} (mA)	K_{VCO} (MHz/V)	C1 (nF)	C2 (nF)	C3 (pF)	R2 (KΩ)	R3 (KΩ)	Output Frequency (MHz)
A	4.0	17	5.6	33	0	4.7	0	900
B	1.0	43	0.47	3.3	90	12	39	1960
C	0.1	48	1	4.7	0	18	0	870

Figure 19.4 *Spur Level vs. Leakage Currents and Phase detector frequency*

Impact of Capacitor Dielectric Absorption on the Phase Detector Spur

A somewhat rare phenomenon can occur when observing the phase detector frequency if the phase detector frequency is low and capacitors with poor dielectric properties are used. This phenomenon is characterized by a ghastly increase in the phase detector spurs right after switching frequencies. After the frequency is changed, it takes an excessively long time for the phase detector spurs to settle down. Assuming that it is not a measurement issue, such as using video averaging, this can be caused by an issue with capacitors called *dielectric absorption*, which causes capacitors to develop a residual charge, which can be modeled as excessive leakage. If this is the case, try using NP0 or film capacitors and often it will make this problem go away.

Pulse Related Spurs

In classical PLL literature, it is customary to model the phase detector spurs based entirely on leakage currents. For older PLLs, where the leakage currents were in the μA range, this made reasonable estimates for phase detector spurs and their behavior. However, modern PLLs typically have leakage currents in the range 1 nA, and therefore other factors tend to dominate the spurs, except at low phase detector frequencies.

Recall that the charge pump comes on for very short periods of time and then is off during most of the time. It is the length of time that these short charge pump corrections are made that determines the pulse related spur. In other words, if leakage is not the dominant factor, then it is this time that the charge pump is on that determines the spur levels. There are several factors that influence this correction pulse width which include dead-zone elimination circuitry, charge pump mismatches, and unequal transistor turn on times.

The dead zone elimination circuitry forces the charge pump to turn on in order to keep the phase detector out of the dead zone. It is this period that the charge pump is on that is the root cause of phase detector spurs when charge pump leakage is not a factor. Note that even though leakage is not the cause of pulse related spurs, it can have a small influence on this pulse width.

Mismatch and unequal turn on times of the charge pump transistors also have a large impact on this minimum turn on time for the charge pump. When the charge pump source and sink currents are not equal, they are said to have mismatch. For instance, if the source current were 10% higher than the sink current, then a rough rule of thumb would be that the charge pump would have to come on 10% longer than its minimum on time when sinking current, producing an overall increase in spur levels. The unequal turn on times of the sink and source transistors also can increase this charge pump on time. In general, the source transistor is a PMOS device, which has twice the turn on time as the sink transistor, which is an NMOS device. The net effect of this is that the effective source current is reduced, and this has a similar effect as having negative mismatch.

For pulse related spur issues, it is important to be aware of the mismatch properties and to base the design around several different parts to get an idea of the full variations. Mismatch properties of parts can vary from date code to date code, so it is important to consider that in the design process. Also, in designs where an op-amp is used in the loop filter, it is best to center the op-amp around half of the charge pump supply voltage or slightly higher. Due to this variation of spur level over tuning voltage to the VCO, the way that spurs are characterized in this chapter are by the worst-case spur when the VCO tuning voltage is varied from 0.5 volts to 0.5 volts below the charge pump supply. The variation can also be mentioned, since this shows how much the spur varies, but ultimately, the worst-case spur should be the figure of merit. To predict the k^{th} phase detector spur caused by the pulsing action of the charge pump, the following rule applies.

$$Pulse\ Spur = BasePulseSpur + 40 \cdot log\left|\frac{f_{Spur}}{1Hz}\right| + \mathrm{SpurGain}(f_{Spur}) + 20 \cdot \log(k) \qquad \textbf{(19.3)}$$

The reader may be surprised to see that the above formula has the additional f_{SPUR} term added. This was first discovered by making observations with a modulation domain analyzer, which displays frequency versus time. In the case of the leakage-dominated spur, the VCO frequency was assumed to be modulated in a sinusoidal manner, which was confirmed with observations on the bench. However, this was not the case for the pulse-dominated spur. For these, frequency spikes occur at regular intervals of time corresponding to when the charge pump turns on. The pulse-dominated spurs were measured and their magnitude could be directly correlated to the magnitude of these frequency spikes. This correlation was independent of the phase detector frequency. Therefore, using the modulation index concept does not work for pulse dominated spurs and introduces an error equal to $20 \cdot log(f_{Spur})$. The pulse spur differs from the leakage spur not by this factor but by $40 \cdot log(f_{Spur})$. The additional factor of $20 \cdot log(f_{Spur})$ comes because it is more proper to model the charge pump noise as a train of pulse functions, not a sinusoidal function. Recall to recover the time domain response of a pulse function applied to a system, this is simply the inverse Laplace transform. In a similar way that the inverse Laplace transform of ***1/s*** is just ***1***, and not involving any factors of ***1/ω***, likewise in this situation, a factor of ***1/ω*** is lost for this reason, thus accounting for the additional factor of $40 \cdot log(f_{Spur})$.

f_{VCO} *MHz*	***N***	f_{PD} kHz	K_{PD} *mA*	K_{VCO} *MHz/V*	***C1*** *nF*	***C2*** *nF*	***C3*** *pF*	***R2*** *KΩ*	***R3*** *KΩ*	**Spur** *dBc*	***Spur Gain*** *dB*	***BasePulse Spur*** *dBc*
This data was all taken from an LMX2330 PLL. The VCO was near the high end of the rail.												
1895	18950	100	4	43.2	2.2	10	0	6.8	0	-51.7	46	-297.7
1895	18950	100	4	43.2	13.9	66	0	2.7	0	-69.7	30	-299.7
1895	18950	100	4	43.2	0.56	2.7	0	15	0	-41.0	58	-299.0
1895	18950	100	4	43.2	1.5	6.8	0	5.6	0	-50.0	49.2	-299.2
1895	18950	100	4	43.2	1.5	6.8	100	5.6	39	-59.8	40.5	-300.3
1895	6064	312.5	4	43.2	4.7	20	0	1.8	0	-60.2	19.6	-299.6
1895	6064	312.5	4	43.2	1.8	5.6	0	1.5	0	-51.1	27.7	-298.6
This data was taken from an LMX2326 PLL with Vtune = 0.29 V and Vcc = 3 V												
231	1155	200	1	12	0.47	3.3	0	12	0	-74.1	23.0	-309.1
881.6	4408	200	1	18	0.47	3.3	0	12	0	-70.1	27.6	-309.7
881.6	1146	770	1	18	0.47	3.3	0	12	0	-70.1	4.9	-308.8
1885	9425	200	1	50	0.47	3.3	0	12	0	-59.7	35.6	-308.6
1885	4343	434	1	12	0.47	3.3	0	12	0	-58.7	22.2	-307.7

Table 19.1 *Demonstration of the Consistency of the BasePulseSpur*

The first seven rows in Table 19.1 demonstrate the consistency of BasePulseSpur over different loop filters and phase detector frequencies. The last five rows show consistency for many different VCO and phase detector frequencies. The tuning voltage was kept to maintain consistent mismatch properties of the charge pump and to also make spurs that were easy to measure. Although this table demonstrates the consistency of BasePulseSpur, the actual value for this is worse than typical as the tuning voltage was forced near the supply rail to emphasize this spur mechanism.

As for the consistency of *BasePulseSpur* with harmonics of pulse dominated spurs, a LMX2326 PLL was tuned in 1 MHz increments from 1900 MHz to 1994 MHz using an automated test program. For these tests, K_{PD}= 1 mA, f_{PD}= 200 kHz, and K_{VCO} = 45 MHz/V. Filter A had components of ***C1*** = 145 pF, ***C2*** = 680 pF, ***R2*** = 33 KΩ, while Filter B had components of ***C1*** = 315 pF, ***C2*** = 1.8 nF, and ***R2*** = 18 KΩ.

	Fundamental (200 kHz)	**2nd Harmonic (400 kHz)**	**3rd Harmonic (600 kHz)**
Minimum (dBc)	-56.2	-65.1	-64.5
Average (dBc)	-52.8	-58.5	-61.9
Maximum (dBc)	-49.3	-54.4	-59.0
Spur Gain for Spur (dB)	45.7	33.8	26.8
20·log(k)	0	6	9.5
BasePulseSpur (dBc)	-307.0	-306.4	-307.4

Table 19.2 *Phase Detector Spurs and their Harmonics for Filter A*

	Fundamental (200 kHz)	**2nd Harmonic (400 kHz)**	**3rd Harmonic (600 kHz)**
Minimum (dBc)	-64.8	-70.4	-69.1
Average (dBc)	-60.8	-65.1	-66.8
Maximum (dBc)	-56.2	-61.1	-64.7
Spur Gain for Spur (dB)	39.0	27.1	20.0
20·log(k)	0	6	9.5
BasePulseSpur (dBc)	-307.2	-306.2	-306.3

Table 19.3 *Phase Detector Spurs and their Harmonics for Filter B*

BasePulseSpur for Various PLLs

PLL	**BasePulseSpur (dBc)**
LMX2301/05, LMX2315/20/25	-299
LMX2330/31/32/35/36/37	-311
LMX2306/16/26	-309
LMX1600/01/02	-292
LMX2470/71, LMX2430/33/34, LMX2485/86/87	-331
LMX2581,LMX2571, LMX2492	-343

Table 19.4 *BasePulseSpur for Various Texas Instruments PLLs*

Impact of Mismatch on BasePulseSpur

The avid reader may inquire about the impact of charge pump mismatch on BasePulseSpur. This can be device specific and related to the turn on times of the transistors in the charge pump. However, one interesting fact is that the unequal turn on times of the transistors may cause it such that ideal mismatch is greater than 0%. To illustrate this, the LMX2315 PLL was used, and the spur level was measured along with the charge pump mismatch. The spur gain of this system was 19.6 dB, and in this system the phase detector frequency was 200 kHz, so the spurs are clearly pulse-dominated. Note that the turn-on time of the charge pump transistors also comes into play, so this result is specific to the LMX2315 family of PLLs. For this PLL, it seems that the optimal spur levels occur around +4% mismatch instead of 0% mismatch due to these unequal transistor turn on times.

Vtune (Volts)	1	1.5	2.2	3	4	4.5
Source (mA)	5.099	5.169	5.241	5.308	5.397	5.455
Sink (mA)	5.308	5.253	5.166	5.047	4.828	4.517
mismatch (%)	- 4.0	- 1.6	1.4	5.0	11.1	18.8
200 kHz Spur (dBc)	- 73.1	- 76.6	- 83.3	- 83.2	- 72.8	- 65.7

Table 19.5 *Sample Variation of Spur Levels and Mismatch with Charge Pump Voltage*

Using statistical models, this suggests that the best spur performance is actually when the charge pump is 3.2 % mismatched and also gives the relationship for this device as:

$$BasePulseSpur_{LMX2315} = -315.6 + 1.28 \cdot |\%mismatch - 3.2\%| \quad \textbf{(19.4)}$$

Combining the Concepts of Leakage Related Spurs and Pulse Related Spurs

Critical Values for Phase Detector Frequency

At lower phase detector frequencies, the leakage spur dominates over the pulse spur, but eventually it is the other way around. It may be of interest to some to know the phase detector frequency where these are both equal. By calculating the spurs with both methods and setting this equal, this critical phase detector frequency can be found to satisfy the following equation.

$$40 \cdot log\left(\frac{f_{PD}}{1\ Hz}\right) = (BaseLeakageSpur - BasePulseSpur) + 20 \cdot log\left|\frac{I_{Leakage}}{K_{PD}}\right| \quad \textbf{(19.5)}$$

Assuming a charge pump gain of 1 mA and a ***BaseLeakageSpur*** of 16.0 dBc the following table can be calculated. Note that the critical frequency is proportional to the square root of the leakage current, and inversely proportional to the square root of the charge pump gain.

		BasePulseSpur (dBc)						
		-290	**-300**	**-310**	**-320**	**-330**	**-340**	**-350**
$I_{Leakage}$ (nA)	**0.1**	14.1	25.1	44.7	79.4	141.3	251.2	446.7
	1.0	44.7	79.4	141.3	251.2	446.7	794.3	1412.5
	10.0	141.3	251.2	446.7	794.3	1412.5	2511.9	4466.8
	100.0	446.7	794.3	1412.5	2511.9	4466.8	7943.3	14125.4
	1000.0	1412.5	2511.9	4466.8	7943.3	14125.4	25118.9	44668.4

Table 19.6 *Critical Values for Phase Detector Frequency in Kilohertz*

Spur Levels vs. Unoptimized Loop Filter Parameters

Table 19.7 showing how various parameters impact leakage and pulse dominated spurs.

Parameter	Description	Leakage Dominated Spurs	Pulse Dominated Spurs
$I_{Leakage}$	*Charge Pump Leakage*	$20 \cdot log\lvert I_{Leakage}\rvert$	*N/A*
mismatch	*Charge Pump Mismatch*	*N/A*	*Correlated to | mismatch - Constant |*
N	*N Counter Value*	*independent*	*independent*
K_{VCO}	*VCO Gain*	$20 \cdot log(K_{VCO})$	$20 \cdot log(K_{VCO})$
f_{PD}	*Phase Detector Frequency*	$-40 \cdot log(f_{PD})$	$-20 \cdot log(f_{PD})$
r	$r = f_{PD}/BW$	$-40 \cdot log(r)$	$-40 \cdot log(r) + 20 \cdot log(f_{PD})$
K_{PD}	*Charge Pump Gain,*	*independent*	$20 \cdot log(K_{PD})$
SG	*Spur Gain*	*SG*	*SG*

Table 19.7 *Spur Levels vs. Parameters if Loop Filter is NOT Redesigned*

f_{PD} Crosstalk Spurs

Modeling of the f_{PD} Crosstalk Spur

Aside from being caused by leakage currents and the pulsed on time of the charge pump, phase detector spurs can also be the result of crosstalk to the VCO. This crosstalk can be the result of spur energy coupling to the power supply of the VCO or from the high frequency input of the PLL to the VCO output. The phase detector frequency is much higher than the loop bandwidth, so loop filter impact is negligible. This spur is typically fairly constant, but can change somewhat with the phase detector frequency. For instance, board bypassing may attenuate this spur energy for higher phase detector frequencies. However, crosstalk can often be more severe at higher frequencies. This makes theoretical sense if one thinks of parallel traces as having a parasitic capacitance between them and therefore the impedance would be less at higher frequencies. The crosstalk can have an increasing tendency with phase detector frequency for a while, and then decrease at even higher phase detector frequencies. In any case, this is part specific. In addition to this, the crosstalk spur can be impacted by the OSCin slew rate as well as other real world effects.

f_{PD} Crosstalk Spurs with Devices with Integrated VCOs

When VCO is integrated with the PLL, there can be crosstalk on-chip. Often times this will be lower for smaller phase detector frequencies and increase 6 dB/decade with the phase detector frequency to some point and then stabilize, or then even start to go down. These spurs can be impacted by the layout and power supply decoupling so modeling of them tends to be part-specific and complicated.

f_{PD} Crosstalk Spurs with Devices with External VCOs

These spurs can also occur when the VCO is a not integrated with the PLL. This can happen when the charge pump supply pin pollutes the power supply or ground plane and this gets to the VCO, or it can be the result of spur energy going to the PLL high frequency input pin and then leaking back to the VCO. In this case that it is coming from the charge pump supply, reducing the charge pump current can often help this spur. This also reduces the loop bandwidth, which will reduce the f_{PD} spur due to leakage and pulsed charge pump output. For these reason, one should be careful not to get the crosstalk spur mechanism confused with these other mechanisms when changing the charge pump current. In the case that the spur is leaking through the high frequency input pin, more isolation such as buffering or resistive pads can sometimes improve this spur.

Conclusion

This chapter has discussed the causes of phase detector spurs and given some techniques to simulate their general behavior. Phase Detector spurs can be caused by leakage, pulse, or crosstalk effects. The total phase detector spur is therefore the sum of the spur from all three of these effects. In other words:

$$PhaseDetectorSpur = 10 \cdot log\left[10^{(LeakageSpur/10)} + 10^{(PulseSpur/10)} + 10^{(CrosstalkSpur/10)}\right] \quad \textbf{(19.6)}$$

As for the accuracy of the formulas presented in this chapter, there will always be some variation between the actual measured result and the theoretical results. Relative comparisons using spur gain tend to be the most accurate. It is recommended to use the empirical value, but to accept that there could be several dB variation between the predicted and measured results. In the case of pulse-dominated spurs, the value for *BasePulseSpur* is purely empirical and is based solely on measured data. These spurs can also change a good 15 dB as the VCO is tuned across its tuning range. The spur metrics presented in this chapter are for the worst case tuning voltage. As for modeling of the phase detector spur due to crosstalk, this has much less to do with PLL theory and more with just having empirical measurements.

Appendix A: Theoretical Calculation of Leakage Based Spurs

The charge pump comes on for a very short period of time to charge the loop filter, and then the leakage occurs over a long period. For practical purposes of modeling this spur, this on time can be assumed to be instantaneous and the FM modulation produced by the leakage can be modeled as a sawtooth waveform as shown.

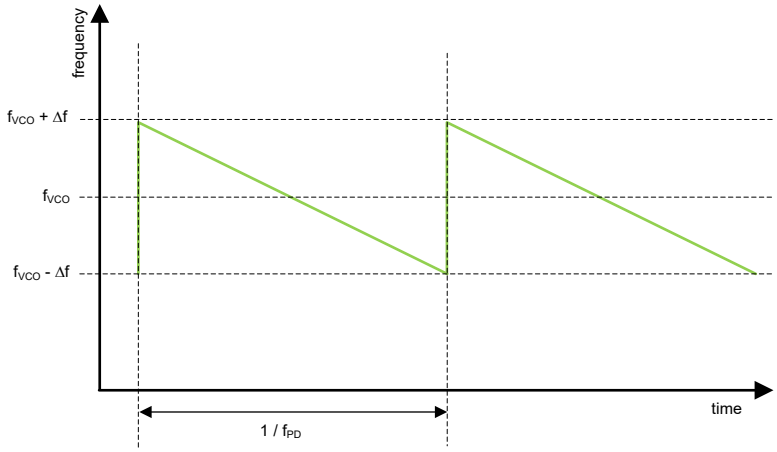


Figure 19.5 *VCO Frequency Output*

The spurs can be modeled by writing a Fourier series for this sawtooth wave.

$$f(t) = f_{VCO} + \Delta f \cdot \sum_{n=1}^{\infty} \frac{sin[2\pi \cdot f_{PD} \cdot k \cdot t]}{k \cdot \pi} = f_{Min} + \sum_{n=1}^{\infty} f_{DEV}(k) \cdot sin[2\pi \cdot f_{MOD}(k) \cdot t] \qquad \textbf{(19.7)}$$

The next task is to figure out the frequency deviation, f_{DEV}, and modulation index, f_{MOD}. The modulation frequency for the nth phase detector spur is given by:

$$f_{MOD}(k) = k \cdot f_{PD} \qquad \textbf{(19.8)}$$

To find the frequency deviation, $f_{DEV}(k)$, some calculations are needed. Since the *BaseLeakageSpur* is theoretically independent of PLL and loop filter, it makes sense to choose the loop filter that is the most basic. A simple capacitor is the most basic loop filter. Although this filter topology is not stable, it is sufficient for the purposes of calculations. Using this simplified loop filter, the voltage deviation to the VCO can easily be calculated. Substituting in known values gives the voltage deviation over one phase detector cycle:

$$\Delta V = \int_0^{1/f_{PD}} \frac{leakage}{C1} \cdot dt = \frac{leakage}{C1 \cdot f_{PD}} \qquad \textbf{(19.9)}$$

The frequency deviation can be found by taking the Fourier series coefficient and multiplying it by the deviation from center frequency, which is half of the total frequency deviation.

$$f_{DEV}(k) = \frac{\Delta f}{2 \cdot k \cdot \pi} = \frac{K_{VCO}}{2 \cdot k \cdot \pi} \cdot \int_0^{1/f_{PD}} \frac{leakage}{C1} \cdot dt = \frac{K_{VCO} \cdot leakage}{2 \cdot k \cdot C1 \cdot f_{PD}} \quad \textbf{(19.10)}$$

The modulation index for the k[th] term in the Fourier series can now be calculated as follows.

$$\beta(k) = \frac{f_{DEV}(k)}{f_{MOD}(k)} = \frac{K_{VCO} \cdot leakage}{2 \cdot C1 \cdot k^2 \cdot {f_{PD}}^2} \quad \textbf{(19.11)}$$

The k[th] leakage spur can now be calculated from the modulation index.

$$LeakageSpur = 20 \cdot log\left(\frac{\beta(k)}{2}\right) = 20 \cdot log\left(\frac{K_{VCO} \cdot leakage}{2 \cdot C1 \cdot k^2 \cdot {f_{PD}}^2}\right) \quad \textbf{(19.12)}$$

Now that the leakage spur is known for this specific case, we next need to calculate the spur gain. For this, we assume the spur is far outside the loop bandwidth. This implies that the spur gain can be approximated with the open loop gain.

$$SpurGain \approx 20 \cdot log\|G(2\pi \cdot j \cdot f_{PD} \cdot k)\| = 20 \cdot log\left|\frac{K_{PD} \cdot K_{VCO}}{4\pi^2 \cdot {f_{PD}}^2 \cdot k^2 \cdot C1}\right| \quad \textbf{(19.13)}$$

The next step is to calculate the BaseLeakageSpur by subtracting (19.13) from (19.12).

$$BaseLeakageSpur = LeakageSpur - SpurGain - 20 \cdot log\left|\frac{leakage}{K_{PD}}\right|$$

$$= 20 \cdot log\left(\frac{K_{VCO} \cdot leakage}{2 \cdot C1 \cdot k^2 \cdot \pi \cdot {f_{PD}}^2} \cdot \frac{4 \cdot \pi^2 \cdot {f_{PD}}^2 \cdot k^2 \cdot C1}{K_{PD} \cdot K_{VCO}} \cdot \frac{K_{PD}}{leakage}\right) \quad \textbf{(19.14)}$$

$$= 20 \cdot log(2\pi) \approx 16.0$$

Appendix B: Derivation for BasePulseSpur

To calculate this index, first start with the filter that is easiest to model that has the key necessary properties as shown below.

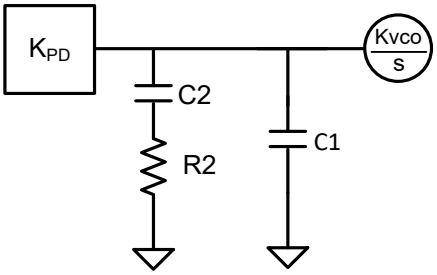


Figure 19.6 *Filter for BasePulseSpur Calculation*

For the purposes of calculating the BasePulseSpur, the steady state tuning voltage can be defined to be zero volts without any loss of generality. Although the pulses may have a different alternating pattern, the tuning voltage as presented to the VCO would look something like as follows:

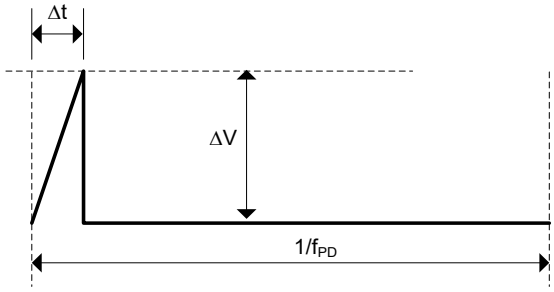


Figure 19.7 *VCO Tuning Voltage, V(t), Modeling of the BasePulseSpur*

To estimate ΔV and Δt, consider the charge pump starting at high impedance and the step response current of amplitude K_{PD}. This step response can be calculated and expressed in terms of filter time constants T1 and T2 as follows:

$$V(t) = \frac{K_{PD}}{C1 + C2} \cdot \left[t + (T2 - T1) \cdot \left(1 - e^{-t/T1}\right)\right] \qquad \textbf{(19.15)}$$

Recall the following Taylor series expansion.

$$e^{x} = 1 + \mathrm{x} + \cdots \qquad \textbf{(19.16)}$$

If it is assumed that the time period is small, then (19.15) can be approximated as follows:

$$V(t) \approx \frac{K_{PD} \cdot T2}{(C1 + C2) \cdot T1} \cdot t \tag{19.17}$$

Assuming the pattern to be repeating, the coefficients in the complex Fourier series for the k^{th} harmonic are as follows

$$c_k = \frac{1}{1/f_{PD}} \cdot \int_0^{\Delta t} K_{VCO} \cdot V(t) \cdot e^{j \cdot k \cdot f_{PD} \cdot t} \tag{19.18}$$

Use the first term of the Taylor series expansion.

$$e^x = 1 + \mathrm{x} + \cdots \approx 1 \tag{19.19}$$

This simplifies to the following.

$$c_k = f_{PD} \cdot \int_0^{\Delta t} K_{VCO} \cdot \left[\frac{K_{PD} \cdot T2}{(C1 + C2) \cdot T1} \cdot t\right] \cdot (1) \approx \frac{f_{PD} \cdot K_{PD} \cdot K_{VCO} \cdot T2 \cdot \Delta t^2}{2 \cdot (C1 + C2) \cdot T1} \tag{19.20}$$

The modulation index as defined as the frequency deviation divided by the modulation frequency

$$\beta(k) = \frac{c_k}{k \cdot f_{PD}} = \frac{K_{PD} \cdot K_{VCO} \cdot T2 \cdot \Delta t^2}{2 \cdot k \cdot (C1 + C2) \cdot T1} \tag{19.21}$$

Now calculate the gain of the loop at the frequency of interest.

$$\begin{aligned} SpurGain(k \cdot f_{PD}) &\approx 20 \cdot log\|G(2\pi \cdot j \cdot f_{PD} \cdot k)\| \\ &= 20 \cdot log\left|\frac{K_{PD} \cdot K_{VCO} \cdot (1 + 2\pi \cdot k \cdot f_{PD} \cdot T2)}{4 \cdot \pi^2 \cdot k^2 \cdot {f_{PD}}^2 \cdot (C1 + C2) \cdot (1 + 2\pi \cdot k \cdot f_{PD} \cdot T1)}\right| \\ &\approx 20 \cdot log\left|\frac{K_{PD} \cdot K_{VCO} \cdot T2}{4 \cdot \pi^2 \cdot k^2 \cdot {f_{PD}}^2 \cdot (C1 + C2) \cdot T1}\right| \end{aligned} \tag{19.22}$$

To justify the last approximation, the phase detector frequency would have to be much farther out than 1/T2 for stability, and can be assumed without loss of generality to be much larger than 1/T1.

Now that both the spur gain and spur are known, subtract away the spur gain to derive the index for BasePulseSpur.

$$
\begin{aligned}
BasePulseSpur &= 20 \cdot log\left(\frac{\beta(k)}{2}\right) - \text{SpurGain}(f_{PD} \cdot k) \\
&= 20 \cdot \log\left(\frac{K_{PD} \cdot K_{VCO} \cdot T2 \cdot \Delta t^2}{2 \cdot 2 \cdot k \cdot (C1 + C2) \cdot T1}\right) - 20 \cdot \log\left(\frac{K_{PD} \cdot K_{VCO} \cdot T2}{4 \cdot \pi^2 \cdot k^2 \cdot {f_{PD}}^2 \cdot (C1 + C2) \cdot T1}\right) \\
&= 20 \cdot \log\left(\frac{K_{PD} \cdot K_{VCO} \cdot T2 \cdot \Delta t^2}{2 \cdot 2 \cdot k \cdot (C1 + C2) \cdot T1} \cdot \frac{4 \cdot \pi^2 \cdot k^2 \cdot {f_{PD}}^2 \cdot (C1 + C2) \cdot T1}{K_{PD} \cdot K_{VCO} \cdot T2}\right) \\
&= 20 \cdot \log\left(\pi^2 \cdot \Delta t^2 \cdot k \cdot {f_{PD}}^2\right)
\end{aligned}
\qquad \textbf{(19.23)}
$$

This can be simplified to the following rule.

$$
BasePulseSpur(k) = 40 \cdot \log(\pi \cdot \Delta t) - 40 \cdot \log(f_{PD}) - 20 \cdot \log(k) \qquad \textbf{(19.24)}
$$

This not only demonstrates the concept for *BasePulseSpur*, but also shows that it implies a charge pump pulse width. For the first harmonic of the phase detector frequency (k=1), here is a table of some commonly measured values for *BasePulseSpur* and the implied Pulse width.

PLL	BasePulseSpur (dBc)	Implied Pulse Width (ns)
LMX2301/05, LMX2315/20/25	-299	10.7
LMX2330/31/32/35/36/37	-311	5.3
LMX2306/16/26	-309	6.0
LMX1600/01/02	-292	16.0
LMX2470/71, LMX2430/33/34, LMX2485/86/87	-331	1.7
LMX2581,LMX2571, LMX2492	-343	0.8

Table 19.8 *BasePulseSpur and Implied Pulse Width*

Appendix C: Impact of Discrete Sampling Effects on Spurs

In situations where the loop bandwidth is wide relative to the phase detector frequency, it is possible in for a cusping effect near the phase detector spurs. In this case, the continuous time approximation gets stretched and some of the discrete sampling effects of the phase detector can be seen in the frequency domain. Near the phase detector frequency, which is the sampling frequency, there will be a "cusping" effect on the spurs as shown in the following figure.

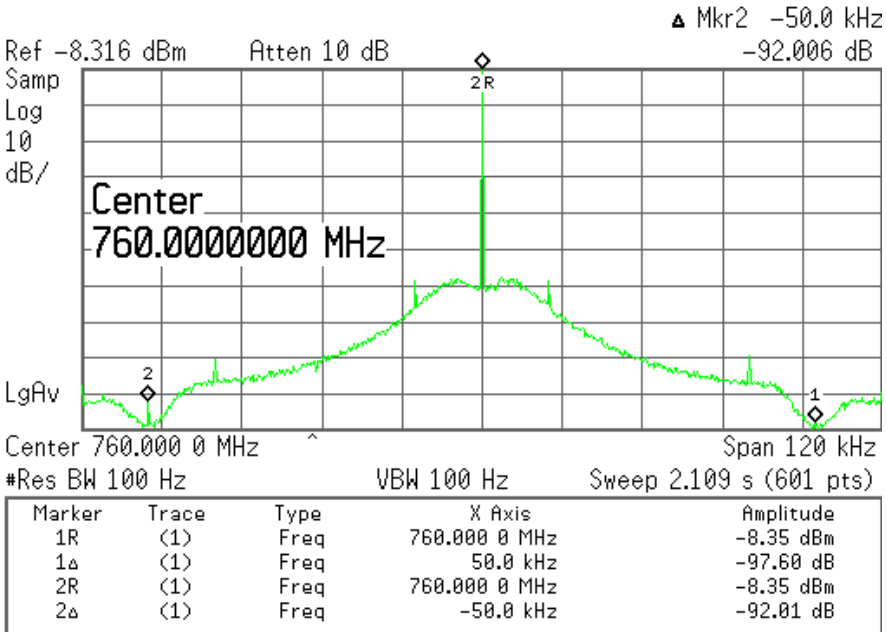


Figure 19.8 *Discrete Sampling Effects causing Cusping of Phase Detector Spur*

Chapter 20 Fundamentals of Fractional Spurs

Introduction

Perhaps one of the greatest fears of using fractional PLLs is the fractional spurs. Understanding of these spurs can be complicated as they can be impacted by the loop filter, PLL fraction, modulator order, dithering, initial modulator state, phase detector frequency, OSCin power level/format, VCO Core, and potentially many other factors. Trying to tackle all of these factors simultaneously leads to a garbled misunderstanding of fractional spurs that overlooks the fundamental patterns. To break through this complexity, the first step is to begin with the simplest case of the first order modulator to understand the fundamental rules and leave the more complicated delta sigma modulators to a later chapter. This chapter begins by establishing some fundamental properties of the first order modulator in order to create a foundation for understanding fractional spurs.

The Fundamental Properties of the First Order Fractional Modulator

Introduction

The fractional PLL has a fraction expressed in the form Fnum/Fden as shown in the following figure:

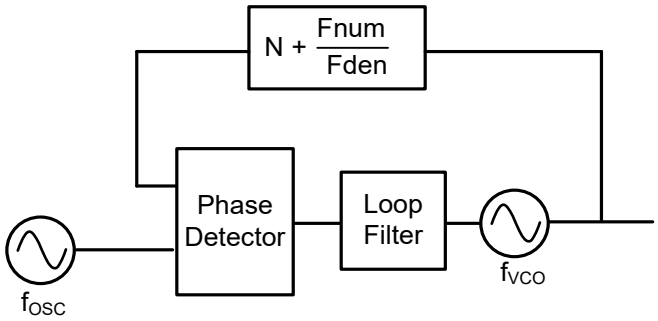


Figure 20.1 *Fractional PLL*

For the first order modulator, there are some fundamental properties that generally hold true that will be discussed throughout the chapter.

- Equivalent Fractions
- Symmetric Fractions
- Initial State Independence
- Fractional Spur Offsets
- Integer Boundary Spurs
- Phase Detector Nulls

The first four will be discussed immediately and then the last two will be discussed after it is shown how to calculate fractional spurs.

Equivalent Fraction Property for the First Order Modulator

The equivalent fraction property says that if two fractions are equivalent, then they theoretically have the same spurs. For instance, ¼, 10/40, and 1000000/4000000 all should have the same spurs. This also means that the fraction of *Fnum/Fden* can assumed to be a lowest terms fraction without loss of generality.

Symmetric Fraction Property for the First Order Modulator

The symmetric fraction property states that *Fnum/Fden* and (*Fden-Fnum)/Fden* theoretically have the same spurs. For example 3/100 and 97/100 theoretically have the same spurs.

Initial State Independence Property for the First Order Modulator

The initial state property states that the initial state of the accumulator, also called the *seed*, has no impact on the spurs. It is assumed that the seed can assume any value from 0 to *Fden-1*. For higher order modulators, a non-zero seed can actually impact the spurs in some cases. Nevertheless, it is good to be aware of this property and be aware of the seed.

In most cases, the seed is zero, but a non-zero seed can be introduced either unintentionally or intentionally. Unintentional ways it can be introduced is for devices that do not reset the modulator. For instance, this might be when the device is powered of and on or changing the N divider values. A non-zero seed can also be intentionally introduced for some devices if one wants to use it to create a phase shift from input to output.

Primary Fractional Spur Occurrence for the First Order Modulator

Assuming that *Fnum* and *Fden* are relatively prime, fractional spurs will occur at offsets of:

$$f_{Spur}(k) = \frac{k}{f_{PD} \cdot Fden} \quad , \quad \mathrm{k} = 1,2,3, \ldots \mathrm{Fden} - 1 \qquad \textbf{(20.1)}$$

For instance, a fraction of 93/100 with a 10 MHz phase detector has spurs that occur in increments of 100 kHz. For higher order modulators, there can be additional fractional spurs, but the primary fractional spurs often tend to be the strongest.

The *integer boundary spur* is perhaps the most feared among fractional spurs and occurs at an offset equal to the distance to the closest integer channel. For instance, with a fraction of 93/100, the integer boundary spur would be at an offset of 700 kHz. Among the fractional channels, the worst case channels are usually the ones just slightly offset from the integer values because the integer boundary spur is closer and stronger. For the fractional denominator of 100, the worst case fractions would be 1/100 and 99/100. The frequencies corresponding to these worst case fractions are called *integer boundary channels*.

Calculation of Fractional Spurs from the Fractional Engine

Calculation of Spurs by Fourier series

To model the spurs, the simplest approach is to consider a PLL with an infinite loop bandwidth and look at the mathematical sequence produced by the modulator and disregard the discrete sampling action of the phase detector and any sort of fractional compensation. In this case the PLL frequency will be modulated between two frequencies with a clock period that is equal to the phase detector period, $1/f_{PD}$. The total period of this modulation will repeat every Fden cycles. The spurs are considered *InBand* spurs because they are inside the loop bandwidth; if they were outside the loop bandwidth that the loop filter would attenuate them. In other words:

$$Spur = InBandSpur + rolloff \tag{20.2}$$

For example, consider the fraction of 3/10 with a phase detector frequency of 1 MHz. This has a sequence of 0,0,0,1,0,0,1,0,0,1,… (repeats) and has a frequency response shown in the following figure.

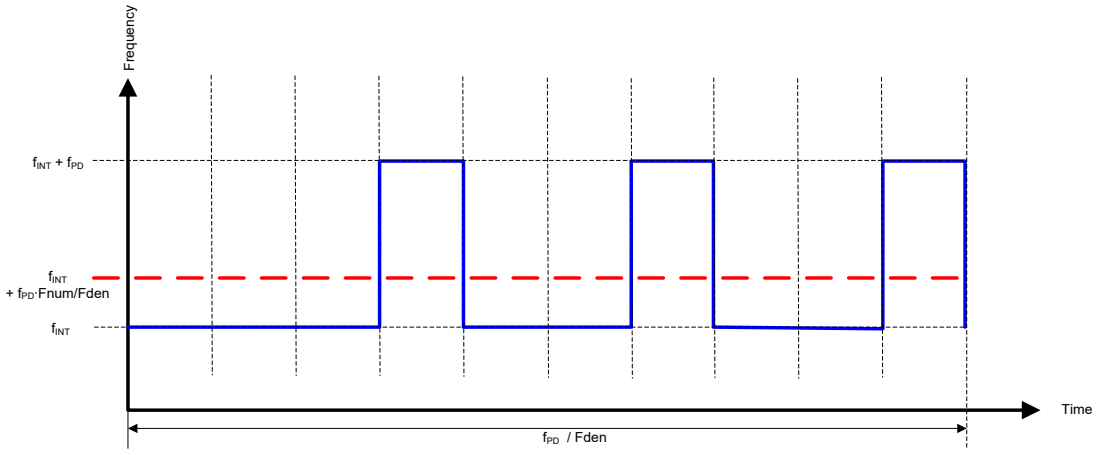


Figure 20.2 *Fractional PLL Output for Infinite Loop Bandwidth for a Fraction of 3/10*

The output of the VCO can be expressed as follows:

$$f(t) = sin[(f_{INT} + f_{PD} \cdot m(t)) \cdot t] \tag{20.3}$$

m(t) is the modulating signal which has a value of 0 or 1 which is periodic over the interval 0 to $1/(Fden \cdot f_{PD})$. Consider the example the fraction 3/10 and with a phase detector frequency of 1 MHz. The waveform has a repeating period of 10 us and has the following equation over that interval.

$$m(t) = \begin{cases} 0 & 0\ \mu s \le t < 3\ \mu s, 4\ \mu s \le t < 6\ \mu s, 7\ \mu s \le t < 9\ \mu s \\ 1 & 3\ \mu s \le t < 4\ \mu s, 6\ \mu s \le t < 7\ \mu s, 9\ \mu s \le t < 10\ \mu s \end{cases} \quad \textbf{(20.4)}$$

$$m(t) = \frac{3}{10} + \sum_{n=1}^{\infty} a_n \cdot \cos\left(\frac{n \cdot \pi \cdot t}{L}\right) + b_n \cdot \sin\left(\frac{n \cdot \pi \cdot t}{L}\right) \quad \textbf{(20.5)}$$

$$a_n = \frac{2}{L} \cdot \int_0^L \cos\left(\frac{n \cdot \pi \cdot t}{L}\right) \cdot dt \quad \textbf{(20.6)}$$

$$b_n = \frac{2}{L} \cdot \int_0^L \sin\left(\frac{n \cdot \pi \cdot t}{L}\right) \cdot dt \quad \textbf{(20.7)}$$

$$L = \frac{10}{f_{PD}} = 10\ \mu s \quad \textbf{(20.8)}$$

The modulation index for the n[th] fractional spur can be calculated as:

$$\beta = \frac{f_{DEV}}{f_{Spur}} = \frac{f_{PD} \cdot \sqrt{(a_n)^2 + (b_n)^2}}{\left({}^{n}/_{L}\right)} \quad \textbf{(20.9)}$$

The first 10 fractional spurs can be calculated as follows:

n	f_{Spur}	a_n	b_n	β	*Spur*
1	100 kHz	-0.44	-0.61	0.75	-8.50
2	200 kHz	0.36	-1.10	0.58	-10.78
3	300 kHz	4.27	-1.39	1.50	-2.51
4	400 kHz	-1.98	-1.44	0.61	-10.28
5	500 kHz	0.00	-1.27	0.25	-17.90
6	600 kHz	1.32	-0.96	0.27	-17.33
7	700 kHz	-1.83	-0.60	0.28	-17.23
8	800 kHz	-0.09	-0.27	0.04	-34.86
9	900 kHz	0.05	-0.07	0.01	-46.67
10	1 MHz	0	0	0	None

Table 20.1 *Table of Fractional Spurs for a Fraction of 3/10*

This exercise can be expanded for all of the fractional numerators with the denominator of 10 to produce the following table:

		Fraction								
		1/10	2/10	3/10	4/10	5/10	6/10	7/10	8/10	9/10
Offset	1 MHz	-0.1		-8.5				-8.5		-0.1
	2 MHz	-6.6	-0.6	-10.8	-4.8		-4.8	-10.8	-0.6	-6.6
	3 MHz	-10.9		-2.5				-2.5		-10.9
	4 MHz	-14.5	-8.4	-10.3	-4.3		-4.3	-10.3	-8.4	-14.5
	5 MHz	-17.9		-17.9		-3.9		-17.9		-17.9
	6 MHz	-21.5	-15.5	-17.3	-11.3		-11.3	-17.3	-15.5	-21.5
	7 MHz	-25.6		-17.2				-17.2		-25.6
	8 MHz	-30.7	-24.7	-34.9	-28.8		-28.8	-34.9	-24.7	-30.7
	9 MHz	-38.3		-46.7				-46.7		-38.3
	10 MHz									

Table 20.2 *Spurs for a Fractional Denominator of 10 and f_{PD}= 10 MHz*

Phase Detector Null Property

For Table 20.2, note that none of the fractions produce a spur at the 10 MHz phase detector frequency. This is generally true for all fractional PLLs and it is also true that there will be no spurs at any multiples of the 10 MHz phase detector frequency. To reason why this is true, consider the waveform that the fractional spur produces as illustrated in Figure 20.2. The modulator changes the output divide every phase detector period. For the coefficients, we are always integrating over some multiple of the phase detector period and multiplying by sines and cosines, which have a net zero value over a phase detector period. This implies that all spurs at multiples of the phase detector frequency due the fractional engine will be not present. However, traditional phase detector spurs will be present due to other mechanisms.

In-Band Fractional Spur Tables for the First Order Modulator

The same method used in the previous example can be used to calculate in-band fractional spurs for any fraction. Table 20.3 shows simulations that for all spurs for fractional numerator and denominator up to 20. This table is condensed to just show the necessary values. For instance, a fraction of 5/10 can be expressed as ½ and a fraction if 13/17 is the same as 4/17.

Fden	Fnum	Spur Order																		
		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
2	1	-3.9																		
3	1	-1.6	-13.7																	
4	1	-0.9	-9.9	-20.0																
5	1	-0.6	-8.4	-15.5	-24.7															
	2	-4.8	-4.3	-11.3	-28.8															
6	1	-0.4	-7.7	-13.5	-19.7	-28.4														
7	1	-0.3	-7.2	-12.3	-17.3	-23.1	-31.4													
	2	-7.3	-2.1	-10.4	-15.4	-18.0	-38.5													
	3	-5.4	-9.1	-5.3	-10.3	-25.1	-36.5													
8	1	-0.2	-6.9	-11.7	-16.0	-20.5	-26.0	-34.0												
	3	-7.9	-6.9	-4.0	-16.0	-12.9	-26.0	-41.7												
9	1	-0.2	-6.7	-11.2	-15.1	-18.9	-23.2	-28.5	-36.3											
	2	-9.4	-1.3	-11.2	-11.4	-15.2	-23.2	-23.0	-45.5											
	4	-5.7	-10.4	-11.2	-5.9	-9.8	-23.2	-32.2	-41.8											
10	1	-0.1	-6.6	-10.9	-14.5	-17.9	-21.5	-25.6	-30.7	-38.3										
	3	-8.5	-10.8	-2.5	-10.3	-17.9	-17.3	-17.2	-34.9	-46.7										
11	1	-0.1	-6.5	-10.6	-14.0	-17.2	-20.3	-23.7	-27.7	-32.6	-40.1									
	2	-11.0	-0.8	-12.2	-9.5	-14.8	-18.0	-19.2	-29.3	-27.0	-51.0									
	3	-10.3	-9.4	-2.1	-14.8	-11.9	-15.1	-24.5	-19.1	-35.5	-50.3									
	4	-8.7	-11.8	-7.7	-3.8	-16.4	-19.6	-13.6	-24.8	-37.9	-48.7									
	5	-5.8	-11.0	-13.0	-12.4	-6.2	-9.4	-22.1	-30.0	-37.1	-45.8									
	6	-5.8	-11.0	-13.0	-12.4	-6.2	-9.4	-22.1	-30.0	-37.1	-45.8									
12	1	-0.1	-6.4	-10.5	-13.7	-16.6	-19.5	-22.5	-25.7	-29.5	-34.4	-41.8								
	5	-11.5	-6.4	-10.5	-13.7	-5.2	-19.5	-11.0	-25.7	-29.5	-34.4	-53.2								
13	1	-0.1	-6.4	-10.3	-13.4	-16.2	-18.9	-21.5	-24.4	-27.5	-31.2	-36.0	-43.3							
	2	-12.4	-0.6	-13.3	-8.5	-15.1	-15.3	-18.0	-23.3	-22.6	-34.2	-30.2	-55.6							
	3	-10.8	-12.4	-1.5	-11.6	-16.7	-12.3	-14.9	-24.9	-25.7	-22.4	-42.0	-54.0							
	4	-8.9	-13.0	-12.2	-2.7	-10.1	-18.3	-21.0	-18.3	-16.8	-33.1	-42.6	-52.1							
	5	-11.9	-9.4	-7.2	-15.1	-4.4	-17.2	-19.9	-12.5	-29.2	-28.1	-39.1	-55.1							
	6	-5.8	-11.3	-13.8	-14.5	-13.2	-6.5	-9.2	-21.4	-28.6	-34.7	-40.9	-49.0							
14	1	-0.1	-6.3	-10.2	-13.2	-15.9	-18.4	-20.8	-23.4	-26.1	-29.2	-32.8	-37.4	-44.6						
	3	-12.2	-11.4	-1.3	-15.2	-12.7	-11.3	-20.8	-16.3	-22.9	-31.1	-23.8	-42.6	-56.8						
	5	-9.0	-13.3	-13.4	-8.1	-3.7	-16.4	-20.8	-21.4	-13.9	-24.0	-36.0	-44.5	-53.6						
15	1	-0.1	-6.3	-10.1	-13.1	-15.6	-18.0	-20.3	-22.6	-25.0	-27.7	-30.7	-34.2	-38.8	-45.9					
	2	-13.7	-0.4	-14.3	-7.8	-15.6	-13.8	-17.7	-20.1	-20.8	-27.7	-25.4	-38.4	-33.0	-59.5					
	4	-11.1	-14.0	-10.1	-2.0	-15.6	-18.0	-12.5	-14.8	-25.0	-27.7	-19.6	-34.2	-46.6	-57.0					
	7	-5.9	-11.5	-14.3	-15.6	-15.6	-13.8	-6.7	-9.0	-20.8	-27.7	-33.2	-38.4	-44.0	-51.7					
	8	-5.9	-11.5	-14.3	-15.6	-15.6	-13.8	-6.7	-9.0	-20.8	-27.7	-33.2	-38.4	-44.0	-51.7					
16	1	-0.1	-6.2	-10.1	-13.0	-15.4	-17.7	-19.8	-22.0	-24.2	-26.5	-29.1	-32.0	-35.5	-40.0	-47.1				
	3	-12.6	-13.9	-1.0	-13.0	-16.9	-10.0	-14.9	-22.0	-19.3	-18.9	-30.6	-32.0	-26.4	-47.7	-59.7				
	5	-9.1	-13.9	-15.0	-13.0	-2.8	-10.0	-18.4	-22.0	-22.8	-18.9	-16.5	-32.0	-40.5	-47.7	-56.2				
	7	-14.1	-6.2	-13.6	-13.0	-11.9	-17.7	-5.8	-22.0	-10.2	-26.5	-25.6	-32.0	-39.0	-40.0	-61.1				
17	1	0.0	-6.2	-10.0	-12.8	-15.3	-17.4	-19.5	-21.5	-23.5	-25.7	-28.0	-30.5	-33.3	-36.8	-41.2	-48.2			
	2	-14.7	-0.3	-15.2	-7.4	-16.3	-12.8	-17.9	-18.1	-20.1	-24.1	-23.3	-31.5	-27.9	-42.0	-35.4	-62.9			
	3	-13.8	-13.1	-0.8	-15.9	-13.8	-9.5	-19.8	-16.0	-18.0	-26.0	-20.1	-29.0	-36.4	-27.6	-48.1	-62.0			
	4	-11.3	-15.0	-13.6	-1.6	-11.6	-18.0	-18.9	-12.7	-14.7	-25.0	-28.6	-26.8	-22.0	-40.4	-50.0	-59.5			
	5	-14.4	-9.5	-12.1	-15.3	-2.5	-18.3	-11.0	-19.6	-21.6	-17.2	-28.9	-17.7	-35.8	-38.9	-44.5	-62.6			
	6	-9.2	-14.1	-15.5	-14.3	-8.4	-3.7	-16.4	-21.2	-23.2	-22.6	-14.2	-23.6	-34.8	-42.3	-49.1	-57.4			
	7	-12.8	-14.7	-6.7	-10.7	-17.2	-15.0	-5.1	-20.6	-22.6	-11.3	-25.5	-32.4	-31.2	-33.5	-49.7	-61.0			
	8	-5.9	-11.6	-14.6	-16.2	-16.9	-16.4	-14.2	-6.8	-8.9	-20.4	-27.0	-32.1	-36.7	-41.4	-46.6	-54.1			
18	1	0.0	-6.2	-9.9	-12.8	-15.1	-17.2	-19.2	-21.1	-23.0	-25.0	-27.0	-29.3	-31.7	-34.5	-37.9	-42.3	-49.3		
	5	-14.7	-11.7	-9.9	-16.5	-2.2	-17.2	-17.4	-11.9	-23.0	-15.8	-25.3	-29.3	-18.8	-38.2	-37.9	-47.8	-63.9		
	7	-12.9	-15.4	-9.9	-7.3	-16.9	-17.2	-4.5	-17.4	-23.0	-21.3	-12.4	-29.3	-33.5	-29.0	-37.9	-51.5	-62.2		
19	1	0.0	-6.2	-9.9	-12.7	-15.0	-17.0	-18.9	-20.8	-22.6	-24.4	-26.3	-28.3	-30.5	-32.9	-35.6	-39.0	-43.4	-50.3	
	2	-15.7	-0.3	-16.1	-7.1	-16.9	-12.1	-18.2	-16.8	-19.9	-21.8	-22.3	-27.5	-25.6	-34.8	-30.1	-45.2	-37.5	-65.9	
	3	-14.2	-15.2	-0.7	-14.3	-17.4	-8.8	-15.5	-21.0	-16.1	-18.0	-26.5	-24.8	-22.2	-35.3	-37.2	-29.8	-52.4	-64.4	
	4	-13.0	-15.9	-12.1	-1.2	-16.1	-18.3	-13.3	-11.3	-21.8	-23.7	-16.8	-22.6	-31.7	-34.0	-24.2	-41.2	-53.1	-63.3	
	5	-11.5	-15.7	-15.6	-10.5	-2.0	-15.9	-19.7	-19.5	-12.8	-14.7	-25.0	-29.0	-29.3	-19.9	-33.4	-44.7	-52.9	-61.7	
	6	-9.3	-14.4	-16.3	-16.2	-13.4	-2.9	-9.9	-18.4	-22.3	-24.2	-23.9	-19.3	-16.3	-31.3	-39.1	-45.4	-51.6	-59.5	
	7	-15.4	-9.5	-13.7	-15.4	-7.9	-18.6	-4.0	-20.3	-18.4	-20.2	-25.8	-13.4	-32.0	-25.8	-38.3	-42.8	-46.7	-65.7	
	8	-14.9	-13.3	-6.6	-16.9	-11.2	-14.3	-19.4	-5.4	-21.1	-22.9	-10.9	-28.8	-27.8	-29.1	-39.8	-35.7	-50.5	-65.2	
	9	-5.9	-11.7	-14.8	-16.6	-17.6	-17.8	-17.0	-14.6	-6.9	-8.8	-20.1	-26.4	-31.2	-35.5	-39.6	-43.9	-48.9	-56.2	
20	1	0.0	-6.2	-9.9	-12.6	-14.9	-16.9	-18.7	-20.5	-22.2	-23.9	-25.7	-27.5	-29.5	-31.6	-34.0	-36.7	-40.0	-44.3	-51.2
	3	-15.1	-14.5	-0.6	-16.8	-14.9	-8.5	-19.6	-16.3	-15.4	-23.9	-18.9	-23.3	-30.4	-23.2	-34.0	-40.9	-30.7	-52.7	-66.3
	7	-9.3	-14.5	-16.6	-16.8	-14.9	-8.5	-3.6	-16.3	-21.3	-23.9	-24.8	-23.3	-14.4	-23.2	-34.0	-40.9	-46.8	-52.7	-60.4
	9	-16.0	-6.2	-15.7	-12.6	-14.9	-16.9	-12.9	-20.5	-6.2	-23.9	-9.7	-27.5	-23.6	-31.6	-34.0	-36.7	-45.9	-44.3	-67.2

Table 20.3 *Calculated Spur Levels for the Uncompensated First Order Modulator*

Integer Boundary Spur Property

Notice that the integer boundary spurs approach 0 dBc as Fnum/Fden approaches zero and if this ratio is less than about $1/5^{th}$, the spur is typically within about 1 dB of this limit. This property holds as a general rule of thumb.

Impact of Fractional Compensation on Fractional Spurs

So far, spurs have been discussed with pure mathematical calculations. On devices where the fractional compensation can be disabled, there tends to be very good agreement between the mathematically calculated spurs and the actual measurement. However, high spurs are never desirable so devices tend to have analog compensation in the form of an adjustable delay at the phase detector or charge injected into the loop filter. For these kinds of compensation, the spurs can be typically modeled using the pure mathematics and some fixed constant can be subtracted from these calculated values to get the spur levels.

Spurs for a device are typically specified with the *InBandSpur* metric which just subtracts this constant away from the default integer boundary spur level of 0 dBc. It also makes it easy to measure the quantity directly. For instance, if a PLL has an InBandSpur of -18 dBc, this means that one can set a fraction such as 1/100 and measure the integer boundary spur within the loop bandwidth and expect around -18 dBc. All the other spurs would be expected to be shifted down by this factor of 18 dBc as well.

For higher level delta-sigma PLLs, there is a more accurate way to calculate the spurs, but one can get a reasonable approximation by treating them as compensated spurs from a first order modulator using the InBandSpur metric. The following table shows this metric for various Texas Instruments PLLs.

PLL	*InBandSpur*	Comments
Uncompensated Fractional PLL	0	This does not apply to fractional spur levels worse than about –12 dBc after they have been filtered by the loop filter.
LMX2350/52/53/54	- 15	InBandSpur for second fractional spur is closer to –12 dBc
LMX2364	-18	InBandSpur for the second fractional spur is closer to –13 dBc. Spur level is sensitive to fractional denominator.
LMX2470/71	-20 to –50 -35 typical	The fractional spurs on this part are better when the phase detector frequency is around 20 MHz and a fractional denominator greater than 100. There is benefit expressing fractions with higher fractional denominators, even if the mathematical values are equivalent.
LMX2485/86/87	-55 to -65 Typical	This is for a fourth order modulator inside the loop bandwidth with a 20 MHz phase detector frequency.

Table 20.4 *In-Band Compensated Fractional Spurs for Various PLLs*

Although the modeling of spurs is very worthwhile, fractional spurs can have many contributors. For the first order modulator, the models tend to match measured data better, but there is no substitute for verification on the bench.

Fractional Spur Avoidance

Introduction

The concept of spur avoidance involves avoiding fractions that are known to have high spurs by either simply avoiding these frequencies or by shifting internal frequencies in the PLL.

Worst Case Numerators for the First Fractional Spur

In most applications, it is the first fractional spur at offset of $1/(f_{PD}f_{DEN})$ that causes the most issues. Although it is known that *1* and *Fden-1* are the worst cases for this spur, there is also interest in knowing the next worst case fractions. Following is a table showing the worst case numerators for the first fractional spur.

Fractional Denominator	In-Band Fractional Spur				Fractional Numerator			
	Worst-case	2nd Worst	3rd Worst	4th Worst	Worst	2nd Worst	3rd Worst	4th Worst
2	-3.9	x	x	x	1	X	x	x
3	-1.6	x	x	x	1	X	x	x
4	-0.9	x	x	x	1	X	x	2
5	-0.6	-4.8	x	x	1	2	x	x
6	-0.4	x	x	x	1	X	x	3
7	-0.3	-5.4	-7.3	x	1	3	2	x
8	-0.2	-7.9	x	x	1	3	x	x
9	-0.2	-5.7	-9.4	x	1	4	2	x
10	-0.1	-8.5	x	x	1	3	x	x
11	-0.1	-5.8	-8.7	-10.3	1	5	4	3
12	-0.1	-11.5	x	x	1	5	x	x
13	-0.1	-5.8	-8.9	-10.8	1	6	4	3
14	-0.1	-9.0	-12.2	x	1	5	3	x
15	-0.1	-5.9	-11.1	-13.7	1	7	4	2
16	-0.1	-9.1	-12.6	-14.1	1	5	3	7
17	0.0	-5.9	-9.2	-11.3	1	8	6	4
18	0.0	-12.9	-14.7	x	1	7	5	x
19	0.0	-5.9	-9.3	-11.5	1	9	6	5
20	0.0	-9.3	-15.1	-16.0	1	7	3	9
21	0.0	-6.0	-11.6	-13.2	1	10	5	4
22	0.0	-9.3	-13.3	-15.5	1	7	9	3
23	0.0	-6.0	-9.4	-11.7	1	11	8	6
24	0.0	-13.4	-15.7	-17.6	1	5	7	11
25	0.0	-6.0	-9.4	-11.7	1	12	8	6
26	0.0	-9.4	-13.5	-15.9	1	9	5	11
27	0.0	-6.0	-11.8	-13.5	1	13	7	11
28	0.0	-9.4	-13.6	-17.6	1	9	11	3
29	0.0	-6.0	-9.4	-11.8	1	14	10	7
30	0.0	-16.1	-18.8	-19.4	1	13	11	7
31	0.0	-6.0	-9.4	-11.8	1	15	10	8
32	0.0	-9.4	-13.7	-16.2	1	11	13	9
33	0.0	-6.0	-11.9	-13.7	1	16	8	13
34	0.0	-9.5	-13.7	-16.3	1	11	7	5
35	0.0	-6.0	-9.5	-11.9	1	17	12	9
36	0.0	-13.7	-16.4	-19.5	1	7	5	13
37	0.0	-6.0	-9.5	-11.9	1	18	12	9
38	0.0	-9.5	-13.8	-16.4	1	13	15	11
39	0.0	-6.0	-11.9	-13.8	1	19	10	8
40	0.0	-9.5	-16.5	-18.4	1	13	17	9
41	0.0	-6.0	-9.5	-11.9	1	20	14	10
42	0.0	-13.8	-19.8	-20.9	1	17	19	13
43	0.0	-6.0	-9.5	-11.9	1	21	14	11
44	0.0	-9.5	-13.8	-16.6	1	15	9	19
45	0.0	-6.0	-11.9	-16.6	1	22	11	13
46	0.0	-9.5	-13.8	-16.6	1	15	9	13
47	0.0	-6.0	-9.5	-12.0	1	23	16	12
48	0.0	-13.8	-16.6	-20.1	1	19	7	13
49	0.0	-6.0	-9.5	-12.0	1	24	16	12
50	0.0	-9.5	-16.6	-18.6	1	17	7	11

Table 20.5 *Calculated First Fractional Spur*

From this table, we see that there is a pattern to the worst case numerators that starts to form once the numerator gets larger than about ten. To see the pattern, first generate the sequence:

$$1,\ floor\left(Fden/_2\right), floor\left(Fden/_3\right), floor\left(Fden/_4\right), floor\left(Fden/_5\right),\ \ldots \qquad \textbf{(20.10)}$$

If it turns out that the term in the sequence is an integer before the floor function is applied, then just skip to the next one. Once this is found, the spur is referenced from the following table.

Term	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Spur Power	0.0	-6.0	-9.5	-12.0	-14.0	-15.6	-16.9	-18.1	-19.1	-20.0	-20.8	-21.6	-22.3	-22.9	-23.5	-24.1	-24.6	-25.1	-25.6	-26.0

Table 20.6 *Fractional Spur Chart for First Primary Fractional Spur*

By observing the kth term in Table 20.6, the spur power follows the following formula.

$$Spur\ Power = 20 \cdot log(k) \qquad \textbf{(20.11)}$$

For example, consider the case where *Fden = 100*, which produces a sequence of 1, 50, 33, 25, 20, 16, …. The worst case numerators would be 1 and 99 and this would correspond to an unfiltered spur level of 0 dBm. For the second element, 50 has a common factor with 100, so we skip this one. It therefore follows that the second worst case pair of fractions would be 33/100 and 67/100, which would have an InBandSpur of -9.5 dBc. The next number is 25. Because this has a factor in common with 100, there is no spur here. The next number is 20, which also has a factor in common with 100, so there is no spur here either. Now the exception comes when the same number is repeated in the sequence. In this case, the spur power is correct, but the numerator is slightly shifted.

Worst Case Numerators for the Second and Higher Order Fractional Spurs

For spurs higher than first order, the worst case denominators for the n^{th} fractional spur are when the numerator is *n* and *Fden-1*. Avoiding the first primary fractional spur is typically the main focus of fractional spur avoidance. For instance, the worst case fractions for the second primary fractional spur with a denominator of 101 would be 2/101 and 99/101. However for those interested in the second primary fractional spur, the offset would be $2/(f_{PD}f_{DEN})$ and the worst case pair of numerators would be ***2*** and ***Fden – 2***. In most cases, the second worst-case spur is at numerator of ***1*** and ***Fden-1***, but there are exceptions. In this case, it is probably best to use the table. For the ***nth*** fractional spur, this is typically worst when the fractional numerator is ***n*** or ***Fden - n***.

Fractional Denominator	In-Band Fractional Spur				Fractional Numerator			
	Worst-case	2nd Worst	3rd Worst	4th Worst	Worst	2nd Worst	3rd Worst	4th Worst
2	x	x	x	x	x	X	1	x
3	-13.7	x	x	x	1	X	x	x
4	-3.9	-9.9	x	x	2	1	x	x
5	-4.3	-8.4	x	x	2	1	x	x
6	-1.6	-7.7	x	x	2	1	x	x
7	-2.1	-7.2	-9.1	x	2	1	3	x
8	-0.9	-6.9	-6.9	x	2	1	3	x
9	-1.3	-6.7	-10.4	x	2	1	4	x
10	-0.6	-4.8	-6.6	-10.8	2	4	1	3
11	-0.8	-6.5	-9.4	-11.0	2	1	3	5
12	-0.4	-6.4	-6.4	x	2	1	5	x
13	-0.6	-6.4	-9.4	-11.3	2	1	5	6
14	-0.3	-5.4	-6.3	-7.3	2	6	1	4
15	-0.4	-6.3	-11.5	-14.0	2	1	7	4
16	-0.2	-6.2	-6.2	-7.9	2	1	7	6
17	-0.3	-6.2	-9.5	-11.6	2	1	5	8
18	-0.2	-5.7	-6.2	-9.4	2	8	1	4
19	-0.3	-6.2	-9.5	-11.7	2	1	7	9
20	-0.1	-6.2	-6.2	-8.5	2	1	9	6
21	-0.2	-6.2	-11.8	-13.4	2	1	10	8
22	-0.1	-5.8	-6.1	-8.7	2	10	1	8
23	-0.2	-6.1	-9.5	-11.8	2	1	7	11
24	-0.1	-6.1	-6.1	-11.5	2	1	11	10
25	-0.2	-6.1	-9.5	-11.9	2	1	9	12

Table 20.7 *Calculated Second Fractional Spur*

Optimal Fraction Choices

Consider the case where a fractional PLL is required for finer tuning resolution, but the required frequencies span is much less than the phase detector frequency. From (20.10) and Table 20.6, one would want to stay away from fractions of 0, ½, 1/3, 2/3, and so on. It therefore makes sense to choose a fraction that is as far as possible. If one considers the total integrated spur energy from 0 to f_{PD}, and considers only prime fractional denominators, one of the optimal points for lowest spurs tends to be around 5/12. If one was to consider the sequence of fractional numerators, this is right between *Fden/3* and *Fden/4*.

For instance, suppose one has the choice of VCO frequency in the range of 2400 to 2412 MHz from a 12 MHz phase detector frequency. The device operates with a fixed frequency, but this frequency needs to be able to tune ±100 kHz in 1 kHz increments. What would be a good choice for the VCO frequency? The worst cases would be 2400, 2412, and 2406 MHz, since moving the VCO frequency slightly would generate the highest spurs. A good choice would be 2405 MHz as this is fairly far from these worst case spurs and moving the VCO frequency a small amount would still be far away from problematic frequencies.

Direct Spur Avoidance

Direct spur avoidance is simply deciding to not use the channels that cause the most grief. In some standard, it is acceptable to simply not use particular channels. In other cases, it might be desirable to have a PLL that has a wide tuning range, but not every frequency is used. This could be the case in applications where the PLL is being used to clock an A/D converter.

Spur Avoidance by Shifting Phase Detector Frequency

If a particular output frequency is necessary, one approach is to shift the phase detector frequency. Sometimes this can be done by shifting the f_{OSC} frequency, and other times it can be done with the same f_{OSC} frequency if the device as a programmable multiplier on the input. In these cases with the programmable input multiplier, be aware that there are spurs other than those due to the fractional circuitry that are caused by the f_{OSC} signal mixing with the f_{VCO} or f_{OUT} signals. For example, the following figure, the programmable multiplier can be used to shift he phase detector from 100 MHz to 75 MHz in order to avoid the integer boundary. This significantly mitigates the spur due to the fractional circuitry, but it is still possible to get a spur at 100 kHz offset due to the mixing of the f_{OSC} and f_{VCO} frequencies.

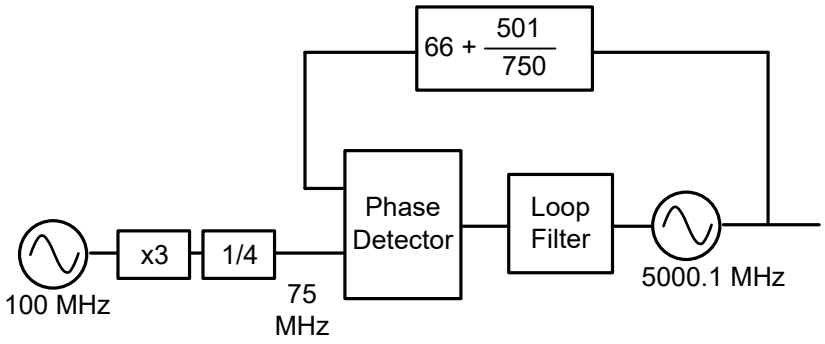


Figure 20.3 *Spur Avoidance by Shifting the Phase Detector Frequency*

Spur Avoidance by Shifting f_{VCO}

It is getting more common to have PLL synthesizers with a divider following the VCO. In these situations, it is often the case that there are multiple frequencies for the VCO that can achieve the same output frequency. In this situation, sometimes it can make a difference for the fractional spurs. In the following diagram, if the output divider was to support values from 1 to 10 and the VCO was to tune from 2-3 GHz, 2750.5 MHz would be a better choice of the VCO frequency for spurs as it would avoid the integer boundary, whereas 2200.4 MHz would be much closer to an integer boundary.

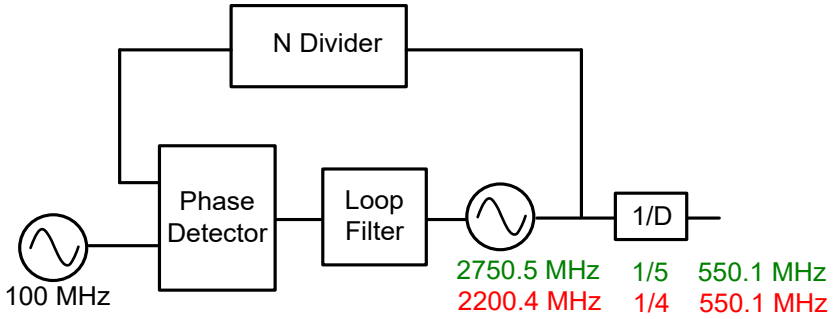


Figure 20.4 *Choosing the Best VCO Frequency for Spurs*

Conclusion

Fractional spurs can be very complicated, and the understanding of the first order modulator is the first step to understanding the fundamental patterns of fractional spurs. For the first order modulator, the key patterns for the spur levels and the offset frequencies are easier to calculate and match measured results fairly well. Higher order modulators add more exceptions and complications to fractional spurs, but understanding the fundamental concepts first is key to understanding these more complicated cases.

Appendix: Justification of the Fundamental Properties of Fractional N

Equivalent Fraction Principle Justification Using the Modulator Sequence

This is easiest to justify by just looking at the fractional sequence for a fraction of 3/12.

Accumulator: 3,6,9,0,3,6,9,0, … (repeats)

Output: 0,0,0,1,0,0,0,1, … (repeats)

The equivalent fraction of ¼ has the sequence of:

Accumulator: 1,2,3,0,1,2,3,0, … (repeats)

Output: 0,0,0,1,0,0,0,1, … (repeats)

We see that the output sequence is the same in both cases as the accumulator value is just multiplied by three. This same reasoning can be used to show the equivalent property holds in general for the fractions of *Fnum/Fden* and (*k*·*Fnum*)/(*k*·*Fden*).

Initial State Independence Principle Justification Using the Modulator Sequence

Consider a fractional PLL with an initial state of *Seed0* < *Fden* and allow for the possibility of the fraction not being lowest terms with numerator of *g*·*Fnum* and denominator of *g*·*Fden*. After *Fden* cycles of the phase detector, the accumulator value will be:

$$(Seed0 + k \cdot g \cdot Fnum) \quad \% \quad g \cdot Fden \qquad \textbf{(20.12)}$$

After *k*=*Fden* clock cycles, we see that this returns the same initial state of *Seed0*. For that matter, one could argue that the accumulator state at any two periods that are *Fden* clock cycles apart will have the same seed, and thus this establishes the sequence length is *Fden*. Now in regards to the output of the modulator, we see that it is just shifted each cycle by adding *Seed0* and taking modulo *Fden*. This implies that the output of the modulator will be the same pattern, but possibly shifted. The following example illustrates this for a fraction of 6/20 and a *Seed0*=7, which has the same sequence advanced one clock cycle

Seed0=0		
Cycle	**Accumulator**	**Output**
0	0	0
1	6	0
2	12	0
3	18	0
4	4	1
5	10	0
6	16	0
7	2	1
8	8	0
9	14	0
10	0	1
11	6	0
12	12	0

Seed0=7		
Cycle	**Accumulator**	**Output**
0	7	0
1	13	0
2	19	0
3	5	1
4	11	0
5	17	0
6	3	1
7	9	0
8	15	0
9	1	1
10	7	0
11	13	0
12	19	0

Table 20.8 *Demonstration that Seed Does Not Impact the Output*

Spur Symmetry Property for the First Order Modulator

Start with the fraction of 3/10 and calculate the output of the modulator.

Accumulator: 3,6,9,2,5,8,1,4,7,0, … (repeats)

Output: 0,0,0,1,0,0,1,0,0,1, … (repeats)

The modulator output and sequence for the symmetric fraction of 7/10 is:

Accumulator: 7,4,1,8,5,2,9,6,3,0,7,4,1,8,5,2,9, (repeats last 10 entries)

Output: 0,1,1,0,1,1,0,1,1,1,0,1,1,0,1,1,0, (repeats last 10 entries)

The pattern many not be as obvious, but if we instead think of 7 as -3, as they are equivalent modulo 10, we get the following sequence, which produces the inverted output of 3/10.

Accumulator: -3,-6,-9,-2,-5,-8,-1,-4,-7, 0, (repeats last 10 entries)

Output: 1, 1, 1, 0, 1, 1, 0, 1, 1, 0, (repeats last 10 entries)

This principle can be generalized to any fraction of the form *Fnum/Fden*.

Primary Fractional Spurs for the First Order Modulator

As it can be assumed that *Fnum* and *Fden* have no common factors, it can be shown that the length of the fractional sequence is *Fden*. To reason this, we can assume that the modulator starts out with a state of zero and after k cycles, the accumulator output is a multiple of *Fden*. Clearly after *Fden* cycles this is true, but it needs to be established that it is not something smaller. Consider the accumulator output.

Accumulator: *0*, *Fnum*, … , *Fnum*·*k*, … (repeats)

In other words,

$$Fnum \cdot k \equiv 0 \ (mod \ Fden) \qquad \textbf{(20.13)}$$

For this modular equation, the fact that *Fnum* and *Fden* are relatively prime guarantees that the inverse of *Fnum* exists and therefore *k* must be a multiple of *Fden*. So it follows that the sequence repeats every *Fden* cycles.

Chapter 21 Delta Sigma Fractional Spurs

Introduction

Delta sigma fractional PLLs build upon the foundation of the first order modulator by adding the concepts of higher order modulators. Higher order modulators reduce spurs by generating a sequence containing more than just two divide values. Perhaps the most common implementation is the *MASH* (Multi-stAge Shaping) architecture. Although it reduces the spurs, additional spurs can also be created. This chapter discuses some key delta sigma fractional concepts.

Comparison of Higher Order Delta Sigma PLLs to the First Order Modulator

The first order modulator has already been discussed to establish some of the fundamentals of fractional N PLLs. With higher order modulators, these fundamentals are a good starting point, but they do not fully hold as shown in Table 21.1.

Property	***First Order Modulator***	***Delta Sigma PLL***
Integer Boundary Spur Offset	*Offset frequency is distance to closest integer channel*	
Phase Detector Nulls	*Fractional engine produces no spur at multiples of the phase detector Frequency.*	
Equivalent Fractions	*Have the same spur*	*Have same spurs if the initial state is zero or if there is a large amount of randomization.*
Symmetric Fractions	*Have the same spur*	*Have the same spurs if fraction is well-randomized, but not in general.*
Initial State Independence	*Does not impact spurs*	*Can impact spurs if the fraction is not well-randomized*
Fractional Spur Offsets	*Occur at integer multiples of f_{PD}/Fden*	*Have spurs at f_{PD}/Fden, but also can get additional sub-fractional spurs, depending on fractional denominator and modulator order.*

Table 21.1 *Comparison of Delta Sigma PLL to the First Order Modulator*

Spur Calculations for Higher Order Modulators

Sub-Fractional Spurs

For higher order modulators, the sequence can have a longer repeat length. Consider the example of a third order modulator with a fraction of 3/10 which produces the following modulator sequence.

0,1,0,0,0,1,1,-1,0,2,-2,3,-2,2,-1,0,2,0,-1,1, … (repeats) …

In this case the sequence has a repeat length of 20, not 10, so this implies that the spurs will have half the offset frequency. If the phase detector frequency was to be 10 MHz, then the spurs at offsets of 1,2,3,4,5,6,7,8, and 9 MHz would be considered *primary fractional spurs* and the spurs at offsets of 0.5,1.5,2.5,3.5,4.5,5.5,6.5,7.5,8.5, and 9.5 MHz would be

considered *sub-fractional spurs*. As the first sub-fractional spurs start at half of the offset of the primary spurs, the can be considered as ½ sub-fractional spurs. For the MASH architecture, the potential occurrence of these sub-fractional spurs depends on the simplified fractional denominator and modulator order. Through simulations, the following table shows when they occur:

Fden Factors	1st Order Modulator	2nd Order Modulator	3rd Order Modulator	4th Order Modulator
No Factor of 2 or 3	None	None	None	None
Factor of 2 but not 3	None	½	½	1/4
Factor of 3 but not 2	None	None	1/3	1/3
Factor of 2 and 3	None	½	1/6	1/12

Table 21.2 *Simplified Fractional Denominator and Sub-Fractional Spurs*

These properties of sub-fractional spurs hold consistently and are proven in the appendix by looking at the modulator sequence.

Impact of the Initial Modulator State (Seed)

Initial State is Device Specific

For all the derivations for the seed in this book, it is assumed that the accumulator counts up and starts at zero and there are no clock delays. However, some devices might have accumulators that count down or there could be clock delays. This could have the impact of shifting seeds from *Seed* to *Fden* - *Seed*, or translating their values. If this is the case, then all the theory concerning seeds still holds, but the impact is that the actual seed programmed to the part may be translated. This book assumes no delays and the accumulators count up, but the reader should be aware that some PLLs may work differently.

Impact of Initial State

For delta sigma modulators of higher than first order, it turns out that the initial accumulator state can impact the spurs. The impact of nonzero seeds can be beneficial or harmful. In general, these principles hold:

- Seeds tend to have minimal impact for larger fractional denominators that are on the order of 500 or greater.
- Seeds tend to have minimal impact when dithering is used.
- Fractions that are not lowest terms with a non-zero seed value can get spurs in addition to what would be expected of the simplified fraction if the seed does not divide into both the numerator and denominator.
- A fraction with numerator zero can have fractional spurs if the seed is non-zero.

One characteristic that nonzero seeds bring is that they can create spurs for fractions that are not zero or that do not simplify. For instance, (21.1) shows the same PLL with a 20 MHz phase detector and a fraction of 0/100. The blue curve is with a seed of zero and has no fractional spurs. The red curve has a seed of one and it can be seen that this creates primary fractional spurs at 2 MHz offset.

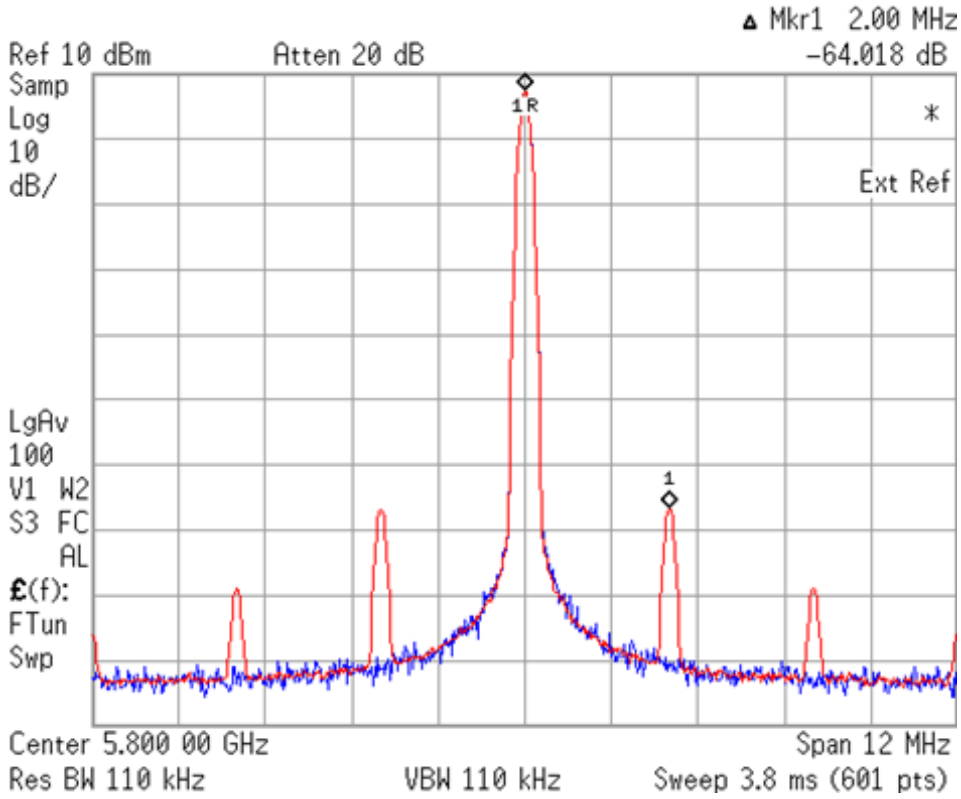


Figure 21.1 *LMX2582 with Fraction of 0/100 and f_{PD}=20MHz with Seed of 1*

The initial state can also be used to improve spurs in some situations as well. In Figure 21.2, the blue trace shows that we can see the introduction of a seed of 11 to the first stage eliminates the primary fractional spur at 100 kHz and reduces the other spur. The first reaction is likely to question the reliability and repeatability of this effect. This seed value was calculated based on pure mathematics and not just measurement. As fractional spurs have many causes, one does have to be aware the programmable seed only affects spurs due to the MASH engine; if the spur is due to crosstalk, then the effect of the seed can be less than expected or nothing at all.

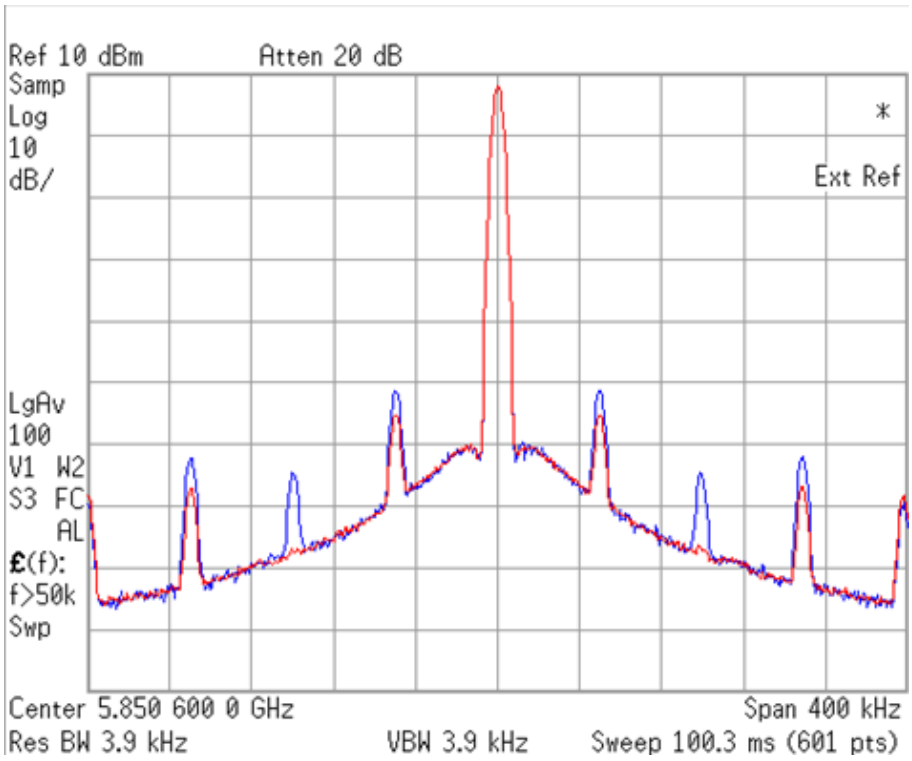


Figure 21.2 *Improvement for a Seed of 11 and 2nd Order Modulator with Fraction of 53/200, f_{PD}=20MHz, Pre-N Divide=2*

Restoring the Symmetrical Fraction Property with Seeds

In general, symmetric fractions like 3/10 and 7/10 do not have the same spurs for modulators higher than first order. However, it is possible to restore this property by using the seed values in Table 21.3. This table was derived by simulations and assumes that the fraction is lowest terms. If the fraction is not, then seed should be multiplied by the greatest common divisor of the fractional numerator and denominator. For instance, if one has a fraction of 55/100 with a second order modulator, a seed of 5, not 1 should be used. If the seed of 1 was to be used, it would generate additional spurs.

Modulator Order	Seed0	Seed1	Seed2	Seed3
First	0	n/a	n/a	n/a
Second	1	0	n/a	n/a
Third	2	1	0	n/a
Fourth	4	2	1	0

Table 21.3 *Symmetrical Seed Values*

Randomization

Concept of Randomization

The basic concept of *randomization* is to change the ordering of the delta sigma sequence while keeping the average value the same. This can theoretically be done with the first order modulator, but typically is done more with the higher order delta sigma modulators. Consider the following sequence:

0,1,0,-1,0,2 … (repeats) …

Now compare to this sequence;

0,1,0,-1,0,2, 2,0,-1,0,1,0… (repeats) …

If we compare these two sequences, we see that they both contain the same numbers, except that the second sequence has a longer repeat length and therefore spreads out the spur energy. When randomization is used, the order is changed, but the repeat sequence for the dithered sequence for a PLL is theoretically very much longer. It is also typically the case that dithering is used for larger fractions and larger equivalent fractions are used. For example, instead of expressing the fraction as 1/3, it could be expressed as 1000000/3000000. This is known as a larger equivalent fraction. By doing so and combining with dithering, the randomization is increased. If no randomization is used and the initial modulator state is zero, this is the same fraction as 1/3.

Randomization Through Larger Unequivalent Fractions

Another approach to randomization is to use a *larger unequivalent fraction*. This means that the fraction is expressed by a large fraction that is very close, but slightly offset from the original. For instance, the fraction of 1/3 can be expressed as 1000000/3000001. In this case, this can actually help reduce some of the primary fractional spurs. There may be some very low spur energy, but if the offset is low enough, it might not be a concern.

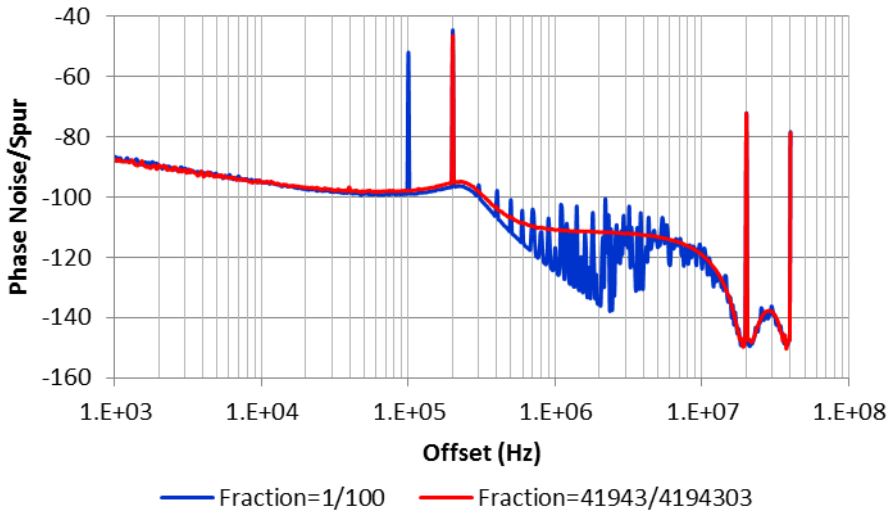


Figure 21.3 *Impact of Fractional Denominator on Randomization*

Non-Ideal Effects of the Delta Sigma Modulator

Charge Pump Nonlinearity

For delta sigma PLLs, charge pump nonlinearity is very important. If the charge pump is not linear, then the spurs at higher frequency will mix down to much lower offset frequencies before the loop filter has an opportunity to shape them. For delta sigma modulator phase noise, it looks like a noise floor as shown in Figure 21.4. Although this is showing phase noise, this shaping also applies to spurs because delta sigma phase noise is actually spurs that are very close together. Due to nonlinearity, the spurs at lower offsets do not follow the calculations as the Fourier series would predict. In fact, it is easier to just use the concept of InBandSpur as used for the first order modulator.

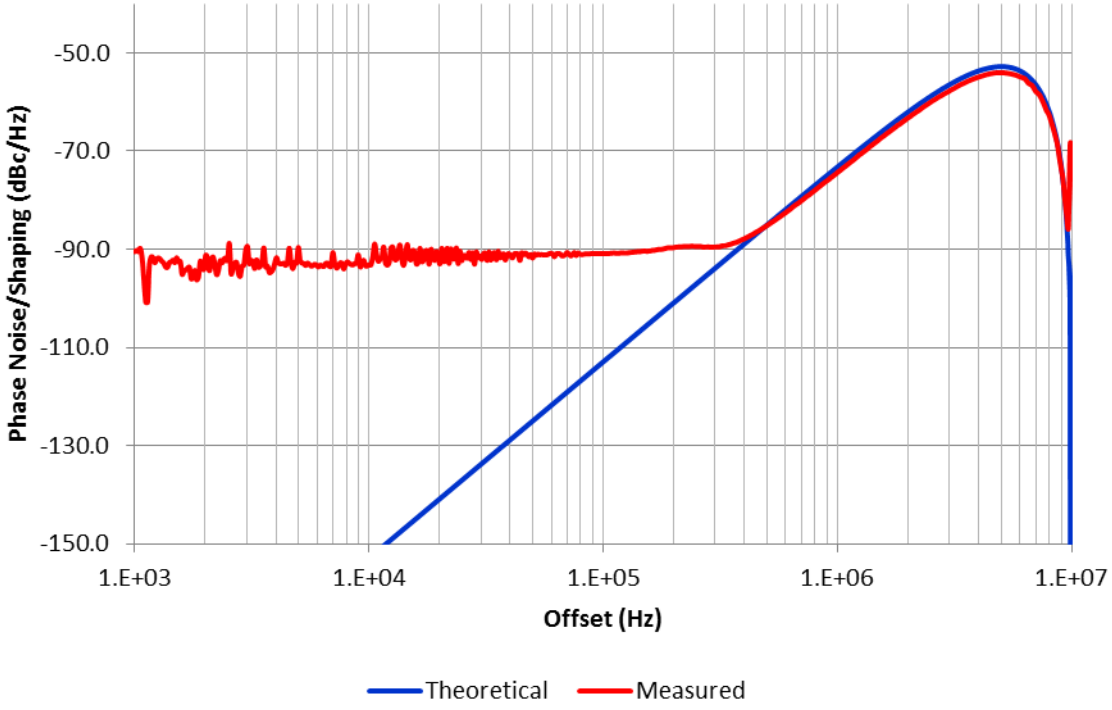


Figure 21.4 *Delta Sigma Noise Shaping Example*

Mash Clock Distortion

Another thing that can rob delta sigma PLLs of spur performance is the MASH clock distortion. So far, it has been assumed that the loop bandwidth is infinite and the output of the VCO perfectly follows the N counter modulation which happens at the phase detector rate. However, the loop bandwidth will be less than this rate and the net effect is that time period that the modulator stays at each N divider state is not exactly the phase detector period, but depends on the Value of the N divider. In general, if the loop bandwidth is more than twice of the spur frequency of interest, then this will help reduce the impact of the MASH clock distortion. Also, this effect is much less for feedback divider values of 50 or greater, but still can be a consideration.

Optimization of Fractional Settings

Now that fractional settings have been discussed, the next question would be how to optimize how to express the fraction, the MASH order, MASH seed, and dithering. Let's assume that all has been done to avoid the worst case fractions. The next thing is to express the desired fraction in the forms of a lowest terms fraction of *Fnum/Fden*. Table 21.4 shows guidelines that should always be followed.

Condition	Always Best Setting	Why
Fnum = 0	Integer Mode	There is no reason to add any fractional energy for an integer N divide. Many fractional PLLs may automatically disable the fractional engine for this case.
Fden ≤ 7	1st Order Modulator	Delta sigma modulators push low frequency spurs to higher frequencies, depending on the modulator order. The point where all the modulators have the same noise is $f_{PD}/6$ (discussed later). So higher order modulators will actually be worse spurs for these very low Fden Values

Table 21.4 *Always Best Guidelines*

Never Best Setting	Condition(s)	Why
Integer Mode	Fnum>0	Cannot hit the frequency
Randomization	• Integer Mode • 1st Order Modulator • 2nd Order Modulator with Fden Odd • 3rd or 4th Order Modulator with Fden not divisible by 2 or 3	Randomization is mainly for reducing sub-fractional spurs. In any one of these four conditions, there are no sub-fractional spurs to reduce and randomization may add unwanted phase noise.

Table 21.5 *Never Best Guidelines*

Now assuming that the always best and never best guidelines have been followed, this will not converge to a definitive answer to the modulator order whether or not to use randomization for the majority of cases. So the following table gives some more general recommendations.

Condition	Recommendation	Why
N Divider < 50	Use lower order modulators, although this is part specific. As a rough guideline, you want at least 50 to use the 4th order modulator, 30 to use the 3rd Order Modulator, and 15 use the 2nd order modulator	MASH clock distortion becomes an issue at lower N divider values and causes higher spurs.
$f_{PD}/Fden$ > 50· BW	1st Order Modulator	The first fractional spur will be far outside the loop bandwidth and likely to be crosstalk dominated.
Fden%2 > 0 *Fden%3 > 0*	3rd or 4th Order Modulator with No Randomization	In this case, there are no sub-fractional spurs, so one can use these higher order modulators without the fear of them
Fden%2=0 *Fden%3>0*	3rd Order Modulator 4th Order Modulator with Randomization	The 2nd and 3rd Order modulator will both have only the ½ sub-fractional spur, but the 3rd order likely has better primary fractional spurs. Use dithering with the 3rd Order modulator if the added phase noise is worth reducing the ½ sub-fractional spurs. The 4th order modulator will have the 1/4th sub-fractional spur, so likely randomization will be needed.
Fden%2>0 *Fden%3=0*	2nd Order Modulator with No Randomization Or 3rd and 4th Order Modulator with Randomization	The 2nd order modulator will have less sub-fractional spurs and add the least noise. If the 3rd or 4th order modulator has better primary fractional spurs, then dithering probably will be required to reduce the additional sub-fractional spurs.

Table 21.6 *Recommendations and Guidelines for Choosing Modulator and Dithering*

Conclusion

Delta sigma spurs add the concepts of modulator order and dithering to fractional spurs. Although they are more complicated, they do offer better fractional spurs.

References

[1] Banerjee, Dean *From Continuous to Discrete* Dogear Publishing 2014

[2] H.H. Perrot, M.D.Trott, G.G.Sodini "A Modeling Approach for a D-S Fractional-N Frequency Synthesizers Allowing Straightforward Noise Analysis" *IEEE Journal of Solid_State Circuits*, Vol 37, No. 8, August 2002

Appendix Occurrence of Fractional Spurs for Delta Sigma Modulators

Offsets of Primary and Sub-Fractional Spurs

The occurrence of fractional spurs can be understood mathematically by looking at the sequence from the accumulator. If one looks at the diagram of the delta sigma modulator and focuses just the accumulator value, we see the accumulator value for the next clock cycle is equal the accumulator value at the current clock cycle plus the output current quantizer at the current stage.

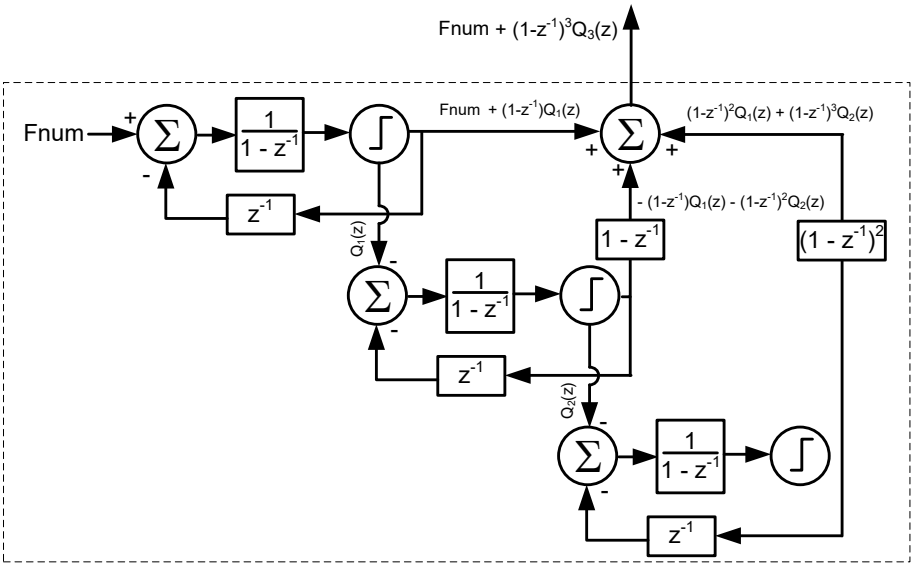


Figure 21.5 *3rd Order Modulator*

This diagram is equivalent to the one previously shown as all that has been done is that everything has been multiplied through by Fden and the quantizers work with Fden and not one. Following the diagram, we can say for the n^{th} stage and the k^{th} clock cycle, the accumulator state (A) and the quantizer output (Q) would be;

$$Q_n(\mathrm{k}) \equiv \mathrm{A}_n(k) \qquad (mod\ Fden) \qquad \textbf{(21.1)}$$

$$A_{n+1}(k+1) \equiv A_{n+1}(k) + Q_{n+1}(k) \qquad (mod\ Fden) \qquad \textbf{(21.2)}$$

This leads to the following conclusion:

$$A_{n+1}(k+1) \equiv A_{n+1}(k) + A_n(k+1) \qquad (mod\ Fden) \qquad \textbf{(21.3)}$$

This difference equation has the following solution:

$$A_{n+1}(k) \equiv \sum_{i=0}^{k-1} A_n\,(\mathrm{i}+1) \equiv \sum_{i=1}^{k} A_n\,(\mathrm{i}) \qquad (mod\ Fden) \qquad \textbf{(21.4)}$$

Without loss of generality, we can also assume the following:

$$A_n(0) \equiv 0 \qquad (mod\ Fden) \tag{21.5}$$

If one assumes a nonzero seed value, this would not change anything as it would appear on both sides of the equations that we end up solving and cancel out.

Accumulator	Symbol	Accumulator State	Additional Restrictions Imposed
First	$A_1(k)$	$Fnum \cdot k$	$k \equiv 0 \pmod{Fden}$
Second	$A_2(k)$	$Fnum \cdot \frac{k \cdot (k+1)}{2}$	$k \equiv 0 \pmod{2 \cdot Fden}$ (only if Fden is even)
Third	$A_3(k)$	$Fnum \cdot \frac{k \cdot (k+1) \cdot (k+2)}{6}$	$k \equiv 0 \pmod{3 \cdot Fden}$ (only if Fden is divisible by 3)
Fourth	$A_4(k)$	$Fnum \cdot \frac{k \cdot (k+1) \cdot (k+2) \cdot (k+3)}{24}$	$k \equiv 0 \pmod{4 \cdot Fden}$ (only if Fden is divisible by 2)

Table 21.7 *Modulator Table*

Table 21.7 shows the fundamental result that the first order modulator has no sub-fractional spurs and the 2nd order modulator has ½ sub fractional spurs for an even denominator. For the third order modulator, it shows that there can be ½ sub fractional spurs if the denominator and a denominator divisible by 3 can create 1/3 sub fractional spurs or even 1/6 sub-fractional spurs if the denominator is even. For the fourth order modulator, it shows how one can get ½, 1/3, or 1/12 sub-fractional spurs depending if the denominator has factors of 2 and 3.

More Rigorous Derivations

To derive these rules in Table 20.7, the concept is to set the accumulator state equal to zero and see when the soonest next clock cycle will be when the accumulator returns to this state. This is done by solving modular equations to find restrictions on k to find the soonest nonzero clock cycle when this occurs for all the modulators. The division/multiplication from reference [2] that is very useful for solving equations and is as follows:

$n \cdot X \equiv \mathrm{n} \cdot \mathrm{Y} \pmod{M}$ and $X \equiv \mathrm{Y} \left(mod\ \frac{M}{GCD(n,M)}\right)$ are equivalent **(21.6)**

For the first accumulator, we get the restriction that:

$$0 \equiv \text{Fnum} \cdot \text{k} \quad (mod\ Fden) \tag{21.7}$$

As *Fnum* and *Fden* are relatively prime, just divide through by Fnum to get the restriction:

$$k = i \cdot Fden \qquad i = 1,2,3,4,.. \tag{21.8}$$

For the second order modulator, we can do the summation with methods presented in reference [2] and this leads to the equation:

$$0 \equiv \frac{k \cdot (k+1)}{2} \qquad (mod\ Fden) \tag{21.9}$$

Now k is a multiple of *Fden* and clearly *k+1* is not. So we can divide this term out. However, if the fractional denominator is even, multiplying by two leads to the additional restriction:

$$k \equiv 0 \qquad (mod\ \ 2 \cdot Fden) \quad if\ Fden\ is\ Even \tag{21.10}$$

Looking at the third order modulator we get:

$$0 \equiv \frac{k \cdot (k+1) \cdot (k+2)}{6} \qquad (mod\ Fden) \tag{21.11}$$

If Fden has no factors of 2 or 3, then we can just multiply through by the 6 and keep the same modulus for the equation. If Fden has a factor of two, we already have a restriction that k=2·i·Fden from the second order modulator. If we replace this for the k+2 term, the factor of two cancels out and it leads to no further restrictions. However, if Fden has a factor of 3, then multiplying through by 6 will triple the modulus for the equation. As *k* would be a multiple of Fden, which is a multiple of 3, k+1 and k+2 will not and we can divide these out. When all is said and done, we get the additional restriction from the third order modulator that:

$$k \equiv 0 \qquad (mod\ 3 \cdot Fden) \quad if\ Fden\ is\ divisible\ by\ 3 \tag{21.12}$$

The fourth order modulator gives the constraint that:

$$0 \equiv \frac{k \cdot (k+1) \cdot (k+2) \cdot (k+3)}{24} \quad (mod\ Fden) \tag{21.13}$$

If Fden was to have a factor of 3, then we could write k=3·i·Fden and the k+3 term would cancel the factor of 3 from the numerator, so this would not add any additional factor of 3. If there was a factor of two, we write k=2·i·Fden and the k and k+2 terms would cancel out a factor of 4 out of the denominator of 24, but we still have a remaining factor of 2. So this would impose our final constraint that:

$$k \equiv 0 \quad (mod\ 4 \cdot Fden) \quad if\ Fden\ is\ divisible\ by\ 2 \tag{21.14}$$

Conclusion

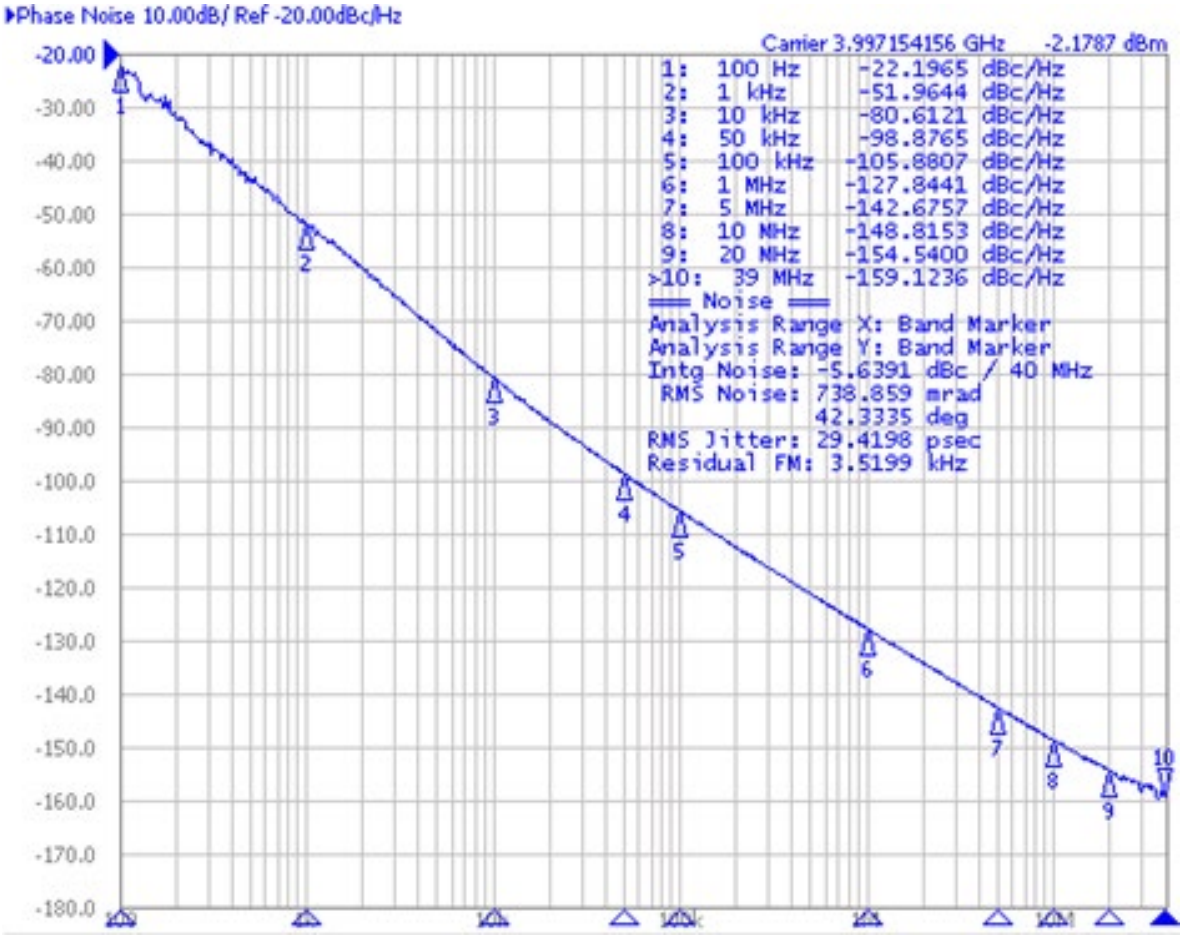
These rules are what imply the rules for the occurrences for sub-fractional spurs. Note that if the initial accumulator values were not zero, the exact reasoning could be applied. Likewise if Fnum and Fden were not lowest terms, but the initial state was zero, these conditions would hold by very similar reasoning. This reasoning would even work for a nonzero seed and Fnum and Fden not lowest terms provided that the initial states were all a multiple of the greatest common multiple of Fnum and Fden. If the seed was not a multiple of the greatest common multiple, then it would create additional sub-fractional spurs. However, this is typically not done intentionally unless it is used as some form of dithering.

Appendix B Modulator Sequence Example

Consider a fraction of 3/10 with the 4th order modulator to illustrate the accumulators and output sequence for the delta sigma modulator.

Accumulators and Quantizers								Outputs and Output Filters							
A1	Q1	A2	Q2	A3	Q3	A4	Q4	Y1	Y2	Y2·(1-1/z)	Y3	Y3·(1-1/z)^2	Y4	Y4·(1-1/z)^3	[SEQUENCE]
3	-3	3	-3	3	-3	3	-3	0	0	0	0	0	0	0	0
6	-6	9	-9	12	-2	5	-5	0	0	0	1	1	0	0	1
9	-9	18	-8	10	0	5	-5	0	1	1	1	-1	0	0	0
12	-2	10	0	0	0	5	-5	1	1	0	0	-1	0	0	0
5	-5	5	-5	5	-5	10	0	0	0	-1	0	1	1	1	1
8	-8	13	-3	8	-8	8	-8	0	1	1	0	0	0	-3	-2
11	-1	4	-4	12	-2	10	0	1	0	-1	1	1	1	4	5
4	-4	8	-8	10	0	0	0	0	0	0	1	-1	0	-4	-5
7	-7	15	-5	5	-5	5	-5	0	1	1	0	-1	0	3	3
10	0	5	-5	10	0	5	-5	1	0	-1	1	2	0	-1	1
3	-3	8	-8	8	-8	13	-3	0	0	0	0	-2	1	1	-1
6	-6	14	-4	12	-2	5	-5	0	1	1	1	2	0	-3	0
9	-9	13	-3	5	-5	10	0	0	1	0	0	-2	1	4	2
12	-2	5	-5	10	0	0	0	1	0	-1	1	2	0	-4	-2
5	-5	10	0	0	0	0	0	0	1	1	0	-2	0	3	2
8	-8	8	-8	8	-8	8	-8	0	0	-1	0	1	0	-1	-1
11	-1	9	-9	17	-7	15	-5	1	0	0	1	1	1	1	3
4	-4	13	-3	10	0	5	-5	0	1	1	1	-1	0	-3	-3
7	-7	10	0	0	0	5	-5	0	1	0	0	-1	0	3	2
10	0	0	0	0	0	5	-5	1	0	-1	0	1	0	-1	0
3	-3	3	-3	3	-3	8	-8	0	0	0	0	0	0	0	0
6	-6	9	-9	12	-2	10	0	0	0	0	1	1	1	1	2
9	-9	18	-8	10	0	0	0	0	1	1	1	-1	0	-3	-3
12	-2	10	0	0	0	0	0	1	1	0	0	-1	0	3	3

Phase Noise


Phase Noise 10.00dB/ Ref -20.00dBc/Hz
Carrier 3.997154156 GHz -2.1787 dBm
-20.00
-30.00
-40.00
-50.00
-60.00
-70.00
-80.00
-90.00
-100.0
-110.0
-120.0
-130.0
-140.0
-150.0
-160.0
-170.0
-180.0
1: 100 Hz -22.1965 dBc/Hz
2: 1 kHz -51.9644 dBc/Hz
3: 10 kHz -80.6121 dBc/Hz
4: 50 kHz -98.8765 dBc/Hz
5: 100 kHz -105.8807 dBc/Hz
6: 1 MHz -127.8441 dBc/Hz
7: 5 MHz -142.6757 dBc/Hz
8: 10 MHz -148.8153 dBc/Hz
9: 20 MHz -154.5400 dBc/Hz
>10: 39 MHz -159.1236 dBc/Hz
Noise
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -5.6391 dBc / 40 MHz
RMS Noise: 738.859 mrad
42.3335 deg
RMS Jitter: 29.4198 psec
Residual FM: 3.5199 kHz

Chapter 22 Oscillator Phase Noise

Introduction

The phased locked loop uses an oscillator on both the input reference and for the VCO. Oscillator phase noise improves at farther offsets from the carrier and can be generally divided into three regions: $1/f^3$, $1/f^2$, and floor. The $1/f^3$ region has phase noise that improves with offset at 30 dB/decade, the $1/f^2$ region has phase noise that improves as 20 dB/decade, and the floor region is flat. This chapter discusses the phase noise of oscillators in these regions and presents modeling methods.

Theory of Oscillator Noise

Simplified Noise Model

A common model for VCO phase noise models just the $1/f^2$ region. A traditional equation that describes phase noise in this region is called Lesson's Equation and is given below [1]:

$$L(f) = 10 \cdot log\left(\frac{1}{2} \cdot \frac{F \cdot k \cdot T}{P} \cdot \left(\frac{f_{VCO}}{2 \cdot Q_L \cdot f}\right)^2\right) \qquad \textbf{(22.1)}$$

$\boldsymbol{L(f)}$	=	Phase noise in dBc/Hz		
$\boldsymbol{f}$	=	Offset Frequency where phase noise is measured		
$\boldsymbol{F}$	=	Noise Figure of Active Device		
$\boldsymbol{k}$	=	Boltzman's constant	=	1.380658×10^{-23} J/K
$\boldsymbol{T}$	=	Temperature in Kelvin		
$\boldsymbol{P}$	=	RF Power at input of active device		
$\boldsymbol{f_{VCO}}$	=	Operating Frequency of the VCO		
$\boldsymbol{Q_L}$	=	Loaded Quality Factor of the inductor	=	X_L / R_L

The model predicts that lower noise figure and higher output power are theoretically better on a dB for dB basis and phase noise at lower temperatures is theoretically better. If all other factors were held constant, then the phase noise would theoretically degrade 6 dB if the VCO frequency was doubled.

Q_L is a critical parameter and discussed much when the objective is to minimize the VCO phase noise. This is measured at the operating frequency and defined as the real ratio of the reactance of the inductor divided by its resistance. Ideally, the resistance of the inductor should be zero and Q_L should be infinite, but this is never the case since there will always be some resistance in the inductor. Just as friction stops the motion of the pendulum, the resistance in the inductor damps the oscillation of the tank circuit. A considerable amount of time spent optimizing phase noise in VCOs involves trying to get as high of a Q_L factor as possible. The Q factor of the inductor goes down considerably as it is loaded, so one must be sure to use the loaded Q for Lesson's Equation.

Full Phase Noise Model

The full phase noise model also accounts for the noise contribution due to the resistance of the varactor diode in the $1/f^2$ region as well as adding a $1/f^3$ region and flat region. The formula below is an expanded version of Lesson's equation that shows the phase noise in all three regions [1].

$$L(f) = 10 \cdot log\left(\frac{1}{2}\left[\left(\frac{f_{VCO}}{2 \cdot Q_L \cdot f}\right)^2 + 1\right] \cdot \left[\frac{f_{1/f^3}}{f} + 1\right] \cdot \left[\frac{F \cdot k \cdot T}{P}\right] + \frac{2 \cdot k \cdot T \cdot R_{var} \cdot {K_{VCO}}^2}{f^2}\right) \quad \textbf{(22.2)}$$

f_{1/f^3} = $1 / f^3$ noise (flicker noise) corner frequency

R_{var} = Noise resistance of the varactor diode

The noise in the $1/f^3$ and $1/f^2$ regions degrades at higher output frequencies and lower Q_L factors in a 20 log sense. In other words, if the output frequency is doubled, the noise in these regions degrades 6 dB. Also, in the $1/f^2$ region, there is an additional term that contains K_{VCO}. What this implies is that the noise resistance of the varactor diode becomes relevant at higher VCO gains. Making the VCO gain smaller will improve the phase noise, but at some point, the other term becomes dominant, and there are diminishing returns.

Practical Modeling of Oscillator Noise

A Simple Method for Modeling Oscillator Noise

The full phase model can be approximated in three different regions and can be re-stated as:

$$L(f) = 10 \cdot log\left(N3 \cdot \left(\frac{f_{default}}{f}\right)^3 + N2 \cdot \left(\frac{f_{default}}{f}\right)^2 + N0\right) \quad \textbf{(22.3)}$$

$$N3 = \frac{1}{f^3} \text{ Noise Coefficient} = \frac{F \cdot k \cdot T}{P} \cdot \frac{f_{1/f^3} \cdot {f_{VCO}}^2}{8 \cdot {Q_L}^2 \cdot {f_{default}}^3} \quad \textbf{(22.4)}$$

$$N2 = \frac{1}{f^2} \text{ Noise Coefficient} = \frac{F \cdot k \cdot T}{P} \cdot \frac{{f_{VCO}}^2}{8 \cdot {Q_L}^2 \cdot {f_{default}}^2} + \frac{2 \cdot k \cdot T \cdot R_{Var}}{{f_{default}}^2} \quad \textbf{(22.5)}$$

$$N0 = VCO\ Noise\ Floor = \frac{F \cdot k \cdot T}{P} \quad \textbf{(22.6)}$$

$$f_{default} = Normalized\ Offset\ for\ Phase\ Noise \quad \textbf{(22.7)}$$

One simple way to model a VCO is to measure it and try to fit a model to all three regions of the VCO. The tricky part is that it is very possible that noise sources from more than one region are contributing to noise at a particular point. For this strategy, one measures the phase noise at three strategic points. The first one should be targeting the $1/f^3$ region, the second one should be targeting the $1/f^2$ region, and the third one should be far out in the flat region.

Application of Model to Measured Phase Noise

Consider that the following data is taken at a frequency of f_{VCO} and modeled.

Phase Noise	Phase Noise Offset	Region Targeted	Typical Offset
$p3 = 10^{P3/10}$	f3	$1/f^3$	1 kHz
$p2 = 10^{P2/10}$	f2	$1/f^2$	100 kHz
$p0 = 10^{P0/10}$	f0	Flat	40 MHz

Table 22.1 *Phase Noise Measurements*

It will save a lot of work in the future if the units are converted to scalar units, as they are done in the table. The first thing to do is check the slope between P3 and P2. This slope should be less than 30, but more than 20. If it is more than 30, then this noise model will not work close in. If it is within measurement error of 30, then both points are on the $1/f^3$ slope. If it is less than 20, then none of the points are on the $1/f^3$ slope.

$$\frac{P2 - P3}{log\left({f2}/{f3}\right)} \tag{22.8}$$

The second thing to do is to check the slope between P2 and P0. This slope should be less than 20, but more than 0. If it is more than 20, then one of these points is on the $1/f^3$ slope. If it is equal to 20, then both points are on the $1/f^2$ slope. If it is zero, clearly both measurements are on the floor.

$$\frac{P2 - P0}{log\left({f2}/{f0}\right)} \tag{22.9}$$

Once it is know what slope the points are on, then this leads to a system of at most 3 equations and unknowns. The equations are as follows:

$$p3 = n3 \cdot \left(\frac{f_{default}}{f3}\right)^3 + \mathrm{n2} \cdot \left(\frac{f_{default}}{f3}\right)^2 + \mathrm{n0} \quad \textbf{(22.10)}$$

$$p2 = n3 \cdot \left(\frac{f_{default}}{f2}\right)^3 + \mathrm{n2} \cdot \left(\frac{f_{default}}{f2}\right)^2 + \mathrm{n0} \quad \textbf{(22.11)}$$

$$p0 = n3 \cdot \left(\frac{f_{default}}{f0}\right)^3 + \mathrm{n2} \cdot \left(\frac{f_{default}}{f0}\right)^2 + \mathrm{n0} \quad \textbf{(22.12)}$$

Now it may be the case that one or more of these equations is redundant and can be ignored. In the case that an equation is ignored, then one of the noise coefficients will be zero, and the work will be simplified. Complex values can occur for ***n0***, ***n2***, or ***n3*** if the VCO being modeled does not fit the assumptions of the model.

A simplifying assumption that can be applied is that the noise floor and the $1/f^3$ noise will not be acting on the same point. Furthermore, it seems to reduce the occurrences of getting complex values for ***n3***, ***n2***, and ***n0***. In the case of point ***n2***, one doesn't know which one of these two sources is acting there, so all terms have to be left in. Using this assumption, this can be reduced to the following matrix equation that has the following solution:

$$\begin{bmatrix} n3 \\ n2 \\ n0 \end{bmatrix} = \begin{bmatrix} \left(\frac{f_{default}}{f3}\right)^3 & \left(\frac{f_{default}}{f3}\right)^2 & 0 \\ \left(\frac{f_{default}}{f2}\right)^3 & \left(\frac{f_{default}}{f2}\right)^2 & 1 \\ 0 & \left(\frac{f_{default}}{f0}\right)^2 & 1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} p3 \\ p2 \\ p0 \end{bmatrix} \quad \textbf{(22.13)}$$

$$N3(f) = 10 \cdot log\left[\frac{n3 \cdot \left(\frac{f_{default}}{f}\right)^3}{10}\right] \quad \textbf{(22.14)}$$

$$N2(f) = 10 \cdot log\left[\frac{n2 \cdot \left(\frac{f_{default}}{f}\right)^2}{10}\right] \quad \textbf{(22.15)}$$

$$N0 = 10 \cdot log\left[\frac{n0}{10}\right] \quad \textbf{(22.16)}$$

The $1/f^3$ to $1/f^2$ corner point is where these two noise sources contribute equally and can be calculated as follows:

$$f_{Corner3} = f_{default} \cdot \frac{n3}{n2} \quad \textbf{(22.17)}$$

The $1/f^2$ to phase noise floor corner point, which is where these two noise sources contribute equally, can be calculated as follows:

$$f_{CornerF} = f_{default} \cdot \sqrt{\frac{n2}{n0}} \quad \textbf{(22.18)}$$

This model gives an excellent match to measured results. It was applied to a VCO at 2.7 GHz output frequency using the values of N3 = -157 dBc/Hz, N2 = -147 dBc/Hz, and N0 = -164 dBc/Hz and the result is Figure 22.1.

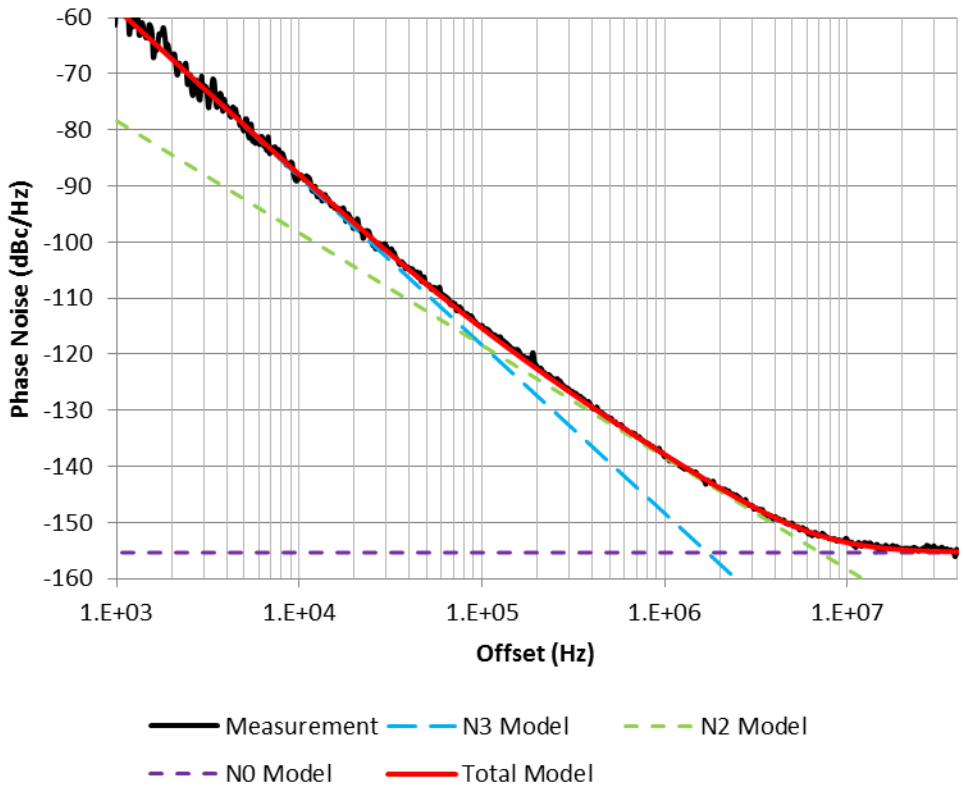


Figure 22.1 *Application of Oscillator Noise to Measured Data*

Conclusion

The phase noise of oscillators, whether it is for a crystal or VCO, typically falls into one of three categories. The $1/f^3$ noise changes 30 dB/decade, the $1/f^2$ changes 20 dB/decade, and the noise floor is flat. By understanding oscillator noise in this way, metrics can be created by normalizing these noise metrics to carrier frequency and offset and the noise can be analyzed and modeled better.

References

[1] Carlini, Jim *A 2.45 GHz Low Cost, High Performance VCO* Microwave Journal April 2000

Chapter 23 Phase Noise of Input Path, Charge Pump, and Dividers

Introduction

The phase noise of the input path, N divider, and charge pump may all be independent, but they may all be grouped together as their noise behaves in a similar way and is also shaped in a similar way by the PLL loop. This chapter studies these noise sources under the assumption that the input reference is noiseless and the loop bandwidth is infinite. Once this is understood, then the appropriate shaping due the transfer function can be applied.

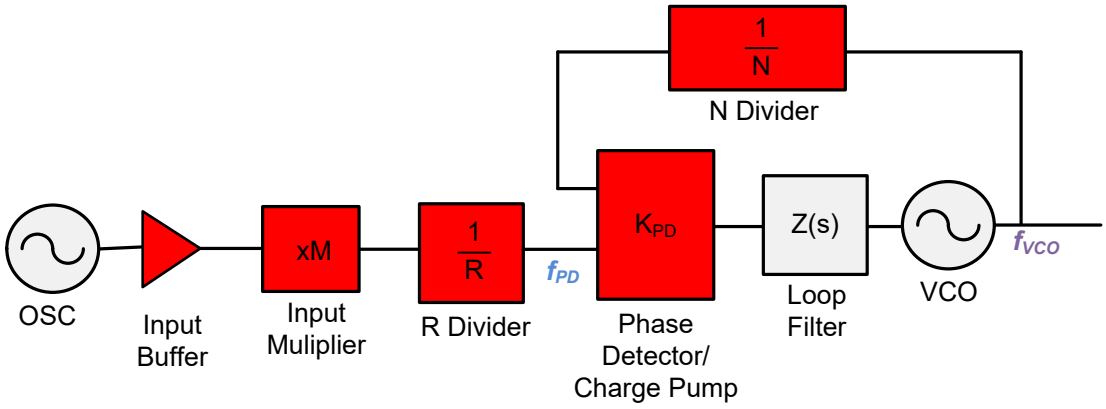


Figure 23.1 *Noise Blocks in the PLL*

The noise transfer functions for these blocks with an infinite loop bandwidth would be as follows:

Source	Transfer Function
Input Buffer	$20 \cdot log(N) + 20 \cdot log(M/R)$
Input Multiplier	$20 \cdot log(N) + 20 \cdot log(1/R)$
R Divider	$20 \cdot log(N)$
N Divider	$20 \cdot log(N)$
Phase Detector/Charge Pump	$20 \cdot log(N) - 20 \cdot log(K_{PD})$

Table 23.1 *Infinite bandwidth transfer functions for various parts of the PLL*

Understanding Correlated and Uncorrelated Error at the Charge Pump Output

There are several blocks in the PLL that can contribute to the noise, but in the final analysis, the noise of all these blocks can be thought of as what noise they contribute at the charge pump output, so the first step is to focus on this.

In the locked condition, the charge pump puts out a pattern with alternating pulses of current as shown in Figure 23.2. The width of these pulses translates to phase detector spurs that have already been discussed in a previous chapter.

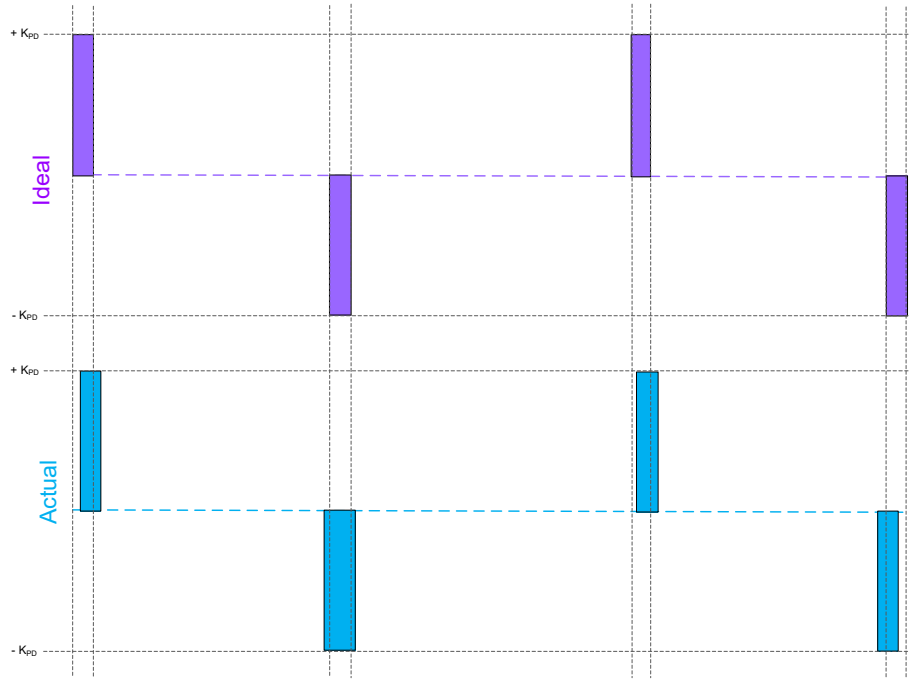


Figure 23.2 *Ideal vs. Actual Charge Pump Output*

Figure 23.4 shows that it is not the width, but the error between the ideal and actual output of the charge pump that determines the phase noise. If the width of one pulse is related to the width of an adjacent pulse, then this noise is said to be *correlated*. On the other hand, if it is completely independent, then it is said to be *uncorrelated*. These error pulses are typically a combination of correlated and uncorrelated noise, which translates to the flicker and flat noise of the PLL. The PLL noise of the charge pump and counters typically can be modeled as a 1/f noise and a flat noise. The 1/f noise is typically correlated and the flat noise is typically uncorrelated.

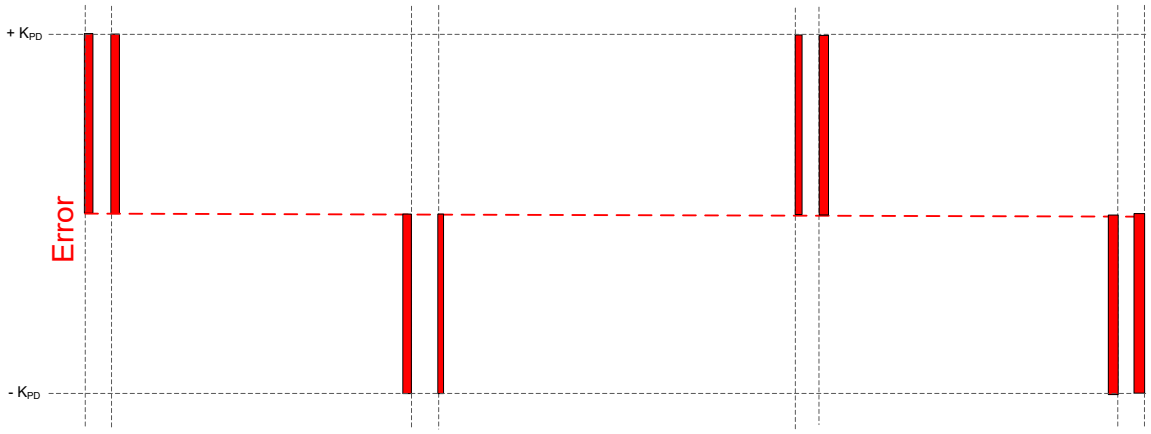


Figure 23.3 *Error Translated to the Charge Pump Output*

Defining PLL Flat and Flicker (1/f) Noise

For earlier integer PLLs and lower phase detector frequencies, it was sufficient to model PLL noise as just flat white noise. However, with the coming of higher phase detector frequencies the flicker noise of the PLL has become a much larger consideration. The flicker noise has a characteristic of decreasing 10 dB/decade and the flat noise tends to show up lower offset frequencies if the reference is sufficiently clean and if the phase detector rate is sufficiently high. The total PLL noise is the resultant of the flat and 1/f noise as shown in Figure 23.4. At offsets below 1 kHz, there is also some contribution from the input reference.

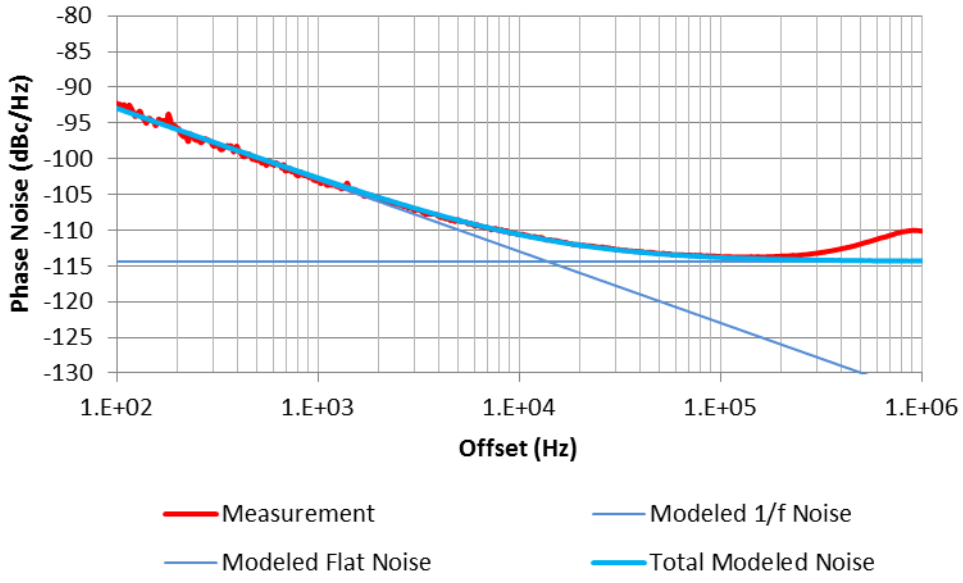


Figure 23.4 *Modeled PLL Noise vs. Measurement for the LMX2541*

Figure 23.4 shows the phase noise of the Texas Instruments LMX2541 delta sigma PLL measured at 3.74 GHz output frequency and a 100 MHz phase detector frequency. The loop bandwidth for this measurement was around 500 kHz, so this phase noise is all in-band. Note how the 1/f and flat noise sum together to add to the total noise

Properties of PLL Flat Noise

Improves as 10·log(f_{PD}) for Fixed VCO Frequency

The flat noise improves with higher phase detector frequencies. The reason is that current error pulses for the flat noise are uncorrelated, which means that their noise power adds in an RMS sense. Consider the impact of increasing the phase detector by a factor two while keeping the VCO frequency the same. The N divider is therefore half and this corresponds to a 6 dB improvement, but the phase detector noise increase by a factor of square root of two which is 3 dB. So the net improvement is only 3 dB.

Degrades as 10·log(N) with Higher N Divider Values and Fixed VCO Frequency

Although increasing the N divider by a factor of $\boldsymbol{K}$ increases the noise multiplication by 20·log($\boldsymbol{K}$), it also decreases the phase detector frequency by a factor of 10·log($\boldsymbol{K}$), so the net degradation is 10·log($\boldsymbol{N}$). Another way of stating this rule is that doubling the phase detector improves the PLL flat noise by a factor of 3 dB.

Increases with VCO Frequency

The PLL flat noise typically increases as 20·log($\boldsymbol{f_{VCO}}$) with the VCO frequency provided that the phase detector frequency is the same. This is due to the larger N multiplication value. Unlike the flicker noise, it does change if the phase detector frequency is simultaneously changed.

Sometimes Degraded by Input Multipliers

When PLL input multipliers are used and the phase detector frequency is not changed, the PLL flat noise is typically degraded and often the flicker noise degradation is less noticeable. One way to measure this is to engage the input multiplier and then increase the R divider by the same factor so as to keep the same frequency. This is typically not a good practice for optimizing phase noise, but a good diagnostic method.

Properties of PLL Flicker Noise

Has 10 dB/decade Slope and How to Distinguish from Input Reference Noise

For test purposes, the 1/f noise is typically measured by choosing a high PLL phase detector frequency, wide loop bandwidth, and using an ultra-low noise crystal oscillator of fixed frequency. Flicker noise that has a characteristic of decreasing as 10 dB/decade with the offset frequency. This property is very helpful in distinguishing the 1/f noise of the PLL from the input reference noise because the input reference noise typically decreases at a much faster rate (closer to 20/dB/decade). It is very often the case when using signal generators, even those claiming to be low noise, that the signal generator noise is higher than the PLL 1/f noise.

Independent of Phase Detector Frequency

Perhaps the most surprising property is that the flicker noise does not improve with higher phase detector frequencies. A way to reason this is consider increasing the phase detector by a factor of ***M*** while keeping the VCO frequency the same. Indeed the N divider is less by a factor of *M* and there is a 20·log(*M*) improvement in this aspect. However, since the noise is correlated, there is also a 20·log(*M*) increase in the noise itself before the multiplication because there are ***M*** times more pulses. So the net effect is the 1/f noise is independent of phase detector frequency as shown in this example from the Texas Instruments LMX2485 PLL.

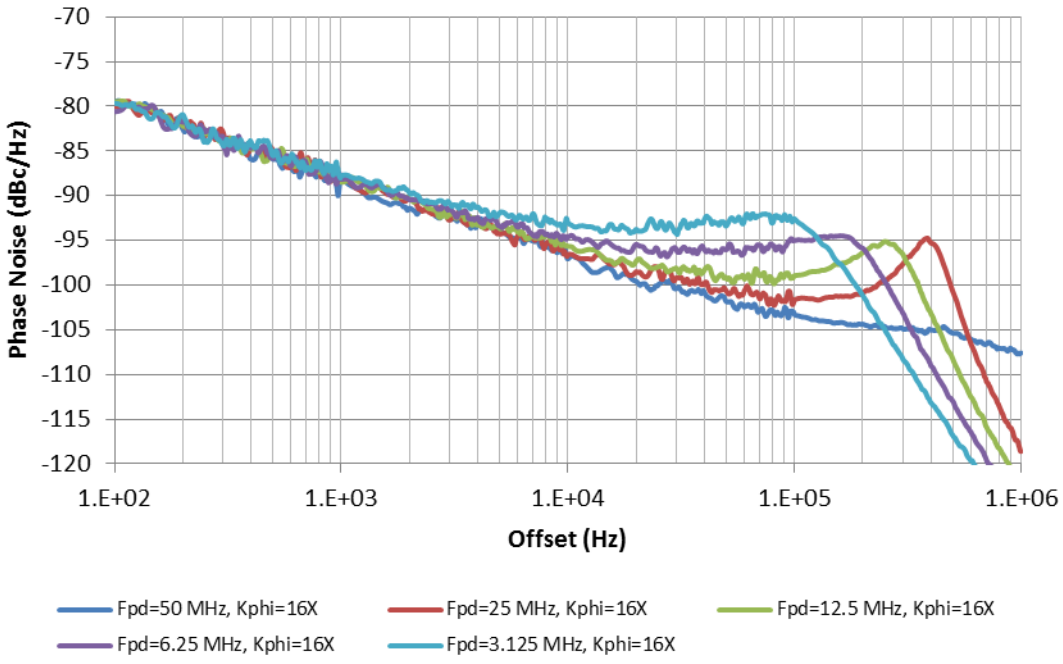


Figure 23.5 *Independence of 1/f noise and Phase Detector Frequency*

Increases with VCO Frequency

The flicker noise typically increases as 20·log(***f_{VCO}***) with the VCO frequency. If the VCO frequency is increased by virtue of a higher phase detector frequency and the same N divider value, it would be higher due to higher noise of the phase detector itself. If the phase detector frequency is held constant and the N divider is increased, the flicker noise increases by virtue of the larger N value. In any case, the flicker noise increases with the higher VCO frequency.

At Some Very Low Offset the Flicker Noise Can No Longer Increase

If one considers the 10·log(Offset) relationship for the flicker noise and calculates the noise power, then theoretically this would be infinite if one goes down to DC. However, this noise must eventually flatten out at sufficiently low offsets, but this point is very low, on the order of less than 1 Hz. An over-simplified but useful way to view this is that any noise below 1 Hz is considered to be the carrier.

Modeling of the PLL Noise

Modeling PLL Flat Noise

The PLL flat noise increases as 20·log(***f_{PD}***) and 10·log(***f_{PD}***). It therefore makes sense to derive a metric that does not vary with these parameters. This metric has been called the PLL figure of merit and also the 1 Hz Normalized PLL noise floor (PN1Hz). This metric is device specific and always modeled with the highest charge pump current of the device. From this metric, the PLL flat noise can be modeled as follows:

$$PLLnoise_{flat} = \text{PN1Hz} + 10 \cdot \log\left(\frac{f_{PD}}{1Hz}\right) + 20 \cdot \log(N) \qquad \textbf{(23.1)}$$

Modeling of the PLL 1/f Noise

For frequencies less than some offset, the 1/f noise needs to be taken into consideration. In general, this noise decreases by 10 dB/decade and a simple way to characterize this is to normalize it to 10 kHz offset frequency and a 1 GHz PLL output frequency, ***PN10kHz***.

$$PLLnoise_{1/f}(f_{OUT}, offset) = \text{PN10kHz} + 20 \cdot \log\left|\frac{f_{OUT}}{1GHz}\right| - 10 \cdot \log\left|\frac{offset}{10kHz}\right| \qquad \textbf{(23.2)}$$

Other Interpretations of PLL Flat and Flicker Noise

1/f Corner Frequency

One common frequency of interest is the offset where the flat and flicker noise cross, often called the corner frequency. This frequency be can easily calculated, but it is not constant and will move with the phase detector frequency. At this offset, the PLL flat noise will be degraded by 3 dB. At twice this offset, the PLL flat noise will be degraded by 1.8 dB. At four times this offset, the PLL flat noise will be degraded by about 1 dB. This crossover frequency can be calculated by equating the PLL flat noise to the PLL 1/f noise and solving for the offset.

$$Corner\ Frequency = f_{PD} \cdot 10^{-14} \cdot 10^{(PN10kHz - PN1Hz)/10} \quad \textbf{(23.3)}$$

Another Interpretation of 1/f Noise -- f_{PD}Knee

If one considers a fixed offset frequency and PLL output frequency and increases the phase detector frequency, the phase noise seems to improve to a point and then reach diminishing returns. The f_{PD}Knee frequency can be used to describe the point where raising the phase detector from this value to infinity would cause a 3 dB theoretical improvement in phase noise. This can be calculated from the normalized flicker noise and PLL figure of merit as follows:

$$PN10kHz + 10 \cdot \log\left|\frac{10kHz}{Offset}\right| = \text{PN1Hz} + 10 \cdot \log\left|\frac{f_{PD}Knee}{1Hz}\right| + 20 \cdot \log\left|\frac{1\ GHz}{f_{PD}Knee}\right| \quad \textbf{(23.4)}$$

Factors Impacting 1/f Noise and PLL Flat Noise

Impact of Charge Pump Gain

If the PLL noise is dominated by the charge pump, then increasing the charge pump gain can sometimes improve it. On the other hand, if the charge pump gain has no impact on the PLL noise, then this typically implies that it is dominated by the input path or dividers. The theoretical reasoning for this is that the charge pump noise is theoretically divided by the charge pump gain. The key caveat for this is that increasing the charge pump gain typically increases the noise of the charge pump itself, so it really can depend how the charge pump gain is increased. If the charge pump gain increase is implemented by a simple multiplication, then this typically does not improve the noise because this multiplies the noise by the same amount. In other charge pumps, the higher current is implemented by adding more current sources in parallel. If this is the case, then the noise is uncorrelated and this theoretically leads to a three dB/decade increase for every doubling of the charge pump gain.

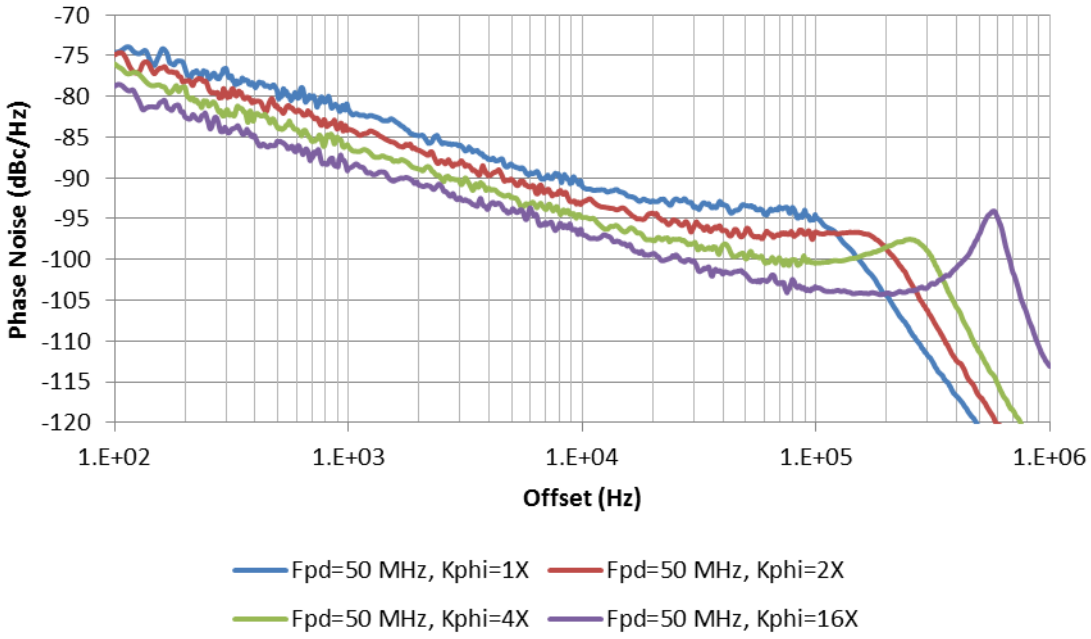


Figure 23.6 *Impact of Charge Pump Current on Flicker Noise*

Figure 23.6 shows the impact of changing the charge pump gain of the LMX2485 PLL while keeping the phase detector frequency constant at 50 MHz using the same setup that was used as was used in Figure 23.5. As the charge pump is the only noise source that has its phase noise theoretically divided by the charge pump gain, one can conclude that the charge pump itself is the dominant source of the 1/f noise as this is the only contributor that has phase noise that is divided by the charge pump gain. It is generally best to use the highest charge pump gain for the best phase noise unless the loop filter capacitors become undesirably large, the higher current is needed for Fastlock or to compensate for VCO gain differences, or a point of diminishing returns for phase noise has been achieved.

Modeling the Impact of Charge Pump Gain on PLL Phase Noise

Depending on the charge pump architecture, increasing the charge pump can help to a point until diminishing returns is reached, which can be described as ***K_{PD}Knee***. If the charge pump current has no impact on phase noise, then this term is zero. Otherwise, it can be thought of the current that theoretically has phase noise worse than an infinite charge pump current. As the highest charge pump current (***K_{PD}Max***) almost always has the best PLL noise, the noise at other charge pump currents can be modeled as follows:

$$PLL_{Noise}(K_{PD}) = \text{PLL\_Noise}(K_{PD}Max) + 10 \cdot \log\left|\frac{K_{PD}Max}{K_{PD}} \cdot \frac{K_{PD} + K_{PD}Knee}{K_{PD}Max + K_{PD}Knee}\right| \quad \textbf{(23.5)}$$

Crosstalk in Dual PLLs

In the dual PLL, it has been found that the optimal phase noise performance is when the other side of the PLL is unused, powered down, and with no VCO connected. Table 23.2 assumes that the other PLL is powered down with its corresponding VCO running. If the actual case is that the other PLL is powered down with no VCO running, this typically results in about a 2 dB improvement in phase noise. If the other PLL is powered up with the VCO running, this typically results in a 1-2 dB degradation from what the table predicts.

Impact of Input Reference Slew Rate on PLL Phase Noise

PLL phase noise often improves with higher input slew rates if it is dominated by the input path. The reason is that the higher slew rates give higher immunity to the noise of the input buffer and R divider. If the R divider is the dominant cause of the PLL noise, then improving the slew rate by a factor of two will improve the flicker noise by about 6 dB. However, at some point, increasing the slew rate no longer improves the noise. The Texas Instruments LMX2541 datasheet has curves that show this. For the purposes of modeling the PLL noise, it is typically assumed that the slew rate is very high and not an issue.

Just as a high slew rate is good for phase noise, a poor slew rate can be bad for dividers. When the input signal is of low frequency or low amplitude, this leads to a lower slew rate. This lower slew rate lowers the noise immunity of the counters and can cause the PLL phase noise to degrade.

Accounting for Input Multipliers in the Input Path

Some PLLs have doublers or multipliers in the input path and the natural question is to wonder how to model this phase noise. For instance, if the input doubler is very low noise, there are some cases where engaging this can actually be used to improve the 1/f noise of the PLL; this is an indication that this flicker noise is due to the input path and not the charge pump. For other input path frequency multipliers, they can add noise and the best way to model this is as degradation in the figure of merit of the PLL.

Spectrum Analyzer Correction Factors

Most modern spectrum analyzers account for correction factors for measuring phase noise. However, some older ones require the user to subtract away the resolution bandwidth (RB) of the instrument as follows:

$$True\ Phase\ Noise = Measured\ Phase\ Noise + 10 \cdot log\left(\frac{RB}{1Hz}\right) \quad \textbf{(23.6)}$$

However, this method is not entirely correct. Spectrum analyzers have a correction factor that is added to the phase noise to account for the log amplifier in the device and minor errors caused due to the difference between the noise bandwidth and the 3 dB bandwidth. This correction factor is in the order of about 2.5 dB. Many spectrum analyzers have a

function called “Mark Noise”, which does account for the spectrum analyzer correction factors. The part-specific numbers for phase noise derived in this chapter do not account for the correction factor of the spectrum analyzer, and are therefore optimistic by about 2 dB. Numbers reported in this chapter account for spectrum analyzer correction factors.

Accounting for Fractional N Dividers

A natural question to ask is how fractional N PLL noise differs from integer PLL noise. The answer to this is it depends on the nature of the noise. The three most common ways this can impact the PLL phase noise and the way it is modeled are: (1) PLL Noise is not degraded at all, (2) PLL Figure of Merit is degraded, or (3) Fractional noise is created that is independent of other PLL noise. The specific scenario that applies to each case can be specific to the fractional PLL used and also the way it is configured and these three scenarios are discussed in the following sections.

Case 1: Fractional Division does not Degrade PLL Noise

In some cases, the use of a fractional N value does not degrade the phase noise at all. This can often be the case when the fraction is not well randomized and dithering is disabled. For instance, if one uses a fraction of 3/10 with a first order modulator, often there will be no degradation in the phase noise at all, just fractional spurs. For some fractional PLLs that have a fixed fractional denominator, sometimes this forces a simple fraction to be well-randomized, which is harmful to the PLL noise.

Case 2: Fractional Division Degrades the PLL Figure of Merit

There are many fractional PLLs that specify the phase noise figure of merit for both integer and fractional mode. In these cases, the close-in fractional noise will vary as a function of the phase detector frequency. Hypothetically, this can be thought of as the noise of the N divider being degraded by the fractional noise, or perhaps it could be due to the addition of the fractional compensation circuitry.

Case 3: Fractional Division Creates a New Independent Noise Floor

In the cases that the fraction is well-randomized, the fractional PLL will actually create a family of many fractional spurs that are very close together that appear to be phase noise on a spectrum analyzer or phase noise analyzer. This close-in phase noise is impacted by the modulator order, but does not change much with phase detector frequency or VCO frequency. Furthermore, at farther out frequencies that are closer to the phase detector frequency, there is a large amount of phase noise, but this can be filtered out by the loop filter. The following example shows a LMX2485 PLL with a 10 MHz phase detector rate and 237 kHz 2nd order loop filter. This was done with a fraction of 1/4194303 with strong dithering. The roll-off of the loop filter was subtracted away from the raw measurement to find the unshaped PLL.

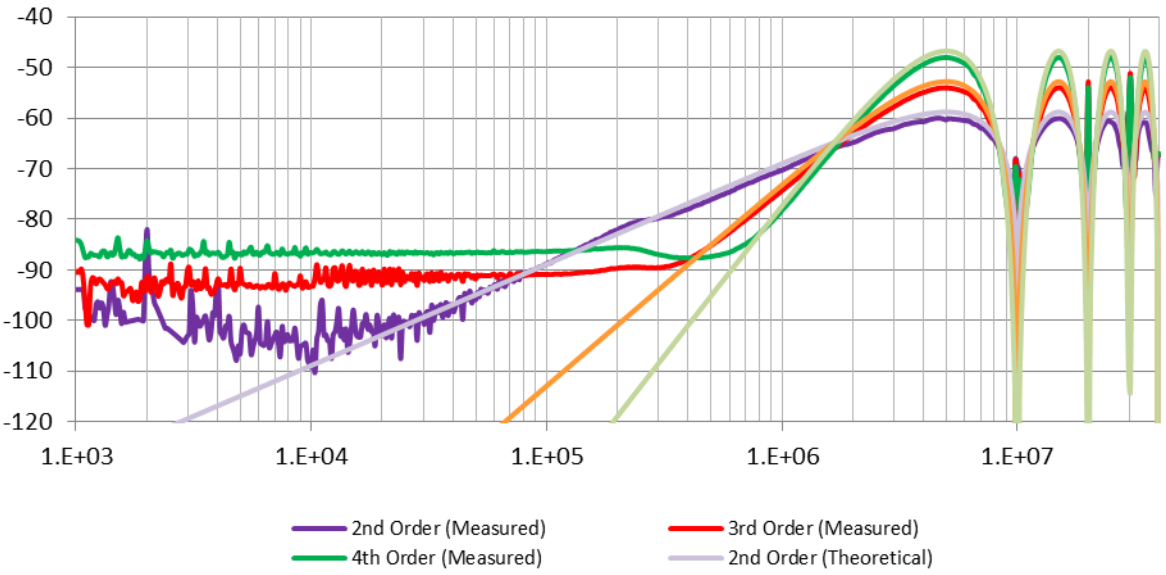


Figure 23.7 *Measured Delta Sigma Modulator Noise*

Comparing the measurements to the theoretical data, there is excellent agreement except at very low frequencies. At these low frequencies, there was also a flat noise floor. In general, experiments show that there is no consistent trend for this noise for a particular modulator order, phase detector frequency, or dithering mode. In this case as shown in Figure 23.7, the quantization noise was well randomized and the assumption that it is a uniformly distributed random variable between 0 and 1 holds. This is why there is such nice agreement. The mathematics behind the modeling this noise is given in the appendix.

Phase Noise Constants for Various Texas Instruments PLLs

Table 23.2 gives typical phase noise metrics for various Texas Instruments PLLs. These measurements were taken with a wide loop bandwidth and an ultra-clean input source to ensure that this was due to the device, not the input or VCO. To simplify the table, devices within a family are considered to have the same metrics. For instance, the LMX2485E, LMX2485Q-Q1, LMX2485, LMX2486, LMX2487, and LMX2487E are all members of the LMX2485 family. For dual PLLs, there is a side column to distinguish both sides. K_{PD}Max and K_{PD}Knee can be used to adjust the figure of merit (FOM) and normalized 1/f metric (PN10kHz) using (23.5). For fractional devices, the strongly dithered phase noise is given for a 2^{nd}, 3^{rd} and 4^{th} order modulator. It is important to understand that all of these fractional devices allow dithering to be disabled and can also be used with simple fractions. In this case, there is no fractional noise added, just fractional spurs.

PLL		Integer Noise Metrics				Fractional Noise Metrics		
Device	***Side***	***K_{PD}Max (mA)***	***K_{PD}Knee (mA)***	***FOM (dBc/Hz)***	***PN10kHz (dBc/Hz)***	***2^{nd} Order***	***3^{rd} Order***	***4^{th} Order***
LMX2306 Family	Main PLL	1	1.0	-208.0	-86.1	n/a	n/a	n/a
LMX2430 Family	RF PLL	4	0.0	-217.8	-99.6	n/a	n/a	n/a
	IF PLL	4	0.0	-217.8	-99.6			
LMX2470 Family	RF PLL	4	0.0	-210.0	-99.6	n/a	n/a	n/a
	IF PLL	4	0.0	-209.0	-99.6			
LMX2485 Family	RF PLL	1.6	0.4	-215.8	-104.6	-100.0	-95.0	-90.0
	IF PLL	1.6	0.0	-210.0	-107.5	n/a	n/a	n/a
LMX2491/92	Main PLL	3.1	1.2	-227.0	-120.0	-100.0	-95.0	-90.0
LMX2531 Family	Main PLL	1.6	2.0	-212.0	-104.0	-100.0	-95.0	-90.0
LMX2541 Family	Main PLL	3.1	0.4	-225.9	-124.9	-100.0	-95.0	-90.0
LMX2571	Main PLL	1.25	0.1	-231.0	-124.0	none	-99.0	-96.0
LMX2581	Main PLL	3.1	0.4	-230.8	-122.6	-107.1	-103.8	-97.7
LMX2582/92	Main PLL	4.8	0.5	-231.0	-126.0	none	-99.0	-99.0

Table 23.2 *PLL Noise Metrics for Various Texas Instruments PLLs*

Conclusion

This chapter has investigated the causes of PLL phase noise and has provided a somewhat accurate model of how to predict it. Within the loop bandwidth, the PLL phase detector is typically the dominant noise source, and outside the loop bandwidth, the VCO noise is often the dominant noise source. It is reasonable to expect a +- 0.5 dB measurement error when measuring phase noise. Phase noise can vary from board to board and part to part, but typically this variation is in the order of a few dB.

References

[1] White, Peter *Understanding Phase Noise from Digital Components in PLL Frequency Synthesizers* Applied Radio Labs Design File DN006 December 2000

[2] The author would like to specially thank Ian Thompson for useful discussions regarding the impact of phase detector frequency on the PLL noise floor, which relevant to the PLL figure of merit.

[3] *Phase noise Measurement of PLL Frequency Synthesizers* Texas Instruments Application Note 1052

[4] Perrot, H.H, M.D.Trott, G.G.Sodini "A Modeling Approach for a D-S Fractional-N Frequency Synthesizers Allowing Straightforward Noise Analysis" IEEE Journal of Solid_State Circuits, Vol 37, No. 8, August 2002

Appendix

Theoretical Delta Sigma PLL Phase Noise

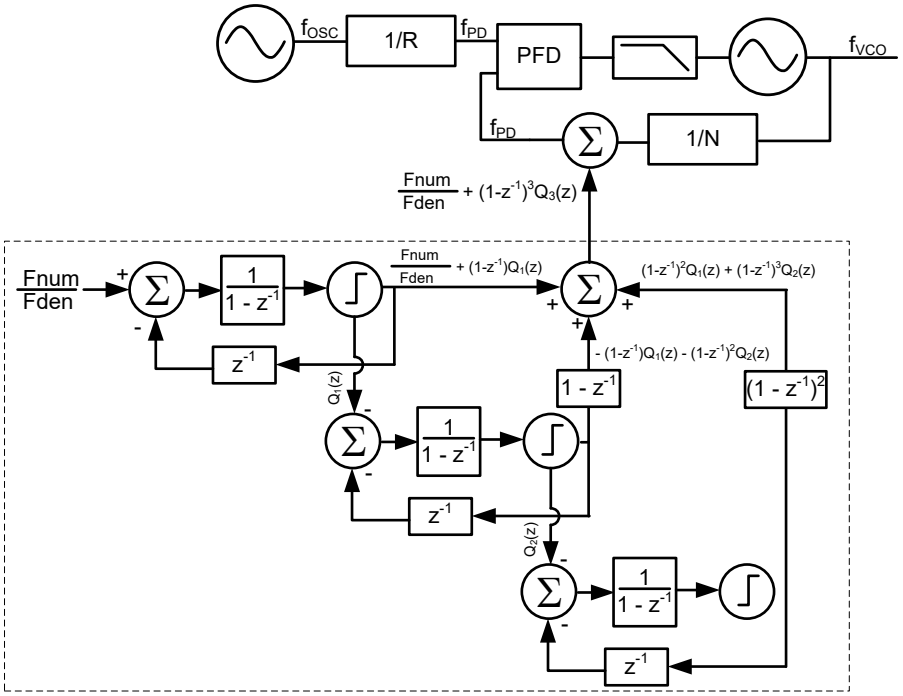


Figure 23.8 *Third Order Delta Sigma Modulator*

Figure 23.8 shows that the quantization noise from all stages except for the last is canceled out. Also, whether the quantization noise is positive or negative makes no impact on the spectrum. That being said, the output of an n[th] order delta sigma modulator is therefore:

$$Y(z) = \frac{Fnum}{Fden} + h(z) \cdot (1 - z^{-1})^n \cdot Q_n(\mathrm{z}) \qquad \textbf{(23.7)}$$

Reference [2] discusses that there are additional factors that arise because the N counter is not constant and the phase detector is actually only on at discrete times. Comparing this result to those in reference [2] show that this unexplained factor of h(z) is as follows:

$$h(z) = 2\pi \cdot \frac{z^{-1}}{1 - z^{-1}} \cdot \frac{1}{f_{PD}} \qquad \textbf{(23.8)}$$

What is of interest is the output spectrum of this delta sigma modulator. To transform from the z domain to the frequency domain, use the following transform:

$$z = e^{s \cdot T} = e^{2\pi \cdot f \cdot t} = \mathrm{e}^{2\pi \cdot \left(\frac{f}{f_{PD}}\right)} \tag{23.9}$$

A handy identity to know is that:

$$\begin{aligned} &\left\|1 - e^{j \cdot x}\right\| = \|1 - \cos(x) - j \cdot \sin(x)\| = (1 - \cos(x))^2 + \sin^2(\mathrm{x}) \\ &= 1 - 2 \cdot \cos(\mathrm{x}) + \cos^2(\mathrm{x}) + \sin^2(\mathrm{x}) = 2 \cdot (1 - \cos(x)) \\ &= 2 \cdot \sin^2\left(\frac{x}{2}\right) \end{aligned} \tag{23.10}$$

Applying the transform and identities yields [2]:

$$Y_{Noise}(f) = (2\pi)^2 \cdot \left(2 \cdot sin\left(\frac{\pi \cdot f}{f_{PD}}\right)\right)^{2 \cdot (n-1)} \cdot \left\|\frac{Q_n(2\pi \cdot j \cdot f)}{f_{PD}}\right\| \tag{23.11}$$

The above formula applies to both phase noise and spurs. However, the discussion of the nature of $Q_n(z)$ now needs to be discussed to understand phase noise and spurs. $Q_n(z)$ is simply the output of the n^{th} quantizer minus its input. Because the output of the quantizer can be 0 or 1, this is bounded between (and including) 0 and 1. The spectral density of the quantization noise, q(s) can change based on the fractional word. However, if the fraction is large and the modulator order is 3 or 4, then it is a fair assumption to assume that this is a uniformly distributed random variable between 0 and 1 [2]. The noise power is related to the variance of this random variable which is given as:

$$Variance\{\mathrm{Q}_n\} = \int_0^1 (t - 1/2)^2 \cdot dt = 1/12 \tag{23.12}$$

So for noise, the appropriate function is [2]:

$$Y_{Noise}(f) = (2\pi)^2 \cdot \left(2 \cdot sin\left(\frac{\pi \cdot f}{f_{PD}}\right)\right)^{2 \cdot (order-1)} \cdot \left(\frac{1Hz}{12 \cdot f_{PD}}\right) \tag{23.13}$$

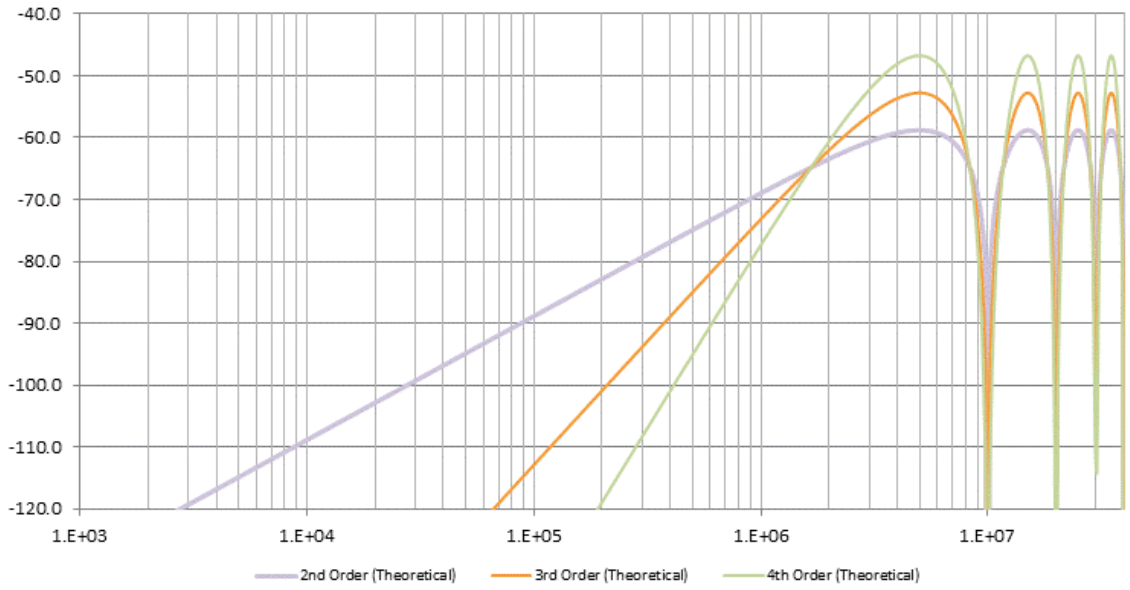


Figure 23.9 *Theoretical Delta Sigma Noise for a 10 MHz Phase Detector Frequency*

From Figure 23.9, note that there is a point at which all the modulators theoretically have the same performance. This can easily be found by setting

$$2 \cdot sin\left(\frac{\pi \cdot f}{f_{PD}}\right) = \pm 1 \qquad \textbf{(23.14)}$$

This implies that this occurs at

$$f = f_{PD} \cdot \left(\frac{1}{6} + \mathrm{k}\right) \qquad \mathrm{k} = 0,1,2,\ldots \qquad \textbf{(23.15)}$$

Of most interest is the case where k=0. Indeed, there are theoretically higher order occurrences, but for these, there are other noise sources that can mask this, and the delta sigma noise tends to be better filtered out anyways for these frequencies. The most interesting occurrence is therefore:

$$f = \frac{f_{PD}}{6} \qquad \textbf{(23.16)}$$

Another frequency of interest is where the unshaped noise peaks in value. This can be found by setting

$$sin\left(\frac{\pi \cdot f}{f_{PD}}\right) = \pm 1 \tag{23.17}$$

This has a solution of:

$$f = \frac{f_{PD}}{2} \cdot (1 + 2 \cdot k) \quad \text{k} = 0,1,2,\ldots \tag{23.18}$$

This result shows that the worst case phase noise is worst case at half the phase detector frequency. Due to the low pass response of the loop filter, it is typically only the first peaking in the phase noise response that is observed. Furthermore, this low pass response typically makes this peaking happen at a frequency slightly less than half the phase detector frequency. The magnitude of the first phase noise peak can be found by substituting this frequency in as is done below:

$$\begin{aligned} PLLnoise_{\Delta\Sigma}\left(\frac{f_{PD}}{2}\right) &= 10 \cdot \log\left[(2\pi)^2 \cdot \left(2 \cdot sin\left(\frac{\pi}{2}\right)\right)^{2\cdot(order-1)} \cdot \left(\frac{1Hz}{12 \cdot f_{PD}}\right)\right] \\ &= 20 \cdot \log(2\pi) + 20 \cdot (\text{order} - 1) \cdot \log(2) - 10 \cdot \log(12) - 10 \cdot \log\left(\frac{1Hz}{f_{PD}}\right) \\ &\approx 6 \cdot \text{order} - 10 \cdot \log\left(\frac{f_{PD}}{1Hz}\right) - 0.8 \end{aligned} \tag{23.19}$$

The theoretical value of this unfiltered first lobe is shown in Table 5.

f_{PD}	2nd Order Modulator	3rd Order Modulator	4th Order Modulator
1.25 MHz	-49.8	-43.8	-37.8
2.5 MHz	-52.8	-46.8	-40.8
5 MHz	-55.8	-49.8	-43.8
10 MHz	-58.8	-52.8	-46.8
20 MHz	-61.8	-54.8	-49.8
40 MHz	-64.8	-57.8	-52.8

Table 23.3 *Magnitude of the First Lobe vs. f_{PD}*

One final property of the delta sigma modulator noise is the slope for lower frequencies of offsets much less than $f_{PD}/2$. At these lower frequencies, sin(x) can be approximated by x and the slope can therefore be approximated as follows.

$$10 \cdot log\left[(2\pi)^2 \cdot \left(2 \cdot sin\left(\frac{\pi \cdot f}{f_{PD}}\right)\right)^{2\cdot(order-1)} \cdot \left(\frac{1Hz}{12 \cdot f_{PD}}\right)\right]$$

$$\approx 20 \cdot (order-1) \cdot log\,(f) + 10 \cdot \log\left[\left(\frac{(2\pi)^2 \cdot 1Hz}{12 \cdot f_{PD}}\right)\left(\frac{2\pi}{f_{PD}}\right)^{2\cdot(order-1)}\right] \qquad \textbf{(23.20)}$$

$$\Rightarrow \quad 20 \cdot (order-1) \;\; db/Decade$$

Based on this slope equation, one commonly stated guideline is that the loop filter order should be one greater than the order of the delta sigma modulator. The reasoning for this rule is this allows the loop filter to roll off the delta sigma noise at a faster rate than it is increasing. If the loop bandwidth is wide relative the phase detector frequency, then this rule has more merit, but it tends to be slightly over-conservative, especially for higher phase detector frequencies. For instance, in the case of a fourth order modulator, it is almost never the case that a fifth order filter is really necessary. Nevertheless, one should be aware that higher order modulators do have increased noise pushed to higher frequencies and in general require higher order loop filters.

Chapter 24 Phase Noise of Passive Loop Filters

Introduction

The passive loop filter contains resistors that can degrade the phase noise at the PLL output due to their thermal noise. Typically this noise shows up at the loop bandwidth of the PLL and is worse for higher resistor values. The general procedure outlined in this chapter for calculating the resistor noise is to multiply the resistor thermal noise voltage by a transfer function to get it to the output and then finally translate this to a phase noise.

Calculating the Resistor Thermal Noise

The voltage due to the resistor, V_X, is easily found as follows:

$$V_x = \sqrt{4 \cdot T_0 \cdot K \cdot Rx} \qquad \textbf{(24.1)}$$

T_0 = Ambient Temperature in Kelvin = 300 Kelvin (typically)
K = Boltzmann's Constant $= 1.380658 \cdot 10^{-23}$ (Joule/Kelvin)
Rx = Resistor Value in Ω

Deriving the Transfer Functions

The first step in deriving the transfer functions is to consider the open loop PLL and find the transfer function that translates the resistor noise to the VCO output. It is easier to break the filter into two sections for analysis and create some commonly used terms and then focus on the specific noise derivations for the resistors of R2, R3, and R4.

Breakdown of the Filter for Analysis

In order to both simplify the analysis and make it more understandable, it makes sense to break the filter down as shown:

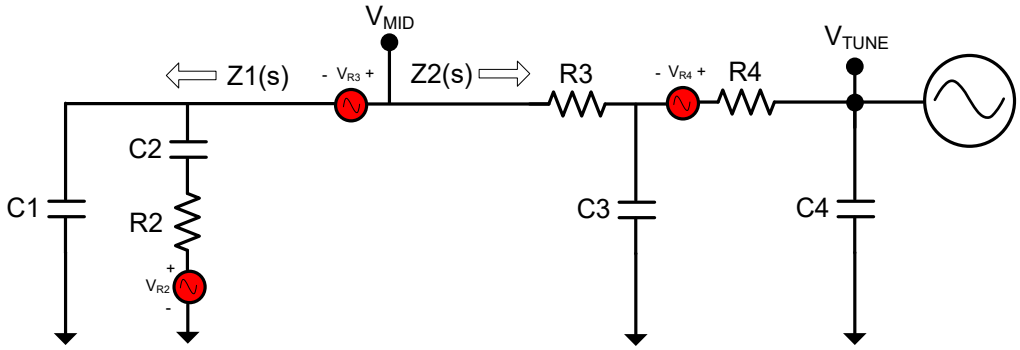


Figure 24.1 *Breakdown of Filter for Resistor Noise Analysis*

In this figure, Z1(s) is the impedance of the loop filter looking from V_{MID} to ground and ignoring the components C3, C4, R3, and R4.

$$\mathrm{Z1(s)} = \frac{1}{s} \cdot \frac{1 + s \cdot C2 \cdot R2}{C1 + C2 + s \cdot C1 \cdot C2 \cdot R2} \tag{24.2}$$

Z2(s) is the impedance as looking from V_{MID} to ground while ignoring the components C1, C2, and R2.

$$\mathrm{Z2(s)} = \frac{1}{s} \cdot \frac{1 + s \cdot (C3 \cdot R3 + C4 \cdot R4 + R3 \cdot C4) + s^2 \cdot C3 \cdot C4 \cdot R3 \cdot R4}{C3 + C4 + s \cdot C3 \cdot C4 \cdot R4} \tag{24.3}$$

A final intermediate function that is very useful is that for a voltage at V_{MID} to V_{TUNE} which is as follows:

$$T_{MID}(\mathrm{s}) = \frac{1}{1 + s \cdot (C3 \cdot R3 + C4 \cdot R4 + R3 \cdot C4) + s^2 \cdot C3 \cdot C4 \cdot R3 \cdot R4} \tag{24.4}$$

R2 Resistor Noise

The situation for the R2 resistor noise looks as follows:

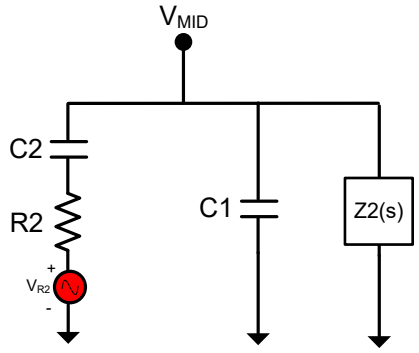


Figure 24.2 *R2 Resistor Noise Analysis*

The noise transfer function to V_{R2} to V_{TUNE} is given in (24.5). Note that in the case of a second order filter, take the limit as Z2(s) = ∞ and the equation can be simplified.

$$\mathrm{T}_{R2}(\mathrm{s}) = \frac{\mathrm{T}_{MID}(\mathrm{s}) \cdot s \cdot C2 \cdot Z2(s)}{1 + s \cdot [C2 \cdot R2 + C1 \cdot Z2(s) + C2 \cdot Z2(s)] + s^2 \cdot C1 \cdot C2 \cdot R2 \cdot Z2(s)} \tag{24.5}$$

R3 Resistor Noise

The situation for the R3 resistor noise looks as follows:

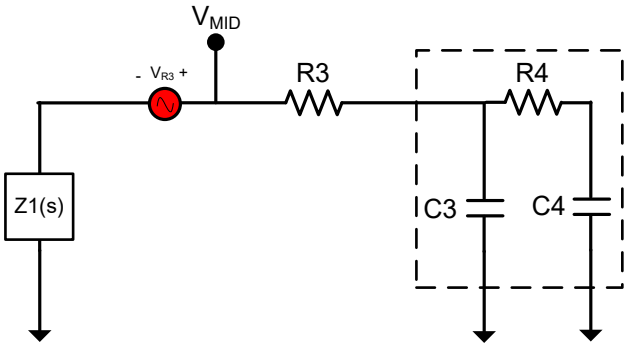


Figure 24.3 *R3 Resistor Noise Analysis*

$$T_{R3}(s) = \frac{T_{MID}(s) \cdot Z2(s)}{Z1(s) + Z2(s)} \qquad \textbf{(24.6)}$$

R4 Resistor Noise

In the situation of the R4 resistor noise, it is easier to derive directly for the V_{TUNE} voltage instead of V_{MID}.

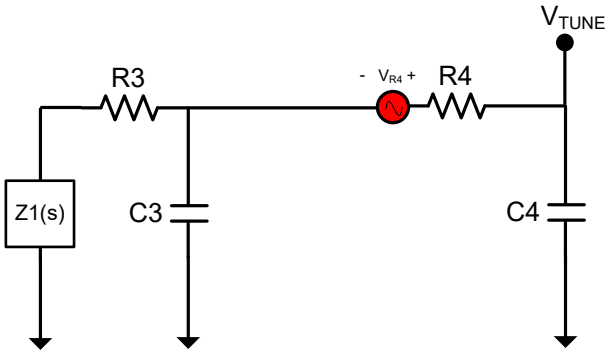


Figure 24.4 *R4 Resistor Noise Analysis*

$$T_{R4}(s) = \frac{1 + s \cdot C3 \cdot \left(R3 + Z1(s)\right)}{1 + s \cdot \left[(C3 + C4) \cdot \left(R3 + Z1(s)\right) + C4 \cdot R4\right] + s^2 \cdot C3 \cdot C4 \cdot R4 \cdot (R3 + Z1(s))} \qquad \textbf{(24.7)}$$

Translating the Noise Voltage to a dBc/Hz number for Phase Noise

This explanation is found in reference listed by Lance Lascari. In a similar way that leakage-based reference spur was shown to relate to the modulation index of the signal, the modulation index is applied here to derive the phase noise.

$$\text{Rx\_Noise(f)} = 20 \cdot \log\left(\frac{\beta(f)}{2}\right) \quad \textbf{(24.8)}$$

The modulation index can be found by multiplying the voltage noise by the VCO gain. Note that it is necessary to multiply the noise voltage by a factor of $\sqrt{2}$ to convert it from an RMS voltage to a peak to peak voltage.

$$\beta(\text{f}) = \frac{f_{DEV}(f)}{f_{MOD}(f)} = \frac{\sqrt{2} \cdot V_{Rx} \cdot K_{VCO}}{f} \cdot \left\| \frac{T_{Rx}(\text{s})}{1 + G(s)/N} \right\|_{s=2\cdot\pi\cdot j\cdot f} \quad \textbf{(24.9)}$$

These formulae can be combined for the final result as follows:

$$\text{Rx\_Noise(f)} = 20 \cdot \log\left(\frac{V_X \cdot K_{VCO}}{\sqrt{2} \cdot f} \cdot \left\| \frac{T_{Rx}(\text{s})}{1 + G(s)/N} \right\|_{s=2\cdot\pi\cdot j\cdot f} \right) \quad \textbf{(24.10)}$$

Conclusion

This chapter has discussed how to calculate resistor noise for loop filter resistors of a passive filter. These concepts will be expanded in the next chapter to also cover active filters.

References

[1] Lascari, Lance *Accurate Phase Noise Prediction in PLL Frequency Synthesizers* Applied Microwave & Wireless Vol.12 No. 5. May 2000

[2] Lascari, Lance *Mathcad PLL Phase Noise Simulation Tool,* http://www.rfdude.com

[3] The author would like to thank Holger Weiss for correcting some errors in the derivations in this chapter.

Chapter 25 Phase Noise of Active Loop Filters

Introduction

The concepts for calculating the phase noise of active filters is very similar to that of passive elements. In fact, the op-amp actually simplifies a lot of the transfer functions and calculations. This being said, the op amp also has the noise voltage and current as well as any resistor noise for biasing circuitry. This chapter discusses these details by first introducing terminology and going through the Active A, Active B, and Active C filters.

Terminology

Symbol	Formula/Description	Units
V_{TUNE}	Noise voltage due to all sources referred to the input of the VCO	$nV/\sqrt{Hz}$
V_{OUT}	Noise voltage at op amp output resulting from op-amp, filter resistors, or bias resistors.	$nV/\sqrt{Hz}$
V_{AMP}	Op-amp noise voltage	$nV/\sqrt{Hz}$
I_{AMP}	Op-amp noise current	$pA/\sqrt{Hz}$
V_{Rx}	$\sqrt{4 \cdot T \cdot k \cdot Rx \cdot B}$	$nV/\sqrt{Hz}$
T	300	K
Rx	Rx could be R1, R2, R3, R4, or Rth	Ω
k	Boltzmann's Constant = 1.380659×10^{-23}	J/K
B	1	Hz
$Z1$	$\frac{1+s \cdot C2 \cdot R2}{s \cdot (C1+C2) \cdot (1+s \cdot T1)}$, $T1 = \frac{R2 \cdot C2 \cdot C1}{C1+C2}$	Ω
$T_{MID}(s)$	$\frac{1}{1 + s \cdot (C3 \cdot R3 + C4 \cdot R4 + R3 \cdot C4) + s^2 \cdot C3 \cdot C4 \cdot R3 \cdot R4}$	none

Table 25.1 *Terms for Active Filter Analysis*

Calculating the Total Phase Noise

The general strategy is to calculate the noise voltage at the output of the op amp, V_{OUT}, and then account for any additional poles in the filter afterwards to find the noise at the VCO input, V_{TUNE}. From this the resulting phase noise calculated using FM Modulation theory.

$$Noise(f) = 20 \cdot \log\left(\frac{V_{TUNE} \cdot K_{VCO}}{\sqrt{2} \cdot f} \cdot \left\| \frac{1}{1 + G(s)/N} \right\|_{s=2 \cdot \pi \cdot j \cdot f} \right) \quad \textbf{(25.1)}$$

Active A Filter Noise Analysis

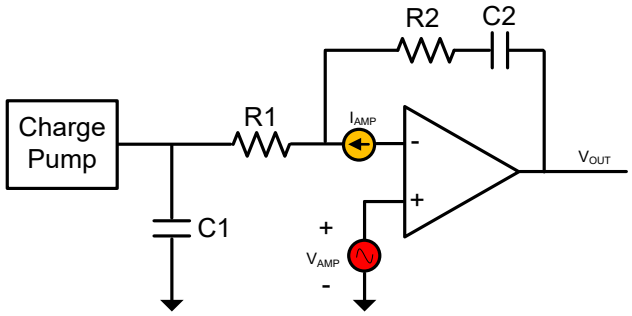


Figure 25.1 *Active A Filter Op-Amp Noise Analysis*

Op Amp Noise Transfer Function

The current from negative terminal to ground due to V_{AMP} is:

$$i = \frac{V_{AMP}}{R1 + {}^{1}/_{(s \cdot C1)}} \tag{25.2}$$

This same current flows through R2 and C2 and generates the following across them.

$$V_{OUT} = V_{AMP} \cdot \frac{R2 + \frac{1}{s \cdot C2}}{R1 + \frac{1}{s \cdot C1}} = V_{AMP} \cdot \frac{C1}{C2} \cdot \frac{1 + s \cdot R2 \cdot C2}{1 + s \cdot R1 \cdot C1} \tag{25.3}$$

Now V_{AMP} is also at the inverting terminal, so the total transfer function is:

$$\frac{V_{OUT}}{V_{AMP}} = 1 + \frac{C1}{C2} \cdot \frac{1 + s \cdot R2 \cdot C2}{1 + s \cdot R1 \cdot C1} \tag{25.4}$$

As for the current noise, this multiplies R2 and C2, but is split with R1 and C1

$$\frac{V_{OUT}}{I_{AMP}} = \frac{1}{s} \cdot \frac{(1 + s \cdot C1 \cdot R1) \cdot (1 + s \cdot C2 \cdot R2)}{C1 + C2 + s \cdot C1 \cdot C2 \cdot (R1 + R2)} \tag{25.5}$$

So the total noise from the amp is:

$$V_{OUT} = \sqrt{\left[V_{AMP} \cdot \left(1 + \frac{C1}{C2} \cdot \frac{1 + s \cdot R2 \cdot C2}{1 + s \cdot R1 \cdot C1}\right)\right]^2 + \left[I_{AMP} \cdot \left(\frac{1}{s} \cdot \frac{(1 + s \cdot C1 \cdot R1) \cdot (1 + s \cdot C2 \cdot R2)}{C1 + C2 + s \cdot C1 \cdot C2 \cdot (R1 + R2)}\right)\right]^2} \tag{25.6}$$

R1 and R2 Resistor Noise Transfer Function

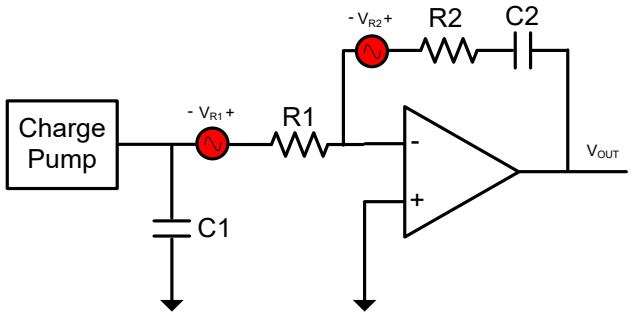


Figure 25.2 *Active A Filter Resistor Noise Analysis*

For R2, the voltage goes straight to the output, so the transfer function is just unity. For R1, current from negative terminal to ground is:

$$i = \frac{V_{R1}}{R1 + {}^{1}/_{(s \cdot C1)}} \tag{25.7}$$

This same current flows through R2 and C2 and generates the following across them.

$$V_{OUT} = V_{R1} \cdot \frac{C1}{C2} \cdot \frac{1 + s \cdot R2 \cdot C2}{1 + s \cdot R1 \cdot C1} \tag{25.8}$$

The total transfer function for R1 and R2 is therefore:

$$V_{OUT} = \sqrt{\left[V_{R1} \cdot \left(\frac{C1}{C2} \cdot \frac{1 + s \cdot R2 \cdot C2}{1 + s \cdot R1 \cdot C1}\right)\right]^2 + (V_{R2})^2} \tag{25.9}$$

Bias Resistor Noise Analysis

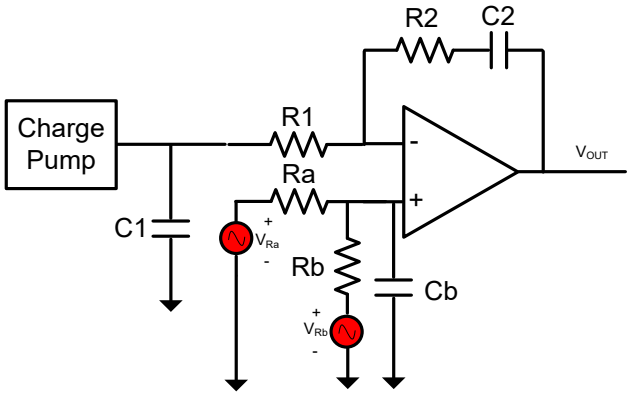


Figure 25.3 *Active A Filter Bias Resistor Noise Analysis*

The first thing to do is redraw the circuit using a Thevenin equivalent combine the noise sources.

$$Rth = \frac{Ra \cdot Rb}{Ra + Rb} \tag{25.10}$$

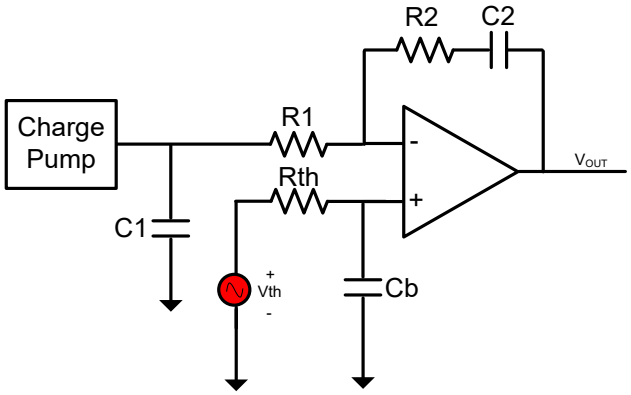


Figure 25.4 *Thevenin Equivalent for Bias Resistor Noise Analysis*

The voltage induced at the output is therefore

$$V_{OUT} = \frac{\sqrt{4 \cdot T \cdot k \cdot Rth \cdot B}}{1 + s \cdot Cb \cdot Rth} \cdot \left(1 + \frac{C1}{C2} \cdot \frac{1 + s \cdot R2 \cdot C2}{1 + s \cdot R1 \cdot C1}\right) \tag{25.11}$$

Active B Filter Noise Analysis

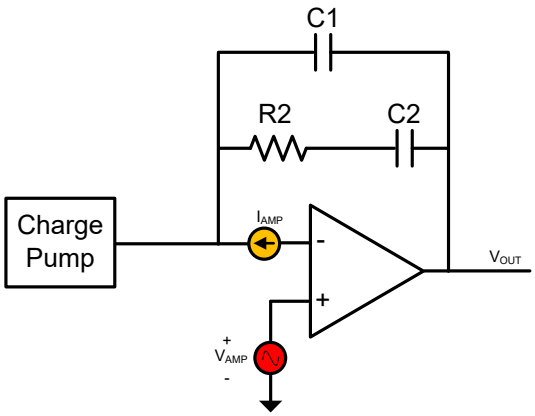


Figure 25.5 *Active B Filter Op-Amp Noise Analysis*

Op Amp Noise Transfer Function

The noise voltage of V_{AMP} goes straight to the output.

$$\frac{V_{OUT}}{V_{AMP}} = 1 \tag{25.12}$$

The noise caused by the op amp noise current is just in the feedback path and can be expressed as follows:

$$\frac{V_{OUT}}{I_{AMP}} = \frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2) \cdot (1 + s \cdot T1)} \tag{25.13}$$

The mathematics can be simplified by introducing a constant for the pole of the filter.

$$T1 = \frac{R2 \cdot C2 \cdot C1}{C1 + C2} \tag{25.14}$$

So the total noise from the amp is:

$$V_{OUT} = \sqrt{(V_{AMP})^2 + \left[I_{AMP} \cdot \left(\frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2) \cdot (1 + s \cdot T1)}\right)\right]^2} \tag{25.15}$$

R2 Resistor Noise Transfer Function

The following figure shows the equivalent circuit for the transfer function for the voltage noise due to resistor R2.

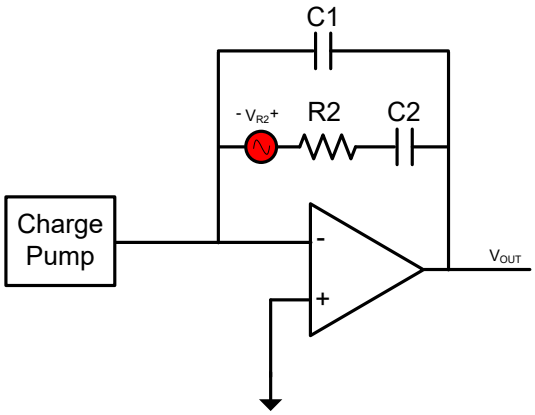


Figure 25.6 *Active B Filter Resistor Noise Analysis*

The noise caused by the resistor R2 is derived by taking the current through the circuit below and multiplying by the impedance of C1.

$$\frac{V_{OUT}}{V_{R2}} = \frac{\frac{1}{s \cdot C1}}{\frac{1}{s \cdot C1} + \frac{1}{s \cdot C2} + R2} = \frac{C2}{(C1 + C2) \cdot (1 + s \cdot T1)} \quad \textbf{(25.16)}$$

So the noise from the resistor R2 to the output is:

$$V_{OUT} = \sqrt{\left[V_{R2} \cdot \left(\frac{C2}{(C1 + C2) \cdot (1 + s \cdot T1)}\right)\right]^2} \quad \textbf{(25.17)}$$

Bias Resistor Noise Analysis

The bias voltage is filtered by the capacitor, but then passes straight to the output. Vth is defined the same way as it is for the Active A filter.

$$V_{OUT} = \frac{Vth}{1 + s \cdot Cb \cdot Rth} \quad \textbf{(25.18)}$$

Active C Filter Noise Analysis

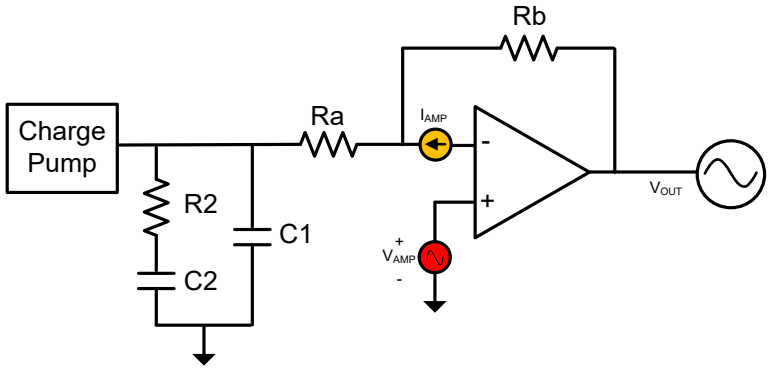


Figure 25.7 *Active C Filter Noise Analysis*

Op Amp Noise Transfer Function

The noise voltage at the output caused by V_{AMP} is derived in a similar way as before.

$$\frac{V_{OUT}}{V_{AMP}} = 1 + \frac{Rb}{Ra + \frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2 + s \cdot R2 \cdot C2 \cdot C1)}} \quad \textbf{(25.19)}$$

The noise voltage at the output caused by I_{AMP} just creates a voltage across Rb

$$\frac{V_{OUT}}{I_{AMP}} = Rb \quad \textbf{(25.20)}$$

The total noise from the op-amp is therefore:

$$V_{OUT} = \sqrt{\left[V_{AMP} \cdot \left(1 + \frac{Rb}{Ra + \frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2 + s \cdot R2 \cdot C2 \cdot C1)}}\right)\right]^2 + (I_{AMP} \cdot Rb)^2} \quad \textbf{(25.21)}$$

R2 Resistor Noise Transfer Function

The R2 Resistor noise is as it was for the Active B, but multiplied by the gain of the op amp.

$$\frac{V_{OUT}}{V_{R2}} = \frac{s \cdot C2}{s \cdot (C1 + C2) \cdot (1 + s \cdot T1)} \cdot \left(1 + \frac{Rb}{Ra}\right) \quad \textbf{(25.22)}$$

Bias Resistor Noise Analysis

The bias voltage is multiplied by the same transfer function as the amp noise voltage, but in this case, the bias can be set to 0 V, so this noise is zero.

Impact of Adding an Extra Pole or Two

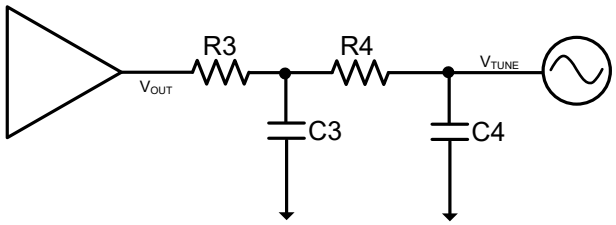


Figure 25.8 *Added Poles after Op-Amp*

Regardless of the approach, it is desirable to add a pole or two after the op amp as this will filter all the noise sources discussed. The transfer function of this added pole is:

$$\frac{V_{TUNE}}{V_{OUT}} = \frac{1}{1 + s \cdot (C3 \cdot R3 + C4 \cdot R4 + R3 \cdot C4) + s^2 \cdot C3 \cdot C4 \cdot R3 \cdot R4} \qquad \textit{(25.23)}$$

For the resistor noise due to these sources, view this as:

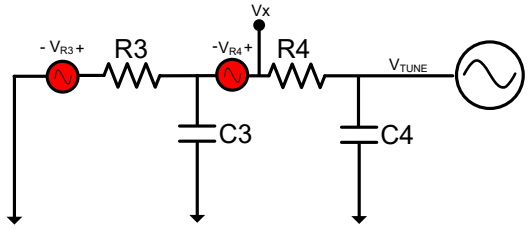


Figure 25.9 *Noise Analysis for Added Poles*

For Resistor Noise R3:

$$Z3 = \frac{1 + s \cdot R4 \cdot C4}{s \cdot C3 + s \cdot C4 + s^2 \cdot C3 \cdot C4 \cdot R4} \qquad \textit{(25.24)}$$

$$\frac{Vx}{V_{R3}} = \frac{Z3}{R3 + Z3} \qquad \textit{(25.25)}$$

$$\frac{V_{TUNE}}{V_{R3}} = \frac{Vx}{V_{R3}} \cdot \frac{1}{1 + s \cdot C4 \cdot R4} = \frac{Z3}{R3 + Z3} \cdot \frac{1}{1 + s \cdot C4 \cdot R4} \qquad \textit{(25.26)}$$

For Resistor Noise R4:

$$Z4 = R4 + \frac{R3}{1 + \mathrm{s} \cdot \mathrm{R3} \cdot \mathrm{C3}} \quad \textbf{(25.27)}$$

$$\frac{V_{TUNE}}{V_{R4}} = \frac{1}{1 + s \cdot C4 \cdot Z4} \quad \textbf{(25.28)}$$

The total noise voltage at the output due to the resistors and added pole is as follows:

$$V_{TUNE} = \sqrt{({V_{OUT}}^2) \cdot Z3^2 + \left[(V_{R3}) \cdot \left(\frac{Z3}{\mathrm{R3} + \mathrm{Z3}} \cdot \frac{1}{1 + s \cdot C4 \cdot R4}\right)\right]^2 + \left[(V_{R4}) \cdot \left(\frac{1}{1 + s \cdot C4 \cdot Z4}\right)\right]^2} \quad \textbf{(25.29)}$$

Conclusion

The noise of an active filter is the sum of the noise due to the filter resistors, op-amp noise voltage, and op-amp noise current. For Active A and B filters, a bias network is also necessary and this noise also adds, but this can be significantly reduced to be a non-contributor by adding a large capacitor in parallel with it. Once the noise from all the sources is added, this creates FM modulation on the VCO in a similar way as a passive filter. The addition of poles after the op amp is often advantageous because it can attenuate the op-amp noise as well as the spurs.

Appendix Summary of Noise Transfer functions

The transfer functions have been derived for the active filters and the table summarizes all the findings.

Noise	Filter Type	Formula
Op Amp	Active A	$\sqrt{\left[V_{AMP}\cdot\left(1+\frac{C1}{C2}\cdot\frac{1+s\cdot R2\cdot C2}{1+s\cdot R1\cdot C1}\right)\right]^2+\left[I_{AMP}\cdot\left(\frac{\left(R2+\frac{1}{s\cdot C2}\right)\cdot(1+s\cdot C1\cdot R1)}{s\cdot C1\cdot(R1+R2)+1+C1/C2}\right)\right]^2}$
	Active B	$\sqrt{{V_{AMP}}^2+[I_{AMP}\cdot Z2]^2}$
	Active C	$\sqrt{\left[V_{AMP}\cdot\left(1+\frac{Rb}{Ra+Z2}\right)\right]^2+[I_{AMP}\cdot Rb]^2}$
Loop Filter Resistors	Active A	$\sqrt{\left[V_{R1}\cdot\left(\frac{C1}{C2}\cdot\frac{1+s\cdot R2\cdot C2}{1+s\cdot R1\cdot C1}\right)\right]^2+(V_{R2})^2}$
	Active B	$V_{R2}\cdot\left(Z2\cdot\frac{s\cdot C2}{1+s\cdot C2\cdot R2}\right)$
	Active C	$V_{R2}\cdot\left(Z2\cdot\frac{s\cdot C2}{1+s\cdot C2\cdot R2}\right)\cdot\left(1+\frac{Rb}{Ra}\right)$
Op Amp Bias Resistors	Active A	$\frac{Vth}{1+s\cdot Cb\cdot Rth}\cdot\left(1+\frac{C1}{C2}\cdot\frac{1+s\cdot R2\cdot C2}{1+s\cdot R1\cdot C1}\right)$
	Active B	$\frac{Vth}{1+s\cdot Cb\cdot Rth}$
	Active C	0
Third and Fourth Pole	All Filter Types	$\sqrt{\left(\frac{Z3}{\mathrm{R3+Z3}}\cdot\frac{V_{R3}}{1+s\cdot C4\cdot R4}\right)^2+\left(\frac{V_{R4}}{1+s\cdot C4\cdot Z4}\right)^2}$ $Z3=\frac{1+s\cdot R4\cdot C4}{\mathrm{s\cdot C3+s\cdot C4+s^2\cdot C3\cdot C4\cdot R4}}$ $Z4=R4+\frac{R3}{1+\mathrm{s\cdot R3\cdot C3}}$

Table 25.2 *Active Filter Formulas*

Chapter 26 Integrated Phase Noise Quantities

Introduction

There are several phase noise metrics that are derived by integrating the phase noise over a certain bandwidth in order to make it easier to interpret the phase noise on the system performance. These metrics include signal to noise ratio (SNR), root mean square (RMS) phase error, jitter, and error vector magnitude (EVM). This chapter discusses all these metrics.

Calculating the Integrated Phase Noise

Formula for Calculation of Integrated Phase Noise

For all of these noise quantities, the first step is to calculate the area under the phase noise profile. For this, there are two limits. ***a*** is the lower limit and ***b*** is the upper limit.

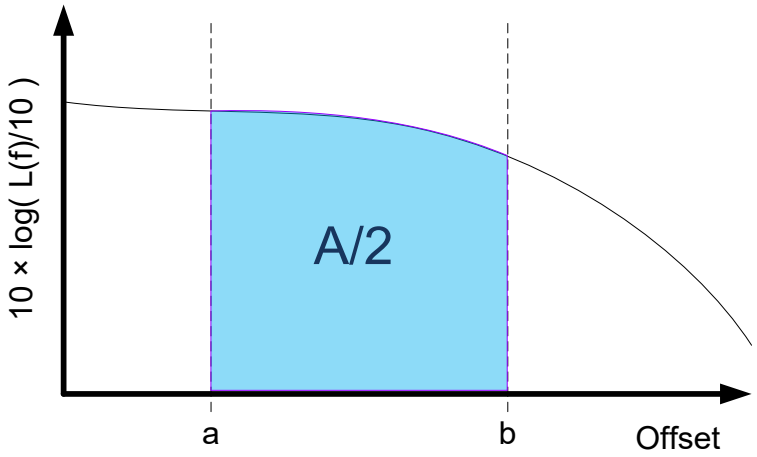


Figure 26.1 *Integrated Phase Noise*

The determination of the lower limit, ***a***, is application specific, for some applications, like GSM, it is chosen to be the frame rate, which would be 1.733 kHz. The upper limit is sometimes chosen to be the bit rate or the channel spacing. Because phase noise rolls off, it is the lower limit that is typically more important, and in many cases, making ***b*** infinite only slightly increases this area. The area needs to be multiplied by two in order to get the phase noise on the left and right sides of the carrier. This formula assumes that the phase noise, ***L(f)***, is in scalar units, not logarithmic units. The *integrated noise*, ***A***, is computed by integrating the phase noise over a specified bandwidth and multiplying by two.

$$A = 2 \cdot \int_a^b L(f) \cdot df \qquad \textbf{(26.1)}$$

L(f) expressed in logarithmic units is in dBc/Hz. After converted to scalar units, it has units of 1/Hz. When this is integrated over frequency, this unit cancels and leaves this as a dimensionless quantity. A few rules of thumb regarding phase noise area can now be seen. If phase noise is increased by 6 dB at all offsets, the phase noise area is quadrupled. Decreasing the lower limit will always increase this area.

Impact of Spurs on the Integrated Phase Noise

In most cases, spurs are outside the loop bandwidth and have only a very small impact on the integrated phase noise. However, many fractional PLLs and especially delta sigma PLLs have spurs that can occur inside the loop bandwidth. The way to treat a spur is to assume that all the energy is inside a 1 Hz bandwidth. The impact of a spur depends on the bandwidth. If one considers the phase noise to be flat within the integration bandwidth, then the spur relates to the phase noise in a 10·log(BW) sense. For instance, a spur that is 40 dB above the noise floor has the same integrated noise as the noise floor itself integrated over a 10 kHz bandwidth. Two spurs that are 37 dB above this noise floor would also have the equivalent noise energy.

Choice of Loop Bandwidth and Phase Margin for Minimum Integrated Phase Noise

The PLL noise (charge pump, input path, and counters) tends to dominate inside the loop bandwidth and the VCO phase noise tends to dominate outside the loop bandwidth. The in-band phase noise sources tend to be more flat and the out-band sources tend to roll off. This implies that there is an offset frequency for which they are equal. If one chooses the loop bandwidth equal to this frequency, then this should be close to the choice that minimizes the integrated noise. In actuality, there are some factors that cause it to be slightly different. The VCO noise can impact the in-band phase noise for narrower loop bandwidths. The PLL noise is not perfectly flat. Furthermore, peaking can also distort this result. Nevertheless, choosing the loop bandwidth to be the offset frequency where the free running VCO noise is equal to the PLL noise is a good starting point for the optimal loop bandwidth. If the PLL noise improves with VCO noise constant, then this optimal loop bandwidth increases. If the VCO noise improves with the PLL noise constant, then this optimal loop bandwidth decreases.

The phase margin also has an impact on the integrated phase noise. Low phase margin typically causes peaking in the phase noise response near the loop bandwidth. This peaking can contribute significantly to the integrated phase noise. In general, designing for the highest phase margin possible yields the lowest integrated phase noise because it causes a much flatter response. There are design trade-offs with the phase margin and lock time as well, and this is discussed in more detail later in this book.

Signal to Noise Ratio (SNR)

The integrated phase noise, ***A***, can be thought of the noise power relative to the carrier, provided that the lower limit, ***a***, is greater than zero so that the carrier signal is not included. All which is necessary to find the SNR is to find the reciprocal of the integrated phase noise.

$$\text{SNR} = \frac{1}{A} \tag{26.2}$$

It is common practice to express the SNR in dB as well as scalar units.

$$\text{SNR}_{dB} = 10 \cdot \log\left(\frac{1}{A}\right) \tag{26.3}$$

Rule of Thumb for Finding the Signal to Noise Ratio of Two Mixed Signals

If two signals are presented to the input of an ideal mixer, then the actual calculation of SNR would involve knowing the spectrum of the two signals. However, some coarse rules of thumb can be developed that require much less work; this is helpful in understanding how a PLL used to generate a local oscillator can impact system performance.

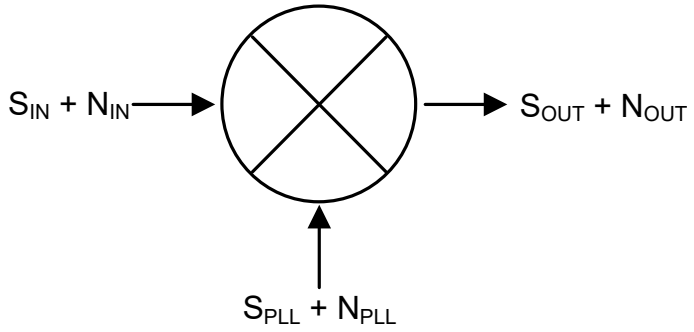


Figure 26.2 *PLL Noise Impact on SNR*

Consider an input signal to a mixer:

$$S_1 = S_{IN} + N_{IN} \tag{26.4}$$

Where S1 is the total input signal, Si is the desired input signal, and Ni is the undesired input noise. Now assume that the PLL signal is:

$$S_2 = S_{PLL} + N_{PLL} \quad \textbf{(26.5)}$$

The output signal is therefore the product of the two signals S1 and S2

$$S_{OUT} + N_{OUT} = S_{PLL} \cdot S_{IN} + S_{PLL} \cdot N_{IN} + S_{IN} \cdot N_{PLL} + N_{PLL} \cdot N_{IN} \quad \textbf{(26.6)}$$

Now the first term is the desired signal power and the last term is negligible. The output signal to noise ratio can therefore be approximated as:

$$SNR = \frac{S_{PLL} \cdot S_{IN}}{S_{PLL} \cdot N_{IN} + S_{IN} \cdot N_{PLL}} = \frac{\left(\frac{S_{PLL}}{N_{PLL}}\right) \cdot \left(\frac{S_{IN}}{N_{IN}}\right)}{\left(\frac{S_{PLL}}{N_{PLL}}\right) + \left(\frac{S_{IN}}{N_{IN}}\right)} = \frac{SNR_1 \cdot SNR_2}{SNR_1 + SNR_2} \quad \textbf{(26.7)}$$

In the above equation, $\boldsymbol{SNR_1}$ and $\boldsymbol{SNR_2}$ represent the signal to noise ratios of $\boldsymbol{S_1}$ and $\boldsymbol{S_2}$, respectively. In an analogous way that two resistances combine in parallel, the lower signal to noise ratio dominates. The above calculations contain some very gross approximations, but they do show how the signal to noise ratio of the PLL can degrade the signal to noise ratio of the whole system.

Understanding Standard Deviation

Introducing the Concept of Standard Deviation

In order to understand integrated noise concepts like RMS phase error, EVM, and jitter, it is necessary to understand the concept of standard deviation. The standard deviation is a measure of central tendency. It can be shown that the average of samples approaches a Gaussian distribution as the sample size approaches infinity, except for the most pathological cases that only a mathematician could dream of. For a Gaussian distribution, it can be shown that if something is sampled, then 68% of the time, the sample will be within one standard deviation of the mean value, 95% of the time, the sample will be within two standard deviations, and 99% of the time will be within three standard deviations.

Estimating Standard Deviation from Minimum, Maximum, and Sample Size

In theory, if one took enough samples, then they would be arbitrary big and arbitrarily small if they came from a Gaussian distribution. Although shunned by theoreticians, a rough guess at the standard deviation can be made from the minimum, maximum, and sample size. One approach is to assume that the minimum and maximum are below and above the average by some number of standard deviations, ***n***. For instance, for a sample size of 40, one would expect roughly 95%, or 38 of these samples to be within two standard deviations.

That implies that two are outside of two standard deviations. If one assumes that the minimum is below by two standard deviations, and the maximum is above by two standard deviations, then one could divide the difference between maximum and minimum by 4 and estimate the standard deviation.

$$\sigma = \frac{Maximum - Minimum}{\rho} \tag{26.8}$$

$$\rho = 2 \cdot \Phi^{-1}\left(1 - \frac{n}{2}\right) \tag{26.9}$$

Φ^{-1} is the inverse of the standard normal distribution function with zero mean and standard deviation of 1. In general, the value that this difference is divided by, ρ, is dependent on the sample size, N. Table 26.1 shows values for the parameter, ρ. A numerical Monte Carlo simulation was also used to for comparison purposes and to increase the confidence in this formula and indeed the results matched. As an example, consider a sample size of 50. To estimate the standard deviation, σ, take the difference between the maximum and minimum and divide by 4.65.

N	Minimum	Maximum	ρ
2	-0.57	0.56	1.35
3	-0.85	0.85	1.93
4	-1.04	1.02	2.30
5	-1.16	1.16	2.56
6	-1.27	1.27	2.77
7	-1.36	1.35	2.93
8	-1.42	1.43	3.07
9	-1.49	1.48	3.19
10	-1.54	1.54	3.29
11	-1.58	1.59	3.38
12	-1.63	1.63	3.46
13	-1.67	1.67	3.54
14	-1.70	1.70	3.61
15	-1.73	1.74	3.67
16	-1.76	1.77	3.73
17	-1.79	1.80	3.78
18	-1.82	1.82	3.83
19	-1.84	1.84	3.88
20	-1.87	1.87	3.92
50	-2.25	2.27	4.65
100	-2.51	2.51	5.15
200	-2.74	2.75	5.61
500	-3.04	3.06	6.18
1000	-3.21	3.24	6.58
10^4	-3.75	3.79	7.78
10^5	-4.42	4.42	8.83
10^6	-4.89	4.89	9.78
10^7	-5.33	5.33	10.65
10^8	-5.73	5.73	11.46
10^9	-6.11	6.11	12.22

Table 26.1 *Calculation of the parameter* ρ

Relating the Integrated Phase Noise to a Standard Deviation

Relating the Integrated Phase Noise to the σ_v^2

The key link to relate integrated noise to the time domain begins with first understanding how integrated phase noise relates to a standard deviation of the noise voltage. It is well established that the standard deviation for a continuous random variable, ***u(x)***, with zero mean can be calculated as follows:

$$\sigma = \int_{-\infty}^{\infty} u^2(x) \cdot dx \qquad \textbf{(26.10)}$$

In the case of phase noise, this is noise power relative to the carrier power, which can be thought of the square of noise voltage to the square of the carrier voltage. This technically would involve a resistance, but as it is the same for both the carrier and the noise, it cancels out. The phase noise limits on the integrated noise formula would just indicate that the noise voltage does not apply beyond these limits. The key relationship that therefore follows is that the integrated noise is the variance of the noise voltage.

$$\mathrm{A} = 2 \cdot \int_a^b L(f) \cdot df \; = \int_{-\infty}^{\infty} v^2(f) \cdot df \; = {\sigma_v}^2 \qquad \textbf{(26.11)}$$

In this case, ***v***, is the voltage noise relative to the carrier and has an average value of zero. σ_v^2 is the square of the standard deviation of the noise voltage. It easily follows that:

$$\sigma_v = \sqrt{2 \cdot \int_a^b L(f) \cdot df} \qquad \textbf{(26.12)}$$

σ_v is a relative voltage. If it has a value of one, this means that the noise power is equal to the carrier power. In general, it is fair to assume that this has a value of much less than one.

Relating Voltage Noise to a Phase Error

Now that it is understood how to calculate the standard deviation of the relative noise voltage, σ_v, it now needs to be related the standard deviation of the phase error, σ_ϕ. For this derivation, σ_ϕ has units of radians and will be considered to be small.

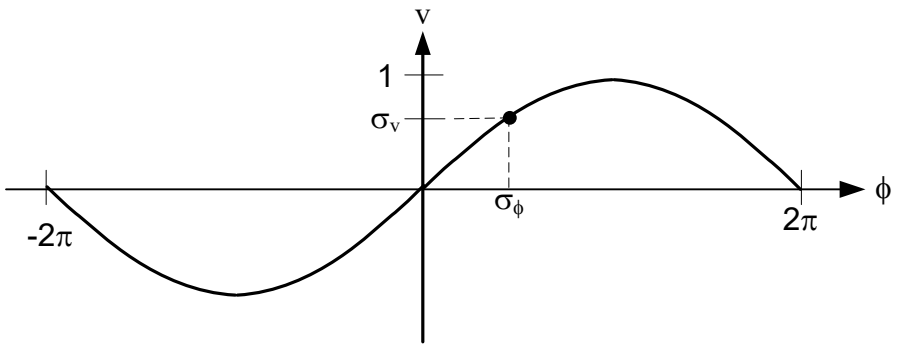


Figure 26.3 *Relating Voltage to Phase*

In the time domain, the carrier can be thought of as a sine wave. ***v*** is the relative noise voltage in relation to the amplitude of this carrier and $\boldsymbol{\phi}$ is the phase of the carrier. A reasonable assumption is to assume that $\boldsymbol{\phi}$ is small which justifies approximating $\boldsymbol{sin(\phi)}$ as $\boldsymbol{\phi}$. It therefore follows that the standard deviation of the relative voltage noise can be equated to the standard deviation of the phase error.

$$\sigma_{\emptyset} \approx \sigma_{v} \tag{26.13}$$

In summary, the integrated noise has been shown to be equal to the variance of the noise voltage. The square root of the noise voltage is by definition the standard deviation of the noise voltage, and the standard deviation of the noise voltage has been shown to be related to the standard deviation of the phase error.

RMS Phase Error Calculation

Equation (26.14) is the final link between integrated phase noise and phase error. The RMS Phase Error expressed in radians can now be calculated.

$$\sigma_{v(rad)} = \sigma_{v} = \sqrt{2 \cdot \int_{a}^{b} L(f) \cdot df} \tag{26.14}$$

Usually, the RMS phase error is expressed in degrees. The conversion is very straightforward.

$$\sigma_{\emptyset(deg)} = \frac{180}{\pi} \cdot \sigma_{\emptyset(rad)} = \frac{180}{\pi} \cdot \sqrt{2 \cdot \int_{a}^{b} L(f) \cdot df} \tag{26.15}$$

RMS Phase Error Interpretation in the Time Domain and Jitter

RMS Phase Error Interpretation in the Time Domain

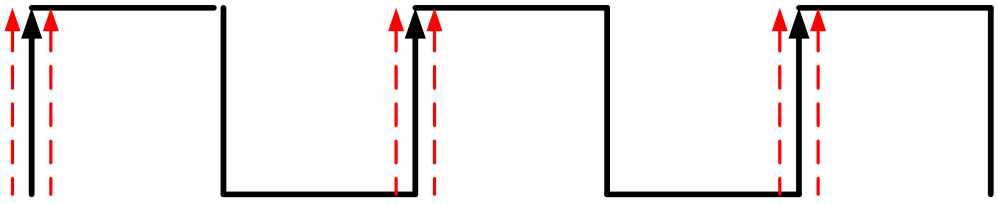


Figure 26.4 *Illustration of RMS Phase Error of a Signal in the Time Domain*

The result of running a square wave with a nonzero RMS phase error through a comparator or any digital gate that squares up the wave will result in a square wave as shown in Figure 26.4. The rising edges of the square wave do not always occur at exactly the time they should, but have a random phase error that can be either positive or negative. The average value of this phase error is zero, but the standard deviation is nonzero and is the RMS phase error.

Understanding Jitter and the Relationship it has to RMS Phase Error

Relationship between RMS Phase Error and Jitter

Notice how the rising edges of the signal in Figure 26.4 do not always start at the time they should, but jitter around the desired value. RMS *Jitter* is the conversion of the RMS phase error to a time error. In order to calculate from RMS phase error to RMS jitter (σ_t) it is necessary to convert this phase difference to cycles, and multiply by the reciprocal of the frequency (f).

$$\sigma_t = \frac{1}{f} \cdot \frac{\sigma_{\emptyset(rad)}}{2\pi} = \frac{1}{f} \cdot \frac{\sigma_{\emptyset(deg)}}{360} \qquad \textbf{(26.16)}$$

For an example, consider a 10 MHz signal with 5 degrees RMS phase error. Since the period of this signal is 0.1 µs, a 5 degree RMS phase error is 5/360 = 1/72 cycles. 0.1µs/72 = 1.339 ns.

Cycle to Cycle Jitter

For cycle to cycle jitter, each rising edge of the signal is compared relative to the previous cycle. This is different than RMS jitter, where it is compared to an ideal signal. Consider a signal for which at some time, all rising edges get shifted by a large phase error. The RMS jitter would be large because all the rising edges are off from what they would be for an

ideal signal. However, the cycle to cycle jitter would be much less degraded by this large phase shift, since it only would be important for one cycle.

Peak to Peak Jitter and Jitter Measurement in the Time Domain

RMS jitter is the standard deviation of the time error of the rising edges. Peak to peak jitter is the maximum over all cycles. In theory, if one waits for a longer time, then the peak to peak jitter would be greater. Unlike RMS jitter and cycle to cycle jitter, Peak to peak jitter can be measured on an oscilloscope. The general method is to set the oscilloscope on infinite persistence, and see the time difference between the minimum and the maximum edges of the signal.

Crude Method of Relating Peak to Peak Jitter to RMS Jitter

The most accurate way to calculate RMS jitter is to use the method of integrating the phase noise. However, a spectrum analyzer is not always available, and many people work with jitter tend to have a more digital focus and familiarity of oscilloscopes. Peak to peak jitter can be measured on an oscilloscope by setting the display to infinite persistence and observing the signal in the time domain. This measurement does not account for the lower and upper integration limits as shown in Figure 26.1. Nevertheless, this method appeals to many because it requires only an oscilloscope and it is more intuitive than measuring jitter in the frequency domain. If one accepts this as the peak to peak jitter, it can be related to RMS jitter by equation (26.8) and (26.9), once the sample size is known. The sample size can be found by taking the sampling time divided by the number of samples taken per second. An even more crude method is to sample for "a long time" and divide this value by three, although this method may not be that accurate.

EVM and RMS Phase Error Interpretation in the Constellation Diagram

RMS Phase Error Interpretation in the Constellation Diagram

If one visualizes the RMS error in the time domain, then it can be seen why this may be relevant in clock recovery applications, or any application where the rising (or falling) edges of the signal need to occur in a predictable fashion. The impact of RMS phase error is more obvious when considering a constellation diagram.

The constellation diagram shows the relative phases of the I (in phase) and Q (in quadrature – 90 degrees phase shift) signals. The I and Q axes are considered to be orthogonal, since their inner product is zero. In other words, for any signal received, the I and Q component can be recovered. Each point on the constellation diagram corresponds to a different symbol, which could represent multiple bits. As the number of symbols is increased, the bandwidth efficiency theoretically increases, but the system also becomes more susceptible to noise. Quadrature Phase Shift Keying (QPSK) is a modulation scheme sometimes used in cellular phones. Figure 26.5 shows the constellation diagram for QPSK.

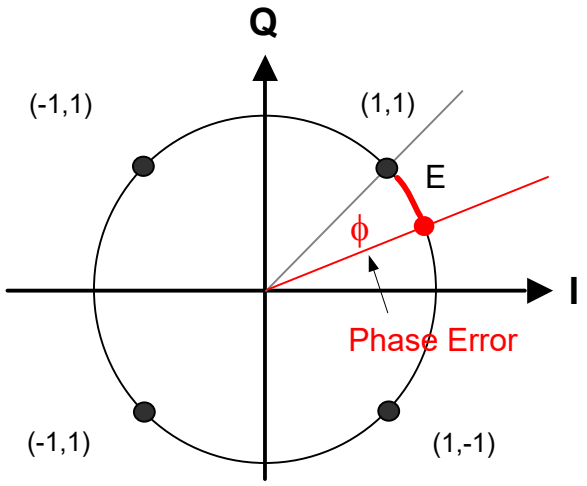


Figure 26.5 *Impact of RMS phase Error Seen on a Constellation Diagram*

Consider an ideal system in which the only noise-producing component is the PLL in the receiver. In this example, the symbol corresponding to the bits (1,1) is the intended message indicated by the darkened circle. However, because the PLL has a non-zero RMS phase error contribution, the received signal is actually the non-filled circle. If this experiment was repeated, then the result would be that the phase error between the received and intended signal was normally distributed with a standard deviation equal to the RMS phase error. If the RMS phase error of the system becomes too large, it could actually cause the message to be misinterpreted as (-1, 1) or (1,-1). This constellation diagram interpretation of RMS phase error shows why higher order modulation schemes are more subject to the RMS phase error of the PLL. A real communications system will have a noisy channel and other noisy components, which reduce the amount of RMS phase error of the PLL that can be tolerated.

Error Vector Magnitude (EVM)

Error Vector Magnitude is the magnitude of the vector formed from the intended message and the actual message received (refer to Figure 26.5). This is commonly expressed as a percentage of the error vector relative to the vector formed between the origin and intended message. Referring to Figure 26.5, assuming the circle has radius R, and applying the law of cosines yields the magnitude of the error vector, ***E***, to be:

$$\mathrm{E} = 2 \cdot R^2 - 2 \cdot R^2 \cdot cos(\emptyset) \qquad \textbf{(26.17)}$$

Assuming that ϕ is small, and using the Taylor series expansion $\cos(\phi) = 1 - \phi^2/2$, yields the following relationship between RMS phase error and EVM:

$$\text{EVM} \approx 100\% \cdot \left(\frac{\pi}{180}\right) \cdot \sigma_{\phi(deg)} \qquad \textbf{(26.18)}$$

Other Interpretations of Integrated Noise

Eye Diagram

The eye diagram gives an indication between the different symbols. If the eye diagram is open, then the bit error rate will be small. If it is more closed, the bit error rate will be increased. Although there is not really a good term to relate RMS phase error to the eye diagram, the impact of the RMS phase error on the eye diagram is that it causes it to close up. This means that the decision region is smaller and it is more likely to make an error in which bits were sent.

Completeness of the Phase Noise Profile

If the phase noise profile is known, then all the integrated phase noise quantities can be calculated. However, it does not work the other way around. If the area under this profile can be found, there are infinitely many ways that area can be achieved. It can be very flat, have a slope, or have most of the energy can be concentrated in one spur. For this reason, the phase noise profile is always good to also have. Nevertheless, the ease of using a single number to quantify phase noise performance is very practical to know and have.

Unifying Theory for Integrated Phase Noise Quantities

Most the noise quantities presented so far are related to the integrated phase noise, ***A***. Many people are familiar with interpreting this integrated phase noise in one way or another. The following table gives a way to relate all these noise quantities to each other.

Given Quantity	Integrated Phase Noise (A)	Signal to Noise Ratio (SNR)	RMS Phase Error ($\sigma_{\phi(deg)}$)	RMS Jitter (σ_t)
A		$1/A$	$\frac{180}{\pi}\sqrt{A}$	$\frac{1}{2\pi f}\sqrt{A}$
SNR	$\frac{1}{SNR}$		$\frac{180}{\pi\sqrt{SNR}}$	$\frac{1}{2\pi f\sqrt{SNR}}$
$\sigma_{\phi(deg)}$	$\left(\frac{\pi \cdot \sigma_{\phi(deg)}}{180}\right)^2$	$\left(\frac{180}{\pi \cdot \sigma_{\phi(deg)}}\right)^2$		$\frac{1}{f} \cdot \frac{\sigma_{\phi(deg)}}{360}$
σ_t	$(2\pi f \cdot \sigma_t)^2$	$\left(\frac{1}{2\pi f \cdot \sigma_t}\right)^2$	$360 \cdot f \cdot \sigma_t$	

Table 26.2 *Unifying Formulas for Integrated Phase Noise Quantities*

RMS Frequency Error (Residual FM)

RMS frequency error is the standard deviation of the frequency error. Following from the definition of the standard deviation, the method is to integrate the phase noise times the square of the offset frequency. By definition, this yields the standard deviation of the frequency error, or more commonly called the RMS frequency error. This is of particular interest in applications involving frequency modulation. More weight is placed at farther offset for this integral. Because it has the factor of f^2 under the integral sign, it does not easily relate to other integrated phase noise quantities.

$$\sigma_f = \sqrt{2 \cdot \int_a^b L(f) \cdot f^2 \cdot df} \qquad \textbf{(26.19)}$$

Conclusion

Integrated noise metrics such as RMS phase error, jitter, and EVM are useful as they give a single number that allows one to interpret the impact of phase noise on the system performance. From a system perspective, it is often easier to understand the impact of an error in phase or time as opposed to using a phase noise profile. All of these integrated noise metrics can be largely impacted by the loop bandwidth of the PLL.

Appendix Sample Calculations with Integrated Phase Error

For this example, a plot was downloaded from the Agilent E4445A spectrum analyzer compared to what the equipment produced. The area was calculated numerically.

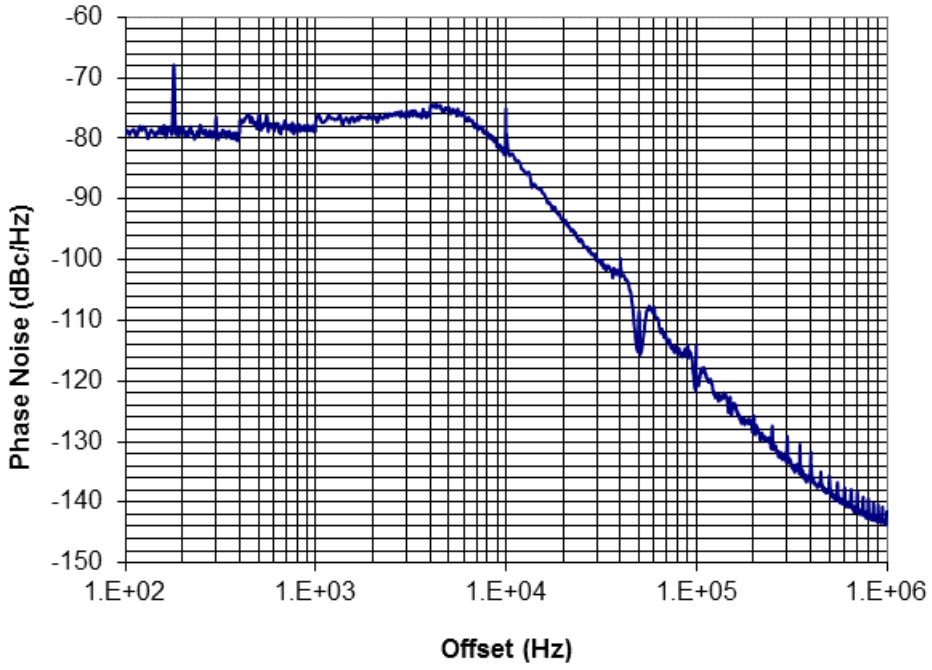


Figure 26.6 *Downloaded Phase Noise Profile*

From this phase noise, integrated phase noise quantities were calculated.

Symbol	Value	Units
f	770	MHz
a	12	kHz
b	100	kHz
A	2.8438×10^{-5}	n/a
$\sigma_{\phi(rad)}$	5.3327×10^{-3}	rad
$\sigma_{\phi(deg)}$	0.3055	deg
EVM	0.533	%
σ_t	1.1023	ps
σ_f	112.6556	Hz

Table 26.3 *Calculated Phase Noise Quantities*

These calculated results can be compared to measurements done by the instrument itself to verify that indeed these calculations are correct.

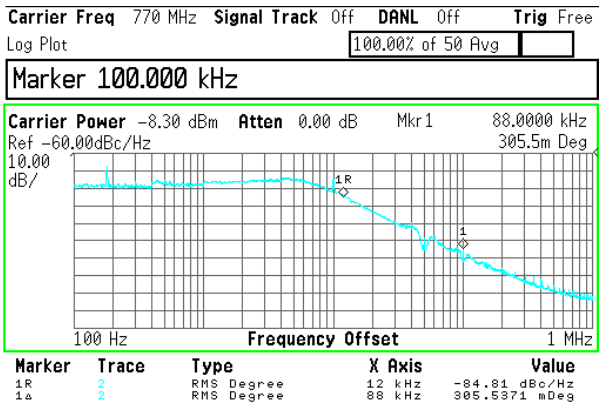
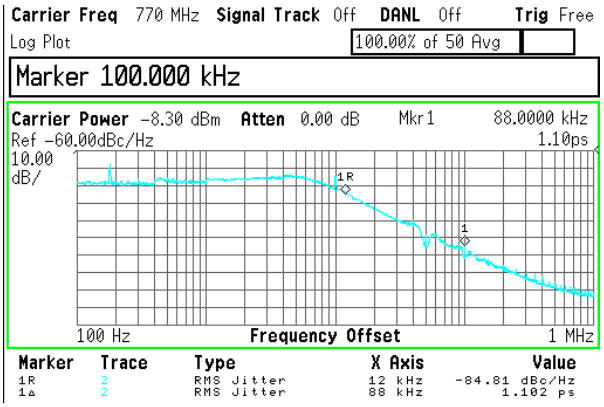
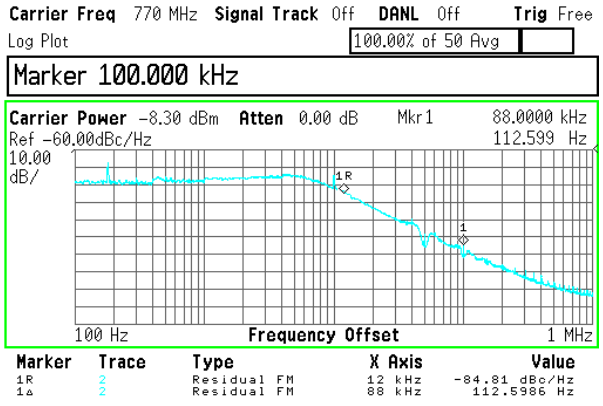
	**RMS Phase Error Calculation**
	**RMS Jitter**
	**RMS Frequency Error**

Figure 26.7 *Integrated Noise Measurements*

Chapter 27 A Sample PLL Phase Noise Analysis

Setup

This chapter goes through the same example presented in the filter analysis chapter, but now focuses on phase noise. A summary of this filter is shown as follows:

Symbol	Description	Value	Units
K_{PD}	Charge Pump Gain	5	mA
K_{VCO}	VCO Gain	30	MHz/V
f_{VCO}	Output Frequency	900	MHz
f_{PD}	Phase detector frequency	200	kHz
C1	Loop Filter Capacitor	5.600	nF
C2	Loop Filter Capacitor	100.00	nF
C3	Loop Filter Capacitor	0.330	nF
*C4**	Loop Filter Capacitor *(Not Accounting For VCO input Capacitance)	0.082	nF
C_{VCO}	VCO Input Capacitance	0.022	nF
R2	Loop Filter Resistor	1.0	kΩ
R3	Loop Filter Resistor	6.8	kΩ
R4	Loop Filter Resistor	33.0	kΩ
N	N Counter Value	4500	none
C4	Loop Filter Capacitor accounting for VCO input Capacitance	0.104	nF
BW	Loop Bandwidth	5.0857	kHz
ϕ	Phase Margin	50.7527	degrees
γ	Gamma Optimization Parameter	1.2313	none

Table 27.1 *Loop Filter Setup from Bode Plot Chapter*

Symbol	Description	Value	Units
K_{PD}Knee	Phase noise knee current	1	mA
*PN1Hz**	1 Hz Normalized Flat Noise for infinite K_{PD}	-214.8	dBc/Hz
*PN10kHz**	10kHz Normalized 1/f Noise for infinite K_{PD}	-101.6	dBc/Hz
VCO_1kHz	Raw VCO phase noise at 1 kHz Offset	-90	dBc/Hz
VCO_10kHz	Raw VCO phase noise at 10 kHz Offset	-115	kHz
VCO_FLR	VCO Phase noise at 10 MHz Offset	-155	dBc/Hz
TCXO10khz	TCXO frequency @ 10 kHz offset	-134	dBc/Hz
f_{TCXO}	TCXO Frequency	20	MHz

Table 27.2 *Phase Noise Coefficients*

TCXO Noise

As the TCXO noise is only specified at one offset, it makes sense to model it with a slope of 20 dB/decade and to scale to the VCO frequency.

$$L_{TCXO}(f) = -134 - 20 \cdot log\left|\frac{f}{10kHz}\right| + 20 \cdot log\left|\frac{f_{VCO}}{f_{TCXO}}\right| = -100.9 - 20 \cdot log\left|\frac{f}{10kHz}\right| \quad \textit{(27.1)}$$

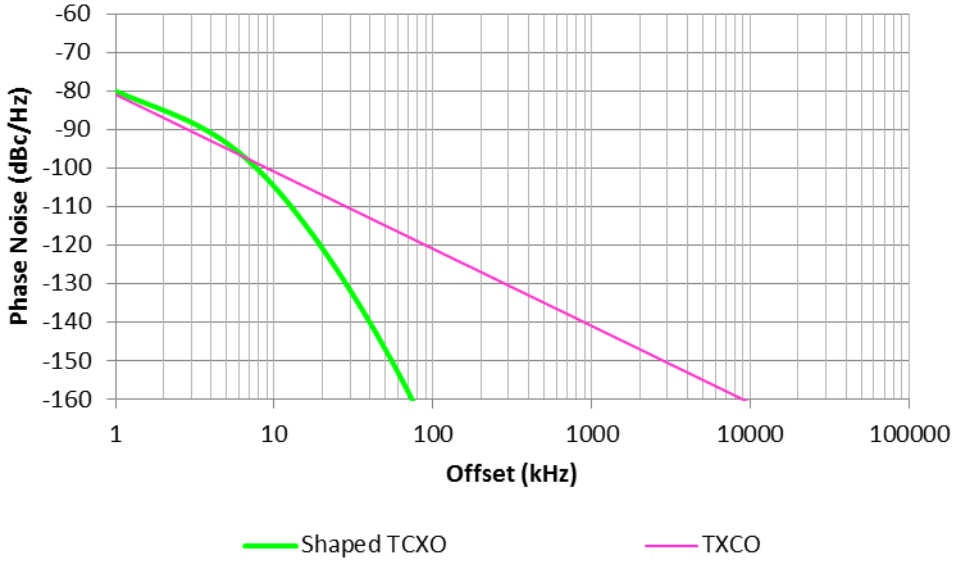


Table 27.3 *TCXO Noise*

PLL Noise

PLL Flat Noise

$$\text{PN1Hz} = -214.8 + 10 \cdot log\left|1 + \frac{1mA}{5mA}\right| = -214 \tag{27.2}$$

$$L_{PLL_{Flat}}(f) = -214 + 10 \cdot log\left|\frac{200kHz}{1Hz}\right| + 20 \cdot \log(4500) = -87.925 \tag{27.3}$$

PLL Flicker Noise

$$\text{PN10Hz} = -101.6 + 10 \cdot log\left|1 + \frac{1mA}{5mA}\right| = -100.8 \tag{27.4}$$

$$\begin{aligned} L_{PLL_{Flicker}}(\text{f}) &= -100.8 + 20 \cdot log\left|\frac{900MHz}{1GHz}\right| - 10 \cdot log\left|\frac{f}{10kHz}\right| \\ &= -101.7 - 10 \cdot log\left|\frac{f}{10kHz}\right| \end{aligned} \tag{27.5}$$

Total PLL Noise

$$L_{PLL}(\text{f}) = 10 \cdot log\left|10^{\left(L_{PLL_{Flat}}(f)/10\right)}\right| + 10^{\left(L_{PLL_{Flat}}(f)/10\right)} + Rolloff \tag{27.6}$$

In the Figure 27.1, the PLL phase noise is shown. Note that the flicker noise can contribute at lower offsets, although the contribution is not that much as this is an integer PLL example. In the cases of a fractional PLL, the flicker noise can be much more dominant due to the higher phase detector frequency.

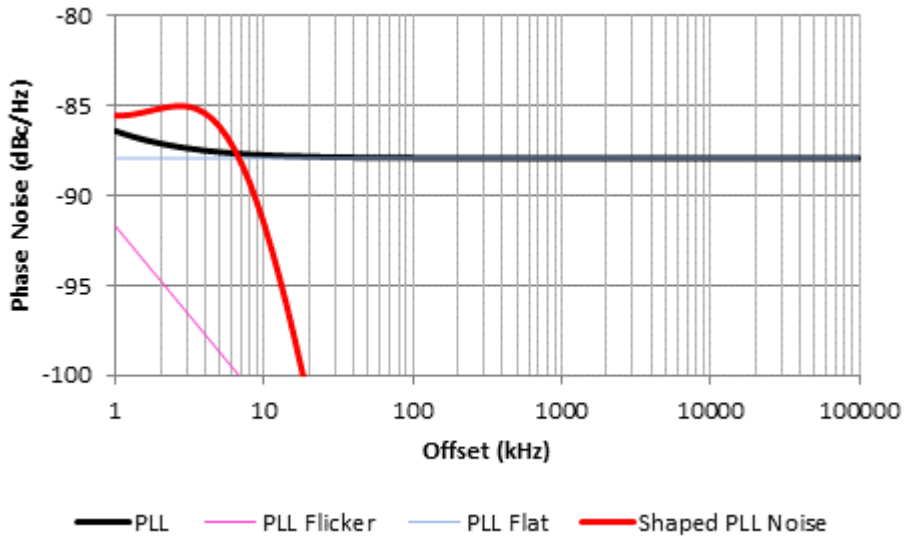


Figure 27.1 *PLL Phase Noise*

VCO Phase Noise

For the VCO phase noise decomposition, the first thing to do is to arrange the three phase noise points by offset in order to check the slope to determine the appropriate model. In the same step, one can convert these offsets to scalar units and translate back to 1 GHz VCO frequency. This is all done in the following table.

Offset	Phase Noise (dBc/Hz)	Slope (dB/decade)	Scalar Units
f3 = 1kHz	-90	n/a	$p3 = \left(\frac{1GHz}{900MHz}\right)^2 \cdot 10^{-(90/10)} = 1.2345 \times 10^{-9}$
f2 = 10kHz	-115	$\frac{-115-(-90)}{log\left(\frac{10kHz}{1kHz}\right)} = -25$	$p2 = \left(\frac{1GHz}{900MHz}\right)^2 \cdot 10^{-(115/10)} = 3.90405 \times 10^{-12}$
f0 = 10MHz	-155	$\frac{-155-(-115)}{log\left(\frac{10MHz}{10kHz}\right)} = -13$	$p0 = \left(\frac{1GHz}{900MHz}\right)^2 \cdot 10^{-(155/10)} = 3.90405 \times 10^{-16}$

Table 27.4 *Analysis of VCO Offsets*

We see that the slope from p3 to p2 is a between -30 and -20 dB/decade which implies that this is a combination of the $1/f^3$ and $1/f^2$ noise. The slope from p2 to p0 is between -20 to 0 dB decade, which it implies it is a combination of the $1/f^2$ and phase noise floor. This therefore leads to a system of 3 equations and 3 unknowns. Choosing $f_{default}$ = 1 MHz and expressing in matrix form we get:

$$1.2345 \times 10^{-9} = n3 \cdot \left(\frac{1MHz}{1kHz}\right)^3 + n2 \cdot \left(\frac{1MHz}{1kHz}\right)^2 \quad \textit{(27.7)}$$

$$3.9040 \times 10^{-12} = n3 \cdot \left(\frac{1MHz}{10kHz}\right)^3 + n2 \cdot \left(\frac{1MHz}{10kHz}\right)^2 \quad \textit{(27.8)}$$

$$3.90405 \times 10^{-16} = n2 \cdot \left(\frac{1MHz}{10MHz}\right)^2 + n0 \quad \textit{(27.9)}$$

This system of equations can be expressed in matrix form as follows:

$$\begin{bmatrix} 1.2345 \times 10^{-9} \\ 3.9040 \times 10^{-12} \\ 3.90405 \times 10^{-16} \end{bmatrix} = \begin{bmatrix} 10^{9} & 10^{9} & 0 \\ 10^{6} & 10^{4} & 0 \\ 0 & 10^{-2} & 1 \end{bmatrix} \bullet \begin{bmatrix} n3 \\ n2 \\ n0 \end{bmatrix} \quad \textit{(27.10)}$$

$$\begin{bmatrix} n3 \\ n2 \\ n0 \end{bmatrix} = \begin{bmatrix} 10^{9} & 10^{6} & 0 \\ 10^{6} & 10^{4} & 0 \\ 0 & 10^{-2} & 1 \end{bmatrix}^{-1} \bullet \begin{bmatrix} 1 \\ 3.9040 \times 10^{-12} \\ 3.90405 \times 10^{-16} \end{bmatrix} \quad \textit{(27.11)}$$

$$\begin{bmatrix} n3 \\ n2 \\ n0 \end{bmatrix} = \frac{1}{9} \cdot \begin{bmatrix} 10^{-8} & -10^{-6} & 0 \\ -10^{-6} & 10^{-3} & 0 \\ 10^{-8} & -10^{-5} & 9 \end{bmatrix} \bullet \begin{bmatrix} 1.2345 \times 10^{-9} \\ 3.9040 \times 10^{-12} \\ 3.90405 \times 10^{-16} \end{bmatrix} = \begin{bmatrix} 9.38 \times 10^{-19} \\ 2.97 \times 10^{-16} \\ 3.87 \times 10^{-16} \end{bmatrix} \quad \textit{(27.12)}$$

The VCO noise metrics as normalized to a 1 GHz carrier and 1 MHz offset are given as follows:

Parameter	Scalar Value	dB Value
n3	9.38×10^{-19}	-180.3
n2	2.97×10^{-16}	-155.3
n0	3.87×10^{-16}	-154.1

Table 27.5 *VCO Noise Metrics*

The $1/f^3$ to $1/f^2$ corner point, which is where these two noise sources contribute equally can be calculated as follows:

$$f_{Corner\_F3} = 1MHz \cdot \frac{9.38 \times 10^{-19}}{2.97 \times 10^{-16}} = 3.162\ kHz \quad \textit{(27.13)}$$

The $1/f^2$ to phase noise floor corner point, which is where these two noise sources contribute equally can be calculated as follows:

$$f_{Corner\_FLR} = 1MHz \cdot \sqrt{\frac{2.97 \times 10^{-16}}{3.87 \times 10^{-16}}} = 871\ kHz \quad \textit{(27.14)}$$

The noise contribution can be translated to any offset via the formulae below:

$$L_{VCO_{F3}}(f) = -180.3 - 30 \cdot log\left(\frac{f}{1MHz}\right) \quad \textit{(27.15)}$$

$$L_{VCO_{F2}}(f) = -155.3 - 20 \cdot log\left(\frac{f}{1MHz}\right) \quad \textit{(27.16)}$$

$$L_{VCO_{FLR}} = -154.1 \quad \textit{(27.17)}$$

The total VCO noise contribution is given by:

$$L_{VCO}(f) = 10 \cdot log\left(10^{L_{VCO_{F3}}(f)} + 10^{L_{VCO_{F2}}(f)} + L_{VCO_{FLR}}\right) \quad \textit{(27.18)}$$

f	$L_{VCO}(f)$	$L_{VCO_{F3}}(f)$	$L_{VCO_{F2}}(f)$	$L_{VCO_{FLR}}$
1 kHz	-90	-91.22	-96.22	-155.02
3.162 kHz	-103.20	-106.21	-106.22	-155.02
10 kHz	-115.02	-121.21	-116.22	-155.02
100 kHz	-136.02	-151.22	-136.22	-155.02
871 kHz	-151.00	-151.00	-155.02	-155.02
1 MHz	-152.56	-181.22	-156.22	-155.02
10 MHz	-155.00	-211.22	-176.22	-155.02

Table 27.6 *VCO Noise at Various Offsets*

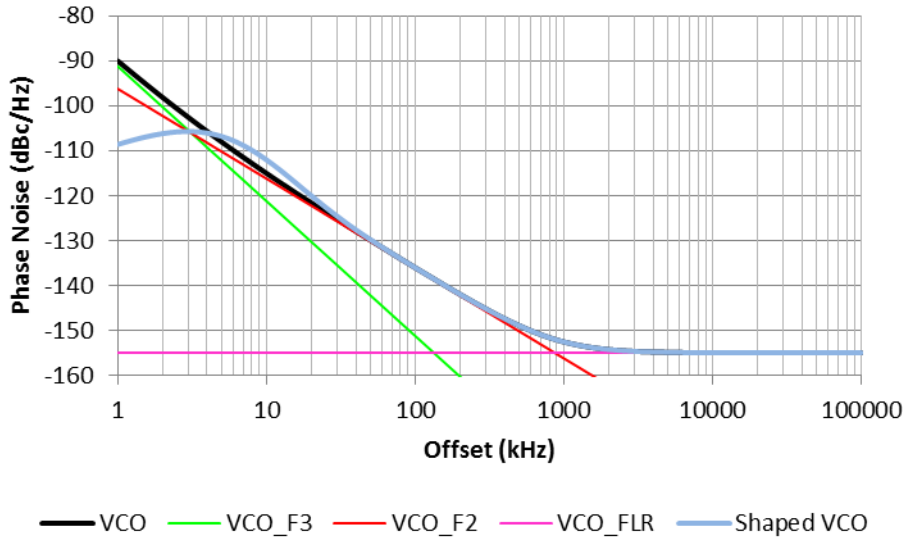


Figure 27.2 *VCO Phase Noise*

Resistor Noises

The general resistor noise formula is:

$$V_{Rx} = \sqrt{4 \cdot T \cdot k \cdot Rx} \qquad \textbf{(27.19)}$$

Symbol	Description	Value	Units
k	Boltzmann's Constant	1.3807	J/K
T	Ambient Temperature	300	K
V_{R2}	Noise Voltage Generated by Resistor ***R2***	4.0704	$nV/\sqrt{Hz}$
V_{R3}	Noise Voltage Generated by Resistor ***R3***	10.0614	$nV/\sqrt{Hz}$
V_{R4}	Noise Voltage Generated by Resistor ***R4***	23.3382	$nV/\sqrt{Hz}$

Table 27.7 *Resistor Noise Calculation*

The transfer functions and translation of this to phase noise is presented in the resistor noises chapter on passive filter noise. The filter noise contribution at various offsets can be found as follows:

Offset	$L_{Filter}(f)$	$L_{Filter_{R2}}(f)$	$L_{Filter_{R3}}(f)$	$L_{Filter_{R4}}$
1 kHz	-84.0	-100.6	-91.8	-84.9
10 kHz	-82.7	-99.8	-90.5	-83.6
100 kHz	-112.7	-144.0	-124.6	-113.0
1 MHz	-151.0	<-200	-180.8	-151.0
10 MHz	-190.9	<-200	<-200	-190.9

Table 27.8 *Resistor Noise at Various Offsets*

It is often the case that the resistor closest to the VCO is the one that contributes the most to the loop filter noise. In this case, it totally dominates it. The filter noise also has a tendency to peak near the loop bandwidth. Unlike the TCXO, PLL, and VCO, there is really no concept of unshaped loop filter noise; it only makes sense to talk about these resistor noises when the actual filter is known.

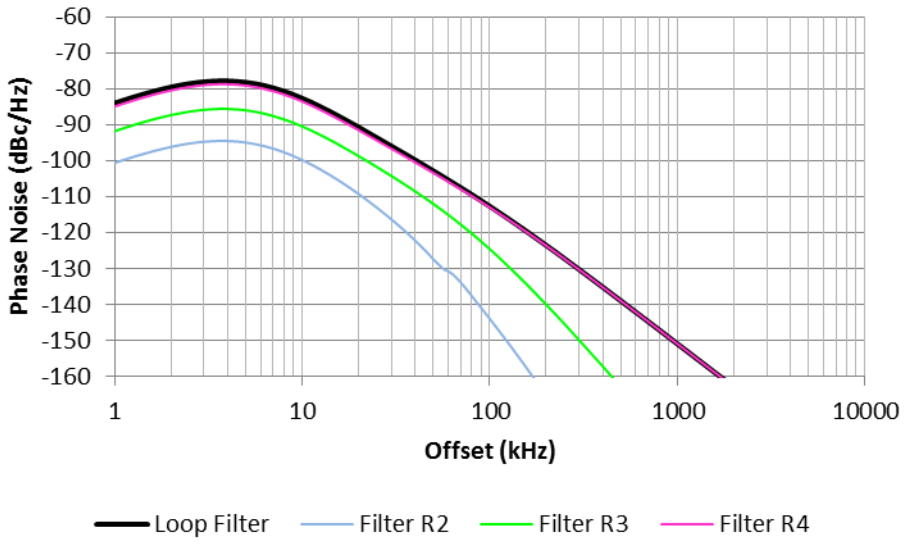


Figure 27.3 *Resistor Noises*

Calculate Total Noise

The total noise is the sum of the shaped TCXO, PLL, VCO, and filter. These have all been computed.

$$L(f) = 10 \cdot log \left| 10^{\left(L_{TXCO}(f)/10\right)} + 10^{\left(L_{PLL}(f)/10\right)} + 10^{\left(L_{VCO}(f)/10\right)} + 10^{\left(L_{Filter}(f)/10\right)} \right| \quad \textbf{(27.20)}$$

Offset	*Total*	*OSC*	*PLL*	*VCO*	*Filter*
0.1	-60.9	-60.9	-80.8	-119.1	-103.5
1	-77.8	-80.1	-85.6	-108.6	-84.0
10	-82.2	-104.8	-91.6	-112.0	-82.7
100	-112.7	-171.0	-138.0	-136.0	-112.7
1000	-148.7	<-200	<-200	-152.6	-151.0
10000	-155.0	<-200	<-200	-155.0	-190.9

Table 27.9 *Total Phase Noise*

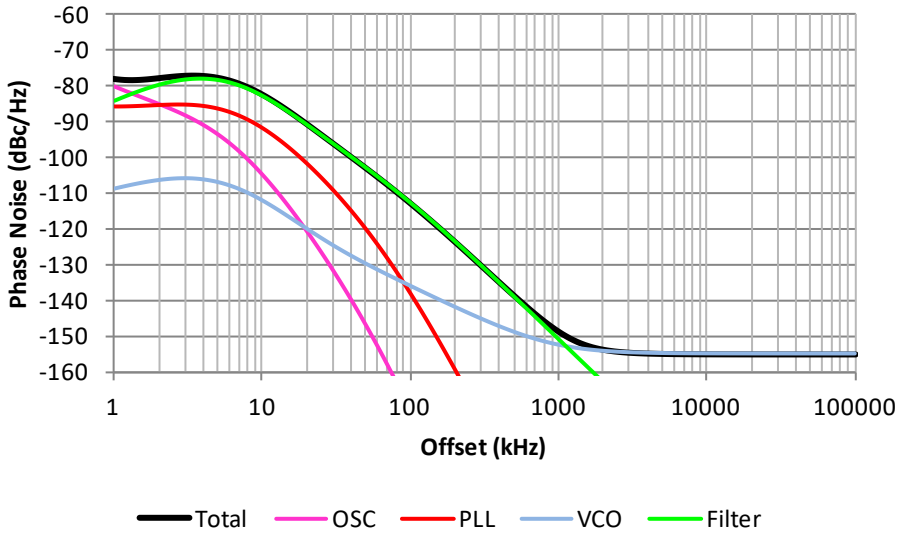


Table 27.10 *Total Noise Analysis*

In this case, the loop filter is actually dominating the phase noise. This is not typically the case, but happens here because the low phase detector causes the filter resistors to be unnecessarily large. In this case, a second order loop filter would have likely been just as good for spurs and the resistor noise could have been virtually eliminated. The following integrated metrics have also been calculated from a bandwidth of 1.7 kHz to 200 kHz.

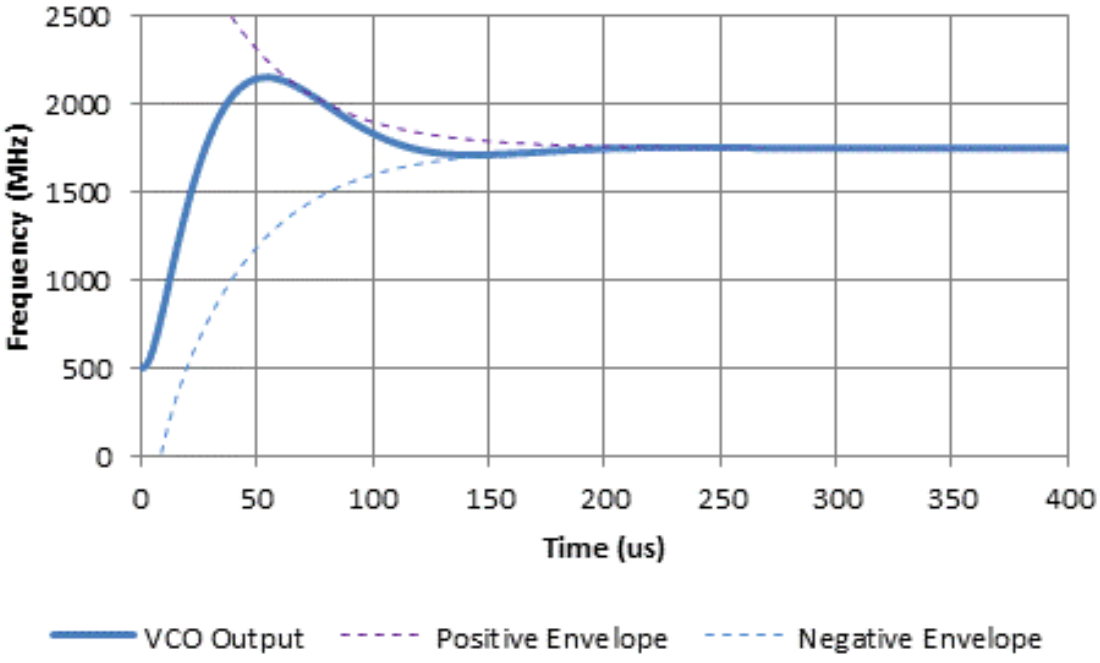
Parameter	Value
Jitter	3.2 ps
RMS Phase Error	1.04 degrees
Error Vector Magnitude	0.0002 %

Table 27.11 *Calculated Integrted Metrics*

Conclusion

The phase noise analysis has been presented in this chapter. The purpose of this analysis was not a reference design that is intended to be copied, but rather to show how to use the equations to calculate the phase noise.

Transient Response



Chapter 28 Transient Response of PLL Frequency Synthesizers

Introduction

This chapter considers the frequency response of a PLL when the ***N*** divider is changed. The phase detector is modeled as having a continuous analog output and it is assumed that the system is ideal; other factors will be discussed in later chapters. It starts out with the derivation of traditional second order approximations involving the natural frequency and damping factor and then relates them to phase margin and loop bandwidth. However, as these approximations are limited in accuracy, a more accurate higher order fourth order model involving the zero and all the poles is derived.

Derivation of Transfer Functions

The filter coefficients ***A0***, ***A1***, ***A2***, and ***A3*** were discussed in a previous chapter. Recall that the transfer function of the loop filter is as follows:

$$Z(s) = \frac{1 + s \cdot T2}{s \cdot [A3 \cdot s^3 + A2 \cdot s^2 + A1 \cdot s + A0]} \quad \textbf{(28.1)}$$

This leads to the following closed-loop transfer function:

$$CL(s) = \frac{K \cdot N \cdot (1 + s \cdot T2)}{A3 \cdot s^5 + A2 \cdot s^4 + A1 \cdot s^3 + A0 \cdot s^2 + K \cdot T2 \cdot s + K} \quad \textbf{(28.2)}$$

$$K = \frac{K_{PD} \cdot K_{VCO}}{N} \quad \textbf{(28.3)}$$

It should be noted that the ***N*** value to use in this equation is the ***N*** value corresponding to the final frequency value, not the initial frequency value or the frequency for which the loop filter was designed for.

Second Order Approximation to Transient Response

Classical PLL Transient Model

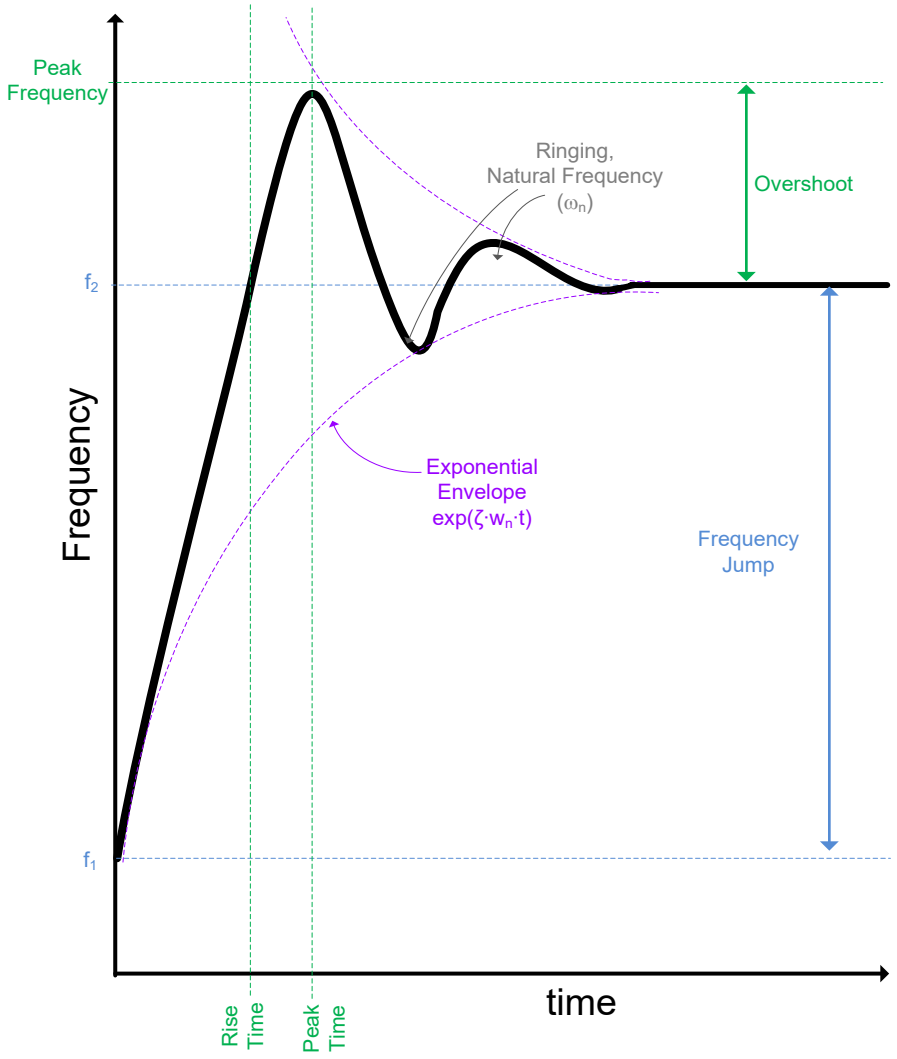


Figure 28.1 *Classical Model for the Transient Response of a PLL*

Figure 28.1 relates the PLL switching from frequency f_1 to frequency f_2 to classical control loop theory. The time that it takes the PLL to reach the intended frequency is called the *rise time*. The time that this takes is called the *peak time* The PLL will then continue on until it reaches the *peak frequency*. The absolute value of the difference of the peak frequency and final frequency is known as *overshoot*. From there, there will be damping and potential ringing until it reaches its final frequency. The absolute value of the difference of the start frequency and end frequency is called the *frequency jump* and the acceptable error to within which the PLL is considered to be locked is called the *tolerance*.

Derivation of Equations

To this point, no approximations have been made, and this form works up to a fourth order loop filter. In this section, ***CL(s)*** will be approximated by a second order expression, in order to derive results that give an intuitive feel of the transient response. The simplified second order expression for (28.2) involves neglecting the zero and higher order poles.

$$CL(s) \approx \frac{N \cdot {\omega_n}^2}{s^2 + 2 \cdot \zeta \cdot \omega_n \cdot s + {\omega_n}^2} \tag{28.4}$$

This assumes the following definitions.

$$\omega_n = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{N \cdot A0}} \tag{28.5}$$

$$\zeta = \frac{T2}{2} \cdot \omega_n \tag{28.6}$$

Assuming that $\zeta < 1$, the poles of this function are at:

$$-\zeta \cdot \omega_n \pm j \cdot \omega_n \cdot \sqrt{1 - \zeta^2} \tag{28.7}$$

Now consider a PLL, which is initially locked at frequency ***f1***, and then the ***N*** counter is changed such to cause the PLL to switch to frequency ***f2***. This event is equivalent to changing the reference frequency from ***f1/N*** to ***f2/N***, or multiplying (28.4) by a factor of ***(f2-f1)/(N·s)***. Using inverse Laplace transforms, it follows that the frequency response is:

$$F(t) = f2 + (f1 - f2) \cdot e^{-\zeta \cdot \omega_n \cdot t} \cdot \left[\cos\left(\omega_n \sqrt{1 - \zeta^2} \cdot t\right) + \frac{\zeta}{\sqrt{1 - \zeta^2}} \cdot \sin\left(\omega_n \sqrt{1 - \zeta^2} \cdot t\right)\right] \tag{28.8}$$

To find the peak time, take the derivative of (28.8) and set to zero. This yields the following equation.

$$PeakTime = \frac{\pi}{\omega_n \cdot \sqrt{1 - \zeta^2}} \tag{28.9}$$

The peak frequency can be found by substituting this expression for peak time into (28.8). The overshoot is found by subtracting the final frequency away from the peak frequency.

$$Overshoot = \frac{f2 - f1}{\sqrt{1-\zeta^2}} \cdot \exp\left(\frac{-\zeta \cdot \pi}{\sqrt{1-\zeta^2}}\right) \qquad \textbf{(28.10)}$$

The *rise time* is defined as the time when the PLL first reaches its final frequency, which can be found by setting the bracketed portion of (28.8) equal to zero and choosing the smallest positive result for the arctangent function.

$$RiseTime = \frac{\tan^{-1}\left(\frac{-\sqrt{1-\zeta^2}}{\zeta}\right)}{\omega_n\sqrt{1-\zeta^2}} \qquad \textbf{(28.11)}$$

To find the lock time, one first calculates the exponential envelope. This is first done by setting the derivative of expression in brackets in (28.8) to zero. Then this result is substituted back into this to find the following maximum value

$$Max\left\{ \cos\left(\omega_n\sqrt{1-\zeta^2}\cdot t\right) + \frac{\zeta}{\sqrt{1-\zeta^2}} \cdot \sin\left(\omega_n\sqrt{1-\zeta^2}\cdot t\right)\right\} = \frac{1}{\sqrt{1-\zeta^2}} \qquad \textbf{(28.12)}$$

Substituting this back into (28.8) and solving for the time yields the following expression for lock time.

$$Lock\ Time = \frac{-ln\left(\frac{tolerance \cdot \sqrt{1-\zeta^2}}{|f2-f1|}\right)}{\zeta \cdot \omega_n} \qquad \textbf{(28.13)}$$

The reader should be aware that although these equations are in a nice closed form solution, they are based on approximations and of limited accuracy.

Relating the Second Order Analysis to Reality

These formulae for the second order are presented not for their stunning accuracy, but rather so that the PLL transient response can be better related to traditional textbook theory. The closed loop formulas are easy to use with a convenient closed form derivation. However, the convenient derivation comes by neglecting the zero and some poles, which limits the accuracy.

The impact of neglecting the zero, T2, has the effect of sacrificing accuracy for the initial part of the lock time. This can be reasoned from the initial value theorem.

$$\lim_{s\to\infty} s \cdot F(s) = f(0^+) \tag{28.14}$$

The zero will become a dominant term and it has a large impact on the peak time and overshoot. The impact of neglecting this has a tendency to underestimate the overshoot and cause the equations to be off for the peak time.

The impact of neglecting the extra poles has the impact of causing the long term behavior to be off, which would translate to inaccuracies in lock time. This can be reasoned by the final value theorem.

$$\lim_{s\to 0} s \cdot F(s) = f(\infty) \tag{28.15}$$

In other words, these formulae are intended to be used in a casual sort of way and one should not let them instill a false sense of confidence. In a following section, the full simulation presented proves to be much more accurate. If the extra calculations prove to be inconvenient, there are also some quick rules of thumb based on phase margin and loop bandwidth that are presented that tend to give a better match to reality than the second order approximations.

Relationship between Phase Margin, Loop Bandwidth, Damping Factor, and Natural Frequency

For a second order filter, the following relationships exist for loop filters designed with γ=1, which is not always the case, but a fair assumption

$$\omega c = 2\pi \cdot BW \ = \ 2 \cdot \zeta \cdot \omega_n \tag{28.16}$$

$$sec\phi - tan\phi = \frac{1}{4 \cdot \zeta^2} \tag{28.17}$$

Phase Margin, ϕ	Damping Factor, ζ	Natural Frequency, ω_n
30.00 degrees	0.6580	0.7599·ωc
35.00 degrees	0.6930	0.7215·ωc
36.87 degrees	0.7071	0.7071·ωc
40.00 degrees	0.7322	0.6829·ωc
45.00 degrees	0.7769	0.6436·ωc
50.00 degrees	0.8288	0.6033·ωc
55.00 degrees	0.8904	0.5615·ωc
60.00 degrees	0.9659	0.5177·ωc
61.93 degrees	1.0000	0.5000·ωc
65.00 degrees	1.0619	0.4709·ωc
70.00 degrees	1.1907	0.4199·ωc

Table 28.1 *Relationship between Phase Margin, Damping Factor and Natural Frequency*

So by specifying the loop bandwidth in radians, ωc, and the phase margin, ϕ, the damping factor and natural frequency can be determined, and vice versa. As a matter of fact, one can re-define the damping factor and natural frequency based on the loop bandwidth and phase margin. Although these equations do not exactly coincide with (28.5) and (28.6) they are often used.

$$\zeta = \frac{1}{2 \cdot \sqrt{sec\phi - tan\phi}} \tag{28.18}$$

$$\omega_n = \frac{\omega c}{2 \cdot \zeta} \tag{28.19}$$

Fourth Order Transient Analysis

This analysis considers all the poles and zeros of the transfer function and gives the most accurate results. To start with, the transfer function in (28.2) is multiplied by ***(f2-f1)/(N·s)***. However, since these formulas are really referring to the phase response, and it is the frequency response that is sought, the whole transfer function is also multiplied by ***s*** to perform differentiation (frequency is the derivative of phase). The resulting expression is rewritten in the following form:

$$F(s) = s \cdot CL(s) \cdot \frac{f2 - f1}{N \cdot s} = \frac{K \cdot (f2 - f1) \cdot (1 + s \cdot T2)}{A3 \cdot s^5 + A2 \cdot s^4 + A1 \cdot s^3 + A0 \cdot s^2 + K \cdot T2 \cdot s + K} \qquad \textbf{(28.20)}$$

The challenge is finding the poles of the closed loop transfer function. The polynomial can be up to fifth order, depending on the loop filter order. *Abel's Impossibility Theorem* states that a closed form solution for polynomials of fifth and higher order cannot exist. Closed form solutions do exist for polynomials of fourth and lower order, although the fourth and third order equations are rather complicated. If the means are not available to solve for the poles, then one can approximate by reducing the order of the polynomial, until it is solvable.

The roots of the denominator correspond to the poles of the closed loop transfer function. For a loop filter of third order or lower, a closed form solution exists to find the poles. If the loop filter is fourth order, the polynomial is fifth order, the options are to use numerical methods to find the poles, or to approximate this as a fourth order polynomial by neglecting the highest order term. The transient response can be rewritten as follows.

$$F(s) = \sum_{i=0}^{4*} B_k \cdot \left[\frac{1}{s \cdot (s - p_i)} + \frac{T2}{s - p_i}\right] \qquad \textbf{(28.21)}$$

$$B_k = \frac{K \cdot (f2 - f1)}{A3*} \cdot \prod_{k \neq i} \frac{1}{p_i - p_k} \qquad \textbf{(28.22)}$$

The above formulas are for the fourth order filter, but are easily modified for lower order filters. For a third order filter, the summation index goes to 3 and the denominator for the coefficients is ***A2***. For a second order filter, the summation index goes to 2 and the denominator for the coefficients is ***A1***. Some of the coefficients $\boldsymbol{B_i}$ will be complex; however, they will combine in such a way that the final solution is real. Now since the poles need to be calculated for this, it will be assumed that they all have negative real parts. If this is not the case, then the design is unstable. Using this assumption that the design is stable, the transient response can be simplified. Also, if the simulator does not do this, the solution can be expressed with all real variables by applying Euler's formula:

$$e^{\alpha+j\cdot\beta} = e^{\alpha}\cdot(cos\beta + j\cdot sin\beta) \quad \textbf{(28.23)}$$

Assuming a stable system, the transient response is:

$$f(t) = f2 + \sum_{i=0}^{4*} B_i \cdot \exp(p_i \cdot t) \cdot \left(\frac{1}{p_i} + T2\right) \quad \textbf{(28.24)}$$

Additional Comments Regarding the Lock Time Formula

Understanding the Transient Curve and Phase Error

One observation regarding the transient curve is that the area above the final frequency will be equal to the area below the transient frequency.

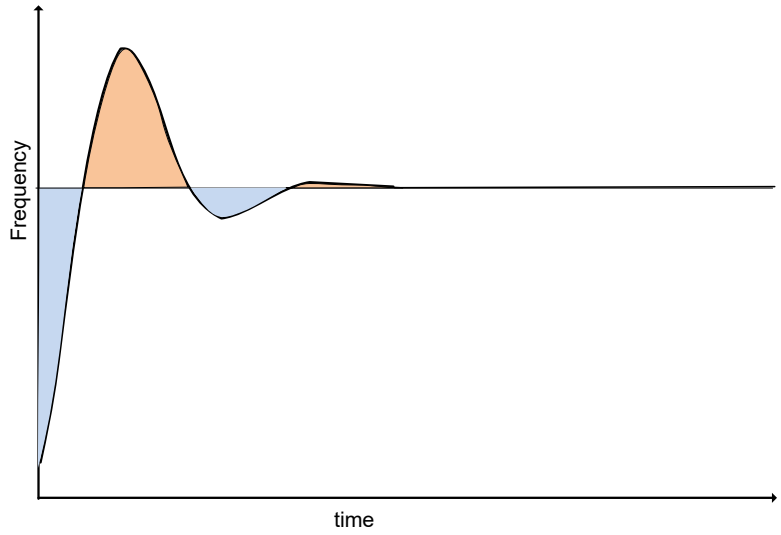


Figure 28.2 *Area under Transient Curve*

This is not a coincidence as phase is the integral of frequency and the PLL locks to phase. The exceptions to this rule can be when the PLL does not fully track the phase all the time, such as the case with cycle slipping or VCO calibration. These topics are discussed in later chapters.

Using the Exponential Envelope

(28.24) provides a complete analysis for the transient response, including all of the ringing of the PLL. However, for the purposes of lock time determination, it is better to eliminate the ringing from the equation and study only the exponential envelope. This makes the prediction of lock time more consistent. The exponential envelope is obtained by applying the triangle inequality to (28.24).

$$Exponential\ Envelope = f2 + \sum_{i=0}^{4*} \left| B_i \cdot \exp(p_i \cdot t) \cdot \left(\frac{1}{p_i} + T2 \right) \right| \qquad \textbf{(28.25)}$$

Dependence of Lock Time on Loop Bandwidth

Consider two loop filters that are designed for the same parameters, except for the second loop filter has a loop bandwidth of ***M*** times the loop bandwidth of the first filter. In this case, the scaling rule for loop filters apples. All the resistor values in the second filter will be ***M*** times the resistor values in the first filter and the capacitors values in the second filter will be $\boldsymbol{1/M^2}$ times the capacitor values of the first filter. Substituting this in for the definition of the filter coefficients yields the result that ***T2*** will be multiplied by a factor of ***1/M***, ***A0*** will be multiplied by $\boldsymbol{1/M^2}$, ***A1*** by $\boldsymbol{1/M^3}$, ***A2*** by $\boldsymbol{1/M^4}$, and ***A3*** by $\boldsymbol{1/M^5}$. It therefore follows that if ***p*** which makes the denominator in equation (28.20) equal to zero for the first filter, then ***M·p*** will make the denominator equal to zero for the second filter. Combining this information with formula (28.22) yields the result that the coefficients $\boldsymbol{B_i}$ are multiplied by a factor of ***M.*** Looking at formula (28.24), the factors of ***M*** all cancel out, except in the exponent. This proves that the transient response for the second loop filter will be identical to that of the first, except for the time axis is scaled by a factor of ***1/M***. The grand result of all this analysis is that it proves that the lock time is inversely proportional to the loop bandwidth, and that the overshoot (undershoot) will theoretically remain exactly the same.

Dependence of Lock Time on the Frequency Jump

The quantity |***f2 - f1***| is the frequency jump. Now consider the same loop filter. For the first lock time measurement, the transient response is recorded. For the second lock time measurement, the final frequency, ***f2***, is kept constant, but the initial frequency, ***f1***, is changed such that the frequency jump is increased by a factor of ***M***, equation (28.22) and (28.24) will be the same for both cases, except for the fact that the coefficients for $\boldsymbol{A_i}$ in the second case will be multiplied by a factor of ***M***. This implies that the transient response will be the same for both cases, except for in the second case, the ringing is multiplied by a factor of ***M***. If the frequency tolerance is also scaled by a factor of ***M***, then the lock time will also be the same. If it is not scaled, then the lock time will be longer, provided ***M***>1.

Coarse Rules of Thumb for Lock time

Although (28.24) is very complete, it is difficult to apply without the aid of computers. It has been shown that lock time is inversely proportional to the loop bandwidth and that the lock time does not change if the frequency jump and frequency tolerance are scaled in equal amounts. Simulations also show optimal lock time occurs with a phase margin around 48 degrees. After running many simulations and seeing general trends, some very simple rules of thumb can be derived that are easy to use for fast approximations.

$$Lock\ Time\ \approx \frac{4}{BW} \tag{28.26}$$

$$Peak\ Time\ \approx \frac{0.8}{BW} \tag{28.27}$$

$$Overshoot\ \approx \frac{|f2 - f1|}{3} \tag{28.28}$$

Simulation vs. Measured Results

Figure 28.5 and Figure 28.6 show the simulated and measured results. Care was taken to ensure that sources of error were eliminated including C0G capacitors, accounting for the VCO input capacitance, measuring the VCO gain, and keeping the charge pump voltage away from the supply rails. When capacitor C2 was changed to X7R dielectric, the lock time increased from 489 µS to 578 µS.

Parameter	2nd Order Approximation	Coarse Rules	Full Simulation	Actual Measurement
Parameters	ζ =0.815 ω_n = 3.069 kHz	BW = 5 kHz ϕ = 48.77 deg	n/a	n/a
Rise Time (µs)	210	n/a	48.5	~50
Peak Time (MHz)	266	160	93	90
Peak Frequency (MHz)	905.3	908.3	908	908
Overshoot (MHz)	0.3	3.3	3	3
Lock Time (µs)	636	800	446 (actual) 485 (envelope)	489

Table 28.2 *Simulated and Calculated Lock Time Comparison*

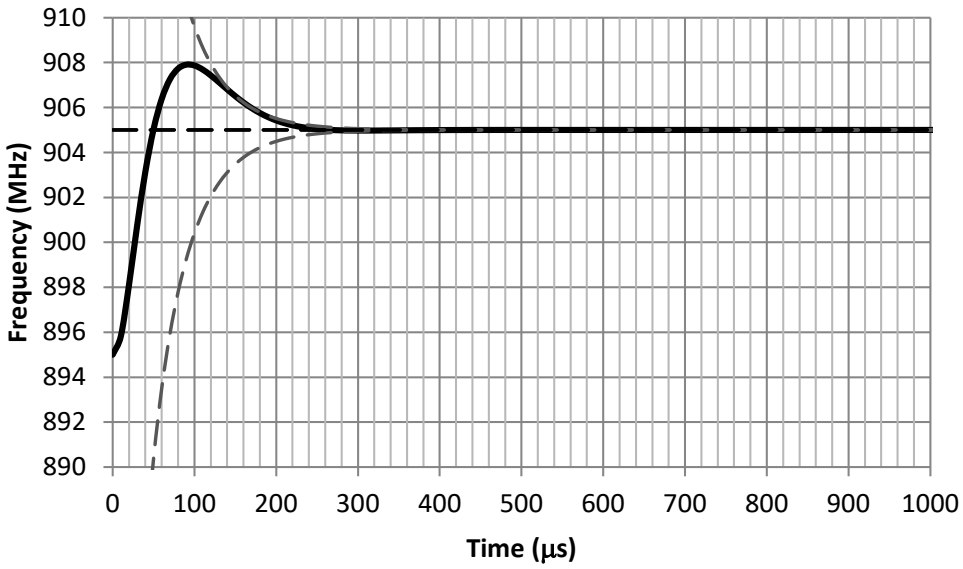


Figure 28.3 *Theoretical Peak Time of 93 µs to Peak Frequency of 908 MHz*

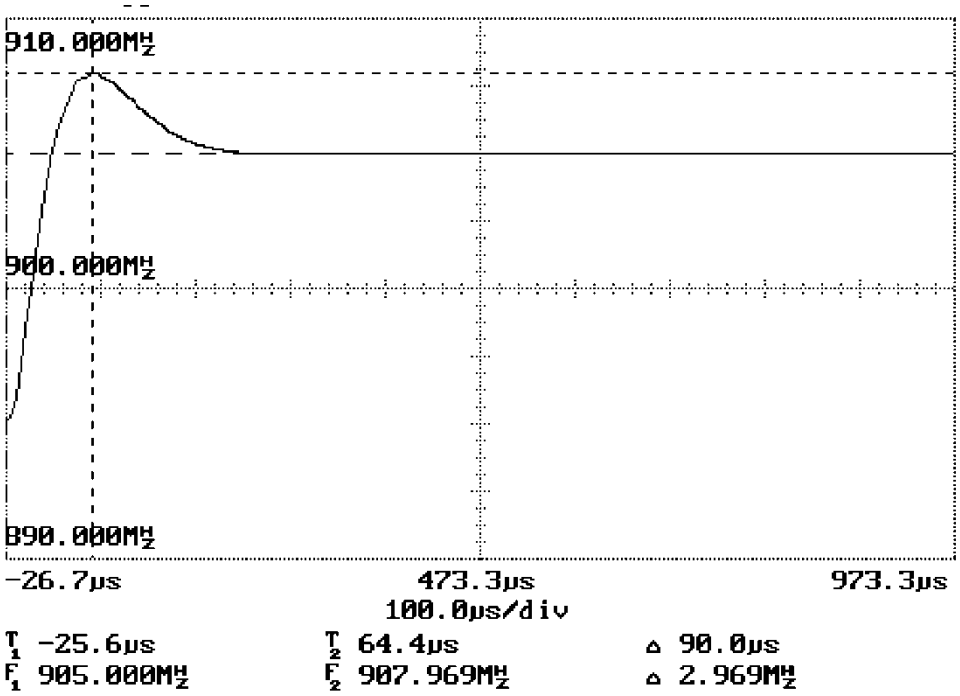


Figure 28.4 *Actual Peak Time of 90 µs to Peak Frequency of 908 MHz*

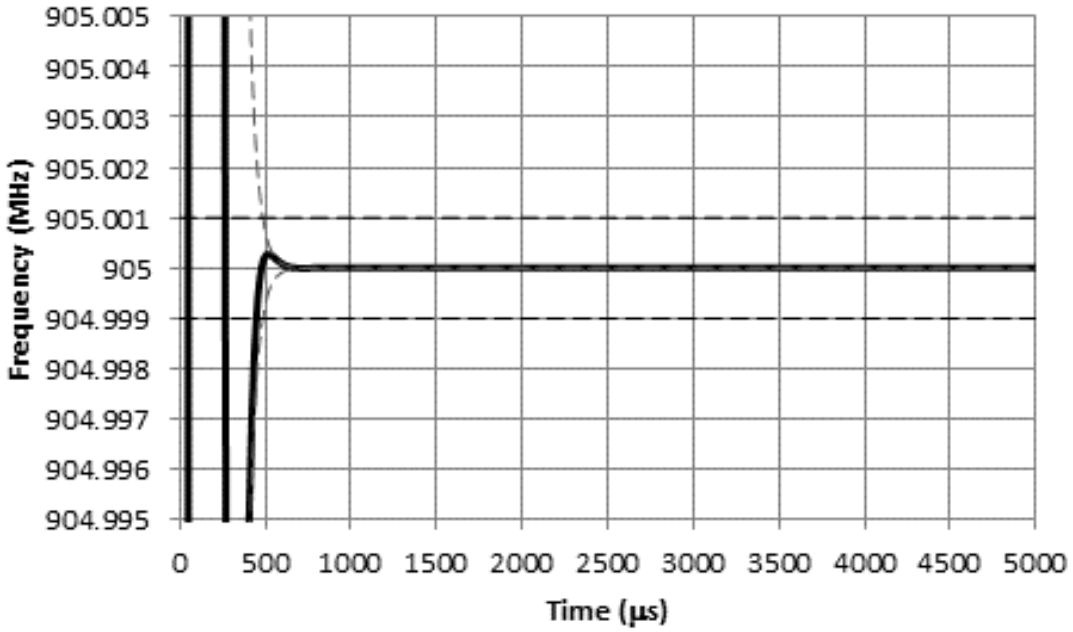


Figure 28.5 *Theoretical Lock Time to 1 kHz Tolerance is 446 µs*

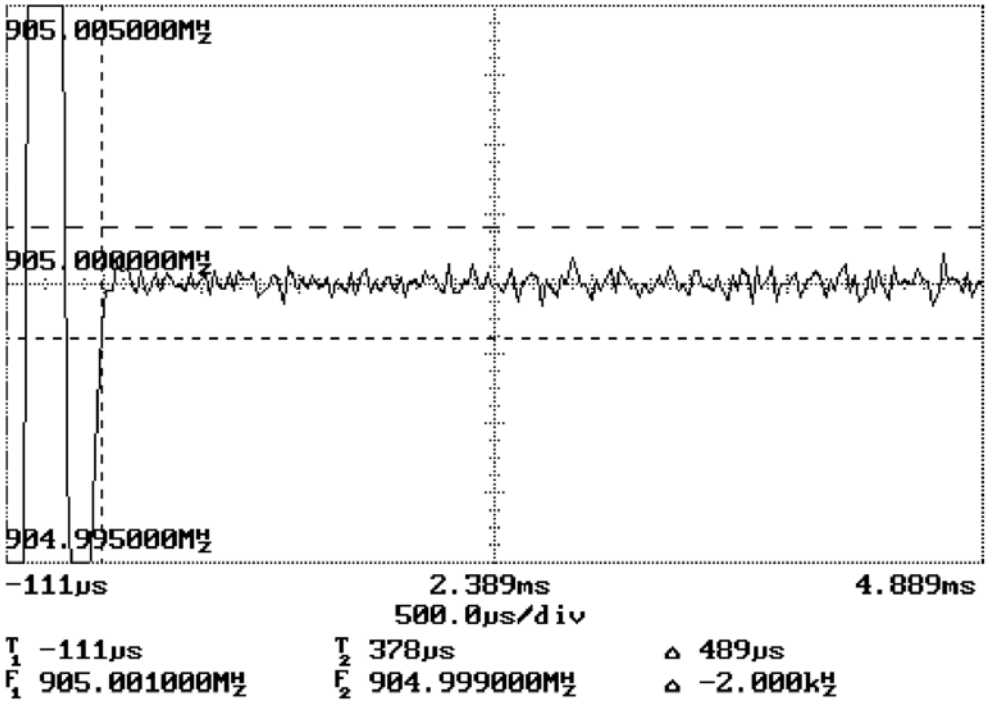


Figure 28.6 *Actual Lock Time to 1 kHz Tolerance is 449 υS*

Factors that Can Degrade Lock Time

Simulations are only as good as the information that goes into them. The model presented does a perfect job at modeling the transient response given the assumptions it was based on. In cases where the simulation does not match the measurement, it makes sense to investigate some of the factors that the model does not account for, which is discussed in the next several paragraphs.

VCO and Charge Pump Non-linearity

Perhaps the biggest real world effect that could throw off this analysis is the non-linear characteristics of the VCO and the charge pump. When switching from one frequency to another, there is typically overshoot in the order of one third of the frequency jump. This overshoot is dependent on the phase margin/damping factor. If the VCO overshoots too far past its intended range for usage, or if the tuning voltage ever gets too close (about 0.5 V) to the supply rails for the charge pump, the first lobe of the transient response gets longer and increases the lock time. The designer should be aware that if overshoot causes the frequency to go outside the tuning range of the VCO, the modeled prediction could lose accuracy. To deal with this, design for a higher phase margin in order to decrease the overshoot.

VCO Input Capacitance

The VCO input capacitance adds in parallel with the capacitor that it is next to. If not accounted for, this could distort the results. This tends to decrease the loop bandwidth, and therefore increase the lock time.

Capacitor Dielectric Absorption

The simulations presented in this chapter assume ideal capacitors. In addition to real world capacitors not being exactly on the correct value, they have other undesired properties. Dielectric absorption is a property of capacitors. In order to test dielectric absorption, a voltage is applied, and then a short is placed across the capacitor and removed. Parts with a low dielectric absorption will have a smaller residual voltage develop across than ones with a larger dielectric absorption. Dielectrics such as NP0 and Film have good performance in this respect. However, for larger capacitor values, it is often necessary to use a lower performance dielectric like X7R. These dielectrics can drastically increase lock times. Some PLL designs seem completely immune to the impact of dielectrics, while others can have the lock time double or increase even more. If the actual lock time is substantially longer than the theoretical lock time, then replace the capacitors, especially capacitor ***C2***, with ones of higher quality. For the example previously given, using a higher dielectric absorption capacitor for component ***C2*** increased the lock time from 489 μS to 578 μS.

Phase Detector Discrete Sampling Effects

The discrete sampling effects of the phase detector usually have little bearing on the lock time, provided that the phase detector frequency is larger than about 10 times the loop bandwidth and less than 100 times the loop bandwidth. Nevertheless, there are those situations where these factors are important. The discrete time model is presented in a later chapter. Although, the discrete model is more accurate, the analog model presented in this chapter is still very useful because it is much faster to calculate and gives one a better insight into what impacts the lock time without relying completely on computer simulations.

When an instantaneous phase error is presented to the phase detector, then *cycle slipping* can occur. When the ***N*** divider value changes, then the phase of the VCO signal divided by ***N*** will initially be incorrect in relation to the crystal reference signal divided by R. If the loop bandwidth is very small (around 1%) relative to the phase detector frequency, then this phase error will accumulate faster than the PLL can correct for it and eventually cause the phase detector to put out a current correction of the wrong polarity. By dividing the phase detector frequency by the instantaneous phase error presented to the phase detector, one can approximate how many cycles it would take the phase detector to cycle slip. If this time is less than about half the rise time of the PLL, then cycle slipping is likely to occur. An easier rule of thumb that is less accurate is that cycle slipping tends to occur when the loop bandwidth is less than 1% of the phase detector frequency. Cycle slips are somewhat rare in integer PLL designs, but are common with fractional N PLL designs, since they typically run at higher comparison frequencies. Many PLLs from Texas Instruments have features such as cycle slip reduction and Fastlock that reduce the effects of cycle slipping significantly or even completely.

Other Comments

There are some other factors that can have a lesser impact on lock time. Charge pump mismatch and charge pump leakage can slow lock time, but only if they are pretty severe. Some capacitors or VCOs can have leakage that can also slow lock time.

Conclusion

This chapter has gone through a rigorous derivation of the equations involved in predicting lock time and the transient response of the PLL when the N divider is changed. A second order and a fourth order model were presented. For the fourth order model, discrepancies between theoretical lock times and measured lock times are on the order of 10 - 20% or less. If theoretical lock times and measured lock times closely agree, then this indicates that this is the best the PLL can do. However, if there is a large discrepancy, it makes sense to check and make sure that there is not some factor that is making the lock time worse than it could be.

Appendix

The Relationship between Natural Frequency (ωn), Damping Factor (ζ), Loop Bandwidth (ωc) , and Phase Margin (ϕ)

The strategy for this derivation is to eliminate the parameters ***T1***, ***T2***, ***A0***, and ***A1*** in order to find the desired relationship. These are all under the assumption that gamma is unity.

$$\gamma = \omega c^2 \cdot T2 \cdot \frac{A1}{A0} \approx 1 \tag{28.29}$$

$$\zeta = \frac{T2}{2} \cdot \omega_n \tag{28.30}$$

$$\omega n = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{N \cdot A0}} \tag{28.31}$$

$$\frac{K_{PD} \cdot K_{VCO}}{N \cdot \omega c^2 \cdot A0} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{1 + \omega c^2 \cdot T1^2}} = 1 \tag{28.32}$$

$$\pi - tan^{-1}(\omega c \cdot T2) + tan^{-1}(\omega c \cdot T1) = \phi \tag{28.33}$$

$$\frac{A1}{A0} = T1 \tag{28.34}$$

Eliminating ***A1*** and ***A0*** yields the following new equations:

$$\omega c^2 \cdot T2 \cdot T1 = 1 \tag{28.35}$$

$$\zeta = \frac{T2}{2} \cdot \omega_n \tag{28.36}$$

$$\frac{\omega n^2}{\omega c^2} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{1 + \omega c^2 \cdot T1^2}} = 1 \tag{28.37}$$

$$T1 = \frac{sec\phi - tan\phi}{\omega c} \tag{28.38}$$

T2 and ***T1*** can be eliminated as follows:

$$T2 = \frac{2 \cdot \zeta}{\omega n} \tag{28.39}$$

$$T1 = \frac{\omega n}{2 \cdot \zeta \cdot \omega c^2} \tag{28.40}$$

These values can be substituted in:

$$\left[4 \cdot \zeta^2 \cdot \left(\frac{\omega n}{\omega c}\right)^2 - 1\right] + \left[\left(\frac{\omega n}{\omega c}\right)^4 - \frac{1}{4 \cdot \zeta^2} \cdot \left(\frac{\omega n}{\omega c}\right)^2\right] = 0 \tag{28.41}$$

This can be written as follows:

$$\left[4 \cdot \zeta^2 \cdot \left(\frac{\omega n}{\omega c}\right)^2 - 1\right] \cdot \left[1 + \frac{1}{4 \cdot \zeta^2} \cdot \left(\frac{\omega n}{\omega c}\right)^2\right] = 0 \tag{28.42}$$

Looking at the bracketed left hand term and solving:

$$\frac{\omega n}{\omega c} = \frac{1}{2 \cdot \zeta} \quad \Rightarrow \quad \omega c = 2 \cdot \zeta \cdot \omega n \tag{28.43}$$

This result can be combined with other equations to find the relationship for phase margin.

$$sec\phi - tan\phi = \frac{1}{4 \cdot \zeta^2} \tag{28.44}$$

Appendix B Calculations for Transient Response

Introduction

Parameter	Description	Value	Unit
K_{PD}	Charge Pump Gain	1	mA
K_{VCO}	VCO Gain	18	MHz/V
f_{PD}	Phase Detector Frequency	200	kHz
N	Feedback Divide	4525	n/a
f_2	Final Frequency	905	MHz
f_1	Starting Frequency	895	MHz
C1	Loop Filter Capacitor	0.47	pF
C2	Loop Filter Capacitor	10	nF
C3*	Loop Filter Capacitor (excluding VCO Input Capacitance)	0.180	nF
C_{VCO}	VCO Input Capacitance	0.047	nF
C3	Loop Filter Capacitor (including VCO Input Capacitance)	0.227	nF
R2	Loop Filter Resistor	8.2	kΩ
R3	Loop Filter Resistor	27	kΩ
Tolerance	Acceptable frequency error	1	kHz

The first step is to define the following constants. Be aware that the frequency used to calculate the ***N*** value is the final frequency.

$$N = \frac{f_2}{f_{PD}} \quad \textbf{(28.45)}$$

$$K = \frac{K_{PD} \cdot K_{VCO}}{N} \quad \textbf{(28.46)}$$

$$T2 = \frac{K_{PD} \cdot K_{VCO}}{N} \quad \textbf{(28.47)}$$

$$A0 = C1 + C2 + C3 \quad \textbf{(28.48)}$$

$$A1 = C2 \cdot R2 \cdot (C1 + C3) + C3 \cdot R3 \cdot (C1 + C2) \quad \textbf{(28.49)}$$

$$A2 = C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3 \cdot R4 \quad \textbf{(28.50)}$$

Symbol	Description	Value	Units
N	N Value for final settling frequency	4575	n/a
K	Constant	3.978	$\frac{1}{s \cdot \Omega}$
T2	Loop Filter Zero	8.2×10^{-5}	s
A0	Loop Filter Constant	10.697	nF
A1	Loop Filter Constant	1.213×10^{-4}	s·nF
A2	Loop Filter Constant	2.362×10^{-10}	s^2·nF

The loop bandwidth, phase margin, and gamma are calculated with the methods presented so far.

Symbol	Description	Value	Units
BW	Loop Bandwidth in kHz	5	kHz
ωc	Loop Bandwidth in radian	795.85	rad
ϕ	Phase Margin	48.77	deg
γ	Gamma Optimization Factor	0.9181	n/a

Second Order Approximation

The damping factor and natural frequency can also be calculated directly from components.

$$\omega_n = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{N \cdot A0}} \tag{28.51}$$

$$\zeta = \frac{T2}{2} \cdot \omega_n \tag{28.52}$$

Once these are known, the second order calculations can be easily done.

$$PeakTime = \frac{\pi}{\omega_n \cdot \sqrt{1 - \zeta^2}} \tag{28.53}$$

$$Overshoot = \frac{f2 - f1}{\sqrt{1 - \zeta^2}} \cdot \exp\left(\frac{-\zeta \cdot \pi}{\sqrt{1 - \zeta^2}}\right) \tag{28.54}$$

$$RiseTime = \frac{\tan^{-1}\left(\frac{-\sqrt{1-\zeta^2}}{\zeta}\right)}{\omega_n\sqrt{1-\zeta^2}} \quad \textbf{(28.55)}$$

$$Lock\ Time = \frac{-ln\left(\frac{tolerance \cdot \sqrt{1-\zeta^2}}{|f2-f1|}\right)}{\zeta \cdot \omega_n} \quad \textbf{(28.56)}$$

Parameter	2nd Order Approximation	Units
ζ	0.815	n/a
ω_n	3.069	kHz
Rise Time	210	µs
Peak Time	266	MHz
Peak Frequency	905.3	MHz
Overshoot	0.3	MHz
Lock Time	636	µs

The next step is to find the poles of the closed loop transfer function. In this case, it would involve solving a fourth order polynomial.

$$A2 \cdot p^4 + A1 \cdot p^3 + A0 \cdot p^2 + K \cdot T2 \cdot p + K \quad \textbf{(28.57)}$$

Symbol	Description	Value	Units
$K \cdot T2$	Constant	3.262×10^{-4}	$\frac{1}{\Omega}$
p_0	Closed Loop Transfer Function Pole	-4.115×10^5	rad/s
p_1	Closed Loop Transfer Function Pole	-5.385×10^4	rad/s
p_2	Closed Loop Transfer Function Pole	$-2.189 \times 10^4 - j \cdot 1.49 \times 10^4$	rad/s
p_3	Closed Loop Transfer Function Pole	$-2.189 \times 10^4 + j \cdot 1.49 \times 10^4$	rad/s

Calculate the Closed Loop Transfer Function Constants

$$B_0 = \frac{K \cdot (f2 - f1)}{A2 \cdot (p_0 - p_1) \cdot (p_0 - p_2) \cdot (p_0 - p_3)} \quad \textbf{(28.58)}$$

$$B_1 = \frac{K \cdot (f2 - f1)}{A2 \cdot (p_1 - p_0) \cdot (p_1 - p_2) \cdot (p_1 - p_3)} \quad \textbf{(28.59)}$$

$$B_2 = \frac{K \cdot (f2 - f1)}{A2 \cdot (p_2 - p_0) \cdot (p_2 - p_1) \cdot (p_2 - p_3)} \quad \textbf{(28.60)}$$

$$B_3 = \frac{K \cdot (f2 - f1)}{A2 \cdot (p_3 - p_0) \cdot (p_3 - p_1) \cdot (p_3 - p_2)} \quad \textbf{(28.61)}$$

Symbol	Description	Value	Units
B_0	Transient Function Constant	-3.137×10^9	$\frac{1}{s^2}$
B_1	Transient Function Constant	3.074×10^{11}	$\frac{1}{s^2}$
B_2	Transient Function Constant	$-1.521 \times 10^{11} + j \cdot 3.35 \times 10^{11}$	$\frac{1}{s^2}$
B_3	Transient Function Constant	$-1.521 \times 10^{11} - j \cdot 3.35 \times 10^{4}$	$\frac{1}{s^2}$

Calculate the Transient Response and Exponential Envelope

The transient response F(t) and the exponential envelope, E(t) can now be calculated.

$$F(t) = f2 + \sum_{i=0}^{3} B_i \cdot \left(\frac{1}{p_i} + T2\right) \cdot \exp(p_i \cdot t) \quad \textbf{(28.62)}$$

$$E(t) = f2 + \sum_{i=0}^{3} \left| B_i \left(\frac{1}{p_i} + T2\right) \cdot \exp(p_i \cdot t) \right| \quad \textbf{(28.63)}$$

Chapter 29 Impact of PFD Discrete Sampling Effects on the Transient Response

Introduction

The analog model for the transient response assumes that the charge pump puts out a continuous current that is proportional to the phase error. This model serves as a good approximation provided that the loop bandwidth of the PLL is between one-tenth and one-hundredth of the phase detector frequency. In cases where this is violated, it becomes more important to account for the discrete sampling effects of the charge pump by modeling the output as a pulse width modulated signal as opposed to a continuous analog current. This chapter models the lock time in a discrete fashion and investigates some of the discrete effects of the charge pump on lock time.

High Level Overview of the Model Derivation

The discrete lock time model for lock time is well suited for computer modeling because it creates a set of difference equations. These are the steps used in deriving the model.

- Define all voltages across the capacitors
- Derive the differential equations involved
- Convert the differential equations to difference equations
- Solve the system by incrementing in small discrete time steps

Deriving the Nomenclature

Although a trivial step, defining the problem in the right way simplifies the analysis. The easiest convention to use is to define all the voltages to be across the capacitors, and all the currents to be through the capacitors. For instance, ***V1*** stands for the voltage across capacitor ***C1***, and ***i1*** stands for the current through capacitor ***C1***. Once this is done, the equations are easy to derive.

Deriving the Equations for the Brute Force Method

The first step is to initialize all voltages to zero. This corresponds to initializing the problem so that the PLL is considered to be locked before the frequency change is initiated. The next thing that needs to be done is to derive equations to calculate the new change in voltages from the old voltages. These voltages are added to the old voltages in order to compute the new voltages. The new VCO frequency can be calculated from this, and from the VCO frequency, the new phase at the N counter can be calculated. It simplifies things to think of this phase in terms of cycles, not radians. This phase can be calculated by adding the product of the time step times the frequency. From this, the charge pump state can be calculated and then the whole process is repeated for the next time step.

Step 1: Initialize all States

Define all states and voltages to be zero. Define a time increment, which should be much smaller than the period of the phase detector frequency. Define the initial frequency of the VCO to be the starting frequency.

Step 2: Determine the new charge pump state and current

Define this as *CPout*. A charge pump event occurs when the phases of one of the inputs to the phase detector exceeds one and it causes the phase detector to change states

Step 3: Determine the new voltage at the VCO

For example, in a second order filter the following equations hold:

$$CPout = i1 + i2 \tag{29.1}$$

$$i1 = \frac{1}{C1} \cdot \frac{\Delta V1}{\Delta t} \tag{29.2}$$

$$i2 = \frac{1}{C2} \cdot \frac{\Delta V2}{\Delta t} \tag{29.3}$$

$$V1 = V2 + i2 \cdot R2 \tag{29.4}$$

Now these equations can be combined to solve for ***ΔV1*** and ***ΔV2***. Once these are known, the new VCO frequency can be found. The table below shows the values for various orders of active and passive loop filters. These are found using the brute force method. This method may take a lot of computer time, but will give an accurate result, provided that step size ***Δt*** is sufficiently small.

Filter Order		
	2nd	$$\Delta V2 = \frac{\Delta t \cdot (V1 - V2)}{C2 \cdot R2}$$ $$\Delta V1 = \frac{\Delta t \cdot CPout - C2 \cdot \Delta V2}{C1}$$
	3rd	$$\Delta V3 = \frac{\Delta t \cdot (V1 - V3)}{C3 \cdot R3}$$ $$\Delta V2 = \frac{\Delta t \cdot (V1 - V2)}{C2 \cdot R2}$$ $$\Delta V1 = \frac{\Delta t \cdot CPout - C2 \cdot \Delta V2 - C3 \cdot \Delta V3}{C1}$$
	4th	$$\Delta V4 = \frac{\Delta t \cdot (V3 - V4)}{C4 \cdot R4}$$ $$\Delta V3 = \frac{\Delta t \cdot (V1 - V3)}{C3 \cdot R3} - \frac{C4 \cdot \Delta V4}{C3}$$ $$\Delta V2 = \frac{\Delta t \cdot (V1 - V2)}{C2 \cdot R2}$$ $$\Delta V1 = \frac{\Delta t \cdot CPout - C2 \cdot \Delta V2 - C3 \cdot \Delta V3 - C4 \cdot \Delta V4}{C1}$$

Table 29.1 *Discrete Lock Time Formulae for a Passive Filter*

Step 4: Calculate the new VCO frequency

The tuning voltage will be the voltage across the highest order capacitor.

Step 5: Calculate the New Phases for the Inputs of the Phase Detector

Recalling that 1 Hz is one cycle per second, calculated the fraction of added cycles by multiplying the frequency times the time step and adding it to the current number of cycles. If this cycle exceeds one, consider a charge pump event. Now return to step 2.

Comments Regarding Computational Accuracy of the Brute Force Method

The accuracy of the computations is limited by the size of the time step Δt. This typically requires a time step that is too small to be practical. However, the transient response that happens up to the peak time is the part that is most impacted by the discrete sampling effects of the charge pump. This portion of the transient response is of the most interest when studying discrete sampling effects and is also much less sensitive to the step size. Using solution methods like Runga-Kutta do not really improve the accuracy because the limiting factor is that there should be at least 8 time cycles within the amount of time the charge pump comes on in order to get a good final settling frequency tolerance. One trick to improve this is to make the size of the time step dynamic such that the resolution is finer near the times the charge pump is on. Another good trick is to bail out of the routine once the frequency is close and there are less than 8 time steps in one charge pump event. If one studies the analog simulation, the increase in lock time due to discrete sampling effects will be roughly equal to the increase in the peak time due to discrete sampling effects. Now although this method will converge to the exact solution provided that the time step, Δt, is small, it takes a very large amount of iterations and takes a while, even with modern computers.

Improvements to the Brute Force Method

Although the brute force method may be intuitive, it has the disadvantages of slower computational time and also requires different formulae based on different filter topologies and for active and passive filters. To improve upon this, the computational speed and accuracy can be improved by calculating the voltages as an exact function of the time step Δt, instead of using an approximation that depends on the time step being very small.

The first reaction may be that the mathematics is hideously complicated, and indeed this is the case. The fourth order passive filter would involve four voltages, and each one interacts with the others to make it a very involved problem. However, there is relief in the fact that it is not necessary to know all of these voltages to know the output voltage, provided that no resistors or components are switched in or out during the time that the PLL is locking. Even if this is the case, the fast locking mode can be modeled as well as the steady state mode. All of these types of routines produce a glitch when they are disengaged, so it proves little to try to add this in the model.

The key assumption is to transform the loop filter into one that the poles are separated. In the case of a fourth order loop filter, it is a rare possibility that the transformed values for ***R3*** and ***R4*** will be complex. In this pathological case, the mathematics still holds. In order to transform this filter, the zero, poles, and loop filter coefficients must first be calculated.

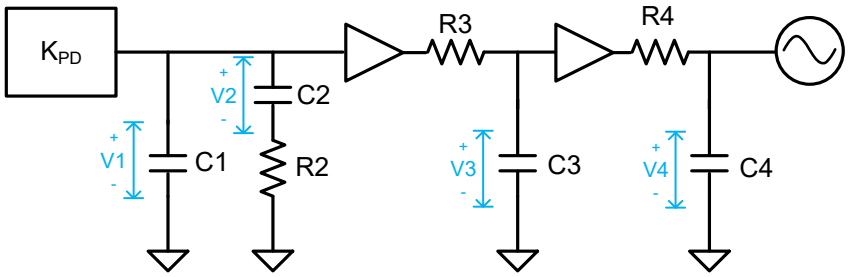


Figure 29.1 *Circuit Used to Simplify Discrete Lock Time Calculations*

The components for this analysis can be calculated from the loop filter time constants as follows:

$$C1 = A0 \cdot \frac{T1}{T2} \tag{29.5}$$

$$C2 = A0 - C1 \tag{29.6}$$

$$R2 = \frac{T2}{C2} \tag{29.7}$$

$$C3 = 1\,nF \tag{29.8}$$

$$R3 = \frac{T3}{C3} \tag{29.9}$$

$$C4 = 1\,nF \tag{29.10}$$

$$R4 = \frac{T4}{C4} \tag{29.11}$$

After the virtual components are calculated, it is then necessary to understand the impact of injecting a current of magnitude, ***CPout***, and duration ***Δt*** on the various voltages of the capacitors in loop. This can be done by simply taking the inverse Laplace Transform of the transfer function and modeling the charge pump on time as a rectangular pulse. AMP represents the op amp gain, which is one in all cases but the Active C Filter.

From these functions, the voltage can be calculated exactly. The positive transitions on the phase detector due to the rising edges of the R counter are known. For the N counter, one method is to approximate this by the phase error. For numerical methods, use half the phase error for the first iteration, and then keep dividing this phase error by 2, until the tolerance on the time error is acceptable. Although the formulas for the third and fourth order filter look especially brutal, dealing with these is actually less effort than tinkering to improve computational accuracy and speed the other way. The only disadvantage of doing it this way is that the formulas are a little more work to use and that these approximations would break down if a component was switched in during Fastlock. In the case that a component is switched in, the glitch caused by doing so is usually very difficult to model, and therefore this model could be applied to the time before and the time after the component was switched in. However, there would be no problem if only the charge pump current or the phase detector frequency was changed.

		Voltage Calculations
Filter Order	V2	$V2_{New} = V2_{Old} + \frac{CPout \cdot \Delta t}{C2}$
	V1	$V1_{Initial} = V2_{Old} + exp\left(-\frac{\Delta t}{T1}\right) \cdot (V1_{Old} - V2_{Old})$ $V1_{Transient} = \frac{CPout}{C2} \cdot (T2 - T1) \cdot \left(1 - exp\left(-\frac{\Delta t}{T1}\right)\right)$ $V1_{New} = V1_{Initial} + V1_{Transient}$
	V3	$V3_{Initial} = \frac{AMP}{C1 + C2} \cdot [V1_{Old} \cdot C1 + V2_{Old} \cdot C2]$ $+\frac{AMP \cdot exp\left(-\frac{\Delta t}{T1}\right)}{C1 + C2} \cdot \left[V1_{Old} \cdot C1 \cdot \left(\frac{T2}{T1} - 1\right) - V2_{Old} \cdot C2\right]$ $+\frac{AMP \cdot exp\left(-\frac{\Delta t}{T3}\right)}{C1 + C2} \cdot \left[-V1_{Old} \cdot C1 \cdot \left(\frac{T2}{T3} - 1\right) - V2_{Old} \cdot C2\right]$ $+V3_{Old} \cdot exp\left(-\frac{\Delta t}{T3}\right)$ $V1_{Transient} = \frac{CPout \cdot AMP}{C1 + C2} \cdot \left[T2 - T1 - T3 + \Delta t + \frac{(T1 - T2) \cdot T1 \cdot exp\left(-\frac{\Delta t}{T1}\right) + (T2 - T3) \cdot T3 \cdot exp\left(-\frac{\Delta t}{T3}\right)}{T1 - T3}\right]$ $V3_{New} = V3_{Initial} + V3_{Transient}$

	V4	$\Delta VC4_{\text{No Initial Conditions}} = \frac{CPout \cdot A}{C1+C2} \cdot \left[T2 - T1 - T3 - T4 + \Delta t + \frac{(T1-T2)\cdot T1^2 \cdot e^{-\Delta t/T1}}{(T1-T3)\cdot(T1-T4)} + \frac{(T2-T3)\cdot T3^2 \cdot e^{-\Delta t/T3}}{(T1-T3)\cdot(T3-T4)} - \frac{(T2-T4)\cdot T4^2 \cdot e^{-\Delta t/T41}}{(T1-T4)\cdot(T3-T4)} \right]$ $V4_{Initial} = \frac{AMP}{C1+C2} \cdot [V1_{Old} \cdot C1 + V2_{Old} \cdot C2]$ $- \frac{AMP \cdot exp\left(-\frac{\Delta t}{T1}\right)}{C1+C2} \cdot \left[\frac{V1_{Old} \cdot C1 \cdot (T2-T1) - V2_{Old} \cdot C2 \cdot T1}{(T1-T3)\cdot(T3-T4)}\right]$ $+ \frac{AMP \cdot exp\left(-\frac{\Delta t}{T3}\right)}{C1+C2} \cdot \left[\frac{V1_{Old} \cdot C1 \cdot (T2-T3) - V2_{Old} \cdot C2 \cdot T3}{(T1-T3)\cdot(T3-T4)}\right]$ $+ \frac{AMP \cdot exp\left(-\frac{\Delta t}{T4}\right)}{C1+C2} \cdot \left[\frac{V1_{Old} \cdot C1 \cdot (T2-T4) - V2_{Old} \cdot C2 \cdot T4}{(T1-T3)\cdot(T3-T4)}\right]$ $+ V4_{Old} \cdot exp\left(-\frac{\Delta t}{T4}\right)$ $V4_{Transient} = \frac{CPout \cdot AMP}{C1+C2} \cdot \left[T2 - T1 - T3 - T4 + \Delta t + \frac{(T1-T2)\cdot T1^2 \cdot exp\left(-\frac{\Delta t}{T1}\right)}{(T3-T1)\cdot(T4-T1)} + \frac{(T2-T3)\cdot T3^2 \cdot exp\left(-\frac{\Delta t}{T3}\right)}{(T1-T3)\cdot(T4-T3)} + \frac{(T2-T4)\cdot T4^2 \cdot exp\left(-\frac{\Delta t}{T4}\right)}{(T1-T4)\cdot(T3-T4)} \right]$ $V4_{New} = V4_{Initial} + V4_{Transient}$

Table 29.2 *Simplified Formulae for Discrete Lock Time Calculation*

Cycle Slipping

Cause of Cycle Slipping

The cause of cycle slipping is that the charge pump goes from a very high duty cycle to a very low duty cycle. The charge pump does not pump in the wrong direction in order to cause a cycle slip. What happens is that a large voltage is developed across the resistor ***R2*** in the loop filter when the charge pump current is flowing, and when it is removed, there is a corresponding drop in the VCO tuning voltage. Note that the capacitor ***C1*** and the other loop filter components may reduce this voltage drop. In the example below, a single cycle slip occurs around 17 µs. In this particular case, the cycle slip has only a small impact on the lock time. However, in the above example, there can be far more cycle slips that can greatly degrade the lock time.

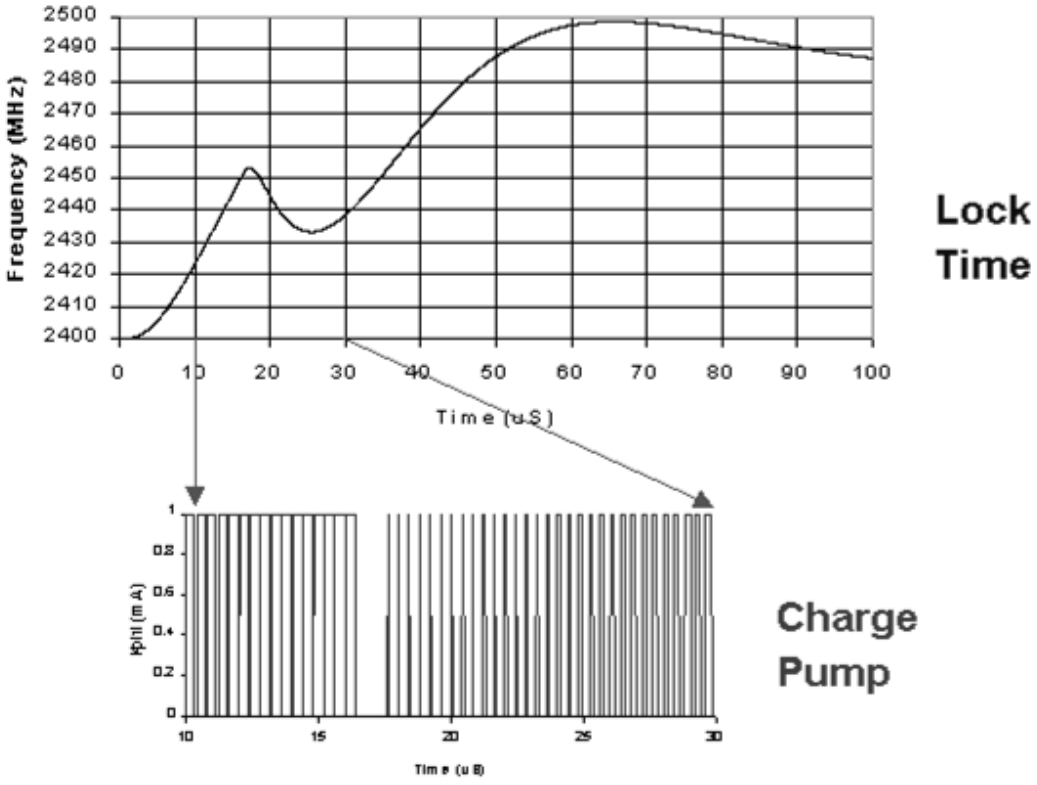


Figure 29.2 *Anatomy of a Cycle Slip*

Calculating when Cycle Slipping is an Issue

Assuming an infinite loop bandwidth and both dividers starting off in phase, the time to the first cycle slip is when the ***N*** divider gets one full cycle ahead of the R divider.

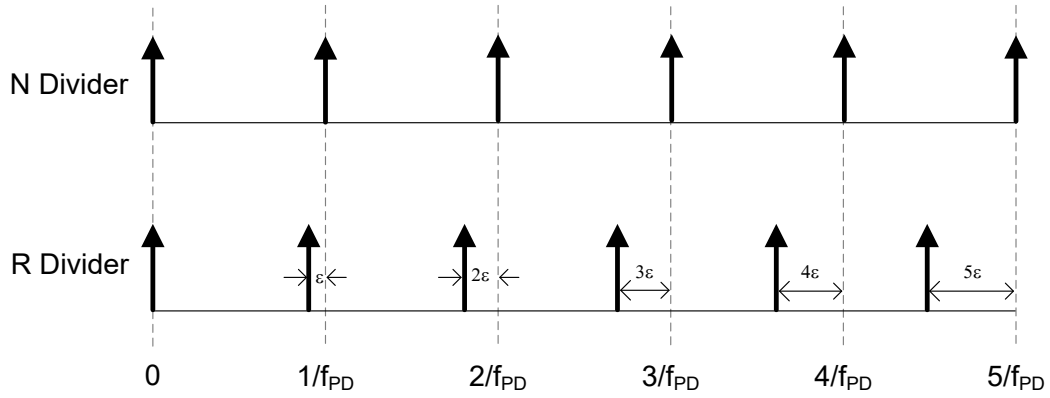


Figure 29.3 *Calculating the time to the First Cycle Slip for an Infinite Loop Bandwidth*

Assuming the N divider output is higher frequency than the R divider output, the time to the first cycle slip with a zero Hz loop bandwidth is:

$$t = \frac{1}{f_{PD}} \cdot \frac{\left(\frac{1}{f_{PD}}\right)}{\varepsilon} = \frac{1}{{f_{PD}}^2 \cdot \left|\frac{N}{f1} - \frac{N}{f2}\right|} = \frac{1}{f_{PD} \cdot \left|1 - \frac{f1}{f2}\right|} \qquad \textbf{(29.12)}$$

Now if the PLL is in lock, no cycle slipping occurs and ***t*** is infinite. However, if not, this time should be about the rise time or more in order to avoid cycle slipping. In actuality, the loop bandwidth is not infinite, and assuming that no cycle slipping occurs before the peak time is not realistic. A more reasonable assumption is to assume that the first cycle slip cannot occur before one-fourth of the peak time. Applying this rule and using the equations for peak time from the previous chapter give the following relationship.

$$\frac{f_{PD}}{BW} < \frac{5}{\left|1 - \frac{f2}{f1}\right|} \qquad \textbf{(29.13)}$$

For instance, if the frequency changes 5%, then the ratio of the phase detector frequency to the loop bandwidth should be no more than 100 if one wants to avoid the effects of cycle slipping. This factor of 100 will be used throughout this book for the sake of simplicity.

Impact of Cycle Slipping on Lock Time

A natural question to ask is what is the impact on lock time due to cycle slipping if condition (29.13) is violated? Intuitively speaking, Figure 29.3 suggests if the magnitude of the frequency change is doubled, then the cycle slipping would occur twice as often. Also, if the loop bandwidth was to be doubled, one would expect the cycle slipping to be about half. Combining these thoughts with (29.13) yields the *peak time multiplier*, which is a coarse estimate of how much the peak time will be multiplied due to cycle slipping.

$$Peak\ Time\ Multiplier = max\left\{\frac{2}{3}\times\frac{\left(\frac{f_{PD}}{BW}\right)\cdot\left|1-\frac{f2}{f1}\right|}{5}, 1\right\} \qquad \textbf{(29.14)}$$

The factor of 2/3 is empirical number from experience, not derivation, and comes in for two reasons. The first is that the overshoot typically is a lot less in cases where cycle slipping is occurring as this decreases the peak time. The second reason is that the severity of the cycle slipping decreases as the PLL gets closer to the target frequency. Figure 29.4 shows the lock time for a PLL system with a 5 kHz loop bandwidth and various phase detector frequencies. This is the same example filter used for the analog lock time. This was simulated for phase detector frequencies of 200 kHz, 2 MHz, 10 MHz, and 20 MHz as well as doing an analog simulation. The charge pump current was adjusted to keep the same loop bandwidth. The peak time multipliers are as follows:

f_{PD} (MHz)	Calculated Peak Time Multiplier	Simulated Peak Time (µs)	Simulated Lock Time (µs)
Analog	n/a	93	446
200	1	95	425
2000	1	93	430
10000	2.9	170	475
20000	5.9	530	825

Table 29.3 *Calculated Values for Figure 29.4*

When the phase detector frequency is less than 100 times the loop bandwidth (200 kHz in this case), the analog and discrete lock time model agree. However, when the phase detector frequency is much larger than 100 times the loop bandwidth, the rise time is greatly increased, which in turn increases the lock time. It is a reasonably accurate rule of thumb to assume that the amount that the lock time is increased due to cycle slipping is equal to the amount that the rise time is increased by cycle slipping.

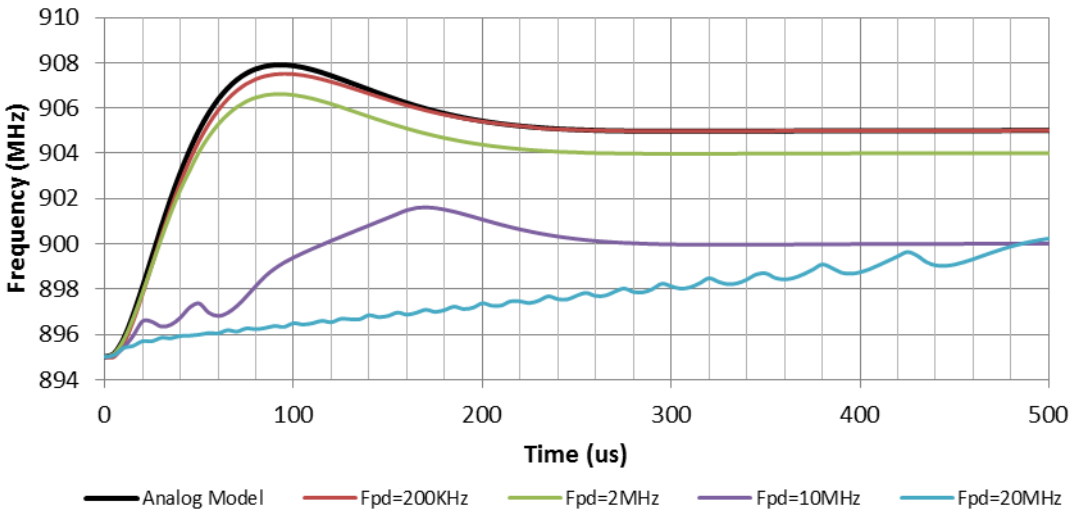


Figure 29.4 *Cycle Slip Example*

Conclusion

The analog model of lock time does a good job provided that the phase detector frequency does not exceed about 100 times the loop bandwidth and is not less than 10 times the loop bandwidth. There are many advantages of the analog method including computational elegance, speed, and accuracy. However, in situations where the phase detector frequency becomes either too small or too large relative to the loop bandwidth, discrete sampling effects become too significant to ignore. In situations where the loop bandwidth is less than about 1% of the phase detector frequency, cycle slipping starts to occur, which greatly increases the rise time and the lock time. When the loop bandwidth exceeds about 10% of the phase detector frequency, discrete sampling effects start to become more relevant and typically degrade lock time. These are just rough guidelines as the amount of the frequency change also matters, so for the most accurate modeling of lock time, it is best to account for the discrete sampling effects of the charge pump.

Chapter 30 VCO Digital Calibration Time for Integrated VCOs

Introduction

Integrated VCOs on silicon are becoming more commonplace in integrated circuits. These VCOs tend to be more complicated and often have multiple internal frequency bands and internally adjusted amplitude settings. Whenever the frequency is changed by more than a small amount, there is typically some sort of calibration process to find the optimal frequency band and amplitude setting. After the calibration is compete, the VCO frequency will be close and then the PLL will settle out the last part of the frequency error using traditional analog locking means. For some designs with narrower loop bandwidths, the VCO calibration can improve lock time because it gets the PLL close to the desired frequency when it is finished. This reduces cycle slipping and can reduce the overall lock time. In other designs with wider loop bandwidths, the VCO calibration can be slower than the traditional analog lock time and it increases the overall lock time. VCO calibration can be device specific in how it is done, but typically the key concerns are the time that the VCO calibration takes and the remaining frequency error when the calibration is finished. This chapter discusses VCO calibration time and presents models for it.

Aspects of VCO Calibration

The VCO calibration typically involves the elements of switching the capacitor bank, switching the inductor cores, and performing the amplitude calibration. The action of switching the VCO frequencies with the capacitor bank and inductor cores will be referred to as the *frequency calibration* and the action of calibrating the amplitude will be referred to as the *amplitude calibration.*

Frequency Calibration by Switching VCO Frequency Bands

The frequency calibration methods often tend to be *linear* or *divide and conquer*. For a linear VCO calibration, the general concept is that the VCO searches for the frequency band by incrementing or decrementing the VCO frequency in small steps. A divide and conquer approach is one that does successive guesses. The first guess is typically near the middle of the frequency range. If the frequency is too high then the next guess is typically the midpoint between this first guess and the lowest VCO frequency. If the guess is too low, then it is the midpoint between the first guess and the highest VCO frequency. This process continues until the correct frequency band is attained. The divide and conquer approach may be faster, but care has to be done to ensure that it reliably converges every time to the correct solution, especially if the initial frequency is near the boundary of two frequency bands. Figure 30.1 shows the divide and conquer approach converging to the correct frequency value. In this particular case, we see another disturbance after the calibration has found the correct frequency band. This is because after the first frequency calibration, the amplitude calibration is run, and then the frequency calibration needs to be re-run as the frequency values get impacted by the amplitude calibration.

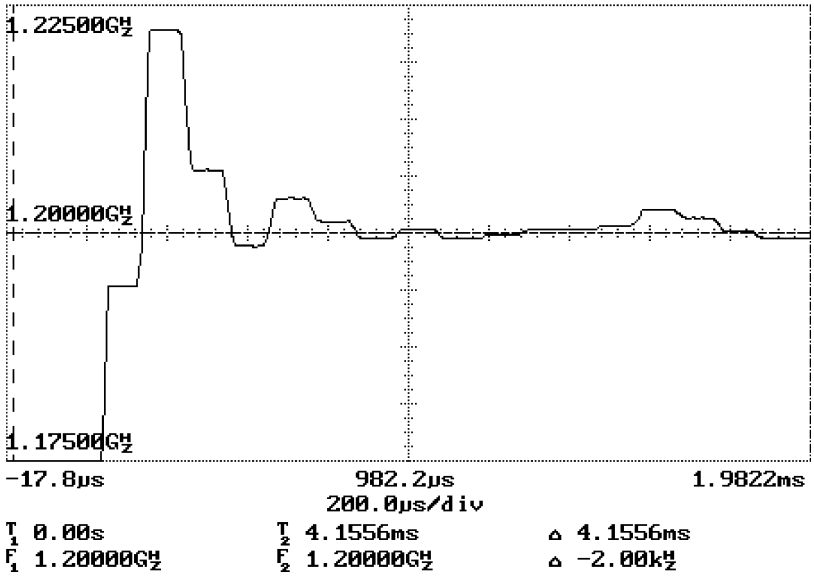


Figure 30.1 *LMX2531 Silicon VCO Using a Divide and Conquer Approach*

Frequency Calibration – Switching between VCO Cores

Multiple core VCOs are becoming more commonplace in the market and the switching between cores can impact the calibration time. The two things to keep in mind when cores are being switched is the frequency error it introduces as well as any additional delays it introduces at each core. The following figure shows the LMX2581 VCO calibration going through each of its four VCO cores. We can see that every time a core is changed, the overlap in frequencies between the cores causes a little disturbance in the frequency ramp.

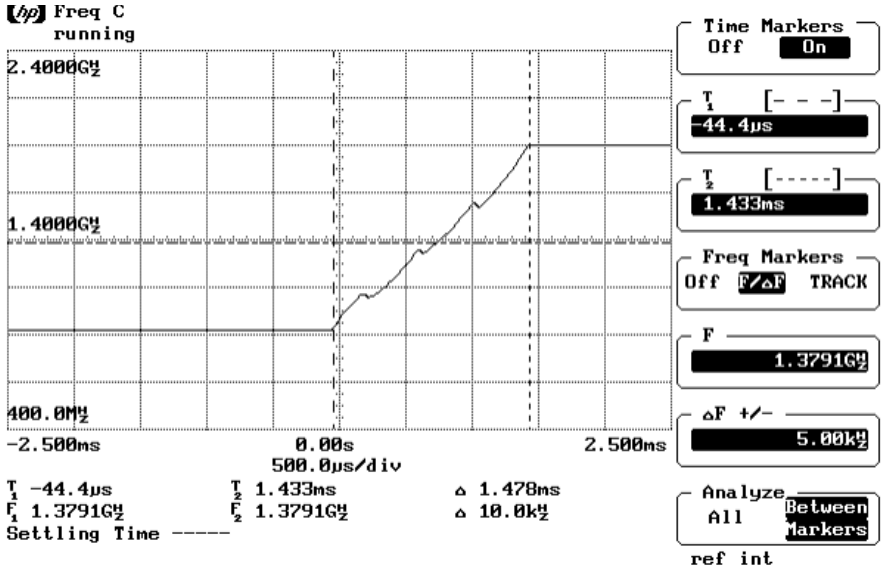


Figure 30.2 *LMX2581 VCO Switching Through All Four Cores*

Aside from just the frequency error switching between the cores, there can be a delay. The following figure shows the LMX2571 switching through VCO cores. We see that there is a long delay at each code to allow an amplitude calibration.

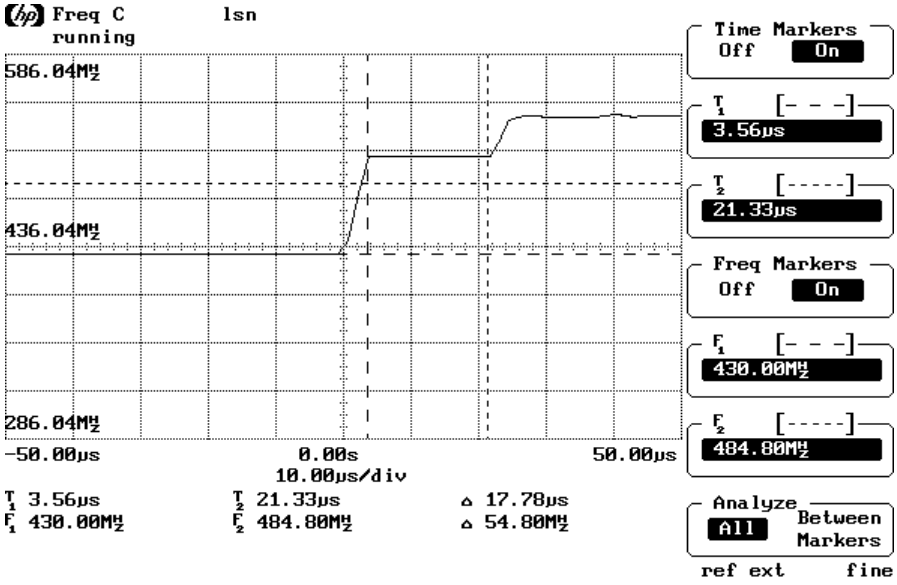


Figure 30.3 *LMX2571 Switching between VCO Cores*

Modeling the VCO Calibration

Understanding the VCO Calibration State Machine Clock and Calibration Error

Two aspects of VCO calibration that apply to just about every digital VCO are the state machine clock frequency and the calibration error. The state machine clock runs the VCO calibration routine. As this clock runs faster, the VCO calibration will run faster, but devices will limit this clock speed because if it runs too fast, it could lead to errors. The state machine is typically calculated by dividing the input frequency by some value, *CalDiv*.

$$f_{CalCLK} = \frac{f_{OSC}}{CalDiv} \tag{30.1}$$

The other universal aspect is the calibration error. After the VCO is settled, the frequency will not be exactly correct and there will be some error, *CalError*, which is typically settled out with the analog PLL. The values of CalDiv and CalError are device specific.

Device	CalDiv
LMX2531	$\begin{cases} 1 & f_{osc} \le 40\ MHz \\ 2 & f_{osc} > 40\ MHz \end{cases}$
LMX2581	$\begin{cases} if\ R = 1 \begin{cases} 1 & f_{osc} \le 64\ MHz \\ 2 & 64\ MHz < f_{osc} \le 128\ MHz \\ 4 & 128\ MHz < f_{osc} \le 256\ MHz \\ 8 & f_{osc} > 256\ MHz \end{cases} \\ if\ R > 1 \begin{cases} 5 & f_{osc} \le 64\ MHz \\ 5 & 64\ MHz < f_{osc} \le 128\ MHz \\ 5 & 128\ MHz < f_{osc} \le 256\ MHz \\ 10 & f_{osc} > 256\ MHz \end{cases} \end{cases}$
LMX2582 LMX2592	$\begin{cases} 1 & f_{osc} \le 200\ MHz \\ 2 & 200\ MHz < f_{osc} \le 400\ MHz \\ 4 & 400\ MHz < f_{osc} \le 800\ MHz \\ 8 & f_{osc} > 800\ MHz \end{cases}$

Table 30.1 *CalDiv Values for Various TI PLLs*

A Simplified VCO Calibration Model

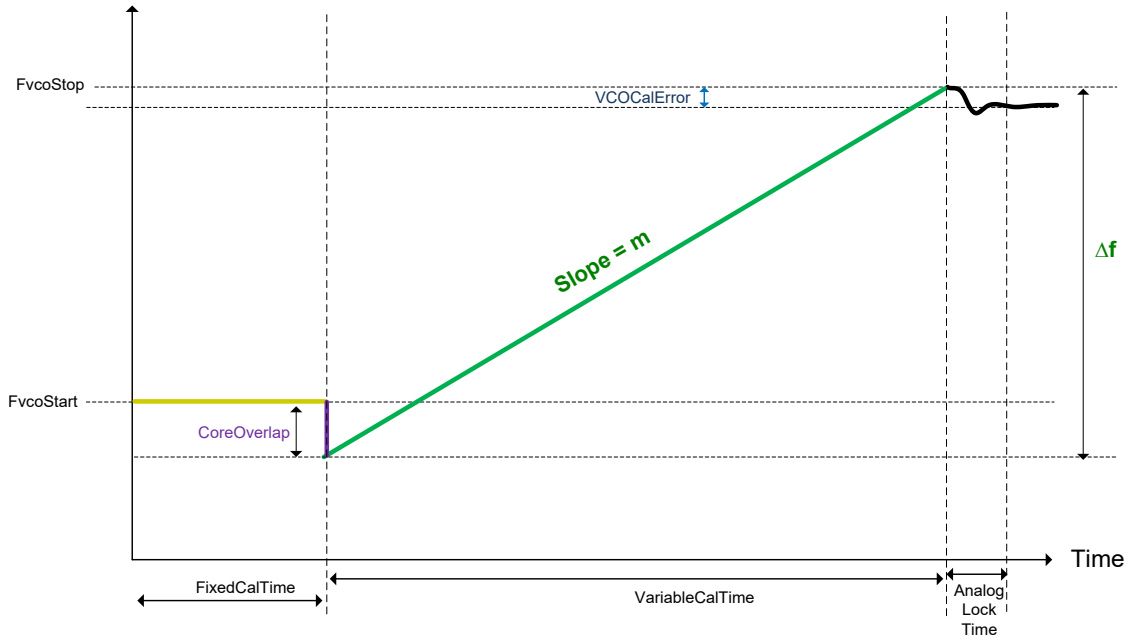


Figure 30.4 *Simplified VCO Calibration Model*

Figure 30.4 shows that the VCO calibration time can be thought of a fixed time and a variable time. The fixed time includes any amplitude calibration and time switching between the VCO cores. The variable time consists of the total amount of frequency the VCO needs to changed (***Δf***) multiplied by the slope (***m***). Δf includes the intended VCO frequency change as VCOCalError, which includes any additional frequency the VCO has to slew due to the differences in frequencies between the cores.

$$VCOCalTime = m \cdot \Delta f + FixedCalTime \tag{30.2}$$

These parameters can further be calculated based on various coefficients.

$$m = C + \frac{D}{CalClk} \tag{30.3}$$

$$FixedCalTime = t_{Fixed} + CoreChanges \cdot t_{Core} \tag{30.4}$$

$$t_{Fixed} = A + \frac{B}{CalClk} \tag{30.5}$$

$$t_{Core} = E + \frac{F}{CalClk} \tag{30.6}$$

Some of these constants for various synthesizers are in the following table.

Device	t_{Fixed}		m		t_{Core}		CalError
	A	B	C	D	E	F	
LMX2531LQ1778E	24	150	0.1	12.0	0	0	2.6
LMX2581	0	0	0	7.5	0	0	2.3
LMX2571	20	0	0.1	0	30	0	2

Table 30.2 *Calibration Constants*

A Full Calibration Model

The simplified calibration model gives a good idea, but assumes that all cores are the same. The truth is that the VCO calibration can be complicated with different coefficients for each VCO core and multiple other options.

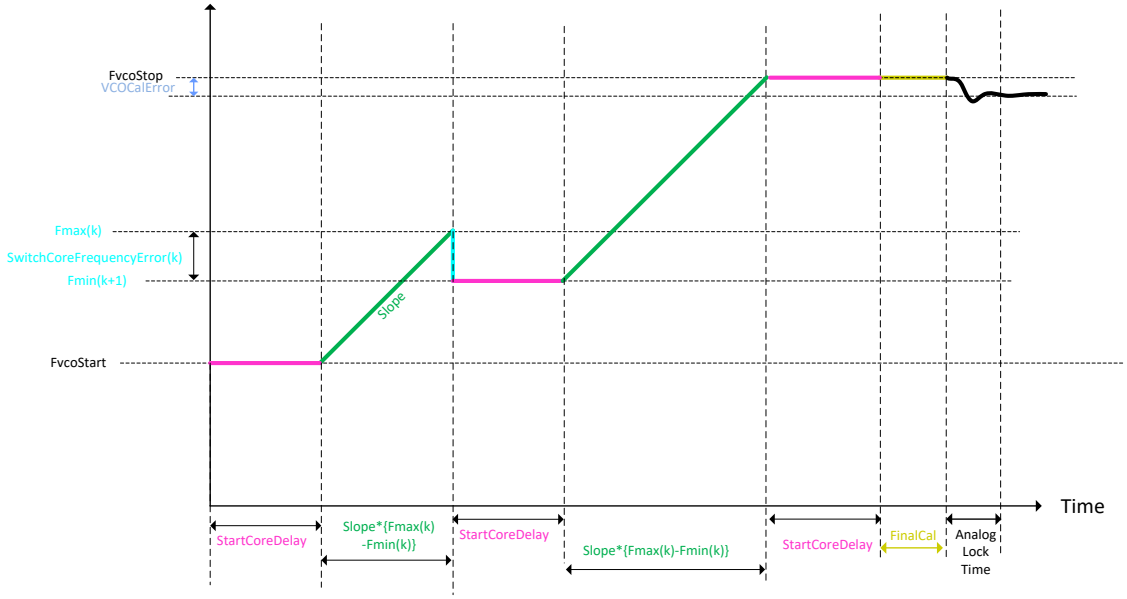


Figure 30.5 *Multiple Core VCO Calibration Model*

Category	Parameter	Symbol	Unit	Description
$f_{VCO}Start$	*Start Frequency*	$f_{VCO}Start$	MHz	The starting VCO frequency. It could be a fixed frequency, a frequency the user programs the VCO to start at, or a frequency the part chooses based in its current frequency
StartCoreDelay	*Formula & Description*	$A + \frac{B}{CalCLK}$	µs	The delay between each core when it switches. It can be zero for some, none, or all VCO cores. For some devices, this delay does not apply for the first core, especially if the VCO starts from a locked state.
	Constant	*A*	µs	
	Gradient	*B*	µs /MHz	
	ApplyFirstCore	*T/F*	*T/F*	
Slope	*Formula & Description*	$C + \frac{D}{CalCLK}$	µs /MHz	This is the frequency change over slope. This applies whenever the frequency is changing. Instant Core Slewing means that for some devices, if it is not the final core, the frequency calibration time for this core is instantaneous. Core overshoot means that on the final VCO core, the device will overshoot the final frequency.
	Constant	*C*	µs /MHz	
	Gradient	*D*	none	
	Instant Core Slewing		T/F	
	Core Overshoot		T/F	
SwitchCore FrequencyError	*Formula & Description*	*Fmax(k)-Fmin(k+1)*	MHz	When the core is switched, this is the error introduced. Fmax(k) is the highest frequency of the previous core and Fmin(k+1) is the lowest frequency of the lowest core. If the lock time goes the other direction, it is Fmax(k+1) and Fmin(k) Because there is overlap, this is nonzero. CoreOverlap is when there is a frequency error introduced in switching cores.
	CoreOverlap	*T/F*	T/F	
	Fmax(k)		MHz	
	Fmin(k+1)		MHz	
Final Calibration	*FinalCal*	$E + \frac{\Delta F}{CalCLK}$	µs	This is the time for any final frequency calibration. For the LMX2531, it is the amplitude calibration. For the LMX2582 the VCO typically overshoots and then settles back to the target frequency.
VCOCalError	*Calibration Error*	*VCOCalError*	MHz	This is the frequency error from the final frequency after the VCO frequency calibration has finished.

Table 30.3 *Multiple Core VCO Calibration Model Parameter Descriptions*

Lock Time Calibration Example with the LMX2581

As an illustrative example, consider the example involving the LMX2581, which is exactly the case for the measurement in Table 30.2. A VCO divider of two was used to make the measurement easier with test equipment.

Parameter	Value	Units
VCO Frequency Change	1880 to 3760	MHz
f_{PD}	20	MHz
f_{OSC}	100	MHz
VCO Divider	2	n/a

Table 30.4 *LMX2581 VCO Calibration Example*

Parameter	Core	Value	Units
VCO Frequency	VCO1	1880 to 2290	MHz
	VCO2	2168 to 2743	
	VCO3	2650 to 3248	
	VCO4	3126 to 3760	
A	All	1880 to 2290	µs
B	All	2168 to 2743	n/a
C	All	2650 to 3248	µs /MHz
D	VCO1	8.6	n/a
	VCO2	7.0	
	VCO3	7.6	
	VCO4	6.6	
E	All	0	MHz
F	All	0	MHz
VCOCalError	VCO1	1.8	MHz
	VCO2	2.3	
	VCO3	2.3	
	VCO4	2.8	

Table 30.5 *LMX2581 VCO Calibration Coefficients*

The first step is to calculate the calibration clock speed. Using Table 30.1, one can calculate this state machine clock as follows.

$$CalClk = \frac{f_{osc}}{CalDiv} = \frac{100\ MHz}{5} = 20\ MHz \quad \textbf{(30.7)}$$

The slope for all four cores can be found by dividing the calibration coefficient (D) by the CalCLK value. The slopes and additional overlap frequency from each core is as follows:

VCO Core	Slope	Overlap from Last Core
VCO1	8.6 / 20 MHz = 0.33 µs/MHz	n/a
VCO2	7.0 / 20 MHz = 0.35 µs/MHz	2168 MHz – 2290 MHz = - 122 MHz
VCO3	7.6 / 20 MHz = 0.38 µs/MHz	2650 MHz – 2743 MHz = - 97 MHz
VCO4	6.6 / 20 MHz = 0.33 µs/MHz	3126 – 3248 MHz = -122 MHz

Table 30.6 *LMX2581 Calculations NOT Accounting for Divide by Two*

These parameters can be combined to create the following simulation, as done with the PLLatinum Sim tool. The calculated calibration time was 1123 µs as compared the measured calibration time of 1478 µs that was measured in Figure 30.2.

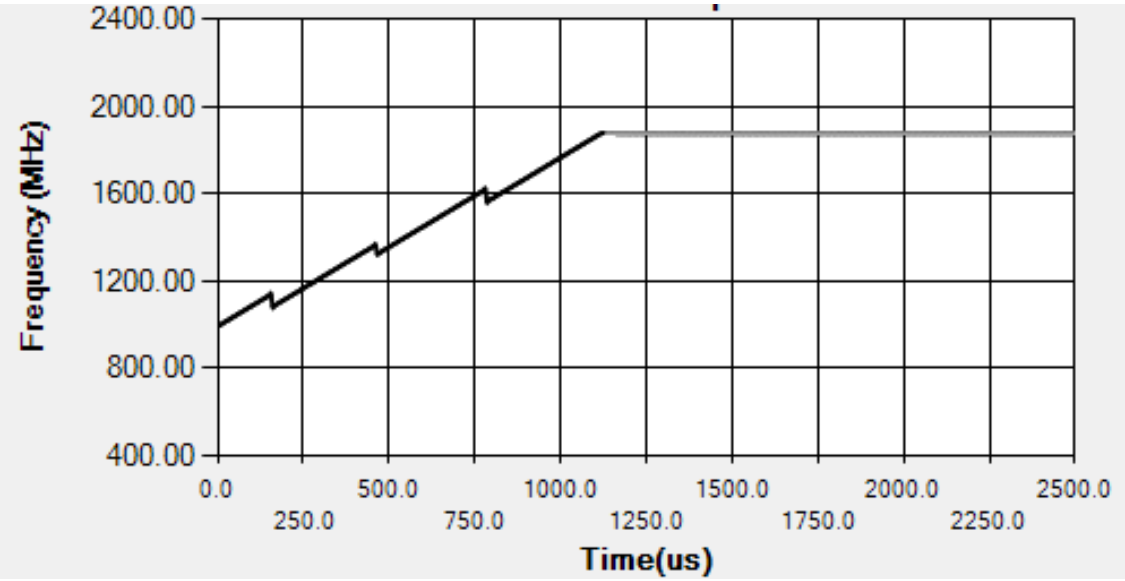


Figure 30.6 *LMX2581 VCO Calibration Simulation with PLLatinum Sim Tool Accounting for Divide by Two*

Conclusion

VCO calibration has many intricacies and many devices give the user options that can help assist and speed up the calibration. The modeling should not be taken as an exact science, but is still useful in getting a good idea of what sort of calibration time to expect.

Chapter 31 Impact of Capacitor Dielectric Absorption and Railing on the Transient Response

Introduction

Aside from the phase detector discrete sampling effects and VCO calibration time, there are other factors that can degrade the lock time. Two of these are dielectric absorption of capacitors and railing.

Dielectric Absorption of Capacitors

Non-ideal capacitors have a property known as dielectric absorption. To understand this property, consider a capacitor that is charged to a voltage, shorted, and the short is then removed. For an ideal capacitor, the voltage will remain at zero volts. A non-ideal capacitor with dielectric absorption will initially have to zero volts when shorted, but then a residual voltage will develop across the capacitor after the short is removed. A simple model for the capacitor with dielectric absorption can be modeled by putting a small capacitance ($C_{DA} << C$) and a large resistance (R_{DA}) as shown in the following figure.

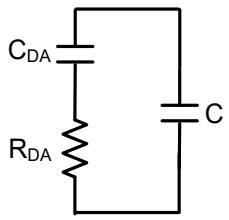


Figure 31.1 *Capacitor Modeling for Dielectric Absorption*

The capacitor with dielectric absorption, the impedance and admittance are as follows:

$$Z(s) = \frac{1 + s \cdot C_{DA} \cdot R_{DA}}{s \cdot C_{DA} + s \cdot C \cdot (1 + s \cdot C_{DA} \cdot R_{DA})} \quad \textbf{(31.1)}$$

+

$$\frac{1}{Z(s)} = \mathrm{s} \cdot \mathrm{C} + \frac{s \cdot C_{DA}}{1 + s \cdot C_{DA} \cdot R_{DA}} \quad \textbf{(31.2)}$$

This means that one can make the following substitution to model these effects.

$$\mathrm{s} \cdot \mathrm{C} + \frac{s \cdot C_{DA}}{1 + s \cdot C_{DA} \cdot R_{DA}} \quad \rightarrow \quad s \cdot C \quad \textbf{(31.3)}$$

The net effect of the dielectric absorption is that there is an extra zero and pole, which degrades the lock time and causes a long tail. As this model was approximate anyways, it is easier to illustrate with an actual example using the conditions in Table 31.1.

Parameter	Value	Unit
C1	6.8	nF
C2	47	nF
R2	1.5	kΩ
K_{PD}	4	mA
K_{VCO}	71	MHz/V
f_{VCO}	2100-2150	MHz
f_{PD}	0.2	MHz
Loop Bandwidth	5.7	kHz
Phase Margin	50.7	degrees

Table 31.1 *Example Loop Filter*

For this filter, the theoretical model using an ideal 47 nF capacitor for C2 is compared with measurements taken using C0G and X7R capacitors of this same value, but non-ideal dielectric absorption. Looking at a wider span, the effect is not very noticeable and the differences are likely due to differences in the actual value of the capacitor and imperfections in the theoretical model.

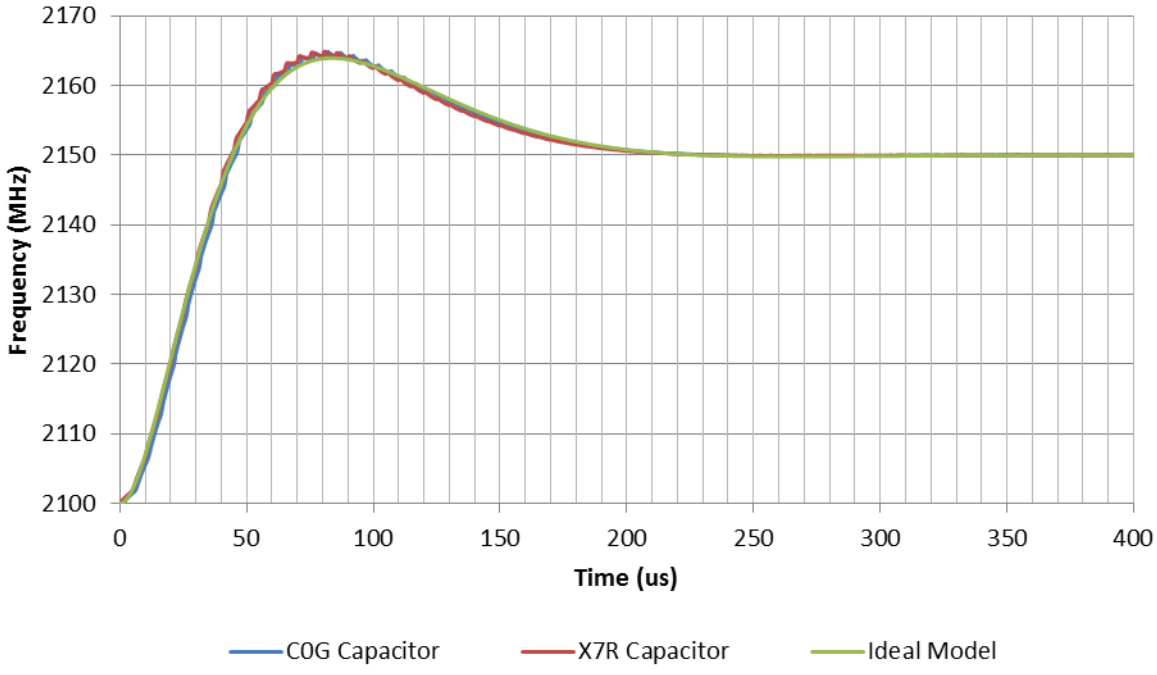


Figure 31.2 *Wide Span Lock Transient Response with Different 47 nF C2 Capacitors*

Although the impact of the capacitor dielectric maybe insignificant when looking at the wider span in Figure 31.2, the impact is much different when looking at a more narrow span as in Figure 31.3.

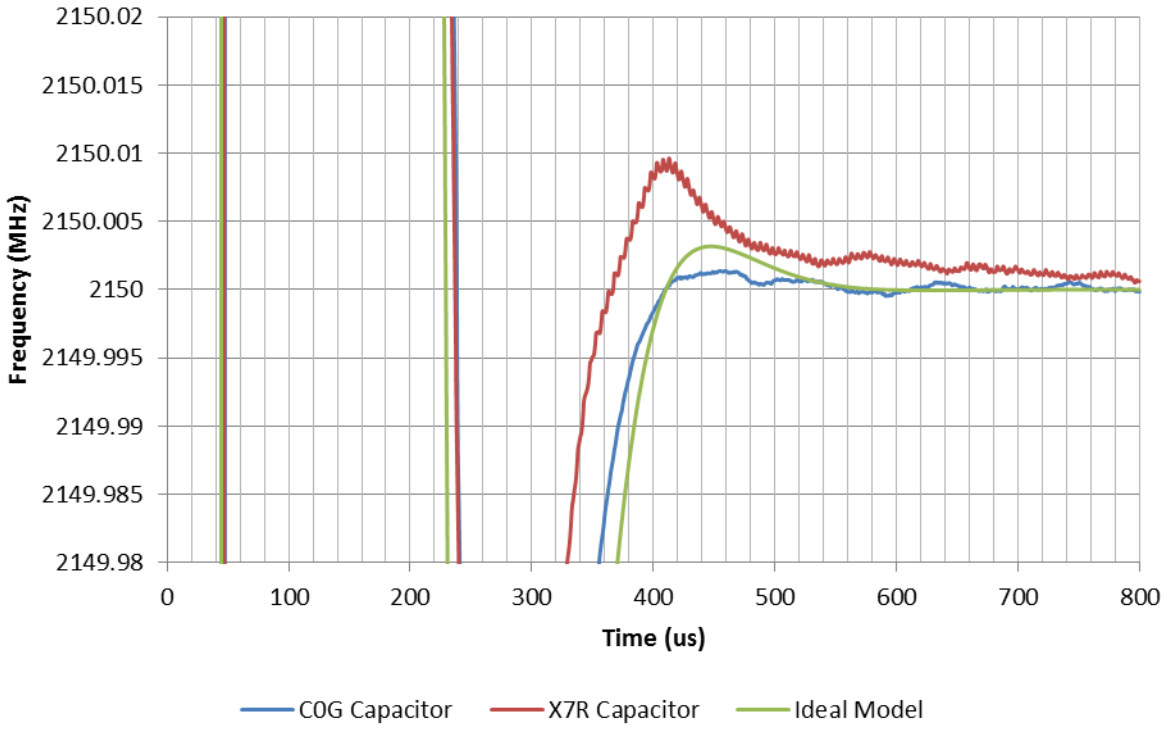


Figure 31.3 *Narrow Span Transient Response Using Different Capacitor Types*

When looking in closer in, the C0G capacitor matches the ideal model pretty well, but the capacitor with the X7R dielectric shows a long tail. As it is very common for lock time to be within 1 kHz or 500 Hz, this added tail can significantly degrade lock time much more this example.

As a general rule of thumb, capacitors that are C0G, NP0, or film tend to have low dielectric absorption and X7R and lesser rated capacitors tend to be worse. It is application specific as to what the impact of the capacitor dielectric will be, if at all. Practically, the best way to spot it when the lock time looks correct when from a wider span, but then shows a long tail when one zooms in to a lower frequency span.

Railing

Another factor that can degrade the lock time is when the VCO gets too close to the charge pump rails. In this case, the charge pump will not be able to drive as much current and the frequency will ride along the rail. This effect can be modeled in the discrete analysis by

relating these minimum and maximum charge pump voltages to a VCO frequency and then derating the charge pump current as follows:

$$K_{PD} *= K_{PD} \cdot \left(1 - exp(|f_{rail} - f|)/f_{knee})\right) \quad \textbf{(31.4)}$$

In this equation, K_{PD}* is the derated charge pump current, f_{rail} is the frequency corresponding to the rail being approached, f is the current frequency, and f_{knee} is the distance from this rail where the charge pump current is degraded to about 63% (1-1/e) of its value. Figure 32.4 shows an example with a 20 kHz loop bandwidth and 1 MHz and with a rail frequency of 1550 MHz and a knee of 50 MHz.

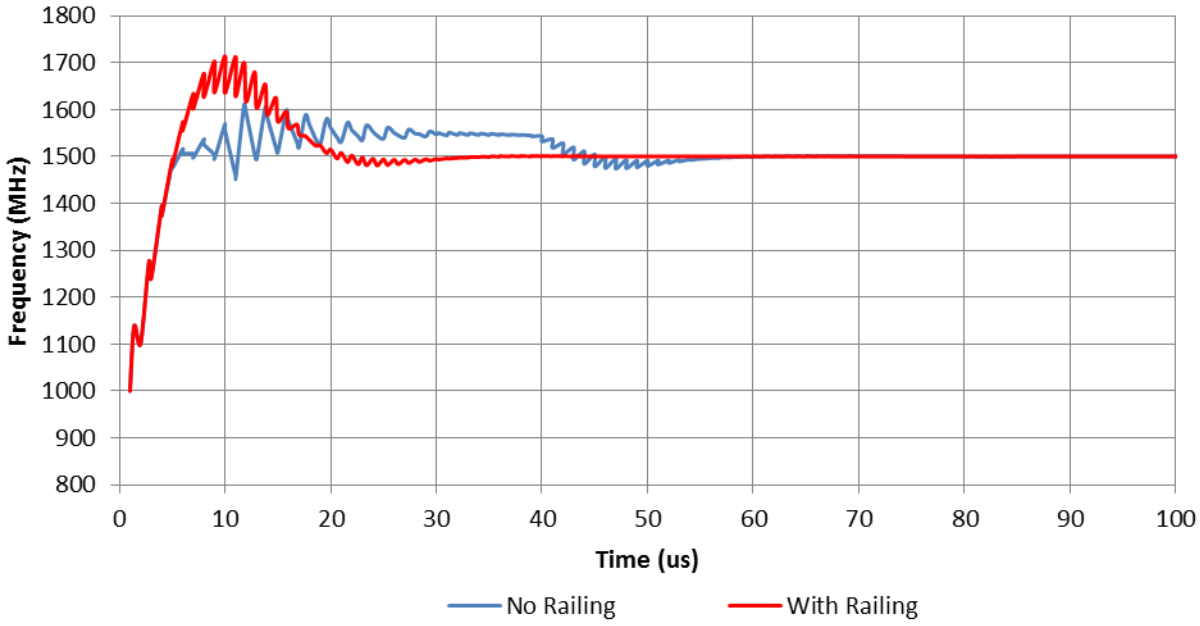


Figure 31.4 *Simulation for Impact of Railing on Lock Time*

Conclusion

There are many factors that can degrade lock time including changes in the VCO gain, cycle slipping, capacitor dielectric absorption, and railing. This chapter has focused on the latter two of these. Dielectric absorption has little effect on the rise time, but can have a substantial effect on the lock time. It is important to be aware of capacitor dielectric properties, especially when lock time is much worse than theoretically anticipated. Realize that there are others such as cycle slipping and VCO gain changes. When lock time is longer than theoretically predicted, it makes sense to ensure that capacitor dielectric absorption or railing are not the culprit.

Chapter 32 Using Fastlock and Cycle Slip Reduction

Introduction

In PLL design, a wider loop bandwidth is desirable for the fastest lock time, but this often is not optimal for the integrated noise, phase noise outside the loop bandwidth, or spurs. This leads to a classical trade-off in loop filter design. If one increases the loop bandwidth, then the lock time decreases at the expense of increasing the spur levels. If one decreases the loop bandwidth, the spurs decrease at the expense of increasing the lock time. The concept of Fastlock is to use a wide loop bandwidth when switching frequencies, and then switch a narrow loop bandwidth when not switching frequencies.

Fastlock Description

Fastlock is a feature of some PLLs that allows a wide loop bandwidth to be used for locking frequencies, and a narrower one to be used in the steady state. This can be used to reduce the spur levels, or phase noise outside the loop bandwidth. Fastlock is typically intended for a second order filter. It can be used in higher order loop filter designs, but the pole ratios (***T31***, ***T43***, and so on) need to be small. Otherwise, switching in the wide loop bandwidth will cause the filter to become very unoptimized and cause the lock time to increase. For this reason, this chapter focuses only on the use of Fastlock for a second order design.

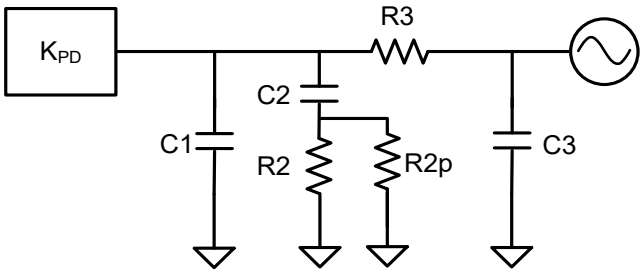


Figure 32.1 *Third Order Filter Using Fastlock*

When the PLL is in the locked state, charge pump gain K_{PD} is used and resistor ***R2p*** is not grounded, therefore having no impact. When the PLL switches frequency, the gain constant of the PLL is increased by a factor of M^2. This can be done by either increasing the charge pump current, phase detector frequency by a factor of M^2, or both such that the product of their increase is M^2. For notation purposes, K_{PD}* and f_{PD}* represent the charge pump gain and phase detector gain when the PLL is switching frequency. During the frequency switching of the PLL, resistor ***R2p*** is also switched in parallel with ***R2***, making the total resistance ***R2**** = ***R2*** || ***R2p*** = ***R2/M***. Recall that the forward loop gain for the second order filter is given by:

$$G(s) = \frac{K_{PD} \cdot K_{VCO}}{N \cdot s} \cdot \frac{1 + s \cdot T2}{s \cdot A0 \cdot (1 + s \cdot T1)} \quad \textbf{(32.1)}$$

$$T2 = R2 \cdot C2 \quad \textbf{(32.2)}$$

$$T1 = \frac{R2 \cdot C2 \cdot C1}{A0} \quad \textbf{(32.3)}$$

$$A0 = C1 + C2 \quad \textbf{(32.4)}$$

Parameter	**Normal Mode**	**Fastlock Mode**
M	$\sqrt{\frac{K_{PD}*}{K_{PD}} \cdot \frac{f_{PD}*}{f_{PD}}}$	
R2p	$\frac{R2}{M-1}$	
Equivalent Resistance, ***R2****	*R2*	$\frac{R2}{M}$
Charge Pump Gain	K_{PD}	K_{PD}*
Phase Detector Frequency	f_{PD}	f_{PD}*
Loop Gain Constant	*K*	*M·K*
Zero, ***T2***	*T2*	$\frac{T2}{M}$
Pole, ***T1***	*T1*	$\frac{T1}{M}$
Loop Bandwidth	*BW*	*M·BW*
Theoretical Lock Time	*LT*	$\frac{LT}{M}$

Table 32.1 *Filter Parameters in Normal and Fastlock Modes*

From the above table, one could conclude that if the charge pump was normally 1 mA, and then was switched to 4 mA, ***M*** would be two and there would be a theoretical 50% improvement in lock time. Another way of thinking about this is that the loop bandwidth could be decreased to half of its original value, thus making a theoretical 12 dB improvement in reference spurs. However, this disregards the fact that there is a glitch when Fastlock is disengaged, and this glitch can be very significant.

The Fastlock Disengagement Glitch

Cause and Behavior of the Glitch

When the Fastlock is disengaged, a frequency glitch is created. This glitch can be caused by parasitic capacitances in the switch that switches out the resistor ***R2p***, and also imperfections in charge pump. When the switch is disengaged, a small current is injected into the loop filter. It therefore follows that the size of the glitch is loop filter and PLL specific.

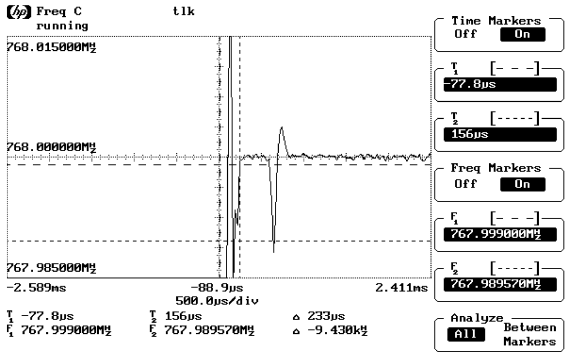
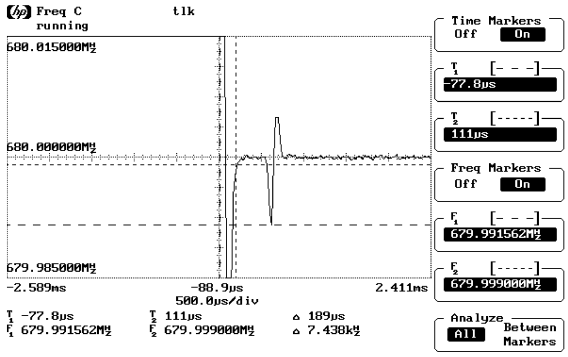
Switching from 680 – 768 MHz	Switching from 768 – 680 MHz
	
This shows a lock time of 233 us and a Fastlock glitch of 10.4 kHz	*This shows a lock time of 189 us and a Fastlock glitch of 8.4 kHz*

Figure 32.2 *Fastlock Disengagement Glitch*

One possible way to simulate the glitch is to model the unwanted charge injected into the loop filter as a delta function times a proportionality constant. From this, one can see why the glitch size is greater for an unoptimized filter and inversely proportional to charge pump gain, assuming an optimized loop filter of fixed loop bandwidth. Experimental results show that the ratio, ***M***, does not have much impact on this glitch, only the charge pump gain used in the steady state. For instance, if the charge pump gain was 800 uA in Fastlock mode and 100 µA in normal mode, then the glitch would be the same if the current was 1600 µA in Fastlock mode and 100 µA in normal mode.

The glitch also decreases as the loop bandwidth decreases. This can yield some unanticipated results. For instance, one would think that a loop filter with 2 kHz loop bandwidth using Fastlock would take twice the time to lock as one with a 4 kHz loop bandwidth using Fastlock. However, it could lock faster than this since the Fastlock glitch for the 2 kHz loop filter is less. In other words, the 4 kHz loop bandwidth filter would lock faster than the 2 kHz loop filter, but maybe not twice as fast. Increasing the capacitor ***C1*** or the pole ratios decrease the glitch, while increasing ***C2*** makes the glitch slightly larger.

Optimal Timing for Fastlock Disengagement

For optimal lock time, the Fastlock should be disengaged at a time such that the magnitude of this glitch is about the magnitude of the ringing of the PLL transient response. If Fastlock is disengaged too early, then the full benefits of the Fastlock are not realized. If it is disengaged too late, then the settle time for the glitch becomes too large of a proportion of the lock time. Figure 32.2 shows the lock time when the Fastlock glitch is taken into consideration.

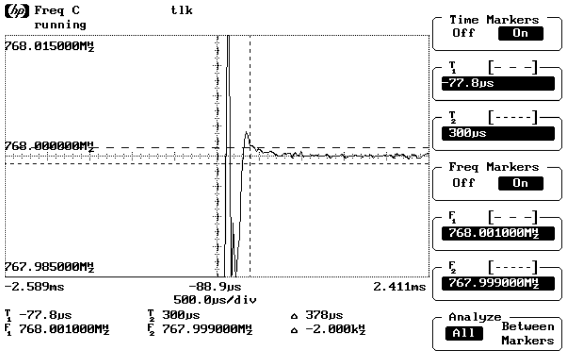
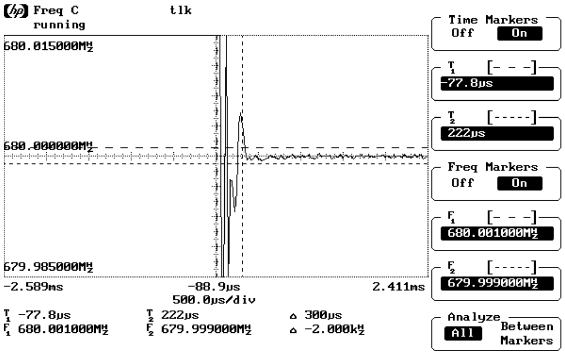
Switching from 680 – 768 MHz	Switching from 768 – 680 MHz
	
This shows a composite lock time of 378 us with a Fastlock timeout of 100 us	*This shows a composite lock time of 300 us with a Fastlock timeout of 100 us*

Figure 32.3 *Lock Time Using Optimal Fastlock Timeout of 100 us*

Disadvantages of Using Fastlock

Increased In-Band Phase Noise

Since Fastlock requires that a higher current is switched in during frequency acquisition, this requires that the PLL is run in less than the highest current mode. Recall from the phase noise chapter that the in-band phase noise is typically better for the higher charge pump gain.

Higher Order Loop Filters

Another disadvantage of using Fastlock is that if one builds a third or higher order filter with much considerable spur attenuation, then it is likely not to work well with Fastlock. Fastlock is most effective for second order loop filters, or higher order filters with small pole ratios.

Benefits of Using Fastlock

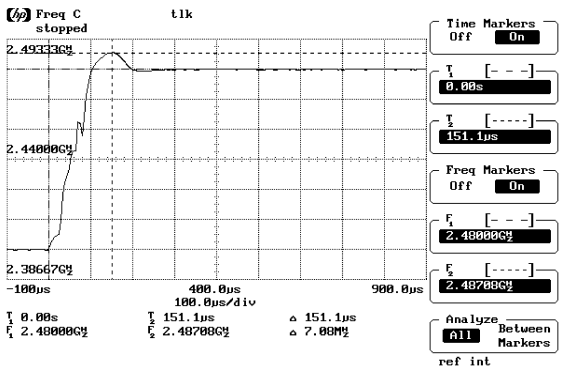
M	**Loop Bandwidth Increase**	**Theoretical Lock Time Reduction**	***R2p***
2:1	× *2*	50 %	$R2$
3:1	× *3*	67 %	$\frac{R2}{2}$
4:1	× *4*	75 %	$\frac{R2}{3}$
M:1	× *M*	$100 \cdot \left(1 - \frac{1}{\boldsymbol{M}}\right)$ %	$\frac{R2}{M-1}$

Table 32.2 *Theoretical Benefits of Using Fastlock*

The theoretical benefits of using Fastlock presented in the above table should be interpreted as theoretical best-case numbers for expected improvement, since they disregard the glitch caused when disengaging Fastlock. Typically, in the type of Fastlock when the charge pump current is increased from 1X to 4X (*M=2*), the actual benefit of using Fastlock is typically about 30%. In the type of Fastlock where the charge pump current is increased from 1X to 16X (***M=4***), the actual benefit of using Fastlock is typically closer to a 50% improvement. These typical numbers are based on Texas Instruments LMX2330 and LMX2350 PLL families. For more modern PLLs, the numbers might be a little different, but these numbers serve as a good rule of thumb.

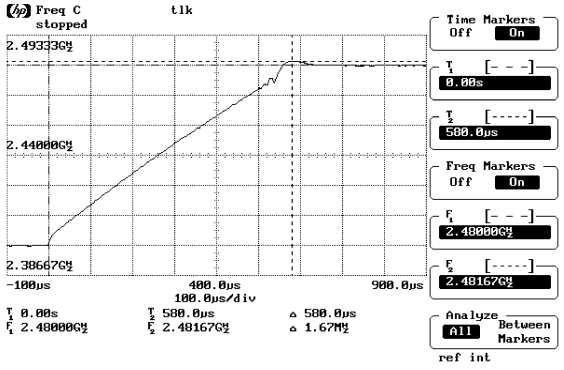
Cycle Slip Reduction

Cycle slipping starts to become a factor in lock time when the phase detector frequency exceeds about 100 times the loop bandwidth. One technique used by some parts from Texas Instruments involves increasing the charge pump current and decreasing the phase detector frequency by the same factor. In this case, all of the loop filter parameters remain the same, but cycle slipping is greatly reduced. This technique works very well in practice. Cycle slip reduction helps to improve the peak time. Normally, the peak time should be about 20% of the total lock time, but if cycle slipping is a problem, it can be the most dominant contributor to lock time. The next several figures show the impact of cycle slip reduction.



Peak Time with Cycle Slip Reduction

Positive peak time using cycle slip reduction is 151 us. Note the cycle slip. The frequency overshoot is 7.1 MHz. The cycle slip reduction factor was 16, which means the charge pump current is increased, and the phase detector frequency is decreased by a factor of 16 during frequency acquisition. For this case BW=10kHz, $\boldsymbol{f_{PD}}$ = 20MHz/16



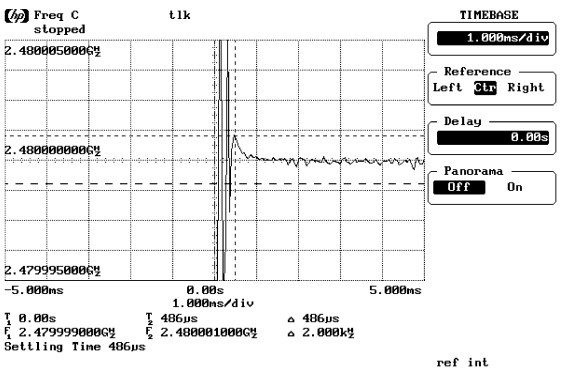
Peak Time without Cycle Slip Reduction

The peak time without using Fastlock is a whopping 561 us due to excessive cycle slipping. Note that the overshoot is only 1.8 MHz. This is due to distortion caused by the cycle slipping.

For this case,

BW=10kHz, $\boldsymbol{f_{PD}}$=20MHz.

Figure 32.4 *Impact of Cycle Slip Reduction on Peak Time*

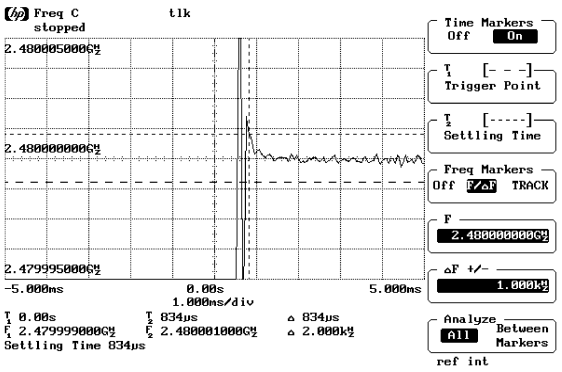


Lock Time with Cycle Slip Reduction

Positive lock time from 2400 to 2480 MHz with cycle slip reduction is to a 1 kHz tolerance is 486 us.

For this case,

$\boldsymbol{BW}$ = 10kHz, $\boldsymbol{f_{PD}}$ = 20MHz/16



Lock Time without Cycle Slip Reduction

Negative lock time from 2480 to 2400 MHz to a 1 kHz tolerance is 491 us. For this case,

$\boldsymbol{BW}$ = 10kHz, $\boldsymbol{f_{PD}}$ = 20MHz/16.

Figure 32.5 *Impact of Cycle Slip Reduction on Total Lock Time*

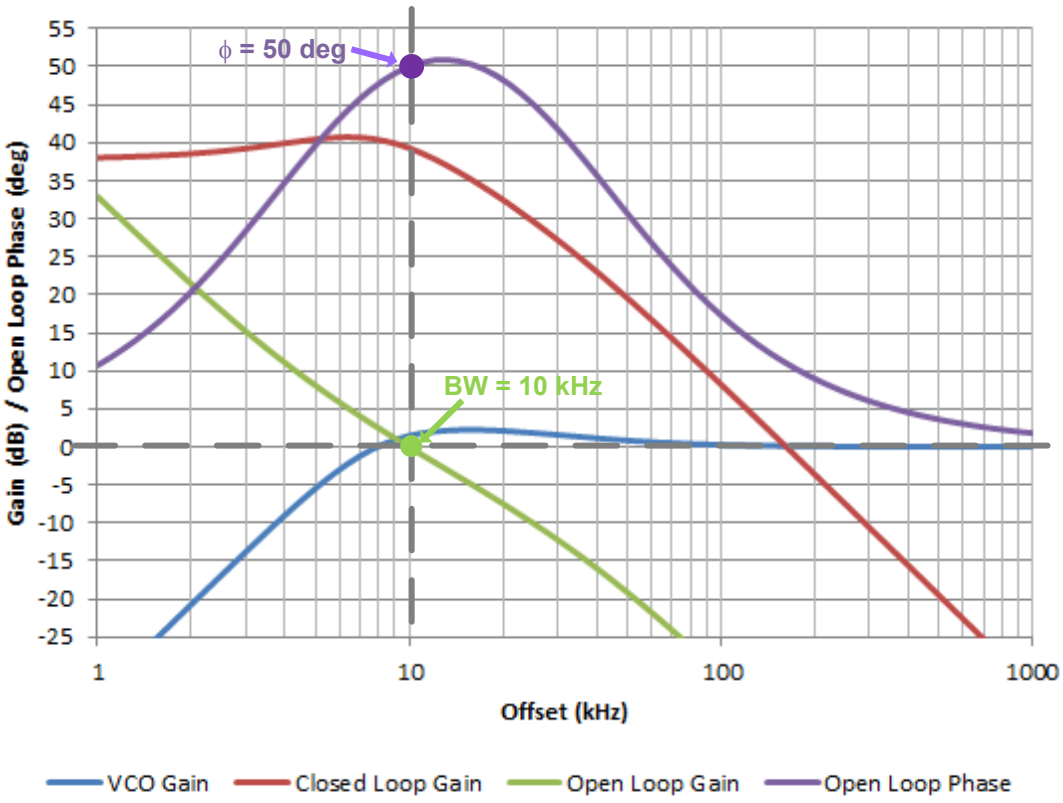
Conclusion

Fastlock is most beneficial in applications where the frequency offset of the most troublesome spur is less than ten times the loop bandwidth. In these situations, higher order filters have little real impact on the spur. As the spur offset frequency becomes farther from the carrier, higher order filters become more practical. An important issue with Fastlock is the glitch created by when it is disengaged. This is application specific, but it can take a significant portion of the lock time.

References

[1] Davis, Craig, et.al. *A Fast Locking Scheme for PLL Frequency Synthesizers*. Texas Instruments AN-1000

Loop Filter Design Fundamentals



Chapter 33 Concepts of Loop Filter Design

Introduction

A few concepts are necessary before the introduction of the equations for PLL loop filter design. These concepts include how to design for a tunable frequency range, the five design parameters (loop bandwidth, phase margin, gamma, T3/T1 ratio, and T4/T3 ratio), and determining the loop filter time constants from these five design parameters.

Designing for a Tunable Frequency Range

The loop filter is designed for a fixed value of N, K_{PD}, and K_{VCO}. However, it is often the case that a PLL tunes over a range of frequencies, which will definitely change the N divider value and possibly the VCO gain as well. The loop gain constant, K, is what impacts the dynamics of the loop filter.

$$K = \frac{K_{PD} \cdot K_{VCO}}{N} \tag{33.1}$$

Provided that the loop gain constant does not change significantly, it is not critical from a loop filter design perspective if the VCO gain, charge pump gain, or N counter value varies. In order to minimize how much the loop bandwidth can vary from the intended design value, design for the loop gain to be the geometric mean of its minimum and maximum values.

$$K_{design} = \sqrt{K_{min} \cdot K_{max}} \tag{33.2}$$

Since the loop gain is not directly specified, one of the parameters, like charge pump current can be adjusted for this. If the VCO gain and charge pump current are relatively constant, then choose the N counter value to be the geometric mean of the minimum and maximum values.

$$N_{design} = \sqrt{N_{min} \cdot N_{max}} \tag{33.3}$$

If the loop gain constant varies by more than about +/- 15% from the nominal value, it starts to make sense to try to compensate for this with the charge pump current, if it is programmable.

$$K_{PD} = K_{PD_{Design}} \cdot \left(\frac{N}{N_{Design}}\right) \cdot \left(\frac{K_{VCO_{Design}}}{K_{VCO}}\right) \tag{33.4}$$

To illustrate this concept, consider the case shown in Table 33.1 where the charge pump gain is adjusted to compensate for changes in then divider value and VCO gain.

Parameter	Unit	f_{min}	f_{design}	f_{max}
f_{VCO}	MHz	1500	1740	2000
K_{VCO}	MHz/V	20	28	40
N	n/a	75	87	100
K_{PD}	µA	2900	2400	1900
K	A·Hz/V	773.3	772.4	772.4

Table 33.1 *Parameters for a Tunable Design*

In this example, the design values were rounded and the charge pump gain has a limited 100 µA resolution and therefore the loop gain constants are not exactly the same, although they are very close.

The Five Loop Filter Design Parameters

The performance of a loop filter is theoretically determined by up to five design parameters of loop bandwidth, phase margin, gamma, T3/T1 Ratio, and T4/T3 ratio. These parameters uniquely determine the zero, poles, and time constant of the loop filter and the performance as well, with the exception of loop filter noise. For filters of higher than second order, it is possible to have additional degrees of freedom with component choice, but the filter parameters will be unique. The table below shows what parameters exist for each filter order.

Parameter	Symbol	Filter Order		
		2nd	3rd	4th
Loop Bandwidth	*BW*	√	√	√
Phase Margin	ϕ	√	√	√
Gamma	γ	√	√	√
T3/T1 Ratio	*T31*		√	√
T4/T3 Ratio	*T43*			√

Table 33.2 *Loop Filter Parameters*

These five parameters are discussed in depth in later chapters, but a brief introduction is given here.

Loop Bandwidth

The loop bandwidth (***BW***) is the most critical design parameter and has a profound impact on spurs, phase noise, and lock time. In fact, it is practically nonsense to talk about spurs or lock time without knowing the loop bandwidth. Wider loop bandwidths give better lock times, but spurs that are not crosstalk dominated will be increased. Inside the loop bandwidth, the PLL phase noise is passed, but the VCO phase noise is attenuated. At the offset frequency where the PLL and VCO phase noise cross is a good starting point for minimizing jitter, but it makes sense to adjust the loop bandwidth upwards or downwards depending on spur and lock time requirements. The maximum loop bandwidth is typically limited to one-tenth of the phase detector frequency. It can also be limited by the VCO input capacitance or by loop filter component values being forced.

Phase Margin

The phase margin (ϕ) is defined as 180 degrees minus the phase of the open loop gain at the loop bandwidth frequency. This has to be greater than zero and less than 180 degrees. Typically it is chosen between 30 and 80 degrees. Simulations suggest that 48 degrees is close to optimal for lock time, but higher phase margins up to 80 degree are preferable for a flatter response and also higher tolerance to variations in VCO gain. Lower phase margins may have more peaking in the response, but give sharper cut-off for better spur attenuation and are also useful in situation where loop bandwidth is limited by the VCO input capacitance or forced component values.

Gamma Optimization Factor

The gamma optimization factor (γ) relates to maximizing the phase margin at the loop bandwidth. This is typically chosen based on the phase margin, but there are some cases with partially integrated loop filters where it makes sense to choose something differently. This will be discussed in another chapter in more depth, but the equation is given below:

$$\gamma = \omega c^2 \cdot T2 \cdot (T1 + T3 + T4) = \frac{\omega c^2 \cdot T2 \cdot A1}{A0} \quad \textbf{(33.5)}$$

T3/T1 Pole Ratio

The T3/T1 pole ratio (***T31***) is a ratio of the pole T3 to T1. If this ratio is zero, the loop filter is less than third order. Choosing this equal to 100% theoretically yields optimal spur attenuation for a fixed loop bandwidth, but yields unrealizable components for a passive filter. It will be shown that if one chooses this as 68%, then this is almost the same spur attenuation as using 100% without leading to unrealizable component values.

$$T3 = T31 \cdot T1 \quad \textbf{(33.6)}$$

T4/T3 Pole Ratio

The T4/T3 pole ratio (***T43***) is a ratio of the pole T4 to T3. If this ratio is zero, the loop filter is less than fourth order. Choosing this equal to 100% yields optimal spur attenuation, but leads to unrealizable component values for a passive filter. For passive filters, it is typically chosen less such that T31+T43<100%.

$$T4 = T1 \cdot T31 \cdot T43 \tag{33.7}$$

Determining the Loop Filter Coefficients and Poles from the Design Parameters

Forward Loop Gain

The loop filter impedance is defined as the output voltage at the VCO divided by current injected at the PLL charge pump. The forward loop gain relates the design parameters to the loop filter coefficients and is shown below.

$$G(s) = \frac{K_{PD} \cdot K_{VCO}}{N \cdot s} \cdot \frac{1 + s \cdot T2}{A0 \cdot s \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)} \tag{33.8}$$

Determining the Time Constants

This method starts with expressing the phase margin in terms of the time constants. The phase margin is specified as 180 degrees plus the phase of the forward loop gain as specified in (33.8).

$$\begin{aligned} \phi = \quad & 180 + tan^{-1}(\omega c \cdot T2) \\ & - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T3) - tan^{-1}(\omega c \cdot T4) \end{aligned} \tag{33.9}$$

Since $\boldsymbol{\phi}$ and the pole ratios are known, this can be simplified to an expression involving ***T1*** and ***T2***. A second expression involving ***T1*** and ***T2*** can be found by setting the derivative of the phase margin equal to zero at the frequency equal to the loop bandwidth. This maximizes the phase margin at this frequency. Simulations show that satisfying this condition minimizes the lock time of the PLL for a second order filter. This method was taken from reference [1].

$$\left.\frac{d\phi}{d\omega}\right|_{\omega=\omega c} = 0 \tag{33.10}$$

$$= \frac{T2}{1 + (\omega c \cdot T2)^2} - \frac{T1}{1 + (\omega c \cdot T1)^2} - \frac{T3}{1 + (\omega c \cdot T3)^2} - \frac{T4}{1 + (\omega c \cdot T4)^2}$$

Equations (33.9) and (33.10) and the pole ratios can be used to create a system of two equations with the two unknowns, ***T1*** and ***T2***. The solution to these equations is presented in chapters to come. This system can always be solved numerically and in the case of a second order filter (***T31*** = ***T43*** = ***0***), an elegant closed form solution exists.

$$T2 = \frac{1}{\omega c^2 \cdot T1} \tag{33.11}$$

Simulations show that using equation (33.11) as a constraint gives a close approximation to the loop filter with the fastest lock time, but this is not exactly correct. Using some approximations, equation (33.11) can extend to all loop filter orders and expressed as follows.

$$T2 = \frac{1}{\omega c^2 \cdot (T1 + T3 + T4)} \tag{33.12}$$

Since this is an approximation to a rule of thumb that is only an approximation to the exact criteria for optimal performance, it makes sense to generalize this equation as:

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1 + T3 + T4)} \tag{33.13}$$

In the above equation, γ is defined as the Gamma Optimization Factor. Now 1.0 is a good starting value for this parameter, but this parameter is discussed in depth in other chapters.

Calculating the Loop Filter Coefficients from the Time Constants

This is the step that is expanded in much greater detail in other chapters. However, one common concept that arises, regardless of the filter order, is the total capacitance. This is the sum of all the capacitance values in the loop filter. If one considers a delta current spike, then it should be intuitive that in the long term, the voltages across all the capacitors should be the same and that its voltage would be the same as if all four capacitors values were added together. The final value theorem says this result can be found by taking the limit of ***s·Z(s)*** as ***s*** approaches zero. This result is ***A0***, the total loop filter capacitance. ***A0*** can be found by setting the forward loop gain (***G(s)*** divided by ***N***) equal to one at the loop bandwidth.

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{N \cdot \omega c^2} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2) \cdot (1 + \omega c^2 \cdot T4^2)}} \tag{33.14}$$

Once the ***A0*** coefficient is known, then the other coefficients can be found as follows:

$$A1 = A0 \cdot (T1 + T3 + T4) \quad \textbf{(33.15)}$$

$$A2 = A0 \cdot (T1 \cdot T3 + T1 \cdot T4 + T3 \cdot T4) \quad \textbf{(33.16)}$$

$$A3 = A0 \cdot T1 \cdot T3 \cdot T4 \quad \textbf{(33.17)}$$

The Pole Sum Constant

One intermediate constant that comes up in a lot of calculations is the *pole sum constant*, which is just the sum of the poles. It is used in later chapters to simplify calculations and has the following definition.

$$\kappa \equiv T1 + T3 + T4 \quad \textbf{(33.18)}$$

Conclusion

The design of the loop filter starts with understanding the key performance parameters of loop bandwidth, phase margin, gamma, and pole ratios. There are many trade-offs involved and there is on one choice for these that is always optimal in all situations. The next several chapters will go on and discuss these parameters in greater depth.

References

[1] Keese, William O. *An Analysis and Performance Evaluation of a Passive Filter Design Technique for Charge Pump Phase-Locked Loops* Application Note 1001. Texas Instruments

Chapter 34 Choosing the Loop Bandwidth

The loop bandwidth is the most critical of all the design parameters and can impact spurs, lock time, and jitter by orders of magnitude. The minimum loop bandwidth approaches zero Hz and is limited by the loop filter capacitors becoming unrealistically large. The maximum loop bandwidth can be limited by either the VCO input capacitance, forced loop components that one designs around, or discrete sampling effects of the phase detector. These discrete effects tend to become an issue around one-tenth of the phase detector frequency and result in instability around one-third of the phase detector frequency.

This leaves a very wide range of choices for the loop bandwidth and it has a very profound impact on lock time, phase noise, spurs, and jitter. There is no loop bandwidth that is optimal for all of these performance metrics, but there is one that is optimal for jitter, BW_{JIT}, which serves as a good starting point for discussing the trade-offs in choosing the loop bandwidth. BW_{JIT} can be found as the offset frequency where the VCO and PLL (and input reference) noise cross as shown in the following Figure 34.1.

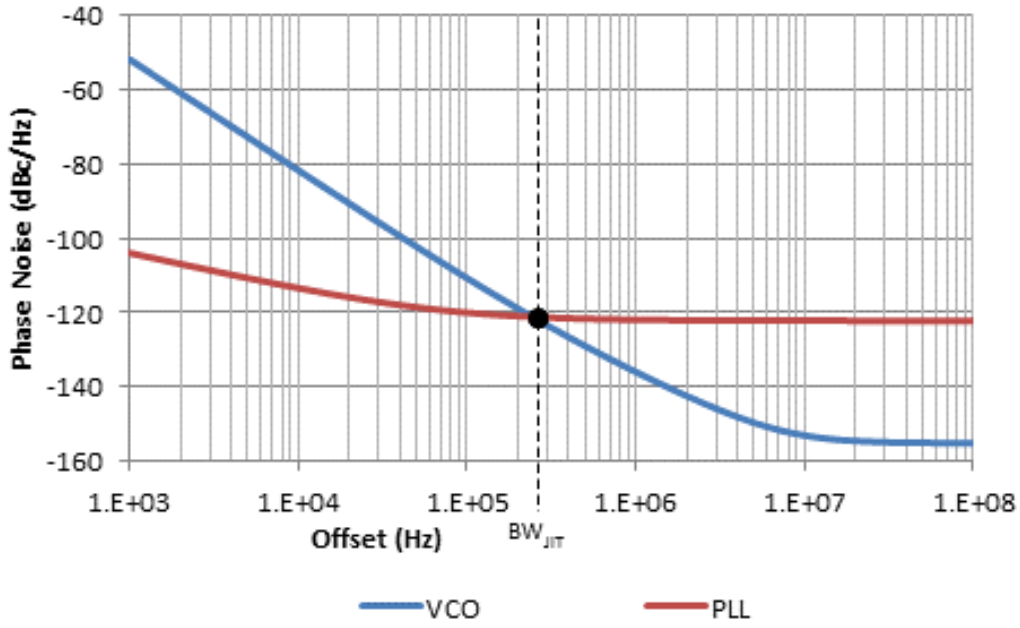


Figure 34.1 *Optimal Jitter Bandwidth*

In the above figure, the optimal bandwidth is where the PLL and VCO noise cross; about 242.5 kHz. If we assume that the loop filter is an ideal filter with a brick wall response and integration limits over the whole range, we can reason this by remembering that jitter is related to the area under the curve. If the loop bandwidth was narrower, then the VCO noise would dominate at some offsets below the BW_{JIT}, if the loop bandwidth was wider, then the PLL noise would be higher for some offsets above BW_{JIT}.

Performance Metric	Optimal Loop Bandwidth	Typical Limiting Factor(s)
Jitter	~ BW_{JIT} or 0 Hz	A bandwidth close to BW_{JIT} is optimal for jitter provided that this number is greater than the lower integration limit for the jitter. If this is not the case, then the optimal bandwidth is as narrow as possible.
Lock Time	$f_{PD}/10$	Increasing the loop bandwidth improves lock time with provided it is not limited by discrete sampling effects (which start to be a consideration when BW > $f_{PD}/10$) or VCO digital calibration (in the case of an integrated VCO). Also, the ability to increase the loop bandwidth may be limited by the VCO input capacitance, or if there are fixed components in the loop filter.
Spurs	0 Hz	Reducing the loop bandwidth generally improves spurs, but some spurs can also have causes that are not filtered by the loop filter (like crosstalk) which will limit much spurs can be improved by decreasing the loop bandwidth.
Phase Noise	0 Hz Or Infinite	If the phase noise is less than the optimal jitter bandwidth, then it will improve with wider bandwidths until it is just the noise due to the input reference and the PLL. If the phase noise offset is greater than the optimal jitter bandwidth, then it will improve for narrower loop bandwidths until it becomes just the free-running VCO noise.

Table 34.2 *Impact of Loop Bandwidth on Critical Parameters*

Table 34.2 gives a good summary about how to choose a loop bandwidth. If jitter is the only care about, then the optimal loop bandwidth is theoretically where VCO and PLL noise cross. In practice, the fact that the loop filter does not have an ideal brick wall response can cause this to be off by a good 25%. How much it is off and whether it is larger or smaller is dependent on the VCO noise profile and phase margin. Even if BW_{JIT} is not the optimal bandwidth, it is close and the definition still remains as the frequency where the PLL and VCO noise cross.

If lock time is the only concern, then make the loop bandwidth as wide as realistically possible, however at some point it will be limited by the fact that the loop filter capacitors get swamped out by the VCO input capacitance, or by the loop bandwidth getting larger than about $1/10^{th}$ of the phase detector frequency. Furthermore, for devices that have integrated VCOs, the VCO digital calibration time can start to dominate the lock time at some point.

For a spur that is outside the loop bandwidth, narrower bandwidths can improve the spur to a point. However, if the spur is due to a mechanism that crosstalks around the loop filter, then narrowing the bandwidth will do no good. For a spur that is inside the loop bandwidth, sometimes widening the loop bandwidth can help. Typically the worst bandwidth for a spur is when it is right near where the loop bandwidth peaks, which gives it the combination of PLL and VCO spur mechanisms working together.

For phase noise of offset less than the optimal jitter bandwidth, opening up the bandwidth will help because it filters out the effect of the VCO noise cropping in. It also improves the flatness of the closed loop response at this offset. If the phase noise is at an offset greater than the optimal jitter bandwidth, then narrowing the bandwidth typically is optimal as it filters out the PLL noise contribution.

The jitter, lock time, and phase noise was calculated for an LMX2581 PLL at 2700 MHz for a noiseless reference to better show the trade-offs involved in choosing the loop bandwidth. The lock time was from 2100 to 2700 MHz to a 1 kHz tolerance. For spurs, the 50 kHz offset spur was calculated for 2700.005 MHz and the 1 MHz offset spur was calculated for 2701 MHz. Note that although BW_{JIT} is 242.5 kHz, the optimal jitter is at a slightly different bandwidth, due to the fact that the loop filter does not have an ideal brick wall response.

Loop Bandwidth (kHz)	**Jitter** (fs)	**Phase Noise (dBc/Hz)**		**Analog Lock Time** (µs)	**Spurs (dBc)**	
		50 kHz Offset	1 MHz Offset		50 KHz Offset	1 MHz Offset
0.1	429.4	-102.2	-136.0	∞	-32.9	-58.9
1	-433.3	-102.2	-136.0	1834.2	-32.9	-58.9
2	444.6	-102.1	-136.0	923.0	-32.8	-58.9
5	500.3	-102.0	-136.0	377.4	-32.7	-58.9
10	551.7	-101.4	-136.0	195.3	-32.1	-58.9
20	456.9	-100.1	-136.0	104.2	-30.7	-58.9
50	232.7	-100.6	-135.9	49.6	-30.0	-58.8
100	133.7	-106.9	-135.7	31.4	-33.0	-58.2
200	91.6	-114.7	-134.2	22.3	-35.7	-54.2
242.5208	87.2	-116.1	-133.2	20.7	-36.1	-52.0
305	85.5	-117.2	-131.4	19.2	-36.4	-49.0
500	91.4	-118.2	-126.2	16.8	-36.8	-42.2
1000	115.7	-118.4	-120.2	15.0	-36.9	-35.5
2000	156.0	-118.5	-119.4	14.1	-37.0	-34.6
5000	238.5	-118.5	-121.1	13.5	-37.0	-36.2
10000	321.9	-118.5	-121.7	13.4	-37.0	-36.8

Table 34.3 *Specific Example for LMX2581 and Loop Bandwidth Trade-off*

Figure 34.2 shows this same data except the data has been normalized. The loop bandwidth has been divided by BW_{JIT} to create a normalized bandwidth, the phase noise and spurs have been normalized to what they were at BW_{JIT}, and the lock time and jitter have been expressed as a percentage increase to what they were for BW_{JIT}. For the phase noise and spurs at 50 kHz offset, we can see that they actually improve for wider bandwidths because they are at an offset less than the normalized bandwidth of one. For the phase noise and spurs at 1 MHz offset, they degrade for wider bandwidths because they are at an offset that is greater than a normalized bandwidth of one.

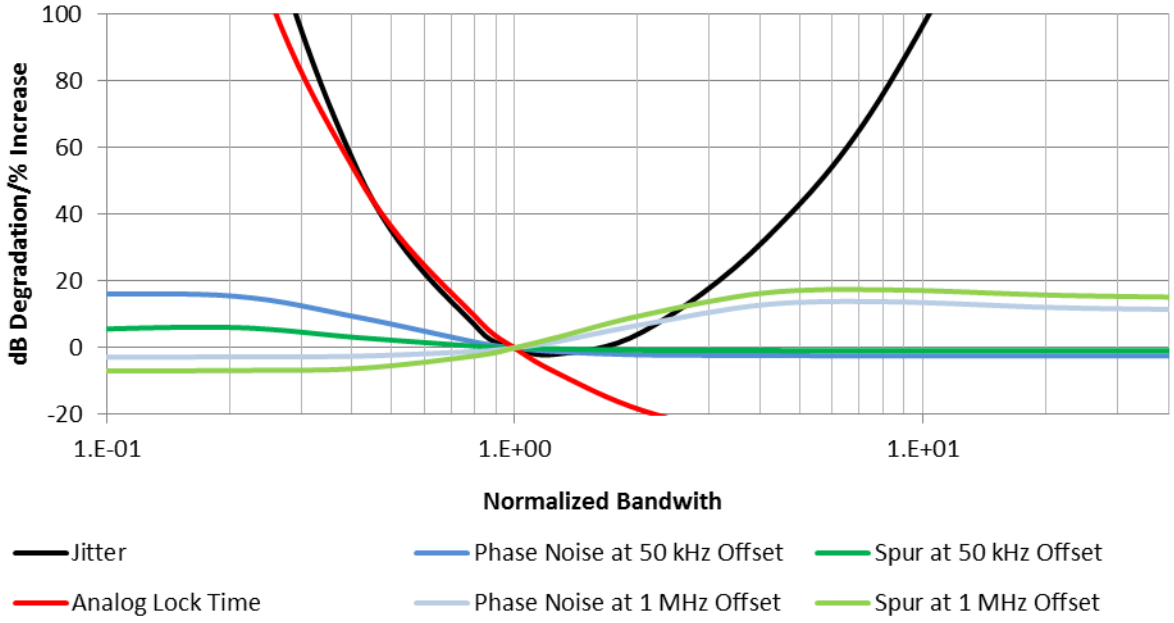


Figure 34.2 *Normalized Filter Performance Example*

Conclusion

In summary, the impact of the loop bandwidth cannot be ignored and it is therefore critical to choose this in an optimal way. This involves balancing jitter, spurs, phase noise, and lock time.

Chapter 35 Optimal Choices for Phase Margin

Introduction

The phase margin has an effect on lock time, integrated noise, and the peaking response of the loop filter. It is true that the phase margin does interact a little with the gamma optimization factor and pole ratios, to be discussed in later chapters, but a good intuitive feel of the phase margin can be achieved by simply studying the case of a second order loop filter with a gamma optimization parameter of one.

Impact of Phase Margin on Loop Response

Impact on Closed Loop Response

Phase margin has an impact on the closed loop response. Higher phase margins tend to give a flatter loop response with less peaking, which is desirable where minimization of integrated noise is a goal. However, by accepting a little peaking in the loop response, one can get more attenuation of spurs outside the loop bandwidth and more attenuation of the VCO noise inside the loop bandwidth. Figure 35.1 demonstrates this with a second order filter with a 10 kHz loop bandwidth and a gamma optimization factor of one.

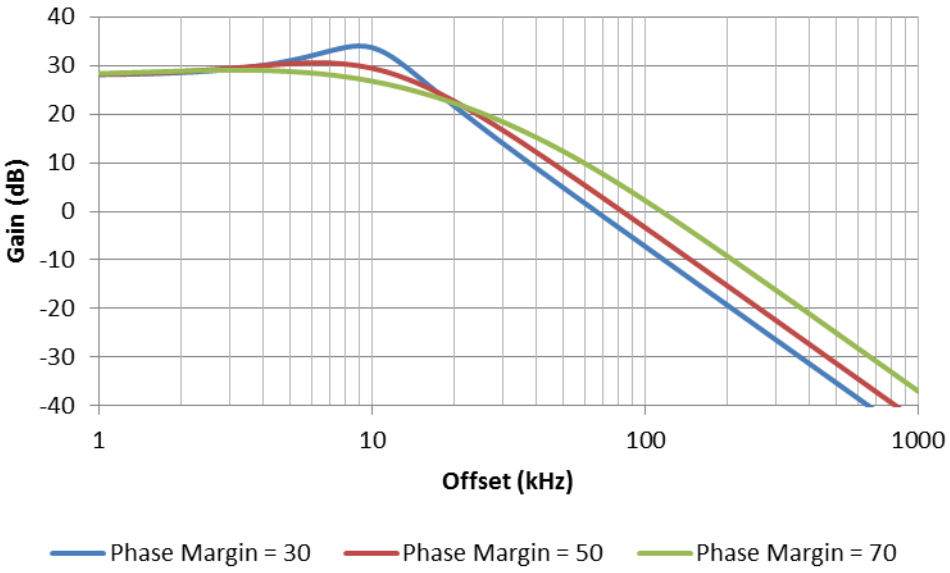


Figure 35.1 *Closed Loop Response vs. Phase Margin*

As the figure shows, the higher phase margin of 70 degrees gives a flatter response with the least peaking, which is good for minimizing integrated noise. However, it also has higher gain starting at offsets of 20 kHz. By the time the offset reaches 100 kHz, this difference stabilizes to about 10 dB. In a later chapter, it will be shown that higher order filters help

with more attenuation at offsets that are at least 10 times the loop bandwidth, but the impact at this offset is on the order of 1 dB; the offset would need to be much higher to see a 10 dB improvement. In summary, lower phase margin is good for attenuating spurs at lower offsets and higher order filters are more effect at much higher offset frequencies

Impact on VCO Noise Transfer Function

Peaking in the phase noise or close in phase noise is not always the result of a low phase margin. It is also possible for VCO phase noise to contribute significant phase noise at and below the loop bandwidth. As a rule of thumb, higher phase margins reduce the peaking in the VCO gain near the loop bandwidth at the expense of having less attenuation of the VCO noise at offsets lower than the loop bandwidth. Figure 35.2 shows the impact of phase margin on gain for a filter with loop bandwidth of 10 kHz and gamma of unity. For 30 degrees phase margin, the VCO noise attenuation is a full 10 dB better for offsets of 1 kHz and below.

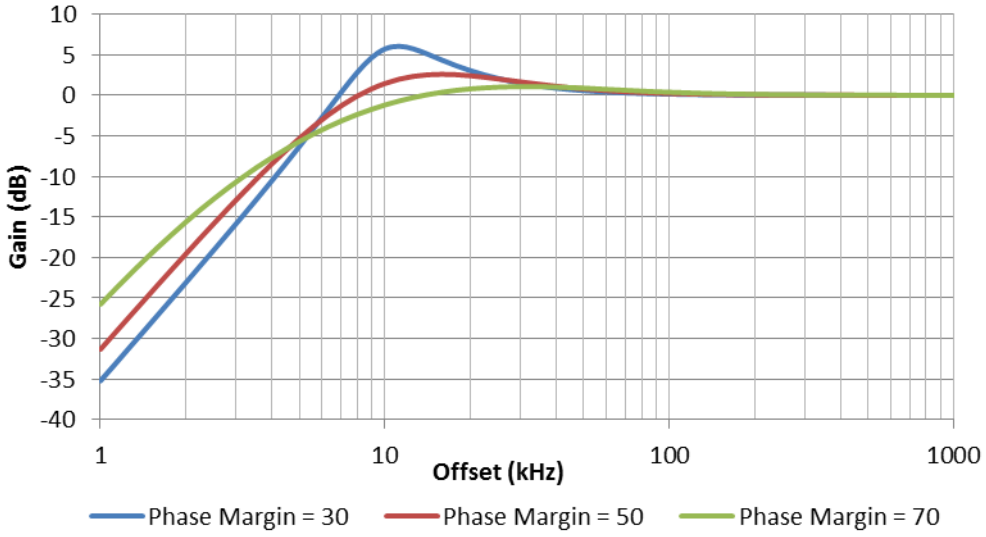


Figure 35.2 *VCO Transfer Function Gain vs. Phase Margin*

Impact on Variation of Filter Response

As a general rule of thumb, the charge pump and VCO gain can vary significantly over process, temperature, and tuning voltage; it is good to try to account for this. For instance, if the VCO gain was to be 40% higher than expected, the loop filter response would be different, but the design with the higher phase margin would change less than the one with the lower phase margin, especially with the peaking in the loop filter. When this peak frequency moves around with process, it can be partially mitigated by designing to a higher phase margin. This is illustrated in Figure 35.3 and Figure 35.4.

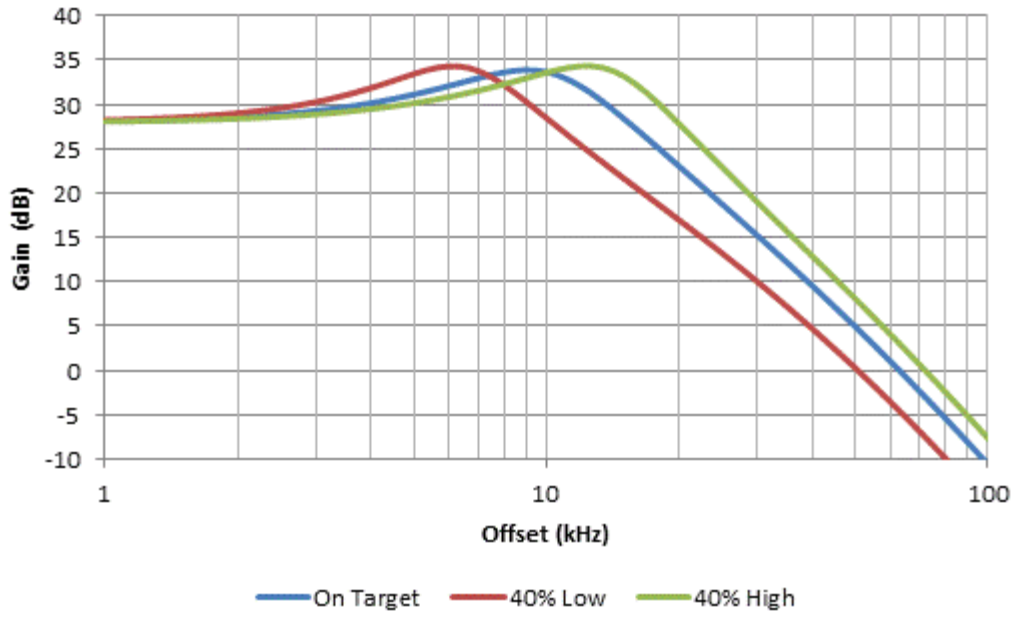


Figure 35.3 *Impact of +/- 40% VCO Gain Change with 30 degrees Phase Margin*

The filter with the higher phase margin filter has less peaking and better tolerance to variation in VCO gain.

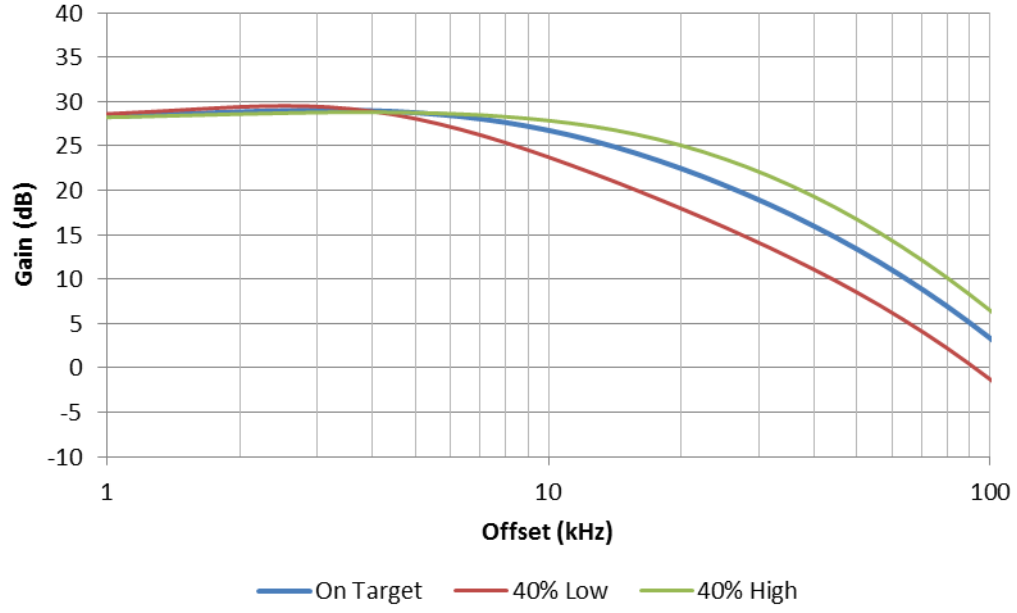


Figure 35.4 *Impact of +/- 40% VCO Gain Change with 70 Degrees Phase Margin*

Impact of Phase Margin on PLL Transient Response

Impact of Phase Margin on Overshoot and Ringing

Higher phase margins translate to less overshoot and ringing in the transient response. The following figure shows the impact of phase margin for a second order loop filter with gamma of one and a 10 kHz loop bandwidth.

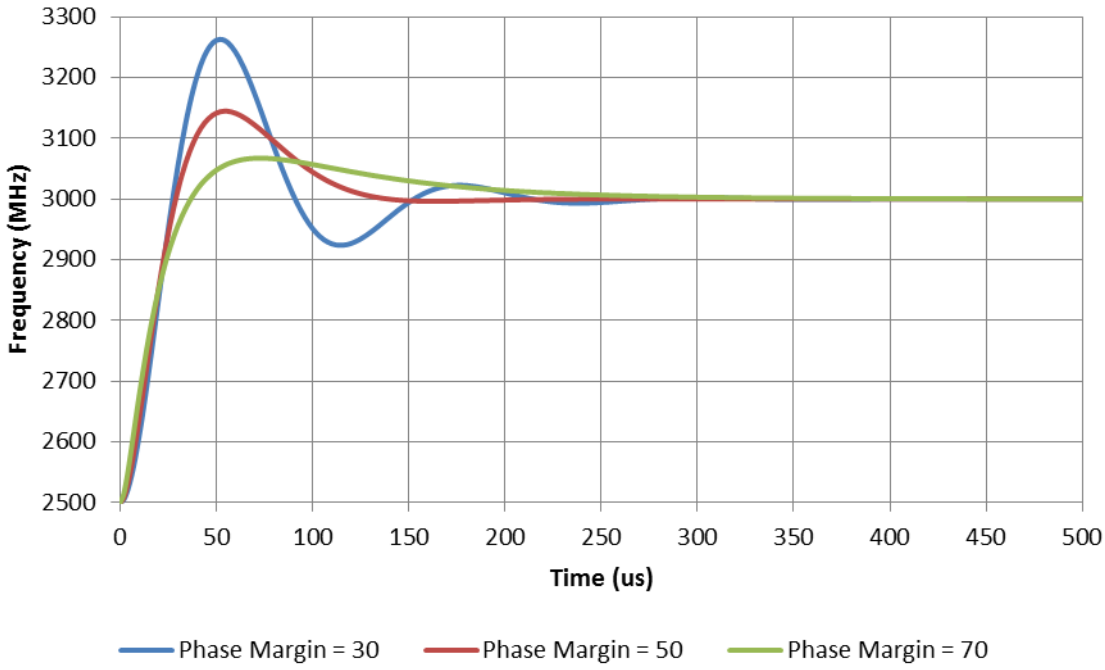


Figure 35.5 *Impact of Phase Margin on Overshoot and Ringing*

Although ringing and overshoot are generally not desirable by themselves, it is typically the lock time that is the more critical specification to worry about. The gamma optimization factor also seems to have a fair amount of impact on the overshoot with a higher factor leading to less overshoot, but this factor has a much smaller impact on the ringing.

Impact of Phase Margin on Lock Time

The lock time is typically more of a concern than the overshoot and the ringing and is also impacted by the gamma optimization factor. For a factor of one, a phase margin near about 48 degrees often gives the optimal lock time result.

Impact of Phase Margin on Stability

Impact on Gain Margin

In regards to stability as defined as all the closed loop poles having negative real parts, recall that it has been shown that the second order loop filter is always stable. However, for higher order filters, a low phase margin less than 20 degrees often results in instability, although this is dependent on other factors, such as gamma and the pole ratios. As the VCO and charge pump gain can vary, one does need to have sufficient gain margin for this as well. As a rule of thumb, higher phase margins translate to higher gain margins.

Impact on Phase Margin for Restricted Loop Bandwidth Filters

In some situations, there could be some component values that are forced in the loop filter that can restrict the loop bandwidth. This could be the case if the VCO input capacitance is an issue or there is a partially integrated loop filter. In either case, a lower phase margin typically allows one to design a wider loop bandwidth.

Conclusion

The choice of phase margin involves a trade-off between integrated noise, lock time, and spurs. For a stable loop filter with real positive components, it is necessary to design with a phase margin greater than zero degrees and less than 90 degrees. If integrated phase noise is the only concern, then typically higher phase margins approaching 90 degrees are good, although 80 degrees is typically as high as one would want to go. Above this, component values in the filter start becoming too small or negative. If spurs outside of the loop bandwidth were the only concern, then designing for a very low phase margin would yield sharper cut-off and better spurious attenuation. However, it would yield horrible peaking near the loop bandwidth and could even lead to instability if the phase margin was too low. If lock time was the only consideration, simulations suggest that 48 degrees is typically close to what is optimal for the fastest lock time, although the gamma optimization factor and pole ratios can influence this number to a small degree.

Chapter 36 Optimal Choices for Gamma Optimization Parameter

Introduction

There are some that may be lead to a false sense of confidence that the loop filter is determined only by loop bandwidth and phase margin. The reality is that it is possible to design two second order loop filters with exactly the same phase margin and loop bandwidth, but with dramatically different lock times and spurs. As a second order filter has three components, three constraints are needed to specify the components. Loop bandwidth and phase margin are two of them and the third is the gamma optimization parameter (γ). Assuming a gamma value of one is a good starting point, but there is further room for optimization. The optimal choice for gamma is dependent on the phase margin. This chapter investigates this optimal choice for gamma based on the phase margin.

Definition of the Gamma Optimization Parameter

If one imposes the design constraint that the phase margin is maximized at the loop bandwidth, then this is equivalent to designing for a gamma value of one. Imposing this restriction yields the following equation:

$$\frac{T2}{1+\omega c^2 \cdot T2^2} = \frac{T1}{1+\omega c^2 \cdot T1^2} + \frac{T3}{1+\omega c^2 \cdot T3^2} + \frac{T4}{1+\omega c^2 \cdot T4^2} \qquad \textbf{(36.1)}$$

This can be approximated as:

$$T2 = \frac{1}{\omega c^2 \cdot (T1+T3+T4)} \qquad \textbf{(36.2)}$$

Choosing the phase margin to be optimized at the loop bandwidth is a good approximation to minimizing the lock time, but not the exact constraint; it makes sense to generalize it. By introducing the variable, γ, but still keeping the equation in a similar form, one has a good idea of what values to try for this new variable. The new constraint can be stated as follows:

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1+T3+T4)} = \frac{\gamma}{\omega c^2 \cdot \kappa} \qquad \textbf{(36.3)}$$

Interpretation of the Gamma Optimization Factor

Although the gamma optimization factor has a straightforward algebraic definition, the reader is likely to try to relate this to some other explanation for this parameter in terms of other terms, such as poles and zeros. For the purposes of this discussion, it is easier to convert the zero of T2 to a frequency by taking the reciprocal and dividing by 2π. Then do the same for the pole sum ratio, κ.

The phase margin is largely determined by the ratio of ***T2*** to κ. The loop bandwidth will always be greater than the frequency corresponding to T2 and less than the frequency corresponding to κ. If gamma is one, then this means that the loop bandwidth is the geometric mean between these two frequencies. If gamma is increased beyond one, the pole comes closer to the loop bandwidth and the zero moves farther away. As gamma goes below one, the pole ratio moves farther away and the zero comes closer to the loop bandwidth.

Gamma	T2	κ	BW/T2	κ/BW	T2/κ
0.10	0.72	13.83	13.83	1.38	0.05
0.20	0.64	7.78	15.58	0.78	0.08
0.50	0.49	4.07	20.34	0.41	0.12
1.00	0.36	2.75	27.47	0.27	0.13
2.00	0.25	2.03	40.67	0.20	0.12
5.00	0.13	1.56	77.92	0.16	0.08
10.00	0.07	1.38	138.32	0.14	0.05
∞	0.00	11.92	∞	1.00	0

Table 36.1 *Gamma Optimization Factor Example for BW=1 kHz, PM=50 degrees*

Eliminating and Normalizing Out Other Design Parameters

Recall that it was proven in the lock time chapter that the lock time was inversely proportional to the loop bandwidth, given all other factors constant. What this means is that whatever choice of phase margin and gamma are optimal for one loop bandwidth, is also optimal for another loop bandwidth. The VCO gain, ***N*** value, and charge pump gain change the filter components, but have no impact on lock time, provided the loop filter is redesigned. So the only thing left to study is the pole ratios, phase margin, and gamma optimization factor. Now it will turn out that the pole ratios will have a small impact on the gamma parameter choice, and the phase margin will have the largest impact.

Results of Computer Simulations

It also turns out that the size of the frequency jump an impact on the lock time, but this effect is minimal. So the approach is to assume fixed conditions for the frequency jump and tolerance, and then compile tables for the optimal gamma value based on computer simulations that cover all cases. Following are the simulation parameters.

Parameter	Value	Units
K_{PD}	5	*mA*
K_{VCO}	20	*MHz/Volt*
BW	10	*kHz*
f_{PD}	200	*kHz*
ϕ	Variable	*Degrees*
Frequency Jump	800 – 900	*MHz*
Frequency Tolerance for Lock Time	1	*kHz*
N	4500	*n/a*

Table 36.2 *Conditions for Simulations*

Phase Margin	Gamma for Fastest Lock Time
30	1.40
35	1.41
40	1.29
45	1.09
50	0.94
55	0.85
60	0.70
65	0.49
70	0.24
75	0.05
80	0.08

Table 36.3 *Optimal Values for Gamma*

First Simulation: Impact of Gamma Value and Phase Margin on Lock Time

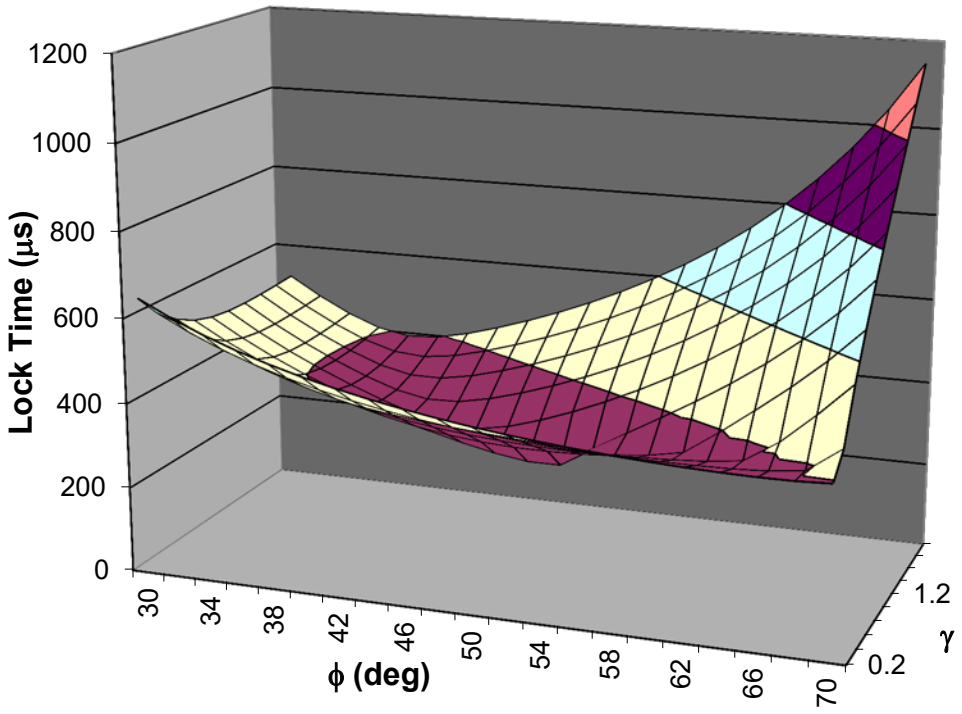


Figure 36.1 *Lock Time as a Function of Phase Margin and Gamma*

Figure 36.1 shows the lock time for this loop filter as a function of phase margin and the gamma optimization parameter for a second order filter. There is a specific value of gamma and phase margin that minimize the lock time. Later in this chapter, this will be shown to be a phase margin of 50.8 degrees and a gamma value of 1.0062.

Figure 36.2 shows the impact of phase margin and gamma on spur gain. The spur gain does not have a minimum point. As the phase margin is decreased and the gamma value is increased, the spur gain decreases. However, the impact of phase margin and gamma on spur gain is much less than the impact of phase margin and gamma on lock time, so it makes sense to choose the phase margin and gamma value such that lock time is minimized.

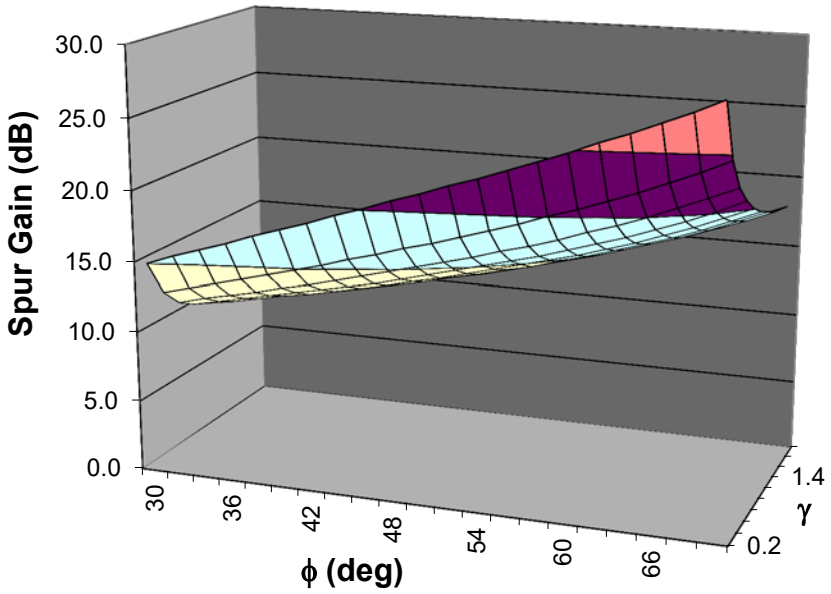


Figure 36.2 *Spur Gain as a Function of Phase Margin and Gamma*

T31 *%*	**Phi** *Deg*	**Gamma** *n/a*	**LT** *µs*	**SG** *dB*
0	50.8	1.006	246.4	29.9
10	49.8	1.045	243.3	28.7
20	49.0	1.075	240.6	26.6
30	48.2	1.098	238.3	24.8
40	47.8	1.115	236.4	23.7
50	47.4	1.127	235.0	22.9
60	47.1	1.136	233.9	22.4
70	47.0	1.141	233.2	22.0
80	47.0	1.144	232.8	21.9
90	46.7	1.147	232.5	21.7
100	46.8	1.147	232.4	21.7

Table 36.4 *Gamma and Phase Margin Values that Minimize Lock Time*

Table 36.4 shows how to choose gamma and the phase margin in order to minimize lock time. These numbers may vary slightly if the frequency jump or frequency tolerance for lock time is changed. One thing that this does not take into consideration is the spur gain. The next simulation does this.

Second Simulation: Optimal Choice of Phase Margin and Gamma to Give the Best Trade-Off between Lock Time and Spurs

For most designs, it is more realistic to try to minimize lock time while keeping the spur levels constant. Although the loop bandwidth is the most dominant factor, phase margin and the gamma optimization parameter have some impact on spurs. Since lock time and spurs are a tradeoff, the following table tries to consider both of these by minimizing the following index:

$$Index = 40 \cdot log\left|\frac{LockTime}{100\,\mu s}\right| + SpurGain \qquad \textbf{(36.4)}$$

T31 *%*	***Phi*** *Deg*	***Gamma*** *n/a*	***LT*** *µs*	***SG*** *dB*
0	49.2	1.024	249.9	29.5
10	46.8	1.081	252.9	27.6
20	44.5	1.144	258.8	24.6
30	43.7	1.168	257.6	22.8
40	43.2	1.184	255.9	21.6
50	42.5	1.203	257.0	20.6
60	42.5	1.204	254.2	20.2
70	42.2	1.212	254.3	19.8
80	42.5	1.207	251.7	19.8
90	42.4	1.209	251.6	19.7
100	42.3	1.211	251.9	19.6

Table 36.5 *Optimal Choices for Phase Margin and Gamma to Minimize Index*

The table above is the fundamental result for this chapter. The bottom line is that one should choose ***T31*** as high as realistically possible for the best lock time and spur performance, while keeping the capacitor size next to the VCO large enough to not be significantly impacted by the VCO input capacitance and the series resistor to the VCO not too large so that it does not contribute too much thermal noise. Once this parameter is chosen, then the optimal value for phase margin and gamma can be found from the table. Note that if the frequency jump or tolerance is changed, these numbers change slightly, but this effect is small and can be disregarded for practical purposes. The ***T43*** ratio was not included because the simulation tool used to generate this table could not model the lock time for this without approximations.

Impact of Gamma Optimization Parameter on Peaking and Flatness

If there is a lot of margin on lock time, then designing for a gamma optimization parameter higher than what is theoretically optimal for lock time might sensible. By doing so, it increases the flatness of the filter and it also pushes the point where the VCO noise transfer function peaks beyond the loop bandwidth. This is useful in situations where the VCO noise is causing the majority of the peaking. It may also be helpful in the case that part of the loop filter is partially integrated, as it allows a wider loop bandwidth. Figure 36.3 shows that increasing gamma decreases peaking of the loop filter response as well as spurs outside the loop bandwidth. The tradeoff is that making gamma large degrades lock time severely. One should also be mindful that although large gamma values make the closed loop response look flatter, it can cause peaking in the VCO phase noise response as shown in Figure 36.4.

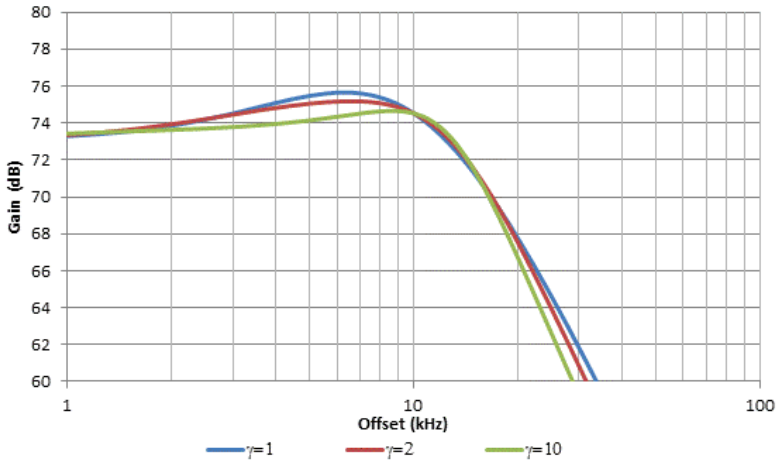


Figure 36.3 *Impact of Gamma Optimization Factor on Closed Loop Gain*

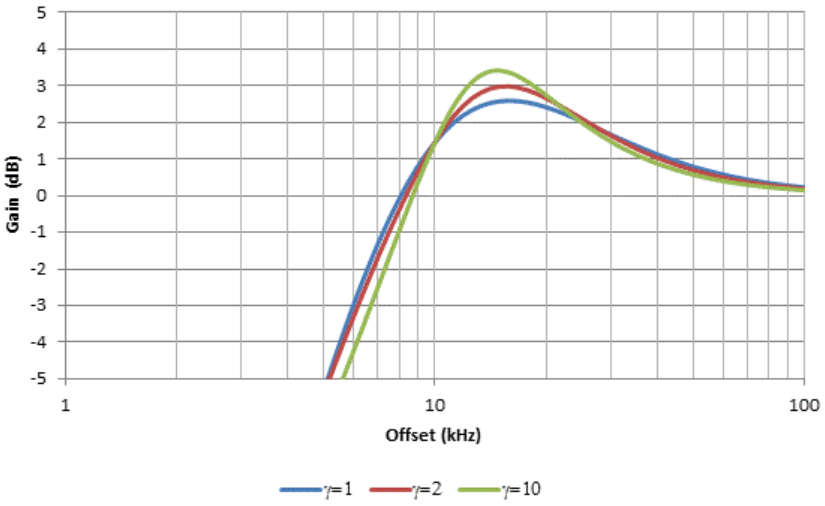


Figure 36.4 *Impact of Gamma on the VCO Transfer Function Gain*

Typically, the VCO noise, PLL noise, and resistor noises peak close to the loop bandwidth. However, when gamma is made much larger than one, these noise sources can peak at different frequencies, making the spectrum look more flat. However, this is more due to noise shaping, instead of simply making the PLL more stable or PLL response less flat.

Adjusting Gamma to Deal with Restricted Loop Bandwidth Situations

In some situations, the loop bandwidth of the PLL can be restricted by the VCO input capacitance or extra fixed poles that are integrated on the chip. In this situation, it is sometimes the case that it is hard to get as wide of a loop bandwidth as desired. If this is the case, consider increasing gamma to allow for a wider loop bandwidth.

Conclusion

Optimal choices for the gamma optimization parameter have been discussed. In most situations, the design objective is a trade-off between lock times and spurs. By simply choosing gamma in an optimal way instead of just equal to one, lock time can be dramatically improved by up to 30% while simultaneously reducing the spur gain. This is done with the restriction that the loop bandwidth is constant. This assumes the goal is minimization of lock time and spurs.

In some situations, the design objective is to make the loop filter response as flat as possible and/or reduce the RMS phase error. In these situations, it may make sense to sacrifice lock time by designing for a much higher phase margin and gamma optimization factor than one would do if they were optimizing for spurs and lock time.

Chapter 37 Choosing Filter Order and Pole Ratios

Introduction

The simplest usable filter is the second order filter, but there is the option of adding additional poles. In the right situation, additional poles can reduce spurs and delta sigma modulator noise. In the wrong situation, additional poles can add resistor noise, restrict the loop bandwidth, or even cause instability. When considering the addition of a pole, conceptually one compares this pole to the previous pole. For instance, when adding a pole to a second order loop filter, one considers the ratio of newly added pole, T3, to the previous pole T1. For this reason, it makes sense to define a pole ratio of T3/T1, or sometimes abbreviated T31. In the case of adding a pole to a third order to make it fourth order, one considers the ratio of the newly added pole, T4, to the last pole T3. In this case, we define a pole ratio of T4/T3, which is sometimes abbreviated as T43.

If these pole ratios are zero, then the filter is considered one order lower. For instance, a third order filter with T31=0 is really a second order filter. A fourth order filter with T43 = 0 and T31>0 is really a third order filter. For the purposes of spur attenuation, choosing the pole ratios to be one, or 100% give the maximum possible result, but this also leads to zero capacitors and infinite resistors.

Although higher order filters will always eventually provide more attenuation of PLL noise and spurs provided the offset is sufficiently high, it is unrealistic to expect this in practice as noise and spurs will eventually be dominated by crosstalk. For instance, if there is a spur at 100 MHz offset, it is likely to be dominated by crosstalk around the loop filter and therefore will not be impacted by additional poles in the loop filter. It therefore makes the most sense to choose some offset frequency of interest and then discuss what the impact of a higher order filter will have at this offset frequency. For an integer PLL, this offset might be chosen to be equal to the phase detector frequency, provided it is not too high (<10 MHz). For a delta sigma fractional PLL, this offset might be chosen to be half the phase detector frequency, which is the frequency where the noise peaks. Another possibility for a fractional PLL might be a particular offset for a fractional spur. Based on the assumption of an offset frequency being chosen, this chapter discusses when higher order filters make sense, what pole ratios might be reasonable to try, and what benefit can be expected from a higher order filter.

Identifying when Additional Poles Can Help

In the appendix, it has been shown that the theoretical maximum attenuation for the added poles is when they are all equal. Although this is physically impossible for a passive filter, it still serves as a good way to make some general guidelines to understand the impact of higher order filters. Another result derived in the appendix is that the zero, T2, and the sum of the poles, T1+T3+T4, is roughly independent of filter order.

A key parameter is the ratio of the offset frequency to the loop bandwidth.

$$r = \frac{Offset}{BW} = \frac{\omega}{\omega c} \tag{37.1}$$

A secondary parameter depends on gamma and the phase margin.

$$\alpha = \frac{2}{\sqrt{(1+\gamma)^2 \cdot tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot tan\,\phi} \tag{37.2}$$

The following table shows some calculated values for this alpha parameter.

		Phase Margin (deg)												
		20	25	30	35	40	45	50	55	60	65	70	75	80
Gamma	0.01	39.305	49.132	59.980	72.108	85.913	101.981	121.192	144.933	175.507	217.056	277.855	377.202	572.974
	0.02	20.949	25.725	31.055	37.060	43.932	51.962	61.591	73.516	88.897	109.825	140.477	190.597	289.408
	0.05	9.704	11.527	13.595	15.958	18.691	21.913	25.802	30.644	36.915	45.474	58.042	78.627	119.265
	0.1	5.744	6.636	7.657	8.834	10.210	11.844	13.832	16.322	19.564	24.006	30.550	41.295	62.544
	0.2	3.580	4.037	4.560	5.169	5.884	6.742	7.792	9.117	10.853	13.245	16.783	22.613	34.174
	0.5	2.062	2.277	2.524	2.812	3.152	3.562	4.067	4.709	5.556	6.731	8.478	11.372	17.131
	1	1.428	1.570	1.732	1.921	2.145	2.414	2.747	3.172	3.732	4.511	5.671	7.596	11.430
	2	1.031	1.139	1.262	1.406	1.576	1.781	2.034	2.355	2.778	3.365	4.239	5.686	8.565
	5	0.716	0.807	0.912	1.034	1.177	1.348	1.558	1.823	2.171	2.649	3.357	4.523	6.835
	10	0.574	0.664	0.766	0.883	1.021	1.184	1.383	1.632	1.956	2.401	3.055	4.129	6.254
	20	0.485	0.576	0.680	0.798	0.935	1.096	1.290	1.532	1.846	2.274	2.902	3.931	5.963
	50	0.419	0.515	0.621	0.741	0.879	1.039	1.232	1.470	1.778	2.197	2.810	3.812	5.788
	100	0.393	0.491	0.600	0.721	0.859	1.020	1.212	1.449	1.755	2.171	2.779	3.772	5.730

Table 37.1 *Calculated Values of α*

Based on these parameters, the theoretical benefit for the 3rd order filter over the second order filter, and the theoretical benefit for the fourth order filter over the third order filter can be derived as done in the appendix.

$$3rd\ Order\ Benefit \approx \sqrt{\frac{\left(1+\left(\frac{r}{2\cdot\alpha}\right)^2\right)^2}{\left(1+\left(\frac{r}{\alpha}\right)^2\right)}} \tag{37.3}$$

$$4th\ Order\ Benefit \approx \sqrt{\frac{\left(1+\left(\frac{r}{3\cdot\alpha}\right)^2\right)^3}{\left(1+\left(\frac{r}{2\cdot\alpha}\right)^2\right)^2}} \qquad (37.4)$$

These functions are graphed in Figure 37.1. One observation to make is that for r/ α values greater than 10, the lines are parallel and go at 20 dB/decade. For instance, for r/α = 100 and a third order filter, the benefit would be about 24 dB.

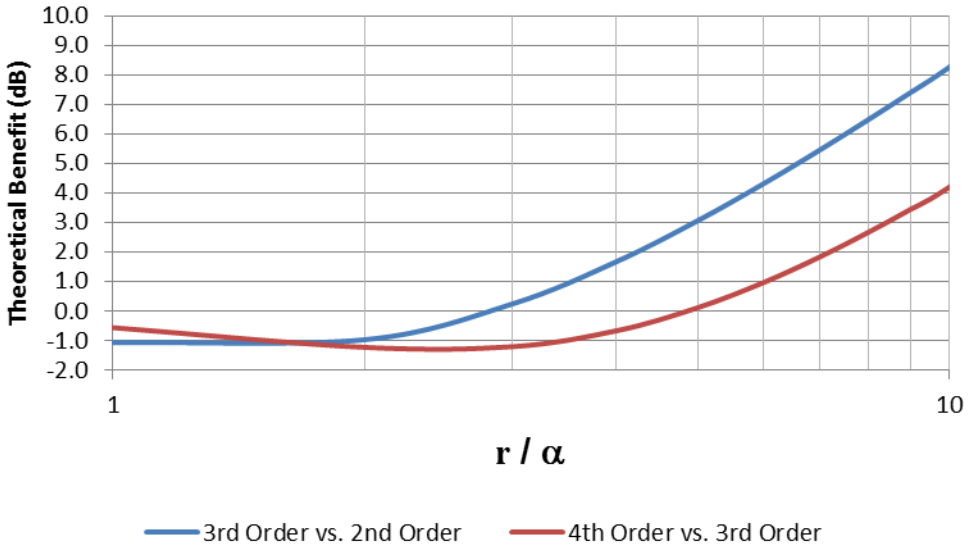


Figure 37.1 *Theoretical Benefits of Higher Order Filters*

r/α	3rd Order vs. 2nd Order	4th Order vs. 3rd Order
1	-1.1	-0.6
2	-1.0	-1.2
3	0.2	-1.2
4	1.7	-0.7
5	3.1	0.1
6	4.3	1.0
7	5.5	1.8
8	6.5	2.7
9	7.4	3.5
10	8.3	4.2
Large r/α > 10	20·log(r/α)-12	20·log(r/α)-16.6

Table 37.2 *Theoretical Maximum Benefits of Higher Order Filters*

Based on Figure 37.1, a reasonable assumption is to assume that higher order filters only make sense if their theoretical benefit is 1 dB or greater for a given offset frequency. This is summarized in Table 37.3.

Criteria	3rd Order Filter	4th Order Filter
0 dB Benefit	r=2.818·α	r =4.868·α
1 dB Benefit	r =3.532·α	r =6.035·α

Table 37.3 *Benefits of Higher Order Filters*

Recall that α is a function of gamma and phase margin. Applying this result to the third order filter for various values of gamma and phase margin yields the following table for the ***r*** ratio.

		Phase Margin (deg)												
		20	*25*	*30*	*35*	*40*	*45*	*50*	*55*	*60*	*65*	*70*	*75*	*80*
Gamma	*0.01*	138.8	173.5	211.8	254.7	303.4	360.2	428.1	511.9	619.9	766.6	981.4	1332.3	2023.7
	0.02	74.0	90.9	109.7	130.9	155.2	183.5	217.5	259.7	314.0	387.9	496.2	673.2	1022.2
	0.05	34.3	40.7	48.0	56.4	66.0	77.4	91.1	108.2	130.4	160.6	205.0	277.7	421.2
	0.1	20.3	23.4	27.0	31.2	36.1	41.8	48.9	57.7	69.1	84.8	107.9	145.9	220.9
	0.2	12.6	14.3	16.1	18.3	20.8	23.8	27.5	32.2	38.3	46.8	59.3	79.9	120.7
	0.5	7.3	8.0	8.9	9.9	11.1	12.6	14.4	16.6	19.6	23.8	29.9	40.2	60.5
	1	5.0	5.5	6.1	6.8	7.6	8.5	9.7	11.2	13.2	15.9	20.0	26.8	40.4
	2	3.6	4.0	4.5	5.0	5.6	6.3	7.2	8.3	9.8	11.9	15.0	20.1	30.3
	5	2.5	2.9	3.2	3.7	4.2	4.8	5.5	6.4	7.7	9.4	11.9	16.0	24.1
	10	2.0	2.3	2.7	3.1	3.6	4.2	4.9	5.8	6.9	8.5	10.8	14.6	22.1
	20	1.7	2.0	2.4	2.8	3.3	3.9	4.6	5.4	6.5	8.0	10.3	13.9	21.1
	50	1.5	1.8	2.2	2.6	3.1	3.7	4.4	5.2	6.3	7.8	9.9	13.5	20.4
	100	1.4	1.7	2.1	2.5	3.0	3.6	4.3	5.1	6.2	7.7	9.8	13.3	20.2

Table 37.4 *Required Offset/BW Ratios for One dB Benefit for 3rd Order Filter*

Applying this result to the third order filter for various values of gamma and phase margin yields Table 37.5.

		Phase Margin (deg)												
		20	*25*	*30*	*35*	*40*	*45*	*50*	*55*	*60*	*65*	*70*	*75*	*80*
Gamma	*0.01*	237.2	296.5	362.0	435.2	518.5	615.5	731.4	874.7	1059.2	1309.9	1676.9	2276.4	3457.9
	0.02	126.4	155.3	187.4	223.7	265.1	313.6	371.7	443.7	536.5	662.8	847.8	1150.3	1746.6
	0.05	58.6	69.6	82.0	96.3	112.8	132.2	155.7	184.9	222.8	274.4	350.3	474.5	719.8
	0.1	34.7	40.0	46.2	53.3	61.6	71.5	83.5	98.5	118.1	144.9	184.4	249.2	377.5
	0.2	21.6	24.4	27.5	31.2	35.5	40.7	47.0	55.0	65.5	79.9	101.3	136.5	206.2
	0.5	12.4	13.7	15.2	17.0	19.0	21.5	24.5	28.4	33.5	40.6	51.2	68.6	103.4
	1	8.6	9.5	10.5	11.6	12.9	14.6	16.6	19.1	22.5	27.2	34.2	45.8	69.0
	2	6.2	6.9	7.6	8.5	9.5	10.7	12.3	14.2	16.8	20.3	25.6	34.3	51.7
	5	4.3	4.9	5.5	6.2	7.1	8.1	9.4	11.0	13.1	16.0	20.3	27.3	41.2
	10	3.5	4.0	4.6	5.3	6.2	7.1	8.3	9.9	11.8	14.5	18.4	24.9	37.7
	20	2.9	3.5	4.1	4.8	5.6	6.6	7.8	9.2	11.1	13.7	17.5	23.7	36.0
	50	2.5	3.1	3.7	4.5	5.3	6.3	7.4	8.9	10.7	13.3	17.0	23.0	34.9
	100	2.4	3.0	3.6	4.4	5.2	6.2	7.3	8.7	10.6	13.1	16.8	22.8	34.6

Table 37.5 *Required Offset/BW Ratios for One dB Benefit for 4th Order Filter*

Choosing the Pole Ratio

So far, the maximum theoretical effectiveness of higher order filters has been discussed, assuming pole ratios of one. As the pole ratio approaches 100%, the benefit maximum of the higher order filter is approached, but this happens with diminishing returns and it is often the case that the pole ratio is chosen less than 100%. For instance, for a passive filter, a 100% pole ratio yields the unrealistic result of zero capacitors and infinite resistors. This section discusses the impact of choosing a pole ratio that is less than 100%, while searching for a reasonable compromise that gives the majority of the benefit.

Based on simulations and derivations in the appendix, the attenuation relative to what it would be for T31 = 1 would be;

$$Relative\ Attenuation = 20 \cdot log \left| \frac{4 \cdot T31}{(1 + T31)^2} \right| \qquad \textbf{(37.5)}$$

The following figure shows that a pole ratio of 51% gets one within 1 dB of the maximum achievable benefit and a pole ratio of 62% gets one within 0.5 dB of the maximum benefit.

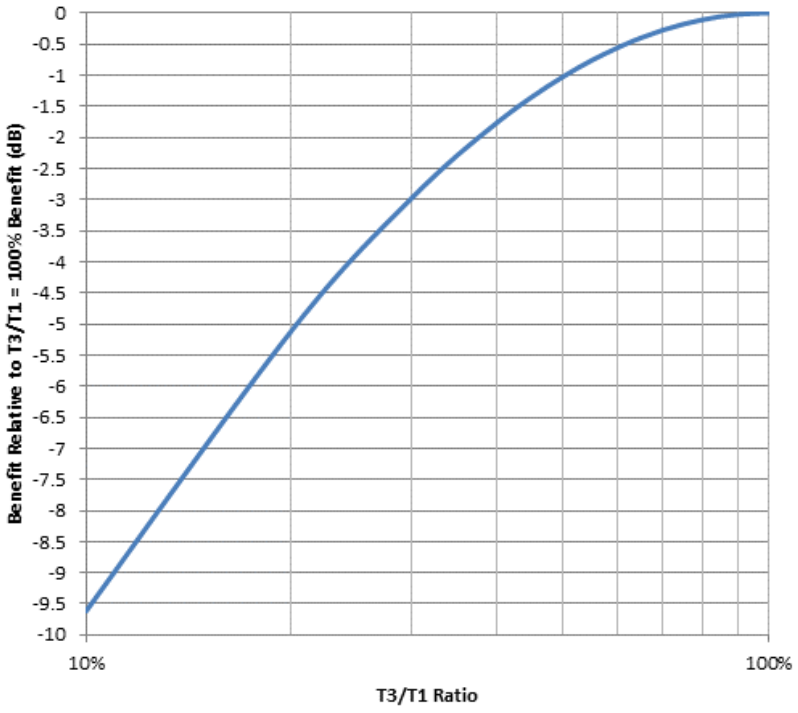


Figure 37.2 *Relative Attenuation for T3/T1 < 100% for r=∞*

In the case of a fourth order filter, the relative attenuation has also been derived in the appendix and is as follows:

$$Relative\ Attenuation = 20 \cdot log \left| \frac{27 \cdot T31^2 \cdot T43}{(1 + T31 + T31 \cdot T43)^3} \right| \qquad \textbf{(37.6)}$$

Table 37.6 shows some of the values calculated from this formula. To illustrate this table, consider a case where both T3/T1 and T4/T3 are 50%. In this case, the attenuation of spurs at sufficiently far offsets is 4 dB worse than is theoretically possible with a filter with both these pole ratios at 100%. T3/T1 and T4/T3 both as 100% is unrealizable and for passive filters as this leads to infinite resistor values and zero capacitor values. As a rule of thumb, a realistic goal might be to get within 1 dB of the maximum possible attenuation. For this goal, there is no way to get there unless both T3/T1 and T4/T3 are above 60%.

		T3/T1									
		10%	20%	30%	40%	50%	60%	70%	80%	90%	100%
T4/T3	10%	-34.1	-24.5	-19.7	-16.8	-14.8	-13.5	-12.4	-11.7	-11.1	-10.7
	20%	-28.3	-18.9	-14.3	-11.5	-9.6	-8.4	-7.4	-6.8	-6.3	-5.9
	30%	-25.0	-15.8	-11.3	-8.7	-6.9	-5.7	-4.9	-4.3	-3.8	-3.5
	40%	-22.7	-13.7	-9.4	-6.8	-5.2	-4.1	-3.3	-2.8	-2.4	-2.1
	50%	-21.0	-12.2	-8.0	-5.6	-4.0	-3.0	-2.3	-1.8	-1.5	-1.3
	60%	-19.7	-11.0	-6.9	-4.6	-3.2	-2.2	-1.6	-1.2	-0.9	-0.7
	70%	-18.6	-10.1	-6.1	-3.9	-2.5	-1.7	-1.1	-0.7	-0.5	-0.4
	80%	-17.6	-9.3	-5.5	-3.4	-2.1	-1.3	-0.8	-0.4	-0.2	-0.1
	90%	-16.8	-8.6	-5.0	-2.9	-1.7	-1.0	-0.5	-0.2	-0.1	0.0
	100%	-16.1	-8.1	-4.5	-2.6	-1.5	-0.8	-0.4	-0.1	0.0	0.0

Table 37.6 *Relative Attenuation Values to Maximum for T3/T1 and T4/T3*

Practical Examples

Close-In Spur Example

Consider the case of a fractional PLL with a 10 MHz phase detector frequency and an output frequency of 2700.015 MHz. Suppose that the integer boundary spur at 15 kHz is troublesome and the loop bandwidth is 10 kHz. Does a higher order filter make sense in this case?

In this case, we calculate r=15 kHz/10 kHz = 1.5. Table 37.4 suggests a very low phase margin of about 20 degrees and an extreme gamma of 50 for just a 1 dB benefit. So from a practical case, the answer is no, a higher order filter does not make sense for reducing this 15 kHz spur.

Intermediate Offset Spur Example

Consider the case of a fractional PLL with a 200 kHz phase detector frequency and an output frequency of 2700 MHz. Suppose that phase detector spur at 200 kHz is troublesome and the loop bandwidth is 10 kHz. Does a higher order filter make sense in this case?

In this case, we calculate r=200 kHz/10kHz = 20. Looking a Table 37.4, it looks like a third order filter does make sense for most values of gamma and phase margin. Looking at Table 37.5, it looks like a fourth order could make sense if the phase margin is 50 degrees or less, but not for a high phase margin design.

Delta Sigma Modulator Noise Example

Consider the case of a fractional PLL with a 20 MHz phase detector frequency and an output frequency of 2700 MHz. Suppose that delta sigma modulator noise is showing up at 10 MHz offset and the loop bandwidth is 100 kHz. Does a higher order filter make sense in this case?

In this case, we calculate ***r*** =10 MHz/100kHz = 100. For such a high ***r*** value, the 4^{th} order filter will definitely be able to attenuate this noise. Maybe a third order filter would be sufficient and the extra pole would not be necessary. In any case, higher order filters definitely make sense in this case.

Far Offset Spur Example

Consider the case of an integer PLL with 10 MHz phase detector frequency and an output frequency of 2700 MHz. Suppose integer boundary spur at 10 MHz is an issue and the loop bandwidth is 10 kHz. Does a higher order filter make sense in this case?

In this case, we calculate r=10 MHz/10kHz = 1000. Based on all the tables and theory, higher order filters could definitely attenuate any spur energy going through the loop filter. However, in practice, this spur is likely due to spur energy crosstalking around the loop filter. So in this case, one might try a higher order filter, but the likely result is that it does not improve the spur as it is caused by crosstalk, not spur energy going through the loop filter.

Active Filter Example

Consider an active filter with a phase detector frequency of 1 MHz and spur of concern is 1 MHz with a loop bandwidth of 1 kHz. Does a higher order filter make sense in this case?

In terms of spur attenuation, higher order filters are unlikely to help. However, the placement of a pole after the op-amp is often beneficial to attenuating the op-amp noise, which is beneficial. In the case of an active filter, it is possible to make T3/T1 = 100% or even higher. Sometimes one might want to make it higher to get even more attenuation of the op-amp noise.

Conclusion

This chapter investigated the impact of designing loop filters of higher than second order and when it makes sense to do so. As a general practice for prototyping, it is good to accommodate the fourth order filter on the PCB board and then use zero ohm resistors if the extra poles are not needed.

The benefits of higher filter orders depend mainly on how far the noise/spur frequency of interest is from the loop bandwidth. Although fully detailed rules are given, if one considers the case for a phase margin of 50 degrees and a gamma of one, these rules suggest a third order loop filter adds value in filtering off noise/spurs that is at least ten times the loop bandwidth and a fourth order loop filter becomes worthwhile for filtering off noise/spurs that is at least 17 times the loop bandwidth.

Appendix: Derivation of Impact of Filter Order

Approximate Independence of T2 and Sum of the Poles vs. Filter Order

A key approximation is that the time constant, ***T2***, is roughly independent of filter order. To see this result, recall the following results for the phase margin.

$$\phi = 180 + tan^{-1}(\omega c \cdot T2) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T3) - tan^{-1}(\omega c \cdot T4) \quad \textbf{(37.7)}$$

Using the knowledge that the poles will be at a higher frequency than the loop bandwidth, the following approximation can be used:

$$\tan^{-1}(\mathrm{x}) \approx x \quad \textbf{(37.8)}$$

Combining these two formulas yield the following:

$$\phi \approx 180 + tan^{-1}(\omega c \cdot T2) - tan^{-1}[\omega c \cdot (T1 + T3 + T4)] \quad \textbf{(37.9)}$$

Recall the definition for gamma:

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1 + T3 + T4)} \quad \textbf{(37.10)}$$

Combining this yields the following approximation:

$$\phi \approx 180 + tan^{-1}(\omega c \cdot T2) - tan^{-1}\left(\frac{\gamma}{\omega c \cdot T2}\right) \quad \textbf{(37.11)}$$

This equation can be solved for *T2* by taking the tangent of both sides.

$$T2 \approx \frac{1}{\omega c} \cdot \frac{2 \cdot \gamma}{\sqrt{(1+\gamma)^2 \cdot tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot tan\,\phi} \quad \textbf{(37.12)}$$

Here we have a function for T2 that involves only phase margin, loop bandwidth and gamma. This demonstrates that T2 is mainly independent of filter order and this also implies that the sum of the poles is mainly independent of filter order.

$$T1 + T3 + T4 = \frac{\gamma}{\omega c^2 \cdot T2} \quad \textbf{(37.13)}$$

Derivation that Maximum Attenuation is when All Poles are Equal
Starting with the approximation that T2 is independent of filter order, one can calculate the benefit of the pole, T1 by taking the filter gain with this pole and dividing it without it.

$$A(\omega) \approx \sqrt{(1+\omega^2 \cdot T1^2) \cdot (1+\omega^2 \cdot T3^2) \cdot (1+\omega^2 \cdot T4^2)} \quad \textbf{(37.14)}$$

We know that the sum of the poles is approximately constant, so using the method of *Lagrange multipliers*, we take a derivative of all the constraints and get the following system of equations. Note that we choose to maximize the square of the filter attenuation to simplify the mathematics.

$$\begin{aligned} F(A^2, \lambda) = {} & (1+\omega^2 \cdot T1^2) \cdot (1+\omega^2 \cdot T3^2) \cdot (1+\omega^2 \cdot T4^2) \\ & - \lambda \cdot \left(T1 + T3 + T4 - \frac{\gamma}{\omega c^2 \cdot T2}\right) \end{aligned} \quad \textbf{(37.15)}$$

Taking the derivative with respect to T1, T3, T4, and λ gives a system of equations

$$dF/_{dT1} = 0 = 2 \cdot \omega^2 \cdot T1^2 \cdot (1+\omega^2 \cdot T3^2) \cdot (1+\omega^2 \cdot T4^2) - \lambda \cdot T1 \quad \textbf{(37.16)}$$

$$dF/_{dT3} = 0 = 2 \cdot \omega^2 \cdot T3^2 \cdot (1+\omega^2 \cdot T1^2) \cdot (1+\omega^2 \cdot T4^2) - \lambda \cdot T3 \quad \textbf{(37.17)}$$

$$dF/_{dT4} = 0 = 2 \cdot \omega^2 \cdot T4^2 \cdot (1+\omega^2 \cdot T1^2) \cdot (1+\omega^2 \cdot T3^2) - \lambda \cdot T4 \quad \textbf{(37.18)}$$

$$dF/_{d\lambda} = T1 + T3 + T4 - \frac{\gamma}{\omega c^2 \cdot T2} \quad \textbf{(37.19)}$$

The first three equations imply that all the poles are equal.

$$T1 = T3 = T4 \quad \textbf{(37.20)}$$

This example was the fourth order filter, but the conclusion is the same that all the poles should theoretically be equal for the maximum attenuation.

Derivation for the Benefit of Higher Order Filters

Using the expression (37.14), we can derive an expression for the theoretical maximum benefit of a third order filter over a second order one.

$$\frac{A_{3rd,Max}(\omega)}{A_{2nd,Max}(\omega)} \approx \sqrt{\frac{\left(1+\omega^2\cdot {T1_{3rd}}^2\right)^2}{\left(1+\omega^2\cdot {T1_{2nd}}^2\right)}} = \sqrt{\frac{\left(1+\omega^2\cdot\left(\frac{\gamma}{2\cdot\omega c^2\cdot T2}\right)^2\right)^2}{\left(1+\omega^2\cdot\left(\frac{\gamma}{\omega c^2\cdot T2}\right)^2\right)}} \qquad \textbf{(37.21)}$$

Combine (37.2) and (37.12) to get the following:

$$\frac{1}{\alpha} = \frac{\sqrt{(1+\gamma)^2\cdot tan^2\phi + 4\cdot\gamma} - (1+\gamma)\cdot tan\,\phi}{2} \approx \frac{\gamma}{\omega c\cdot T2} \qquad \textbf{(37.22)}$$

Combining (37.1) with (37.22) allows the following substitution:

$$\left(\frac{r}{\alpha}\right)^2 \rightarrow \omega^2\cdot\left(\frac{\gamma}{\omega c^2\cdot T2}\right)^2 \qquad \textbf{(37.23)}$$

This can be rearranged as follows:

$$\frac{A_{3rd,Max}(r\cdot\alpha)}{A_{2nd,Max}(r\cdot\alpha)} \approx \sqrt{\frac{\left(1+\left(\frac{r}{2\cdot\alpha}\right)^2\right)^2}{\left(1+\left(\frac{r}{\alpha}\right)^2\right)}} \qquad \textbf{(37.24)}$$

Here we have an expression that relates the third order attenuation benefits as only a function α, which is a function of the ratio of the offset to loop bandwidth, phase margin, and gamma. A similar reasoning can be used to derive the theoretical benefits of a fourth order filter over a third one.

$$\frac{A_{4th,Max}(r\cdot\alpha)}{A_{3rd,Max}(r\cdot\alpha)} \approx \sqrt{\frac{\left(1+\left(\frac{r}{3\cdot\alpha}\right)^2\right)^3}{\left(1+\left(\frac{r}{2\cdot\alpha}\right)^2\right)^2}} \qquad \textbf{(37.25)}$$

Derivation of Formula for Attenuation Relative to Maximum Attenuation for Large Offset

Recall that the open loop gain is as follows

$$|G(\omega)| = \frac{K_{PD} \cdot K_{VCO}}{A0 \cdot \omega^2} \cdot \sqrt{\frac{1 + \omega^2 \cdot T2^2}{(1 + \omega^2 \cdot T1^2) \cdot (1 + \omega^2 \cdot T3^2) \cdot (1 + \omega^2 \cdot T4^2)}} \quad \textbf{(37.26)}$$

The sum of the poles has been shown to be approximately constant and therefore we can say that:

$$\kappa = T1 + T3 + T4 = T1 \cdot (1 + T31 + T43 \cdot T31) \quad \textbf{(37.27)}$$

It therefore follows that:

$$T1 = \frac{\kappa}{1 + T31 + T43 \cdot T31} \quad \textbf{(37.28)}$$

$$T3 = \frac{\kappa \cdot T31}{1 + T31 + T43 \cdot T31} \quad \textbf{(37.29)}$$

$$T4 = \frac{\kappa \cdot T43 \cdot T31}{1 + T31 + T43 \cdot T31} \quad \textbf{(37.30)}$$

Now we can reason that T2, the sum of the poles, and A0 is roughly constant as a function of filter order. Now also consider an approximation for large offsets for ω.

For the third order case, we get:

$$|G(\omega, T31)| = \frac{K_{PD} \cdot K_{VCO} \cdot T2 \cdot (1 + T31)^2}{A0 \cdot \omega^3 \cdot \kappa^2 \cdot T31} \quad \textbf{(37.31)}$$

Now consider the ratio of this arbitrary gain to a gain with T31=1.

$$\frac{|G(\omega,1)|}{|G(\omega,T31)|}=\frac{4\cdot T31}{(1+T31)^2} \tag{37.32}$$

For the fourth order case, we get:

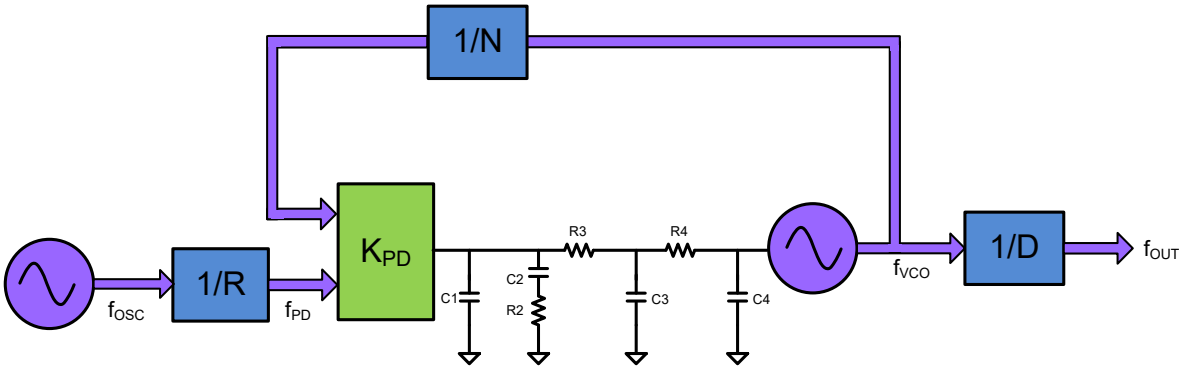
$$|G(\omega,T31)| \ =\frac{K_{PD}\cdot K_{VCO}\cdot T2\cdot(1+T31+T31\cdot T43)^3}{A0\cdot\omega^4\cdot\kappa^3\cdot T31^2\cdot T43} \tag{37.33}$$

Now consider the ratio of this arbitrary gain to a gain with T31=T43=1.

$$\frac{|G(\omega,1,1)|}{|G(\omega,T31,T43)|}=\frac{27\cdot T31^2\cdot T43}{(1+T31+T31\cdot T43)^3} \tag{37.34}$$

Note that this derivation implies that this result is independent of phase margin or gamma, which is also confirmed by simulations. Recall that there were some approximations introduced, but simulations confirm that these results are relatively true. The results presented were taken by doing 20·log of this result.

Equations for PLL Design



Chapter 38 Equations for a Passive Second Order Loop Filter

Introduction

The second order loop filter is the most rudimentary loop filter and allows one to explicitly solve for the component values in closed form. It has the smallest resistor thermal noise and largest capacitor next to the VCO to minimize the impact of VCO input capacitance. This filter also has the most tolerance to variations in VCO gain and charge pump gain. In cases where the first spur to be filtered is less than 10 times the loop bandwidth frequency, filter orders higher than third order do not provide much real improvement in spur levels. For the second order filter ***T3 = T4 = T31 = T43 = 0***.

Loop Filter Impedance, Pole, and Zero

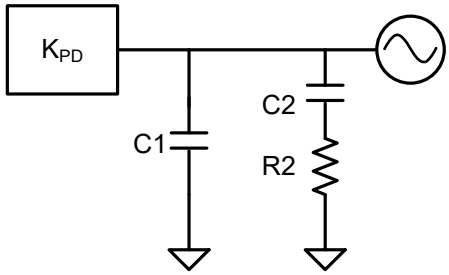


Figure 38.1 *A Second Order Passive Loop Filter*

The transfer function of a second order loop filter is given below:

$$Z(s) = \frac{1 + s \cdot T2}{s \cdot A0 \cdot (1 + s \cdot T1)} = \frac{1 + s \cdot C2 \cdot R2}{s \cdot (C1 + C2) \cdot \left(1 + s \cdot \frac{C1 \cdot C2 \cdot R2}{C1 + C2}\right)} \quad \textbf{(38.1)}$$

From the above equation, it should be clear:

$$T2 = R2 \cdot C2 \quad \textbf{(38.2)}$$

$$T1 = \frac{C1 \cdot C2 \cdot R2}{C1 + C2} \quad \textbf{(38.3)}$$

$$A0 = C1 + C2 \quad \textbf{(38.4)}$$

A system of two equations and two unknowns can be established by calculating the phase margin and also setting the derivative of the phase margin equal to zero at the loop bandwidth.

$$\phi = 180 + arctan(\omega c \cdot T2) - arctan(\omega c \cdot T1) \quad \textbf{(38.5)}$$

$$T2 = \frac{\gamma}{\omega c^2 \cdot T1} \quad \textbf{(38.6)}$$

Substituting (38.6) into (38.5), taking the tangent of both sides, and then solving yields:

$$T1 = \frac{\sqrt{(1+\gamma)^2 \cdot tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot \tan\phi}{2 \cdot \omega c} \quad \textbf{(38.7)}$$

The time constant ***T2*** can now be easily found using equation (38.6). The total loop filter capacitance, ***A0***, can be found and ***C1*** can be calculated.

$$A0 = \frac{C1 \cdot T2}{T1} = \frac{K_{PD} \cdot K_{VCO}}{N \cdot \omega c^2} \cdot \sqrt{\frac{1 + \omega^2 \cdot T2^2}{1 + \omega^2 \cdot T1^2}} \quad \textbf{(38.8)}$$

Once the total capacitance is known, the components can be easily found:

$$C1 = A0 \cdot \frac{T1}{T2} \quad \textbf{(38.9)}$$

$$C2 = A0 - C1 \quad \textbf{(38.10)}$$

$$R2 = \frac{T2}{C2} = \frac{K_{PD} \cdot K_{VCO}}{N \cdot \omega c^2} \quad \textbf{(38.11)}$$

The Degenerate 2nd Order Filter with γ→0

One interesting case is when γ=0. It turns out that this makes C1=0, which would theoretically would be unstable for a charge pump PLL because the entire charge pump current would create a voltage across R2. Nevertheless, this still can be done and it turns out that the input capacitance of the VCO actually makes C1 effectively greater than zero. To derive this case, take an approximation of equation (38.6) and (38.7) and take the limit as γ→0.

$$T2 = \frac{\gamma}{\omega c^2 \cdot T1} = \lim_{\gamma \to 0} \left\{ \frac{\gamma}{\omega c^2} \frac{2 \cdot \omega c}{\sqrt{(1+\gamma)^2 \cdot tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot \tan\phi} \right\} \qquad \textbf{(38.12)}$$

In this expression, both the numerator and denominator go to zero. Simplifying and using L'Hopital's rule to take the derivative with respect to γ for both the numerator and denominator yields the following.

$$\begin{aligned} T2 &= \frac{2}{\omega c} \cdot \lim_{\gamma \to 0} \left\{ \frac{{}^{d}/_{d\gamma}(\gamma)}{{}^{d}/_{d\gamma}\left(\sqrt{(1+\gamma)^2 \cdot tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot \tan\phi\right)} \right\} \\ &= \frac{2}{\omega c} \cdot \left\{ \frac{1}{\frac{2 \cdot tan^2\phi + 4}{2 \cdot \tan\phi} - \tan\phi} \right\} = \frac{\tan\phi}{\omega c} \end{aligned} \qquad \textbf{(38.13)}$$

In this way, C1 is already known to be zero and C2 and R2 can be solved for as normal. Again, it is important to stress that with no C1 capacitor, this is theoretically unstable for a charge pump PLL, but can be stable if the VCO has a nonzero input capacitance to make up for the missing C1.

Conclusion

The formulas for the second order passive loop filter have been presented in this chapter. The second order filter has an elegant closed form solution for the component values and also tends the most simple and most stable, but higher order filters spurs if they are far outside the loop bandwidth.

Reference

[1] Keese, William O.*An Analysis and Performance Evaluation for a Passive Filter Design technique for Charge Pump Phase-Locked Loops.* Application Note 1001, Texas Instruments

Appendix A: A Second Order Loop Filter Design

Design Specifications

Symbol	Description	Value	Units
BW	Loop Bandwidth	10	kHz
ϕ	Phase Margin	49.2	degrees
γ	Gamma Optimization Parameter	1.024	none
K_{PD}	Charge Pump Gain	1	mA
K_{VCO}	VCO Gain	60	MHz/V
f_{VCO}	Output Frequency	1960	MHz
f_{PD}	Phase detector frequency	50	kHz

Calculate Poles and Zero

$$N = \frac{f_{VCO}}{f_{PD}} \tag{38.14}$$

$$\omega c = 2\pi \cdot BW \tag{38.15}$$

$$T1 = \frac{\sqrt{(1+\gamma)^2 \cdot tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot \tan\phi}{2 \cdot \omega c} \tag{38.16}$$

$$T2 = \frac{\gamma}{\omega c^2 \cdot T1} \tag{38.17}$$

Calculate Loop Filter Coefficient

$$A0 = \frac{C1 \cdot T2}{T1} = \frac{K_{PD} \cdot K_{VCO}}{N \cdot \omega c^2} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2}{1 + \omega c^2 \cdot T1}} \tag{38.18}$$

Solve For Components

$$C1 = A0 \cdot \frac{T2}{T1} \tag{38.19}$$

$$C2 = A0 - C1 \tag{38.20}$$

$$R2 = \frac{T2}{C2} \tag{38.21}$$

Results

Symbol	Description	Value	Units
N	N Counter Value	39200	none
ωc	Loop Bandwidth	6.283×10^{4}	rad/s
T1	Loop Filter Pole	5.989×10^{-6}	s
T2	Loop Filter Zero	4.331×10^{-5}	s
A0	Total Capacitance	1.052	nF
C1	Loop Filter Capacitor	0.145	nF
C2	Loop Filter Capacitor	0.906	nF
R2	Loop Filter Resistor	47.776	kΩ

Chapter 39 Equations for a Passive Third Order Loop Filter

Introduction

The third order loop filter is useful in filtering spurs or noise caused by the PLL that is at an offset frequency of ten times the loop bandwidth or greater. Designing the loop filter involves solving for the time constants, and then determining the loop filter components from the time constants. The time constants can be calculated either by introducing a closed form approximate solution or using numerical methods. From these time constants, the components can be found. In addition to specifying the loop bandwidth, (ωc), phase margin (ϕ), and gamma (γ), the user also has to specify the pole ratio, ***T31***. This chapter discusses how to determine the component values for a passive filter from these parameters.

Calculating the Loop Filter Impedance and Time Constants

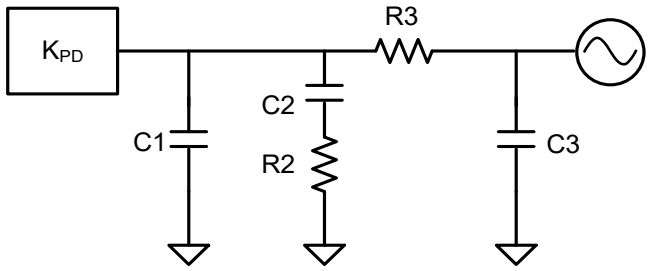


Figure 39.1 *Third Order Passive Loop Filter*

For the loop filter shown in Figure 39.1, the impedance is given below:

$$Z(s) = A0 \cdot \frac{1 + s \cdot T2}{s \cdot A0 \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3)} \quad \textbf{(39.1)}$$

$$T2 = R2 \cdot C2 \quad \textbf{(39.2)}$$

$$A0 = C1 + C2 + C3 \quad \textbf{(39.3)}$$

$$A1 = A0 \cdot (T1 + T3) = C2 \cdot C3 \cdot R2 + C1 \cdot C2 \cdot R2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3 \quad \textbf{(39.4)}$$

$$A2 = A0 \cdot T1 \cdot T3 = C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3 \quad \textbf{(39.5)}$$

Loop Filter Calculation

Calculation of Time Constants

The gamma optimization parameter is defined with the equation as follows:

$$T2 = \frac{\gamma}{\omega c^2 \cdot T1 \cdot (1 + T31)} \tag{39.6}$$

The phase margin is given by:

$$\phi = tan^{-1}(\omega c \cdot T2) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T3) \tag{39.7}$$

Substituting in the expression for T2 yields the following

$$\phi = tan^{-1}\left(\frac{\gamma}{\omega c \cdot T1 \cdot (1 + T31)}\right) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T31 \cdot T1) \tag{39.8}$$

The only unknown in this is equation is T1 and it can be found by numerical methods. If an approximation is acceptable, one can introduce the following:

$$\tan(x) \approx x \approx tan^{-1}(x) \tag{39.9}$$

Using this approximate rule, an elegant solution for T1 can be found.

$$T1 \approx \frac{sec(\phi) - \tan(\phi)}{\omega c \cdot (1 + T31)} \tag{39.10}$$

So whether numerical methods or approximation (39.10) are used to find ***T1***, the other time constants can easily be found.

$$T3 = T1 \cdot T31 \tag{39.11}$$

$$T2 = \frac{\gamma}{\omega c \cdot (T1 + T3)} \tag{39.12}$$

Solution of Component Values from Time Constants

Calculation of Filter constants

The first step is to calculate the filter constants:

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2)}} \quad \textbf{(39.13)}$$

$$A1 = A0 \cdot (T1 + T3) \quad \textbf{(39.14)}$$

$$A2 = A0 \cdot T1 \cdot T3 \quad \textbf{(39.15)}$$

Finding Components from Filter Coefficients

Recall that the loop filter components relate to the time constants in the following manner for a passive filter.

$$T2 = R2 \cdot C2 \quad \textbf{(39.16)}$$

$$A0 = C1 + C2 + C3 \quad \textbf{(39.17)}$$

$$A1 = C2 \cdot C3 \cdot R2 + C1 \cdot C2 \cdot R2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3 \quad \textbf{(39.18)}$$

$$A2 = C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3 \quad \textbf{(39.19)}$$

Here we have a system of four equations with five unknowns. As this system has infinitely many solutions, it makes sense to impose an additional constraint. In this case, a very good choice would be to maximize the value of ***C3*** in order to minimize the impact of the VCO input capacitance. This choice is also close to choice that would that would minimize the resistor noise due to resistor ***R3***. Using these equations to find ***C3*** as an expression of ***C1*** yields the following:

$$C3 = \frac{-T2^2 \cdot C1^2 + T2 \cdot A1 \cdot C1 - A2 \cdot A0}{T2^2 \cdot C1 - A2} \quad \textbf{(39.20)}$$

By taking the derivative of this equation with respect to C1 and treating C3 as a function of C1 and setting *dC3/dC1*=0, we obtain the following expression for C1. Further justification for this derivation is in the appendix.

$$C1 = \frac{A2}{T2^2} \cdot \left(1 + \sqrt{1 + \frac{T2}{A2} \cdot (T2 \cdot A0 - A1)}\right) \quad \textbf{(39.21)}$$

Once ***C1*** is known, ***C3*** can be found and then ***C2*** and the other components can now be derived.

$$C2 = A0 - C1 - C3 \quad \textbf{(39.22)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(39.23)}$$

$$R3 = \frac{A2}{C1 \cdot C3 \cdot T2} \quad \textbf{(39.24)}$$

Conclusion

This chapter has presented a method for calculating a third order passive loop filter. Unlike the second order filter equations, there is no closed form solution for the time constants, although it is easy to solve for them numerically. Once these time constants are known, then the component values can be calculated. For those who wish to avoid these numerical methods, simplified approximate equations for the time constants have also been presented.

Regardless of the filter calculation method used, the VCO input capacitance adds to capacitor ***C3***, so this component should be at least four times the VCO input capacitance. If this is not possible then try decreasing the value of ***T31*** so that ***C3*** will become larger and ***R3*** will become smaller. Choosing ***C3*** as large as possible also corresponds to choosing ***R3*** as small as possible. It is desirable to not have the ***R3*** resistor too large, or else the thermal noise from this resistor can add to the out of band phase noise.

References

[1] Keese, William O.*An Analysis and Performance Evaluation for a Passive Filter Design technique for Charge Pump Phase-Locked Loops.* Application Note 1001, Texas Instruments

Appendix: Choosing C1 to Maximize C3

This appendix shows the justification for the optimal choice of C1 to maximize C3. This involves finding the critical point of the equation, verifying that this is a maximum, and then ensuring that this leads to positive component values.

*Find the Critical Points for the Expression for **C3** in terms of **C1** and Find the Critical Point*

The first step is to apply the first derivative to equation (39.20) and equate this to zero in order to find the critical points.

$$\frac{dC3}{dC1} = -\frac{C1^2 - \left(\frac{2 \cdot A2}{T2^2}\right) \cdot C1 + \left(\frac{A1 \cdot A2}{T2^3} - \frac{A2 \cdot A0}{T2^2}\right)}{\left(C1 - \frac{A2}{T2^2}\right)^2} = 0 \qquad \textbf{(39.25)}$$

By setting the numerator equal to zero and solving, the following result is obtained.

$$C1 = \frac{A2}{T2^2}\left(1 \pm \sqrt{1 + \frac{T2}{A2} \cdot (T2 \cdot A0 - A1)}\right) \qquad \textbf{(39.26)}$$

*Find the Correct Critical Point and Verify that it is a Global Maximum for **C1**>0*

Recall that if the second derivative is negative, it indicates the critical point is a local maximum, and if it is positive, it indicates that it is a local minimum. Taking another derivative of (39.25) yields:

$$\frac{d^2C3}{dC1^2} = -\frac{2 \cdot A2 \cdot A0 \cdot \left(T1 \cdot T3 + T2 \cdot (T2 - T1 - T3)\right)}{T2^4 \cdot \left(C1 - \frac{A2}{T2^2}\right)^3} \qquad \textbf{(39.27)}$$

The numerator of this expression is always positive provided T2>T1+T3, which will be the case as it is a requirement for stability. Therefore the requirement on C1 is that:

$$C1 > \frac{A2}{T2^2} \qquad \textbf{(39.28)}$$

This will be satisfied if and only if we take the positive root in expression (39.26).

$$C1 = \frac{A2}{T2^2}\left(1 + \sqrt{1 + \frac{T2}{A2} \cdot (T2 \cdot A0 - A1)}\right) \qquad \textbf{(39.29)}$$

Proof that All Components will be Positive for T31<100%

It is possible to choose the component C1 so that this leads to negative component values. However, if C1 is chosen in accordance to (39.29), then it can be proven that this is never the case. The approach to doing this is to first show that C3 is positive, then C2 is positive, then it easily follows that R2 and R3 are positive as well.

*Proof that **C3** Will Always be Positive*

The expression for ***C3*** can be expressed in terms of time constants, ***C1***, and ***A0***.

$$C3 = \frac{-T2^2 \cdot C1^2 + T2 \cdot A0 \cdot (T1 + T3) \cdot C1 - T1 \cdot T3 \cdot A0^2}{T2^2 \cdot C1 - T1 \cdot T3 \cdot A0} \quad \textbf{(39.30)}$$

By using inequality (39.28), we can see that the denominator will be positive for the optimal choice of ***C1***, but the numerator is not so obvious. The quadratic formula can be applied and the result simplified to yield the restrictions on ***C1*** which are necessary to make ***C3***>0. It is assumed, by definition, that ***T3***>***T1***.

$$\frac{T3}{T2} \cdot A0 < C1 < \frac{T1}{T2} \cdot A0 \quad \textbf{(39.31)}$$

Now applying these above restrictions to the value of ***C1*** shows that they will be satisfied, provided the following conditions are met.

$$T2 > T1 > T3 \quad \textbf{(39.32)}$$

Note that ***T2>T1*** is required for stability and ***T1>T3*** is satisfied since T31<100%. It therefore follows that C3 will always be positive.

*Proof that **C1** is Always be Positive*

To prove that C2 is always positive, the first step is to solve for C2 in terms of C1 using equations (39.16), (39.17), (39.18), and (39.19).

$$C2 = A0 \cdot \frac{\frac{T1 \cdot T3}{T2} + T2 - T1 - T3}{T2 - \frac{A2}{T2 \cdot C1}} \quad \textbf{(39.33)}$$

One can reason that the denominator in expression (39.33) is positive by virtue of (39.28) and one can reason that the numerator is positive by virtue of the stability criteria that T2 > T1+T3. It therefore follows that C2 will be always positive for filters that are designed to be stable.

Appendix A: A Third Order Loop Filter Design

Design Specifications

Symbol	Description	Value	Units
BW	Loop Bandwidth	2	kHz
ϕ	Phase Margin	47.1	degrees
γ	Gamma Optimization Parameter	1.136	none
K_{PD}	Charge Pump Gain	4	mA
K_{VCO}	VCO Gain	30	MHz/V
f_{VCO}	Output Frequency	1392	MHz
f_{PD}	Phase detector frequency	60	kHz
$T31$	Ratio of pole $T3$ to Pole $T1$	0.6	none

Calculate Poles and Zero

$$N = \frac{f_{VCO}}{f_{PD}} \tag{39.34}$$

$$\omega c = 2\pi \cdot BW \tag{39.35}$$

$T1$ is the only unknown. Solve for this using numerical methods.

$$\phi = tan^{-1}\left(\frac{\gamma}{\omega c \cdot T1 \cdot (1 + T31)}\right) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T1 \cdot T31) \tag{39.36}$$

$$T3 = T1 \cdot T31 \tag{39.37}$$

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1 + T3)} \tag{39.38}$$

Calculate Loop Filter Coefficients

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2)}} \quad \textit{(39.39)}$$

$$A1 = A0 \cdot (T1 + T3) \quad \textit{(39.40)}$$

$$A2 = A0 \cdot T1 \cdot T3 \quad \textit{(39.41)}$$

Symbol	Description	Value	Units
N	N Counter Value	23200	none
ωc	Loop Bandwidth	1.2566×10^{4}	rad/s
T1	Loop Filter Pole	2.0333×10^{-5}	s
T2	Loop Filter Zero	2.2112×10^{-4}	s
T3	Loop Filter Zero	1.2200×10^{-5}	s
A0	Total Capacitance	92.6372	nF
A1	First order loop filter coefficient	3.0138×10^{-3}	nF·s
A2	Second Order loop filter coefficient	2.2980×10^{-8}	$nF \cdot s^2$

Solve For Components

$$C1 = \frac{A2}{T2^2} \cdot \left(1 + \sqrt{1 + \frac{T2}{A2} \cdot (T2 \cdot A0 - A1)}\right) \quad \textit{(39.42)}$$

$$C3 = \frac{-T2^2 \cdot C1^2 + T2 \cdot A1 \cdot C1 - A2 \cdot A0}{T2^2 \cdot C1 - A2} \quad \textit{(39.43)}$$

$$C2 = A0 - C1 - C3 \quad \textbf{(39.44)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(39.45)}$$

$$R3 = \frac{A2}{C1 \cdot C3 \cdot T2} \quad \textbf{(39.46)}$$

Results

Symbol	Description	Value	Units
C1	Loop Filter Capacitor	6.5817	nF
C2	Loop Filter Capacitor	85.5896	nF
C3	Loop Filter Capacitor	0.4660	nF
R2	Loop Filter Resistor	2.5835	kΩ
R3	Loop Filter Resistor	33.8818	kΩ

Chapter 40 Equations for a Passive Fourth Order Loop Filter

Introduction

The fourth order loop becomes worthwhile to consider when the spur or PLL noise energy to be filtered is at an offset of about twenty times the loop bandwidth or greater. In the case of a delta sigma PLL of order three or higher, a fourth order loop filter is often beneficial to reduce the delta sigma modulator that peaks around half of the phase detector frequency.

More added complexity comes with the 4^{th} order loop filter design, especially in terms of the equations for calculating the component values from the loop filter coefficients. One oddity that comes is that it is actually possible to design a stable fourth order loop filter that has all real components, yet has complex poles. Although this may prove advantageous in some pathological situations, this chapter assumes all poles in the filter are real.

The fourth order passive filter has seven component values, but only 5 loop parameters (bandwidth, phase margin, gamma, T3/T1, and T4/T3); this leaves two components to be freely chosen. Ideally, one wants to choose them to maximize the component C4, but the exact equations are complicated and these values need to be carefully chosen to ensure it does not lead to negative component values. The basic strategy presented in this chapter is to design a third order loop filter in order to determine a good choice for the components C1 and R3 and then find the other components in the filter. Although this solution does not yield the maximum possible value for ***C4***, it comes fairly close.

Calculating the Loop Filter Impedance and Time Constants

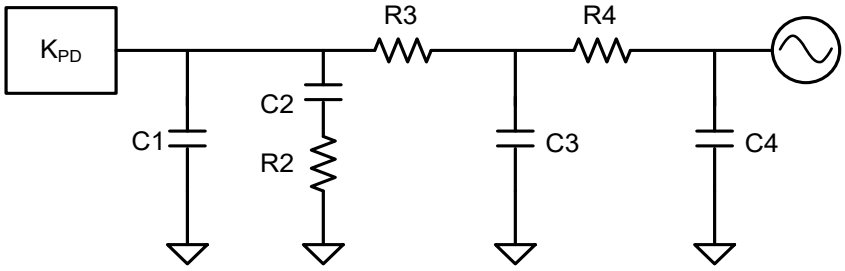


Figure 40.1 *Fourth Order Passive Loop Filter*

For the loop filter shown in Figure 40.1, the impedance is given below:

$$Z(s) = \frac{1 + s \cdot T2}{s \cdot A0 \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + sT4)} \qquad \textbf{(40.1)}$$

Loop Filter Calculation

Calculation of Time Constants

The phase margin is given by:

$$\phi = tan^{-1}(\omega c \cdot T2) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T3) - tan^{-1}(\omega c \cdot T4) \quad \textbf{(40.2)}$$

$$\phi = tan^{-1}\left(\frac{\gamma}{\omega c \cdot T1 \cdot (1 + T31 + T43 \cdot T31)}\right) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T3) - tan^{-1}(\omega c \cdot T4) \quad \textbf{(40.3)}$$

Now ***T1*** is the only unknown in the equation above, and this can be solved for numerically for ***T1***, and afterwards, ***T2***, ***T3***, and ***T4*** can easily be found.

$$T3 = T1 \cdot T31 \quad \textbf{(40.4)}$$

$$T4 = T3 \cdot T43 \quad \textbf{(40.5)}$$

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1 + T3 + T4)} \quad \textbf{(40.6)}$$

Solution of Component Values from Time Constants

Calculation of Filter Impedance Coefficients

The loop filter coefficients can be calculated as follows:

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2) \cdot (1 + \omega c^2 \cdot T4^2)}} \quad \textbf{(40.7)}$$

$$A1 = A1 \cdot T1 \cdot T3 \cdot T4 \quad \textbf{(40.8)}$$

$$A2 = A0 \cdot (T1 \cdot T3 + T1 \cdot T4 + T3 \cdot T4) \quad \textbf{(40.9)}$$

$$A3 = A0 \cdot T1 \cdot T3 \cdot T4 \quad \textbf{(40.10)}$$

Relation of Filter Impedance Coefficients to Component Values

Relating the filter impedance coefficients and zero, ***T2***, to the component values yields a system of five equations and seven unknowns. The unknowns are the components ***C1***, ***C2***, ***C3***, ***C4***, ***R2***, ***R3***, and ***R4***.

$$T2 = R2 \cdot C2 \tag{40.11}$$

$$A3 = R2 \cdot R3 \cdot R4 \cdot C1 \cdot C2 \cdot C3 \cdot C4 \tag{40.12}$$

$$\begin{gathered} A2 = R2 \cdot R3 \cdot C1 \cdot C2 \cdot (C3 + C4) \\ +R4 \cdot C4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2 + C2 \cdot C3 \cdot R2) \end{gathered} \tag{40.13}$$

$$\begin{gathered} A1 = R2 \cdot C2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) \\ +R4 \cdot C4 \cdot (C1 + C2 + C3) \end{gathered} \tag{40.14}$$

$$A0 = C1 + C2 + C3 + C4 \tag{40.15}$$

Since there are seven unknowns and only five constraining equations, two parameters are free to be chosen. There are several considerations in choosing these two parameters. One consideration is that it would be nice if it was possible to solve the system of equations that results from this choice without resorting to numerical methods. A second consideration is that once two components are chosen, they must be chosen in such a way the remaining components turn out to be positive real values. A final consideration is that it would be nice to be able to choose these components such that the capacitor ***C4*** is maximized, or at least reasonably close to being maximized. All of these above three issues have been explored in depth, although the reader will be spared most of this. It is actually possible to solve these equations exactly and find the one that maximizes the capacitor ***C4***. The problem with this is that often yields negative component values and it is also very complicated.

The favored method is to choose ***C1*** and ***R3*** in a strategic way. This method leads to equations are possible to solve without resorting to numerical methods and that lead to positive real component values for all cases that have been tried. This method is far less work and much more robust compared to the method that yields the maximum possible value for ***C4***. Furthermore, the resulting value for ***C4*** turns out to be very close.

Choosing the Components C1 and R3

This method involves choosing ***C1*** and ***R3*** from the third order loop filter design, and then using these values to find the other components for the fourth order filter. For this solution, it is important to strictly order the poles such that ***T1***>***T3***>***T4***. The method starts with keeping filter coefficient ***A0*** as it would be for the fourth order filter, but modifying the filter coefficients ***A1*** and ***A2*** to be as they would be for ***T4*** be set to zero with the other time constants kept the same. In the following equations, $a1_{T3}$ and $a2_{T3}$ are intentionally not capitalized because they are intermediate calculations, not the true filter coefficients.

$$A0 = C1 + C2 + C3 + C4 \tag{40.16}$$

$$A1_{T3} = A0 \cdot (T1 + T3) \tag{40.17}$$

$$A2_{T3} = A0 \cdot T1 \cdot T3 \tag{40.18}$$

Based on these values, intermediate C1, C3, an R3 can be calculated with the formulae used for the third order passive filter. These values are intentionally not capitalized and have subscripts to indicate that they are intermediate calculations, not final values.

$$c1_{T3} = \frac{a2_{T3}}{T2^2} \cdot \left(1 + \sqrt{1 + \frac{T2}{a2_{T3}} \cdot (T2 \cdot A0 - a1_{T3})}\right) \tag{40.19}$$

$$c3_{T3} = \frac{-T2^2 \cdot {c1_{T3}}^2 + T2 \cdot a1_{T3} \cdot c1_{T3} - a2_{T3} \cdot A0}{T2^2 \cdot c1_{T3} - a2_{T3}} \tag{40.20}$$

$$r3_{T3} = \frac{a2_{T3}}{c1_{T3} \cdot c3_{T3} \cdot T2} \tag{40.21}$$

It turns out that if one uses these values of $c1_{T3}$ and $r3_{T3}$ as the actual component values for ***C1*** and ***R3***, then ***C4*** will be zero and ***R4*** will be infinite, and the product of ***C4*** and ***R4*** will be the pole ***T4***. Although these are not the correct values for ***C1*** and ***R3***, they are limits for choosing these values.

If ***C1*** is chosen slightly less than $c1_{T3}$, then real solutions will result. But this begs the question of how much slightly less is. If ***C1*** is chosen too small, then it turns out that ***C4*** becomes zero, ***R4*** becomes infinite, and their product becomes the pole ***T3***.

Using the above calculations as one limit, all that is necessary is to do the same calculations, except replacing the pole ***T3*** with the pole ***T4***.

$$a1_{T4} = A0 \cdot (T1 + T4) \tag{40.22}$$

$$a2_{T4} = A0 \cdot T1 \cdot T4 \tag{40.23}$$

$$c1_{T4} = \frac{a2_{T4}}{T2^2} \cdot \left(1 + \sqrt{1 + \frac{T2}{a2_{T4}} \cdot (T2 \cdot A0 - a1_{T4})}\right) \tag{40.24}$$

$$c3_{T4} = \frac{-T2^2 \cdot {c1_{T4}}^2 + T2 \cdot a1_{T4} \cdot c1_{T4} - a2_{T4} \cdot A0}{T2^2 \cdot c1_{T4} - a2_{T4}} \tag{40.25}$$

$$r3_{T4} = \frac{a2_{T4}}{c1_{T4} \cdot c3_{T4} \cdot T2} \tag{40.26}$$

Now that the extreme limits are known, a good estimate is to guess somewhere in between. Although it turns out that using a weighted average can sometimes make capacitor ***C4*** slightly larger than a simple average the impact of doing this is very small and design specific and not worth the effort. Therefore, a simple average can be used.

$$C3 = \frac{C3_{T3} + C3_{T4}}{2} \tag{40.27}$$

$$R3 = \frac{R3_{T3} + R3_{T4}}{2} \tag{40.28}$$

Determination of C2

Now that C1 and R3 are known, the equations simplified can be rewritten in this form:

$$\frac{A3}{T2 \cdot C1 \cdot R3} = C3 \cdot C4 \cdot R4 \quad \textbf{(40.29)}$$

$$\frac{A2}{A3} - \frac{1}{T2} - \frac{1}{C1 \cdot R3} = \frac{1}{C4 \cdot R4} + \frac{1}{C3 \cdot R4} + \frac{1}{C1 \cdot R2} + \frac{1}{C3 \cdot R3} \quad \textbf{(40.30)}$$

$$A1 - T2 \cdot A0 - \frac{A3}{T2 \cdot C1 \cdot R3} = -T2 \cdot C2 + R3 \cdot (C1 + C2) \cdot (C3 + C4) + C4 \cdot R4 \cdot (C1 + C2) \quad \textbf{(40.31)}$$

$$A0 - C1 = C2 + C3 + C4 \quad \textbf{(40.32)}$$

Rearranging these equation yields the following result.

$$k0 = C2 \cdot \left(\frac{1}{T2 \cdot C1} - \frac{T2 \cdot C1 \cdot R3}{A3}\right) + \frac{1}{C1 \cdot R3} \quad \textbf{(40.33)}$$

$$k1 = -T2 \cdot C2 + C2 \cdot [R3 \cdot (A0 - C1)] + \frac{1}{C3 \cdot R3} \cdot (C1 + C2) \cdot \left(\frac{A3}{T2 \cdot C1 \cdot R3}\right) \quad \textbf{(40.34)}$$

This is based on introducing the following intermediate constants.

$$k0 = \frac{A2}{A3} - \frac{1}{T2} - \frac{1}{C1 \cdot R3} - \frac{(A0 - C1) \cdot T2 \cdot R3 \cdot C1}{A3} \quad \textbf{(40.35)}$$

$$k1 = A1 - T2 \cdot A0 + \frac{A3}{T2 \cdot C1 \cdot R3} - (A0 - C1) \cdot R3 \cdot C1 \quad \textbf{(40.36)}$$

By combining the previous equations to eliminate $\frac{1}{C3 \cdot R3}$, ***C2*** can be found by solving the following quadratic equation that results:

$$a \cdot C2^2 + b \cdot C2 + c = 0 \quad \textbf{(40.37)}$$

$$a = \frac{A3}{(T2 \cdot C1)^2} \quad \textbf{(40.38)}$$

$$b = T2 + R3 \cdot (C1 - A0) + \frac{A3}{T2 \cdot C1} \cdot \left(\frac{1}{T2} - k0\right) \quad \textbf{(40.39)}$$

$$c = k1 - \frac{k0 \cdot A3}{T2} \quad \textbf{(40.40)}$$

Now that these constants have been defined, the value of C2 can finally be derived with the quadratic formula. Note that the positive root is the only valid one that makes C2 positive.

$$C2 = \frac{-b + \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a} \quad \textbf{(40.41)}$$

Solution for Other Components

Once ***C2*** is known, the other components can easily be found.

$$C3 = \frac{T2 \cdot A3 \cdot C1}{R3 \cdot [k0 \cdot T2 \cdot A3 \cdot C1 - C2 \cdot (A3 - R3 \cdot (T2 \cdot C1)^2)]} \quad \textbf{(40.42)}$$

$$C4 = A0 - C1 - C2 - C3 \quad \textbf{(40.43)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(40.44)}$$

$$R4 = \frac{A3}{T2 \cdot C1 \cdot C3 \cdot C4 \cdot R3} \quad \textbf{(40.45)}$$

Conclusion

This chapter has discussed the design of a fourth order passive filter. A lot of the complexity comes in from solving for the component values, once the filter coefficients are known. Unlike the third order solution, there is no proof that the component values yielded are always positive, nor is there a proof that the capacitor next to the VCO is the largest possible, in fact, it is not. However, all cases tested provided positive real component values provided that the restriction is followed:

$$T31 + T43 \leq 1 \qquad \textbf{\textit{(40.46)}}$$

In addition to this, the solution method presented in this chapter was compared against the solution that does yield the maximum value for the capacitor, ***C4***, and the values were close. The reason that the other method was not presented is that it is much more complicated and it has problems converging to real component values in all cases. In the cases tested that it does converge to a solution with real component values, the value for the capacitor, ***C4***, was only marginally larger.

Appendix A: A Fourth Order Loop Filter Design

Design Specifications

Symbol	Description	Value	Units
BW	Loop Bandwidth	10	kHz
ϕ	Phase Margin	47.8	degrees
γ	Gamma Optimization Parameter	1.115	none
K_{PD}	Charge Pump Gain	4	mA
K_{VCO}	VCO Gain	20	MHz/V
f_{VCO}	Output Frequency	900	MHz
f_{PD}	Phase detector frequency	200	kHz
$T31$	Ratio of pole ***T3*** to Pole ***T1***	0.4	none
$T43$	Ratio of pole ***T4*** to Pole ***T1***	0.4	none

Calculate Poles and Zero

$$N = \frac{f_{VCO}}{f_{PD}} \tag{40.47}$$

$$\omega c = 2\pi \cdot BW \tag{40.48}$$

T1 *is the only unknown. Use the Exact Method to Solve for* ***T1*** *Using Numerical Methods*

$$\phi = tan^{-1}\left(\frac{\gamma}{\omega c \cdot T1 \cdot (1 + T31 + T43 \cdot T31)}\right) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T3) - tan^{-1}(\omega c \cdot T4) \tag{40.49}$$

$$T3 = T1 \cdot T31 \tag{40.50}$$

$$T4 = T3 \cdot T43 \tag{40.51}$$

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1 + T3 + T4)} \tag{40.52}$$

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2) \cdot (1 + \omega c^2 \cdot T4^2)}} \quad \textbf{(40.53)}$$

Symbol	Description	Value	Units
N	N Counter Value	4500	none
ωc	Loop Bandwidth	6.2832×10^{4}	rad/s
T1	Loop Filter Pole	4.0685×10^{-6}	s
T2	Loop Filter Zero	4.4500×10^{-5}	s
T3	Loop Filter Pole	1.6274×10^{-6}	s
T4	Loop Filter Pole	6.5096×10^{-7}	s
A0	Total Capacitance	12.8773	nF

Solve For Components *C1* and *R3*

First solve using the pole T3

$$a1_{T3} = A0 \cdot (T1 + T3) \quad \textbf{(40.54)}$$

$$a2_{T3} = A0 \cdot T1 \cdot T3 \quad \textbf{(40.55)}$$

$$c1_{T3} = \frac{a2_{T3}}{T2^2}\left(1 + \sqrt{1 + \frac{T2}{a2_{T3}} \cdot (T2 \cdot A0 - a1_{T3})}\right) \quad \textbf{(40.56)}$$

$$c3_{T3} = \frac{-T2^2 \cdot {c1_{T3}}^2 + T2 \cdot a1_{T3} \cdot c1_{T3} - a2_{T3} \cdot A0}{T2^2 \cdot c1_{T3} - a2_{T3}} \quad \textbf{(40.57)}$$

$$r3_{T3} = \frac{a2_{T3}}{c1_{T3} \cdot c3_{T3} \cdot T2} \quad \textbf{(40.58)}$$

Symbol	Description	Value	Units
$a1_{T3}$	Intermediate First order loop filter coefficient	7.3348 x 10^{-5}	nF·s
$a2_{T3}$	Intermediate Second order loop filter coefficient	8.5262 x 10^{-11}	nF·s^2
$c1_{T3}$	Intermediate Loop Filter Capacitor	0.7397	nF
$c3_{T3}$	Intermediate Loop Filter Capacitor	0.1688	nF
$r3_{T3}$	Intermediate Loop Filter Resistor	15.3409	kΩ

Now solve using the Pole T4

$$a1_{T4} = A0 \cdot (T1 + T4) \quad \textbf{(40.59)}$$

$$a2_{T4} = A0 \cdot T1 \cdot T4 \quad \textbf{(40.60)}$$

$$c1_{T4} = \frac{a2_{T4}}{T2^2}\left(1 + \sqrt{1 + \frac{T2}{a2_{T4}} \cdot (T2 \cdot A0 - a1_{T4})}\right) \quad \textbf{(40.61)}$$

$$c3_{T4} = \frac{-T2^2 \cdot {c1_{T4}}^2 + T2 \cdot a1_{T4} \cdot c1_{T4} - a2_{T4} \cdot A0}{T2^2 \cdot c1_{T4} - a2_{T4}} \quad \textbf{(40.62)}$$

$$r3_{T4} = \frac{a2_{T4}}{c1_{T4} \cdot c3_{T4} \cdot T2} \quad \textbf{(40.63)}$$

Symbol	Description	Value	Units
$a1_{T4}$	Intermediate First order loop filter coefficient	6.0774 x 10^{-5}	nF·s
$a2_{T4}$	Intermediate Second order loop filter coefficient	3.4105 x 10^{-11}	nF·s^2
$c1_{T4}$	Intermediate Loop Filter Capacitor	0.4628	nF
$c3_{T4}$	Intermediate Loop Filter Capacitor	0.4401	nF
$r3_{T4}$	Intermediate Loop Filter Resistor	3.7628	kΩ

Now find the Actual Values for C1 and R3

$$C3 = \frac{C3_{T3} + C3_{T4}}{2} \tag{40.64}$$

$$R3 = \frac{R3_{T3} + R3_{T4}}{2} \tag{40.65}$$

Symbol	Description	Value	Units
C1	Loop Filter Capacitor	0.6013	nF
R3	Loop Filter Resistor	9.5519	kΩ

Solve for C2

$$A3 = R2 \cdot R3 \cdot R4 \cdot C1 \cdot C2 \cdot C3 \cdot C4 \tag{40.66}$$

$$\begin{gathered} A2 = R2 \cdot R3 \cdot C1 \cdot C2 \cdot (C3 + C4) \\ +R4 \cdot C4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2 + C2 \cdot C3 \cdot R2) \end{gathered} \tag{40.67}$$

$$\begin{gathered} A1 = R2 \cdot C2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) \\ +R4 \cdot C4 \cdot (C1 + C2 + C3) \end{gathered} \tag{40.68}$$

$$k0 = \frac{A2}{A3} - \frac{1}{T2} - \frac{1}{C1 \cdot R3} - \frac{(A0 - C1) \cdot T2 \cdot R3 \cdot C1}{A3} \tag{40.69}$$

$$k1 = A1 - T2 \cdot A0 + \frac{A3}{T2 \cdot C1 \cdot R3} - (A0 - C1) \cdot R3 \cdot C1 \tag{40.70}$$

$$a = \frac{A3}{(T2 \cdot C1)^2} \tag{40.71}$$

$$b = T2 + R3 \cdot (C1 - A0) + \frac{A3}{T2 \cdot C1} \cdot \left(\frac{1}{T2} - k0\right) \tag{40.72}$$

$$c = k1 - \frac{k0 \cdot A3}{T2} \tag{40.73}$$

$$C2 = \frac{-b + \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a} \tag{40.74}$$

Symbol	Description	Value	Units
A1	First order loop filter coefficient	8.1731×10^{-5}	nF·s
A2	Second Order loop filter coefficient	1.3301×10^{-10}	$nF \cdot s^2$
A3	Third Order loop filter coefficient	5.5502×10^{-17}	$nF \cdot s^3$
k0	Intermediate Calculation for finding ***C2***	-5.4328×10^{7}	1/s
k1	Intermediate Calculation for finding ***C2***	-5.6202×10^{-4}	nF·s
a	Intermediate Calculation for finding ***C2***	7.7528×10^{-8}	s/nF
b	Intermediate Calculation for finding ***C2***	3.9983×10^{-5}	s
c	Intermediate Calculation for finding ***C2***	-4.9426×10^{-4}	nF·s
C2	Loop Filter Capacitor	12.0790	nF

Solve for the Other Components

Once ***C2*** is known, the other components can easily be found.

$$C3 = \frac{T2 \cdot A3 \cdot C1}{R3 \cdot [k0 \cdot T2 \cdot A3 \cdot C1 - C2 \cdot (A3 - R3 \cdot (T2 \cdot C1)^2)]} \quad \textbf{(40.75)}$$

$$C4 = A0 - C1 - C2 - C3 \quad \textbf{(40.76)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(40.77)}$$

$$R4 = \frac{A3}{T2 \cdot C1 \cdot C3 \cdot C4 \cdot R3} \quad \textbf{(40.78)}$$

Symbol	Description	Value	Units
C3	Loop Filter Capacitor	0.1245	nF
C4	Loop Filter Capacitor	0.0726	nF
R2	Loop Filter Resistor	3.6840	kΩ
R4	Loop Filter Resistor	24.0453	kΩ

Chapter 41 Fundamentals of PLL Active Loop Filter Design

Introduction

For reasons of cost and noise, the passive filter is often the preferred approach as it can be done with resistors and capacitors and no active devices.

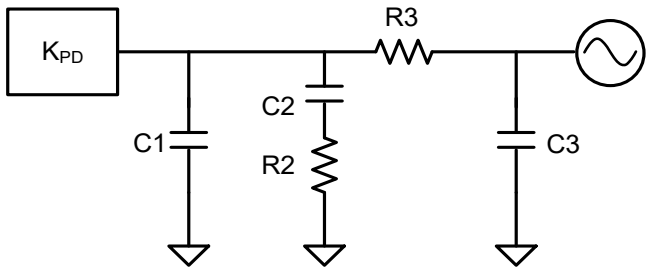


Figure 41.1 *Passive Filter*

That being said, there are some situations where it does make sense to add an op-amp to create an active filter. The most common reason for this is that the charge pump cannot supply the full voltage range required by the VCO. Other less common reasons to use an active filter might to be to isolate the VCO input capacitance, monitor the tuning voltage, or isolate the loop filter from excessive VCO leakage.

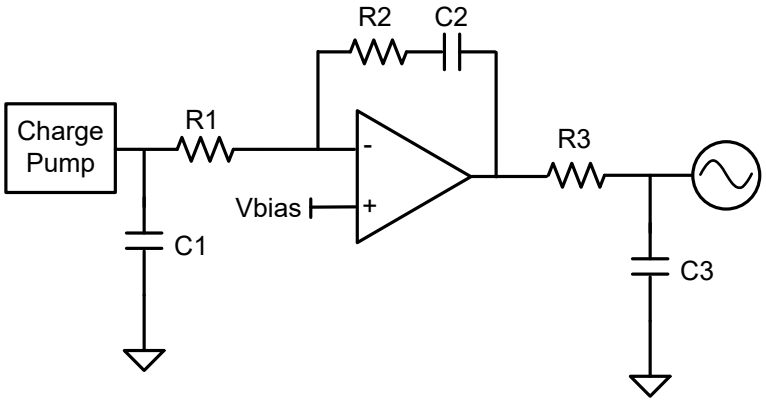


Figure 41.2 *Active and Passive Loop Filter Example*

The selection of the op-amp is typically made based on certain desirable characteristics that impact the performance. Once these characteristics are understood and the op amp is chosen, the next step is to design the loop filter. After this, the design can be simulated and compared to the actual measurement. As there is some art to the op amp performance, it is highly encouraged to compare these simulations to actual performance as there are many characteristics of op-amps that are hard to model in the loop filter. This chapter goes through the op amp characteristics and selection criteria, then discusses filter design, and finally does some simulations and comparisons to actual measurements.

Op-Amp Characteristics and Selection

Real world op amps have several characteristics that can impact performance and influence the selection of the op amp. Among these characteristics are voltage rails, minimum stable gain, noise performance, bandwidth, bias currents, and slew rate. This section discusses each of these characteristics and how they impact the op amp selection.

Voltage Rails

Op amps have both input and output rails that restrict how close the input and output can be to the power supply. If the input of the op amp cannot accept the voltage that the charge pump is biased to, *Vbias*, then it cannot be used unless this Vbias voltage is shifted, which might lead to a compromise in performance. Typically, the headroom from the negative input supply rail is more likely to be an issue than the one from the positive one and the PLL charge pump supply is typically less than the op amp voltage supply. In terms of the output supply headroom, this just needs to be able to supply whatever voltage range is required for the VCO to operate. These statements can be summarized in the table below.

	Symbol	Description	Restrictions
PLL	*CPoutMin*	Minimum possible charge pump voltage, typically 0.5 V.	It is assumed that the PLL is chosen and these are fixed.
	CPoutMax	Maximum charge pump output voltage, which is typically 0.5 V less than charge pump supply, but consult the datasheet.	
	Vbias	Charge pump voltage that gives optimal performance and is typically ½ of the charge pump supply voltage.	
AMP	*AMPinMin*	Minimum possible input voltage, assuming that the negative supply is grounded.	AMPinMin ≤ Vbias
	AMPinMax	Maximum allowable input voltage, which is the op amp supply minus the positive input rail.	AMPinMax ≥ Vbias
	AMPoutMin	Minimum possible output voltage of the op amp, which is equal to the negative output rail, assuming that the negative supply is grounded.	AMPoutMin≤ VCOinMin
	AMPoutMax	Maximum possible output voltage of the op amp and is equal to the op amp supply minus the positive output rail.	AMPoutMax ≥ VCOinMax
VCO	*VCOinMin*	Minimum required tuning voltage of the VCO, which is the voltage corresponding to the lowest frequency needed from the VCO, accounting for margin. This assumes a positive VCO tuning characteristic.	It is assumed that the VCO is chosen and these are fixed
	VCOinMax	Maximum required tuning voltage of the VCO, which is the voltage corresponding to the highest frequency needed from the VCO, accounting for margin. This assumes a positive VCO tuning characteristic.	

Table 41.1 *Op Amp Supply Headroom Requirements*

Minimum Stable Gain

An op-amp is said to be *unity gain stable* if it can operate with a gain of one. If it is not, then the *minimum stable gain* is the lowest gain where it can operate. As a general rule of thumb, having gain in an active filter is undesirable as it multiplies the voltage noise of the op amp. If gain is required for the op-amp, then it would ideally have very low voltage noise to compensate for this.

Noise Current and Noise Voltage

The noise of the op amp can be modeled as a noise source and a current source at the input. This noise goes to the input of the VCO and creates phase noise. Typically the impact of voltage noise is most seen at the loop bandwidth because it gets attenuated significantly at lower offsets by the VCO transfer function and decreases as 20 dB/decade with offset. Current noise typically has much less impact and can often be disregarded, but the impact is mainly at lower offsets, if at all.

In order to determine if the op-amp noise is appropriate, full simulations are best, but a simplified analysis can be done based on normalizing the noise sources and introducing some simplifying assumptions. The simplified approach is to focus on the impact of the noise voltage near the loop bandwidth of the PLL and also account for any multiplication. The loop filter will be designed to minimize the multiplication, so this factor will the minimum stable gain of the op amp, or one if the op amp is unity gain stable. The op amp voltage noise will create FM modulation on the VCO tuning line at the loop bandwidth frequency, and this at the loop bandwidth frequency gets multiplied by the VCO gain and generates the following noise power.

$$PN_{AMP} \approx 20 \cdot log\left(\frac{AmpGain \cdot Vn \cdot K_{VCO}}{\sqrt{2} \cdot BW}\right) \qquad \textbf{(41.1)}$$

In this equation, *AmpGain* is equal to one, except for the active C filter, where it can be greater. For example, consider an op amp with 1 nV/√Hz noise and 100 kHz bandwidth. Also suppose that VCO gain was 200 MHz/V and AmpGain was unity. In this case, the phase noise due to just the op amp would be -117 dBc/Hz. This formula can also be worked backwards by assuming a tolerable phase noise for PN_{AMP} and working this backward to see what op amp noise voltage this implies. In either case, the following figure summarizes the result.

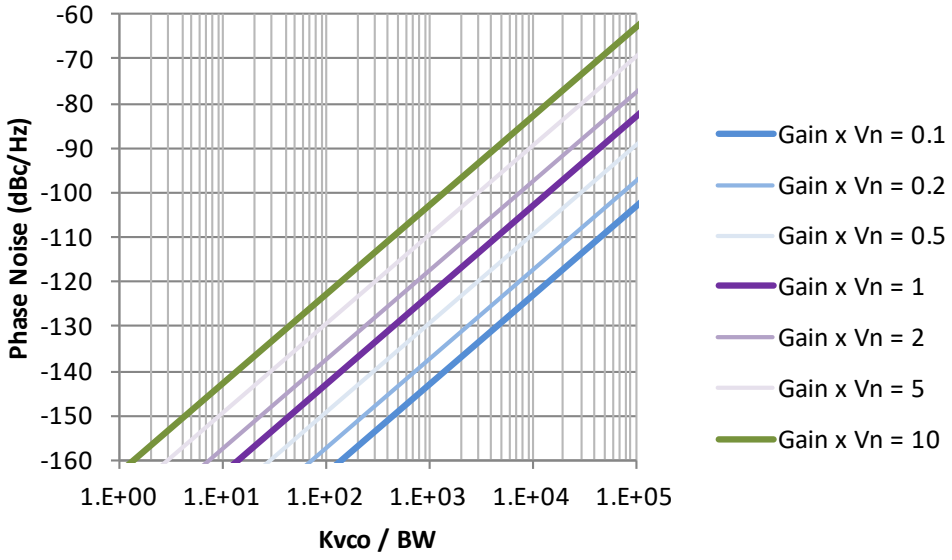


Figure 41.3 *Phase Noise Generated at Loop Bandwidth by Op Amp*

Bias Current Considerations

The inputs to the op amp might claim to be high impedance, but the bias currents may be important to consider if they are not less than the charge pump leakage of the PLL, which typically in the nA range. PLLs with higher phase detector frequencies tend to be much more tolerant of these leakage current, unless it gets in the µA range. Assuming a PLL with BasePulseSpur=-340 dBc, 1 nA charge pump leakage, and 1 mA charge pump gain, the following table gives some rough guidelines for tolerable bias currents.

Phase Detector Frequency	Tolerable Bias Currents
≤100 kHz	0.5 nA
1 MHz	1.6 nA
10 MHz	160 nA
100 MHz	16 µA

Table 41.2 *Tolerable Op Amp Bias Currents*

As another rule of thumb, if the bias currents were to exceed more than about 10% of the charge pump current, then it might also cause stability issues, but this should almost never happen.

Speed Considerations

For speed considerations, one might consider the *slew rate* and bandwidth. This section shows some simple requirements that are easier to understand and then goes through some other effects that might be more difficult to explain, such as the ones related to the speed of the op amp.

Slew rate tends not to be that big of a deal in most situations unless the PLL lock time is extremely fast. As a rule of thumb, the first 20% of the lock time is getting close to the correct frequency and the last 80% is settling this to a finer tolerance. For instance, if 900 MHz corresponds to 1 V and 2000 MHz corresponds to 21 V and the expected lock time is 5 us, then the slew rate would need to be faster than 20 V/us. If it was slower, then it would impact the time the PLL would take to lock, although it would still lock.

Another consideration is the *gain bandwidth product*. This is relatively constant and is the product of the offset frequency and the op amp gain. When the gain drops below 10 dB, then the assumption that the op amp holds both inputs to the same voltage starts to come apart. At offsets sufficiently higher than the PLL loop bandwidth, this distortion will be attenuated and as general of rule to prevent this distortion is.

$$GainBandwidthProduct > 10 \times PLL\ Loop\ Bandwidth \qquad \textbf{(41.2)}$$

If this rule is violated, then one way that this can show up is peaking near the offset frequency that corresponds to zero dB gain. A simplified way to think of this is the op-amp introduces a phase shift, which will cause a peak in the phase noise near the point of unity gain. To illustrate this, the following figure compares various loop filters of the same bandwidth. The active filter was done with the LM6211 op amp that has a gain bandwidth product of 17 MHz, which would mean at this frequency, the op-amp gain would be about 0 dB. Indeed, near this frequency, we see a large peak in the noise in Figure 41.4.

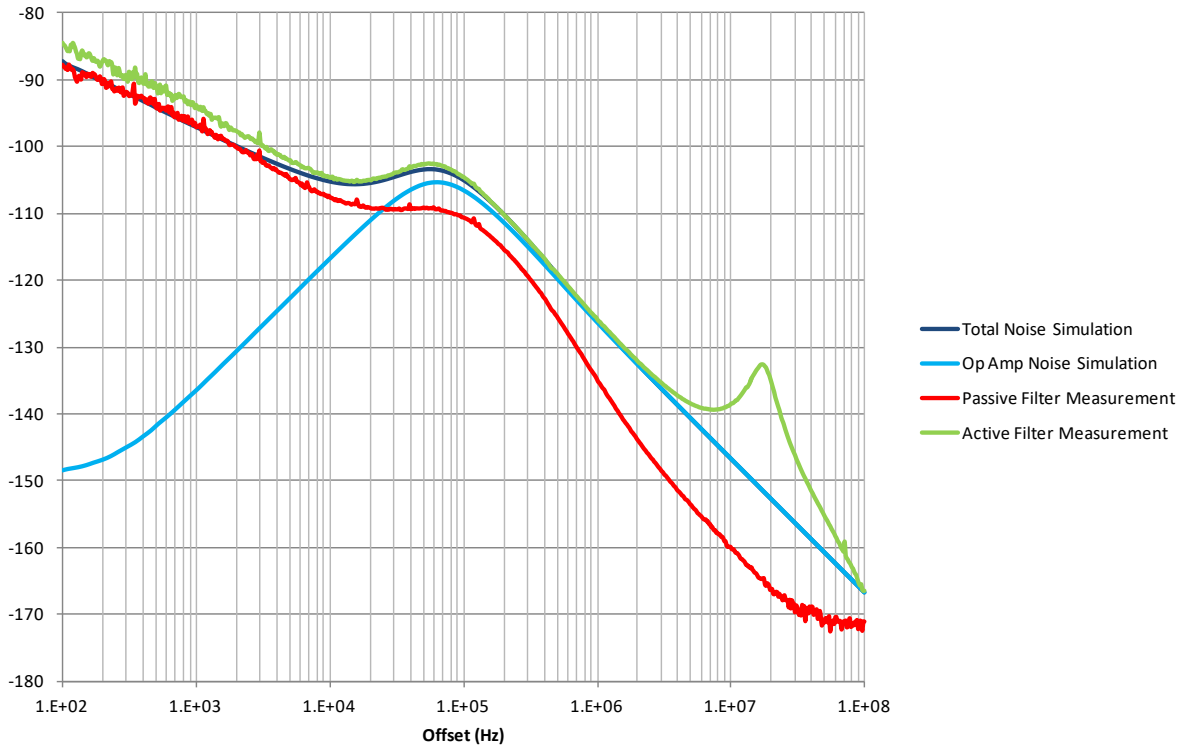


Figure 41.4 *Phase Noise Simulation and Actual Measurement*

Note that in the region of 100 Hz to 10 kHz, we see the phase noise of the active filter, specifically the PLL 1/f noise, degraded about 3 dB relative to the passive filter and the simulation. The most likely reason for this is that the op amp was not fast enough to respond to the fast current pulses from the charge pump. The charge pump output is normally off and only comes on every phase detector cycle to put out fast correction pulses of length T_{ON}. Modern PLLs can have a time of T_{ON} of 460 ps, which is much faster than most op amps. If the op amp is not fast enough, it lengthens the on time of the charge pump. Recall from the PLL phase noise chapter that the PLL 1/f noise relates directly to the on time of the charge pump and this is why there is an increase in the PLL 1/f noise. The PLL flat noise relates to the standard deviation of the on time of the charge pump. This may be also impacted, but this noise is masked out by the op amp noise in Figure 41.4.

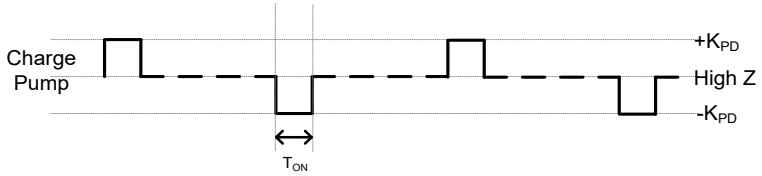


Figure 41.5 *Typical Charge Pump Output*

Other experiments were used to validate this theory. To do this, the minimum charge pump on time T_{ON} was adjusted using the Texas Instruments LMX2492 PLL. Increasing this on time theoretically degrades phase noise very slightly, but it actually improved it with the op amp to an extent as shown in the Figure 41.6.

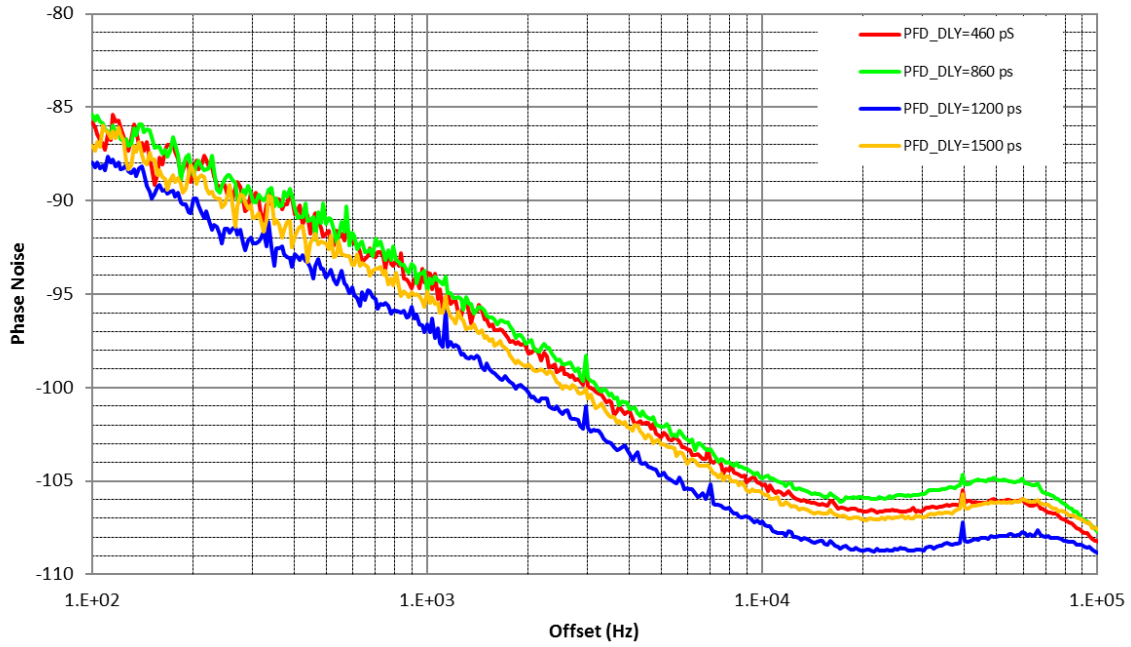


Figure 41.6 *Impact of Charge Pump on Time (PFD_DLY) on PLL Noise*

Another experiment that was done was to put the entire loop filter before the op amp and again this noise improved, so indeed this close in noise is most likely related to the op amp not responding fast enough to the fast charge pump output pulses.

It is strongly emphasized that these examples are not to showcase the performance of the LM6211 op amp or to present an optimized design, but rather agitate the issues to make them easily visible and easier to study; there are techniques that can be utilized to mitigate these effects.

Although typically not much of an issue, one can also consider the impact of the op amp speed on the lock time and transient response of the PLL. The first thing to think about slew rate of the op amp needs to be fast enough to accommodate the rise time of the PLL, which is almost always the case. A little more obscure, but interesting consideration is that the op amp can also suppress cycle slipping. In the following figure, the same loop filter was used for a second order passive vs. a second order active filter.

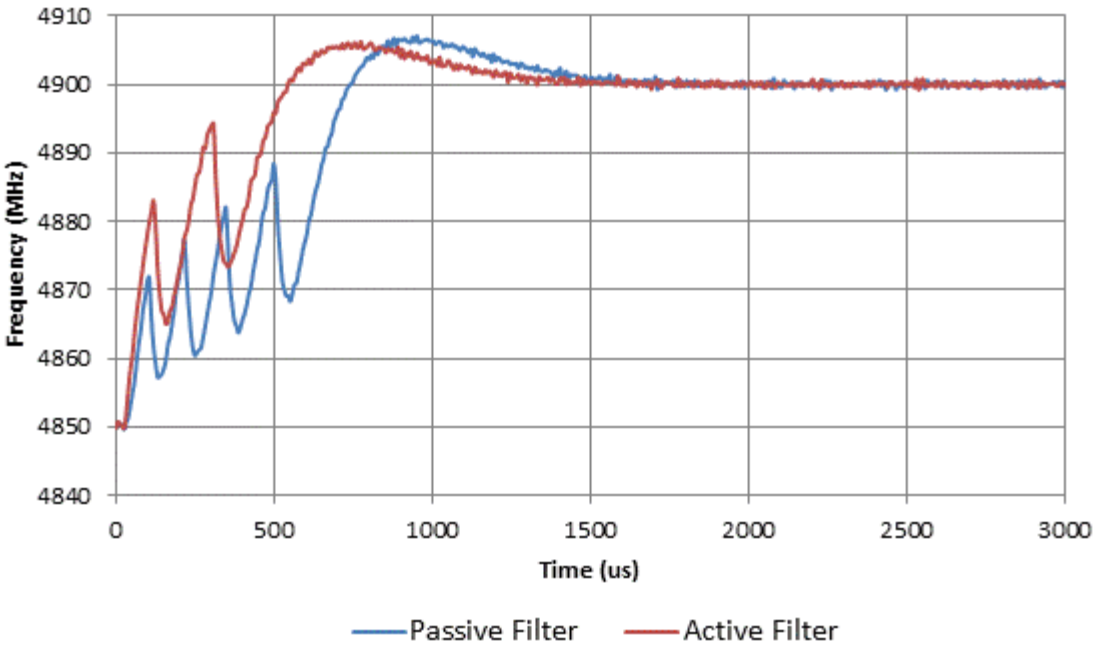


Figure 41.7 *Active and Passive Filter Transient Response Comparison*

Active Filter Types

Active A Filter

The Active A filter is generally recommended for its many advantages. The pole before the op-amp helps reduce some of the speed requirements for the op amp for frequencies above the pole, T1. It also allows the op amp to be biased at the optimal tuning voltage. The noise of the op-amp is gained by 1 + R2/R1, but this is typically only a little greater than one as R1 can be chosen large to minimize this gain. However, if R1 is chosen too large, then the resistor noise becomes a consideration, so there is a trade-off involved that will be discussed later. For this configuration, it is recommended to use a unity gain stable op-amp.

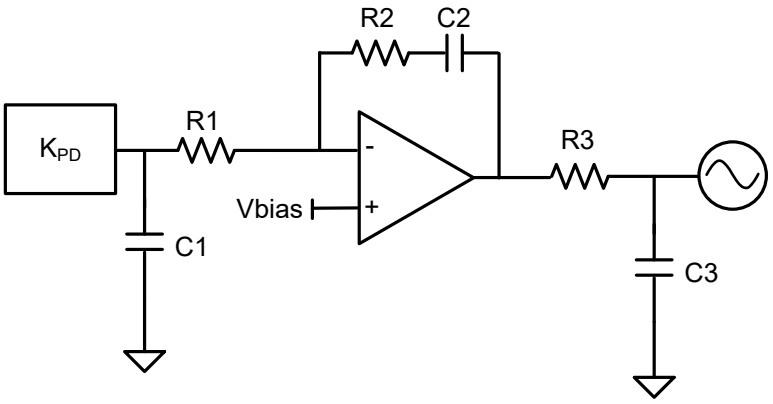


Figure 41.8 *Active A Filter*

One variation of the Active A filter is to not include the pole before the op-amp and put it after the op amp as shown. This is the equivalent as the limiting case at the T3/T1 ratio approaches infinity.

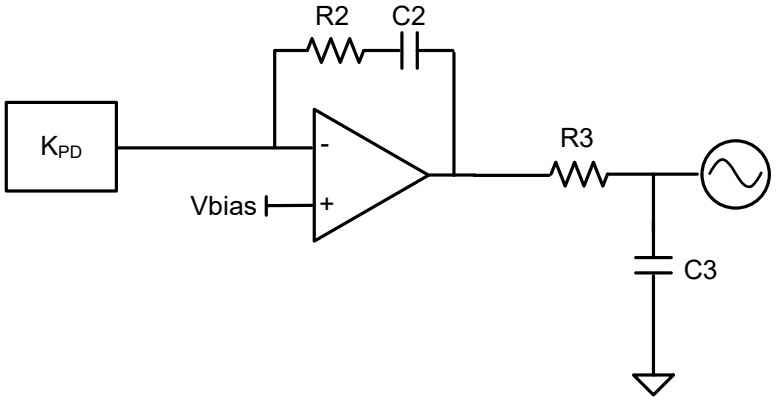


Figure 41.9 *Active A Filter with T3/T1 = ∞*

This configuration puts the most stringent requirements on the op-amp, but has the advantage that the lowest frequency pole can be placed after the op amp. It makes sense in the case where the op amp can handle the fast pulse action of the charge pump, or the pole after the op amp is able to attenuate any undesired issues due to the op amp. With this variation of the Active A filter, the fourth order case is not covered. For this case, consider the Active B filter.

Active B Filter

The Active B filter puts stringent requirements on the op amp and requires it to be unity gain stable. The only advantage of this filter type over the active A would be that the noise is not multiplied up at all and there is no concern about the R1 resistor noise.

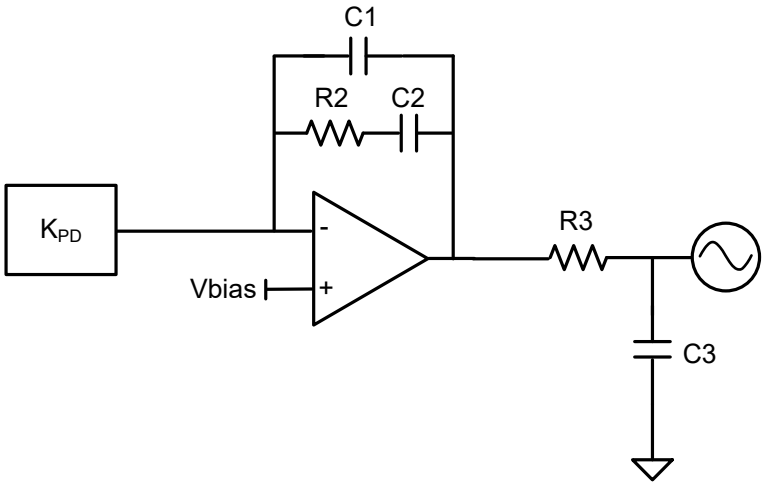


Figure 41.10 *Active B Filter*

The Active B filter is generally not recommended as it wastes the lowest frequency pole, T1, in the feedback path of the op amp. It makes more sense to use an Active A filter and either put the pole before the op amp if it helps to deal with the fast pulsing action of the charge pump, or after the op amp to help attenuate its noise.

Active C Filter

The active C filter is often chosen because it is the most intuitive approach. For instance, if the charge pump can output up to 5 V and 15 V is required, then the gain is chosen to be equal to three. The general equation for the gain is:

$$AmpGain = 1 + Ra/Rb \tag{41.3}$$

It has the advantage of lower speed requirements for the op amp, which could be beneficial to the close in 1/f noise. Also, the op amp does not need to be unity gain stable for this configuration.

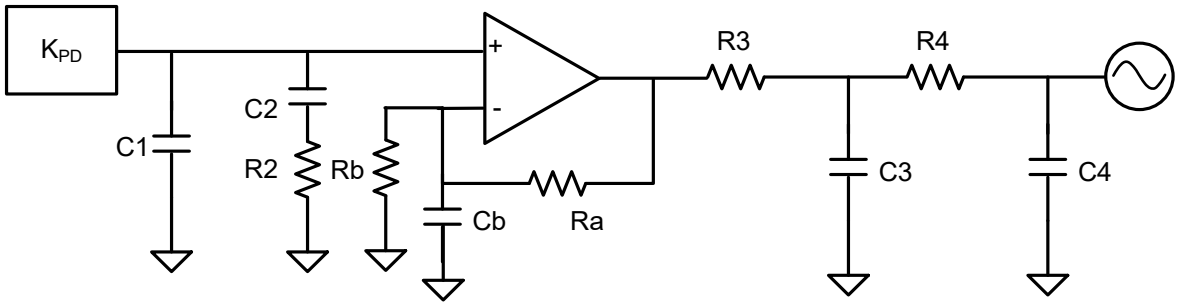


Figure 41.11 *Active C Filter*

Setting Up the Bias Voltage

Both the Active A and Active B need to establish a bias voltage, Vbias. For optimal performance, the best phase noise and spurs are typically at half of the charge pump supply voltage. The most common way of establishing this voltage is to use a simple voltage divider off the charge pump supply voltage. It is a good idea to place a capacitor, *Cb*, because it rolls off the resistor noise and also provides significant filtering of any supply noise.

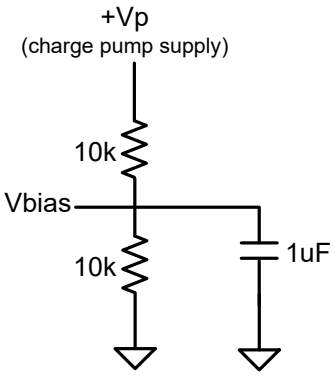


Figure 41.12 *Bias Voltage Setup for Op-Amp*

In terms of calculating the resistor noise, recall the formula:

$$ResistorNoise = \sqrt{4 \cdot K_B \cdot T \cdot R} \tag{41.4}$$

K_B is Boltzmann's constant, which is 1.38066 x 10^{-23} J/K, T is the temperature in Kelvin, which is 300° at room temperature, and R is the resistance. R is the Thevenin equivalent of the resistor, which looks like a 5k resistor and shunt 1 µF capacitor. For the example in Figure 41.12, the calculated resistor noise is 9.1 nV/√Hz. The noise for this combination as well as other values is shown below:

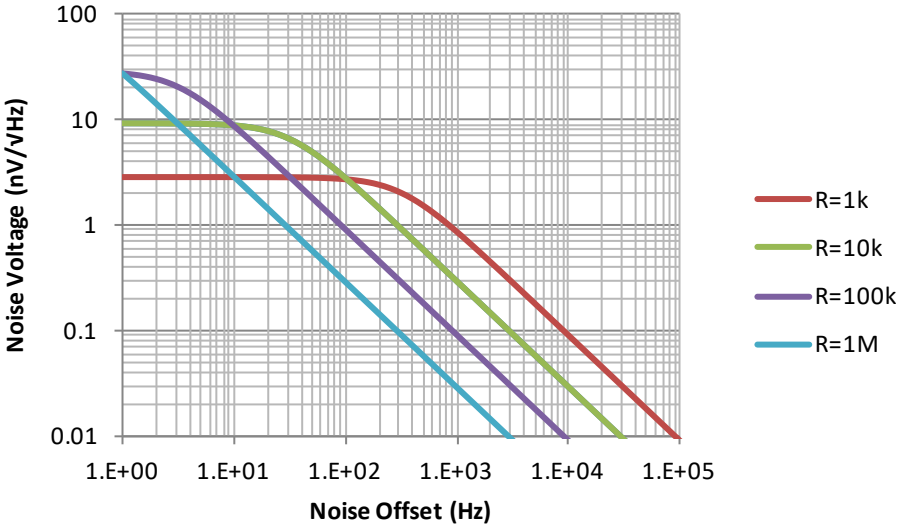


Figure 41.13 *Bias Resistor Noise*

In summary, the bias voltage noise can be made a non-issue with just a 1 µF capacitor. With a larger capacitor, it can be rolled off more, although this is probably not necessary; the noise of the bias network is essentially a non-contributor next to the op amp voltage noise. Realize that at low offsets below 1 kHz, this noise is shaped by the VCO transfer function, which will greatly attenuate this noise. Furthermore the input reference and PLL 1/f noise will contribute here, so it is less likely at lower offsets that this will be a big deal. Based on this graph, 100 kΩ might seem a more sensible bias resistor value, although making this resistance too high makes this bias network susceptible to the bias currents of the op amp.

The Pole Switching Trick

Making the T3/T1 Ratio Greater than 100%

For passive filters the T3/T1 ratio needs to be strictly less than 100%. However, for active filters, this is not a requirement. In fact, it is typically beneficial to put the larger (lower frequency) pole after the op-amp as this can attenuate the op-amp noise and other undesirable effects of the op amp. In the following figure, a third order filter is being used with bigger pole before and after the op amp and the benefit can be seen.

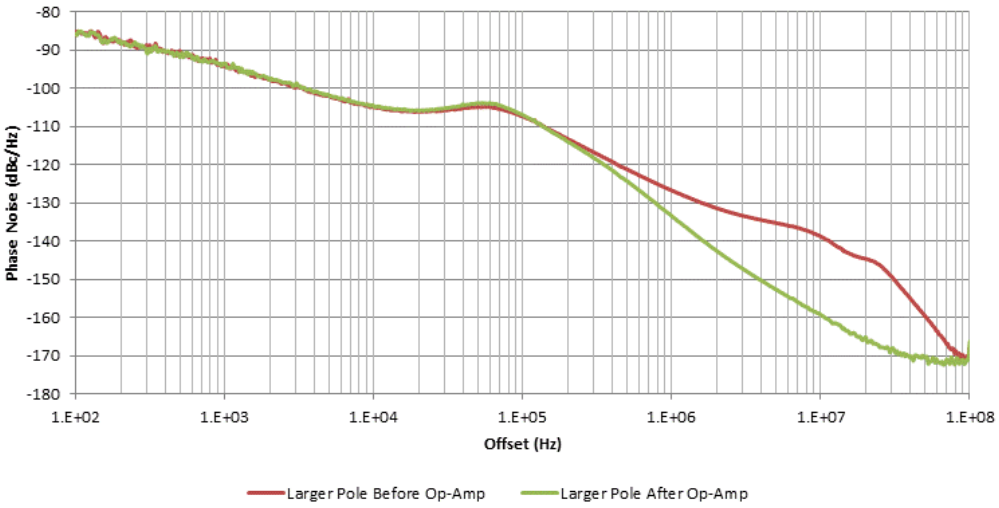


Figure 41.14 *Impact of Switching Poles and Charge Pump on Time*

The big bump in phase noise at 10 MHz in Figure 41.14 is due to insufficient bandwidth of the op-amp and potentially other issues. In any case, regardless of the issues, a larger pole after it can help this effect. If we consider this pole switching effect to an extreme and take T3/T1 →∞, then the maximum attenuation after the op amp can be placed, but it does put more stringent requirements on the op-amp

Designing the Loop Filter

Defining the Loop Equations

Regardless of what filter topology is used, the loop filter impedance is defined as the output voltage to the VCO generated by a current produced from the charge pump. The expression is very similar to the passive expression, except there is a term, A, to represent the gain in the case it is different than one for the case of a type C active filter.

$$Z(s) = \frac{AmpGain}{s \cdot A0} \cdot \frac{1 + s \cdot T2}{(1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)} \quad \textbf{(41.5)}$$

Assuming that the charge pump polarity is inverted, the open loop gain becomes:

$$Z(s)_{/N} = -\frac{AmpGain \cdot K_{PD} \cdot K_{VCO}}{s \cdot N} \cdot \frac{1 + s \cdot T2}{s \cdot A0 \cdot (1 + s \cdot T1) \cdot (1 + s \cdot T3) \cdot (1 + s \cdot T4)} \quad \textbf{(41.6)}$$

	Active A	Active B	Active C
T1	$C1 \cdot R1$	$\frac{C1 \cdot C2 \cdot R2}{C1 + C2}$	
T2	$C2 \cdot R2$		
T3	$\frac{(C3 \cdot R3 + C4 \cdot R3 + C4 \cdot R4) + \sqrt{(C3 \cdot R3 + C4 \cdot R3 + C4 \cdot R4)^2 - 4 \cdot C3 \cdot C4 \cdot R3 \cdot R4}}{2}$		
T4	$\frac{(C3 \cdot R3 + C4 \cdot R3 + C4 \cdot R4) - \sqrt{(C3 \cdot R3 + C4 \cdot R3 + C4 \cdot R4)^2 - 4 \cdot C3 \cdot C4 \cdot R3 \cdot R4}}{2}$		
A0	C1	C1+C2	
AmpGain	-1	-1	$1 + Ra/Rb$

Table 41.3 *Filter Parameters as they relate to the Filter Components*

The time constants can be found in the same manner that they are found for the passive filter, except that the *AmpGain* needs to be accounted for. In all cases but the Active C filter, this can be ignored as the charge pump polarity can be inverted to make this effectively one. For the Active C filter, simply multiply the VCO gain by *AmpGain* and proceed as normal.

Finding the Time Constants for an Active A Filter with T31→∞

Finding of the time constants for active filters is an identical process to that for passive filters with the one case exception of the Active A filter where one takes T31→∞. In this case, use the design with the substitutions T31=0 and T43→T31.

Ordering the Poles

When the poles are solved for, it is arbitrary for the ordering of T1, T3, and T4. However, as a general practice, it is best to put the maximum attenuation after the op amp. So in this case, one would typically want T1 to be the smallest (highest frequency) pole, T3 to be the largest pole, and T4 to be the second largest pole.

Solving for the Components

Once that ***A0*** is found, the other components can be found using the Table 23.4. For a third order loop filter, ***C3*** should be at least four times the VCO input capacitance and at least ***C1/5***. For a fourth order loop filter, ***C4*** should be at least this stated limit above.

	Active A	**Active B**	**Active C**
R1	*Free to choose, but want R1>>R2 for optimal noise while still keeping C1 large enough. Recommended choice:* $R1 = 10 \cdot R2$	n/a	n/a
C1	$C1 = \frac{T1}{R1}$	$A0 \cdot \frac{T1}{T2}$	$A0 \cdot \frac{T1}{T2}$
C2	$A0$	$A0 \cdot \left(1 - \frac{T1}{T2}\right)$	$A0 \cdot \left(1 - \frac{T1}{T2}\right)$
R2	$\frac{T2}{C2}$		
Third Order Filter Components			
C3	*Free to choose. Recommend to choose at least 4x the VCO input capacitance and at least 220 pF. Consider smaller if R3 gets less than about 40 Ω.*		
R3	$\frac{T3}{C3}$		
Fourth Order Filter Components			
C4	*Free to choose. Recommend to choose at least 4x the VCO input capacitance and at least 220 pF. Consider decreasing it if R3 gets less than about 40 Ω.*		
C3	$C4 \cdot \frac{4 \cdot T3 \cdot T4}{(T3 - T4)^2}$		
R3	$C4 \cdot \frac{T3 + T4}{2 \cdot (C3 + C4)}$		
R4	$C4 \cdot \frac{T3 + T4}{2 \cdot C4}$		

Table 41.4 *Loop Filter Component Values Computed from Time Constants*

Using Transistors for the Standard and Alternative Feedback Approaches

For those who are averse to using op-aps, transistors can be used to replace the op-amp in order to reduce the cost and the noise. However, be warned that this is a little of a science experiment as the gain of the loop depends on the tuning voltage. For the approach presented here, the transistors can only sink current, so a pull-up resistor, ***Rpp***, is required. The choice of ***Rpp*** is design and possibly transistor specific, but ***Rpp = 10 KΩ*** is a good starting value. ***Rpp*** sets the gain of the circuit. Choosing this resistor too large will cause the circuit to be unstable and the carrier to dance around the frequency spectrum. Choosing it too small will cause excessive current consumption since ***Vpp*** is grounded through the resistor ***Rpp*** when the transistors turn on. This particular design has been built and tested to 30 volt operation. The optional 20 KΩ resistor may reduce the phase noise. In some cases, this resistor can also be replaced by a capacitor. The 220 Ω resistor sets the bias point for the charge pump output pin. The 1 kΩ resistor limits the sink current.

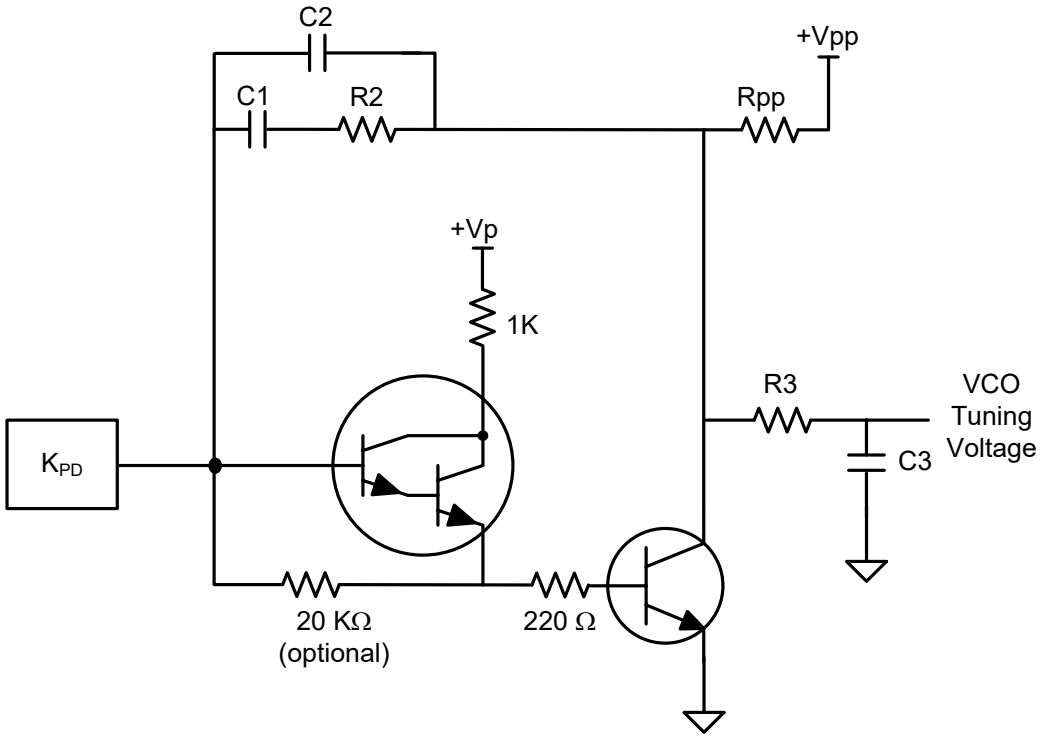


Figure 41.15 *Third Order Active B Filter Using Transistors*

Conclusion

The equations for active loop filter design have been presented. Active filters are necessary when the charge pump cannot operate at high enough voltages to tune the VCO and can also help reduce the ill effects of the VCO input capacitance. There are many aspects of designing with an op-amp and it adds another degree of freedom and complexity. As a general rule of thumb, it might first debug the design using a second order passive filter before bringing in the extra variable of the op amp.

In terms of filter design, there are three types of active filters: Active A, Active B, and Active C. In general, Active A is a good starting point, but maybe Active C makes sense if the op-amp has issues with close in noise due to the charge pump pulsing action. Whatever approach is chosen, it is generally a good practice to put the lowest frequency pole after the op amp to attenuate to attenuate as much of the noise from it as possible.

The choice of the op-amp is somewhat of an art. One has to balance the input and output rails, bias currents, noise voltage, and noise current. The input rail, especially the negative one, needs to be less than the maximum charge pump output voltage in order to avoid the need for a negative supply. If the output rail is too high, the VCO might not be able to tune the entire range. Bias currents contribute to leakage-induced spurs. If a fractional PLL is used, it might be possible to make the phase detector frequency high enough to tolerate these higher bias currents. If an integer PLL is used, then one needs to choose an op-amp with lower bias currents. Low noise voltage and noise current are very important because they contribute to the overall phase noise. Below are some recommendations for op-amps that can be used.

Device	Supply Voltage (V)		Input Rails (V)		Output Rails (V)		Noise Voltage (nV/√Hz)	Minimum Stable Gain (V/V)	Bias Currents (nA)	GBW (MHz)
	Min	*Max*	*Min from V-*	*Max From V+*	*Min from V-*	*Max from V+*				
LME49990	10	36	3	-3	2	-2	0.9	1	500	110
OPA211	4.5	36	1.8	-1.4	0.2	-0.2	1.1	1	175	45
LM6211	5	24	0	-1.7	0.1	-0.1	5.5	1	0.005	17

Table 41.5 *Op Amp Recommendations*

References

[1] I had useful conversations with John Bittner and Eric Eppley regarding active filter design.

[2] I had useful conversations with Hooman Hashemi regarding op-amps and non-ideal behaviors in active loop filters.

[3] Banerjee, Dean Signal Chain Basics (Part 96): Active Loop Filter Designs December 2014

Appendix A: Guidelines for Choosing Component R1 for an Active A Filter

The general strategy for this analysis is to determine what choice of R1 minimizes the noise contribution of the resistor R1 itself and the op-amp voltage noise without making C1 too small. The expression for the R1 resistor noise has already been derived.

$$Vr = \sqrt{\left[(V_{R1})^2 \cdot \left\| \frac{C1}{C2} \cdot \frac{1 + s \cdot R2 \cdot C2}{1 + s \cdot R1 \cdot C1} \right\| \right]^2} \tag{41.7}$$

Note that the voltage noise for R1

$$\sqrt{4 \cdot K_B \cdot T \cdot R1} \tag{41.8}$$

Using this expression for R1 and the definition of the time constants, the noise due to resistor R1 can be simplified with these. Note that this function is a decreasing function of R1, which implies that one should choose R1 as large as possible to minimize the resistor noise at the output of the op-amp.

$$Vr = \frac{4 \cdot K_B \cdot T}{R1} \cdot \left\| \frac{T1}{A0} \cdot \frac{1 + s \cdot T2}{1 + s \cdot T1} \right\| \tag{41.9}$$

Switching to the op-amp voltage noise, recall that it has the following expression.

$$Vamp = \sqrt{\left[Vn \cdot \left\| 1 + \frac{C1}{C2} \cdot \frac{1 + s \cdot R2 \cdot C2}{1 + s \cdot R1 \cdot C1} \right\| \right]^2} \tag{41.10}$$

Substituting in the component values and poles allows this to be rewritten

$$Vamp = Vn \cdot \left\| 1 + \frac{T1}{A0 \cdot R1} \cdot \frac{1 + s \cdot T2}{1 + s \cdot T1} \right\| \tag{41.11}$$

Again, we have a function that is decreasing in R1. So the conclusion is that choosing R1 larger improves both the noise due to the op-amp and also for the resistor itself. For a generic rule of thumb, we see that there are diminishing returns if the following condition is met.

$$\left\| \frac{T1}{A0 \cdot R1} \cdot \frac{1 + s \cdot T2}{1 + s \cdot T1} \right\| \ll 1 \tag{41.12}$$

Using the definitions of poles and component values, this constraint can be translated for low frequencies into:

$$\frac{T1}{A0 \cdot R1} \ll 1 \quad \Rightarrow \quad \frac{T1 \cdot R2}{T2 \cdot R1} \ll 1 \quad \Rightarrow \quad R2 \ll \frac{T2}{T1} \cdot R1 \tag{41.13}$$

At high frequencies, this constraint can be translated into

$$\frac{T2}{A0 \cdot R1} \ll 1 \quad \Rightarrow R2 \ll R1 \tag{41.14}$$

As T2 is always bigger than T1, this constraint will also satisfy the lower frequency constraint. To make this a non-issue, make this a factor of 10. If this leads to unrealistic values for other components, then revisit

$$R1 = 10 \cdot R2 \tag{41.15}$$

Appendix B: An Active Filter Design Example

Symbol	Description	Value	Units
BW	Loop Bandwidth	20	kHz
ϕ	Phase Margin	47.8	degrees
γ	Gamma Optimization Parameter	1	none
K_{PD}	Charge Pump Gain	3.1	mA
K_{VCO}	VCO Gain	44	MHz/V
f_{VCO}	Output Frequency	2442	MHz
f_{PD}	Phase detector frequency	2000	kHz
T31	Ratio of pole ***T3*** to Pole ***T1***	1000%	none
T43	Ratio of pole ***T4*** to Pole ***T1***	50%	none
AmpGain	Gain of op-amp	1 for Active A,B 3 for Active C	none

Calculate Poles and Zero and *A0*

$$N = \frac{f_{VCO}}{f_{PD}} \tag{41.16}$$

$$\omega c = 2\pi \cdot BW \tag{41.17}$$

T1 *is the only unknown. Solve for* ***T1*** *Using Numerical Methods*

$$\phi = tan^{-1}\left(\frac{\gamma}{\omega c \cdot T1 \cdot (1 + T31 + T43 \cdot T31)}\right) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T11 \cdot T31) - tan^{-1}(\omega c \cdot T1 \cdot T31 \cdot T43) \tag{41.18}$$

$$T3 = T1 \cdot T31 \tag{41.19}$$

$$T4 = T3 \cdot T43 \tag{41.20}$$

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1 + T3 + T4)} \tag{41.21}$$

$$A0 = \frac{K_{PD} \cdot K_{VCO} \cdot AmpGain}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2) \cdot (1 + \omega c^2 \cdot T4^2)}} \quad \textbf{(41.22)}$$

Symbol	Description	Value	Units
N	N Counter Value	1221	none
ωc	Loop Bandwidth	1.2566×10^5	rad/s
T1	Loop Filter Pole	1.8853×10^{-7}	s
T2	Loop Filter Zero	2.0994×10^{-5}	s
T3	Loop Filter Pole	1.8853×10^{-6}	s
T4	Loop Filter Pole	9.4263×10^{-7}	s
A0	Loop Filter Coefficient for Active A and B	31.0982	nF
	Loop Filter Coefficient for Active C	93.2945	nF

C3, C4, R3, and R4 for All Active Filters

$$C4 = 560\ pF \quad \textbf{(41.23)}$$

$$C3 = C4 \cdot \frac{4 \cdot T3 \cdot T4}{(T3 - T4)^2} \quad \textbf{(41.24)}$$

Symbol	Value	Units
C4	560	pF
C3	4480	pF
R3	280.5	Ω
R4	2524.9	Ω

560 pF was chosen for C4 as it is likely to be much larger than the VCO input capacitance. We see that the load presented to the op amp output is greater than 50 Ω, as R3 is larger than this alone, so therefore this choice of C4 was good. Had it been too small, then we would need to choose a smaller value for C4. However, the choice seems to have been a good one.

Active A Filter

$$C2 = A0 \tag{41.25}$$

$$R2 = \frac{T2}{C2} \tag{41.26}$$

$$R1 = 10 \cdot R2 \tag{41.27}$$

$$C1 = \frac{T1}{R1} \tag{41.28}$$

Symbol	Value	Units
C2	31.0982	nF
R2	0.6751	kΩ
R1	6.7508	kΩ
C1	0.0279	kΩ

Active B and C Filters

$$C1 = A0 \cdot \frac{T1}{T2} \tag{41.29}$$

$$C2 = A0 \cdot \left(1 - \frac{T1}{T2}\right) \tag{41.30}$$

$$R2 = \frac{T2}{C2} \tag{41.31}$$

Symbol	Value		Units
	Active B	Active C	
A0	31.0982	93.2945	nF
C1	0.2793	0.8378	nF
C2	30.8189	92.4568	nF
R2	681.2	227.1	Ω

Chapter 42 Active Filter from Differential Phase Detector Outputs

Introduction

This chapter investigates the design and performance of a loop filter designed using the differential phase detector outputs, ϕ_R and ϕ_N. In general, modern PLLs have excellent charge pumps on them and it is generally recommended not to bypass it. In doing so, all models concerning phase noise and spurs presented in this book become invalid. In fact, most modern PLLs do not have these differential phase detector outputs, with one notable exception of the Texas Instruments LMX2492 that allows the up and down signals to be multiplexed to some of the output pins. For those who insist on bypassing the charge pump and using these differential outputs, this chapter is included.

Loop Filter Topology

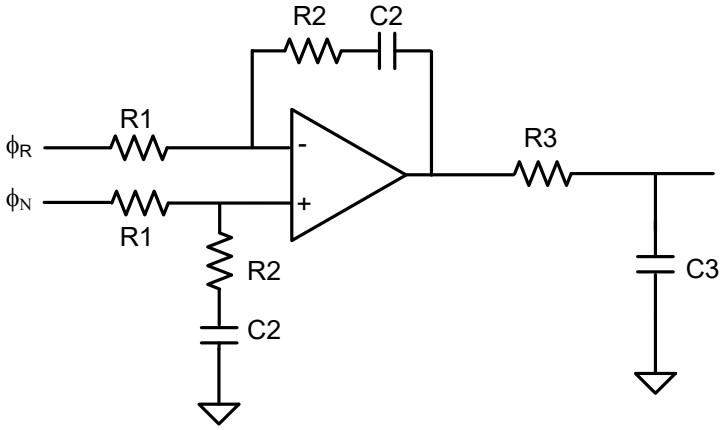


Figure 42.1 *Active Filter Topology Used*

The transfer function of the filter is given by:

$$Z(s) = \frac{1 + s \cdot T2}{s \cdot T \cdot (1 + s \cdot T1)} \quad \textbf{(42.1)}$$

Where

$$T2 = R2 \cdot C2 \quad \textbf{(42.2)}$$

$$T1 = R3 \cdot C3 \quad \textbf{(42.3)}$$

$$T = R1 \cdot C2 \quad \textbf{(42.4)}$$

The open loop gain is given by:

$$G(s) = \frac{K_V \cdot K_{VCO} \cdot (1 + s \cdot T2)}{s^2 \cdot T \cdot (1 + s \cdot T1)} \quad \textbf{(42.5)}$$

This transfer function has many similarities to the one for the passive second order filter. If the following substitutions are applied to expression for the open loop response for the second order filter, then the result is the transfer function for this loop filter topology. In these equations, $\boldsymbol{K_V}$ represents the maximum voltage output level of the phase detector outputs

$$T \Rightarrow A0 \quad \textbf{(42.6)}$$

$$K_V \Rightarrow K_{PD} \quad \textbf{(42.7)}$$

The case where ***R3 = C3 = 0*** presents a special case and has different equations, but is a topology that is sometimes used. This approach will be referred to as the alternative approach, and the case where ***T1>0*** will be referred to as the standard approach. In either case, the equations for the time constants and filter components are shown in Table 42.1.

Component	Standard Approach	Alternative Approach
T1	$\frac{sec(\phi) - tan(\phi)}{\omega c}$	*0*
T2	$\frac{\gamma}{\omega c^2 \cdot T1}$	$\frac{tan(\phi)}{\omega c}$
T	$\frac{K_V \cdot K_{VCO}}{N \cdot \omega c^2} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{1 + \omega c^2 \cdot T1^2}}$	$\frac{K_V \cdot K_{VCO}}{N \cdot \omega c^2 \cdot cos(\phi)}$
C2	*Choose this value*	*Choose this value*
R2	$\frac{T2}{C2}$	$\frac{T2}{C2}$
R1	$\frac{T}{C2}$	$\frac{T}{C2}$
C3	*Free to Choose.*	*0*
R3	$\frac{T1}{C3}$	*0*

Table 42.1 *Calculation of Components*

Conclusion

This chapter has presented design equations that can be used with the differential phase detector outputs. This approach is generally not recommended, because it requires an op-amp and most PLLs do not have these differential output pins. The reader should also be very aware of the states of the outputs. For instance, when this type of loop filter is used with Texas Instruments' LMX2301/05/15/20/25 PLLs, it is necessary to invert either ϕ_R or ϕ_N. For the LMX2492, this signal can be routed to the TRIG1,TRIG2, MOD, and MUXout pins.

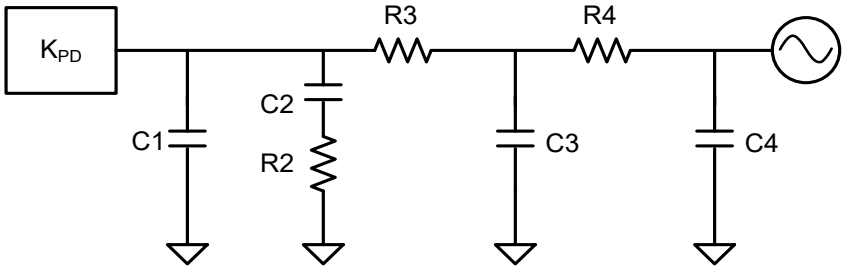
There are other approaches to loop filter design using these differential outputs. One such approach is to omit the components ***R3*** and ***C3***. This topology is more popular with older PLL designs than newer ones.

The lock time can be predicted with a formula, but the phase noise and spurs for this filter differ than those in a passive filter. The *BasePulseSpur* and *1HzNoiseFloor* are different, since the charge pump has been bypassed.

Reference

[1] *Phase-Locked Loop Design Fundamentals* Application Note 535 Motorola Semiconductor Products, 1970

Chapter 43 Partially Integrated Loop Filters



Introduction

In the age of higher integration, it is becoming more common practice for the VCO and loop filter to be integrated with the PLL synthesizer. Aside from cost and size, another advantage of partially integrating the loop filter is that it may be able to help filter crosstalk on the chip that can get to the VCO. The biggest disadvantage is that it is less flexible and integrating larger capacitors on silicon can be an expensive use of die area. A good compromise is for the loop filter to be partially integrated. This practice tends to be more common for passive filters, so this is the main focus on this chapter, but there is a section at the end to address active filters for the purposes of completion. As there are many combinations, only the more common combinations will be covered. For those designs not covered, the logic and reasoning used to derive the examples can be used as a guide for the other cases. In this chapter, the cases covered will fall under one of the following categories.

1. Second order loop filter
    a. Exactly One Component is fixed
        i. This forces the loop bandwidth
2. Third Order Loop Filter
    a. Exactly One component is fixed
        i. Loop parameters are free
        ii. The valid range to fix one component is restricted
    b. R3 and C3 are Fixed
        i. T3/T1 ratio is forced
        ii. The loop bandwidth is restricted to a maximum possible value
        iii. The phase margin will be close, but slightly off
3. Fourth Order Filters
    a. R3, R4, C3, and C4 are Fixed
        i. T3/T1 ratio is fixed
        ii. T4/T3 ratio is fixed
        iii. The loop bandwidth is restricted to a maximum possible value
        iv. The loop bandwidth will be close, but slightly off
        v. The phase margin will be close, but slightly off
        vi. The gamma optimization parameter will be close, but slightly off

General Concepts

Calculation of the Pole Sum Constant, κ

For all filters, one can define a constant that depends only on phase margin and gamma that comes up in many situations.

$$\kappa = \frac{\sqrt{(1+\gamma)^2 \cdot tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot tan\,\phi}{2} \quad \textbf{(43.1)}$$

The following relationship holds exactly in the case of a 2nd order filter and is a very good approximation in the case of higher order filters.

$$T1 + T3 + T4 \approx \frac{\kappa}{\omega c} \quad \textbf{(43.2)}$$

If we assume that the phase margin and gamma are chosen, then κ will be a constant and this relationship will be very useful in determining the components.

Calculation of the Time Constant, T2

For all filters, the pole sum constant can be used to approximate T2.

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1 + T3 + T4)} \approx \frac{\gamma}{\omega c \cdot \kappa} \quad \textbf{(43.3)}$$

Second Order Loop Filter with Exactly One Component Integrated

General Relationships

Using the known relationships, the following equations can be derived without introducing any approximations.

$$T1 = \frac{\kappa}{\omega c} \quad \textbf{(43.4)}$$

$$T2 = \frac{\gamma}{\omega c \cdot \kappa} \quad \textbf{(43.5)}$$

From this, the ratio of time constants can be found.

$$\frac{T2}{T1} = \frac{\gamma}{\kappa^2} \tag{43.6}$$

$$\frac{T2}{T1} = \frac{R2 \cdot C2}{\left(\frac{R2 \cdot C2 \cdot C1}{C1 + C2}\right)} = 1 + \frac{C2}{C1} \tag{43.7}$$

This allows the ratio of the capacitors to be expressed in a simple form that can be used to find C2 from C1 or vice versa.

$$\frac{C2}{C1} = \frac{\gamma}{\kappa^2} - 1 \tag{43.8}$$

Another relationship can be derived from the loop filter coefficient A0.

$$A0 = C1 + C2 = \frac{K_{PD} \cdot K_{VCO}}{N \cdot \omega c^2} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2}} \tag{43.9}$$

This can be manipulated to find the loop bandwidth.

$$\omega c = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{N \cdot A0} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2}}} \tag{43.10}$$

C1 or C2 is Fixed

Since the relationship between C1 and C2 is known, if you know one, the other can be easily found. For instance, if C1 is known, C2 can be found.

$$C2 = C1 \cdot \left(\frac{\gamma}{\kappa^2} - 1\right) \tag{43.11}$$

If C2 is known, C1 can easily be found.

$$C1 = \frac{C2}{\frac{\gamma}{\kappa^2} - 1} \tag{43.12}$$

Once these two are known, the loop bandwidth can easily be calculated.

$$\omega c = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{N \cdot (C1 + C2)}} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2}} \tag{43.13}$$

Once the loop bandwidth is known, T2 can be calculated. This result can then be used to find R2.

$$T2 = \frac{\gamma}{\omega c \cdot \kappa} \tag{43.14}$$

$$R2 = \frac{T2}{C2} \tag{43.15}$$

R2 is Fixed

In this case, some work is needed to find the loop bandwidth. We can say that:

$$C2 = \frac{T2}{R2} \Rightarrow C2 = \frac{\gamma}{\omega c \cdot \kappa \cdot R2} \tag{43.16}$$

Substituting this into the expression for loop bandwidth yields the following equation.

$$\omega c = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{N \cdot \left(\frac{\gamma}{\omega c \cdot \kappa \cdot R2}\right) \cdot \left(\frac{1}{\frac{\gamma}{\kappa^2} - 1} + 1\right)}} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2}} \tag{43.17}$$

This equation can be solved for ωc.

$$\omega c = \frac{K_{PD} \cdot K_{VCO} \cdot R2 \cdot (\gamma - \kappa^2) \cdot \kappa}{N \cdot \gamma^2} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2}} \tag{43.18}$$

Once the loop bandwidth is found, it is easy to solve for the other components.

$$T2 = \frac{\gamma}{\omega c \cdot \kappa} \tag{43.19}$$

$$C2 = \frac{T2}{R2} \tag{43.20}$$

$$C1 = \frac{C2}{\frac{\gamma}{\kappa^2} - 1} \tag{43.21}$$

Third Order Loop Filter with Exactly One Component Integrated

Recall that the third order passive filter has one degree of freedom. To satisfy this, an additional constraint was specified to maximize the value of ***C3***. However, if a component is already specified, then all that is necessary to do is to drop this constraint, and plug in the known value and solve. The following filter constants are for a passive third order filter and will be used throughout this section.

$$T2 = R2 \cdot C2 \tag{43.22}$$

$$A2 = C1 \cdot T2 \cdot C3 \cdot R3 \tag{43.23}$$

$$A1 = T2 \cdot (C1 + C3) + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3 \tag{43.24}$$

$$A0 = C1 + C2 + C3 \tag{43.25}$$

C2 or R2 is Fixed

The basic strategy in this case is to find C2, if it is not known already. Then from this case, one can focus on finding the other components from C2. For instance, if R2 is the specified component, then C2 can easily be found.

$$C2 = \frac{T2}{R2} \tag{43.26}$$

The next step is to find the value of C1. For this, realize that the product of C3 and R3 can be found from (43.23). Combined with (43.24) and (43.25), the following equations can be derived.

$$A1 = T2 \cdot (C1 + C3) + C1 \cdot \left(\frac{A2}{C1 \cdot T2}\right) + C2 \cdot \left(\frac{A2}{C1 \cdot T2}\right) \tag{43.27}$$

$$C3 = A0 - C1 - C2 \tag{43.28}$$

Combining these two equations gives the following relationship between C1 and C2.

$$A1 = T2 \cdot A0 - T2 \cdot C2 - \frac{A2}{T2} + \frac{C2}{C1} \cdot \left(\frac{A2}{T2}\right) \tag{43.29}$$

This can be rearranged to find the equation for C1.

$$C1 = \frac{A2}{T2} \cdot \frac{C2}{A1 - T2 \cdot (A0 - C2) - \frac{A2}{T2}} \tag{43.30}$$

At this point, C1, C2, and R2 are all known and C3 and R3 can easily be found.

$$C3 = A0 - C1 - C2 \tag{43.31}$$

$$R3 = \frac{A2}{T2 \cdot C1 \cdot C3} \tag{43.32}$$

C1 or C3 is Fixed

If C1 is the fixed component, then C3 can be derived by (39.20) as used for the third order passive filter.

$$C3 = \frac{-T2^2 \cdot C1^2 + T2 \cdot A1 \cdot C1 - A2 \cdot A0}{T2^2 \cdot C1 - A2} \tag{43.33}$$

In the case that C3 is fixed, some work is needed to find C1. Note that there is a maximum value for C3 that would be the value for the unrestricted third order filter. The approach is to rearrange the equations in order to find an expression for the product of C3 and R3.

$$\frac{A2}{T2 \cdot C1} = C3 \cdot R3 \tag{43.34}$$

The next step is to substitute this into the equation for A1.

$$A1 - T2 \cdot C3 = T2 \cdot C1 + (A0 - C3) \cdot \frac{A2}{T2 \cdot C1} \tag{43.35}$$

This leads to a quadratic equation for C1 that has the following solution.

$$C1 = \frac{A1 - T2 \cdot C3 + \sqrt{(A1 - T2 \cdot C3)^2 - 4 \cdot (A0 - C3)}}{2 \cdot T2} \tag{43.36}$$

Note that it is possible for this expression to C1 to not be a positive real number, so this check needs to be made to ensure this. Assuming that the solution for C1 is proper, the other components can be easily found.

$$C2 = A0 - C1 - C3 \tag{43.37}$$

$$R2 = \frac{T2}{C2} \tag{43.38}$$

$$R3 = \frac{A2}{C1 \cdot C3 \cdot T2} \tag{43.39}$$

R3 is Fixed

This case has some similarities to the case that ***C3*** is integrated. If ***R3*** is too small, it causes issues, just as having ***C3*** too large. That being said, it does involve more work. The first step is to arrange the filter coefficient equations as shown.

$$\frac{A2}{T2 \cdot R3} = C1 \cdot C3 \tag{43.40}$$

$$A1 - \frac{A2}{T2} = T2 \cdot C3 + C1 \cdot T2 + C2 \cdot C3 \cdot R3 \tag{43.41}$$

$$A0 = C1 + C2 + C3 \tag{43.42}$$

These can be combined to create the following equation.

$$A1 - \frac{A2}{T2} = \frac{A2}{C1 \cdot R3} + C1 \cdot T2 + \left(A0 - C1 - \frac{A2}{T2 \cdot R3 \cdot C1}\right) \cdot \frac{A2}{T2 \cdot C1} \tag{43.43}$$

This equation can be arranged to form a cubic polynomial in C1, which can be solved.

$$T2 \cdot C1^3 - A1 \cdot C1^2 + \left(\frac{A2}{R3} + \frac{A0 \cdot A2}{T2}\right) \cdot C1 - \frac{A2^2}{T2^2 \cdot R3} = 0 \tag{43.44}$$

C2 can be solved for in terms of C1 as follows:

$$C2 = \frac{A1 \cdot C1 \cdot T1 - A2 \cdot C1 - C1 \cdot A0 \cdot T2^2}{A2 - T2^2 \cdot C1} \tag{43.45}$$

Once these components are known, R2 and C3 can be easily found.

The Loop Filter is Third Order with R3 and C3 Integrated

Finding the New Filter Coefficients and Time Constants

Under the assumption that R3 and C3 are known, the challenge is that this puts a restriction on the loop parameters and T3/T1 cannot be chosen if one wants the other parameters as desired. It also puts a restriction on the loop bandwidth as well. What this means is that all the filter coefficients and constants have to be treated as unknowns. However, they can be found from the design parameters. The first step is to find an expression for the sum of the poles, which has already been found.

$$T1 + T3 \approx \frac{\kappa}{\omega c} \tag{43.46}$$

$$T2 \approx \frac{\gamma}{\omega c \cdot \kappa} \tag{43.47}$$

The second step is much more involved, but involves finding an expression for the product of the two poles, T1 and T3. This starts with taking the filter design equations and equation for A0.

$$T2 = R2 \cdot C2 \tag{43.48}$$

$$A2 = A0 \cdot T1 \cdot T3 = C1 \cdot T2 \cdot C3 \cdot R3 \tag{43.49}$$

$$A1 = A0 \cdot (T1 + T3) = T2 \cdot C3 + C1 \cdot T2 + C1 \cdot C3 \cdot R3 + C2 \cdot C3 \cdot R3 \tag{43.50}$$

$$A0 = C1 + C2 + C3 \tag{43.51}$$

These equations can be combined to eliminate C2 and R2.

$$\frac{A0}{T2 \cdot C3 \cdot R3} = \frac{C1}{T1 \cdot T3} \tag{43.52}$$

$$A0 \cdot \frac{\kappa}{\omega c} = C3 \cdot T2 + C1 \cdot T2 + (A0 - C3) \cdot R3 \cdot C3 \tag{43.53}$$

These equations can be combined to eliminate C1 and express A0 in terms of other quantities.

$$A0 \cdot \frac{\kappa}{\omega c} = T2 \cdot C3 + \frac{A0 \cdot T1 \cdot T3}{C3 \cdot R3} + (A0 - C3) \cdot R3 \cdot C3 \tag{43.54}$$

This equation can be solved for A0.

$$A0 = \frac{R3 \cdot C3^2 \cdot (T2 - R3 \cdot C3)}{\frac{\kappa}{\omega c} \cdot R3 \cdot C3 - T1 \cdot T3 - (R3 \cdot C3)^2} \quad \textbf{(43.55)}$$

Recall that A0 can also be calculated in a different way.

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2)}} \quad \textbf{(43.56)}$$

.

This can also be expressed in another form with T1·T3 and T1+T3 being the only unknowns.

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{1 + \omega c^2 \cdot (T1 + T3)^2 - 2 \cdot \omega c^2 \cdot T1 \cdot T3 + \omega c^4 \cdot (T1 \cdot T3)^2}} \quad \textbf{(43.57)}$$

Some further approximate relations can be substituted for T2 and T1+T3.

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2 - 2 \cdot \omega c^2 \cdot (T1 \cdot T3) + \omega c^4 \cdot (T1 \cdot T3)^2}} \quad \textbf{(43.58)}$$

Equations (43.55) and (43.56) are both for finding A0 and can be equated.

$$\frac{\omega c^2 \cdot R3 \cdot C3^2 \cdot (T2 - R3 \cdot C3)}{\omega c \cdot \kappa \cdot R3 \cdot C3 - \omega c^2 \cdot T1 \cdot T3 - \omega c^2 \cdot (R3 \cdot C3)^2} = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N \cdot \kappa} \cdot \sqrt{\frac{\kappa^2 + \gamma^2}{1 + \kappa^2 - 2 \cdot \omega c^2 \cdot T1 \cdot T3 + \omega c^4 \cdot (T1 \cdot T3)^2}} \quad \textbf{(43.59)}$$

The expression can expressed in a simpler form using some substitutions

$$\frac{A}{B-x} = \frac{1}{\sqrt{\kappa^2 + (1-x)^2}} \tag{43.60}$$

$$A = \frac{\omega c^4 \cdot N \cdot \kappa \cdot R3 \cdot C3^2 \cdot (T2 - R3 \cdot C3)}{K_{PD} \cdot K_{VCO} \cdot \sqrt{\kappa^2 + \gamma^2}} \tag{43.61}$$

$$B = \omega c \cdot \kappa \cdot R3 \cdot C3 - \omega c^2 \cdot (R3 \cdot C3)^2 \tag{43.62}$$

$$x = \omega c^2 \cdot T1 \cdot T3 \tag{43.63}$$

This can be written in the form of a quadratic equation:

$$(1 - A^2) \cdot x^2 + 2 \cdot (A^2 - B) \cdot x + (B^2 - A^2 - A^2 \cdot \kappa^2) = 0 \tag{43.64}$$

The product of the poles can be found by using the quadric formula.

$$T1 \cdot T3 = \frac{x}{\omega c^2} = \frac{B - A^2 \pm \sqrt{(A^2 - B)^2 + (A^2 - 1) \cdot (B^2 - A^2 - A^2 \cdot \kappa^2)}}{\omega c^2 \cdot (1 - A^2)} \tag{43.65}$$

This formula can be further simplified.

$$(T1 \cdot T3) = \frac{B - A^2 \pm A \cdot \sqrt{\kappa^2 \cdot (1 - A^2) + (B-1)^2}}{\omega c^2 \cdot (1 - A^2)} \tag{43.66}$$

One needs to check which solution gives the correct answer for (43.66); the wrong one will have a negative sign. From this, the loop filter coefficient A0 can be found.

$$A0 = \frac{R3 \cdot C3^2 \cdot (T2 - R3 \cdot C3)}{\frac{\kappa}{\omega c} \cdot R3 \cdot C3 - (T1 \cdot T3) - (R3 \cdot C3)^2} \tag{43.67}$$

Now the other components are easy to find.

$$C1 = \frac{A0 \cdot (T1 \cdot T3)}{T2 \cdot R3 \cdot C3} \tag{43.68}$$

$$C2 = A0 - C1 - C3 \tag{43.69}$$

$$R2 = \frac{T2}{C2} \tag{43.70}$$

Finding the Maximum Possible Loop Bandwidth

For the reader who has not grown weary of this case, the maximum possible loop bandwidth for components can be found. This can be done by setting T1 to zero in equation (43.59) and T2 as defined in (43.47).

$$\frac{{\omega c_{max}}^3 \cdot C3 \cdot \left(\frac{\gamma}{\omega c_{max} \cdot \kappa} - R3 \cdot C3\right)}{\kappa - \omega c_{max} \cdot R3 \cdot C3} = \frac{K_{PD} \cdot K_{VCO}}{N \cdot \kappa} \cdot \sqrt{\frac{\kappa^2 + \gamma^2}{1 + \kappa^2}} \tag{43.71}$$

This leads to the following cubic equation.

$${\omega c_{max}}^3 + b2 \cdot {\omega c_{max}}^2 + b1 \cdot \omega c_{max} + b0 = 0 \tag{43.72}$$

$$b2 = -\frac{\gamma}{\kappa \cdot R3 \cdot C3} \tag{43.73}$$

$$b1 = -\frac{K_{PD} \cdot K_{VCO}}{\kappa \cdot N \cdot C3} \cdot \sqrt{\frac{\kappa^2 + \gamma^2}{1 + \kappa^2}} \tag{43.74}$$

$$b0 = \frac{K_{PD} \cdot K_{VCO}}{N \cdot R3 \cdot C3^2} \cdot \sqrt{\frac{\kappa^2 + \gamma^2}{1 + \kappa^2}} \tag{43.75}$$

This cubic polynomial can be solved to find the maximum possible loop bandwidth exactly. Care must be taken to choose the proper root. To check this, consider only the positive real roots. If there is more than one positive real root, then the correct one can be found by finding the component values with them and seeing which one leads to positive component values.

What to do if the Maximum Achievable Loop Bandwidth is Exceeded

If this maximum loop bandwidth is greater than the specified loop bandwidth, there are a few options:

(1) Choose this maximum loop bandwidth which will lead to C1 = 0 and one less pole. However, it will have the maximum loop bandwidth.

(2) Respecify the loop bandwidth to something less than this maximum loop bandwidth and redesign.

(3) Lower the phase margin and/or increase gamma to increase the maximum achievable loop bandwidth.

In the first scenario when one chooses to keep this maximum loop bandwidth and make C1=0, the design equations are simplified by setting T1·T3 = 0. For this scenario, the filter values can be found

$$T2 = \frac{\gamma}{\omega c_{max} \cdot \kappa} \tag{43.76}$$

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{N \cdot \kappa \cdot \omega c_{max}} \cdot \sqrt{\frac{\gamma + \kappa^2}{1 + \kappa^2}} \tag{43.77}$$

$$C1 = 0 \tag{43.78}$$

$$C2 = A0 - C3 \tag{43.79}$$

$$R2 = \frac{T2}{C2} \tag{43.80}$$

Passive Fourth Order Filter

One or Two Components is Integrated

In this case, one can theoretically solve exactly. However, the issue is that this could lead to negative or complex component values. As most of these cases are not too likely and there are 28 of them they will not be covered.

Case of a Passive Fourth Order Loop Filter with C3, R3, C4, and R4 Integrated

When the case of a third order filter was considered, an approximation was already introduced. In this case of a fourth order passive partially integrated filter, the attempt to find an elegant closed form solution without introducing any approximations or resulting to numerical methods is left to the avid and very determined reader, if even possible all. For everybody else, it greatly simplifies the problem to approximate ***R3***, ***R4***, ***C3***, and ***C4*** as a simple RC low pass filter and then apply the third order passive formulas. In order to get this approximate low pass filter, two constraints need to be applied. Two possible constraints are that at a frequency equal to the loop bandwidth, the loading on the filter and the transfer function through these components need to be the same as it would be if all four components were used. The load of the four components is:

$$L(s) = R3 + \frac{\frac{1}{s \cdot C3} \cdot \left(R4 + \frac{1}{s \cdot C4}\right)}{\frac{1}{s \cdot C3} + \frac{1}{s \cdot C4} + R4} \qquad \textbf{(43.81)}$$

The transfer function of the four components is:

$$T(s) = \frac{1}{1 + s \cdot (C3 \cdot R3 + C4 \cdot R3 + C4 \cdot R3) + s^2 \cdot C3 \cdot C4 \cdot R3 \cdot R4} \qquad \textbf{(43.82)}$$

Now, since there are actually two components, these two constraints can be met exactly. The component, C, will always be real and can be found.

$$C = \frac{-1}{\omega c \cdot Imag\{\, L(j \cdot \omega c)\,\}} \qquad \textbf{(43.83)}$$

However, R will be complex in general. So an approximation needs to be introduced where R is approximated with its real component

$$R = Real\left(\frac{\frac{1}{T(j \cdot \omega c)} - 1}{C \cdot j \cdot \omega c}\right) \qquad \textbf{(43.84)}$$

From this, the equations for the third order filter can be applied.

Active Partially Integrated Filters

General Comments

Integrated active filters tend to be much less common, but for the sake of completeness, they are addressed here. The mathematics are greatly simplified because the op-amp ads isolation between the poles. In general, the same general relationships hold.

$$T1 + T3 + T4 = \frac{\kappa}{\omega c} \tag{43.85}$$

$$T2 = \frac{\gamma}{\omega c \cdot \kappa} \tag{43.86}$$

Second Order Filter with One Specified Component

These equations are very similar to the passive case. For the Active B, they are exactly the same. For the Active C, they are the same, but the VCO gain is multiplied by the gain in the loop due to the op-amp. For the Active A filter, the isolation of R1 and C1 make it so that one can freely choose one and design the other component.

Third Order Filter with One Specified Component

If the specified component is R3 or C3, then this is a degree of freedom and one can design and have the same loop filter parameters. If the integrated component is C1, C2 or R2, one could find equations, but this is a very rare scenario and is not handled.

Third and Fourth Order Filters with R3, R4, C3, and C4 Specified

In the case of a third order filter, consider R4=C4=0. For this case, the sum of the poles T3+T4 is easy to find from the components.

$$T3 + T4 = C3 \cdot R3 + C4 \cdot R3 + C4 \cdot R4 \tag{43.87}$$

The maximum achievable loop bandwidth is also easy to find once this sum is known by setting T1=0.

$$\omega c_{max} = \frac{\kappa}{T3 + T4} \tag{43.88}$$

Pole T1 can be found as follows:

$$T1 = \frac{\kappa}{\omega c} - (T3 + T4) \tag{43.89}$$

Now it is necessary to explicitly calculate the poles T3 and T4. For the fourth order filter, the following equations can be used. In the case of a third order filter, these calculations simplify to T3 equaling R3·C3.

$$T3 = \frac{(T3 + T4) + \sqrt{(T3 + T4)^2 - 4 \cdot C3 \cdot C4 \cdot R3 \cdot R4}}{2} \tag{43.90}$$

$$T4 = \frac{(T3 + T4) - \sqrt{(T3 + T4)^2 - 4 \cdot C3 \cdot C4 \cdot R3 \cdot R4}}{2} \tag{43.91}$$

The filter coefficient A0 can now be found. *AmpGain* is included and is different than one in the case of an Active C filter.

$$A0 = \frac{K_{PD} \cdot K_{VCO} \cdot AmpGain}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2) \cdot (1 + \omega c^2 \cdot T4^2)}} \tag{43.92}$$

Once A0 is known, the other components are easy to find. For the Active A Filter:

$$C2 = A0 \tag{43.93}$$

$$R2 = \frac{T2}{C2} \tag{43.94}$$

$$\text{Choose } R1 = 10 \cdot R2 \tag{43.95}$$

$$C1 = \frac{T1}{R1} \tag{43.96}$$

For the Active B and C Filters:

$$C1 = \frac{T1 \cdot A0}{T2} \quad \textbf{(43.97)}$$

$$C2 = A0 - C1 \quad \textbf{(43.98)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.99)}$$

Conclusion

Partially integrated loop filters have come about in the age that more and more is being integrated. This chapter has discussed many possible configurations for this type of filter. Aside from saving components, partially integrated loop filters may be useful because they have the ability to filter noise on the chip itself. If the loop filter is integrated on chip, then there is a good probability that the VCO may also be integrated. Crosstalk on chips should always be taken as a serious issue, and if at least part of the loop filter is on the chip, it may be able to filter noise that otherwise could not be filtered. Aside from dealing with the case that the component is integrated, the equations could also be used if one wanted to force a particular value of component in the loop filter.

Forcing component values may put restrictions on the loop bandwidth, phase margin, gamma, or pole ratios. In those cases where the loop filter is totally integrated, but there are selectable values for each component, the best approach might be to resort to computers and numerical methods.

Appendix A: Design Examples for Partially Integrated Loop Filters

All Loop Filters

Unless otherwise specified, the conditions below apply to all of the examples presented in this appendix.

Symbol	Description	Value	Units
BW	Loop Bandwidth	10	kHz
ϕ	Phase Margin	50	degrees
γ	Gamma Optimization Parameter	1	none
K_{PD}	Charge Pump Gain	5	mA
K_{VCO}	VCO Gain	20	MHz/V
f_{VCO}	Output Frequency	2450	MHz
f_{PD}	Phase detector frequency	200	kHz

Calculate the Pole Sum Constant and N

$$\kappa = \frac{\sqrt{(1+\gamma)^2 \cdot tan^2\phi + 4 \cdot \gamma} - (1+\gamma) \cdot tan\phi}{2} \quad \textbf{(43.100)}$$

$$N = \frac{f_{VCO}}{f_{PD}} \quad \textbf{(43.101)}$$

Symbol	Description	Value	Units
κ	Pole Sum Constant	0.3640	n/a
N	Feedback Divider	12250	n/a

Second Order Loop Filters

C1 is Fixed

Assume that C2 is the one that is integrated. If this is not the case and the integrated component is R2, the one an easily find C2 via one of these two equations.

$$C2 = C1 \cdot \left(\frac{\gamma}{\kappa^2} - 1\right) \quad \textbf{(43.102)}$$

$$\omega c = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{N \cdot (C1 + C2)} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2}}} \quad \textbf{(43.103)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.104)}$$

$$\frac{T2}{T1} = \frac{\gamma}{\kappa^2} \quad \textbf{(43.105)}$$

Symbol	Description	Value	Units
κ	Calculation Constant	0.3657	n/a
C1	Specified C1 Value	0.82	nF
C2	Loop Filter Capacitor	5.3699	nF
$\frac{\omega c}{2\pi}$	Respecified Loop Bandwidth	9.5802	kHz
T2	Loop Filter Zero	4.5643×10^{-5}	sec
R2	Loop Filter Resistor	8.500	kΩ

C2 is Fixed

Assume that C2 is the one that is integrated. If this is not the case and the integrated component is R2, the one an easily find C2 via one of these two equations.

$$C1 = \frac{C2}{\frac{\gamma}{\kappa^2} - 1} \quad \textbf{(43.106)}$$

$$\omega c = \sqrt{\frac{K_{PD} \cdot K_{VCO}}{N \cdot (C1 + C2)} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2}}} \quad \textbf{(43.107)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.108)}$$

$$\frac{T2}{T1} = \frac{\gamma}{\kappa^2} \quad \textbf{(43.109)}$$

Symbol	Description	Value	Units
κ	Calculation Constant	0.3657	n/a
C2	Specified C2 Value	4.7	nF
C1	Loop Filter Capacitor	0.7177	nF
$\frac{\omega c}{2\pi}$	Respecified Loop Bandwidth	10.2403	kHz
T2	Loop Filter Zero	4.2701×10^{-5}	sec
R2	Loop Filter Resistor	9.0854	kΩ

R2 is Fixed

$$\omega c = \frac{K_{PD} \cdot K_{VCO} \cdot R2 \cdot (\gamma - \kappa^2) \cdot \kappa}{N \cdot \gamma^2} \cdot \sqrt{\frac{1 + \left(\frac{\gamma}{\kappa}\right)^2}{1 + \kappa^2}} \quad \textbf{(43.110)}$$

Once the loop bandwidth is found, it is easy to solve for the other components.

$$T2 = \frac{\gamma}{\omega c \cdot \kappa} \quad \textbf{(43.111)}$$

$$C2 = \frac{T2}{R2} \quad \textbf{(43.112)}$$

$$C1 = \frac{C2}{\frac{\gamma}{\kappa^2} - 1} \quad \textbf{(43.113)}$$

Symbol	Description	Value	Units
κ	Calculation Constant	0.3657	n/a
R2	Specified Value	10	kΩ
$\frac{\omega c}{2\pi}$	Respecified Loop Bandwidth	11.2711	kHz
T2	Loop Filter Zero	3.8796×10^{-5}	sec
C2	Loop Filter Capacitor	3.8796	nF
R2	Loop Filter Resistor	0.5924	nF

Third Order Loop Filters

Symbol	Description	Value	Units
BW	Loop Bandwidth	10	kHz
ϕ	Phase Margin	50	degrees
γ	Gamma Optimization Parameter	1	none
$T31$	T3/T1 Pole Ratio	50	%
K_{PD}	Charge Pump Gain	5	mA
K_{VCO}	VCO Gain	20	MHz/V
f_{VCO}	Output Frequency	2450	MHz
f_{PD}	Phase detector frequency	200	kHz

Third Order Filter of one Fixed Component

In this case, the poles and time constants are calculated exactly.

$$T1 = \frac{root\left[\emptyset - tan^{-1}\left(\frac{\gamma}{\omega c \cdot T1 \cdot \gamma \cdot (1+T31)}\right) - tan^{-1}(\omega c \cdot T1) - tan^{-1}(\omega c \cdot T1 \cdot T31)\right]}{\omega c} \quad \textbf{(43.114)}$$

$$T3 = T1 \cdot T31 \quad \textbf{(43.115)}$$

$$T2 = \frac{\gamma}{\omega c^2 \cdot (T1 + T3)} \quad \textbf{(43.116)}$$

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{\omega c^2 \cdot N} \cdot \sqrt{\frac{1 + \omega c^2 \cdot T2^2}{(1 + \omega c^2 \cdot T1^2) \cdot (1 + \omega c^2 \cdot T3^2)}} \quad \textbf{(43.117)}$$

Symbol	Description	Value	Units
$T1$	Loop Filter Pole	3.8057×10^{-6}	sec
$T2$	Loop Filter Zero	4.4370×10^{-5}	sec
$T3$	Loop Filter Pole	1.9032×10^{-6}	sec
$A0$	Loop Filter Coefficient	5.9142	nF
$A1$	Loop Filter Coefficient	3.3764×10^{-5}	sec·nF
$A2$	Loop Filter Coefficient	4.2837×10^{-11}	sec^2·nF

C1 is Fixed

Symbol	Description	Value	Units
C1	Specified Loop Filter Capacitor	0.390	**nF**
C2	Loop Filter Capacitor	5.4808	**nF**
R2	Loop Filter Resistor	8.0955	**kΩ**
C3	Loop Filter Capacitor	43.4110	**pF**
R3	Loop Filter Resistor	57.02845	**kΩ**

$$C3 = \frac{-T2^2 \cdot C1^2 + T2 \cdot A1 \cdot C1 - A2 \cdot A0}{T2^2 \cdot C1 - A2} \quad \textbf{(43.118)}$$

$$C2 = A0 - C1 - C3 \quad \textbf{(43.119)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.120)}$$

$$R3 = \frac{A2}{T2 \cdot C1 \cdot C3} \quad \textbf{(43.121)}$$

C2 is Fixed

Symbol	Description	Value	Units
C2	Specified Loop Filter Capacitor	5.6	**nF**
C1	Loop Filter Capacitor	0.2867	**nF**
R2	Loop Filter Resistor	7.9232	**kΩ**
C3	Loop Filter Capacitor	27.5034	**pF**
R3	Loop Filter Resistor	122.4242	**kΩ**

$$C1 = \frac{A2}{T2} \cdot \frac{C2}{A1 - T2 \cdot (A0 - C2) - \frac{A2}{T2}} \quad \textbf{(43.122)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.123)}$$

$$C3 = A0 - C1 - C2 \quad \textbf{(43.124)}$$

$$R3 = \frac{A2}{T2 \cdot C1 \cdot C3} \quad \textbf{(43.125)}$$

$$C1 = \frac{A2}{T2} \cdot \frac{C2}{A1 - T2 \cdot (A0 - C2) - \frac{A2}{T2}} \quad \textbf{(43.126)}$$

At this point, C1, C2, and R2 are all known and C3 and R3 can easily be found.

$$C3 = A0 - C1 - C2 \quad \textbf{(43.127)}$$

$$R3 = \frac{A2}{T2 \cdot C1 \cdot C3} \quad \textbf{(43.128)}$$

R2 is Fixed

Symbol	Description	Value	Units
R2	Specified Loop Filter Resistor	8.2	**kΩ**
C2	Loop Filter Capacitor	5.4110	**nF**
C1	Loop Filter Resistor	0.4990	**nF**
C3	Loop Filter Capacitor	4.2385	**pF**
R3	Loop Filter Resistor	456.4505	**kΩ**

$$C2 = \frac{T2}{R2} \tag{43.129}$$

$$C1 = \frac{A2}{T2} \cdot \frac{C2}{A1 - T2 \cdot (A0 - C2) - \frac{A2}{T2}} \tag{43.130}$$

$$C3 = A0 - C1 - C2 \tag{43.131}$$

$$R3 = \frac{A2}{T2 \cdot C1 \cdot C3} \tag{43.132}$$

C3 is Fixed

Symbol	Description	Value	Units
C3	Specified Loop Filter Capacitor	33	nF
C1	Loop Filter Capacitor	0.4311	nF
C2	Loop Filter Resistor	5.4501	nF
R2	Loop Filter Resistor	8.1411	kΩ
R3	Loop Filter Resistor	67.8570	kΩ

$$C1 = \frac{A1 - T2 \cdot C3 + \sqrt{(A1 - T2 \cdot C3)^2 - 4 \cdot (A0 - C3)}}{2 \cdot T2} \quad \textbf{(43.133)}$$

$$C2 = A0 - C1 - C3 \quad \textbf{(43.134)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.135)}$$

$$R3 = \frac{A2}{C1 \cdot C3 \cdot T2} \quad \textbf{(43.136)}$$

R3 is Fixed

Symbol	Description	Value	Units
R3	Specified Loop Filter Capacitor	68	kΩ
C1	Loop Filter Capacitor	0.4314	nF
C2	Loop Filter Resistor	5.4499	nF
R2	Loop Filter Resistor	8.1414	kΩ
C3	Loop Filter Capacitor	32.9093	pF

The following cubic polynomial needs to be solved for C1.

$$T2 \cdot C1^3 - A1 \cdot C1^2 + \left(\frac{A2}{R3} + \frac{A0 \cdot A2}{T2}\right) \cdot C1 - \frac{A2^2}{T2^2 \cdot R3} = 0 \quad \textbf{(43.137)}$$

$$C2 = \frac{A1 \cdot C1 \cdot T1 - A2 \cdot C1 - C1 \cdot A0 \cdot T2^2}{A2 - T2^2 \cdot C1} \quad \textbf{(43.138)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.139)}$$

$$C3 = A0 - C1 - C2 \quad \textbf{(43.140)}$$

$$R3 = \frac{A2}{T2 \cdot C1 \cdot C3} \quad \textbf{(43.141)}$$

Passive Third Order Loop Filter with R3 and C3 Integrated

Symbol	Description	Value	Units
C3	Specified Loop Filter Capacitor	100	**pF**
R3	Specified Loop Filter Resistor	40	**kΩ**
κ	Previously calculated constant	0.3657	n/a

First calculate the loop bandwidth to ensure that it is not larger than the specified value.

$$\omega c_{max}{}^3 + b2 \cdot \omega c_{max}{}^2 + b1 \cdot \omega c_{max} + b0 = 0 \quad \textbf{(43.142)}$$

$$b2 = -\frac{\gamma}{\kappa \cdot R3 \cdot C3} \quad \textbf{(43.143)}$$

$$b1 = -\frac{K_{PD} \cdot K_{VCO}}{\kappa \cdot N \cdot C3} \cdot \sqrt{\frac{\kappa^2 + \gamma^2}{1 + \kappa^2}} \quad \textbf{(43.144)}$$

$$b0 = \frac{K_{PD} \cdot K_{VCO}}{N \cdot R3 \cdot C3^2} \cdot \sqrt{\frac{\kappa^2 + \gamma^2}{1 + \kappa^2}} \quad \textbf{(43.145)}$$

Symbol	Description	Value	Units
b2	Calculated Value	-6.8687×10^5	Hz
b1	Calculated Value	-2.2428×10^{11}	Hz^2
b0	Calculated Value	2.0408×10^{16}	Hz^3
$\frac{\omega c_{max}}{2\pi}$	Maximum Attainable Bandwidth	12.0110	kHz

$$A = \frac{\omega c^4 \cdot N \cdot \kappa \cdot R3 \cdot C3^2 \cdot (T2 - R3 \cdot C3)}{K_{PD} \cdot K_{VCO} \cdot \sqrt{\kappa^2 + \gamma^2}} \quad \textbf{(43.146)}$$

$$B = \omega c \cdot \kappa \cdot R3 \cdot C3 - \omega c^2 \cdot (R3 \cdot C3)^2 \quad \textbf{(43.147)}$$

$$(T1 \cdot T3) = \frac{B - A^2 \pm A \cdot \sqrt{\kappa^2 \cdot (1 - A^2) + (B - 1)^2}}{\omega c^2 \cdot (1 - A^2)} \quad \textbf{(43.148)}$$

Symbol	Description	Value	Units
A	Calculated Value	1.0377×10^{-2}	n/a
B	Calculated Value	2.8310×10^{-2}	n/a
$\boldsymbol{T1 \cdot T3}$	Calculated Value	4.4170×10^{-12}	sec^2

$$A0 = \frac{R3 \cdot C3^2 \cdot (T2 - R3 \cdot C3)}{\frac{\kappa}{\omega c} \cdot R3 \cdot C3 - (T1 \cdot T3) - (R3 \cdot C3)^2} \quad \textbf{(43.149)}$$

$$C1 = \frac{A0 \cdot (T1 \cdot T3)}{T2 \cdot R3 \cdot C3} \quad \textbf{(43.150)}$$

$$C2 = A0 - C1 - C3 \quad \textbf{(43.151)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.152)}$$

Symbol	Description	Value	Units
A0	Loop Filter Coefficient	5.7699	nF
C1	Loop Filter Capacitor	0.1457	nF
C2	Loop Filter Capacitor	5.5242	nF
R2	Loop Filter Resistor	7.9156	kΩ

Passive Fourth Order Filter with C3, C4, R3, and R4 Fixed

Symbol	Description	Value	Units
BW	Loop Bandwidth	10	kHz
ϕ	Phase Margin	50	degrees
γ	Gamma Optimization Parameter	1	none
K_{PD}	Charge Pump Gain	5	mA
K_{VCO}	VCO Gain	20	MHz/V
f_{VCO}	Output Frequency	2450	MHz
ωc	Previously Calculated Value	62.382	kHz
κ	Previously Calculated Constant	0.3657	n/a
f_{PD}	Phase detector frequency	200	kHz
C3	Specified Loop Filter Capacitor	100	pF
C4	Specified Loop Filter Capacitor	100	pF
R3	Specified Loop Filter Resistor	40	kΩ
R4	Specified Loop Filter Resistor	40	kΩ

$$L = \left[R3 + \frac{\frac{1}{s \cdot C3} \cdot \left(R4 + \frac{1}{s \cdot C4} \right)}{\frac{1}{s \cdot C3} + \frac{1}{s \cdot C4} + R4} \right]_{s=j \cdot \omega c} \quad \textbf{(43.153)}$$

$$T = \left[\frac{1}{1 + s \cdot (C3 \cdot R3 + C4 \cdot R4 + C4 \cdot R3) + s^2 \cdot C3 \cdot C4 \cdot R3 \cdot R4} \right]_{s=j \cdot \omega c} \quad \textbf{(43.154)}$$

$$C = \frac{-1}{\omega c \cdot imag(L)} \quad \textbf{(43.155)}$$

$$R = Real \left[\frac{\frac{1}{T} - 1}{s \cdot C} \right]_{s=j \cdot \omega c} \quad \textbf{(43.156)}$$

Symbol	Description	Value	Units
L	Effective Load	49.8445 – j80.8146	kΩ
T	Effective Transfer Function	0.6478 – j0.5214	n/a
C	Equivalent Resistance at Loop Bandwidth	0.1969	nF
R	Equivalent Capacitance at Loop Bandwidth	60.9328	kΩ

First calculate the loop bandwidth to ensure that it is not larger than the specified value.

$$\omega c_{max}{}^3 + b2 \cdot \omega c_{max}{}^2 + b1 \cdot \omega c_{max} + b0 = 0 \quad \textbf{(43.157)}$$

$$b2 = -\frac{\gamma}{\kappa \cdot R3 \cdot C3} \quad \textbf{(43.158)}$$

$$b1 = -\frac{K_{PD} \cdot K_{VCO}}{\kappa \cdot N \cdot C3} \cdot \sqrt{\frac{\kappa^2 + \gamma^2}{1 + \kappa^2}} \quad \textbf{(43.159)}$$

$$b0 = \frac{K_{PD} \cdot K_{VCO}}{N \cdot R3 \cdot C3^2} \cdot \sqrt{\frac{\kappa^2 + \gamma^2}{1 + \kappa^2}} \quad \textbf{(43.160)}$$

Symbol	Description	Value	Units
b2	Calculated Value	-2.2896×10^5	Hz
b1	Calculated Value	-1.1389×10^{11}	Hz^2
b0	Calculated Value	3.4542×10^{15}	Hz^3
$\frac{\omega c_{max}}{2\pi}$	Maximum Attainable Bandwidth	4.5943	kHz

Now in this case, the maximum loop bandwidth is 4.5943 kHz, but the design was specified for 10 kHz. So both cases will be handled. First, try designing for 4.5943 kHz. In this case the following would be true.

$$C1 = 0 \quad \textbf{(43.161)}$$

$$A0 = \frac{K_{PD} \cdot K_{VCO}}{N \cdot \kappa \cdot \omega c_{max}} \cdot \sqrt{\frac{\gamma + \kappa^2}{1 + \kappa^2}} \quad \textbf{(43.162)}$$

$$C2 = A0 - C3 - C4 \quad \textbf{(43.163)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.164)}$$

Symbol	Description	Value	Units
A0	Calculated Value	26.9154	nF
C1	Loop Filter Capacitor	0	nF
C2	Calculated Value	26.7184	nF
R2	Loop Filter Resistor	3.5622	kHz

Let's now assume that this was not what was wanted and re-design for a loop filter bandwidth of 4 kHz to get around this limitation. This will shift R, C, and the maximum attainable bandwidth slightly. After using the same equations as before, the following results are obtained.

Symbol	Description	Value	Units
BW	Loop Bandwidth	4	kHz
L	Load of integrated components at loop bandwidth	49.9668 – j173.78	kΩ
T	Transfer function value of integrated components at loop bandwidth	0.9023 – j0.3168	n/a
C	Equivalent Filter Capacitance	0.1995	nF
R	Equivalent Resistance	60.1512	kΩ
b2	Coefficient for max loop bandwidth calculation	-2.2896×10^{5}	sec^{-1}
b1	Coefficient for max loop bandwidth calculation	-1.1242×10^{11}	sec^{-2}
b0	Coefficient for max loop bandwidth calculation	3.4099×10^{15}	sec^{-3}
$\frac{\omega c_{max}}{2\pi}$	Maximum Achievable Loop Bandwidth.	4.5915	kHz

$$T2 = \frac{\kappa}{\omega c} \tag{43.165}$$

$$T1 + T3 = \frac{\gamma}{\omega c \cdot \kappa} \tag{43.166}$$

$$A = \frac{\omega c^4 \cdot N \cdot \kappa \cdot R3 \cdot C3^2 \cdot (T2 - R3 \cdot C3)}{K_{PD} \cdot K_{VCO} \cdot \sqrt{\kappa^2 + \gamma^2}} \tag{43.167}$$

$$B = \omega c \cdot \kappa \cdot R3 \cdot C3 - \omega c^2 \cdot (R3 \cdot C3)^2 \tag{43.168}$$

$$(T1 \cdot T3) = \frac{B - A^2 \pm A \cdot \sqrt{\kappa^2 \cdot (1 - A^2) + (B - 1)^2}}{\omega c^2 \cdot (1 - A^2)} \quad \textbf{(43.169)}$$

Symbol	Description	Value	Units
T2	Calculated Value	1.0932×10^{-4}	sec
T1+T3	Calculated Value	1.4482×10^{-5}	sec
A	Calculated Value	3.8946×10^{-3}	n/a
B	Calculated Value	1.8813×10^{-2}	n/a
$T1 \cdot T3$	Calculated Value	2.3307×10^{-11}	sec^2

$$A0 = \frac{R3 \cdot C3^2 \cdot (T2 - R3 \cdot C3)}{\frac{\kappa}{\omega c} \cdot R3 \cdot C3 - (T1 \cdot T3) - (R3 \cdot C3)^2} \quad \textbf{(43.170)}$$

$$C1 = \frac{A0 \cdot (T1 \cdot T3)}{T2 \cdot R3 \cdot C3} \quad \textbf{(43.171)}$$

$$C2 = A0 - C1 - C3 \quad \textbf{(43.172)}$$

$$R2 = \frac{T2}{C2} \quad \textbf{(43.173)}$$

Symbol	Description	Value	Units
A0	Loop Filter Coefficient	35.9746	nF
C1	Loop Filter Capacitor	0.6392	nF
C2	Loop Filter Capacitor	35.1360	nF
R2	Loop Filter Resistor	3.1113	kΩ

Chapter 44 Switched and Multimode Loop Filter Design

Introduction

In some cases, the same PLL can be used to support multiple modes and frequencies. For instance, some VCOs have a band switch pin that change the frequency band in which they operate. Another example would be a cellular phone that needs a loop filter that supports both the CDMA and AMPS standards. The phase noise, spur, and lock time requirements may be drastically different for these different standards. In general, there are two types of situations. For the first type of situation, there is no need to switch in additional components and the VCO frequency or phase detector frequency is changing, but the desire is to keep the loop bandwidth the same. For the second situation, drastically different loop bandwidths are required and it is necessary to switch in components.

Supporting Multiple Modes with the Same Bandwidth and No Component Switching

Loop Gain Constant

The concept used in many switched and multimode filters is the *loop gain constant*.

$$K = \frac{K_{PD} \cdot K_{VCO}}{N} \tag{44.1}$$

If the loop gain constant is held the same, and the loop filter components are not changed, then the phase margin, loop bandwidth, gamma optimization factor, and pole ratios will all remain unchanged. This is a strategy if the loop bandwidth is to remain about the same.

The No Work Switched Filter

This situation is where the filter is used for two or more different means, but no adjustments need to be made. One common situation might be where two different VCO frequencies are used and the change in the N value tracks the VCO gain. In other cases, it might be that the requirements are lax enough that it is not necessary to go through additional effort. If considering using this approach, the second order loop filter is often a good choice because it is more resistant to changes in the loop gain.

The No Switched Component Filter

In this situation, the charge pump setting can be programmed to different settings to account for differences in the N divider value, VCO gain, or phase detector frequency. For instance, consider an integer PLL with the same VCO with one application that uses a 3 MHz phase detector and another that uses a 5 MHz phase detector frequency. In this situation, one could make the ratio of the charge pump currents 3:5 and this would balance the loop gain constant. In other words one could use a charge pump current of 3 mA with the 5 MHz phase detector frequency and 5 mA with the 3 MHz phase detector frequency. In this case, the loop bandwidth is the same for both applications.

Supporting Multiple Loop Bandwidths and Switching in Components

Using the Fastlock Resistor for Switched Filters

Fastlock can be used to switch in a wider loop bandwidth when the PLL is changing frequencies, and then a narrower one when the frequency is closed to the final value. Aside from this application, it can be also used in situations where there are multiple modes that need a drastically different loop bandwidth. In this case, the loop gain constant changes too much to not switch in any additional components. Switching in a Fastlock resistor in parallel with ***R2*** serves as a quick remedy. In this case, the loop bandwidth may change, but the loop filter stays optimized. Fastlock has been discussed in depth in another chapter.

The Full Switched Mode Filter

For this case, a new filter is switched in parallel with the old filter. The most common strategy for using this method is to have one filter with a faster lock time requirement, and one with a slower lock time requirement. For the mode with fast lock time, the other filter is not switched in. For the mode with the slower lock time and better spectral performance, a second loop filter is switched in with components that swamp out the other components.

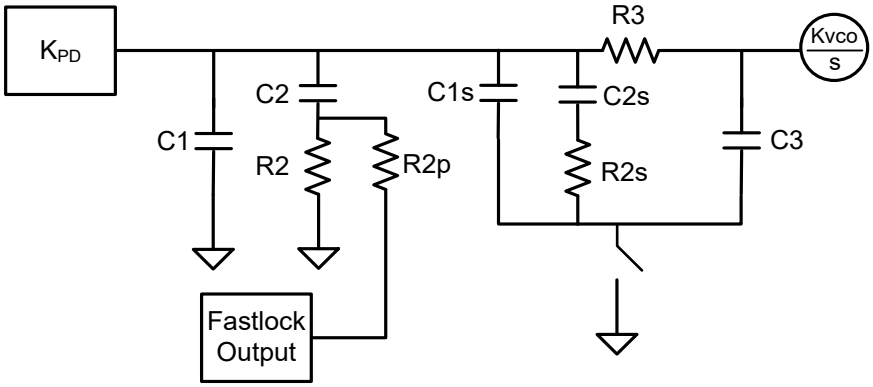


Figure 44.1 *Full Switched Loop Filter*

The strategy with this loop filter design is first to design ***C1***, ***C2***, ***R2***, and ***R2***p (Fastlock Resistor) for the mode with fast switching speed. The impact of all the other components is negligible because the switch to ground is off. The components ***C3***, ***C1s***, ***C2s***, and ***R2s*** add in parallel to ***R3*** in order to reduce the resistor noise due to this component. In the mode with the narrower loop bandwidth, the switch to ground is on and ***R3*** and ***C3*** form the extra pole for the filter.

Once the filter is designed for the fast mode, then another traditional filter is designed for the slow switching mode. Denote these components with the 'd' suffix. So, ***R2d*** is the desired component value in slow mode for a non-switched filter. When the switch is grounded, ***C1*** and ***C1s*** add together. The transfer function formed by ***C2***, ***C2s***, ***R2***, and ***R2s*** is as follows:

$$Z(s) = \frac{1 + s \cdot (C2 \cdot R2 + C2s \cdot R2s) + s^2 \cdot C2 \cdot C2s \cdot R2 \cdot R2s}{s \cdot (C2 + C2s) + s^2 \cdot C2 \cdot C2s \cdot (R2 + R2s)} \quad \textbf{(44.2)}$$

By observing the numerator, it should be apparent that the final transfer function will have a factor of s^2. Because of this, there is no hope of achieving the exact transfer function. Looking at the first term in the denominator, it can be seen that ***C2*** and ***C2s*** add to make ***C2d***. For ***R2***, the middle term should resemble ***R2d*·*C2d***. Now the ***C2*·*R2*** makes the calculated value for ***R2s*** smaller, but the s^2 term would make this smaller. Because these are both second order effects and they roughly cancel out, they can both be neglected. In practice, this approximation seems to work reasonably well. As for ***R3s*** and ***C3s***, all the calculations have been made so far to make the second order part of the loop filter as close as possible, so it makes sense to make these equal to their design target values. Applying all of these concepts, the switched components can be solved for.

$$C1s = C1d - C1 \quad \textbf{(44.3)}$$

$$C2s = C2d - C2 \quad \textbf{(44.4)}$$

$$C3s = C3d \quad \textbf{(44.5)}$$

$$R2s = \frac{R2d \cdot C2d}{C2s} \quad \textbf{(44.6)}$$

$$R3s = R3d \quad \textbf{(44.7)}$$

Note that the way that these switched component values are calculated is by calculating what the equivalent impedance of the loop filter would be with the components switched together and then solving for the switched values. For instance, capacitor ***C1*** and ***C1s*** add to get ***C1d***. From this, it is easy to solve for ***C1s***. Some coarse approximations have been used, so there could definitely be some benefit to tweaking the components manually.

Example of a Full Switched Filter

Symbol	Units	Fast Filter	Ideal Slow Filter	Switched Components for Slow Filter
f_{OUT}	*MHz*	1930-1990	1392 (Fixed Frequency)	
f_{PD}	*kHz*	50	60	
K_{PD}	*mA*	1	4	
K_{VCO}	*MHz/V*	60	30	
N	*n/a*	39200	23200	
BW	*kHz*	10.0	2.0	1.9
ϕ	*Deg.*	50.0	50.0	48.9
γ	*n/a*	1.1	1.1	
T3/T1	*%*	0	50	
C1, C1d, C1s	*nF*	0.58494	5.86096	5.27602
C2, C2d, C2s	*nF*	3.83824	91.17890	87.34066
C3d, C3s	*nF*		0.75962	0.75962
R2, R2d, R2s	*kΩ*	23.9181	2.56228	2.67488
R2p	*kΩ*	23.9181		
R3d, R3s	*kΩ*		18.57557	18.57557

Table 44.1 *Full Switched Filter Example*

Conclusion

Switched filters are useful in situations where the loop filter is to be used under two different conditions. In some cases, it is not necessary to switch in additional components. However, if the requirements of the loop filters are much different, then it might be necessary. Also, there can be times when the requirements for two different modes may be different. Usually, this means that there is one mode that has a faster lock time requirement, and another mode that has a more stringent spur requirement.

Chapter 45 Rounding Techniques for Loop Filter Components

Introduction

One real world issue that will come up when the component values are found is how to round them to standard component values. The most natural method might be to individually round each component to the closest standard value, but there is a better way to get closer to the desired design parameters. This chapter discusses standard component values and this improved method of rounding component values.

EIA Standard Values and Common Component Stocking

The EIA (Electronic Industries Association) standard divides each decade into a prescribed number of values per decade of 6 (E6), 12 (E12), 24 (E24), 48 (E48), 96 (E96), or 192 (E192) values per decade. For practical purposes, it is common to stock only E12 values for resistors and capacitors. When the values start getting bigger, then sometimes only E6 values are stocked. The common E24 and sub families of this are shown in the table below:

	E6	E12	E24
Values/Decade	6	12	24
Theoretical Ratio	1.468	1.212	1.101
Tolerance	20%	10%	5%
Values	1	1	1
			1.1
		1.2	1.2
			1.3
	1.5	1.5	1.5
			1.6
		1.8	1.8
			2
	2.2	2.2	2.2
			2.4
		2.7	2.7
			3
	3.3	3.3	3.3
			3.6
		3.9	3.9
			4.3
	4.7	4.7	4.7
			5.1
		5.6	5.6
			6.2
	6.8	6.8	6.8
			7.5
		8.2	8.2
			9.1

Table 45.1 *Standard E24 and Smaller Values*

Comparison of Rounding Methods

Simple Rounding Method

The simple method of rounding loop filter components is to simply round every component value to the closest standard value. The advantages of this technique are that it is simple, independent of loop filter type, and the calculated component values will always be positive. These advantages come at the cost the loop filter being farther off from the design target than necessary.

Advanced Rounding Method

The advanced rounding method involves choosing components in a sequential order in order to try to get as close the design targets for the filter zero (T2) and loop filter coefficients (A0,A1,A2, and A3). After each component is chosen, the next target value is chosen to try to make the loop filter coefficients as close as possible. For notational purposes, an "a" will be added to each component value to indicated the rounded value. For instance, "C1" is the ideal value and "C1a" is the rounded value. The function "Round" is introduced to mean to round to a standard value. There are multiple ways to approach this problem, but one method that makes a reasonable trade-off between accuracy and complexity is as follows:

1. Choose loop filter component C2a as close to C2 as possible. The reasoning for choosing C2 first is that this dominates the filter coefficient A0.

$$C2a = Round\{\ C2\ \} \tag{45.1}$$

2. Choose loop filter component R2a to make T2 as close to value as possible. In other words, choose R2a to be as close to T2/C2a as possible.

$$R2a = Round\left\{\ \frac{C2 \cdot R2}{C2a}\ \right\} \tag{45.2}$$

3. The method differs based on filter order and filter type, but ideal strategy would be to get the ratio of A1/A0 as close to the design target as possible, as this would be the sum of the poles. For the second order filter, there is a nice formula for this. For higher order filters, other decision criteria are used to simplify the calculations.

These steps apply to the passive filter. In the case of the active filter, the first two steps are the same, but the third step will involve choosing the components to get the poles T1, T3, and T4 as close to the target values as possible. In general, the added isolation from the op-amp simplifies the calculations.

Rounding Methods for the Second Order Filter

For the second order method, the steps are easy and never lead to negative component values. The value that gets the ratio of A1/A0 as close to the design target is as follows.

$$C1a = Round\left\{\frac{C1}{C2} \cdot C2a\right\} \tag{45.3}$$

Parameter	Units	Ideal Components	Simple Method	Advanced Method
K_{PD}	*mA*	1		
K_{VCO}	*MHz/V*	35		
N	*n/a*	150		
BW	*kHz*	20	20.95	21.72
ϕ	*Degrees*	50	48.10	51.02
γ	*n/a*	1	1.27	1.17
C2	*nF*	35.21872	33	33
R2	*kΩ*	0.6208	0.68	0.68
C1/C2	*n/a*	0.1527	0.1697	0.1424
C1	*nF*	5.37803	5.6	4.7

Table 45.2 *Advanced Rounding Method Example for a Second Order Filter Assuming Resistor and Capacitor in Steps of 10%*

Table 45.2 shows an example of rounding components to the nearest 10% value. In this case, even though components do not come with a 10% tolerance, it is a very common practice to order 5% components and stock every other value. The effect of this is the same as having standard 10% values. These values are a power of ten multiplied by one of the following values: 1.0, 1.2, 1.5, 1.8, 2.2, 2.7, 3.3, 3.9, 4.7, 5.6, 6.8, or 8.2. For the case of the simple method, the components were simply rounded to the nearest value.

Rounding Methods for the Third order Filter

Advanced Method

The components C2a and R2a are found as usual.

$$C2a = Round\{C2\} \tag{45.4}$$

$$R2a = Round\left\{\frac{T2}{C2a}\right\} \tag{45.5}$$

The next step involves finding C1a then C3a. It is possible, however unlikely, that the rounding error could cause C3a to be negative. If this is the case, then the best approach is to just find C1a, C3a, and R3a using the simple rounding method. The first step is to find the product of R3 and C3 (R3tC3) as it would be calculated from C2a and R2a. The derivation for this is in the appendix.

$$C3tR3 = \frac{A1 - C2a \cdot R2a \cdot (A0 - C2a) - \frac{A2}{C2a \cdot R2a}}{C2a} \tag{45.6}$$

Once this is known, C1a, C3a, and R3a can be found.

$$C1a = Round\left\{\frac{A1}{C3tR3 \cdot C2a \cdot R2a}\right\} \tag{45.7}$$

$$C3a = Round\{A0 - C1a - C2a\} \tag{45.8}$$

$$R3a = Round\left\{\frac{C3tR3}{C3a}\right\} \tag{45.9}$$

Parameter	Units	Ideal Components	Simple Method	Advanced Method
K_{PD}	*mA*	1		
K_{VCO}	*MHz/V*	35		
N	*n/a*	150		
BW	*kHz*	20	19.58	19.86
ϕ	*Degrees*	50	49.69	50.19
γ	*n/a*	1	0.96	0.96
T3/T1	*%*	20	19.56	20.9
C2	*nF*	38.28894	39	39
R2	*kΩ*	0.57741	0.56	0.56
C3tR3	*s*	1.08649×10^{-6}	1.23×10^{-6}	1.51539×10^{-6}
C1	*nF*	1.97892	1.8	1.5
C3	*nF*	1.44671	1.5	1.2
R3	*kΩ*	0.75101	0.82	1.2

Table 45.3 *Advanced Rounding Method Example for a Third Order Filter Assuming Resistor and Capacitor Steps of 10%*

Rounding Methods for Fourth Order Filter

Recall the equations for the fourth order filter passive filter coefficients.

$$A0 = C1 + C2 + C3 + C4 \tag{45.10}$$

$$A1 = C2 \cdot R2 \cdot (C1 + C3 + C4) + R3 \cdot (C1 + C2) \cdot (C3 + C4) + C4 \cdot R4 \cdot (C1 + C2 + C3) \tag{45.11}$$

$$A2 = C1 \cdot C2 \cdot R2 \cdot R3 \cdot (C3 + C4) + C4 \cdot R4 \cdot (C2 \cdot C3 \cdot R3 + C1 \cdot C3 \cdot R3 + C1 \cdot C2 \cdot R2 + C2 \cdot C3 \cdot R2) \tag{45.12}$$

$$A3 = C1 \cdot C2 \cdot C3 \cdot C4 \cdot R2 \cdot R3 \cdot R4 \tag{45.13}$$

The components C2a and R2a are found as usual.

$$C2a = Round\{C2\} \tag{45.14}$$

$$R2a = Round\left\{\frac{T2}{C2a}\right\} \tag{45.15}$$

As the equations can be complicated, a fair compromise is to use simple rounding for C3, C4, and R4.

$$C3a = Round\{C3\} \tag{45.16}$$

$$C4a = Round\{C4\} \tag{45.17}$$

$$R4a = Round\{R4\} \tag{45.18}$$

Once these are known, C1a can be easily solved for using (45.10).

$$C1a = Round\{A0 - C2a - C3a - C4a\} \tag{45.19}$$

R3a can be solved for by rearranging (45.11).

$$R3a = Round\left\{\frac{A1 - C2a \cdot R2a \cdot (C1a + C3a + C4a) - C4a \cdot R4a \cdot (C1a + C2a + C3a)}{(C1a + C2a) \cdot (C3a + C4a)}\right\} \quad \textbf{(45.20)}$$

Parameter	Units	Ideal Components	Simple Method	Advanced Method
K_{PD}	*mA*	1		
K_{VCO}	*MHz/V*	35		
N	*n/a*	150		
BW	*kHz*	20	19.83	19.78
ϕ	*Degrees*	50	50.22	49.41
γ	*n/a*	1	0.95	0.99
T3/T1	*%*	20	20.91	20.78
T4/T3	*%*	20	19.81	21.12
C2	*nF*	38.98098	39	39
R2	*kΩ*	0.56671	0.56	0.56
C4	*nF*	1.04502	1	1
R4	*nF*	0.73196	0.68	0.68
C3	*nF*	0.38527	0.39	0.39
C1	*nF*	1.38357	1.5	1.5
R3	*kΩ*	0.45861	0.47	0.56

Table 45.4 *Fourth Order Passive Filter Example with Component Rounding*

With the advanced rounding method, maybe the values are closer, especially for Gamma, but it is very close.

Conclusion

One reality of loop filter design is dealing with standard component values. The simple method is the most intuitive way and involves rounding each component to the closest standard value. A better method is to round off components in a more systematic order so as to try to keep the loop filter coefficients as close to the desired value as possible. Both of these methods were presented. For the avid reader, one could come up with more sophisticated methods to try even harder to keep the loop filter coefficients the same, but these do not always perform that much closer to the design values and they also introduce complexity and the possibility of the method yielding negative component values. If this ever happens with one of these more sophisticated methods, then just revert back to the simple method.

Appendix Derivations for Filter Rounding Methods

Method for C2 and R2

This section derives the equations for rounding for the 2nd, 3rd, and 4th order filters. This assumes passive filters, but similar logic can be used to derive equations for active filters. Regardless of the filter order or if it is active or passive, T2, is always calculated the same.

$$T2 = C2 \cdot R2 \tag{45.21}$$

For every technique, we choose C2a to be as close to C2 as possible. Therefore:

$$R2a = Round\left\{ \frac{C2 \cdot R2}{C2a} \right\} \tag{45.22}$$

Also recall that:

$$A1 = A0 \cdot (T1 + T3 + T4) \tag{45.23}$$

In other words, by choosing the ratio of A1/A0 to be as close as possible to the design target, this gets the sum of the poles as close to the design target as possible.

Second Order Loop Filter

Recall the loop filter coefficients for a passive filter.

$$A0 = C1 + C2 \tag{45.24}$$

$$A1 = C1 \cdot C2 \cdot R2 \tag{45.25}$$

The ratio of these is as follows:

$$\frac{A1}{A0} = \frac{C1 \cdot C2 \cdot R2}{C1 + C2} = \frac{R2}{\left({}^{C1}/_{C2}\right) + \frac{1}{\left({}^{C1}/_{C2}\right)}} \tag{45.26}$$

In other words, if one chooses C1 to make C1a/C2a as close to the design target of C1/C2, then this will get the pole, T2, as close to target value as possible. This yields the following equation for C1a.

$$C1a = Round\left\{ \frac{C1}{C2} \cdot C2a \right\} \tag{45.27}$$

Third Order Loop Filter
Recall the loop filter coefficients for a passive filter.

$$A0 = C1 + C2 + C3 \tag{45.28}$$

$$A1 = C2 \cdot R2 \cdot (C1 + C3) + C3 \cdot R3 \cdot (C1 + C2) \tag{45.29}$$

$$A1 = C1 \cdot C2 \cdot C3 \cdot R2 \cdot R3 \tag{45.30}$$

As C2 and R2 are known, (45.28) can be used to find the sum of C1 and R3 and (45.30) can be used to find the product of C1, C3, and R3. Substituting this into (45.29), using the known values of C2a and R2a, and simplifying yields the following result.

$$C3tR3 = \frac{A1 - C2a \cdot R2a \cdot (A0 - C2a) - \frac{A2}{C2a \cdot R2a}}{C2} \tag{45.31}$$

Substitution into (45.30) yields the expression for C1.

$$C1a = Round\left\{\frac{A1}{C3tR3 \cdot C2a \cdot R2a}\right\} \tag{45.32}$$

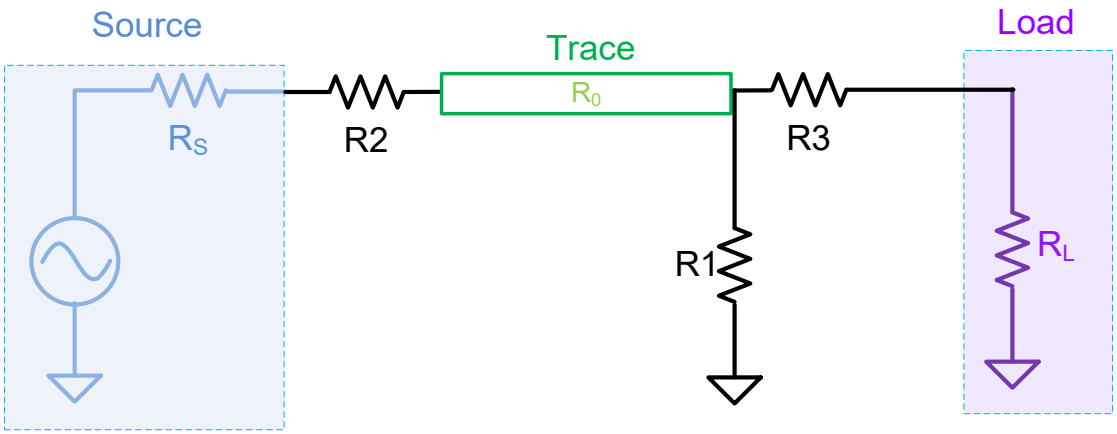
C3 can be found through (45.28).

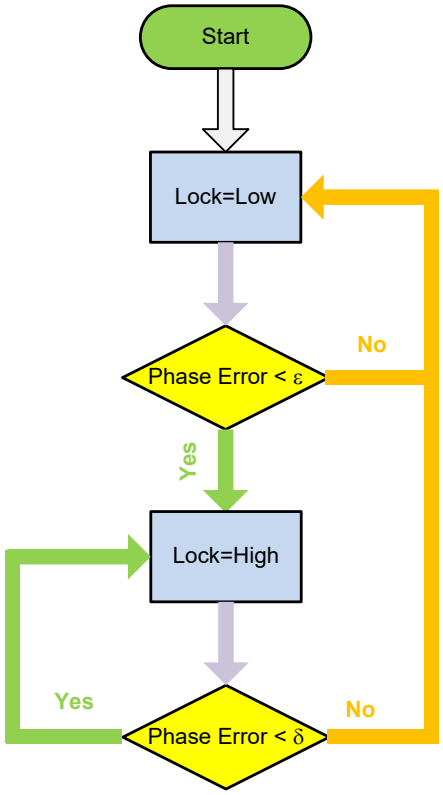
$$C3a = Round\{A0 - C1a - C2a\} \tag{45.33}$$

R3 is found by simple division.

$$R3a = Round\left\{\frac{C3tR3}{C3a}\right\} \tag{45.34}$$

Additional Topics





Chapter 46 PLL Lock Detect

Introduction

The ability for a PLL to reliably indicate when it is in lock is critical for many applications. An ideal lock detect circuit gives a high indication when the PLL is locked and a low indication when the PLL is unlocked. Although this may seem like a simple task, the problem of a PLL determining when it is in lock can actually be fairly complicated. Lock detect has several different types and has evolved over the years. The four lock detect methods discussed in this chapter will be nicknamed *Analog*, *Digital*, *Vtune*, and *Calibration Status*.

Type	Output	Lock Detect Basis
Analog	Pulse width modulated signal.	Charge pump on time
Digital	Logic high or low	Error at phase detector
Vtune	Logic High/Low	VCO tuning voltage
Calibration Status	Logic High/Low	VCO calibration finished

Table 46.1 *Lock Detect Types*

Analog Lock Detect

How it works

The first type of lock detect to come along was the analog lock detect. This works by creating a signal that is mostly high with a series of low pulses with a period corresponding to when the charge pump is coming on. When the PLL goes out of lock, the width of these pulses gets wider.

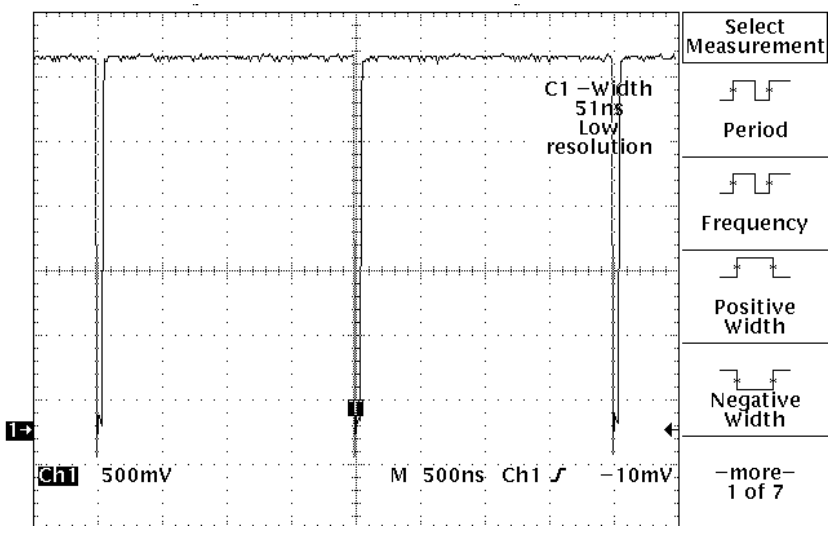


Table 46.2 *Typical Lock Detect Pin Output for Analog Lock Detect*

The user creates a circuit that integrates the width of these negative pulses and converts this signal into a logic low or high signal. The construction and simulation of this circuit depends on the width of these low pulses in both the locked and unlocked condition and is discussed in the appendix. The information concerning the PLL in or out of the locked state is in no individual pulse, but rather in the average pulse width.

Estimating the Pulse Width of the Analog Lock Detect Circuit

Although the pulses can sometimes be sort of triangular due to the turn on times of transistor, they can be approximated as rectangular for the sake of simplicity. The width of these pulses varies between the locked and unlocked conditions.

In the locked condition, the width of the pulses is application specific and can also vary with the PLL being used. One example for these pulses in locked condition is the LMX2485 family which has pulses on the order of 25-70 ns. The width of these pulses can vary based on many factors. One such factor is the charge pump current; for higher charge pump currents, the pulse width tends to be narrower. They can also vary over temperature, charge pump mismatch, charge pump leakage, and process.

When the PLL is the unlocked state, the width of the pulses can vary based on the situation. First consider the situation where the PLL is trying to force the VCO to a frequency that it cannot go. In this case, N and R divider outputs will be different frequency and therefore have a rolling phase. Imagine this first as the divider outputs starting in phase. In this case, the width of the first negative pulse would simply be just the difference in the periods of the two counter outputs. The width at each phase detector period will increase until the phase error exceeds one full cycle and then it resets. In this case, the average low period of the lock detect circuit would be half the phase detector period. The other scenario for the PLL in the unlocked state would be when the PLL is able to track the VCO frequency. In this case, the first pulse width would again be the difference of the periods of the N and R divider outputs. The width of the next pulse might be similar if the PLL was able to track it. So in general, one can assume the following about the low time of the lock detect signal.

$$T_{LowUnlock} = \begin{cases} \dfrac{1}{2 \cdot f_{PD}} & PLL\ Not\ Tracking\ VCO \\ \left| \dfrac{1}{f_{PD}} - \dfrac{N}{f_{VCO}} \right| & PLL\ is\ Tracking\ VCO \end{cases} \quad \textbf{(46.1)}$$

(46.1) is based on somewhat bold assumptions and is intended to give only a rough approximation; it is always best to verify the pulse width through direct measurement.

Advantages and Disadvantages

The key disadvantage of analog lock detect is that it requires external circuitry to convert the pulse stream to a logic low or high. If all that is really desired is a circuit to determine if the VCO is slammed against the rail, then this circuit is not too difficult. However, if it is desired to have something that is a little more sensitive, then the construction of this circuit is sort of a science experiment as it depends on comparing the width of these negative pulses when the device is out of lock and also is specific to the family of device.

The advantages of the analog lock detect is that the user has the ability to tune it to just what they want, it is hard to fool by abruptly removing the input reference, and it has no problems with higher phase detector frequencies or fractional modulation.

Digital Lock Detect

Overview

The undesired requirement of extra components and challenges with pulse width estimation for the analog lock detect were likely motivators for invention of digital lock detect. Digital lock detect works by looking at the phase error at the phase detector at each phase detector cycle output of the R divider as shown in the flowchart below.

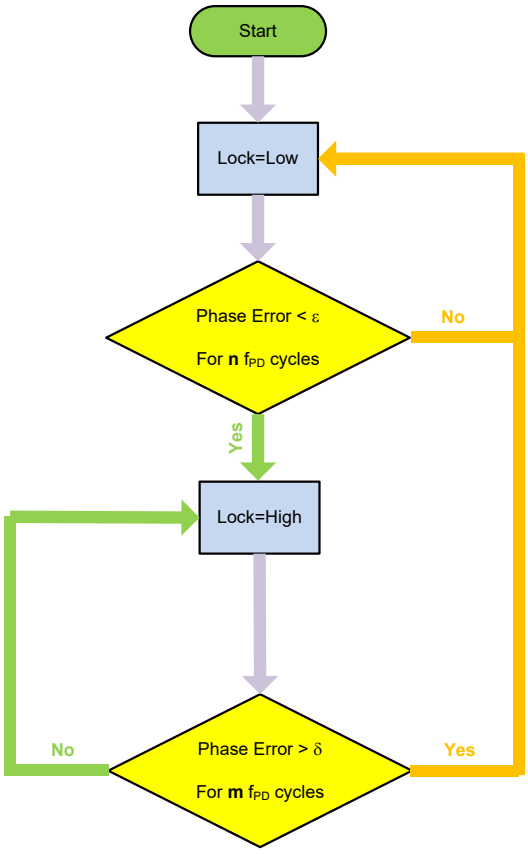


Figure 46.1 *Digital Lock Detect Flowchart*

The circuit starts with indicating the unlocked condition. After there have been n phase detector cycles with less than a phase error of ε, then the circuit indicates a locked condition. Once the circuit is in the locked condition, it will stay in that state until there are m phase detector cycles with a phase error greater than δ. For example, the LMX2306 was one of the first PLLs to have this kind of digital lock detect. This PLL would indicate a locked condition when there were 3 to 5 (user programmable) phase detector cycles with a phase error of less than 15 ns. Then once the PLL was locked, it would require a single phase error of greater than 30 ns to cause the circuit to indicate an unlocked condition.

As phase detector frequencies became higher, the values for ε and δ became smaller to accommodate this. For instance, if the phase detector frequency is 200 MHz, then this works out to a period of 5 ns, so clearly ε would need to be much less than this. With the rise of fractional N PLLs, this presented more challenges as the fractional modulation would introduce errors at the phase detector. In this case, it started to become necessary to make $m>1$ to accommodate this as done in such devices as the LMX2581.

Digital Lock Detect Issues with Loss of Reference and OSCin Pin Self-Oscillation

The nemesis of digital lock detect has always been detecting the condition when the input reference goes away. The reason why this is problematic is that the input reference drives the phase detector frequency, which is the state machine for the lock detect circuit. If this state machine clock goes away, then the PLL could be initially in a locked condition and then the input frequency could abruptly go away and then the lock detect circuit improperly indicate that the PLL is locked.

The additional factor that has caused tremendous confusion with this loss of reference condition is the potential self-oscillation of the OSCin pin. When there is no input signal present at the OSCin pin, then it can often self-oscillate. In this case, there is state machine clock and the digital lock detect will properly detect the loss of the input frequency. As self-oscillation property varies over devices, process, voltage and temperature, it can distract away from the fundamental issue of not having an input reference.

Vtune Lock Detect

As the challenges of loss of input reference, higher phase detector frequencies, and fractional PLLs put more challenges on the digital lock detect, another form of lock detect came along. This Vtune lock detect simply measures the voltage at the VCO input (Vtune) and gives a logic high or low indication based on whether it is within a certain range or not. This lock detect is simple and works for the loss of reference condition, but tends to be less sensitive. Sometimes this can be used in addition to analog lock detect for a more reliable lock detect indication.

Calibration Status Lock Detect

Yet another type of lock detect that has come about is the calibration status style. For this lock detect, the circuit indicates low when the VCO is calibrating and then indicates high when the calibration is finished. A delay can be added to this to allow for the analog settling time of the PLL. This lock detect is very simple, but it will not correctly indicate an unlock condition if the PLL ever does go out of lock after the calibration has finished. Aside from giving a lock detect indication, the calibration status lock detect can also sometimes be used as a diagnostic to measure the VCO digital calibration time in the case of integrated VCOs.

Conclusion

The problem of getting the PLL to properly tell when it is or is not in a locked condition is a key function. Although it seems like a simple problem, it has had its challenges and lock detect circuits have evolved through the years.

Appendix: Construction and Simulation of Analog Lock Detect Circuit

Lock Detect Circuit Construction

The basic strategy for the lock detect circuit is to integrate over some number of phase detector periods in order to accumulate a DC value which can then be compared to a threshold value. This comparison can be made with a comparator or transistor. In cases where only a gross lock detect is needed, the lock detect circuit output can be sent directly to the input logic gate, provided the difference in the voltage level produced between the in lock and out of lock conditions is large enough to be recognized as a high or low. Some microprocessors also have A/D input pins that can also be used for this function.

When a more sensitive lock detect circuit is needed, it may be necessary to use unbalanced time constants to maximize sensitivity as the average DC contributions of the pulses are small relative to the rest of the time. The recommended circuit is shown in Figure 46.2. Note that there are some PLLs in which the lock detect output is open drain, which eliminates the need for the diode and increases the sensitivity of the circuit by making V_D = 0. There are still other PLLs with digital lock detect, that eliminate the need for a lock detect circuit entirely.

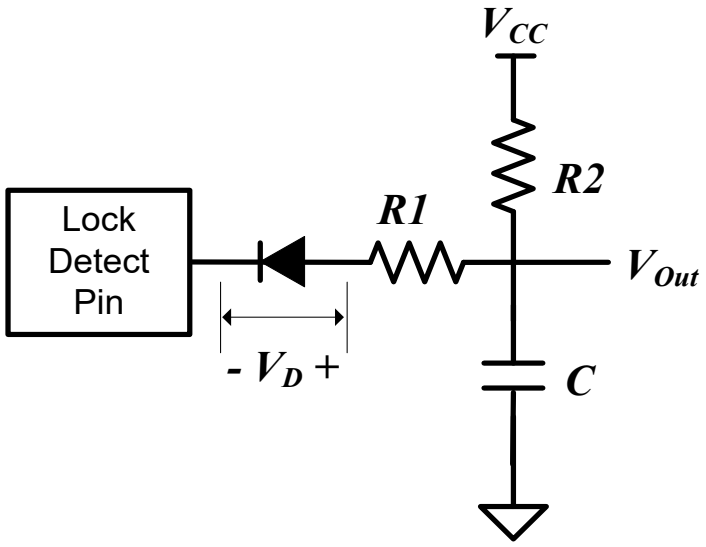


Figure 46.2 *Lock Detect Circuit*

Theoretical Operation of the Lock Detect Circuit

Consider the event when the lock detect pin first goes to its low voltage. The voltage drop across the diode is V_D. The diode will conduct, and if *R2 >> R1* then the following holds:

$$V_{out} = -R1 \cdot C \cdot \frac{dV_{out}}{dt} \qquad \textbf{(46.2)}$$

The main interest is the amount that the voltage V_{out} changes during the period that the lock detect pin is low. To simplify the mathematics, it is easiest to discretize the problem. The size of the discrete time step is T_{Low}, which is the time which the lock detect pin stays low. This applies to both cases when the PLL is out of lock and when it is in lock. The following definitions can be used to convert the differential equation into a difference equation:

$$V_n = V_{out}(0) \tag{46.3}$$

$$V_{n+1} = V_{out}(T_{Low}) \tag{46.4}$$

The above difference equations have the following solution:

$$V_{n+1} = V_D + (V_n - V_D) \cdot \beta \tag{46.5}$$

$$\beta = e^{\left(\frac{-T_{Low}}{R1 \cdot C}\right)} \tag{46.6}$$

When the lock detect output goes high, then the diode will not conduct, and the capacitor will charge through the resistor ***R2***. In an analogous way that was done for the case of the lock detect pin state being low, the results can also be derived for the case when the lock detect pin is high. In this case, T_{High} represents the time period that the lock detect pin stays high.

$$V_{n+1} = V_{CC} + (V_n - V_{CC}) \cdot \alpha \tag{46.7}$$

$$\alpha = e^{\left(\frac{-T_{High}}{R2 \cdot C}\right)} \tag{46.8}$$

Now if one considers the two cases for V_n, then a general expression can be written for V_n. For sufficiently large n, the series will alternate between two steady state values. Call these two values V_{High} and V_{Low}. These values can be solved for by realizing that the initial voltage when the lock detect pin just goes low will be V_{High} and the final voltage will be V_{Low}. Also, the initial voltage when the lock detect pin just goes high will be V_{Low} and the final voltage will be V_{High}.

This creates a system of two equations and two unknowns.

$$V_{Low} = V_D + (V_{High} - V_D) \cdot \beta \quad \textbf{(46.9)}$$

$$V_{High} = V_{CC} + (V_{Low} - V_{CC}) \cdot \alpha \quad \textbf{(46.10)}$$

This system of equations has the following solution:

$$V_{Low} = V_{CC} + \frac{(1 - \beta) \cdot (V_D - V_{CC})}{1 - \alpha \cdot \beta} \quad \textbf{(46.11)}$$

$$V_{High} = V_D + \frac{(1 - \alpha) \cdot (V_{CC} - V_D)}{1 - \alpha \cdot \beta} \quad \textbf{(46.12)}$$

Lock Detect Circuit Design

The above expressions for V_{Low} and V_{High} show what two values the voltage will oscillate between, once the component values are known. This is based on the assumption that T_{High} and T_{Low} do not change. For the purposes of designing a lock detect circuit, these parameters actually need to be considered in two cases. One case is when the PLL is locked, and the other is when the PLL is unlocked with the minimum detectable frequency error. For design of the circuit, the following information is needed.

V_{CC} This is the voltage supply to the lock detect circuit.

V_D This is the voltage drop across the diode. It is zero for an open drain lock detect output, since the diode is omitted in this case.

$V_{HighUnlock}$ This is the highest voltage the circuit should achieve when the PLL is unlocked. Therefore, this is the low trip point. Below this voltage, output is considered to be low. It may turn out that this low trip point is not really as low as a voltage as desired, however, it must satisfy the constraint that $V_{HighUnock} < V_{LowLock}$. If the circuit is intended to be very sensitive, this may only be a few hundred millivolts below $V_{LowLock}$. In this case, a comparator or low speed A/D converter could be used to interpret this voltage as an indication of lock or unlock.

$V_{LowUnlock}$ This is the lowest voltage the circuit should be when the PLL is unlocked. This must be less than $V_{HighUnlock}$. The lower this is chosen, the more sensitive the circuit will be, but the noisier the lock detect output will be as well. For maximum sensitivity, choose this equal to VD.

$T_{HighUnlock}$ This is the time the lock detect output is high for the PLL in the unlocked state.

$T_{LowUnlock}$ This is the width of the LD pulses that are to be detected in the unlocked condition.

C This is the value of the capacitor in the circuit that can arbitrarily be chosen.

The parameter α depends on the parameters T_{High}. Although this parameter does change slightly between the locked and unlocked conditions, the change is small enough to assume that this parameter is a constant. Using the expressions for V_{High} and V_{Low} in equations (46.11) and (46.12), the following equations can be derived.

$$\alpha = \frac{V_{CC} - V_{HighUnlock}}{V_{CC} - V_{LowUnlock}} \tag{46.13}$$

$$\beta = \frac{V_{LowUnlock} - V_D}{V_{HighUnlock} - V_D} \tag{46.14}$$

Finally, the components can be solved for. To do so, the capacitor, C, can be chosen arbitrarily. Once C is known, the other components can also be found.

$$R1 = \frac{-T_{LowUnlock}}{C \cdot \ln(\beta)} \tag{46.15}$$

$$R2 = \frac{-T_{HighUnlock}}{C \cdot \ln(\alpha)} \tag{46.16}$$

Parameter	Value	Units
V_{CC}	4.1	Volts
V_D	0.7	Volts
$V_{HighUnlock}$	2.1	Volts
$V_{LowUnlock}$	2	Volts
$T_{HighUnlock}$	945	ns
$T_{LowUnlock}$	55	ns
C	680	pF

Table 46.3 *Specified Parameters*

Parameter	Value	Units
α	0.9524	n/a
β	0.9286	
$R1$	1.0914	kΩ
$R2$	28.4833	kΩ

Table 46.4 *Calculated Results*

Simulation

After the design is done, it is necessary to assure that the lowest voltage in the locked state ($V_{LowLocked}$) is higher than the highest voltage unlocked condition ($V_{HighUnlocked}$). For the circuit specified in Table 46.3 and Table 46.4, the results are given. The simulation shows that in twenty reference cycles, the circuit gets reasonably close to its final steady state values. When the PLL is in lock, the lock detect circuit output voltage will not go below 2.54 Volts; in the unlocked state, the output voltage will not go above 2.10 Volts. This may not seem like much voltage difference, but this is because this circuit is extremely sensitive. If one was to use a pulse width of 100 ns out of lock, then this voltage difference would be much greater.

In practice, is necessary to include a lot of margin for error, since it is very difficult to get an accurate idea of the width of the negative pulses from the lock detect pin. It was also assumed that these pulses were square and of constant period, which may be a rough assumption. Furthermore, as shown in Figure 46.3, it does take time for the system to settle down to its final state. Although not directly stated, the phase detector frequency can be inferred to be 1 MHz from the low and high times.

Calculated Parameters					
Voltages			***Constants***		
$V_{LowLocked}$	2.6774	Volts	α	0.9524	n/a
$V_{HighUnlocked}$	2.1000		$\beta_{Unlocked}$	0.9286	
$V_{LowUnlocked}$	2.0000		β_{Locked}	0.9669	

Table 46.5 *Calculated Final Voltages and Constants*

Iteration	$V_{OutHigh}$	V_{OutLow}
0	2.5000	2.3714
1	2.4537	2.3285
2	2.4128	2.2905
3	2.3767	2.2569
4	2.3447	2.2272
5	2.3164	2.2009
6	2.2913	2.1777
7	2.2692	2.1571
8	2.2496	2.1390
9	2.2323	2.1229
10	2.2170	2.1087
20	2.1342	2.0318
30	2.1100	2.0093
40	2.1029	2.0027
50	2.1009	2.0008

Table 46.6 *Typical Lock Detect Circuit Simulation for a Starting Voltage of 2.5 Volts*

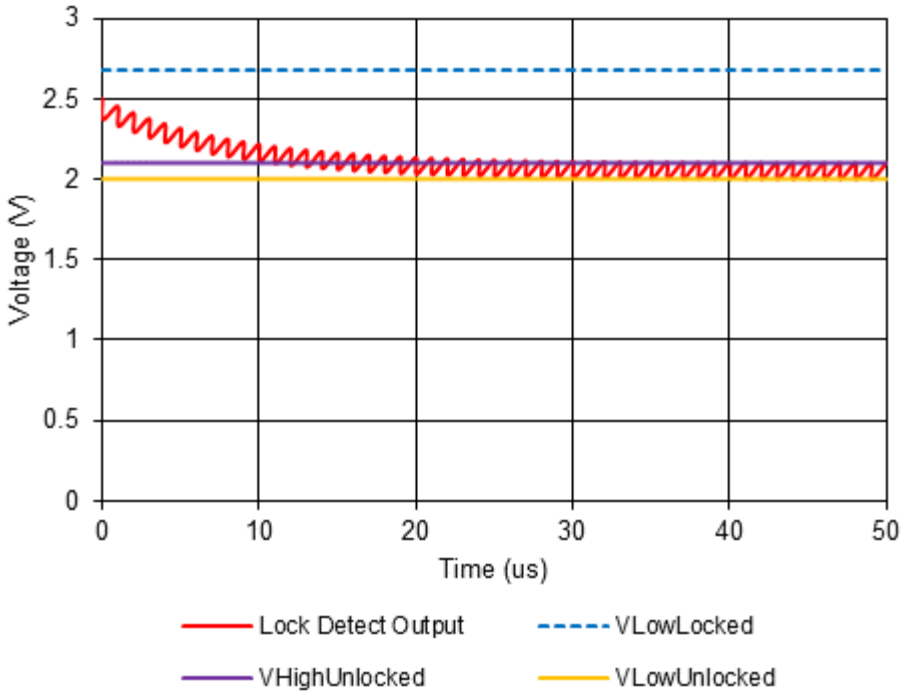


Figure 46.3 *Typical Lock Detect Circuit Simulation for a Starting Voltage of 2.5 Volts*

Parting Thoughts on Lock Detect Circuits

It is necessary for the designer to have some idea how much the width of the lock detect pulses are changing between the locked and unlocked condition. Although a formula for a rough estimate was given, it really is something that should be measured as well. Also, it is not really true that these pulses are rectangular in shape, so there are many assumptions and these formulae should be taken as a guideline, not the final design.

There will be ripple on the output of this circuit and the low and high signals may or may not be far enough apart for whatever input device is using the lock detect information. Filtering can reduce the ripple, and a comparator can deal with the issue if these two voltages are too close. Some microcontrollers also have low speed A/D inputs that can also deal with this issue.

The example presented is actually a very sensitive lock detect circuit that can detect an error kilohertz off. If the out of lock indication is much greater than this, then the low and high voltages from the circuit to indicate lock and unlock are more separated.

Chapter 47 Impedance Matching Issues and Techniques for PLLs

Introduction

The PLL can have up to two inputs for a signal to drive it. These would be the input reference pin (OSCin) and the VCO frequency input pin (Fin). The input impedance of neither of these pins is even close to 50 Ω, and this has caused some confusion regarding what circuit is best for matching. Improper drive levels, low slew rates, or poor matching at these pins can cause issues with phase noise, spurs, or even the ability of the PLL to lock. This chapter discusses some general matching principles and then different methods for matching at these pins.

General Transmission Line Theory

Trace Characteristic Impedance Calculation

The characteristic impedance of any microstrip trace on a PCB board is determined by the width of the trace, ***W***, the height of the trace above the ground plane, ***H***, and the relative dielectric constant, ε_r, of the material used for the PCB board. The reader should be careful to not confuse the characteristic impedance of a microstrip line with the input impedance of the PLL or the output impedance of the VCO; these things are all different.

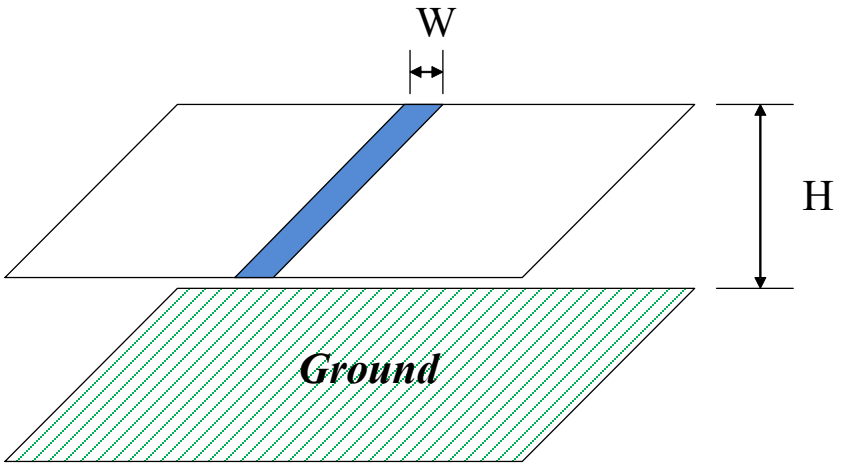


Figure 47.1 *Microstrip Trace on a PCB*

The precise calculation of the trace impedance is rather involved. However, it is a reasonable approximation to say that the trace impedance is independent of frequency and approximate with the following formula from the first reference:

$$Z_0 = \sqrt{\frac{L}{C}} = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \cdot ln\left(7.5 \cdot \frac{H}{W}\right) \qquad \textbf{(47.1)}$$

In this formula, ***L*** represents the inductance per unit length and ***C*** represents the capacitance per unit length. This formula can also be rearranged in order to determine what ratio of height to width is necessary to produce the desired impedance:

$$\frac{W}{H} = \frac{7.5}{exp\left(\frac{Z_0 \cdot \sqrt{\varepsilon_r + 1.41}}{87}\right)} \tag{47.2}$$

Two common PCB board materials are FR4 and Rogers 4003 and the most desired impedance is 50 Ω yields. For these common conditions, the width to height ratio can be easily calculated.

Material	ε_r	W/H for Z_0 = 50 Ω
FR4	4	2
Rogers 4003	3.38	2.1

Table 47.1 *W/H Ratio for Various Materials*

In other words, if the thickness from the top layer to the ground plane is 10 mils (thousandths of an inch) and one wants a 50 Ω trace on an FR4 board, then the width of the trace should be 20 mils. There are many online calculators for microstrip impedance, such as the first reference presented that give more exact calculations.

Reflection Coefficient

When an AC signal encounters a discontinuity in impedance, then part of the signal will be transmitted and part of it will be reflected. The case when the trace and load have mismatched impedances can be modeled as shown in the following figure.

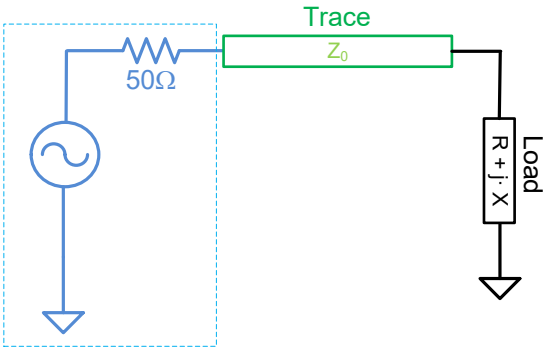


Figure 47.2 *Transmission Line Model*

If the load impedance does not match that of the trace, there will be a reflected wave. The amplitude of the voltage of the reflected wave will be as follows.

$$\Gamma = \frac{Z_0 - (R + X)}{Z_0 + (R + X)} = \frac{reflected\ voltage}{transmitted\ voltage} \tag{47.3}$$

Sometimes this is thought of in terms of power instead of voltage. In this case the reflection coefficient is used and is derived as followed.

$$\rho = \sqrt{\frac{(R - Z_0)^2 + X^2}{(R + Z_0)^2 + X^2}} = \sqrt{\frac{reflected\ power}{transferred\ power}} \tag{47.4}$$

The reflected wave will add constructively or destructively with the original signal to create the final result. Consider the example in the following figure when the trace length is one wavelength and half of the voltage is reflected back towards the source.

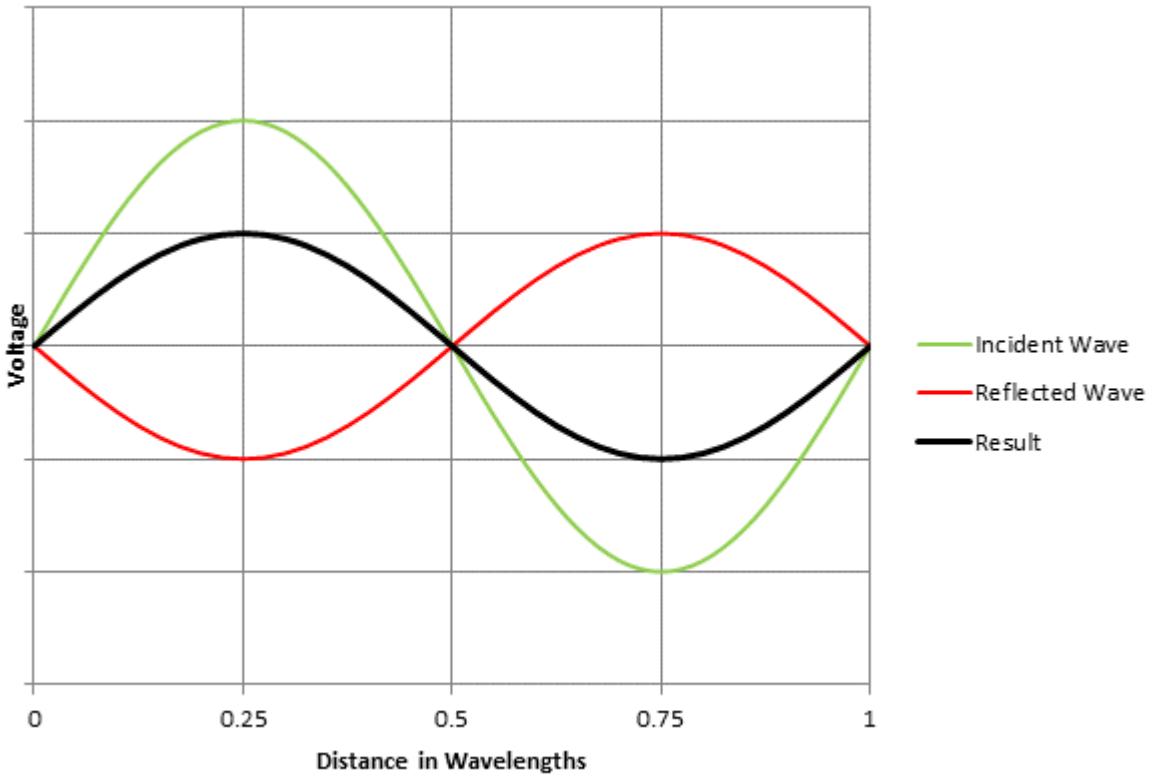


Figure 47.3 *Example of Reflected Wave*

In Figure 47.3, the incident and reflected waves add destructively and the result has lower amplitude. As the incident wave varies with time, then so will the reflected wave. In this example, at ½ of a wavelength from the source, there will be no voltage at all for all time. At a distance of ¼ of a wavelength, the result is half of the original voltage. These results can vary based on how far the load is from the source and how much voltage is reflected back, but generally the AC voltage will vary as a function of where it is measured along the trace. For a sufficiently long trace, one can measure the Voltage to Standing Wave Ratio (***VSWR***). This can be calculated as a function of the trace impedance, $\boldsymbol{Z_0}$, and the load impedance, R+j·X.

$$VSWR = \frac{1+\Gamma}{1-\Gamma} \tag{47.5}$$

As a general rule of thumb, higher VSWR values are undesirable as they indicate a mismatch between the transmission line and the load. Not also that if one assumes that the trace length is less than about $1/10^{th}$ of a wavelength, then the transmission line effects will not be significant.

Real World Component Effects at High Frequencies

Capacitor Equivalent Series Resistance (ESR) and Self-Resonant Frequency (SRF)

Real-world capacitors can be modeled as an ideal capacitance in series with an equivalent series resistance (ESR) and equivalent series inductance (ESL). As a general rule of thumb, the ESR and ESL tend to be larger for higher capacitor values. They also vary with the capacitor type. For instance, tantalum capacitors tend to have much higher ESR than ceramic capacitors.

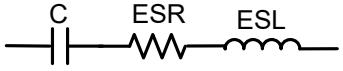


Figure 47.4 *High Frequency Capacitor Model*

The impedance of this real-world capacitor is as follows:

$$Z(f) = ESR + j \cdot \left(2\pi \cdot f \cdot ESL - \frac{1}{2\pi \cdot f \cdot C}\right) \tag{47.6}$$

At low frequencies, the impedance of the ideal capacitor tends to dominate. As the frequency increases, the impedance due to ESL begins to cancel out the impedance due the capacitor. At the self-resonant frequency (SRF), these impedances perfectly cancel and the impedance is just the ESR.

$$SRF = \frac{1}{2\pi \cdot \sqrt{ESL \cdot C}} \quad (47.7)$$

. The following figure shows the magnitude of this impedance for a 100 nF capacitor with an ESR of 100 mΩ and an ESL of 2 nH.

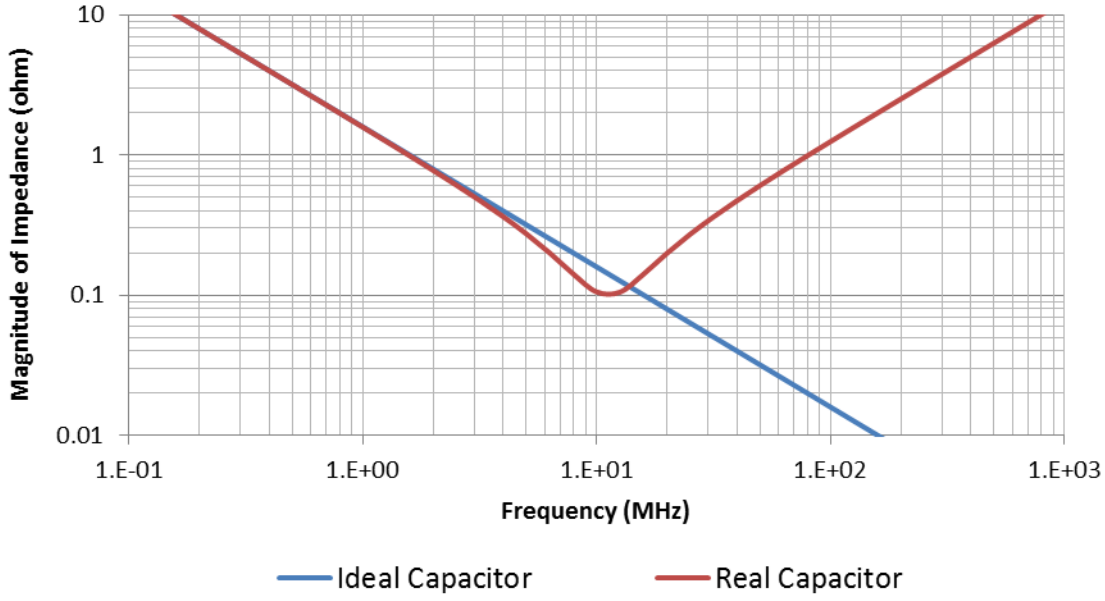


Figure 47.5 *Capacitor Impedance Example*

In truth, this capacitor model is a little oversimplified, but it demonstrates some of the fundamental concepts. If the goal is to make the magnitude of the impedance as small as possible, then a very rough rule of thumb might be to choose the capacitance such that the impedance at the desired frequency is on the order of 100 mΩ.

Resistors

The real-world resistor has an equivalent parallel capacitance (EPC) and equivalent series inductance (ESL). These values may vary drastically with resistor type, but a rough rule of thumb could be to assume that the EPC = 0.2 pF and ESL = 1 nH.

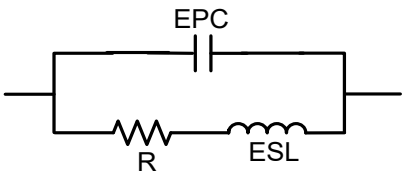


Figure 47.6 *High Frequency Model for a Resistor*

Applying these values to the above the model above for a 1 kΩ resistor gives the following resistance curve.

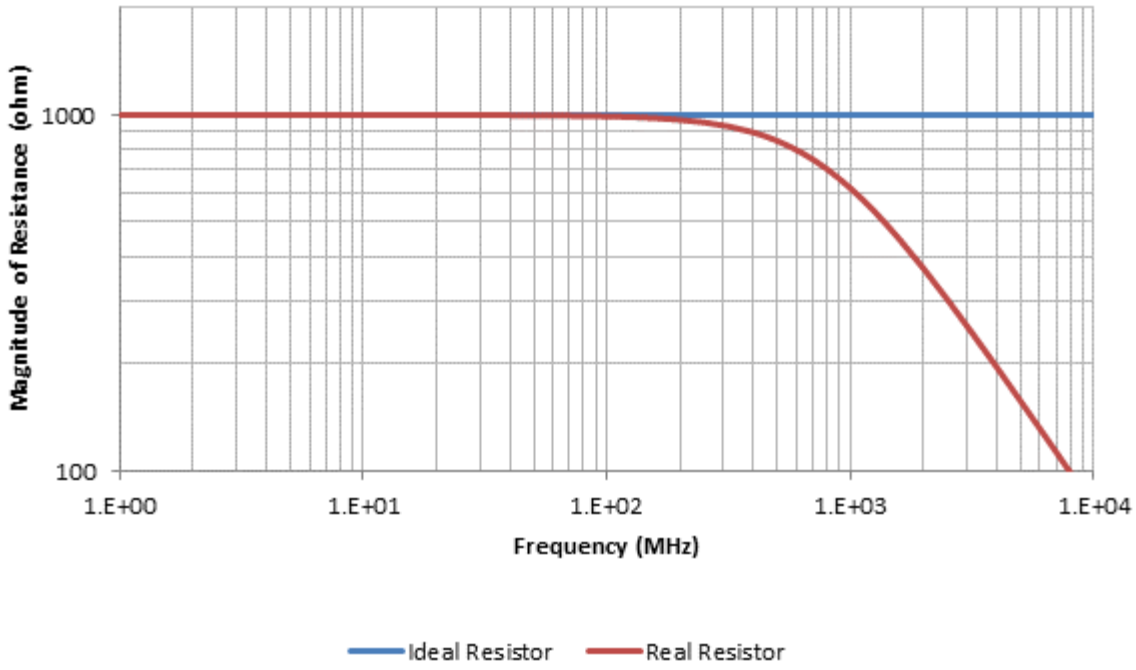


Figure 47.7 *High Frequency Resistor Example*

One guideline to get from this model is not to believe high resistance values at high frequencies. For instance, a real 1 kΩ resistor at 2 GHz operation is probably going to look a lot different than an ideal resistor under these conditions.

Strategies for Dealing with High Frequency Behaviors

For capacitors, the challenge may be that a low capacitance value is good at high frequency, but poor at low frequency. One strategy could be to use a few capacitors of different values to create a good broadband low impedance. For resistors, one can consider using different networks that have lower resistor values. As a final strategy, consider using components specialized for high frequency, such as the few examples in the following table.

Component	Value	Footprint	Manufacturer	Part	Frequency
Resistor	50 ohm	402	Vishay	FC0402E50R0BST1	20 GHz
	50 ohm	603	Vishay	FC0603E50R0BTBST1	20 GHz
Capacitor	0.01 µF	402	ATC	520L103KT16T	16 GHz
	0.1 µF	402	ATC	550L104KCAT	40 GHz

Table 47.2 *Typical High Frequency Components*

Impedance Matching Strategies

Keeping Traces Short and Adjusting Trace Width

Impedance matching becomes an issue when the trace length is more than about $1/10^{th}$ of a wavelength and the load impedance is mismatched from the characteristic impedance. So if it is possible to make the trace length very short, then impedance matching is not an issue any more. This also makes the design less susceptible to variations in the impedance of the load or discontinuities in the impedance caused by putting components in the trace.

Another strategy is to adjust the trace width. Although standard test equipment is 50 ohm input impedance, this does not mean that the design itself has to conform to this standard. If the trace width is made to match the load impedance, then transmission line effects can be reduced.

Eliminating the Imaginary Part of the Impedance

As transmission line impedance is real, any imaginary component to the load impedance will make the reflection coefficient worse. A strategy with coping with this is to put a series inductor or capacitor to cancel this impedance. For instance, the high frequency input pin of a PLL typically has a large negative imaginary impedance. A possible narrowband matching strategy would be to use a series inductor to cancel this. This narrowband matching strategy might work, but then the inductor will have its own non-ideal high frequency behaviors. Many times, this pin requires the signal to be AC coupled, and this is done with a capacitor. One realization is that if the capacitor self-resonant frequency is exceeded, then this might actually be beneficial as the capacitor now starts to look like an inductor and this will cancel with the negative imaginary component of the load. As a matter of fact, it is a common mistake to choose an AC coupling capacitor that is too small to avoid the self-resonant frequency only to have the capacitor impedance be too large. Also this tends to attenuate the desired signal more than the harmonics.

Narrowband Tuned Matching Circuits with Inductor and Capacitor

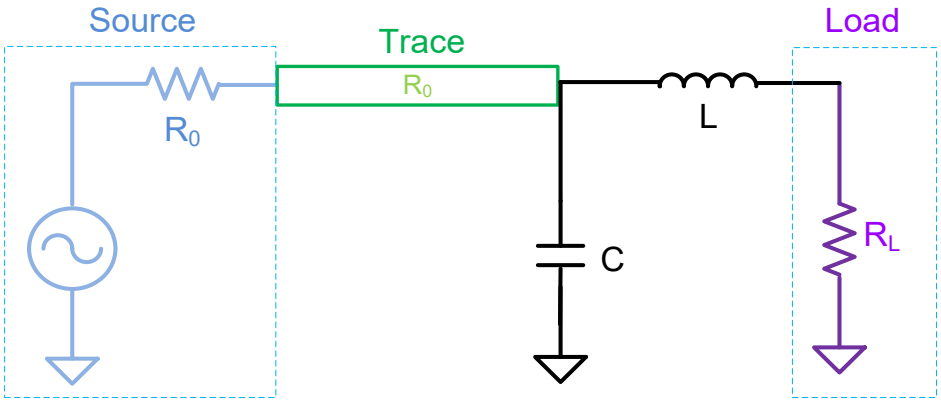


Figure 47.8 *Typical Impedance Matching Circuit*

When the frequency of operation is not too wide, the impedances are well known, and the load is a pure resistance, a tuned circuit using an inductor and capacitor can be used for matching. Figure 47.8 assumes the load impedance is greater than the line impedance, but if this were not the case, then the inductor L, needs to be moved to the left hand side of capacitor ***C***, instead of the right hand side and the values for the load and source resistance need to be switched. The matching circuit is designed so that both the load and source see a matching impedance. This yields a system of two equations and two unknowns that can be calculated ***L*** and ***C***. In the case that the load has a negative reactance and also has less resistance than the source, it is convenient to compensate for the negative reactance by making the inductor, ***L***, bigger by the appropriate amount.

$$\frac{R_0}{1 + s \cdot C \cdot R_0} + s \cdot L = R_L \tag{47.8}$$

$$\frac{s \cdot L + R_L}{s^2 \cdot L \cdot C + s \cdot R_L \cdot C + 1} = R_0 \tag{47.9}$$

Solving these simultaneous equations and assuming a frequency of f_0 yields the following:

$$C = \frac{\sqrt{\frac{R_0}{R_L} - 1}}{2\pi \cdot f_0 \cdot R_0} \tag{47.10}$$

$$L = C \cdot R_0 \cdot R_L \tag{47.11}$$

This matching strategy can be expanded to the case where the load has negative imaginary part to the impedance. In this case, an inductor can be added to cancel that. If it also turns out that the real impedance of the load is greater than the source impedance, then one can simply increase the value of the inductor that is already there to tune out this negative imaginary part.

The Simple Match for High Impedance Load

If it is known that the load is high impedance relative to the transmission line impedance, then a simple shunt resistor can be used to match the impedance. However, when this approach, one needs to be sure that the impedance is high, or else the shunt resistance could make the impedance matching worse.

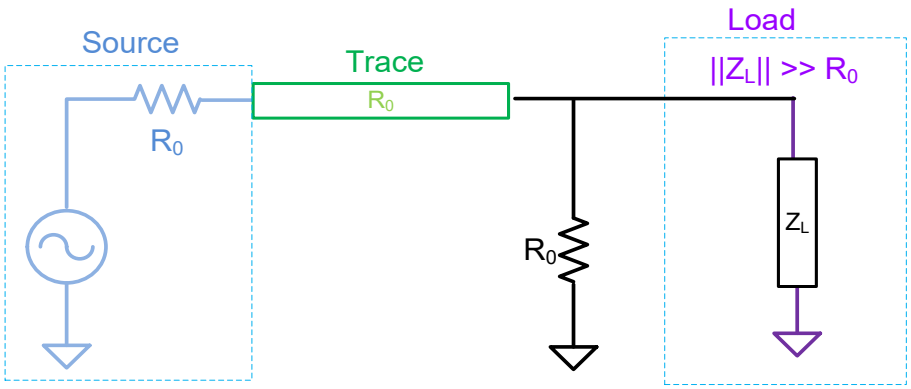


Table 47.3 *Resistive Matching with a Shunt Impedance*

The Resistive Pi-Pad

The resistive pad is a good way to give a broadband impedance match. The general concept is to force the impedance of the pad and the load to look like 50 ohm, regardless of the load impedance, or frequency. The advantages are that it is a broadband match, it does not require more expensive inductors, and is much more tolerant to variations in the load impedance. The main disadvantage is that some power to the load needs to be sacrificed in order to obtain this matching. As more power to the load is sacrificed, the matching ability of the pad increases.

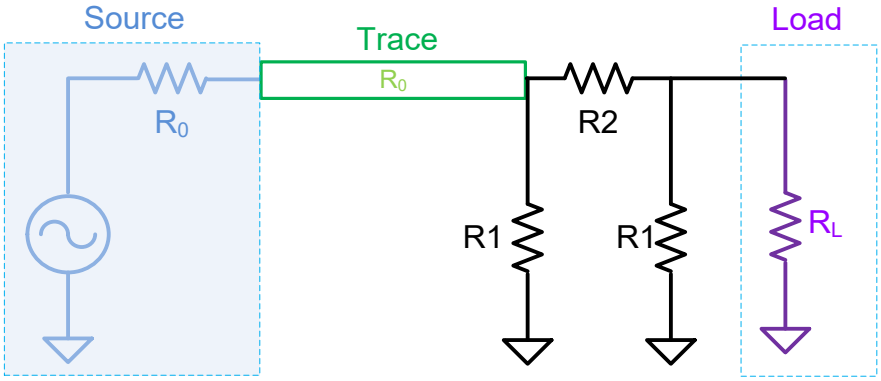


Figure 47.9 *Typical Resistive Pad*

For the resistive pad, the attenuation of the pad is specified, and it is designed assuming that both the source and load impedance are equal to ***Ro***, usually 50 Ω. The resistor values satisfy the following equations.

$$R_0 = R1\,||(R1 + R1||R_0) \qquad \textit{(47.12)}$$

$$10^{Atten/20} = \frac{(R1||R_0) \cdot R1}{R1 + R2 + R1||R_0} \quad \textit{(47.13)}$$

In these equations, ***R_0*** is the source impedance, ***Atten*** is the attenuation of the pad, and ***x*** || ***y*** is used to denote the parallel combination of two components, ***x*** and ***y***. The components ***R1*** and ***R2*** can be calculated as follows:

$$R1 = R_0 \cdot \frac{10^{Atten/20} + 1}{10^{Atten/20} - 1} \quad \textit{(47.14)}$$

$$R2 = \frac{2 \cdot R_0 \cdot R1}{R1^2 - {R_0}^2} \quad \textit{(47.15)}$$

In most situations, R_0=50Ω and the attenuation value is either 3 dB or 6 dB. For these common cases the values are calculated.

Atten	*R1*	*R2*
3 dB	292.4 Ω	17.6 Ω
6 dB	150.5 Ω	37.4 Ω

Table 47.4 *Resistor Values for 3 dB and 6 dB Pi-Pads*

The Resistive T-Pad

The resistive T-Pad is a variation on the resistive Pi pad that is mathematically equivalent and has the same number of components, but in a different layout. The T-Pad gives more flexibility for tinkering or converting to an LC match circuit. The Pi-Pad has only one series component and this might be a consideration for high frequency operation.

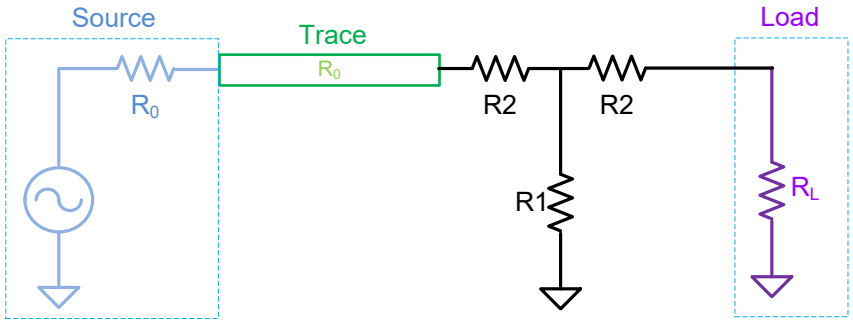


Figure 47.10 *Resistive T-Pad*

The equations for the T-Pad are as follows.

$$R_0 = R2 + R1 \,||(R2 + R_0) \tag{47.16}$$

$$10^{-Atten/20} = \frac{R1}{R1 + R2 + R_0} \tag{47.17}$$

In these equations, R_0 is the source impedance, ***Atten*** is the attenuation of the pad, and $x \,||\, y$ is used to denote the parallel combination of two components, x and y. These equations can be solved for R2 and R1

$$R2 = R_0 \cdot \left(\frac{10^{\frac{Atten}{20}} - 1}{10^{\frac{Atten}{20}} + 1} \right) \tag{47.18}$$

$$R2 = R1 \cdot \left(10^{\frac{Atten}{20}} - 1 \right) - R_0 \tag{47.19}$$

In most situations, R_0=50 Ω and the attenuation value is either 3 dB or 6 dB. For these common cases the values are calculated.

Atten	*R1*	*R2*
3 dB	8.6 Ω	141.9 Ω
6 dB	16.6 Ω	66.9 Ω

Table 47.5 *Resistor Values for 3 dB and 6 dB T-Pads*

6 dB Splitter

If one takes a 6 dB pad and instead considers replacing the grounded resistor with another load and series resistor, the 6 dB splitter is attained. Just as with the resistive pad, the splitter will transform the impedance to look closer to 50 ohms.

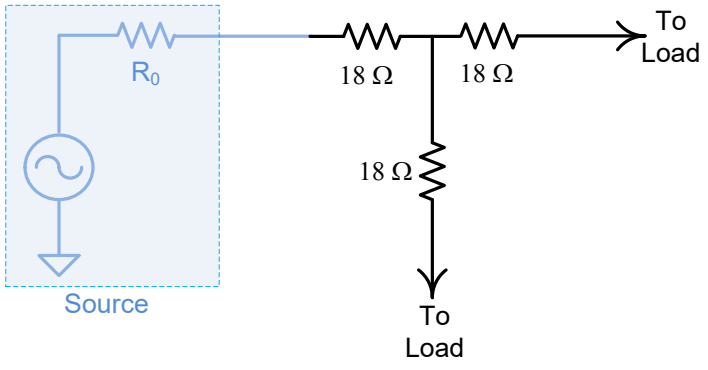


Figure 47.11 *6 dB Splitter*

Impedance Matching Strategies for PLL Input Pins

OSCin Pin

For the OSCin pin, one can generally just use a simple shunt resistor to ground in many cases as this pin is typically high impedance, at least at lower frequencies. If this is not the case, a resistive T-Pad is a good choice as this layout also accommodates many other options such as an LC match to use three different resistor values to accommodate a source impedance that does not match the line impedance. Many devices have a differential OSCin pin and it is generally best for spurs to make the impedance as looking out from both the OSCin and its complimentary pin to look roughly the same.

Fin Pin

The high frequency input pin tends not to be high impedance and tends to be capacitive. A typical example of what this impedance might look like is shown in the following figure.

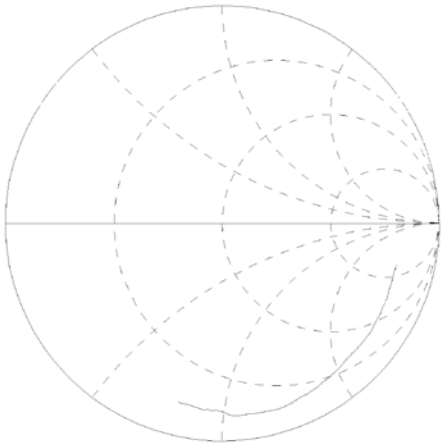


Figure 47.12 *Smith Chart Typical Fin Input Impedance*

As this input impedance tends to vary around with frequency, the 6 dB T-Pad is often a good choice for matching. If this sacrifices too much power, then this value can be reduced or one can tinker with using an LC approach. As a general rule of thumb and from experience, it seems that overly complicated matching circuits should be done with care as they can sometimes agitate problems with matching or the VCO harmonics. One particular pitfall to watch out for is to not be overly averse to avoiding the self-resonant frequencies of the AC blocking capacitor. For instance, the following example shows the use of a 2 pF capacitor for a 1 GHz AC coupling capacitor. 2 pF at 1 GHz is 79.5 Ω, which will definitely be too large next to the series 18 Ω and cause the impedance matching to be poor and a large loss of signal.

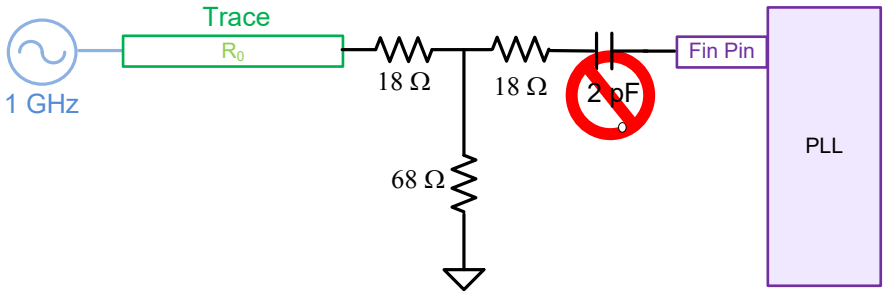


Figure 47.13 *Using Too Small of an AC Coupling Capacitor*

Conclusion

Although impedance matching networks are not always necessary for matching the PLL to the VCO, they may be needed in when the input impedance of the PLL is poorly matched to the PCB trace impedance. When the trace length between the VCO and PLL approaches one-tenth of a wavelength, the trace is considered long and undesired transmission line effects can result. If there is plenty of VCO power to spare, the resistive pad serves as an economical and process-resistant solution. Otherwise, if the PLL is grossly mismatched to the VCO, the approach with inductors and capacitors can provide a good match. When using any sort of matching network, it is important to put this network as close to the PLL as possible.

References

[1] Danzer, Paul (editor) *The ARRL Handbook (Chapter 19)* The American Radio Relay League. 1997

[2] I had useful conversations with Thomas Mathews regarding real-world component behavior.

Chapter 48 PLL Debugging Techniques

Introduction

When one has a problem getting a PLL up and running, this can be a frustrating experience. It can be often compounded by premature assumptions and lack of a systematic debugging process. The general steps should be to first establish that one is communicating with the PLL, then lock the PLL, and thirdly optimize the performance. This chapter goes through this systematic debugging process and then shares some common mistakes that can cause a PLL to go wrong.

Establishing Communication with the PLL

The first step is to confirm that one is actually communicating with the device. What this means is that a command can be given to the PLL through the serial bus and it will respond to it in the way it should. It is not sufficient to simply observe the programming signals at the PLL pins as this does not establish that the PLL is actually responding to it. It is best to use software commands that require a minimum amount of hardware setup conditions to work such as the methods presented to follow.

Readback Method

Some devices support reading back of registers. If this can be done, then it is an excellent way to verify that communication is working. However, if this method does not work, it does not necessarily demonstrate that communication is not working. For instance, this could be the case if the device is not properly configured for readback in hardware or software.

Powerdown Method

The general premise of this method is to demonstrate that the device is communicating by powering it up and down via a software programming bit. The powerdown status of the device can be typically be determined by current consumption, frequency input pin bias levels, or device LDO output voltages. Current consumption may be the easiest way, but this assumes that the PLL is being powered by a power supply that can read current. If this is not the case, typically the high frequency input pin (Fin) biases to about 1.6V when powered up and 0 V when powered down. Also, the input reference pin (OSCin) typically biases up to about Vcc/2 when powered up and 0V when powered down. For devices with LDOs, sometimes these voltages can be toggled with the powerdown bit.

IO Pin Toggling Method

Often times PLLs have I/O pins that can be toggled high and low to demonstrate communication with the device. For instance, it is common that multiple functions are multiplexed onto the lock detect pin or there is a frequency test pin (MUXout).

Phase Detector Polarity Method

This method is easy to try and an effective way to verify communication is working. However, if it fails, this does not necessarily mean that communication is not working. The idea is to just simply toggle the phase detector polarity. This should cause the carrier to jump to a different frequency. For an integrated VCO, be aware that there are multiple frequency bands, so the jump is likely much less than the frequency range of the device.

Common Causes of Communication Issues

If none of the methods presented demonstrate communication with the PLL, then there are several common causes for this.

- Readback not Configured Correctly in Hardware or Software
- Crossed Programming Lines
- Device is always in Powerdown Mode
    - This could be the result if there is a chip enable pin that is pulled low.
- Improperly Soldered Power Pins
- Ground DAP not Grounded
- Intentionally Disconnected Power Pins
    - When using a dual PLL, do not disconnect the power pins to an unused side unless directed to. These pins can often power other blocks, such as the programming interface
- Input Reference not Connected
    - Not having any input reference can interfere with the powerdown/powerup test for some devices.
- Latch Enable (also called CSB) being held High
    - On some devices if the latch enable pin is held high, programming is ignored.
- Insufficient Slew Rate for Programming Pins
    - As a rough rule of thumb, it is desirable to have at least 30V/µs slew rate on the programming lines, although this is device specific.
    - Sometimes there is the practice of putting low pass filters on the programming interface pins to reduce EMI. If this is done, be very cautious not to reduce the slew rate.
- Timing and Voltage Issues with Programming Lines
    - If timing or voltage specs are violated, then this can cause issues with programming

Getting the PLL to Lock

Once communication is established, the next step is to try to get the PLL to lock. There are several issues that can cause this which are discussed.

Program the VCO Frequency within Range

Although PLLs tend to be broadband, this is not the case for many VCOs. A common problem is to try to program the VCO to a frequency beyond what it can achieve. One thing to consider is that many parts have a VCO divider and the final output frequency is not the VCO frequency. For instance, if a device has VCO that tunes 2-4 GHz and a 100 MHz output frequency is desired, then the correct is to program the VCO to 2400 MHz and then divide by 24 to get a 100 MHz output frequency; it would be incorrect to directly program the VCO frequency to 100 MHz.

Debugging Using the Lock Detect

Lock detect is generally not the best way to very lock in a debugging situation as a problem with the lock detect could give the wrong impression. That being said, sometimes a spectrum analyzer is not available or possible to attach to the output. If using lock detect, try to also verify with another method. For instance, checking the VCO tuning voltage is a good way to cross-validate the lock detect. If the VCO tuning voltage is not at the rail, yet the lock detect pin indicates an unlocked situation, some common causes for this are improper settings on the programmable lock detect settings. Also, digital lock detect becomes more challenging for higher phase detector frequencies and higher modulator orders, so reducing the phase detector frequency or modulator order is a good diagnostic.

Debugging the Loop Filter

The loop filter has a large impact on performance, but at this stage, the goal is to simply get the PLL to lock. To do this, try commands that cause the VCO frequency to move, such as toggling the phase detector polarity, removing/changing the input reference frequency, or changing the N divider value by drastic amounts. Typical issues with the loop filter could be that it could be shorted to ground or not connected. Also be aware that it is common practice to accommodate higher order filters and put 0 Ω resistors for R3 and R4. If these resistors are missing, this could be the issue. In the case of an active filter, the op-amp is a huge degree of freedom, so if ensure that the voltage rails are not being violated and bypass it if possible for debugging purposes if nothing else works.

If the loop filter is unstable, typically the frequency will move, but it might slew across the frequency range. Shorting out resistors R3 and R4 will make a theoretically stable filter. It is typically a symptom if instability if lowering the charge pump current can help the device to lock, but just because this does not work does not rule out instability. Common causes for loop filter instability include neglecting to account for the VCO input capacitance, using an integrated filter that over-restricts the loop bandwidth, or using the PLL with different settings (charge pump gain, VCO gain, VCO frequency, or phase detector frequency) than it was originally designed for.

Debug the R and N Dividers

If the R and N dividers are improperly working, then this will cause the PLL to mislock. Aside from putting the wrong frequency or insufficient voltage levels, it is also possible to have problems with matching and harmonics. Most PLLs have a way to view the actual output of these N and R dividers to check that this frequency is actually correct.

Debug the VCO Calibration

For devices with integrated VCOs, the frequency range is typically divided into several different bands. Incorrect programming can cause the VCO to lock to the wrong band. The VCO calibration is typically initiated by the programming of a particular register and therefore one should ensure that the other software and hardware conditions (especially input reference frequency) are proper when this register is programmed to allow the calibration to work correctly.

Analyze the PLL Programming

The PLL programming has many things that could cause the PLL not to lock. Analyzing the programming might be a necessary task if no other methods get the PLL to lock. When doing this, often this can be facilitated by using the programming software and manually entering in the programming information so that it can be interpreted easier.

Optimizing the PLL Performance

Once the PLL is locked, the next step is to debug any issues that could cause the performance to degrade.

Peaking and Instability

Peaking is typically observed as a large peaking in the phase noise response near the loop bandwidth. It can also show up as excessive ringing in the transient response. This can be the result of VCO phase noise, incorrect component values, the VCO input capacitance, or a large difference in the loop gain, *K*, than what the loop filter was designed for.

Peaking can sometimes be caused by the VCO phase noise, if the loop bandwidth is much less than the minimum jitter bandwidth, the VCO noise can crop inside the loop bandwidth and create peaking. This is often misinterpreted as low phase margin when in fact it is just the VCO noise and more of a matter of optimizing the loop filter and not a functional problem or issue with stability.

Incorrect component values are another cause of peaking and instability. Some of the common mistakes are to accidentally swap C1 and C2, which leads to severe peaking or to have C3 or C4 assembled on the board but disregarded in the design. The VCO input capacitance adds in parallel with the input capacitance and this can cause peaking or instability if unaccounted for. In the actual design of a loop filter, one mistake is to try to

push the loop bandwidth as wide as possible when it gets limited by the VCO input capacitance or integrated and fixed components on the chip. In this case, some design tools will return the correct loop bandwidth, but it might have a lot of peaking in the response. Good PLL design tools allow the user to type in the component values and analyze the performance and stability of this.

Yet another cause of peaking and instability is when the loop filter is designed for one loop gain and it changes considerably. For instance, if a loop filter is designed for a VCO with a gain of 20 MHz/V an then the VCO is replaced with one of similar frequency with a gain of 100 MHz/V, then the loop dynamics change unless this is compensated for with the charge pump current or the loop filter is re-designed. This same concept applies if the phase detector frequency or VCO frequency is changed by a large amount.

One quick way to diagnose a loop filter stability issue is to observe the impact of reducing the loop gain, ***K***. Also, if a loop filter is not very stable, this also shows up as an excessive lock time with a lot of ringing. This can be done by reducing the charge pump current or increasing the ***N*** divider value. Usually, the PLL will lock in this case, but there will be severe peaking.

Counter Sensitivity Issues

If the power delivered to the input pin of the PLL for the input reference or VCO is marginal, then this can cause issues that look like instability, increased phase noise, or even high spurs. On the VCO input pin, matching can sometimes agitate these issues. Aside from checking these power levels, some other things that can be done is to see if there is any impact by touching the PLL and areas near these pins with your finger. Although this is not a realistic solution, it is a great and easy way to sometimes pinpoint the problematic area.

Bad PLL Phase Noise

Common causes of high PLL phase noise are insufficient slew rate on the input reference, high noise on the input reference, and a narrow loop bandwidth. If using a signal generator as the reference source, realize that they tend to be dirty relative to a PLL and will mask the PLL noise. One signal generator trick is to raise the frequency and divide down by a larger R divided to the same phase detector frequency. If this improves the PLL noise, then this often indicates that the signal generator is higher noise than the PLL. Also, the output power can be adjusted to test slew rate. Another cause of high PLL noise issue is when the loop bandwidth of the PLL is too narrow to filter out the VCO noise. It may look flat, but the VCO noise can impact the phase noise inside the loop bandwidth in this case.

High VCO Phase Noise

Power supply noise and VCO calibration issues are common causes of high VCO noise. One diagnostic for the power supply if it uses an LDO (low dropout regulator) is to either bypass the LDO or force it out of regulation by lowering the input voltage. In terms of VCO calibration, one check is to look at the VCO tuning voltage ensure that it is not near the rail.

Inconsistent Performance with the Same Chip

In some situations, the PLL is locked on different occasions to the same frequency with the exact same hardware and software conditions, yet there is a difference in performance. If the difference is fractional spurs, one cause could be if the fractional modulator is not being reset to the same initial state when the PLL is programmed. This initial state impacts the modulator sequence of the fractional engine and can impact spurs. This being said, this tends to be an issue with only older PLLs as most modern PLLs automatically reset the modulator when the N divider is changed.

Another cause is when the VCO calibration is choosing a different VCO core or band within the core. For instance, consider the situation where the desired frequency is at the boundary of two VCO cores. If the VCO calibration chooses the lower frequency VCO core, then the frequency will be near the high end of the frequency for this core, typically implying a higher VCO gain. If the higher VCO core is chosen, then the exact opposite is true. This difference in VCO gain translates into a change in the loop bandwidth. In addition to the VCO gain, this could also lead to differences in the VCO tuning voltage which would cause differences in the charge pump performance. Yet another consideration is that different VCO cores can have different spurs and VCO phase noise performance.

Conclusion

The debugging process for the PLL needs to be systematic starting with establishing communication, establishing lock, and then optimizing performance. It is often the premature assumptions that are not true that can cause the debugging process to be longer than necessary.

Chapter 49 Solutions to Higher Order Polynomial Equations

Introduction

In several chapters, it becomes necessary to find the roots third or fourth order polynomials. These come up in a few cases such as calculating the closed loop poles for calculating the analog transient response and a few places involving partially integrated loop filters. This chapter is for those readers who want the satisfaction of a closed form solution when these polynomials arise. It also turns out that as these roots tend to be complex, a closed form solution is often the best approach.

Solution of the Quadratic Polynomial

Consider the quadratic equation of the form:

$$a \cdot x^2 + b \cdot x + c = 0 \tag{49.1}$$

If ***a***=0, then this a linear equation, and the solution is trivial. If not, divide through by ***a*** and introduce the following substitution

$$y \rightarrow x - \frac{b}{2 \cdot a} \tag{49.2}$$

This approach may be slightly different than the traditional approach of setting the square, but is introduced as this substitution method is also useful for the cubic and quartic equation solutions as well. This substitution removes the linear term and simplifies the equation.

$$y^2 = \frac{b^2}{4 \cdot a^2} - \frac{c}{a} = \frac{b^2 - 4 \cdot a \cdot c}{4 \cdot a^2} \tag{49.3}$$

Take the square root of both sides to solve for y and then reverse the substitution (49.2) to get the familiar quadratic equation.

$$x = \frac{-b \pm \sqrt{b^2 - 4 \cdot a \cdot c}}{2 \cdot a} \tag{49.4}$$

Solution of the Cubic Polynomial

Although not commonly taught, the cubic equation does have a closed form solution. For this kind of equation, one can assume without loss of generality that the leading coefficient is one. If this is not the case, then the equation can easily be reduced. If the leading coefficient is zero, then this is actually a quadratic equation, which has already been solved. If it is not the case, then divide through by the leading coefficient. In summary, the cubic equation is of the following form.

$$x^3 + a_2 \cdot x^2 + a_1 \cdot x + a_0 = 0 \tag{49.5}$$

The first step is to eliminate the square term by introducing the following substitution.

$$y - \frac{a_2}{3} \rightarrow x \tag{49.6}$$

$$\left(y - \frac{a_2}{3}\right)^3 + a_2 \cdot \left(y - \frac{a_2}{3}\right)^2 + a_1 \cdot \left(y - \frac{a_2}{3}\right) + a_0 = 0 \tag{49.7}$$

After a little work, this reduces the equation to "depressed cubic".

$$y^3 + q \cdot y + r = 0 \tag{49.8}$$

$$q = \frac{{a_2}^2}{3} - \frac{2}{3} \cdot {a_2}^2 + a_1 = a_1 - \frac{{a_2}^2}{3} \tag{49.9}$$

$$r = -\frac{{a_2}^3}{27} + \frac{{a_2}^3}{9} - \frac{a_1 \cdot a_2}{3} + a_0 = a_0 + \frac{2 \cdot {a_2}^3}{27} - \frac{a_1 \cdot a_2}{3} \tag{49.10}$$

The derivation for the solution of the depressed cubic typically involves another substitution. Mathematician Gerolamo Cardano was first to publish a solution, but the substitution presented by the French mathematician François Viète is a little easier to understand. To do this, introduce the following substitution.

$$w - \frac{q}{3 \cdot w} \rightarrow y \tag{49.11}$$

$$\left(w - \frac{q}{3 \cdot w}\right)^3 + p \cdot \left(w - \frac{q}{3 \cdot w}\right) + r = 0 \qquad \textbf{(49.12)}$$

This simplifies the equation as follows:

$$w^6 + r \cdot w^3 - \frac{q^3}{27} = 0 \qquad \textbf{(49.13)}$$

This equation is quadratic in w^3 and can be solved with the quadratic formula:

$$w = \sqrt[3]{\frac{-r \pm \sqrt{r^2 + \frac{4}{27} \cdot q^3}}{2}} = \sqrt[3]{R \pm \sqrt{D}} \qquad \textbf{(49.14)}$$

$$Q = \frac{q}{3} = \frac{3 \cdot a_1 - {a_2}^2}{9} \qquad \textbf{(49.15)}$$

$$R = -\frac{r}{2} = \frac{9 \cdot a_1 \cdot a_2 - 2 \cdot {a_2}^3 - 27 \cdot a_0}{54} \qquad \textbf{(49.16)}$$

$$D = R^2 + Q^3 \qquad \textbf{(49.17)}$$

Now assume that D>=0 and focus on just the first real root for (49.14) and call this w0.

$$w0 = \sqrt[3]{R + \sqrt{R^2 + Q^3}} \qquad \textbf{(49.18)}$$

Substituting this back yields the first real root.

$$p0 = y - \frac{a_2}{3} = w0 + \frac{Q}{w0} - \frac{a_2}{3} = \sqrt[3]{R + \sqrt{R^2 + Q^3}} + \frac{Q}{\sqrt[3]{R + \sqrt{R^2 + Q^3}}} - \frac{a_2}{3} \qquad \textbf{(49.19)}$$

This can further be simplified with the following new variables

$$p0 = S + T - \frac{a_2}{3} \tag{49.20}$$

$$S = \sqrt[3]{R + \sqrt{R^2 + Q^3}} = \sqrt[3]{R + \sqrt{D}} \tag{49.21}$$

$$T = \frac{-Q}{\sqrt[3]{R + \sqrt{R^2 + Q^3}}} \cdot \frac{\sqrt[3]{R - \sqrt{R^2 + Q^3}}}{\sqrt[3]{R + \sqrt{R^2 + Q^3}}} = \sqrt[3]{R - \sqrt{R^2 + Q^3}} = \sqrt[3]{R - \sqrt{D}} \tag{49.22}$$

Now there are actually three cube roots of this equation. To do this, first realize that there are actually three cube roots of one, which would be as follows.

$$\sqrt[3]{1} = 1\ , -\frac{1}{2} + \frac{j\sqrt{3}}{2}, -\frac{1}{2} - \frac{j\sqrt{3}}{2} \tag{49.23}$$

So to find the other roots for (49.14), use the other cube roots of one.

$$\begin{aligned} w1 = w0 \cdot \left(-\frac{1}{2} + \frac{j\sqrt{3}}{2} \right) \\ = \left(-\frac{1}{2} + \frac{j\sqrt{3}}{2} \right) \cdot \sqrt[3]{R + \sqrt{R^2 + Q^3}} \left(-\frac{1}{2} + \frac{j\sqrt{3}}{2} \right) \cdot S \end{aligned} \tag{49.24}$$

This leads to the next root.

$$p1 = w1 + \frac{Q}{w1} - \frac{a_2}{3}$$

$$= \left(-\frac{1}{2} + \frac{j\sqrt{3}}{2}\right) \cdot S \frac{Q}{\left(-\frac{1}{2} + \frac{j\sqrt{3}}{2}\right) \cdot \sqrt[3]{R + \sqrt{R^2 + Q^3}}} - \frac{a_2}{3}$$

$$= \left(-\frac{1}{2} + \frac{j\sqrt{3}}{2}\right) \cdot S + \frac{T}{\left(-\frac{1}{2} + \frac{j\sqrt{3}}{2}\right)} \cdot \frac{-\frac{1}{2} - \frac{j\sqrt{3}}{2}}{-\frac{1}{2} - \frac{j\sqrt{3}}{2}} \quad \textbf{(49.25)}$$

$$= -\frac{S}{2} + S \cdot \frac{j\sqrt{3}}{2} - \frac{T}{2} - \frac{T}{2} \cdot j\sqrt{3}$$

$$p1 = -\frac{a_2}{3} - \frac{S+T}{2} - \frac{j\sqrt{3}}{2} \cdot (S - T) \quad \textbf{(49.26)}$$

Using a very similar derivation, the final root can be found:

$$p2 = -\frac{a_2}{3} - \frac{S+T}{2} + \frac{j\sqrt{3}}{2} \cdot (S - T) \quad \textbf{(49.27)}$$

The one assumption made so far was that D>=0. If it is the case that D<0, then leads to taking the cube root of a complex number, which can be a little messy. In the case that D<0, this would involve taking a cube root of a complex number to find S and T and this is a little complicated. One can use Euler's identity to express these complex numbers in polar form to state these roots in terms of trigonometric functions.

$$\theta = cos^{-1}\left(\frac{R}{\sqrt{-Q^3}}\right) \quad \textbf{(49.28)}$$

$$p0 = -\frac{a_2}{3} + 2\sqrt{-Q} \cdot cos\left(\frac{\theta}{3}\right) \quad \textbf{(49.29)}$$

$$p1 = -\frac{a_2}{3} + 2\sqrt{-Q} \cdot cos\left(\frac{\theta + 2\pi}{3}\right) \quad \textbf{(49.30)}$$

$$p2 = -\frac{a_2}{3} + 2\sqrt{-Q} \cdot cos\left(\frac{\theta + 4\pi}{3}\right) \quad \textbf{(49.31)}$$

Solution to the Quartic Equation

The quartic equation does have a closed form solution and the equations are involved. This section will show the key concepts to the derivation and then give the formula. Consider an equation of the following form

$$x^4 + a_3 \cdot x^3 + a_2 \cdot x^2 + a_1 \cdot x + a_0 = 0 \quad \textbf{(49.32)}$$

The first step is to eliminate the square term by introducing the following substitution.

$$y - \frac{a_3}{4} \rightarrow x \quad \textbf{(49.33)}$$

After a little work, this reduces the equation to "depressed quartic".

$$y^4 + A \cdot y^2 + B \cdot y + C = 0 \quad \textbf{(49.34)}$$

$$A = a_2 - \frac{3 \cdot {a_3}^2}{8} \quad \textbf{(49.35)}$$

$$B = a_1 + \frac{{a_3}^3}{8} - \frac{a_3 \cdot a_2}{2} \quad \textbf{(49.36)}$$

$$C = a_0 - \frac{3 \cdot {a_3}^4}{256} + \frac{{a_3}^2 \cdot a_2}{16} - \frac{a_3 \cdot a_1}{4} \quad \textbf{(49.37)}$$

Now if *B*=0, then this equation becomes something that is quadratic in y^2, which can easily be solved. If *C*=0, then one can factor out *y* and we are left with a cubic equation; both of these cases can be handled. For the more difficult case where *B* and *C* are both nonzero, the general strategy is to try to write this equation as two squared expressions. To do this, the strategy is to introduce a new variable, *u*, and rewrite the equation using this new variable.

$$(y^2 + u)^2 = (2 \cdot u - A) \cdot y^2 - B \cdot y - C + u^2 \quad \textbf{(49.38)}$$

The left hand side is a perfect square. The strategy is to choose u such that the right hand side is also a perfect square. The first step is some rearranging.

$$(y^2+u)^2 = (2\cdot u - A)\cdot\left(y - \frac{B}{2\cdot(2\cdot u - A)}\right)^2 - \frac{B^2}{4\cdot(2\cdot u - A)} - C + u^2 \qquad \textbf{(49.39)}$$

The right hand side of this equation can be expressed as a perfect square if the following constraint is imposed.

$$-\frac{B^2}{4\cdot(2\cdot u - A)} - C + u^2 = 0 \qquad \textbf{(49.40)}$$

This can be rearranged to the following cubic equation.

$$8\cdot u^3 - 4\cdot A\cdot u^2 - 8\cdot C\cdot u + 4\cdot A\cdot C - B^2 = 0 \qquad \textbf{(49.41)}$$

This is a cubic equation and can be solved using the methods presented. Let u_0 be a real root of this equation. Then we substitute this back into (49.39) and get the following equation.

$$(y^2+u_0)^2 = (2\cdot u_0 - A)\cdot\left(y - \frac{B}{2\cdot(2\cdot u_0 - A)}\right)^2 \qquad \textbf{(49.42)}$$

One can take the square root of this equation and solve for *y*.

$$y^2 + u_0 = \pm\sqrt{2\cdot u_0 - A}\cdot\left(y - \frac{B}{2\cdot(2\cdot u_0 - A)}\right) \qquad \textbf{(49.43)}$$

This can be rearranged into a quadratic form that can be solved.

$$y^2 \mp y\cdot\sqrt{2\cdot u_0 - A} + \left(u_0 \pm \frac{B}{2\cdot\sqrt{2\cdot u_0 - A}}\right) = 0 \qquad \textbf{(49.44)}$$

The above method can be used to find all four roots for *y,* and this can be used to find all the roots of the original equation.

This being said, it turns out that there is a substitution that can be introduced simplify the result and also make it more consistent with the formulae that are commonly presented. To do this, introduce the following substitution into (49.41).

$$\frac{z - {a_3}^2/_8}{2} \to u \qquad \textbf{(49.45)}$$

Substituting this in the cubic equation and using the definitions of A, B, and C yields the following cubic equation after some labor.

$$z^3 - a_2 \cdot z^2 + (a_1 \cdot a_3 - 4 \cdot a_0) \cdot z + (4 \cdot a_2 \cdot a_0 - {a_1}^2 - {a_3}^2 \cdot a_0) = 0 \qquad \textbf{(49.46)}$$

Let z_0 be a solution to (49.46) and apply all the substitutions into (49.44).

$$x^2 + \frac{1}{2} \cdot \left(a_3 \pm \sqrt{{a_3}^2 + 4 \cdot z_0 - 4 \cdot a_2}\right) \cdot x + \frac{1}{2} \cdot \left(z_0 \mp \sqrt{{z_0}^2 - 4 \cdot a_0}\right) \qquad \textbf{(49.47)}$$

This can be solved using the regular quadratic equation. Care needs to be taken when dealing with complex numbers and roots to make sure that they do not get switched around.

Fifth and Higher Order Polynomials

For polynomials of order five and higher, it has been proven that there cannot be a general closed form solution that can be written as a finite number of algebraic operations. This is known as *Abel's Impossibility Criteria*.

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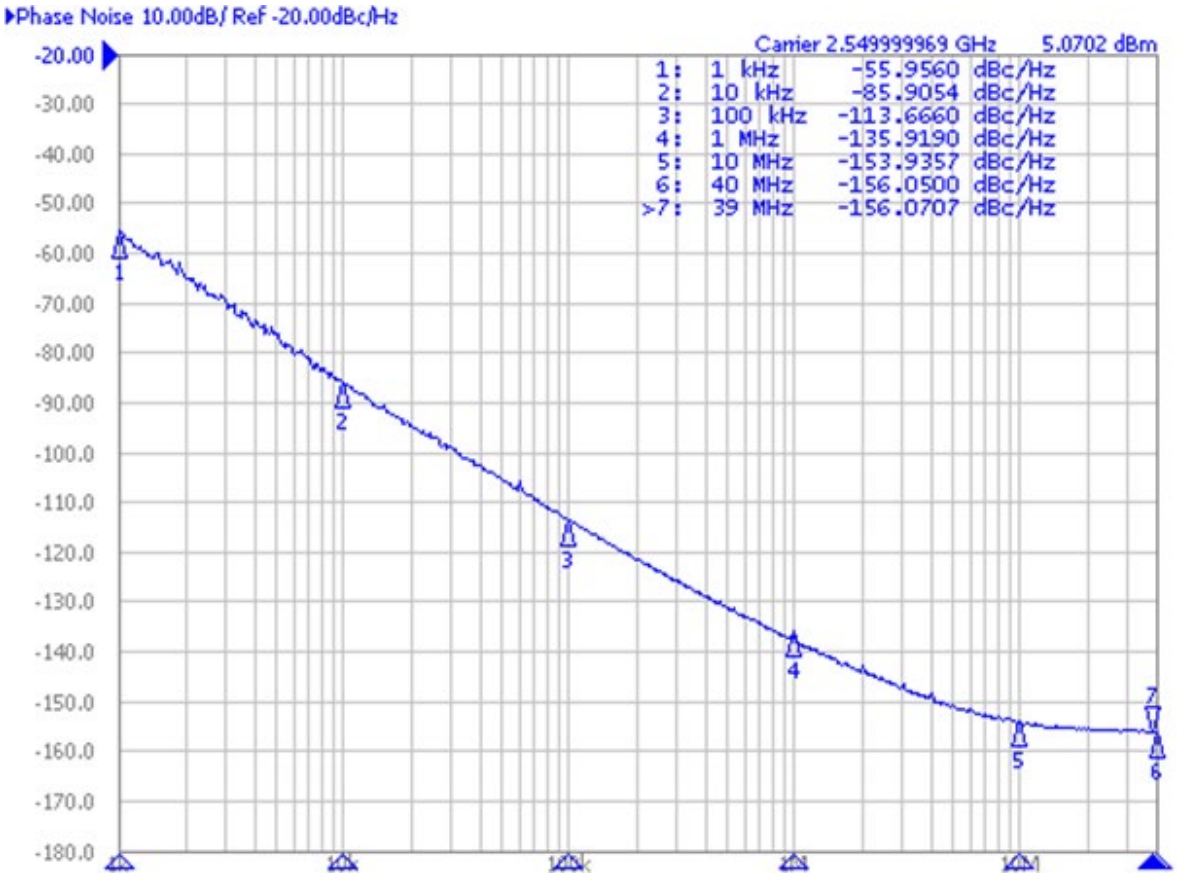
Supplemental Information



Glossary

Channel and Channel Spacing

In many applications, a set of frequencies is to be generated that are evenly spaced apart. These frequencies to be generated are often referred to as channels and the spacing between these channels is often referred to as the channel spacing.

Charge Pump

Used in conjunction with the phase-frequency detector, this device outputs a current of constant amplitude, but variable polarity and duty cycle. It is usually modeled as a device that outputs a steady current of value equal to the time-averaged value of the output current.

Charge Pump Gain (K_{PD})

The output current of the charge pump when it is fully on. Note that this textbook does not divide this by 2π.

Closed Loop Transfer Function, *CL(s)*

This is given by $\frac{G(s)}{1+G(s)\cdot H}$ where $H = \frac{1}{N}$ and ***G(s)*** is the open loop transfer function.

Continuous Time Approximation

This is the assumption that discrete current pulses of the charge pump can be approximated as a continuous current with magnitude equal to the time-averaged value of the current pulses.

Control Voltage, *Vtune*

The VCO tuning voltage that controls the VCO frequency.

Damping Factor, ζ

For a second order transient response, this determines the shape of the exponential envelope that multiplies the frequency ringing.

Dead Zone

This is a region near zero phase error for the phase frequency detector caused by component delays. Since the components making up the PFD have a non-zero delay time, this causes the phase detector to be insensitive to very small phase errors.

Dead Zone Elimination Circuitry

This circuitry can be added to the phase detector to avoid having it operating in the dead zone. This usually works by causing the charge pump to always come on for some minimum amount of time.

Delta Sigma PLL

A fractional PLL that achieves fractional N values by alternating the N counter value between two or more values. Usually, the case of two values is considered a trivial case and sometimes called a traditional fractional PLL or a first order modulator.

Fraction, Simplified

In reference to fractional PLLs, this is the fractional part of the N divider simplified to lowest terms.

Fraction, Larger Equivalent

This is a fraction that has the exact same mathematical value, but has the numerator and denominator multiplied by a constant term. For instance, 100000/1000000 is a larger equivalent fraction for 1/10. Sometimes there is a benefit to expressing fractions in larger equivalent forms for fractional PLLs, other times is not or even detrimental.

Fraction, Larger Uneqivalent

This is a fraction that has very close to the same mathematical value, but with a much larger numerator and denominator that do not simplify. For instance, 100000/1000001 is a larger uneqivalent fraction for 1/10. Sometimes there is a benefit to expressing fractions in larger uneqivalent forms for fractional PLLs, other times is not or even detrimental.

Fractional Denominator, *Fden*

The fractional denominator used for in the fractional word in a fractional PLL.

Fractional *N* PLL

A PLL in which the ***N*** divider value can be a fraction.

Fractional Spur

This is a spurs that occur in a fractional N PLL due to the fractional circuitry.

Fractional Spur, Primary

Primary fractional spurs occur at multiples of the phase detector frequency divided by the simplified fractional denominator.

Fractional Spur, Sub-Fractional

Fractional spurs that occur at ½, 1/3, ¼, 1/6, or $1/12^{th}$ of the offset of the primary fractional spur. They depend on the simplified fractional denominator and the modulator order.

Frequency Jump

In reference to the PLL transient response, this is the frequency difference between initial and final (target) frequencies.

Frequency Synthesizer

This is a PLL that has the VCO integrated on the chip, which can be used to synthesize a wide variety of signals.

Frequency Tolerance, *tolerance*

This is the acceptable error tolerance for calculating lock time. If the frequency error is less than this tolerance, the PLL is said to be in lock. Typical values for this are 500 Hz or 1 kHz.

Gamma Optimization Parameter, γ

A loop filter parameter that has some impact on performance, especially lock time. This is often chosen roughly close to one, but not exactly.

$$\gamma = \frac{\omega c^2 \cdot T2 \cdot A1}{A0}$$

Input Reference Frequency, f_{OSC}

The input frequency to a PLL from which the all other PLL frequencies are derived.

Locked PLL

A PLL such that the output frequency is within acceptable tolerance of the desired frequency. In this state, the inputs to the phase detector should be close in phase.

Lock Time

The time it takes for a PLL to switch from an initial frequency to a final frequency for a given frequency jump to within a given tolerance.

Loop Bandwidth, ωc or BW

The frequency at which the magnitude of the open loop transfer function is equal to 1. ωc is the loop bandwidth in radians and BW is the loop bandwidth in Hz.

Loop Filter

A low pass filter that takes the output currents of the charge pump and turns them into a voltage, used as the tuning voltage for the VCO. ***Z(s)*** is often used to represent the impedance of this function. Although not perfectly accurate, some like to view the loop filter as an integrator.

Loop Gain Constant, *K*

This is an intermediate calculation that is used to derive many results.

$$K = \frac{K_{PD} \cdot K_{VCO}}{N}$$

Modulation Domain Analyzer

A piece of RF equipment that displays the frequency vs. time of an input signal.

Modulation Index, β

This is in reference to a sinusoidally modulated RF signal. The formula is given below, where ***F(t)*** stands for the frequency of the signal.

$$f(t) = constant + f_{DEV} \cdot sin(2\pi \cdot f_{MOD} \cdot t)$$

$$\beta = \frac{f_{DEV}}{f_{MOD}}$$

N Divider
A divider that divides the high frequency (and phase) output by a factor of N.

Natural Frequency , ωn

For a second order transient response, this is the frequency of the ringing of the frequency response.

Open Loop Transfer Function, *G(s)*

The transfer function which is obtained by taking the product of the VCO Gain, Charge Pump Gain and Loop Filter Impedance divided by N.

$$G(s) = \frac{K_{PD} \cdot K_{VCO} \cdot Z(s)}{s}$$

Overshoot

In reference to the transient response, this is the amount that the target frequency is initially exceeded before it finally settles in to the proper frequency.

Phase Detector

A device that produces an output signal that is proportional to the phase difference of its two inputs.

Phase detector frequency, f_{PD}

The input reference frequency divided by the ***R*** counter value.

Phase-Frequency Detector, PFD

Very similar to a phase detector, but it also produces an output signal that is proportional to the frequency error as well.

Phase-Locked Loop, PLL

A circuit that uses feedback control to produce an output frequency from an input reference frequency. Note that a PLL does not necessarily have the VCO integrated on the same chip. In the case that it does, it is typically referred to as a frequency synthesizer.

Phase Margin, ϕ

180 degrees minus phase of the open loop transfer function at the loop bandwidth. Loop filters are typically designed for a phase margin between 30 and 70 degrees. Simulations show that around 48 degrees yields the fastest lock time. The formula is given below:

$$\phi = 180^{\circ} - \angle G(j \cdot \omega c)$$

Phase Noise

This is noise on the output phase of the PLL. Since phase and frequency are related, it is visible on a spectrum analyzer. Within the loop bandwidth, the PLL is the dominant noise source. The metric used is dBc/Hz (decibel relative to the carrier per Hz). This is typically normalized to a 1 Hz bandwidth by subtracting 10*(Resolution Bandwidth) of the spectrum analyzer.

Phase Noise Floor

This is the phase noise minus 20·log(N). It is generally not a constant because it tends to be dominated by the charge pump, which gets noisier at higher phase detector frequencies.

Pole Sum Constant, κ

This is an intermediate constant used in loop filter design and is an approximation the sum of the poles of the loop filter. It can be calculated directly from the poles or from the loop filter coefficients.

$$\kappa = T1 + T3 + T4 = {}^{A1}/_{A0}$$

Prescaler

Frequency dividers included as part of the ***N*** divider used to divide the high frequency VCO signal down to a lower frequency.

Quality Factor (Q)

The ratio of the imaginary reactance to the resistance of an inductor at a given frequency.

R Divider

A divider that divides the input reference frequency (and phase) by a factor of R.

Rolloff

The closed loop gain of the PLL minus 20·log(N) at a particular frequency of interest. Typically this term is used in spur calculations.

Sensitivity

Power limitations to the high frequency input of the PLL chip (from the VCO). At these limits, the counters start miscounting the frequency and do not divide correctly.

Smith Chart

A chart that shows how the impedance of a device varies over frequency.

Spectrum Analyzer

High frequency test equipment that displays the power vs. frequency for an input signal. This piece of equipment works by taking a frequency ramp function and mixing it with the input frequency signal. The output of the mixer is filtered with a bandpass filter, which has a bandwidth equal to the resolution bandwidth. The narrower the bandwidth of this filter, the less noise that is let through.

Spur

Undesired noise concentrated in a very narrow bandwidth at some specified offset from the carrier. There are many different types of spurs and they are often named by the offset from the carrier. In many cases, they occur at equal offsets to the right and left of the carrier.

Spur Gain, *SG*

This refers to the magnitude of the open loop transfer function evaluated at the phase detector frequency. This gives a good indication of how the reference spurs of two loop filters compare.

Stability

The ability for a PLL to stay at a locked frequency.

Stability, Discrete Sampling

PLL stability determined the discrete sampling action of the phase detector not being too wide relative to the loop bandwidth as to cause the PLL to lose lock.

Stability, Transfer Function

PLL stability determined by all the poles of the closed loop transfer function having no positive real parts.

T31 Ratio (T3/T1 Ratio)

This is the ratio of the poles of a third order loop filter. If this ratio is 0, then this is actually a second order filter. If this ratio is 1, then this turns out to be the value for this parameter that yields the lowest reference spurs.

T43 Ratio (T4/T3 Ratio)

This is the ratio of the pole ***T4*** to the pole ***T3***. A rough rule of thumb is to choose this no larger than the ***T31*** ratio.

Temperature Compensated Crystal Oscillator, TCXO

A crystal that is temperature compensated for improved frequency accuracy.

Varactor Diode

This is a diode inside a VCO that is reverse biased. As the tuning voltage to the VCO changes; it varies the junction capacitance of this diode, which in turn varies the VCO voltage.

Voltage Controlled Oscillator, VCO

A device that produces an output frequency that is dependent on an input (Control) voltage.

Symbols an Abbreviations

Loop Filter Parameters

A0, A1, A2, A3	Loop Filter Coefficients
C1, C2, C3, C4	Loop filter capacitor values
CL(s)	Closed loop PLL transfer function
f	Frequency of interest in Hz
BW	Loop bandwidth in kHz
f_{OSC}	Input reference frequency
f_{PD}	Phase detector frequency
f_{SPUR}	Spur Frequency
f_{VCO}	VCO Frequency
f_{OUT}	PLL output frequency after potential VCO divider
f_N	VCO frequency divided by N
f_R	FOSC frequency divided by R
Fden	Fractional denominator
Fnum	Fractional Numerator
G(s)	Loop filter transfer function
H	PLL feedback, which is 1/N
i, j	The complex number $\sqrt{-1}$
K	Loop gain constant.
K_{PD}	Charge pump gain in mA/(2π radians)
K_{VCO}	VCO gain in MHz/V
N	***N*** divider Value
PFD	Phase/Frequency Detector
PLL	Phase-Locked Loop
r	Ratio of the spur frequency to the loop bandwidth
R	***R*** divider value
Q	The quality factor of the inductor = Reactance/Resistance
R2, R3, R4	Loop filter resistor values
s	Laplace transform variable = $2\pi \cdot f \cdot j$

T2	The zero in the loop filter transfer function
T1, T3, T4	The poles in the loop filter transfer function
T31, ***T3/T1***	The ratio of the pole ***T3*** to the pole ***T1***
T43, T4/T3	The ratio of the pole ***T4*** to the pole ***T3***
tolerance	Frequency tolerance for lock time
Vcc	The main power supply voltage
VCO	Voltage Controlled Oscillator
Vpp	The power supply voltage for the PLL charge pump
Z(s)	Loop filter impedance
Z_L	Load Impedance
Z_0	Line Impedance

Greek Symbols

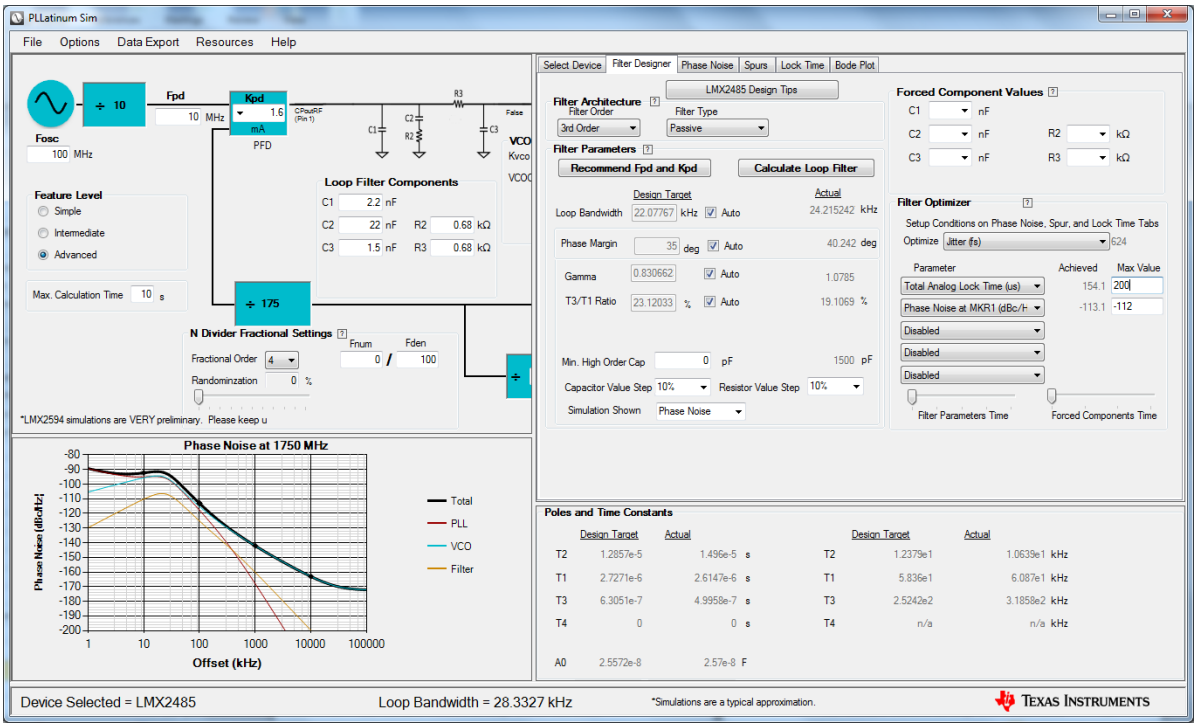
β	The modulation index
κ	The pole sum constant
ϕ	The phase margin
ϕ_R	The output phase of the R divider
ϕ_N	The output phase of the N divider
ω	The frequency of interest in radians
ωc	The loop bandwidth in radians
ωn	Natural Frequency
ζ	Damping Factor
γ	Gamma Optimization Parameter

Software Recommendations

PLLatinum Sim Tool

http://www.ti.com/tool/pllatinumsim-sw

This tool is very comprehensive and the formulae are very consistent with what is in this book. This tool is free to download and does very comprehensive filter design as well as simulations for bode plot, phase noise, spurs, and lock time. This tool is strongly based on the formulae and concepts in this book.

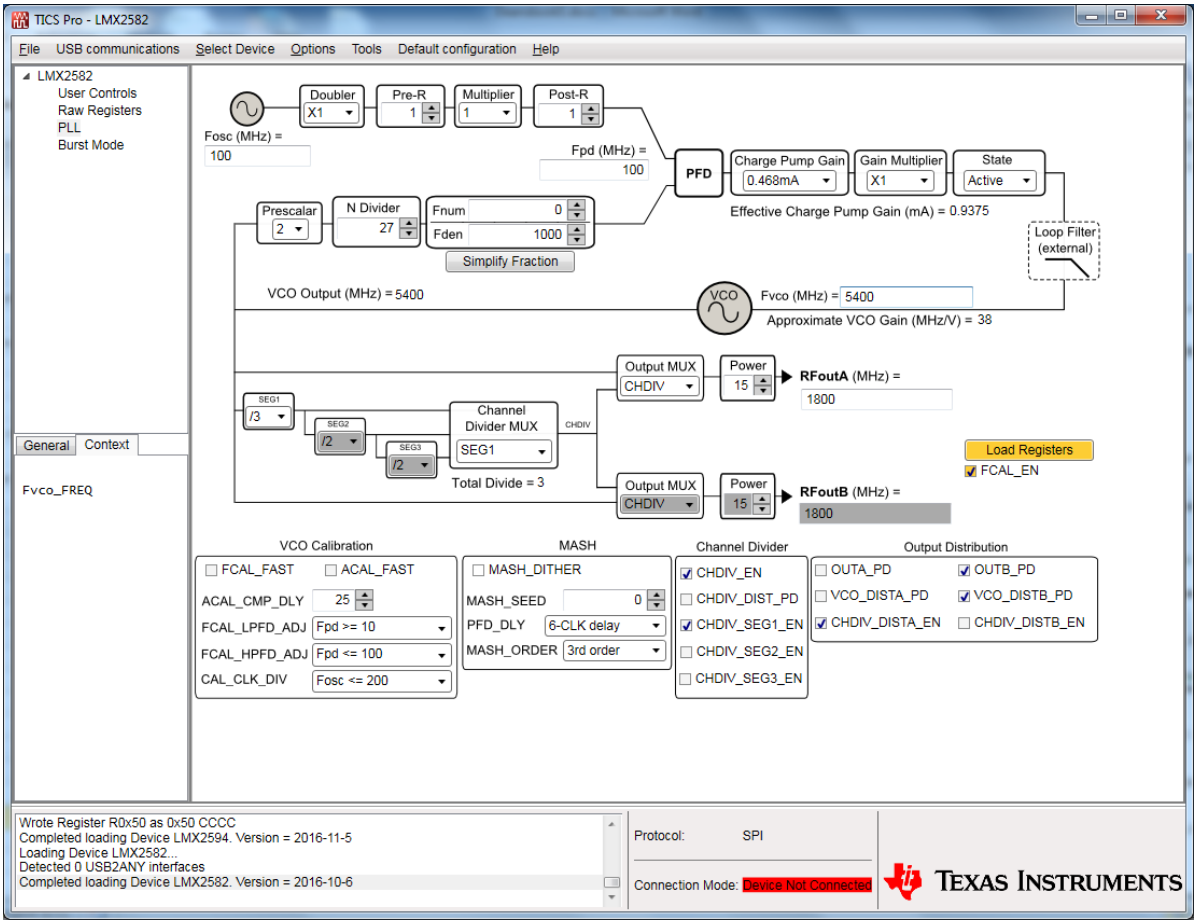


It does comprehensive filter design and simulates phase noise, spurs, and lock time. It allows import and export of phase noise data and has three feature levels to allow users of all levels to be able to use this tool.

TICSPro Programming Tool

http://www.ti.com/tool/TICSPRO-SW

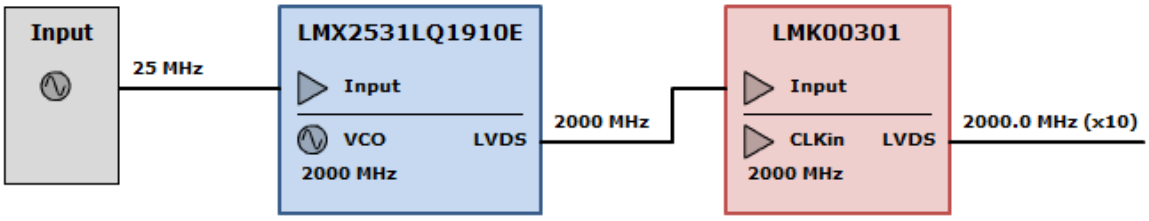
This tool is for programming Texas Instruments PLLs and gives a great understanding of how the registers interact. It can be useful for programming evaluation boards, but is also useful without an evaluation board to understand the register programming.

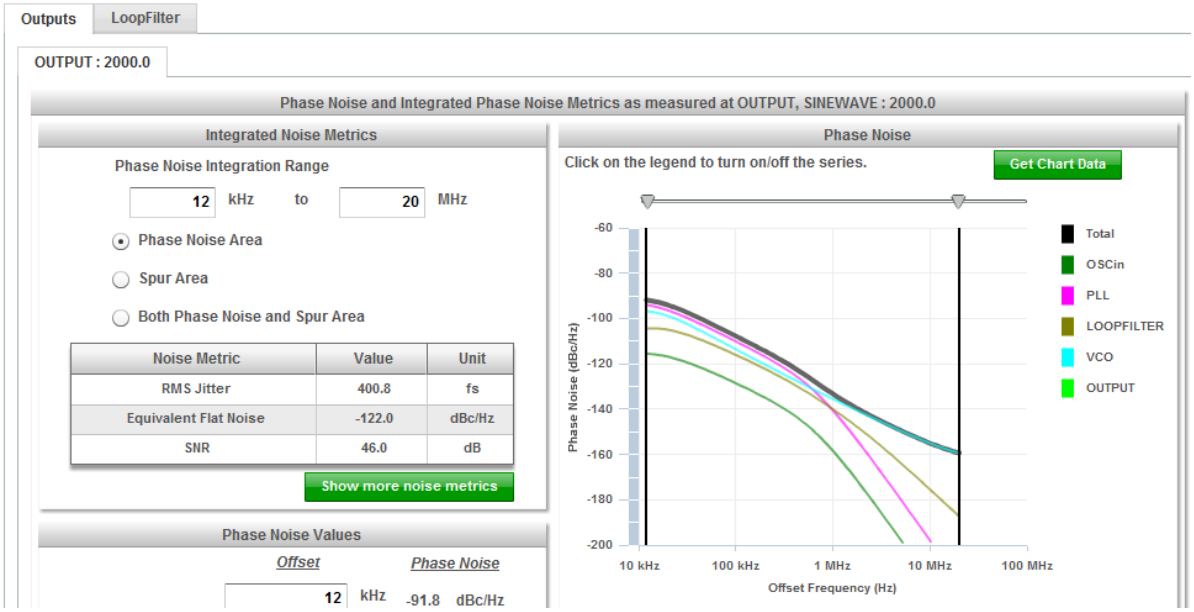


Clock Architect Tool

https://webench.ti.com/webench5/power/webench5.cgi

This is the Texas Instruments clock architect that allows the creation and simulation of solutions using multiple devices. The design equations also are strongly based on the formulae in this book. When going to the website, be sure to select the clocks tab.





Other Websites

http://tools.rfdude.com/

Lance Lascari's RF Tools Page. The Mathcad based PLL design worksheet is pretty good.

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Stephen Hoffman		X			
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