TI Designs

4K UHD display chip sub-system Reference Design featuring DLP660TE and DLPC4422

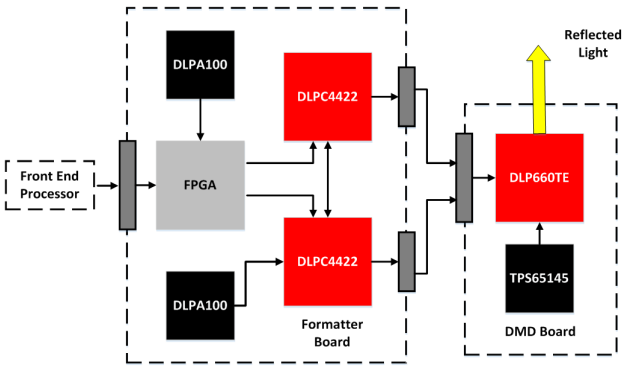
Description

4K ultra-high definition (UHD) projection displays can be used in laser TV, home theater, digital signage, and smart lighting. At the core of these products is a DLP imaging chipset that creates high quality digital displays. This design guide explains how to integrate TI's first mainstream 4K UHD chipset into display systems requiring bright, high resolution video and image projection.

Resources

TIDA-01347	Design Folder
DLP660TE	Product Folder
DLPC4422	Product Folder
DLPA100	Product Folder
TPS65145	Product Folder

TI E2E™ Community — Ask Our E2E Experts



Features

- DMD board includes the DLP660TE
- Formatter board includes the DLPC4422 digital controller and DLPA100 PMIC and motor driver
- Combining the DMD board and Formatter board with an appropriate optical engine and illumination source enables displays up to 5000 lumens and 3840 x 2160 resolution
- PC software GUI to reprogram and control the system

Applications

ti.com/dlp4kuhd

- Laser TV
- Digital Signage
- Business and Education Display

1 System Overview

1.1 Key System Level Specifications

Table 1. Key System Specifications - Electronics

PARAMETER	SPECIFICATION
Vin Voltage	12V
Power Consumption	Power consumption depends on light source and power design efficiency. The TI Reference electronics (no light source) draw 27 Watts (including fans and optical actuator)
Required Software	TI provides all firmware required in the FPGA and the base software for the DLPC4422 to control the DMD, fans, light source, etc. The end system designer has some control over high level controller software (display color and modes, on-screen display, and more.) See Section 5.
DMD Handling	Follow all TI recommendations concerning proper handling and assembly of the DMD to avoid permanently damaging the device - see DLP660TE datasheet.
DMD Thermal Load	The DMD is designed to conduct absorbed and dissipated heat to the back of the package. The cooling system must be capable of maintaining the package within the temperature range specified in the datasheet. For example, the Array Temperature, Long-term operational must be kept between 10°C and 70°C depending on micromirror landed duty cycle. See DLP660TE datasheet.
DMD Illumination Wavelengths and Power	< 395 nm: Maximum 2 mW/cm2
	Between 395 nm and 800 nm: Thermally limited
	> 800 nm: Maximum 10 mW/cm2 See DLP660TE datasheet

Table 2. Key System Specifications - Electronics with Optical Engine

PARAMETER	SPECIFICATION
Maximum Projected Lumens	5000
Display Resolution	Up to Ultra HD (3840 x 2160 pixels on screen)
Supported Light Sources	Lamp, LED, Direct Laser, Laser Phosphor, and Hybrid illumination
Optical Engine Design	The DLP660TE supports both telecentric and non-telecentric optical engine designs

1.2 Applications

Laser TV is an emerging group of products that offer large, bright projections by utilizing a laser light source. Laser light sources are longer lasting and more efficient that more traditional lamps, and can be incorporated into a wide array of electronic media devices. By combining laser illumination sources with DLP® technology, developers can create beautiful, high brightness images and videos without the need for bulky panels, or even projection screens. Developers interested in ultra-low power solutions (including mobile applications) should reference DLP Smart TV products.

Digital signage is an application for displaying information and digital content for a target audience, such as menus, navigation guides, event statuses, and advertising in hotels, restaurants, airports, and other large public area. Combine network connectivity with digital signage to create dynamic content and incorporate user interactivity. DLP technology can be used to create bright, free-form displays on a wide range of surfaces indoors and outdoors. For ultra-mobile Digital Signage, visit DLP Pico Technology.

Business and Education projection solutions offer bright, high-resolution, easily readable content for viewing presentations, video, and even high-detail spreadsheets in the classroom and at the office. Developers can choose illumination sources including lamps, LEDs, laser, and laser phosphor to create the right product for any environment or room size. High resolution, large screen displays enabled by DLP technology allow everyone in the classroom or the conference room to easily read and see details in presentations and lectures.

1.3 System Description

The DLP® 0.66” 4K UHD chipset combines the fast switching speed of the Digital Micromirror Device (DMD) with advanced image processing to bring 4K Ultra HD solution to new markets. The chipset consists of the high-resolution DLP660TE DMD, the high-speed DLPC4422 digital controller, and dedicated DLPA100 power management IC and motor driver. These devices can be combined with many different optical and mechanical components to meet a diverse set of performance level requirements.

This reference design offers designers electrical component selection, high speed data trace routing, electrical and software control of the DLP660TE DMD, as well as optical design choices such as illumination type and third party optical engine information.

1.4 Block Diagram

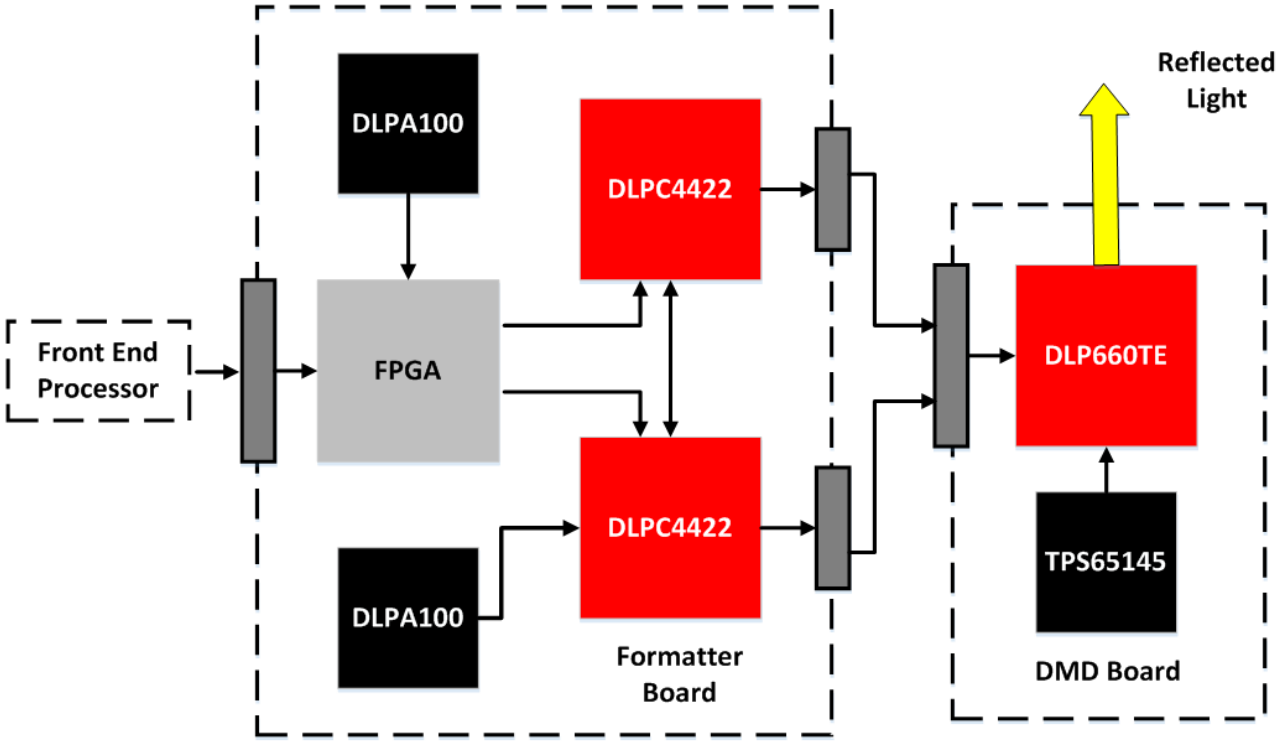


Figure 1. System Block Diagram

1.5 Highlighted Products

1.5.1 DLP660TE

The DLP660TE digital micromirror device (DMD) is based on a breakthrough micromirror technology, called TRP. With a smaller pixel pitch of 5.4 μm and increased tilt angle of 17 degrees, TRP chipsets enable high resolution in a smaller form factor, and enhanced image processing features, while maintaining high optical efficiency. Figure 2 is a block diagram that describes at a high level the internal hardware control circuitry inside the DLP660TE DMD.

Features

- 0.66-Inch diagonal micromirror array
  - 2716 × 1528 array of aluminum micromirrors
  - 5.4 micron micromirror pitch
  - ± 17° micromirror tilt (relative to flat surface)
  - bottom illumination
- 2x LVDS input data bus
- DLP technology high switching capability paired with an optical actuator enables 829 million onscreen pixels

Not to Scale. Details Omitted for Clarity. See Accompanying Notes in this Section.

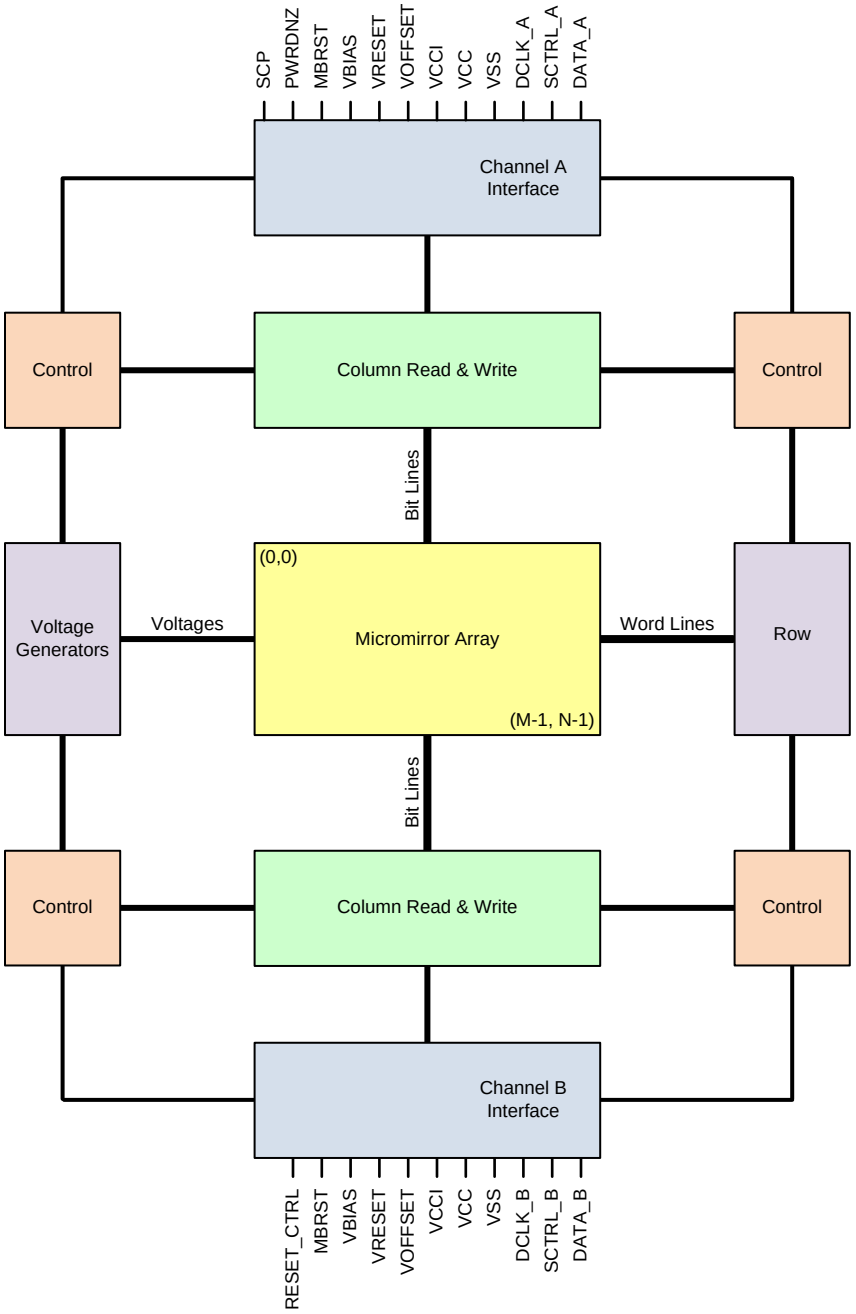


Figure 2. DLP660TE Block Diagram

1.5.2 DLPC4422

The DLPC4422 is a video and imaging controller chip that integrates all the DMD data formatting onto a single integrated circuit. It provides 1 Gbit of internal DRAM for all data path processing needs. The DLPC4422 processes the digital input image and converts the data into bit-plane format as needed by the DLP660TE. The image data is 100% digital from the DLPC4422 input port to the image projected on to the display screen. The image stays in digital form and is never converted into an analog signal. This reference design utilizes two DLPC4422 controllers to handle the large amount of data required to produce a UHD display at 60 frames per second. Figure 3 shows a functional block diagram of the internal video processing provided by the DLPC4422 controller. Some of the important processing steps include Chroma Interpolation, Color Space Conversion, and De-Gamma. See the DLPC4422 datasheet for more information on these and other features.

Features

- Provides for two 30-bit input pixel ports, which can be used as one 60-bit port (two pixels per clock)
  - 8, 9, or 10 bits per color
  - Pixel clock support up to 175 MHz for 30-bit, 160 MHz for 60-bit
  - High speed, low voltage differential signaling (LVDS) DMD interface
- Microprocessor peripherals:
  - 83 OEM programmable GPIO pins
  - Programmable PWM and capture timers
  - One USB 1.1 slave port
- System control
  - Built-in lamp ballast control
  - DMD power and reset driver control
  - DMD horizontal and vertical image flip
  - Supports lamp, hybrid, LED, and laser systems

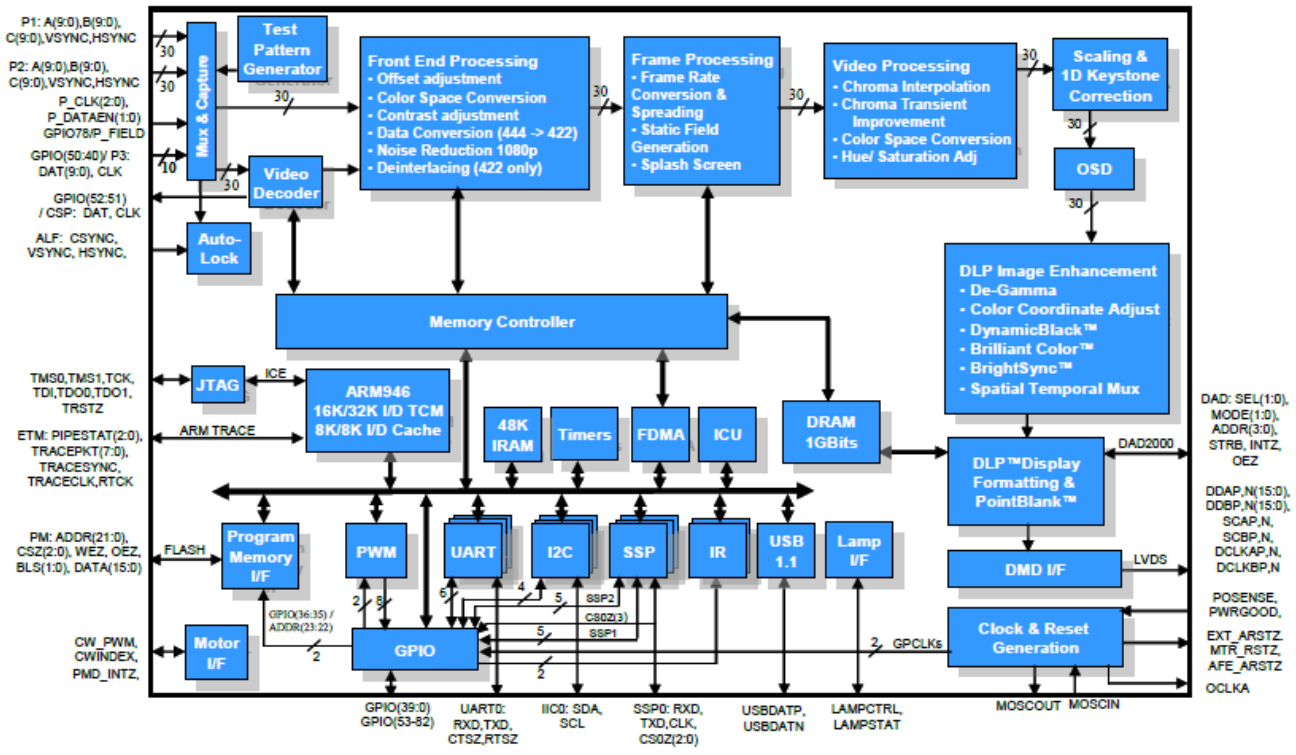


Figure 3. DLPC4422 Block Diagram

1.5.3 DLPA100

The DLPA100 is a power management solution and motor driver in one integrated circuit. The DLPA100 provides multiple linear and switching power regulators to power the DLP660TE, the two DLPC4422s, the FPGA, and other electronics in the TIDA-01347 reference design. The DLPA100 also contains a 3-phase BEMF motor driver and a motor supply switching regulator to power, spin, and control color-wheels and phosphor-wheels if needed by the end application of the TIDA-01347 design. Figure 4 shows a functional block diagram of the internal logic blocks in the DLPA100. For a more detailed description of these blocks, see the DLPA100 datasheet.

Features

- 2.5V fixed, 3.3-V fixed, 5V fixed, and 1.0V-3.3V adjustable switching regulators
- 2 Adjustable linear regulators with enable
- Power supply sequencing control
- Three fan drivers
- 3-phase BEMF motor driver/controller
- Motor supply switching regulator

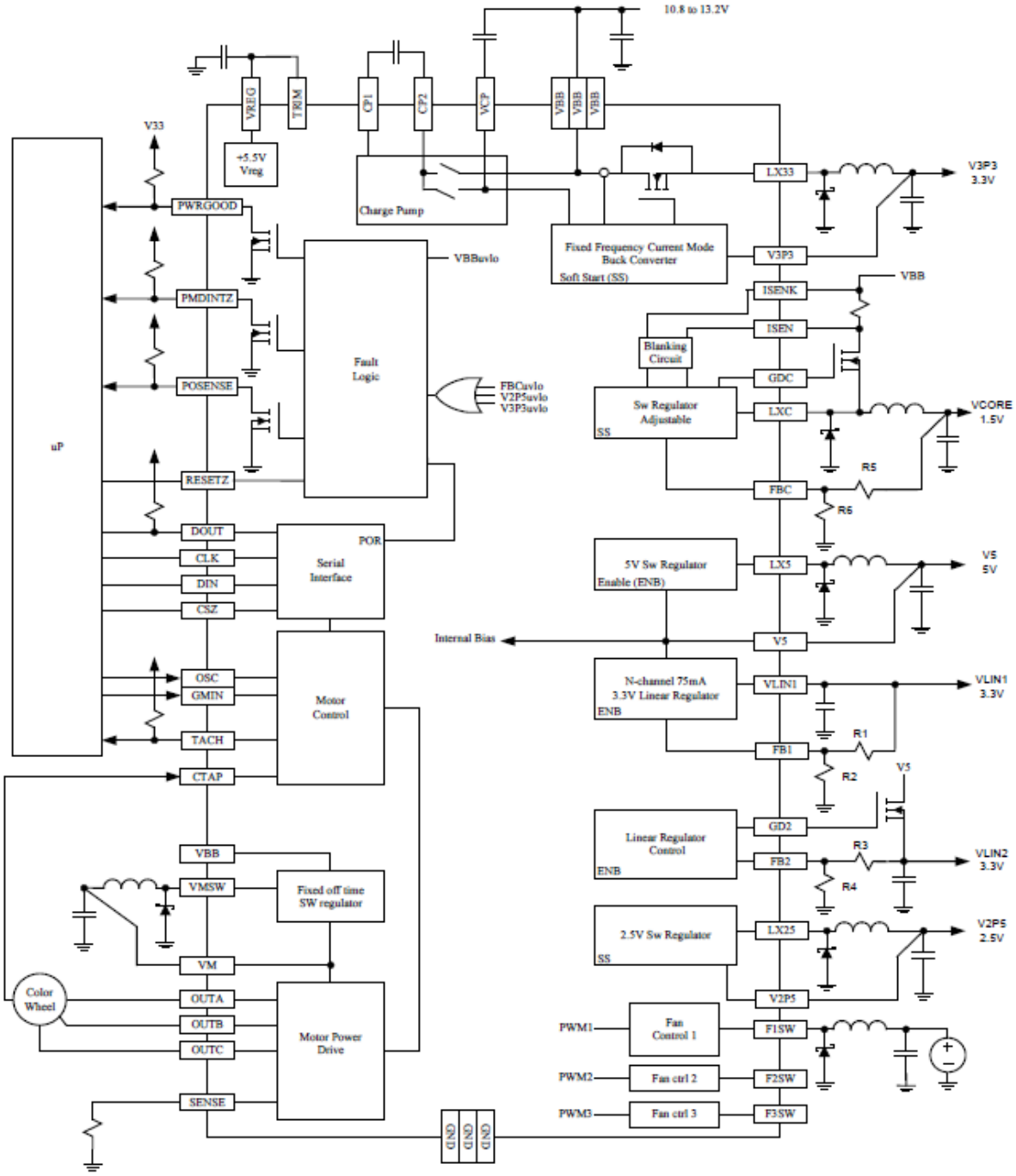


Figure 4. DLPA100 Block Diagram

1.5.4 TPS65145

The TPS65145 offers a compact and small power supply solution to provide all three voltages required to control the DMD mirrors (VOffset, VReset, VBias - see reference design). The TPS65145 provides control of power-up sequencing of the three voltage outputs to ensure correct power-up of the DLP660TE DMD. Due to the high 1.6-MHz switching frequency of the charge pumps, inexpensive and small capacitors can be used. Additionally, the TPS65145 has a system power good output to indicate when all supply rails are acceptable for the DMD. Figure 5 shows a functional block diagram of the internal logic blocks in the TPS65145. For a more detailed description of these blocks, see the TPS65145 datasheet.

Features

- 2.7-V to 5.8-V input voltage range
- 1.6 MHz fixed switching frequency
- 3 independent adjustable outputs
- Internal power-on sequencing
- System power good

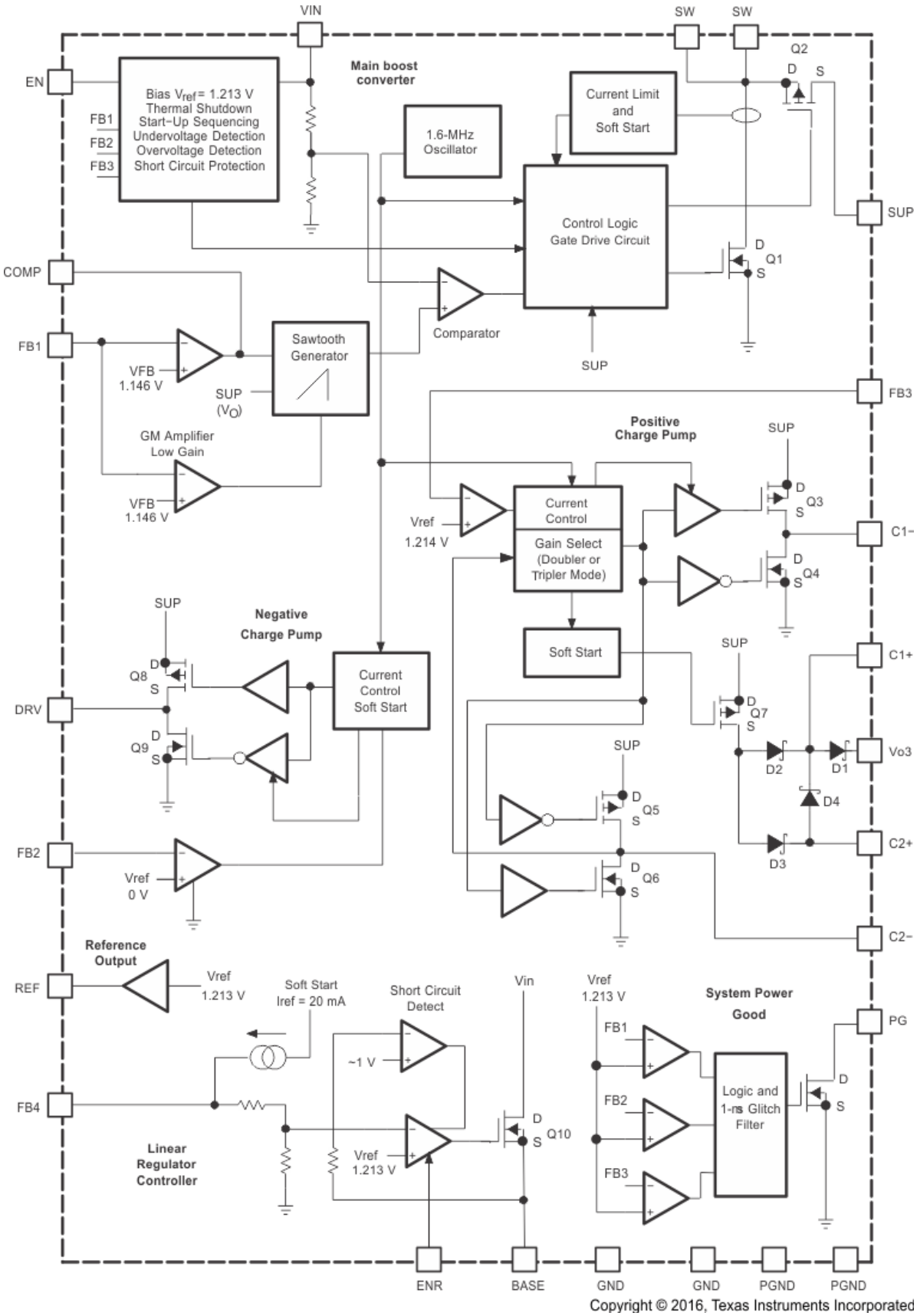


Figure 5. TPS65145 Block Diagram

2 Getting Started Hardware and Software

2.1 Hardware

This reference design can be applied to a wide variety of projection and display systems. The electronics that drive these systems will therefore have a great deal of variability to suit the application. This section will describe the minimum steps needed to get the TIDA-01347 reference design up and running in order to send video and imaging data to the DMD. Any deviation from the reference design may require additional steps before the system is up and running.

Power Supply

TI recommends using an AC power adaptor with a 12V output at 5A to power the TIDA-01347 reference design. The power supply TI uses is:

Manufacturer: PHIHONG

Model: PSAA60M-120

Jumpers

Within this design, Jumpers are defined as a small conductor capable of shorting two pins on the reference design PCB together. This circuit change is detected by the DLPC4422 and is used to customize the performance of the reference design. Jumper selections needed to get TIDA-01347 reference design up and running will depend on design choices made during schematic capture and layout. On the TI reference design PCB, the jumpers which need to be connected for a lamp-illuminated system to power-up are listed in Figure 6. The jumper locations on the TI reference design PCB are shown in Figure 7.

Jumper	Description
J11	Power Main Board from Front End Board
	Uninstalled - Main Board is powered from its own AC adaptor (Default)
	Installed - Front End Board can provide 12 V with enough current to power the Main Board
	NOTE: DO NOT INSTALL THIS JUMPER IF ALSO USING POWER INPUT (J22)
J14	Blue LED enable or Lamp Ballast
	Pins 1,2 connected Blue LED Enable
	Pins 2,3 connected Lamp Mode
J28	TDO1 or TDO2
	Pins 1,2 connected TDI in to slave is from TDO1 from Master
	Pins 2,3 connected TDI in to slave is from TDO2 from Master
J29	Manual Reset
	Uninstalled – Normal Operation (Default)
	Installed – Hold in reset
J31	Hold in Boot Loader
	Uninstalled – Normal Operation (Default)
	Installed – Hold in Boot Loader
J32	Vx1 Swap P/N
	Uninstalled - Swapping P and N
	Installed - Not swapping P and N (Default)
J33	Vx1 Swap Bit Order
	Uninstalled - Swapping Bit Order
	Installed - Not swapping Bit Order (Default)
J34	LED Enable invert
	Pins 1,2 connected LED_EN inverted
	Pins 2,3 connected LED_EN not inverted (Default)
J38	Light to Frequency Sensor or ADC Integrating Sensor
	Pins 1,2 connected ADC Integrating Sensor (Default)
	Pins 2,3 connected Comparator Sensor
J40	High current Fan 5 or Fan 6
	Pins 1,2 connected for high current Fan 5
	Pins 2,3 connected for Fan 6 (default)

Figure 6. Jumper Description

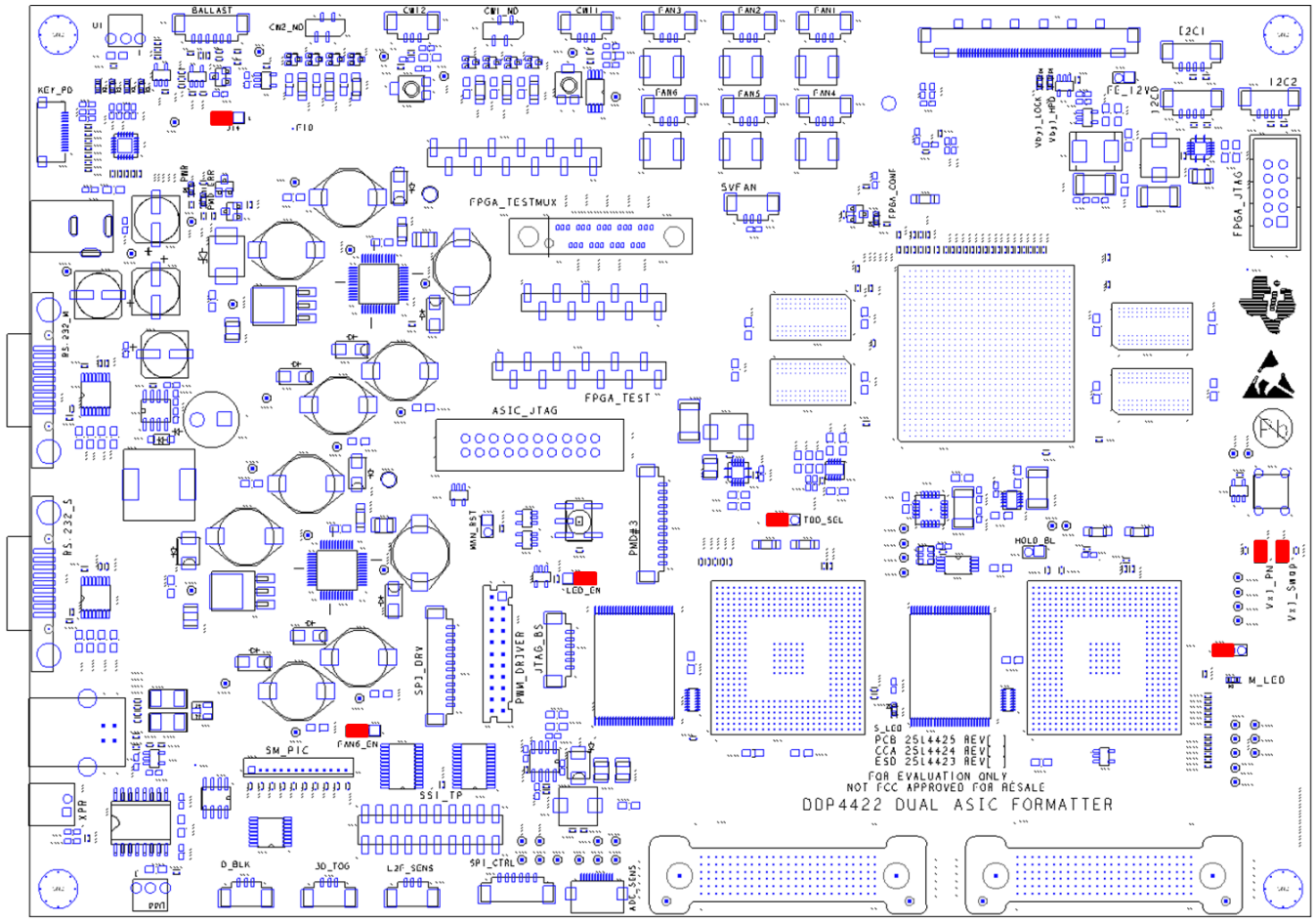


Figure 7. Jumper Locations

Connections

Cable connections needed to get TIDA-01347 reference design up and running will depend on design choices made during schematic capture and layout. On the TI reference design PCB, the connections which need to be made for a lamp-illuminated system to power-up are listed below.

- DMD, DMD Board, Flex Cables
  - Use flat-head screwdriver to turn DMD socket locking screw counter-clockwise to move the socket to unlocked position
  - Position the DLP660TE DMD in place on the DMD socket
  - Turn locking screw clockwise to secure the DMD
  - Secure the DMD board and DMD against system optics (or leave on bench for visual evaluation of DMD mirrors)
  - Attach flex cables from DMD board to Formatter board – method will vary depending on flex cable choice. Follow instructions from manufacturer.
- PWM controlled Fans
- Color Wheel Index
- Color Wheel Motor Drive
- Lamp Ballast
- Actuator Driver
- Keypad

Other illumination sources will need different connections depending on illumination type, illumination driver circuit, fans, number of color and/or phosphor and/or filter wheels. Designers should consult with third party OEM to determine connections needed for their specific use.

Initialize the System

To initialize the system:

1. Move switch SW1 to Park
2. Apply power to illumination power supply
3. Apply +12V DC power to the TIDA-01347 electronics
4. Move switch SW1 to Run
5. There should be a heartbeat blinking from diode D11

2.2 Bootloader

The TIDA-01347 reference design requires specialized software written by TI to run the DLPC4422, to perform image processing on the FPGA, and to control the DLP660TE DMD. To be able to install the DLPC4422 software and the FPGA firmware onto the electronics after assembly, the DLPC4422 Flash memory must have an ARM bootloader programmed into it. To ensure functionality of the electronics during first start up, TI recommends loading the ARM bootloader into the DLPC4422 Flash before the assembly of the electronics. Many third party Flash retailers and PCB assembly shops offer Flash loading services with the bootloader binary provided with this TI Design.

Once the Flash has been loaded with the bootloader and assembled onto the PCB, the ASIC software for the DLPC4422 can be loaded onto the board from a PC via USB.

2.3 Software

The DLPC4422 controller includes a Windows™ based GUI application to control the module through I2C commands. This section provides instructions on where to find the TI-provided software and how to use features provided by the GUI application to communicate with the DLPC4422 controller.

2.3.1 Set Up DLP Composer™ Lite Tool Suite

2.3.1.1 System Requirements

The following list shows the minimum recommended system requirements for the DLPC4422 Composer Lite GUI application software:

- PC with 1.4 GHz Pentium IV CPU or higher
- Windows™ XP SP3 or higher
- 512 MB of RAM
- 10 MB of free hard-disk space
- USB Port

The user needs to have an I2C converter box. For more details, see the following websites and check for:

- USB-I2CIO USB interface hardware at www.devasys.com
- USB-to-I2C Professional at www.i2ctools.com/products.html

2.3.1.2 DLPC4422 Composer Lite GUI Software Installation

Download the installation setup for DLPC4422 Composer Lite GUI PC software from www.ti.com/product/DLPC4422 to the desired folder in your PC. Execute DLPC6401 GUI v1.0 Setup.exe, and follow the instructions for software installation.

2.3.1.3 Communication Interface Driver Installation

When using the DLPC4422 Composer Lite GUI, the user must have a communication link established between the DLPC4422 controller and the computer running this software. This allows the user to read and write to the controller from the computer. The DLPC4422 Composer Lite GUI supports the I2C. The user needs to install device drivers for the I2C adaptors from the following websites:

- DeVaSys USB-to-I2C driver at www.devasys.com
- USB-to-I2C Professional drivers at www.i2ctools.com/products.html

2.3.1.4 DLP660TE Software Files

Download the DLP660TE software files to the desired folder in your PC. This zip file contains the flash image and files needed to communicate with the DLPC4422 controller.

- DLPC4422_p66_TRP_UHD_xxx.img – Flash image to configure DLPC4422 controller per illumination
- DLPC4422_FPGA.rpd – Image file to configure FPGA
- DLPC4422xf.projector – Projector control file used to communicate with the DLPC4422 via the DLP Composer Lite GUI
- FlashDeviceParameters.txt – Required by DLP Composer Lite GUI tool to define the flash parameters

2.3.1.5 User Interface Overview

When the installation successfully completes, execute “DLPLite.exe” from Start → All Programs, or from the shortcut provided on the desktop. When the application starts, the following GUI screen displays. The GUI window contains these sections:

- Project Tree Pane: The project tree pane lists the projector control tool and flash loader tool, which are used to communicate with the DLPC4422 controller. Select a tool to open the associated tool pane and any tabs or toolbars.
- Tool Pane: The tool pane displays the active panel for the tool selected in the project tree.
- Output Log Window: The output log window displays information associated with the user's project and is mostly used for debugging. The output log window has its own set of tool tabs (projector control and so forth) located at the bottom of the window that allows the user to toggle through the various tool output logs without changing the active tool in the tool pane.
- Menu Bar: The menu bar contains several menus the user can click to access other features, such as editing preferences (Edit → Preferences).
- Toolbar: This bar contains common support functions for the project selected from project tree pane.

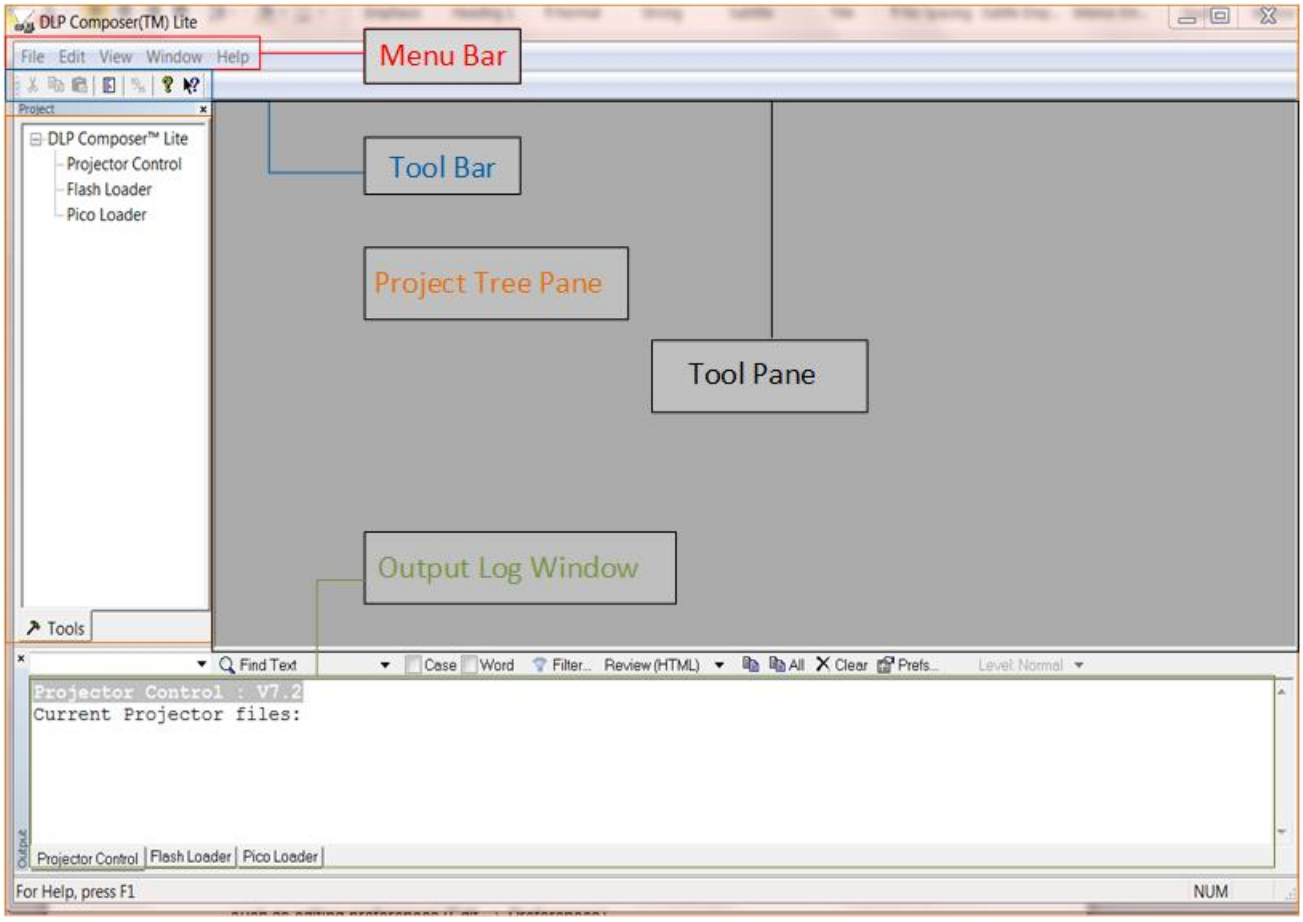


Figure 8. DLP Composer Lite GUI

2.3.1.6 Using the Edit Menu

Select Preferences from the Edit menu to specify DLP Composer Lite GUI options:

- Output window and logging options
- Communication options
- Flash loader options

Output Window and Logging Options

1. From the Edit menu, select Preferences (The Preferences dialog box appears).
2. Click Output - Memory / Log and Output - Font / Speed, and select features as desired
3. Click OK

2.3.1.7 I2C Interface

1. Select I2C interfaces using one of these options
   - DeVaSys
   - I2C Tools
   - Cypress
2. At the end of the dialog box, select 100 kHz as the I2C speed
3. Click OK

Note: All other communication interfaces should be ignored for this device.

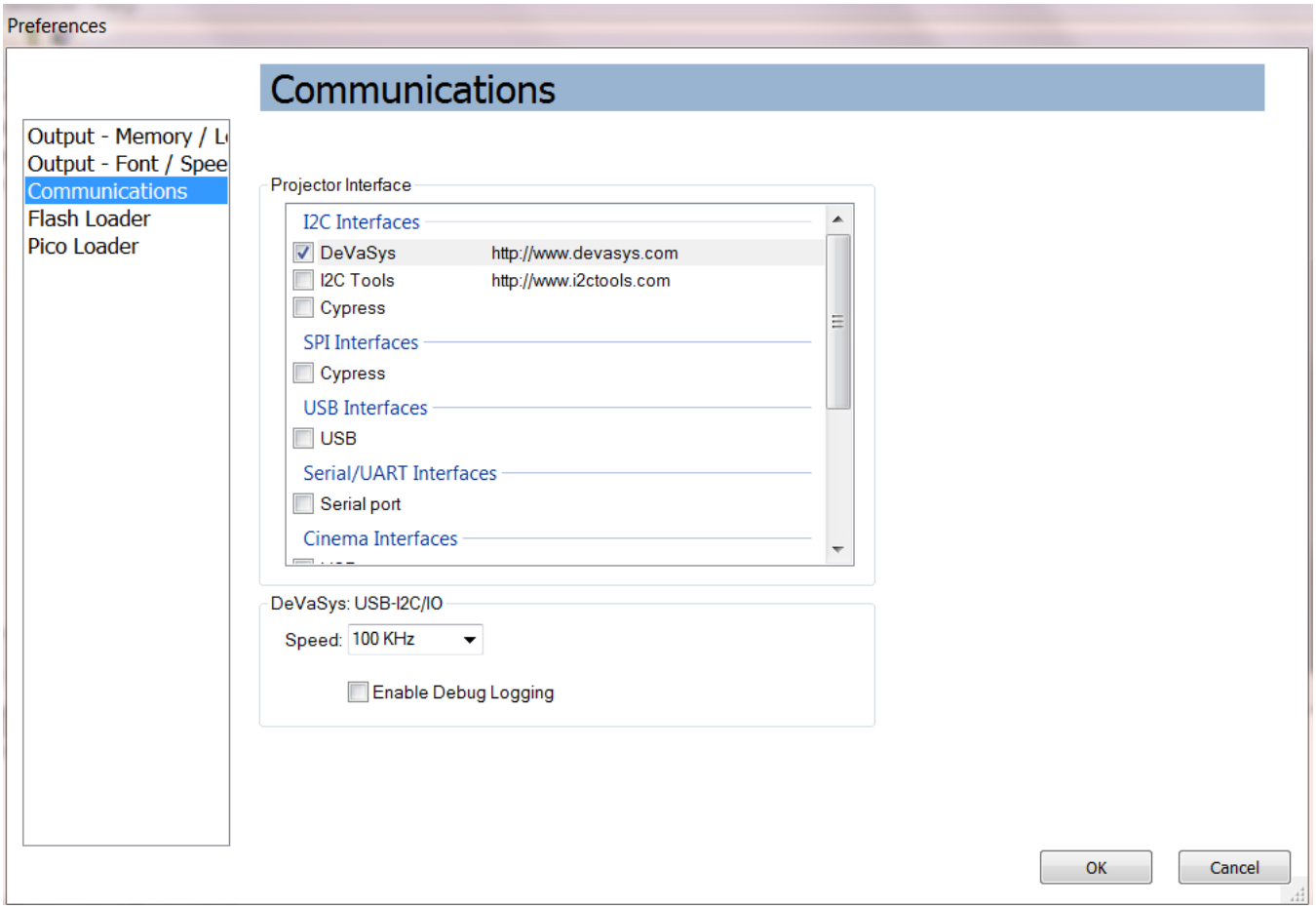


Figure 9. I2C Communications Options

2.3.1.8 Flash Loader Options

1. Set the Auto Restart Timer
2. Select 3000 milliseconds as the Programming Mode Delay
3. At the end of the dialog box, select 100 kHz as the I2C speed
4. Click OK

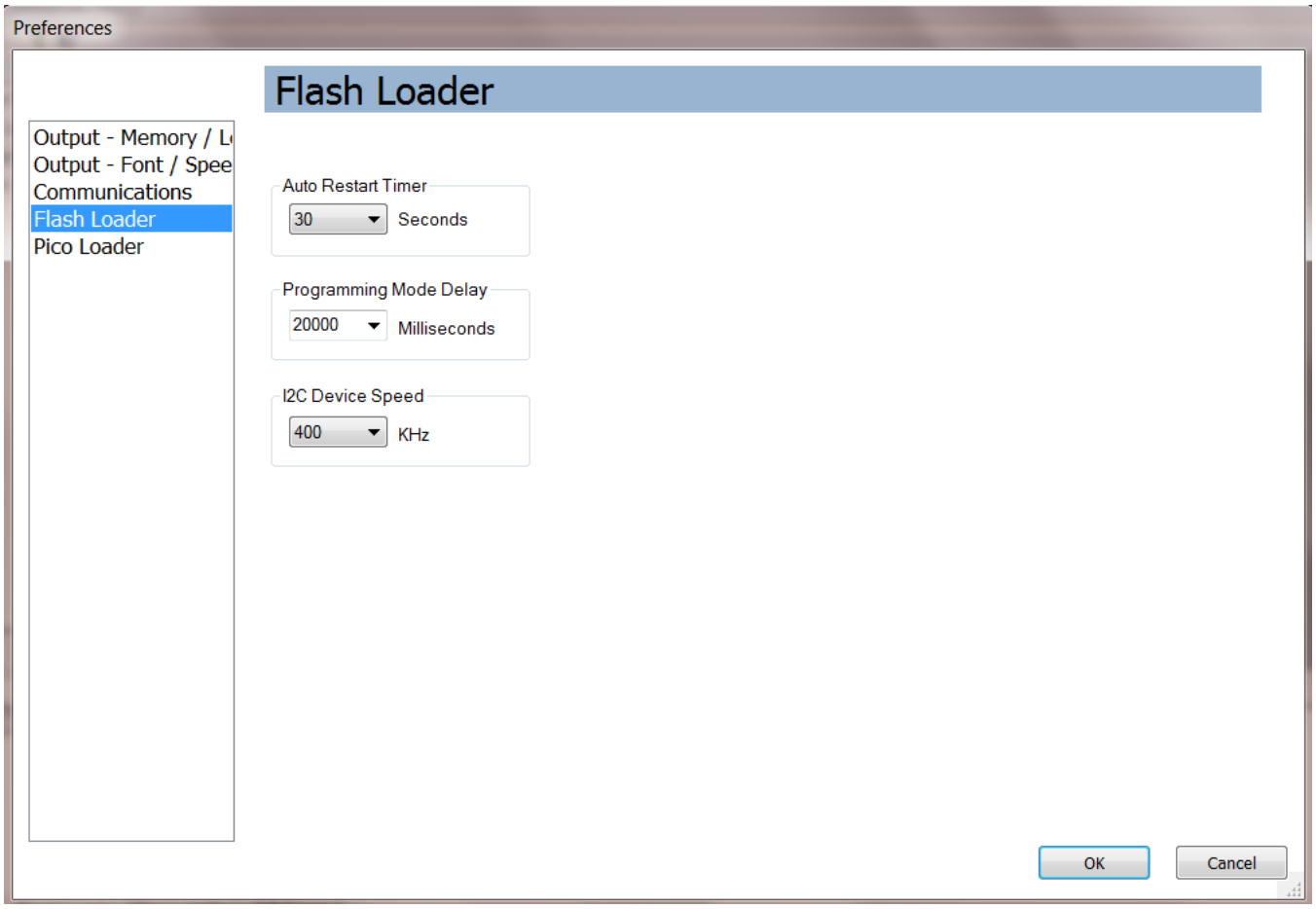


Figure 10. Flash Loader Options

2.3.2 Using DLP Composer Lite GUI Tools

2.3.2.1 Using Projector Control

The Projector Control tool is used to control a DLPC4422 controller by issuing I2C commands. Use this tool to construct batch files consisting of multiple I2C commands (and other commands) to automate simple tasks when developing and testing a new projector using the Batch Files page. Several other pages are available to issue commands and view data.

2.3.2.2 Using Flash Loader

Using Flash Loader Use this tool to send a flash image file to a DLPC4422 controller using I2C. The user should obtain the flash image file for the DLPC4422 controller and copy it onto the user's PC. After the user obtains the flash image, select Flash Loader from the project tree pane. The Flash Loader GUI appears in the tool pane.

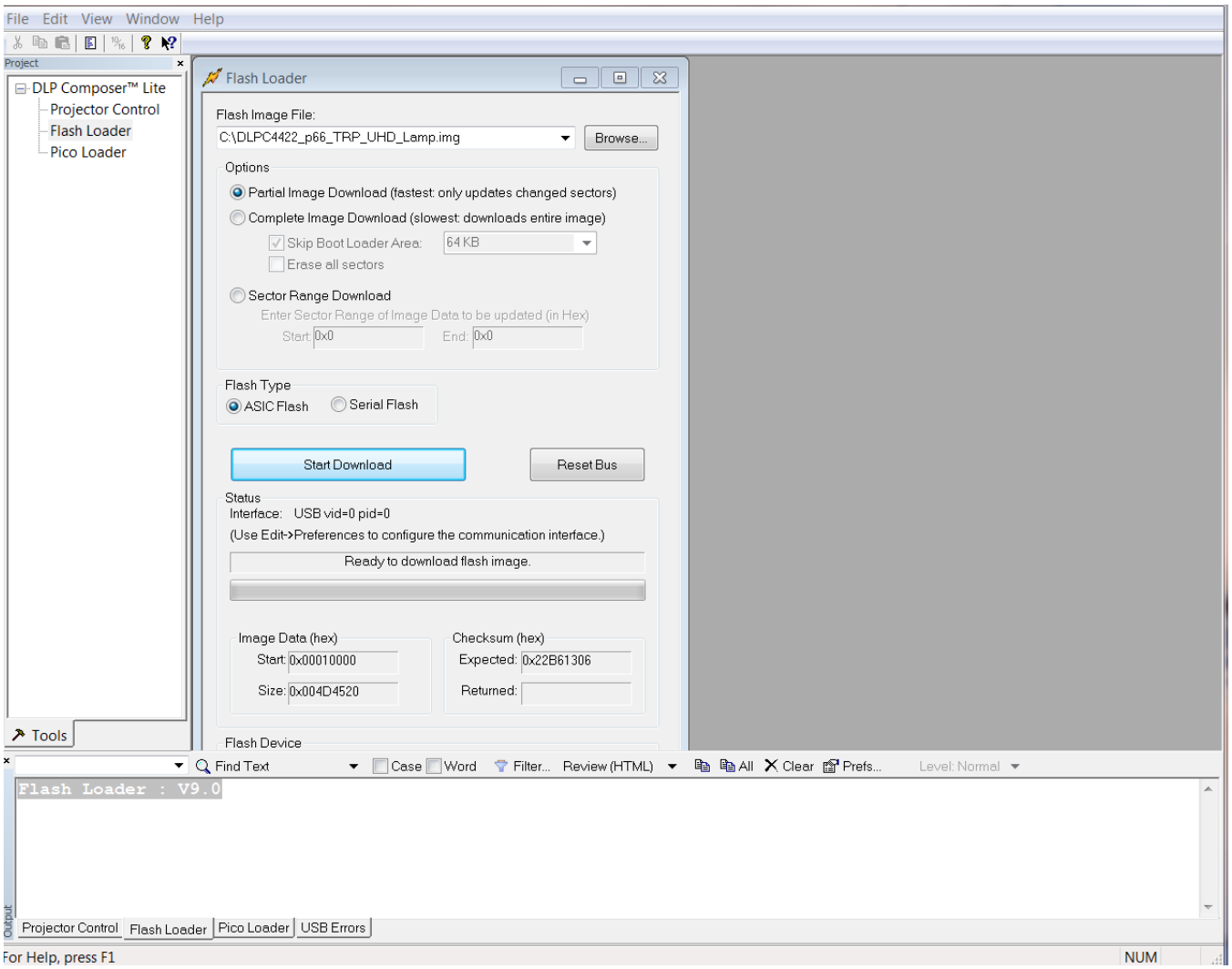


Figure 11. Flash Loader GUI

To download the flash image, follow these steps:

1. Click Browse to select the filename
2. (Optional) Select sector range parameters
3. Power the device by connecting the USB cable to the PC, and ensure connectivity
4. Click Start Download to begin the transfer
5. Do not interrupt power until after the download completes

Note: Partial Image Download can be used for consecutive downloads. It compares Flash images and only overwrites sectors that are different. Partial Image Download can only be used after doing a Complete Download to the unit at least one time. The user should skip the bootloader section unless the user wants to purposely overwrite the bootloader.

2.4 Optical Actuator

The DLP660TE DMD is capable of producing full UHD resolution by creating two individual onscreen pixels with a single DMD mirror. The image from this one mirror is shifted to two positions onscreen using an optical actuator. Designers utilizing the TIDA-01347 should contact TI's network of optical module manufacturers (OMMs) for actuator specifications and procurement information. Once the TIDA-01347 reference design PCB has been assembled with an optical engine, the optical actuator must be calibrated and adjusted to create the clearest possible image for its end use. For a detailed description of the calibration process, please contact the OMMs.

2.5 Optical Engine and Light Source

The TIDA-01347 reference design is a highly customizable 4K UHD display solution, and as such, the optical engine and illumination sources are complex systems. To make the evaluation and design process as simple as possible, TI is collaborating with third party OMMs to help provide optical engines and illumination sources that work in conjunction with this reference design.

Display systems based on DLP technology require an illumination source to create a projected image. DLP technology can be used with a wide array of light sources, including lamps, LEDs, lasers and laser phosphor. Many traditional projectors still use lamps as an illumination source; however, a significant market has developed for laser phosphor illuminated systems. Laser based illumination typically last many times longer than lamp illumination. Laser based system benefits can include a wide color gamut and instant on/off capabilities. The designer's illumination choice will depend on the end application and system requirements. It is encouraged that developers work with third party optical engine manufacturers if needed for optical system expertise.

3 Testing and Results

3.1 EMI Compliance

The TIDA-01347 reference design hardware was not optimized or tested for low EMI performance. Users of the information found in this TI design are responsible for ensuring their products meet all applicable EMI regulations.

3.2 Start-up and Shut-down Power Sequencing Measurements

The start-up and shut-down power sequencing of the four power supplies to the DLP660TE are critical to ensure DMD functionality. The micromirrors in the DMD are controlled electrostatically by electrodes held at three control voltages. These potentials are provided by the VReset (-14V), VOffset (10V), and VBias (18V) supplies to the DMD. The fourth power supply is the CMOS logic supply, DMD_P1P8V (1.8V). Since DMD_P1P8V is created directly from DMD_P3P3V (3.3V) by a linear regulator on the DMD board, TI uses the start-up of DMD_P3P3V to trigger the measurement of the start-up and shut-down power sequencing.

Power Up and Power Down timing requirements are described in detail in the DLP660TE datasheet. Key signals measured are power supplies to the DMD: DMD_P3P3V, VBIAS, VOFFSET, and VRESET. For more details on the timing requirements please refer to the DLP660TE device datasheet

The location of test points for the four DMD voltages will depend on design choices made during schematic capture and layout. The locations of the test points on the TI EVM can be seen in Figure 3 1: DMD Voltage Test Points.

The start-up and shut-down power sequence timing requirements can be found in the DLP660TE datasheet, which should be consulted to ensure full compliance.

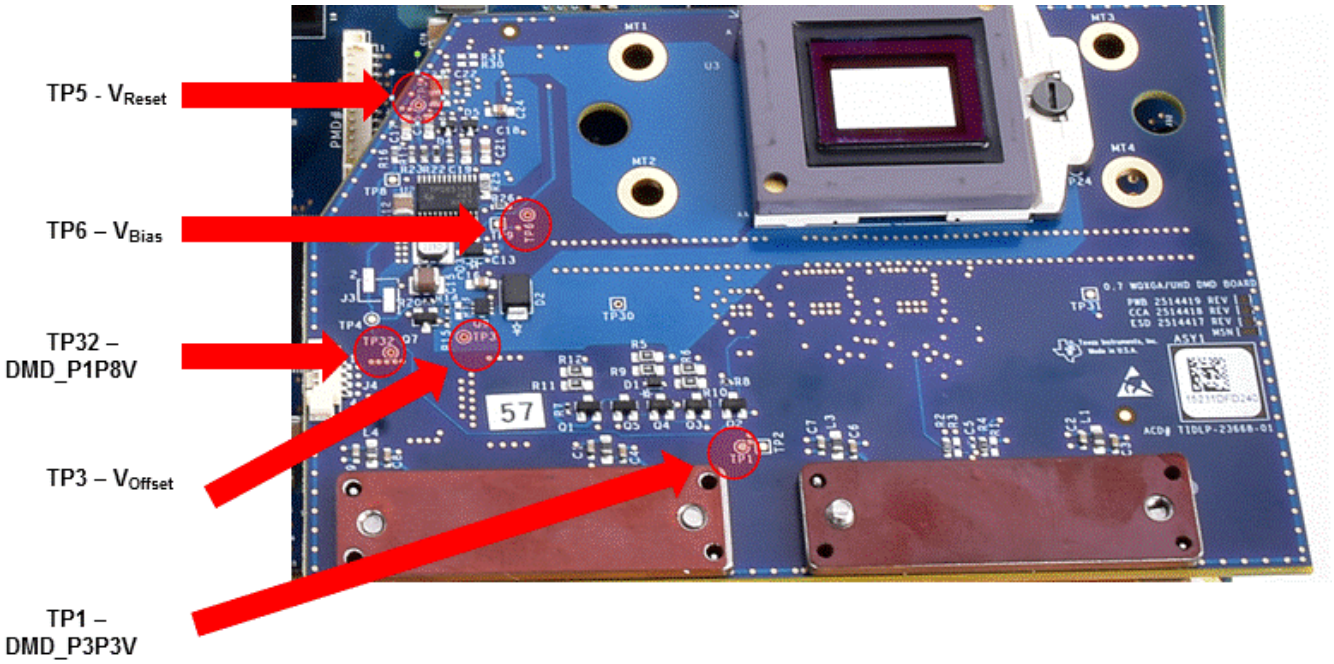


Figure 12. DMD Board Test Points

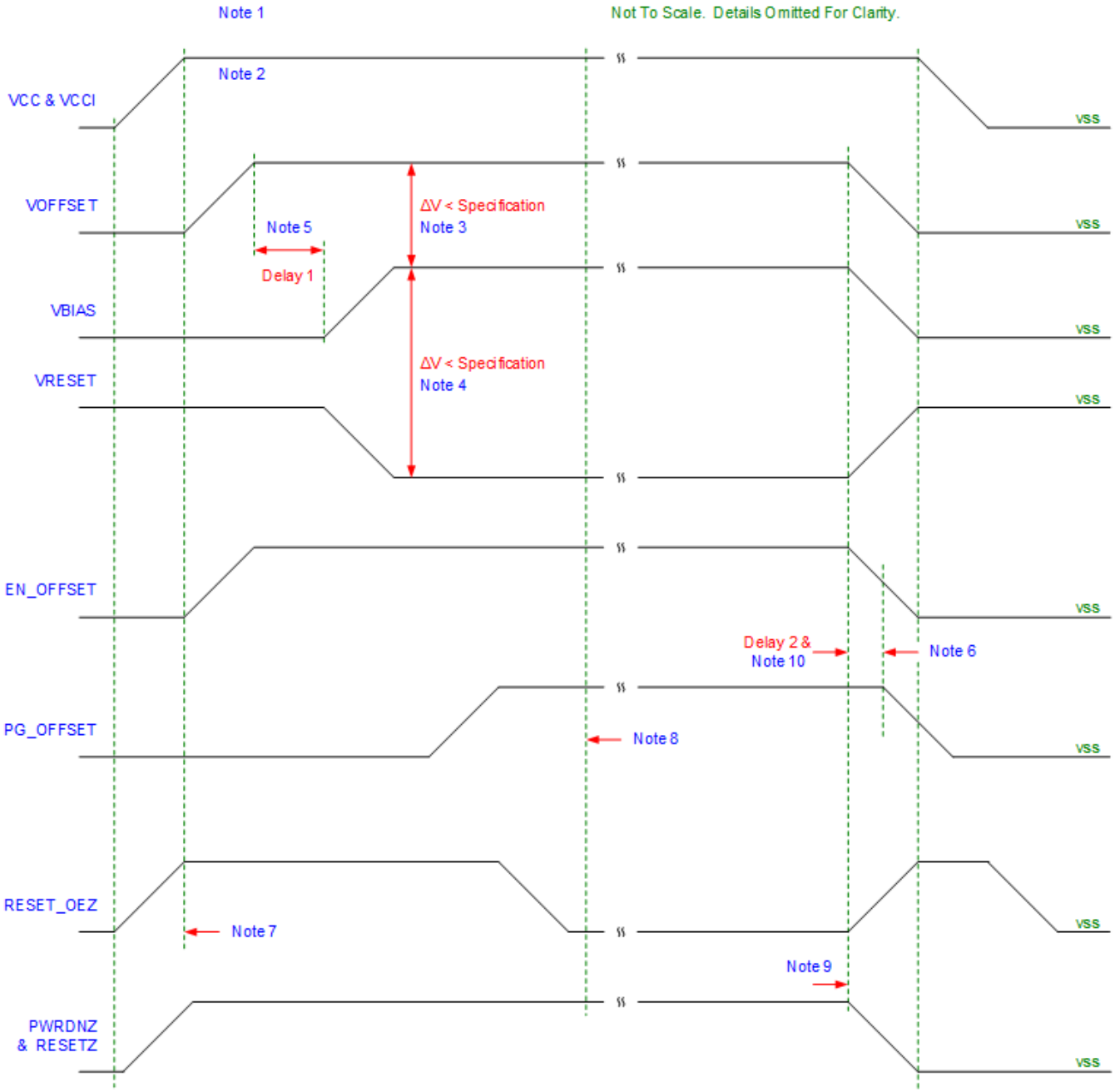


Figure 13. DMD Power Supply Timing Diagram

Notes

1. See Datasheet Recommended Operating Conditions, Pin Functions
2. To prevent excess current, the supply voltage delta |VCCI – VCC| must be less than specified limit in the datasheet
3. To prevent excess current, the supply voltage delta |VBIAS – VOFFSET| must be less than specified limit in the datasheet.
4. To prevent excess current, the supply voltage delta |VBIAS – VRESET| must be less than specified limit in the datasheet.
5. VBIAS should power up after VOFFSET has powered up, per the Delay1 specification in Figure 3 3: DMD Power Supply Requirements.

6. PG_OFFSET should turn off after EN_OFFSET has turned off, per the Delay2 specification in Figure 3 3: DMD Power Supply Requirements.
7. DLPL controller software enables the DMD power supplies to turn on after RESET_OEZ is at logic high.
8. DLP controller software initiates the global VBIAS command.
9. After the DMD micromirror park sequence is complete, the DLP controller software initiates a hardware power-down that activates PWRDNZ and disables VBIAS, VRESET, and VOFFSET.
10. Under power-loss conditions where emergency DMD micromirror park procedures are being enacted by the DLP controller hardware, EN_OFFSET may turn off after PG_OFFSET has turned off. The OEZ signal should go high prior to PG_OFFSET turning off to indicate the DMD micromirror has completed the emergency park procedures.

Table 3. DMD Power Supply Requirements

Parameter	Description	MIN	NOM	MAX	UNIT
Delay1	Delay from VOFFSET settled at recommend operating voltage to VBIAS and VRESET power up	1	2		ms
Delay2	PG_OFFSET hold time after EN_OFFSET goes low	100			ms

DMD Power Supply Power-Up Procedure

- During power-up, VCC and VCCI must always start and settle before VOFFSET plus Delay1 specified in Table 3, VBIAS, and VREST voltages are applied to the DMD.
- During power-up, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-up are flexible, provided that the transient voltage levels follow the requirements specified in the datasheet.
- During power-up, LVCMOS input pins must not be driven high until after VCC and VCCI have settled at operating voltages listed in the datasheet.

DMD Power Supply Power-Down Procedure

- During power-down, VCC and VCCI must be supplied until after VBIAS, VRESET, and VOFFSET are discharged to within the specified limit of ground.
- During power-down, it is a strict requirement that the voltage delta between VBIAS and VOFFSET must be within the specified limit shown in the datasheet
- During power-down, there is no requirement for the relative timing of VRESET with respect to VBIAS.
- Power supply slew rates during power-down are flexible, provided that the transient voltage levels follow the requirements specified in the datasheet.
- During power-down, LVCMOS input pins must be less than specified in the datasheet.

Test Results

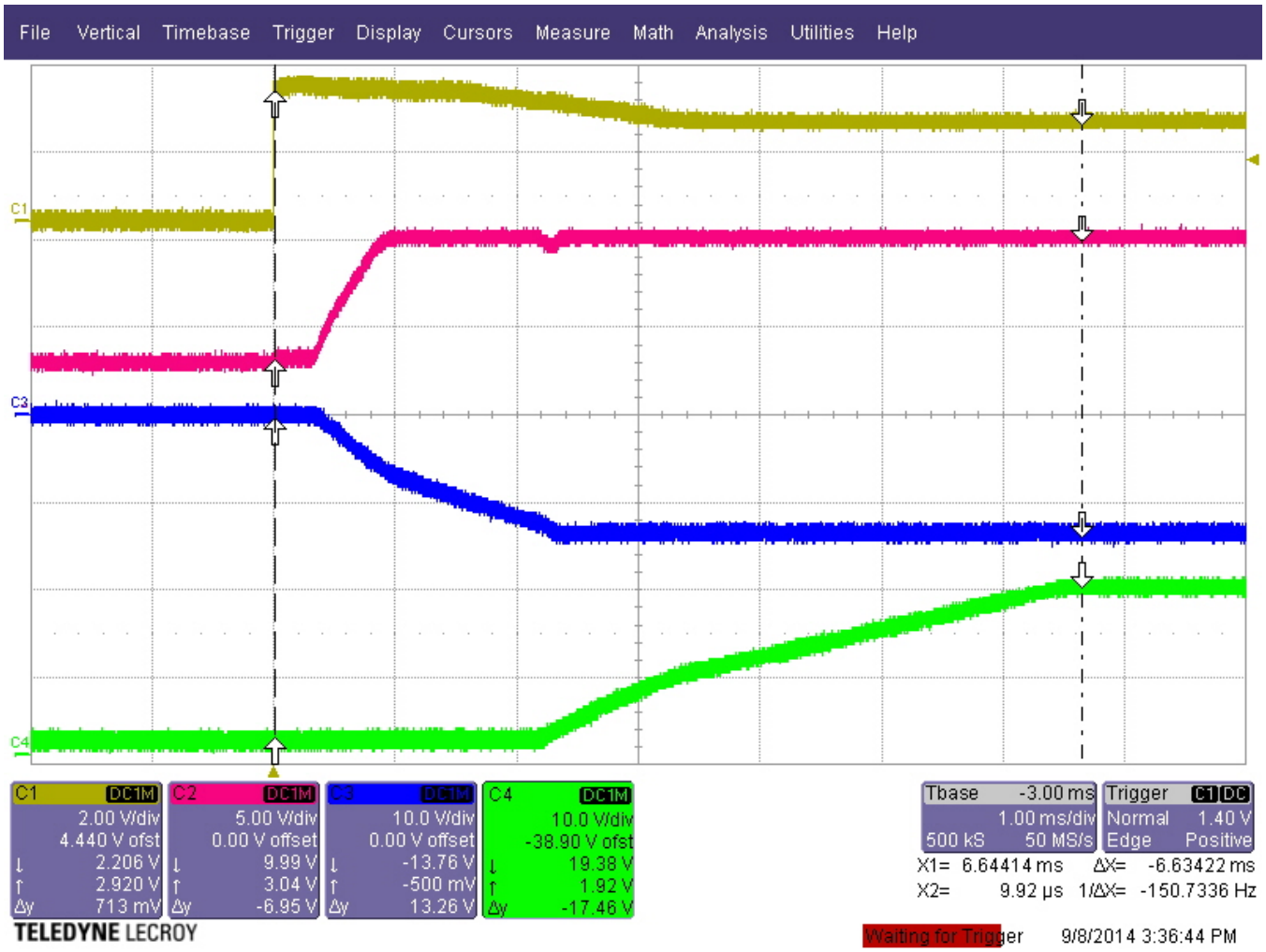


Figure 14. DMD Start-up Power Sequencing

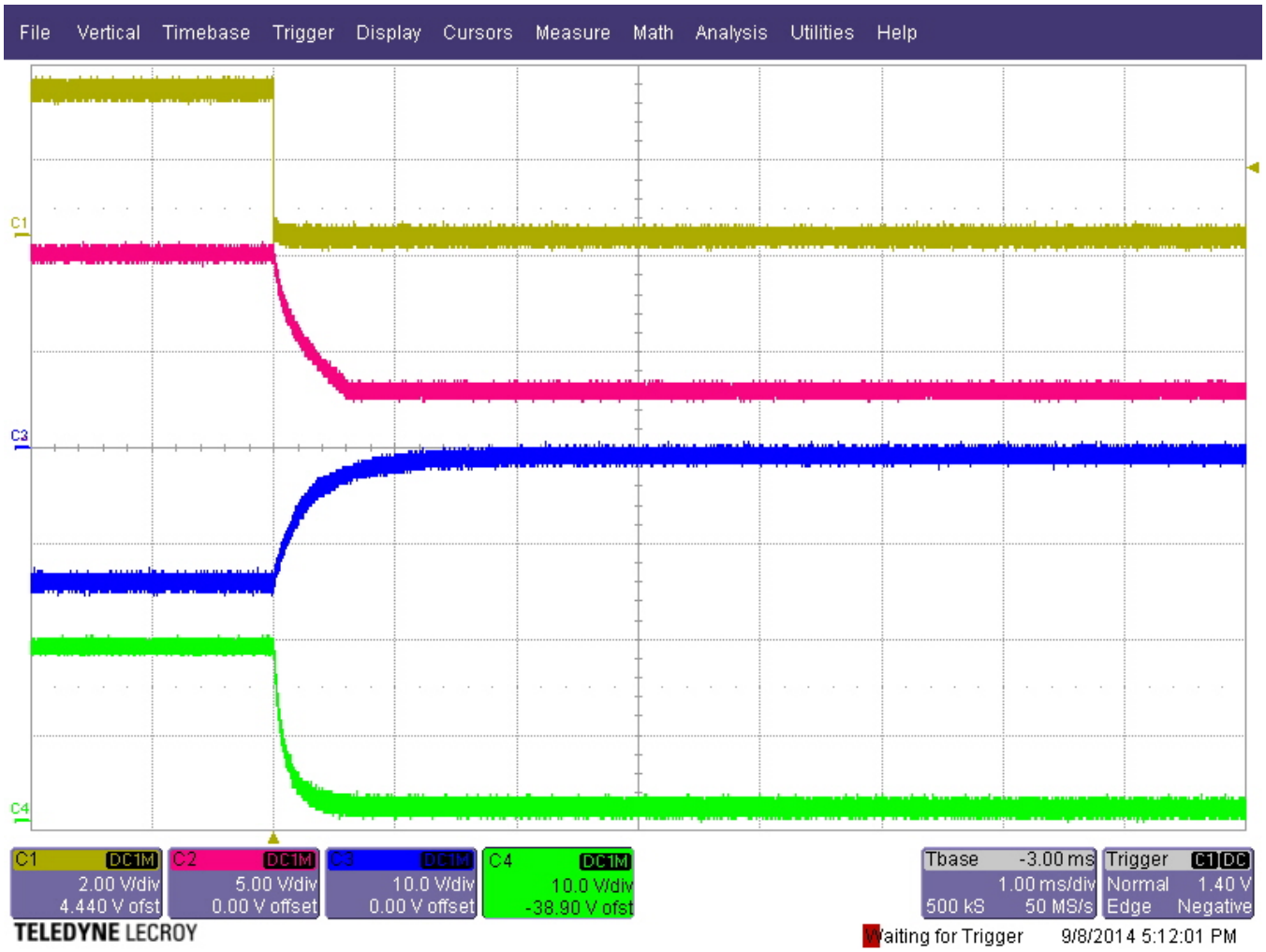


Figure 15. DMD Shut-down Power Sequencing

4 Design Files

4.1 Schematics

To download the schematics for each board, see the design files atTIDA-01347.

4.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at TIDA-01347.

4.3 PCB Layout Recommendations

4.3.1 Layout Recommendations

TI strongly recommends the PCB have solid ground planes and power planes with no splits if possible. If splits are unavoidable, no signals should be routed across the plane layer splits to avoid EMI compliance problems. Designers should avoid running signal traces on power and ground planes. Trace spacing and layer separation rules should be followed for all high speed signals, especially the video data entering and leaving the DLPC4422 controller. Refer to the Layout Guidelines section of the DLPC4422, DLP660TE, and DLPA100 datasheets for specific layout requirements for these parts. DDR3 routing guidelines should be followed wherever DDR3 signaling is used.

High speed interfaces include:

- 3 GHz High Speed Differential interface from a front end daughter card connector to the FPGA
- 533 MHz DDR3 interface from FPGA
- 400 MHz(DDR) LVDS interface from DLPC4422 ASICs to DLP660TE DMD
- Up to 170 MHz LVTTL interface from the FPGA to the DLPC4422 ASICs and FLASH
- 143 MHz Arm trace port output (8 bit data bus shared with DLPC4422 test points)
- USB Interface

The PCB will require controlled impedance design for signal layers. The target impedance for the PCB should be 50 Ohms with the LVDS traces being 100 Ohm differential.

The reference design layout files provided along with this TI Design are only intended as evaluation modules. The reference design hardware was not optimized or tested for low EMI performance. Users of the information found in this TI design are responsible for ensuring their products meet all applicable EMI regulations.

4.3.2 Layout Prints

To download the layout prints for each board, see the design files at ti.com/tool/TIDA-01347.

4.4 Allegro Cadence Project

To download the Allegro Cadence project files for each board, see the design files at ti.com/tool/TIDA-01347.

4.5 Gerber and CAD files

To download the Gerber and CAD files for each board, see the design files at ti.com/tool/TIDA-01347.

4.6 Assembly Drawings

To download the assembly drawings for each board, see the design files at ti.com/tool/TIDA-01347.

5 Software Files

To download the software files for this reference design, please see the link at ti.com/tool/TIDA-01347.

6 Related Documentation

1. Texas Instruments, *TI DLP ® Pico ™ System Design: Brightness Requirements and Tradeoffs* , Application Report (DLPA068)
2. Texas Instruments, *Getting Started with TI DLP ® Pico ™ Technology* , Application Report (DLPA069)
3. Texas Instruments, *TI DLP Technology for Laser TV Displays* White Paper (DLPC105)
4. Texas Instruments, *TI DLP Technology for Digital Signage*, White Paper

6.1 Trademarks

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