

Analog Engineer's Circuit

True Differential, 4 × 2 MUX, Analog Front End, Simultaneous-Sampling ADC Circuit



Luis Chioye

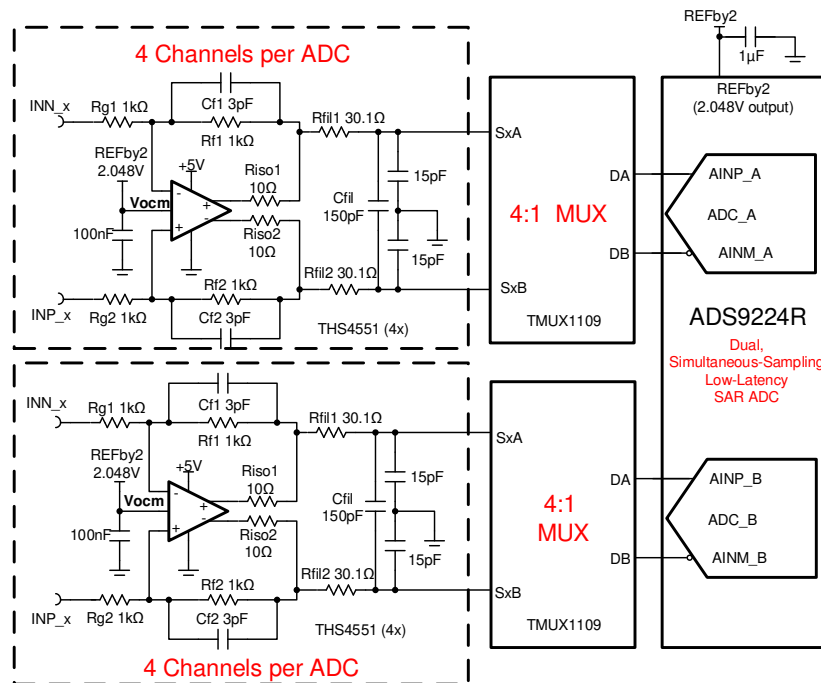
Input (THS4551 Inputs)	ADC Input (THS4551 Output)	Digital Output ADS7042
VinP = +0.23V, VinN = +3.866V, VinMin(Dif) = -3.636V	VoutP = +0.23V, VoutN = 3.866V, Vout(Dif) = -3.636V	8E60 _H -29088 ₁₀
VinP = +3.866V, VinN = 0.23V, VinMax(Dif) = +3.636V	VoutP = 3.866V, VoutN = +0.23V, Vout(Dif) = +3.636V	71A0 _H +29088 ₁₀

Power Supplies

Vcc	Vee	Vref	Vocm
5	0V	4.096V	2.048V

Design Description

This dual simultaneous-sampling SAR ADC and 4 × 2 channel multiplexed analog front end data acquisition solution can measure differential voltage signals in the range of ±3.866V supporting ADC sampling rates up to 3-MSPS (or effective sampling rate of 750-kSPS per channel) with 16-B resolution. The circuit consists of a dual simultaneous sampling SAR ADC, with each SAR ADC connected to two 4:1 (2x) multiplexers, providing 4 differential input channels per ADC. Eight *Fully Differential Amplifiers* (FDAs) drive the multiplexed SAR ADC inputs. This circuit is applicable in the accurate measurement of dual simultaneous signals in applications such as [Optical Modules](#) and [Analog Input Modules](#). It also can be used in motor drive applications such as [Servo Drive Control Module](#), [Servo Drive Position Feedback](#), and [Servo Drive Position Sensor](#).



Specifications

Specification	Goal	Calculated	Simulated
Dual ADC Sampling Speed	3Msps	3Msps	3Msps
Sampling Rate per Channel (dual, simultaneous)	750kSPS (3MSPS / 4)	750kSPS (3-MSPS / 4)	750-kSPS (3MSPS / 4)
Transient ADC Input Settling	<< 1 LSB << 125 μ V	NA	20 μ V
Noise (at ADC Input)	50 μ V _{rms}	55.9 μ V _{rms}	51.1 μ V _{rms}

Design Notes

- The ADS9224R was selected because of the dual simultaneous sampling and high throughput (3-MSPS) requirements.
- The TMUX1109 4:1 (2x) multiplexer was selected to support 4-channel differential inputs for each ADC.
- Find ADC full-scale range, resolution and common-mode range specifications. This is covered in the component selection.
- Determine the linear range of the FDA (THS4551) based on common-mode and output swing specification. This is covered in the component selection section.
- Select COG capacitors for all filter capacitors at the ADC input to minimize distortion.
- Select the FDA gain resistors RF1,2 , RG1,2. Use 0.1% 20ppm/°C film resistors or better for good accuracy, low gain drift and to minimize distortion.
- [Introduction to SAR ADC Front-End Component Selection](#) covers the methods for selecting the charge bucket circuit Rfil1, Rfil1 and Cfil. These component values are dependent on the amplifier bandwidth, data converter sampling rate, and data converter design. The values shown here will give good settling and AC performance for the amplifier and data converter in this example. If the design is modified, a different RC filter must be selected.
- The THS4551 is commonly used in high-speed precision fully differential SAR applications as it has sufficient bandwidth to settle to charge kickback transients from the ADC input sampling, and multiplexer charge injection and provides the common-mode level shifting to the voltage range of the SAR ADC.

Component Selection

1. Find ADC full-scale input range. In this circuit, ADS9224 internal $V_{REF} = 2.5V$

$$ADC_{Full-Scale\ Range} = (\pm 1.6384V/V) \cdot V_{REF} = \pm 4.096V \text{ from ADS9224R datasheet}$$

2. Find required ADC common-mode voltage 2.

$$V_{CM} = \frac{+ADC_{Full-Scale\ Range}}{2} = +2.048V \text{ from ADS9224R datasheet}$$

Use REFby2 Output pin of ADS9224R to connect to FDA (THS4551) $V_{COM} = 2.048V$

3. Find FDA absolute output voltage range for linear operation:

$$0.23V < V_{out} < 4.77V \text{ from THS4551 output low/high specification for linear operation}$$

4. Find FDA differential output voltage range for linear operation. The general output voltage equations for this circuit:

$$V_{outMin} = \frac{V_{outDifMin}}{2} + V_{cm}$$

$$V_{outMax} = \frac{V_{outDifMax}}{2} + V_{cm}$$

Rearrange the equations and solve for $V_{outDifMin}$ and $V_{outDifMax}$. Find maximum differential output voltage range based on worst case:

$$V_{outDifMax} = 2 \cdot V_{outMax} - 2 \cdot V_{cm} = 2 \cdot (4.096V) - 2 \cdot (2.048V) = 4.096V$$

$$V_{outDifMin} = 2 \cdot V_{outMin} - 2 \cdot V_{cm} = 2 \cdot (0.23V) - 2 \cdot (2.048V) = -3.636V$$

Based on combined worst case, choose $V_{outDifMin} = -3.636V$ and $V_{outDifMax} = +3.636V$

5. Set FDA gain to 1 V/V

$$Gain_{FDA} = \frac{R_f}{R_g} = \frac{1.00k\Omega}{1.00k\Omega} = 1V/V$$

6. Select the minimum charge kickback capacitor filter to optimize circuit for fastest settling.

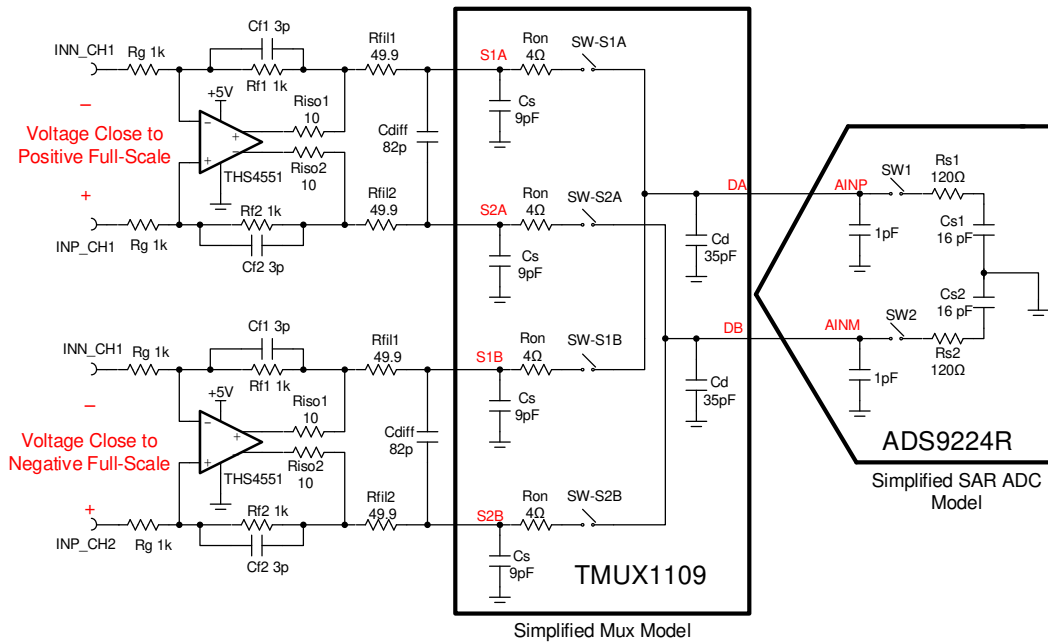
$$C_{sh} = 16pF \text{ internal sample-and-hold capacitor from ADS9224R datasheet}$$

Select a capacitor $10\times$ larger than $C_{sh} = 150pF$

7. Optimize RC charge kickback filter resistors R_{fil1}, R_{fil2} and feedback capacitors C_{f1}, C_{f2} for both settling and stability using TINA simulations. This is covered in the transient settling optimization and stability simulation sections.

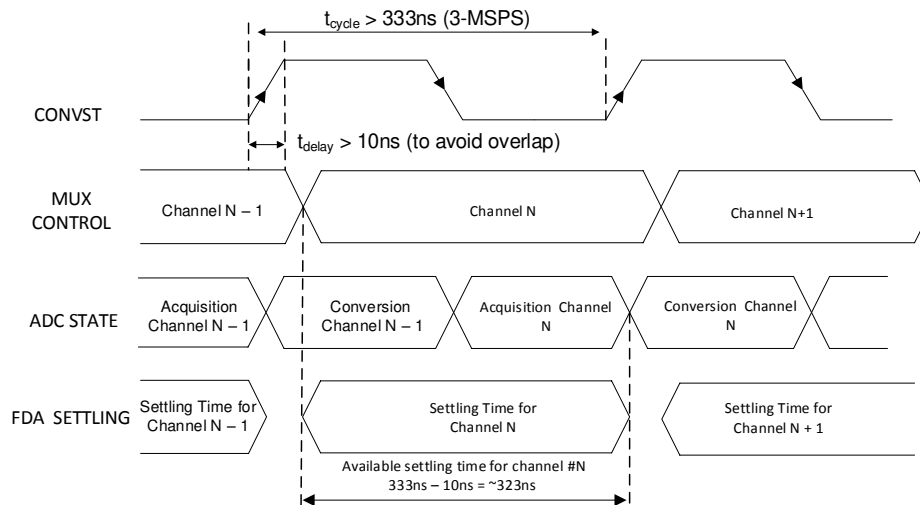
Transient Settling Optimization

TINA simulation is used to optimize the RC kickback filter for stability and transient settling. The transient simulation incorporates two adjacent channels of the multiplexer (TMUX1109). To simulate worst case transient settling during the multiplexer scanning sequence, the two adjacent channels are set to a voltage close to positive full-scale and negative full-scale respectively. The multiplexer drain capacitance and series resistance are modeled in the multiplexer simulation circuit. The sample and hold capacitor of the SAR ADC must settle within the 16-bit resolution of the SAR ADC during the acquisition period. A simplified schematic of the simulation circuit follows:



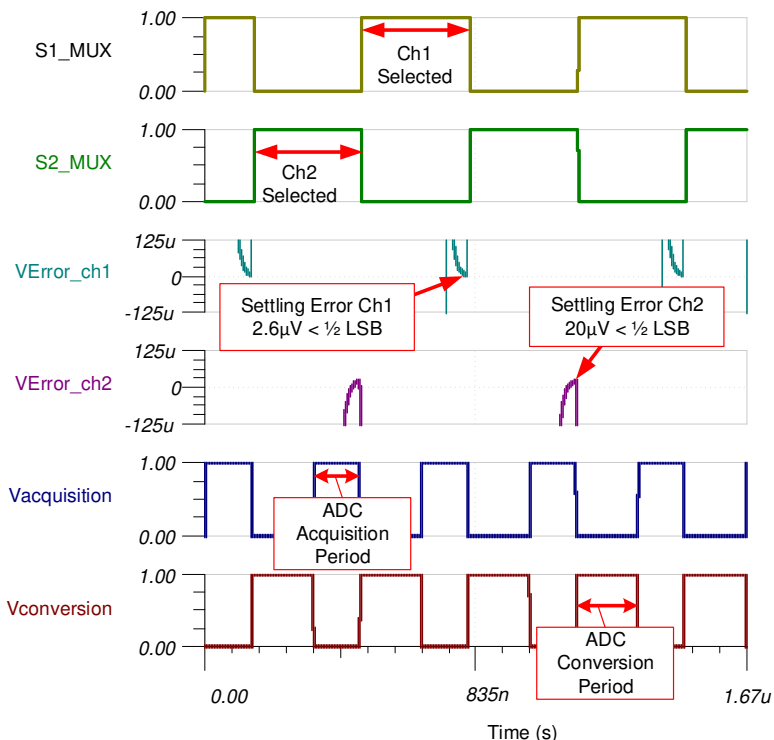
Multiplexer and ADC Control Timing

The following plot shows the ADC conversion control (CONVST) and multiplexer channel control timing. The ADS9224R supports a maximum sampling rate of 3MSPS or a minimum cycle time of 333ns. To avoid switching channels prior to the rising edge of the CONVST signal, a small delay is implemented in the MUX channel control timing after the CONVST rising edge. Refer to TI design [16-Bit, 400-kSPS, Four-Channel MUX Data Acquisition System for High-Voltage Inputs Reference Design](#) for detailed theory in the subject.



Transient Settling Results

The following TINA transient simulation shows settling of the FDA, multiplexer, and SAR ADC sample and hold after a full-scale step change between adjacent MUX channels. This type of simulation shows that the sample and hold kickback circuit, and AFE amplifier circuit is properly selected. See [Introduction to SAR ADC Front-end Component Selection](#) for an explanation of how to select the RC filter for best settling and AC performance.

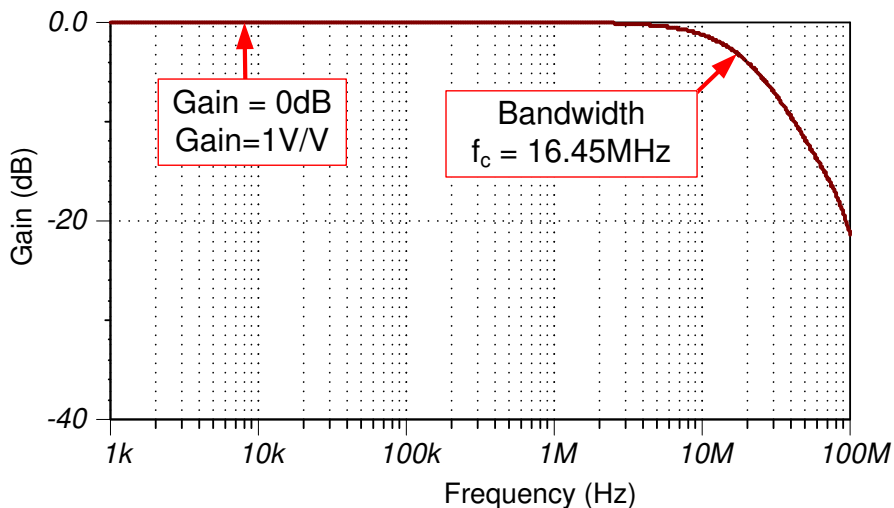


AC Transfer Characteristics

The circuit has a gain of 0-dB (1-V/V) and a simulated frequency bandwidth of 16.45-MHz. Notice that the calculated and simulated bandwidth compare well (calculated = 17.62MHz, simulated = 16.45MHz). See [Op Amp Bandwidth](#) for a general overview of bandwidth calculations and simulations.

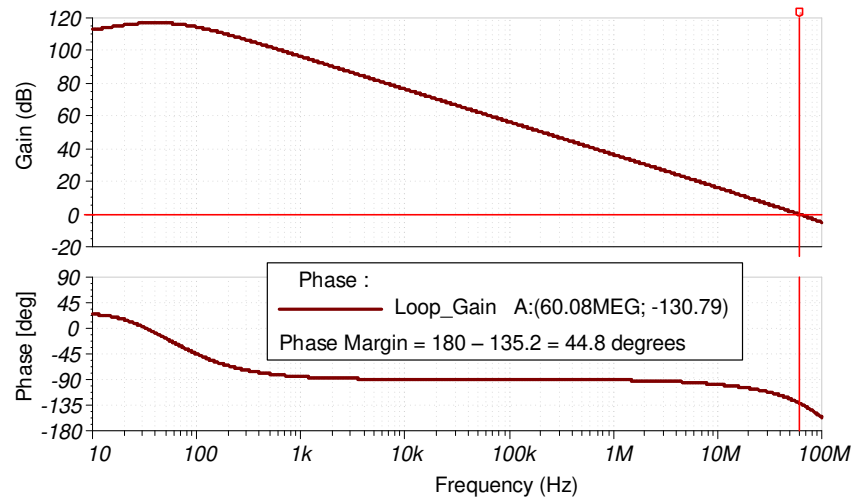
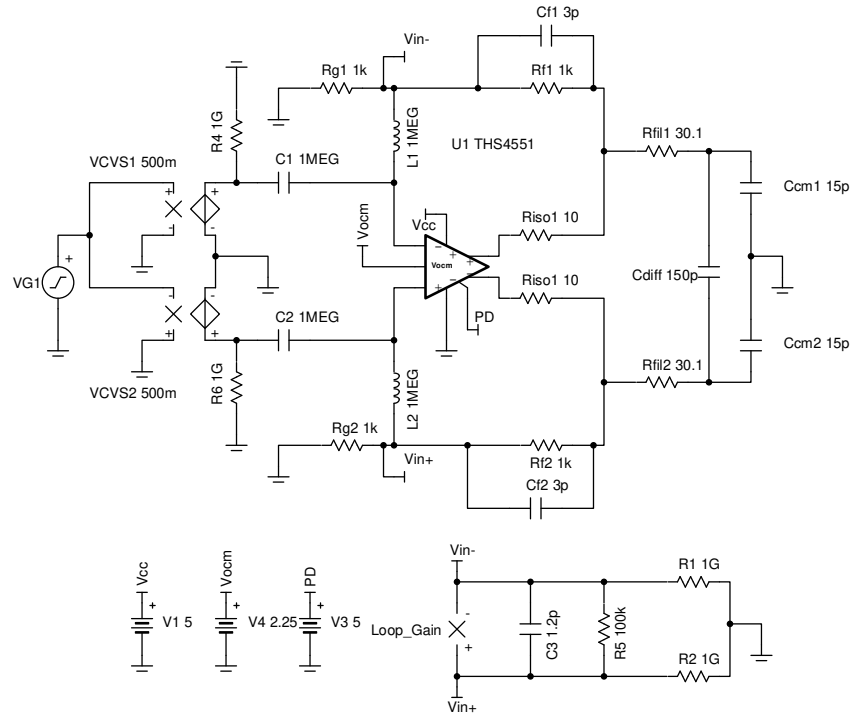
The system bandwidth is set by the output filter:

$$f_c = \frac{1}{2\pi (R_{fil1} + R_{fil2})C_{diff}} = \frac{1}{2\pi (30.1\Omega + 30.1\Omega)(150pF)} = 17.62MHz$$



Stability Simulation Graph

The following circuit is used in TINA to measure loop gain and verify phase margin using AC analysis in TINA. Resistors RISO = 10Ω are used inside the feedback loop to increase phase margin. The circuit has good stability (approximately 45 degrees of phase margin). See [Op Amp Stability](#) for detailed theory on this subject.



Noise Simulation

Simplified noise calculation estimate:

The dominant pole in this data acquisition circuit is in the RC kickback filter:

$$f_c = \frac{1}{2\pi(R_{fil1} + R_{fil2})C_{diff}} = \frac{1}{2\pi(30.1\Omega + 30.1\Omega)(150pF)} = 17.62MHz$$

Noise of THS4551 FDA referred to ADC input

$$\text{Noise Gain: } NG = 1 + R_f / R_g = 1 + \frac{1k\Omega}{1k\Omega} = 2V/V$$

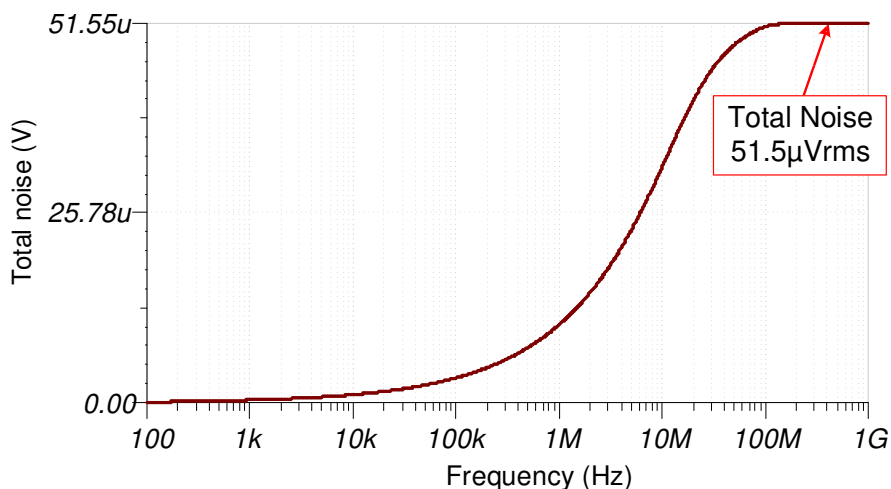
$$e_{noFDA} = \sqrt{(e_{nFDA} \cdot NG)^2 + 2(j_{nFDA} \cdot R_f)^2 + 2(4kTR_f \cdot NG)}$$

$$e_{noFDA} = \sqrt{(3.4nV / \sqrt{Hz} \cdot 2.00V / V)^2 + 2(0.5pA / \sqrt{Hz} \cdot 1k\Omega)^2 + 2(16.56 \cdot 10^{-18} \cdot 2.00V / V)}$$

$$e_{noFDA} = 10.629nV / \sqrt{Hz}$$

$$E_{nFDA} = e_{noFDA} \cdot \sqrt{K_n \cdot f_c} = (10.629nV / \sqrt{Hz}) \sqrt{1.57 \cdot 17.62MHz} = 55.90\mu V_{rms}$$

The following figure shows the TINA simulated total noise for the FDA circuit. See [Calculating the Total Noise for ADC systems](#) for detailed theory on this subject. Note that the calculated and simulated noise compare well (calculated = 55.9 μ V_{rms}, simulated = 51.5 μ V_{rms}).



Design Featured Devices

Device	Key Features	Link	Other Possible Devices
ADS9224R	16-bit resolution, SPI, 3-MSPS sample rate, fully-differential input, integrated 2.5-V reference, dual, simultaneous sampling, low-latency	16-bit, 3MSPS, dual-channel, simultaneous-sampling SAR ADC with internal reference and enhanced SPI	Analog-to-digital converters (ADCs)
THS4551	150MHz, 3.3nV + \sqrt{Hz} input voltage noise, fully-differential amplifier	Low Noise, Precision, 150MHz, Fully Differential Amplifier	Fully differential amplifiers

Link to Key Files

Texas Instruments, [SBAC219 TINA files](#), software support

Trademarks

All trademarks are the property of their respective owners.

Revision History

Changes from Revision A (November 2018) to Revision B (August 2024) **Page**

- Updated the format for tables, figures, and cross-references throughout the document..... [1](#)
-

Changes from Revision * (October 2019) to Revision A (November 2019) **Page**

- Downscale title. Updated the schematic in the *Transient Settling Optimization* section..... [1](#)
-

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated