Application Note

TLV320ADCx140/PCMx140-Q1 Sampling Rates and Programmable Processing Blocks Supported

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ABSTRACT

This application note describes the available processing blocks in the decimation filter chain of the TLV320ADCx140/PCMx140-Q1 family of devices. The document also explains which configurations of the processing blocks are supported as a function of the sample rate and number of channels.

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Trademarks

1 Introduction

The TLV320ADCx140/PCMx140-Q1 is a family of quad-channel, audio analog-to-digital converters that includes a highly flexible signal chain with programmable digital processing blocks, making it suitable for a wide variety of applications. The data sheet provides the overview for all of the device features. Figure 1-1 shows the signal processing chain. The device can support four analog microphone channels, 8 digital PDM microphone channels, or a combination of analog and digital microphones channels. The decimation filters, digital summer and mixer block, and bi-quad filters shown in Figure 1-1 are highly configurable, so it can suit different application scenarios. In addition, the device also supports an Automatic Gain Controller (AGC) block and Dynamic Range Enhancer (DRE) block on the analog microphone channels. These digital features all share the same fixed processing resources. Therefore, the number of channels enabled, the nature of each channel (analog or digital), and the sample-rate determine the configuration possibilities for the processing blocks and filters.

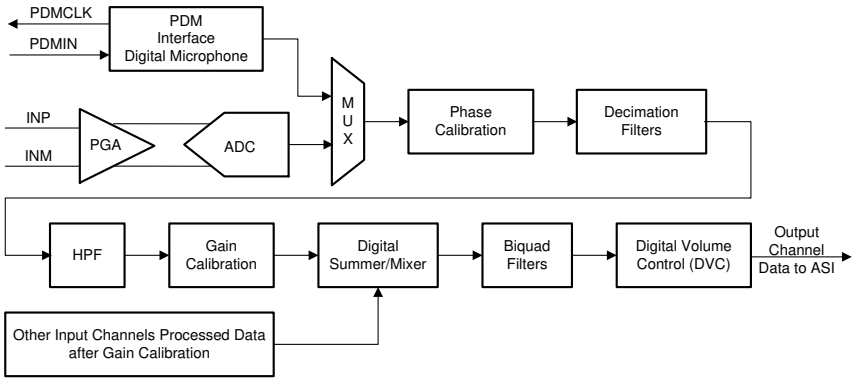

Figure 1-1. TLV320ADCx140/PCMx140-Q1 Channel Signal Chain Processing Flow Chart

The TLV320ADCx140/PCMx140-Q1 device family supports two sets of sample rates. One set of sample rates cover the nine submultiples and multiples of 48 kHz, from 8 kHz to 768 kHz. The other set of sample rates cover the sample rates from 7.35 kHz to 705.6 kHz, which are submultiples and multiples of 44.1 kHz. This application note only refers to the set of 48 kHz sample rates, but they are applicable to the corresponding sample rate from the set of 44.1 kHz sample rates. For example, features supported for the 8 kHz sample rate are also supported for 7.35 kHz.

The next section reviews the processing blocks, configuration options and input channels they are supported on, and the supported sample rates. The subsequent section reviews the channel combinations that are supported for different sample rates, and the processing blocks that are supported for the given channel combination.

2 Processing Blocks of TLV320ADCx140/PCMx140-Q1

The following sections describe the device configurations required to use:

- Decimation filters
- AGC or DRE
- Programmable biquads
- Summers
- Digital mixers

2.1 Decimation Filter Response

The decimation filter processes the oversampled data from either the multi-bit delta-sigma modulator of the analog channels or the oversampled PDM stream from the digital microphones, and generates the output PCM samples at the FSYNC rate. The decimation filter option is selected by configuring the DECI_FILT, P0_R107_D[5:4] register bits. Table 2-1 shows the configuration register setting for the decimation filter mode selection for the record channel. It can be set to linear phase, low latency, or ultra-low latency.

Table 2-1. Decimation Filter Mode Selection for the Record Channel

P0_R107_D[5:4] : DECI_FILT[1:0]	DECIMATION FILTER MODE SELECTION
00 (default)	Linear phase decimation filters
01	Low-latency approximately linear phase decimation filters
10	Ultra-low latency decimation filters
11	Reserved

2.1.1 Supported Sample Rates

The response of the default decimation filter is linear phase. It is supported for all sample rates from 8 kHz to 768 kHz. The low latency and ultra-low latency responses are supported for a subset of the sample rates as shown in Table 2-2. Unsupported filters are marked as 'NA'. For supported filters, Table 2-2 lists the maximum channel count. Note that to support the channel count shown in Table 2-2, certain processing blocks may have to be disabled, as shown in Section 3.

Table 2-2. Maximum Channel Count for Decimation Filters

SAMPLE RATE (kHz)	LINEAR PHASE	LOW LATENCY	ULTRA-LOW LATENCY
8	2	2	NA
16	2	2	2
24	2	2	2
32	2	2	2
48	2	2	2
96	2	2	2
192	2	2	2
384	2	NA	2
768	1	NA	NA

2.2 AGC or DRE

Analog channels include two additional processing blocks:

- Automatic Gain Control (AGC) is an algorithm that dynamically controls the gain of the ADC channel to maintain a nominally constant output level. AGC is available on all TLV320ADCx140/PCMx140-Q1 device variants.
- Dynamic Range Enhancer (DRE) is an algorithm that dynamically adjusts the PGA gain of the ADC channel to enhance the dynamic range. DRE is available on the TLV320ADC5140 and TLV320AD6140 devices.

Only one of these blocks can be enabled at a time. These blocks are enabled by setting the DRE_AGC_SEL bit in DSP_CFG1 (P0_R108_D[3]) to 1. Table 2-3 shows the AGC_SEL definition.

Table 2-3. AGC Selection Register Field Description

P0_R106_D[3] : AGC_SEL[1:0]	AGC or DRE SELECTION
0 (default)	AGC is not selected (DRE is selected for TLV320ADC5140 and TLV320ADC6140).
1	AGC is selected (DRE is not selected).

2.2.1 Supported Sample Rates

AGC or DRE is supported from 16 kHz to 192 kHz sample rates. AGC or DRE is not supported for 8 kHz, 384 kHz, and 768 kHz sample rates. Do not change the value of the DRE_AGC_SEL bit for unsupported sample rates.

2.2.2 Channel Assignment

AGC or DRE is only available for analog channels. Analog channels are assigned to input channels 1 and 2. Table 2-4 shows the maximum number of analog channels supported by the device when AGC or DRE is enabled.

Table 2-4. Number of Analog Channels Supported with AGC/DRE Enabled

SAMPLE RATE (kHz)	NUMBER OF CHANNELS SUPPORTED WITH AGC/DRE ENABLED
16	2
24	2
32	2
48	2
96	2
192	1

2.3 Channel Summer, Digital Mixer, and Bi-quads

The device supports one four-channel mixer, one channel summation mode, and up to three bi-quads per channel. These features are supported for all sample rates from 8 kHz to 192 kHz. See Table 2-5 for configuration details of the summer and mixer modes. The programmable mixer feature is available only if CH_SUM[2:0] is set to 2'b00. The mixer function is only supported for input channel 1 to channel 4.

The number of bi-quad filters per channel can be set using the P0_R108:BQ_CFG bits, as shown in Table 2-6. For additional information on bi-quad filter configuration, refer to the *TLV320ADCx140/PCMx140-Q1 Programmable Bi-quad Filter Configuration and Applications*, application note.

Table 2-5. Channel Summing Mode and Digital Mixer Programmable Settings

P0_R107_D[3:2] : CH_SUM[1:0]	CHANNEL SUMMING MODE FOR INPUT CHANNELS
00 (Default)	Channel summing mode is disabled (Digital Mixer is enabled).
01	Output channel 1 = (input channel 1 + input channel 2) / 2
	Output channel 2 = (input channel 1 + input channel 2) / 2
10	Reserved
11	Reserved

Table 2-6. Bi-quad Configuration Settings

P0_R108_D[6:5] : BQ_CFG[1:0]	BI-QUAD CONFIGURATION
00 (Default)	No bi-quads per channel; bi-quads are all disabled.
01	1 bi-quad per channel
10	2 bi-quads per channel
11	3 bi-quads per channel

Table 2-7 lists the processing blocks that are available for a given input channel. These assignments are fixed and cannot be changed. The two-channel summer mode is available for the first two channels, and cannot be assigned to channels 3 and 4, even if some of the other channels are disabled. Whereas, the four-channel mixer

and three bi-quads per channel are available for all the four channels. Input channels 1 to 2 support the most features, while channels 3 and 4 support the least number of features.

Table 2-7. Processing Block Assignments Across Input Channels

POST-PROCESSING LOCK	1	2	3	4
Two-channel Summer	√	√	x	x
Four-channel Mixer	√	√	√	√
Bi-quads Available	3	3	3	3

3 Processing Blocks Supported for Different Sample Rates

This section describes the specific processing blocks available for different sample rates.

3.1 8 kHz Sample Rate

Only the linear phase (default) decimation filter response is supported for the 8 kHz sample rate. Supported processing blocks include bi-quads, digital mixer, and channel summer. The AGC or DRE block is not supported for the 8 kHz sample rate. Bi-quads, channel summers, and digital mixer blocks are supported on the respective input channels (Table 2-7).

Figure 3-1 shows the analog-channel and digital-channel combinations that can be supported for an 8 kHz sample rate. For example, it can be seen that with two analog channels (third column), up to two digital channels can be supported, whereas with one analog channel also, only two digital channels can be supported. The cell entry indicates the number of bi-quads available for that channel combination. For example, with the combination of two analog and two digital microphones, three bi-quads per channel can be supported.

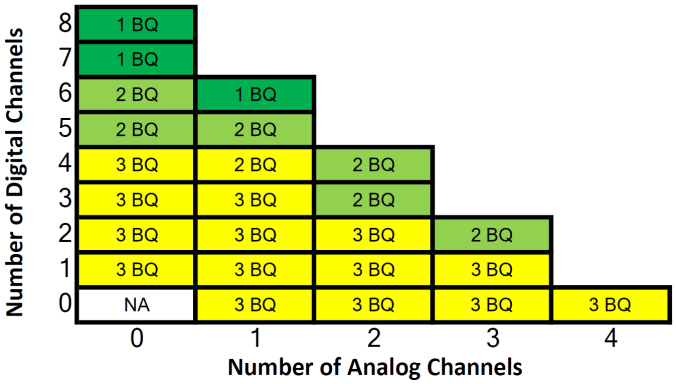

Figure 3-1. Supported Channel Combinations for 8 kHz to 48 kHz Sample Rates

3.2 16 kHz-48 kHz Sample Rate

All processing blocks and digital filter options are supported for the 16 kHz to 48 kHz sample rates.

The decimation filter can be configured to linear phase, low latency, or ultra-low latency. AGC or DRE is supported for all analog channels. Bi-quads, channel summers, and digital mixer blocks are supported on their respective input channels (Table 2-7). Figure 3-1 shows the channel combinations supported for an 8 kHz operation. These remain the same. For a supported channel combination, the cell entry in Figure 3-1 indicates the number of bi-quads available for that channel combination.

3.3 96 kHz Sample Rate

All three decimation filter options are supported for 96 kHz operation. 96 kHz mode supports AGC and DRE, but not for all channel combinations. Figure 3-2 shows the channel combinations supported when AGC or DRE is enabled. Figure 3-3 shows the channel combinations support when AGC or DRE is disabled.

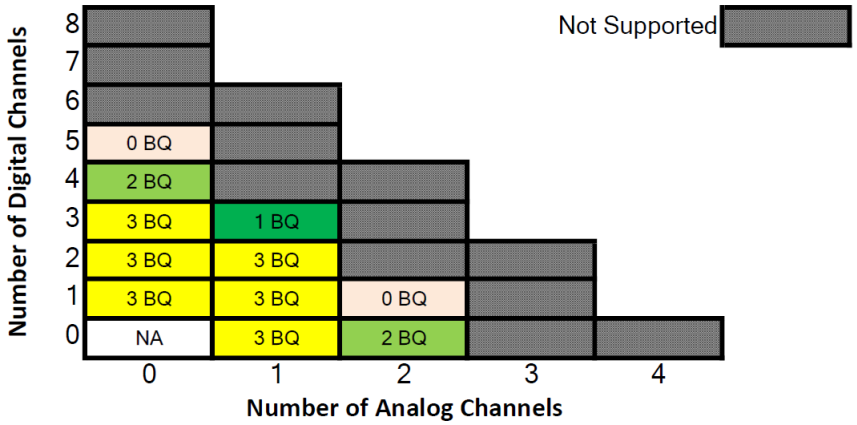

Figure 3-2. Channel Combinations for 96 kHz with DRE/AGC Enabled

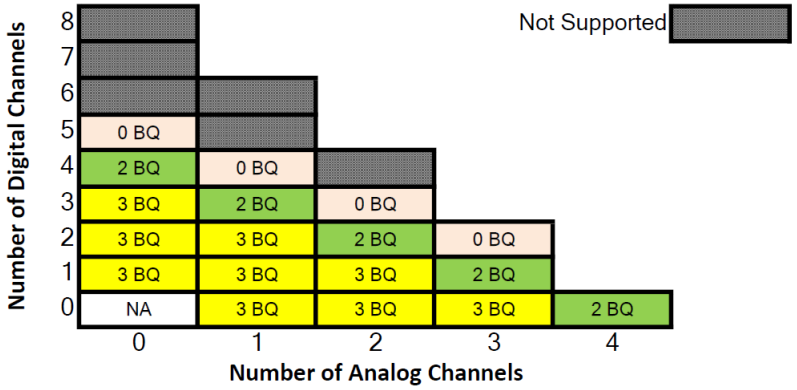

Figure 3-3. Channel Combinations for 96 kHz with DRE/AGC Disabled

3.4 192 kHz Sample Rate

All three decimation filter options are supported for 192 kHz operation. AGC and DRE, channel summers, and digital mixer are supported with the linear phase decimation filter option. Bi-quads are not supported for this mode.

For the low latency (and ultra-low latency) decimation filter response option, a maximum of three channels are supported when AGC or DRE is disabled. Only one channel is supported when AGC or DRE is enabled. Bi-quads, channel summers, and digital mixer are not supported for this mode.

3.5 384 kHz Sample Rate

Linear phase (DECI_FILT = 00) and ultra-low latency (DECI_FILT = 10) decimation filter responses are supported for the 384 kHz sample rate. AGC and DRE, bi-quads, channel summers, and digital mixer blocks are not supported for 384 kHz operation. A maximum of two channels are supported for 384 kHz and they can be analog, digital, or a combination of both.

3.6 768 kHz Sample Rate

Only linear phase (DECI_FILT = 00) decimation filter response is supported for 768 kHz sample rate. AGC and DRE, bi-quads, channel summers, and digital mixer blocks are not supported. Just one channel is supported. It can be an analog channel or a digital PDM microphone.

4 Example Configurations

A few example device configuration scripts for different combinations are presented below.

Example 1: Two input channels with four output channels using digital mixer.

1. Differential 2-channel input
2. Linear phase decimation filter
3. 24-bit TDM mode
4. Enable digital mixer mode
5. Digital Mixer 3: Ch3 Out = 0.5×Ch1 + 0.5×Ch2
6. Digital Mixer 4: Ch4 Out = 0.5×Ch1 - 0.5×Ch2

```
# Key: w 98 XX YY ==> write to I2C address 0x98, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# Differential 2-channel 24-bit TDM mode : INP1/INM1 - Ch1, INP2/INM2 - Ch2
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
################################################################
#
#
# Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# Wait for 1ms.
#
w 98 00 00 # Goto Page 0
w 98 02 81 # Wake-up device by I2C write into P0_R2 using internal AREG
w 98 6B 01          # Linear Phase Decimation Filter with digital mixer
# Digital Mixer 3 Configuration
w 98 00 04          # Goto Page 4
w 98 28 40 00 00 00 # Digital Mixer 3: Channel 1 Coefficient (MIX3_CH1) = 0.5
w 98 2C 40 00 00 00 # Digital Mixer 3: Channel 2 Coefficient (MIX3_CH2) = 0.5
w 98 30 00 00 00 00 # Digital Mixer 3: Channel 3 Coefficient (MIX3_CH3) = 0.0
w 98 34 00 00 00 00 # Digital Mixer 3: Channel 4 Coefficient (MIX3_CH4) = 0.0
# Digital Mixer 4 Configuration
w 98 00 04          # Goto Page 4
w 98 38 40 00 00 00 # Digital Mixer 4: Channel 1 Coefficient (MIX4_CH1) = 0.5
w 98 3C C0 00 00 00 # Digital Mixer 4: Channel 2 Coefficient (MIX4_CH2) = -0.5
w 98 40 00 00 00 00 # Digital Mixer 4: Channel 3 Coefficient (MIX4_CH3) = 0.0
w 98 44 00 00 00 00 # Digital Mixer 4: Channel 4 Coefficient (MIX4_CH4) = 0.0

w 98 00 00 # Goto Page 0
w 98 07 20 # TDM Mode with 24 Bits/Channel
w 98 73 c0 # Enable Ch.1 - Ch.2
w 98 74 f0 # Enable Ch.1 - Ch.4 ASI Output channels
w 98 75 e0 # Power up ADC
```

Example 2: Four input channels with channel summer.

1. Differential 4-channel input
2. Linear phase decimation filter
3. 32-bit TDM mode
4. Two-channel summer mode

```
# Key: w 98 XX YY ==> write to I2C address 0x98, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# The following list gives an example sequence of items that must be executed in the time
# between powering the device up and reading data from the device. Note that there are
# other valid sequences depending on which features are used.
#
# See the corresponding EVM user guide for jumper settings and audio connections.
#
# Differential 4-channel : INP1/INM1 - Ch1, INP2/INM2 - Ch2, INP3/INM3 - Ch3 and INP4/INM4 - Ch4
# FSYNC = 48 kHz (Output Data Sample Rate), BCLK = 11.2896 MHz (BCLK/FSYNC = 256)
####################################################################
#
#
# Power up IOVDD and AVDD power supplies keeping SHDNZ pin voltage LOW
# Wait for IOVDD and AVDD power supplies to settle to steady state operating voltage range.
# Release SHDNZ to HIGH.
# Wait for 1ms.
#
w 98 00 00 # Goto Page 0
w 98 02 81 # Wake-up device by I2C write into P0_R2 using internal AREG
w 98 6B 05 # Linear Phase Filter with 2 channel summer mode (DSP_CFG0)
w 98 00 00 # Goto Page 0
w 98 07 30 # TDM Mode with 32 Bits/Channel
w 98 73 f0 # Enable Ch.1 - Ch.4
w 98 74 f0 # Enable ASI Output channels
w 98 75 e0 # Power up ADC
```

5 References

- Texas Instruments, *TLV320ADC5140 Quad-Channel, 768-kHz, Burr-Brown Audio ADC*, data sheet.
- Texas Instruments, *TLV320ADC3140 Quad-Channel, 768-kHz, Burr-Brown Audio ADC*, data sheet.
- Texas Instruments, *PCM5140-Q1 Quad-Channel, 768-kHz, Burr-Brown™ Audio ADC*, data sheet.
- Texas Instruments, *PCM3140-Q1 Quad-Channel, 768-kHz, Burr-Brown™ Audio ADC*, data sheet.
- Texas Instruments, *TLV320ADCx140/PCMx140-Q1 Programmable Bi-quad Filter Configuration and Applications*, application note.

6 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2024) to Revision B (May 2024)	Page
• Updated *192 kHz Sample Rate* section	6

Changes from Revision * (April 2019) to Revision A (January 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Added PCMx140-Q1 throughout the document	1

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