Functional Safety Information

INAx180-Q1, INAx181-Q1, and INA185-Q1 Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for INAx180-Q1 (SOT-23-5, VSSOP-8, and TSSOP-14 packages), INAx181-Q1 (SOT-23-6, VSSOP-10, TSSOP-20, and DCK packages) and INA185-Q1 DCK package to aid in a functional safety system design. In this report, INAx180-Q1, INAx181-Q1, and INA185-Q1 refer to the family of devices including:

- INA180-Q1
- INA2180-Q1
- INA4180-Q1
- INA181-Q1
- INA2181-Q1
- INA4181-Q1
- INA185-Q1

Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

INA180-Q1 Functional Block Diagram, Figure 1-2, Figure 1-3, Figure 1-4, Figure 1-5, and Figure 1-6 show the device functional block diagrams for reference.

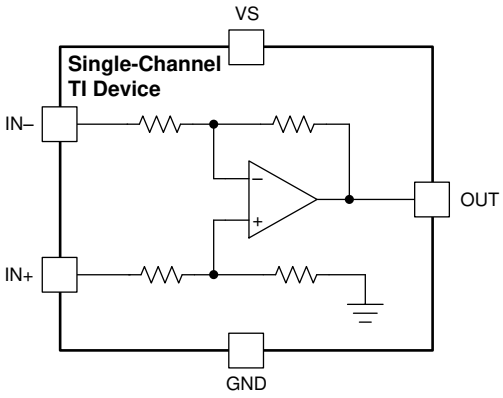

Figure 1-1. INA180-Q1 Functional Block Diagram

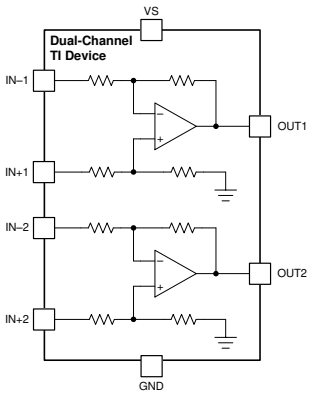

Figure 1-2. INA2180-Q1 Functional Block Diagram

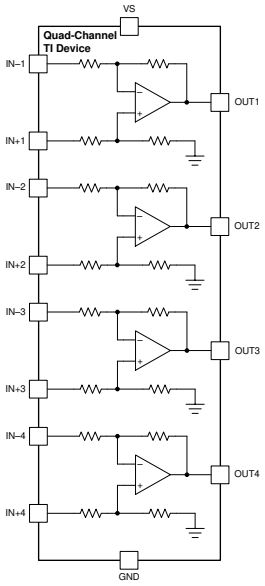

Figure 1-3. INA4180-Q1 Functional Block Diagram

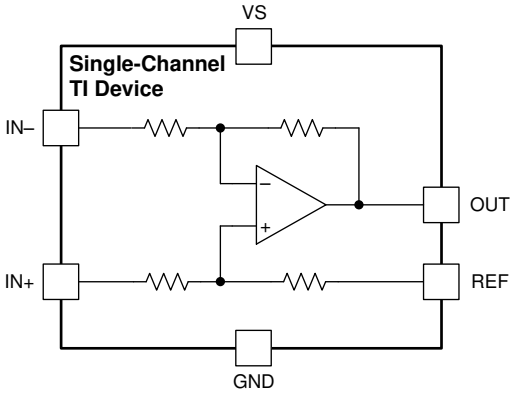

Figure 1-4. INA181-Q1 and INA185-Q1 Functional Block Diagram

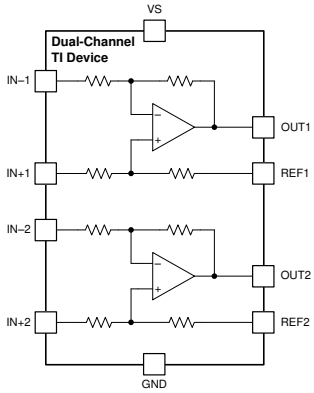

Figure 1-5. INA2181-Q1 Functional Block Diagram

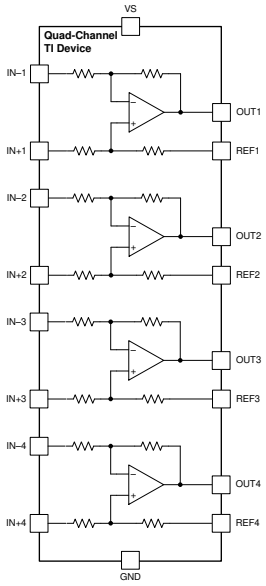

Figure 1-6. INA4181-Q1 Functional Block Diagram

INAx180-Q1, INAx181-Q1, and INA185-Q1 were developed using a quality-managed development process, but were not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 INA180-Q1, SOT-23-5 Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOT-23-5 package of INA180-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	4
Die FIT Rate	2
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 10 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 INA2180-Q1, VSSOP-8 Package

This section provides Functional Safety Failure In Time (FIT) rates for the VSSOP-8 package of INA2180-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 15 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.3 INA4180-Q1, TSSOP-14 Package

This section provides Functional Safety Failure In Time (FIT) rates for the TSSOP-14 package of INA4180-Q1 based on two different industry-wide used reliability standards:

- Table 2-5 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-6 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-5. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	10
Die FIT Rate	2
Package FIT Rate	8

The failure rate and mission profile information in Table 2-5 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 20 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-6. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-6 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.4 INA181-Q1, SOT-23-6 Package

This section provides Functional Safety Failure In Time (FIT) rates for the SOT-23-6 package of INA181-Q1 based on two different industry-wide used reliability standards:

- Table 2-7 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-8 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-7. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	4
Die FIT Rate	2
Package FIT Rate	2

The failure rate and mission profile information in Table 2-7 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 10 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-8. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-8 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.5 INA2181-Q1, VSSOP-10 Package

This section provides Functional Safety Failure In Time (FIT) rates for the VSSOP-10 package of INA2181-Q1 based on two different industry-wide used reliability standards:

- Table 2-9 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-10 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-9. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	2
Package FIT Rate	4

The failure rate and mission profile information in Table 2-9 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 15 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-10. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-10 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.6 INA4181-Q1, TSSOP-20 Package

This section provides Functional Safety Failure In Time (FIT) rates for the TSSOP-20 package of INA4181-Q1 based on two different industry-wide used reliability standards:

- Table 2-11 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-12 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-11. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	13
Die FIT Rate	2
Package FIT Rate	11

The failure rate and mission profile information in Table 2-11 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Automotive Control
- Power dissipation: 20 mW
- Climate type: World-wide Table 8
- Package factor: Lambda 3 Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-12. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op amp, comparators, voltage monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-12 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.7 INA181-Q1 and INA185-Q1, DCK Package

This section provides functional safety failure in time (FIT) rates for the DCK package of the INA181-Q1 and INA185-Q1 based on two different industry-wide used reliability standards:

- Table 2-13 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-14 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-13. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total component FIT rate	4
Die FIT rate	2
Package FIT rate	2

The failure rate and mission profile information in Table 2-13 comes from the reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission profile: Automotive Control
- Power dissipation: 10 mW
- Climate type: World-wide table 8
- Package factor (lambda 3): Table 17b
- Substrate material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-14. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp comparators, voltage monitors	8 FIT	45°C

The reference FIT rate and reference virtual T_J (junction temperature) in Table 2-14 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INAx180-Q1, INAx181-Q1 and INA185-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	10%
OUT to GND	20%
OUT to VS	15%
OUT functional, not in specification	50%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INAx180-Q1 (SOT-23-5, VSSOP-8, and TSSOP-14 packages), INAx181-Q1 (SOT-23-6, VSSOP-10, and TSSOP-20 packages), and INA185-Q1 (DCK package.) The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2, Table 4-6, Table 4-10, Table 4-14, Table 4-18, Table 4-22, and Table 4-26)
- Pin open-circuited (see Table 4-3, Table 4-7, Table 4-11, Table 4-15, Table 4-19, Table 4-23, and Table 4-27)
- Pin short-circuited to an adjacent pin (see Table 4-4, Table 4-8, Table 4-12, Table 4-16, Table 4-20, Table 4-24, and Table 4-28)
- Pin short-circuited to VS (see Table 4-5, Table 4-9, Table 4-13, Table 4-17, Table 4-21, Table 4-25, and Table 4-29)

Table 4-2 through Table 4-29 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 2.7 V to 5.5 V
- V_{IN+} = 12 V
- V_{REF} = V_S / 2 (INAx181-Q1 only)

4.1 INA180-Q1, SOT-23-5 Package (Pinout A)

INA180-Q1 Pin Diagram (SOT-23-5 Package, Pinout A) shows the INA180-Q1 pin diagram for the SOT-23-5 package (pinout A). For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the INA180-Q1 data sheet.

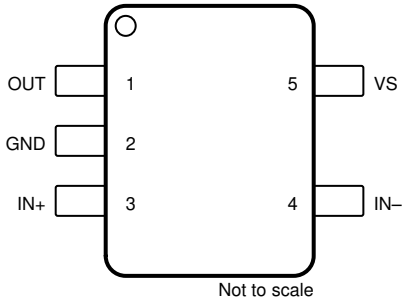

Figure 4-1. INA180-Q1 Pin Diagram (SOT-23-5 Package, Pinout A)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Normal operation.	D
IN+	3	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-	4	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
VS	5	Power supply shorted to GND.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
GND	2	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
IN+	3	Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-	4	Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
VS	5	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	2 - GND	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	B
GND	2	3 - IN+	In high-side configuration, a short from the bus supply to GND will occur.	B
IN+	3	4 - IN-	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-	4	5 - VS	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
VS	5	1 - OUT	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Power supply shorted to GND.	B
IN+	3	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-	4	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
VS	5	Normal operation.	D

4.2 INA180-Q1, SOT-23-5 Package (Pinout B)

Figure 4-2 shows the INA180-Q1 pin diagram for the SOT-23-5 package (pinout B). For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the INA180-Q1 datasheet.

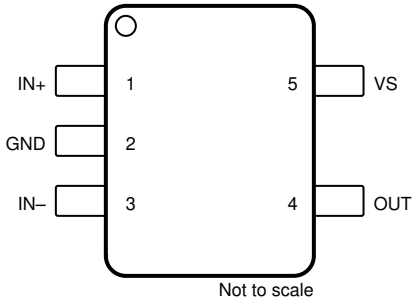

Figure 4-2. INA180-Q1 Pin Diagram (SOT-23-5 Package, Pinout B)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	2	Normal operation.	D
IN-	3	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT	4	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	5	Power supply shorted to GND.	B

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
GND	2	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
IN-	3	Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
OUT	4	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
VS	5	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	2 - GND	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	2	3 - IN-	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
IN-	3	4 - OUT	In high-side configuration, OUT pin shorted to bus supply. In low side configuration, output is shorted to GND.	A for high-side; B for low-side
OUT	4	5 - VS	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	5	1 - IN+	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side

Table 4-9. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	1	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
GND	2	Power supply shorted to GND.	B
IN-	3	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
OUT	4	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	5	Normal operation.	D

4.3 INA2180-Q1, VSSOP-8 Package

INA2180-Q1 Pin Diagram (VSSOP-8 Package) shows the INA2180-Q1 pin diagram for the VSSOP-8 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA2180-Q1 datasheet.

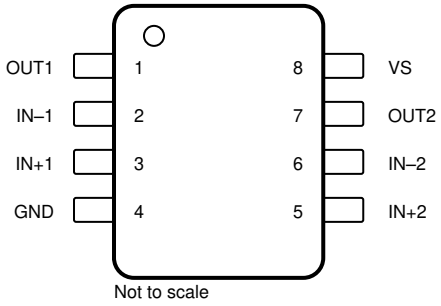

Figure 4-3. INA2180-Q1 Pin Diagram (VSSOP-8 Package)

Table 4-10. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-1	2	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
IN+1	3	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	4	Normal operation.	D
IN+2	5	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-2	6	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT2	7	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	8	Power supply shorted to GND.	B

Table 4-11. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
IN-1	2	Shunt resistor is not connected to amplifier. IN-1 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN+1	3	Shunt resistor is not connected to amplifier. IN+1 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
GND	4	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
IN+2	5	Shunt resistor is not connected to amplifier. IN+2 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-2	6	Shunt resistor is not connected to amplifier. IN-2 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
OUT2	7	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
VS	8	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B

Table 4-12. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	2 - IN-1	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
IN-1	2	3 - IN+1	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN+1	3	4 - GND	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	4	5 - IN+2	In high-side configuration, a short from the bus supply to GND will occur.	B
IN+2	5	6 - IN-2	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-2	6	7 - OUT2	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
OUT2	7	8 - VS	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	8	1 - OUT1	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

Table 4-13. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-1	2	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
IN+1	3	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
GND	4	Power supply shorted to GND.	B
IN+2	5	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-2	6	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
OUT2	7	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	8	Normal operation.	D

4.4 INA4180-Q1, TSSOP-14 Package

INA4180-Q1 Pin Diagram (TSSOP-14 Package) shows the INA4180-Q1 pin diagram for the TSSOP-14 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA4180-Q1 datasheet.

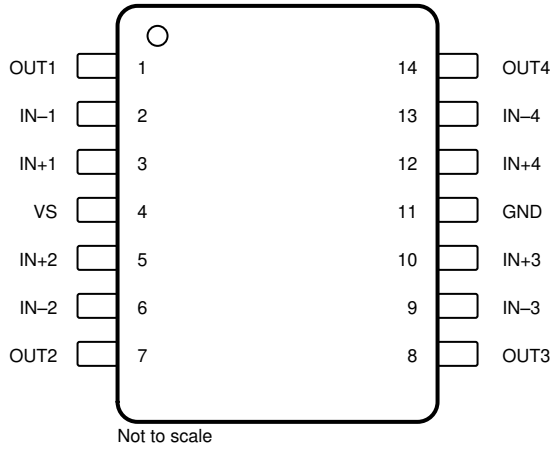

Figure 4-4. INA4180-Q1 Pin Diagram (TSSOP-14 Package)

Table 4-14. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-1	2	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
IN+1	3	In high-side configuration, a short from the bus supply to GND will occur.	B
VS	4	Power supply shorted to GND.	B
IN+2	5	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-2	6	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT2	7	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
OUT3	8	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-3	9	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
IN+3	10	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	11	Normal operation.	D
IN+4	12	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-4	13	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT4	14	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

Table 4-15. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
IN-1	2	Shunt resistor is not connected to amplifier. IN-1 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN+1	3	Shunt resistor is not connected to amplifier. IN+1 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
VS	4	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B
IN+2	5	Shunt resistor is not connected to amplifier. IN+2 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-2	6	Shunt resistor is not connected to amplifier. IN-2 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
OUT2	7	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
OUT3	8	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
IN-3	9	Shunt resistor is not connected to amplifier. IN-3 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN+3	10	Shunt resistor is not connected to amplifier. IN+3 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
GND	11	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
IN+4	12	Shunt resistor is not connected to amplifier. IN+4 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-4	13	Shunt resistor is not connected to amplifier. IN-4 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
OUT4	14	Output can be left open. There is no effect on the IC, but the output will not be measured.	C

Table 4-16. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	2 - IN-1	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
IN-1	2	3 - IN+1	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN+1	3	4 - VS	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
VS	4	5 - IN+2	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN+2	5	6 - IN-2	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-2	6	7 - OUT	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
OUT2	7	8 - OUT3	Outputs shorted together. Output stage of each channel will contest for control of output voltage. Depending on input voltage conditions, output current may be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	B
OUT3	8	9 - IN-3	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
IN-3	9	10 - IN+3	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN+3	10	11 - GND	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	11	12 - IN+4	In high-side configuration, a short from the bus supply to GND will occur.	B
IN+4	12	13 - IN-4	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-4	13	14 - OUT4	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
OUT4	14	1 - OUT1	Outputs shorted together. Output stage of each channel will contest for control of output voltage. Depending on input voltage conditions, output current may be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	B

Table 4-17. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-1	2	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
IN+1	3	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
VS	4	Normal operation.	D
IN+2	5	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-2	6	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
OUT2	7	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
OUT3	8	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-3	9	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
IN+3	10	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
GND	11	Power supply shorted to GND.	B
IN+4	12	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-4	13	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
OUT4	14	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

4.5 INA181-Q1, SOT-23-6 Package

INA181-Q1 Pin Diagram (SOT-23-6 Package) shows the INA181-Q1 pin diagram for the SOT-23-6 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA181-Q1 datasheet.

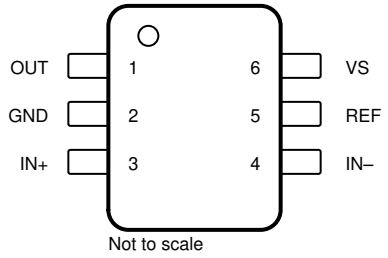

Figure 4-5. INA181-Q1 Pin Diagram (SOT-23-6 Package)

Table 4-18. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Normal operation.	D
IN+	3	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-	4	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
REF	5	Normal operation if REF pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF=GND by design; B otherwise
VS	6	Power supply shorted to GND.	B

Table 4-19. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
GND	2	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
IN+	3	Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-	4	Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
REF	5	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
VS	6	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B

Table 4-20. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	2 - GND	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	3 - IN+	In high-side configuration, a short from the bus supply to GND will occur.	B
IN+	3	4 - IN-	Inputs shorted together, so no sense voltage applied. Output will stay close to REF potential.	B
IN-	4	5 - REF	In high-side configuration, REF shorted to bus supply. In low-side configuration, REF shorted to GND (normal operation if REF is at GND potential by design).	A for high-side; B for low-side (D if REF=GND by design)
REF	5	6 - VS	Normal operation if REF pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF=VS by design; B otherwise
VS	6	1 - OUT	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

Table 4-21. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Power supply shorted to GND.	B
IN+	3	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-	4	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
REF	5	Normal operation if REF pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF=VS by design; B otherwise
VS	6	Normal operation.	D

4.6 INA2181-Q1, VSSOP-10 Package

INA2181-Q1 Pin Diagram (VSSOP-10 Package) shows the INA2181-Q1 pin diagram for the VSSOP-10 package. For a detailed description of the device pins please refer to the '*Pin Configuration and Functions*' section in the INA2181-Q1 datasheet.

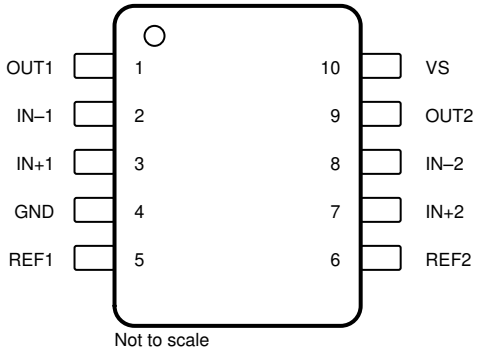

Figure 4-6. INA2181-Q1 Pin Diagram (VSSOP-10 Package)

Table 4-22. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-1	2	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
IN+1	3	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	4	Normal operation.	D
REF1	5	Normal operation if REF1 pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF1=GND by design; C otherwise
REF2	6	Normal operation if REF2 pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF2=GND by design; C otherwise
IN+2	7	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-2	8	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT2	9	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	10	Power supply shorted to GND.	B

Table 4-23. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
IN-1	2	Shunt resistor is not connected to amplifier. IN-1 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN+1	3	Shunt resistor is not connected to amplifier. IN+1 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
GND	4	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
REF1	5	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
REF2	6	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
IN+2	7	Shunt resistor is not connected to amplifier. IN+2 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-2	8	Shunt resistor is not connected to amplifier. IN-2 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
OUT2	9	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
VS	10	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B

Table 4-24. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	2 - IN-1	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
IN-1	2	3 - IN+1	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN+1	3	4 - GND	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	4	5 - REF1	Normal operation if REF1 pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF1=GND by design; B otherwise
REF1	5	6 - REF2	Normal operation if REF1 and REF2 are at the same potential by design; otherwise the system measurement will be incorrect.	D if REF1=REF2 by design; B otherwise
REF2	6	7 - IN+2	In high-side configuration, REF2 shorted to bus supply. In low-side configuration, REF2 shorted to GND through R_{SHUNT} (normal operation if REF2 is at GND potential by design).	A for high-side; B for low-side (D if REF2=GND by design)
IN+2	7	8 - IN-2	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-2	8	9 - OUT2	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
OUT2	9	10 - VS	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	10	1 - OUT1	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

Table 4-25. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	1	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-1	2	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
IN+1	3	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
GND	4	Power supply shorted to GND.	B
REF1	5	Normal operation if REF1 pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF1=VS by design; B otherwise
REF2	6	Normal operation if REF2 pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF2=VS by design; B otherwise
IN+2	7	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-2	8	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
OUT2	9	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
VS	10	Normal operation.	D

4.7 INA4181-Q1, TSSOP-20 Package

INA4181-Q1 Pin Diagram (TSSOP-20 Package) shows the INA4181-Q1 pin diagram for the TSSOP-20 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA4181-Q1 datasheet.

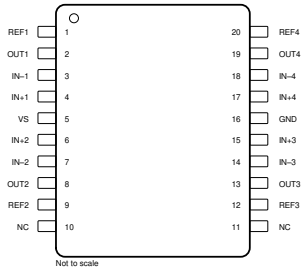

Figure 4-7. INA4181-Q1 Pin Diagram (TSSOP-20 Package)

Table 4-26. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF1	1	Normal operation if REF1 pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF1=GND by design; C otherwise
OUT1	2	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-1	3	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
IN+1	4	In high-side configuration, a short from the bus supply to GND will occur.	B
VS	5	Power supply shorted to GND.	B
IN+2	6	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-2	7	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT2	8	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
REF2	9	Normal operation if REF2 pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF2=GND by design; C otherwise
NC	10	No internal connection.	D
NC	11	No internal connection.	D
REF3	12	Normal operation if REF3 pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF3=GND by design; C otherwise
OUT3	13	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-3	14	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
IN+3	15	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	16	Normal operation.	D
IN+4	17	In high-side configuration, a short from the bus supply to GND will occur.	B

Table 4-26. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-4	18	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT4	19	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
REF4	20	Normal operation if REF4 pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF4=GND by design; C otherwise

Table 4-27. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF1	1	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
OUT1	2	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
IN-1	3	Shunt resistor is not connected to amplifier. IN-1 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN+1	4	Shunt resistor is not connected to amplifier. IN+1 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
VS	5	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B
IN+2	6	Shunt resistor is not connected to amplifier. IN+2 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-2	7	Shunt resistor is not connected to amplifier. IN-2 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
OUT2	8	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
REF2	9	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
NC	10	No internal connection.	D
NC	11	No internal connection.	D
REF3	12	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
OUT3	13	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
IN-3	14	Shunt resistor is not connected to amplifier. IN-3 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN+3	15	Shunt resistor is not connected to amplifier. IN+3 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
GND	16	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
IN+4	17	Shunt resistor is not connected to amplifier. IN+4 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-4	18	Shunt resistor is not connected to amplifier. IN-4 pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
OUT4	19	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
REF4	20	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B

Table 4-28. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
REF1	1	2 - OUT1	Output shorted to reference voltage. Output voltage will be incorrect. Depending on state of output voltage, reference voltage source may be short circuit limited.	B

Table 4-28. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT1	2	3 - IN-1	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
IN-1	3	4 - IN+1	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN+1	4	5 - VS	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
VS	5	6 - IN+2	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN+2	6	7 - IN-2	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-2	7	8 - OUT2	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
OUT2	8	9 - REF2	Output shorted to reference voltage. Output voltage will be incorrect. Depending on state of output voltage, reference voltage source may be short circuit limited.	B
REF2	9	10 - NC	Normal operation.	D
NC	10	11 - NC	Normal operation.	D
NC	11	12 - REF3	Normal operation.	D
REF3	12	13 - OUT3	Output shorted to reference voltage. Output voltage will be incorrect. Depending on state of output voltage, reference voltage source may be short circuit limited.	B
OUT3	13	14 - IN-3	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
IN-3	14	15 - IN+3	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN+3	15	16 - GND	In high-side configuration, a short from the bus supply to GND will occur.	B
GND	16	17 - IN+4	In high-side configuration, a short from the bus supply to GND will occur.	B
IN+4	17	18 - IN-4	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-4	18	19 - OUT4	In high-side configuration, a short from the bus voltage to the output stage will occur. The device may become damaged. In low-side configuration, output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating, could cause die junction temperature to exceed 150°C.	A for high-side; B for low-side
OUT4	19	20 - REF4	Output shorted to reference voltage. Output voltage will be incorrect. Depending on state of output voltage, reference voltage source may be short circuit limited.	B
REF4	20	1 - REF1	Normal operation if REF1 and REF4 are at the same potential by design; otherwise the system measurement will be incorrect.	D if REF1=REF4 by design; B otherwise

Table 4-29. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
REF1	1	Normal operation if REF1 pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF1=VS by design; B otherwise
OUT1	2	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-1	3	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
IN+1	4	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
VS	5	Normal operation.	D
IN+2	6	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-2	7	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
OUT2	8	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
REF2	9	Normal operation if REF2 pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF2=VS by design; B otherwise
NC	10	No internal connection.	D
NC	11	No internal connection.	D
REF3	12	Normal operation if REF3 pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF3=VS by design; B otherwise
OUT3	13	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
IN-3	14	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
IN+3	15	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
GND	16	Power supply shorted to GND.	B
IN+4	17	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-4	18	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
OUT4	19	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
REF4	20	Normal operation if REF4 pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF4=VS by design; B otherwise

4.8 INA181-Q1 and INA185-Q1, DCK Package

Figure 4-8 shows the INA181-Q1 and INA185-Q1 pin diagram for the DCK package. For a detailed description of the device pins, see the *Pin Configuration and Functions* section in the INA181-Q1 and INA185-Q1 data sheets.

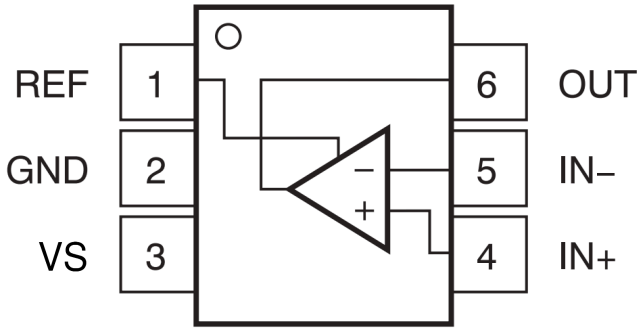

Figure 4-8. Pin Diagram (DCK) Package

Table 4-30. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
REF	1	Normal operation if REF pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF = GND by design; B otherwise
GND	2	Normal operation	D
VS	3	Power supply shorted to GND.	B
IN+	4	In high-side configuration, a short from the bus supply to GND will occur.	B
IN-	5	In high-side configuration, a short from the bus supply to GND will occur (through R_{SHUNT}). High current will flow from bus supply to GND. The shunt may be damaged. In low-side configuration, normal operation.	B for high-side; D for low-side
OUT	6	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

Table 4-31. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
REF	1	Output common-mode voltage is not defined. Output will not maintain a linear relationship with differential input voltage.	B
GND	2	When GND is floating, output will be incorrect as it is no longer referenced to GND.	B
VS	3	No power to device. Device may be biased through inputs. Output will be incorrect and close to GND.	B
IN+	4	Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
IN-	5	Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	B
OUT	6	Output can be left open. There is no effect on the IC, but the output will not be measured.	C

Table 4-32. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effects	Failure Effect Class
REF	1	GND	Normal operation if REF pin is at GND potential by design; otherwise the system measurement will be incorrect.	D if REF=GND by design; B otherwise
GND	2	VS	Power supply shorted to GND.	B
VS	3	IN+	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND.	A for highside; B for low-side
IN+	4	IN-	Inputs shorted together, so no sense voltage applied. Output will stay close to REF potential.	B
IN-	5	OUT	In high-side configuration, OUT shorted to bus supply with damage possible. In low-side configuration, OUT shorted to GND.	A for high-side; B for low-side
OUT	6	REF	Output shorted to reference voltage. Output voltage will be incorrect. Depending on state of output voltage, reference voltage source may be short circuit limited.	B

Table 4-33. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effects	Failure Effect Class
REF	1	Normal operation if REF pin is at VS potential by design; otherwise the system measurement will be incorrect.	D if REF=VS by design; B otherwise.
GND	2	Power supply shorted to GND.	B
VS	3	Normal operation.	D
IN+	4	In high-side configuration, device power supply shorted to bus supply. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for highside; B for low-side
IN-	5	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}). In low-side configuration, device power supply shorted to GND .	A for highside; B for low-side
OUT	6	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B

5 Revision History

Changes from Revision A (September 2020) to Revision B (October 2023)	Page
• Added INA181-Q1 (DCK) package and INA185-Q1 to the document	2

Changes from Revision * (March 2020) to Revision A (September 2020)	Page
• Added information for INA2180-Q1, INA4180-Q1, INA2181-Q1, and INA4181-Q1	2
• Updated the numbering format for tables, figures, and cross-references throughout the document	2

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