Functional Safety Information

INA253-Q1
Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA253-Q1 (TSSOP-20 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

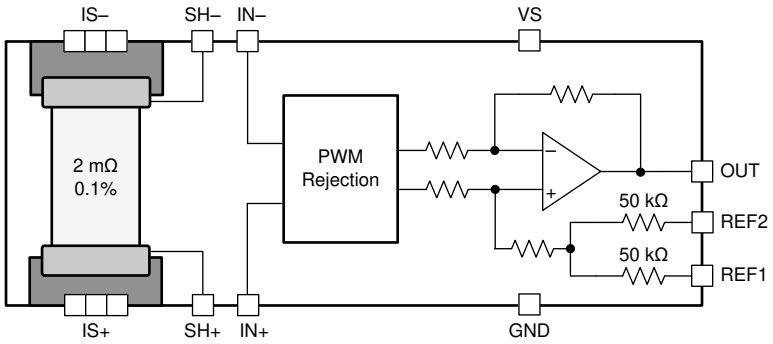

Figure 1-1. Functional Block Diagram

INA253-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA253-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	15
Die FIT Rate	3
Package FIT Rate	12

Failure for shunt resistor IN+, IN-, SH+, SH- included as a part of the package FIT rate.

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 82 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS/BICMOS Analog & Mixed ≤ 50V Supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA253-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	10%
OUT saturated to VS or GND	40%
OUT functional, not in specification	40%
Shunt resistor open pin (IN+, IN-, SH+, SH-)	5%
Pin to pin short, any two pins	5%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA253-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to VS (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the INA253-Q1 pin diagram. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA253-Q1 data sheet.

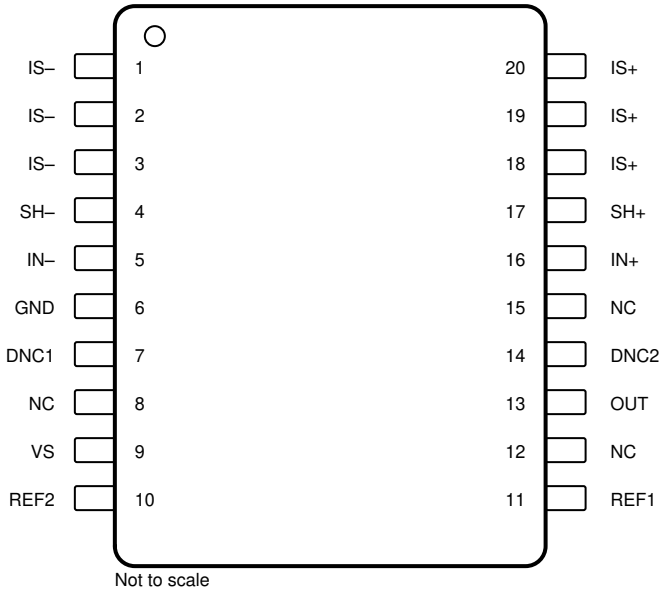

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_S = 5 V
- V_{CM} = 12 V
- $V_{REF1} = V_{REF2} = V_S / 2$

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IS-	1	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. The shunt could be damaged due to high current. In low-side configuration, normal operation.	A for high-side; D for low-side

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IS-	2	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. The shunt could be damaged due to high current. In low-side configuration, normal operation.	A for high-side; D for low-side
IS-	3	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. The shunt could be damaged due to high current. In low-side configuration, normal operation.	A for high-side; D for low-side
SH-	4	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. Shunt bond wires of pin SH- and die metal trace between pin IN- and SH- may be damaged. In low-side configuration, normal operation.	A for high-side; D for low-side
IN-	5	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. Shunt bond wires of pin SH- and die metal trace between pin IN- and SH- may be damaged. In low-side configuration, normal operation.	A for high-side; D for low-side
GND	6	Normal operation.	D
DNC1	7	High current may flow in or out of this pin. Device may be damaged.	A
NC	8	Normal operation.	D
VS	9	Power supply shorted to GND. No power to device.	B
REF2	10	Normal operation if this pin is at GND potential by design, otherwise the system measurement will be incorrect.	D if REF2=GND by design; C otherwise
REF1	11	Normal operation if this pin is at GND potential by design, otherwise the system measurement will be incorrect.	D if REF1=GND by design; C otherwise
NC	12	Normal operation.	D
OUT	13	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
DNC2	14	High current may flow in or out of this pin. Device may be damaged.	A
NC	15	Normal operation.	D
IN+	16	A short from the bus supply to GND will occur. High current will flow from bus supply to GND. Bond wires of pins IN+ and SH+ and die metal trace between pin IN+ and SH+ will be damaged.	A
SH+	17	A short from the bus supply to GND will occur. High current will flow from bus supply to GND. Bond wires of pins IN+ and SH+ and die metal trace between pin IN+ and SH+ will be damaged.	A
IS+	18	A short from the bus supply to GND will occur. High current will flow from bus supply to GND. This will affect the system functionality but will not affect the IC.	C
IS+	19	A short from the bus supply to GND will occur. High current will flow from bus supply to GND. This will affect the system functionality but will not affect the IC.	C
IS+	20	A short from the bus supply to GND will occur. High current will flow from bus supply to GND. This will affect the system functionality but will not affect the IC.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IS-	1	Bus supply to load path is cut off and no load current will flow. IN- will be at the same potential as bus supply. Differential input voltage is 0V.	C
IS-	2	Bus supply to load path is cut off and no load current will flow. IN- will be at the same potential as bus supply. Differential input voltage is 0V.	C
IS-	3	Bus supply to load path is cut off and no load current will flow. IN- will be at the same potential as bus supply. Differential input voltage is 0V.	C
SH-	4	Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	C

Table 4-3. Pin FMA for Device Pins Open-Circuited (continued)

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	5	Shunt resistor is not connected to amplifier. IN- pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	C
GND	6	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
DNC1	7	Normal operation.	D
NC	8	Normal operation.	D
VS	9	No power to device. Device may be biased through inputs. Output will be close to GND.	B
REF2	10	Output common-mode voltage is not defined correctly, therefore the output will not maintain a linear relationship with differential input voltage.	C
REF1	11	Output common-mode voltage is not defined correctly, therefore the output will not maintain a linear relationship with differential input voltage.	C
NC	12	Normal operation.	D
OUT	13	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
DNC2	14	Normal operation.	D
NC	15	Noise pickup on this pin may corrupt output.	C
IN+	16	Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	C
SH+	17	Shunt resistor is not connected to amplifier. IN+ pin may float to an unknown value. Output will go to an unknown value not to exceed VS or GND.	A
IS+	18	Bus supply to load path is cut off and no load current will flow. IN+ will be at the same potential as GND. Differential input voltage is 0V.	C
IS+	19	Bus supply to load path is cut off and no load current will flow. IN+ will be at the same potential as GND. Differential input voltage is 0V.	C
IS+	20	Bus supply to load path is cut off and no load current will flow. IN+ will be at the same potential as GND. Differential input voltage is 0 V.	C

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IS-	1	2 - IS-	Normal operation.	D
IS-	2	3 - IS-	Normal operation.	D
IS-	3	4 - SH-	Measurement accuracy will be degraded. There is no effect on the IC.	C
SH-	4	5 - IN-	Normal operation.	D
IN-	5	6 - GND	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. Shunt bond wires of pin SH- and die metal trace between pin IN- and SH- may be damaged. In low-side configuration, normal operation.	A for high-side; D for low-side
GND	6	7 - DNC1	High current may flow in or out of DNC1 pin. Device may be damaged.	A
DNC1	7	8 - NC	Normal operation.	D
NC	8	9 - VS	Normal operation.	D
VS	9	10 - REF2	Normal operation if REF2 is at VS potential by design, otherwise the system measurement will be incorrect.	D if REF2=V2 by design; C otherwise
REF2	10	11 - REF1	Normal operation is REF1 and REF2 pins are shorted by design, otherwise the system measurement will be incorrect.	D if REF1=REF2 by design; C otherwise
REF1	11	12 - NC	Normal operation.	D
NC	12	13 - OUT	Normal operation.	D
OUT	13	14 - DNC2	High current may flow in or out of DNC2 pin. Device may be damaged.	A
DNC2	14	15 - NC	Normal operation.	D
NC	15	16 - IN+	Normal operation.	D

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin (continued)

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
IN+	16	17 - SH+	Normal operation.	D
SH+	17	18 - IS+	Measurement accuracy will be degraded. There is no effect on the IC.	C
IS+	18	19 - IS+	Normal operation.	D
IS+	19	20 - IS+	Normal operation.	D
IS+	20	1 - IS-	Shunt resistor is bypassed. Differential input voltage is 0 V.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to VS

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IS-	1	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt could be damaged due to high current. In low side configuration, system functionality will be affected negatively but not the IC.	A for high-side; C for low-side
IS-	2	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt could be damaged due to high current. In low side configuration, system functionality will be affected negatively but not the IC.	A for high-side; C for low-side
IS-	3	In high-side configuration, a short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt could be damaged due to high current. In low side configuration, system functionality will be affected negatively but not the IC.	A for high-side; C for low-side
SH-	4	A short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt and die metal trace between pin IN- and SH- will be damaged.	A
IN-	5	A short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. The shunt and die metal trace between pin IN- and SH- will be damaged.	A
GND	6	Power supply shorted to GND. No power to the device.	B
DNC1	7	High current may flow in or out of this pin. Device may be damaged.	A
NC	8	Normal operation.	D
VS	9	Normal operation.	D
REF2	10	Normal operation if this pin is at VS potential by design, otherwise the system measurement will be incorrect.	D if REF2=VS by design; C otherwise
REF1	11	Normal operation if this pin is at VS potential by design, otherwise the system measurement will be incorrect.	D if REF1=VS by design; C otherwise
NC	12	Normal operation.	D
OUT	13	Output will be pulled to VS and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
DNC2	14	High current may flow in or out of this pin. Device may be damaged.	A
NC	15	Normal operation, with a slight increase in quiescent current.	C
IN+	16	A short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Die metal trace between pin IN+ and SH+ will be damaged.	A
SH+	17	A short from the bus supply to VS will occur. High current will flow from bus supply to VS or vice versa. Die metal trace between pin IN+ and SH+ will be damaged.	A
IS+	18	In low-side configuration, a short from VS to GND will occur. The shunt could be damaged due to high current. In high side configuration, bus supply is shorted to VS and system functionality will be affected negatively but not the IC.	A for low-side; C for high-side
IS+	19	In low-side configuration, a short from VS to GND will occur. The shunt could be damaged due to high current. In high side configuration, bus supply is shorted to VS and system functionality will be affected negatively but not the IC.	A for low-side; C for high-side
IS+	20	In low-side configuration, a short from VS to GND will occur. The shunt could be damaged due to high current. In high side configuration, bus supply is shorted to VS and system functionality will be affected negatively but not the IC.	A for low-side; C for high-side

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