SoundPlus™ Digitally-Controlled MICROPHONE PREAMPLIFIER

FEATURES

- FULLY DIFFERENTIAL INPUT-TO-OUTPUT ARCHITECTURE
- DIGITALLY-CONTROLLED GAIN USING SPI™:
  - Gain Range: 9dB through 60dB, 3dB per Step
  - Unity (0dB) Gain Setting via Serial Port
- DYNAMIC PERFORMANCE:
  - Equivalent Input Noise with Z_S = 150Ω and Gain = 30dB: –123dBu
  - Total Harmonic Distortion plus Noise (THD+N) with Gain = 30dB: 0.0006%
- ZERO CROSSING DETECTION MINIMIZES AUDIBLE ARTIFACTS WHEN GAIN SWITCHING
- INTEGRATED DC SERVO MINIMIZES OUTPUT OFFSET VOLTAGE
- COMMON-MODE SERVO IMPROVES CMRR
- FOUR-WIRE SERIAL CONTROL PORT INTERFACE:
  - Simple Interface to Microprocessor or DSP Serial Ports
  - Supports Daisy-Chaining of Multiple PGA2505 Devices
- OVER-RANGE OUTPUT PIN PROVIDES CLIPPING INDICATION
- FOUR GENERAL-PURPOSE DIGITAL OUTPUT PINS
- ±5V POWER SUPPLIES
- AVAILABLE IN AN SSOP-24 PACKAGE

APPLICATIONS

- MICROPHONE PREAMPLIFIERS AND MIXERS
- DIGITAL MIXERS AND RECORDERS
- DIGITAL AUDIO EDITING SYSTEMS
- BROADCAST EQUIPMENT
- INTERCOMS

DESCRIPTION

The PGA2505 is a digitally-controlled, analog microphone preamplifier designed for use as a front-end for high-performance audio analog-to-digital converters (ADCs). The PGA2505 features include low noise, wide dynamic range, and a differential signal path. An on-chip dc servo loop is employed to minimize dc offset, while a common-mode servo function may be used to enhance common-mode rejection.

The PGA2505 features a gain range of 9dB through 60dB (3dB/step), along with a unity gain setting. The wide gain range allows the PGA2505 to be used with a variety of microphones. Gain settings and internal functions are programmed using a 16-bit control word, which is loaded using a simple serial port interface. A serial data output pin provides support for daisy-chained connection of multiple PGA2505 devices. Four programmable digital outputs are provided for controlling the external switching of input pads, phantom power, and high-pass filters. The PGA2505 requires both +5V and –5V power supplies and is available in a small SSOP-24 package.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		PGA2505	UNIT
Supply Voltage, AGND or DGND to VA+		–0.3 to +5.5	V
Supply Voltage, AGND or DGND to VA–		+0.3 to –5.5	V
Supply Voltage, AGND or DGND to VD–		+0.3 to –5.5	V
Voltage Difference, VA– to VD–		±0.3	V
Ground Difference, AGND to DGND		±0.3	V
Analog Input Voltage		(VA–) –0.3 to (VA+) +0.3	V
Digital Input Voltage		(DGND) – 0.3 to (VA+) + 0.3	V
Input Current of All Pins Except Supply		±10	mA
Power Dissipation		See Electrical Characteristics, *Thermal Resistance* parameter	
Junction Temperature Range, T_J		–40 to +150	°C
Operating Free-Air Temperature Range, T_A		–40 to +85	°C
Storage Temperature Range, T_{STG}		–60 to +150	°C
ESD Ratings	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	150	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
PGA2505	SSOP-24	DB	PGA2505I

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, VA+ = +5V, VA– = –5V, VD– = –5V, and V_{COM}IN = 0V, unless otherwise noted.

PARAMETERS		CONDITIONS	PGA2505 MIN	PGA2505 TYP	PGA2505 MAX	UNIT
DC CHARACTERISTICS						
Step Size		Gain = 9dB through 60dB		3		dB
Gain Error		All gain settings		±0.5		dB
AC CHARACTERISTICS						
THD+N		f_{IN} = 1kHz, Gain = 0dB, V_{OUT} = 3.5V_{RMS}		–110	–100	dB
		f_{IN} = 1kHz, Gain = 30dB, V_{OUT} = 3.5V_{RMS}		–105	–95	dB
ANALOG INPUT						
Maximum Input Voltage		Gain = 0dB	VA– +1.5		VA+ –2.0	V
Input Resistance						
Per Input Pin				4600		Ω
Differential				9200		Ω
ANALOG OUTPUT						
Output Voltage Range		V_{COM}IN = 0V, R_L = 600Ω	VA– +0.9		VA+ –0.9	V
Output Offset Voltage		DC servo on, any gain		±0.08	±1	mV
Input-Referred Offset		DC servo off, gain = 30dB		±1		mV
Output Resistive Loading			600			Ω
Load Capacitance Stability				100		pF
Short Circuit Current		10-second duration		100		mA
DIGITAL CHARACTERISTICS						
High-Level Input Voltage	V_{IH}		+2.0		VA+	V
Low-Level Input Voltage	V_{IL}		–0.3		0.8	V
High-Level Output Voltage	V_{OH}	I_O = 200µA	(VA+) – 1.0			V
Low-Level Output Voltage	V_{OL}	I_O = –3.2mA			0.4	V
Input Leakage Current	I_{IN}			2	10	µA
POWER SUPPLY						
Operating Voltage						
VA+			+4.75	+5	+5.25	V
VA–			–4.75	–5	–5.25	V
VD–			–4.75	–5	–5.25	V
Quiescent Current						
IA+		VA+ = +5V		30	40	mA
IA–		VA– = –5V		30	40	mA
ID–		VD– = –5V		1	2	mA
TEMPERATURE RANGE						
Operating Free-Air Temperature Range	T_A		–40		÷85	°C
Thermal Resistance						
SSOP-24	θ_{JA}	High-K board		72		°C/W
	θ_{JC}	High-K board		42		°C/W

SWITCHING CHARACTERISTICS

Over operating free-air temperature range (unless otherwise noted).

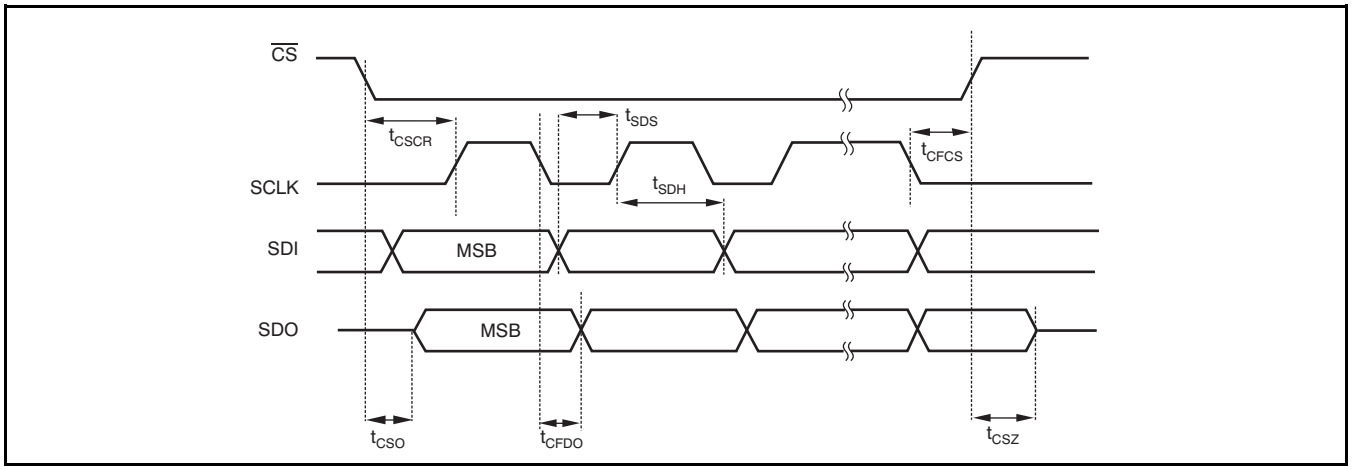
PARAMETER		TEST CONDITIONS	PGA2505			UNIT
			MIN	TYP	MAX	
f_{SCLK}	Serial clock (SCLK) frequency		0		6.25	MHz
t_{PH}	Serial clock (SCLK) pulse width low		80			ns
t_{PL}	Serial clock (SCLK) pulse width high		80			ns

TIMING REQUIREMENTS

Over operating free-air temperature range (unless otherwise noted).

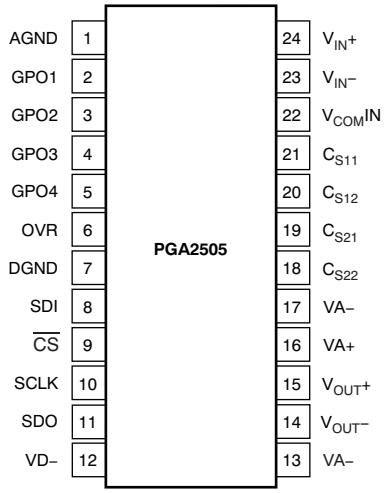
PARAMETER		TEST CONDITIONS	PGA2505			UNIT
			MIN	TYP	MAX	
INPUT TIMING						
t_{SDS}	SDI setup time		20			ns
t_{SDH}	SDI hold time		20			ns
t_{CSCR}	$\overline{CS}$ falling to SCLK rising		90			ns
t_{CFCS}	SCLK falling to $\overline{CS}$ rising		35			ns
OUTPUT TIMING						
t_{CSO}	$\overline{CS}$ low to SDO active				35	ns
t_{CFDO}	SCLK falling to SDO data valid				60	ns
t_{CSZ}	$\overline{CS}$ high to SDO high impedance				100	ns

SERIAL PORT TIMING DIAGRAM



PIN CONFIGURATION

DB PACKAGE
SSOP-24
(TOP VIEW)



PIN ASSIGNMENTS

TERMINAL		DESCRIPTION
NAME	PIN#	
AGND	1	Analog Ground
GPO1	2	General-Purpose CMOS Logic Output
GPO2	3	General-Purpose CMOS Logic Output
GPO3	4	General-Purpose CMOS Logic Output
GPO4	5	General-Purpose CMOS Logic Output
OVR	6	Over Range Output (Active High)
DGND	7	Digital Ground
SDI	8	Serial Data Input
$\overline{CS}$	9	Chip Select Input (Active Low)
SCLK	10	Serial Data Clock Input
SDO	11	Serial Data Output
VD–	12	–5V Digital Supply
VA–	13	–5V Analog Supply
V_{OUT}–	14	Inverting Analog Output
V_{OUT}+	15	Noninverting Analog Output
VA+	16	+5V Analog Supply
VA–	17	–5V Analog Supply
C_{S22}	18	External DC Servo Capacitor #2, Terminal 2
C_{S21}	19	External DC Servo Capacitor #2, Terminal 1
C_{S12}	20	External DC Servo Capacitor #1, Terminal 2
C_{S11}	21	External DC Servo Capacitor #1, Terminal 1
V_{COM}IN	22	Common Mode Voltage Input, 0V to +2.5V
V_{IN}–	23	Inverting Analog Input
V_{IN}+	24	Noninverting Analog Input

TYPICAL CHARACTERISTICS

At T_A = +25°C, VA+ = +5V, VA– = –5V, VD– = –5V, and V_{COM}IN = 0V, unless otherwise noted.

EQUIVALENT INPUT NOISE AS A FUNCTION OF GAIN WITH Z_S = 0Ω

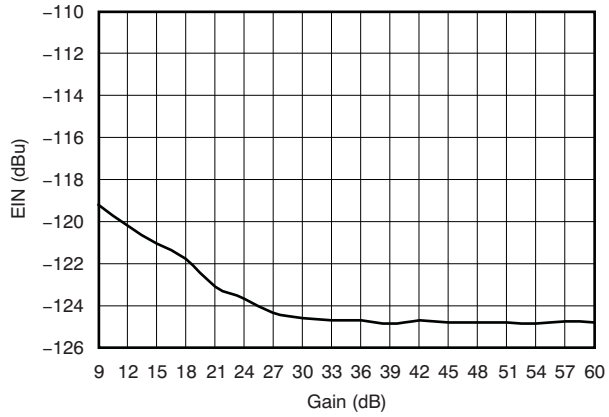


Figure 1.

EQUIVALENT INPUT NOISE AS A FUNCTION OF GAIN WITH Z_S = 150Ω

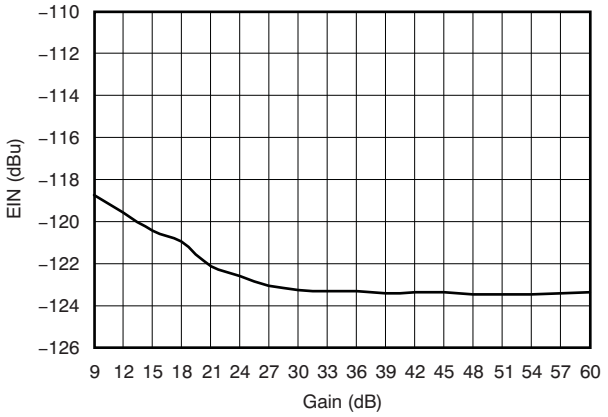


Figure 2.

THD+N vs GAIN

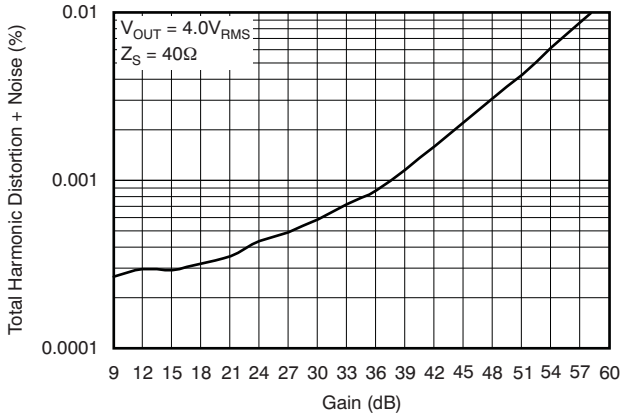


Figure 3.

THD+N vs GAIN AND NOISE vs GAIN

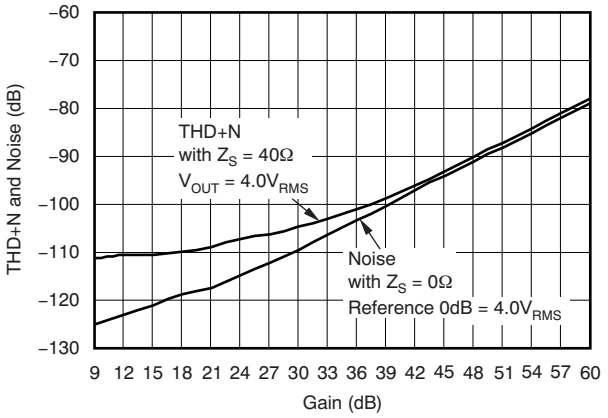


Figure 4.

THD + N vs FREQUENCY (Z_S = 40Ω, R_L = 600Ω, V_{COM}IN = 0V, BW = 22Hz to 22kHz)

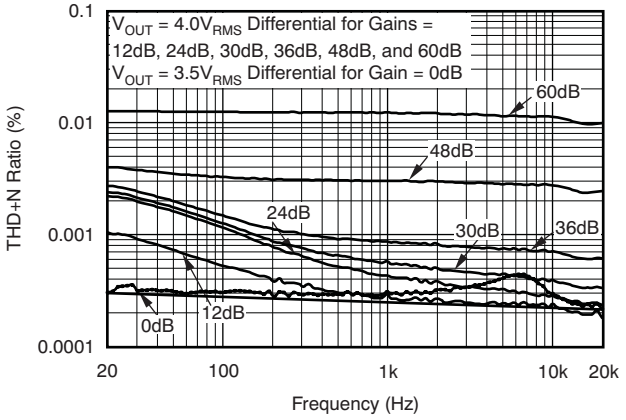


Figure 5.

THD + N vs FREQUENCY (Z_S = 40Ω, R_L = 600Ω, V_{COM}IN = +2.5V, BW = 22Hz to 22kHz)

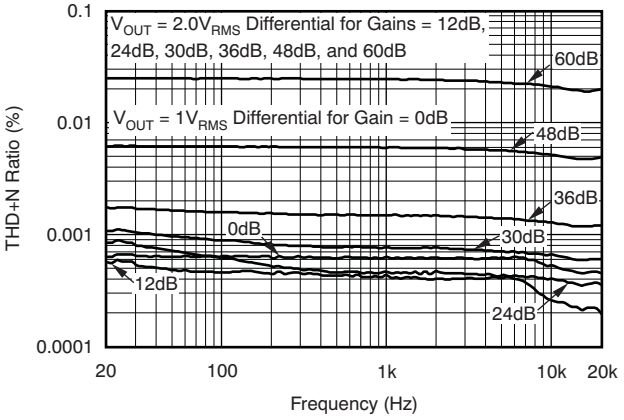


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, VA+ = +5V, VA– = –5V, VD– = –5V, and V_{COM}IN = 0V, unless otherwise noted.

THD + N vs FREQUENCY
(Z_S = 40Ω, R_L = 600Ω, V_{COM}IN = +2.5V, BW = 22Hz to 22kHz)

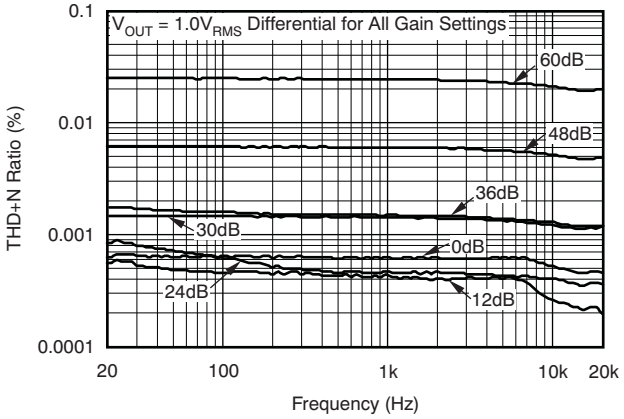


Figure 7.

THD + N vs OUTPUT SWING
(Z_S = 40Ω, R_L = 600Ω, V_{COM}IN = 0V, BW = 22Hz to 22kHz)

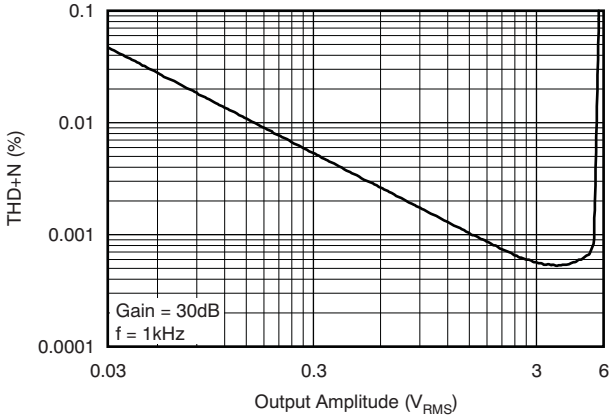


Figure 8.

APPLICATION INFORMATION

OVERVIEW

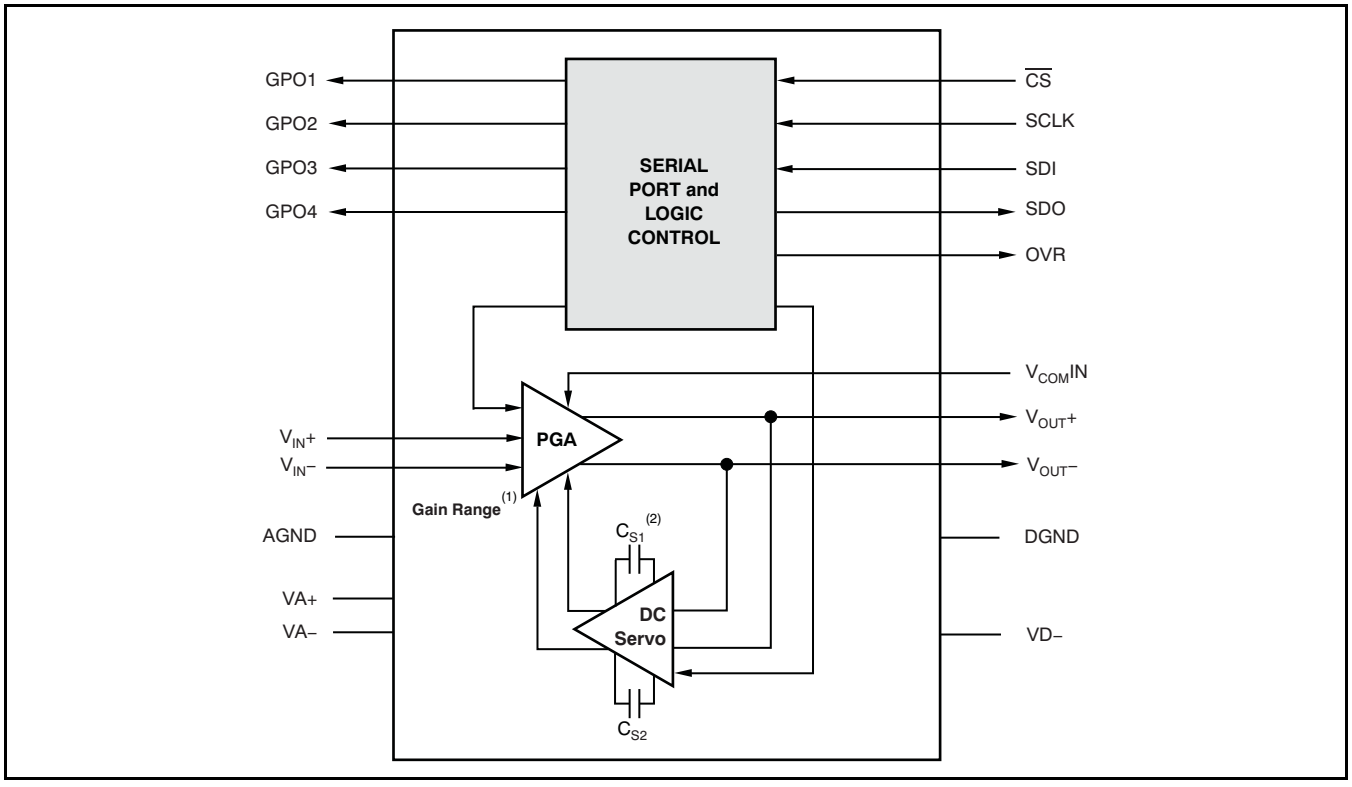
The PGA2505 is a digitally-controlled microphone preamplifier integrated circuit designed to amplify the output of dynamic and condenser microphones and drive high-performance audio analog-to-digital converters (ADCs). A functional block diagram of the PGA2505 is shown in Figure 9.

The analog input to the preamplifier is provided differentially at the V_{IN}+ and V_{IN}– inputs (pins 24 and 23, respectively). The programmable gain amplifier can be programmed to either pass through the signal at unity gain, or apply 9dB to 60dB of gain to the input signal. The gain of the amplifier is adjustable over the full 9dB to 60dB range in 3dB steps. The differential output of the PGA2505 is made available at V_{OUT}+ and V_{OUT}– (pins 15 and 14, respectively). Gain is controlled using a serial port interface.

The four-wire serial port interface is used to program the PGA2505 gain and support functions. A 16-bit control word is utilized to program these functions (see Figure 10). A serial data output pin provides support for daisy-chaining multiple PGA2505 devices on a single serial interface bus (see Figure 11).

The differential analog output of the PGA2505 is constantly monitored by a dc servo amplifier loop. The purpose of the servo loop is to minimize the dc offset voltage present at the analog outputs by feeding back an error signal to the input stage of the programmable gain amplifier. The error signal is then used to correct the offset. The $\overline{DC}$ servo may be disabled by setting the dc bit in the serial control word to '1'.

Two external capacitors are required for the dc servo function, with one capacitor connected between C_{S11} and C_{S12} (pins 21 and 20), and the second capacitor connected between C_{S21} and C_{S22} (pins 19 and 18). A capacitor value of 1µF is recommended for use in most microphone preamplifier applications. Capacitor values up to 4.7µF may be used. However, larger valued capacitors result in longer settling times for the dc servo loop. Smaller capacitors under 0.22µF may result in additional distortion in the low frequency audio bandwidth.



(1) Gain Range: 0dB, or +9dB to +60dB (3dB/step).

(2) C_{S1} and C_{S2} are external dc servo integrator capacitors, and are connected across the C_{S11}/C_{S12} and C_{S21}/C_{S22} pins, respectively.

Figure 9. PGA2505 Functional Block Diagram

The PGA2505 includes a common-mode servo function. This function is enabled and disabled using the CM bit in the serial control word; see Figure 10. When enabled, the servo provides common-mode negative feedback at the input differential pair, resulting in very low common-mode input impedance. The differential input impedance is not affected by this feedback. This function is useful when the source is floating, or has a high common-mode output impedance.

When the source is floating, the only connection between the source and the ground is through the PGA2505 preamplifier input resistance. The input common-mode parasitic current is determined by high output impedance of the source, not by input impedance of the amplifier. Therefore, input common-mode interference can be reduced by lowering the common-mode input impedance while at the same time not increasing the input common-mode current. Increasing common-mode current degrades common-mode rejection. Using the common-mode servo, overall common-mode rejection can be improved by suppressing low and medium frequency common-mode interference.

The common-mode servo function is designed to operate with a total common-mode input capacitance (including the microphone cable capacitance) of up to 10nF. Beyond this limit, stable servo operation is not assured.

The common-mode voltage control input, named V_{COM}IN (pin 22), allows the PGA2505 output and input to be dc-biased to a common-mode voltage between 0V and +2.5V and should not be left floating. This configuration allows for a dc-coupled interface between the PGA2505 preamplifier output and the inputs of common single-supply audio ADCs.

The zero crossing control input is provided for enabling and disabling the internal zero crossing detector function. This function is enabled and disabled using the ZC bit in the serial control word; see Figure 10. Zero crossing detection is used to force gain changes on zero crossings of the analog input signal. This configuration limits the glitch energy associated with switching gain, thereby minimizing audible artifacts at the preamplifier output. Because zero crossing detection can add some delay when performing gain changes (up to 16ms maximum for a detector timeout event), there may be cases where the user may wish to disable the function. Setting the ZC bit high enables zero crossing detection, with gain changes occurring immediately when programmed.

Note that because the zero crossing detector requires setup, the user should set the ZC bit as a first operation. Subsequent changes in gain occur on the zero crossings provided that the ZC bit setting is maintained.

An over-range indicator output, OVR, is provided at pin 6. The OVR pin is an active high, CMOS-logic-level output. The over-range output is forced high when the preamplifier output voltage exceeds one of two preset thresholds. The threshold is programmed through the serial port interface using the OR bit. If OR = '0', then the output threshold is set to $5.1V_{RMS}$ differential, which is approximately 1dB below the specified output voltage range. If OR = '1', then the output threshold is set to $4.0V_{RMS}$ differential, which is approximately 3dB below the specified output voltage range.

The PGA2505 includes four programmable digital outputs, named GPO1, GPO2, GPO3, and GPO4 (pins 2, 3, 4, and 5 respectively), that are controlled via the serial port interface. These pins are CMOS-logic-level outputs. These pins may be used to control relay drivers or switches used for external preamplifier functions, including input pads, filtering, polarity reversal, or phantom power.

ANALOG INPUTS AND OUTPUTS

An analog signal is input differentially across the V_{IN}+ (pin 24) and V_{IN}– (pin 23) inputs. The input voltage range and input impedance are provided in the Electrical Characteristics table. The Applications Information section of this data sheet provides additional details regarding typical input circuit considerations when interfacing the PGA2505 to a microphone input.

Both V_{IN}+ and V_{IN}– are biased at approximately 0.65V below the common-mode input voltage, supplied at V_{COM}IN (pin 22). The use of ac-coupling capacitors (see Figure 10) is highly recommended for the analog inputs of the PGA2505. If dc-coupling is required for a given application, the user must take this offset into account.

It is recommended that a small capacitor be connected from each analog input pin to analog ground. Values of at least 50pF are recommended. See Figure 10 for larger capacitors used for EMI filtering, which satisfies this requirement.

The analog output is presented differentially across V_{OUT}+ (pin 15) and V_{OUT}– (pin 14). The output voltage range is provided in the Electrical Characteristics table. The analog output is designed to drive a 600Ω differential load while meeting the published THD+N specifications and typical performance graphs.

SERIAL PORT OPERATION

The serial port interface for the PGA2505 is comprised of four wires: $\overline{CS}$ (pin 9), SCLK (pin 10), SDI (pin 8), and SDO (pin 11). Figure 10 illustrates the serial port protocol.

The $\overline{CS}$ input functions as the chip select and word latch clock for the serial port. The $\overline{CS}$ input must be low in order to clock data into and out of the serial port. The control word is latched on a low-to-high transition of the $\overline{CS}$ input.

The serial port ignores the SCLK and SDI inputs when $\overline{CS}$ is high, and the SDO output is set to a high impedance state while $\overline{CS}$ is high.

The SCLK input is used to clock serial data into the SDI pin and out of the SDO pin. The SDI pin functions as the serial data input, and is used to write the serial port register. The SDO pin is the shift register serial output, and is used for either register read-back or for daisy-chaining multiple PGA2505 devices. Data on SDI are sampled on the rising edge of SCLK, while data are clocked out of SDO on the falling edge of SCLK.

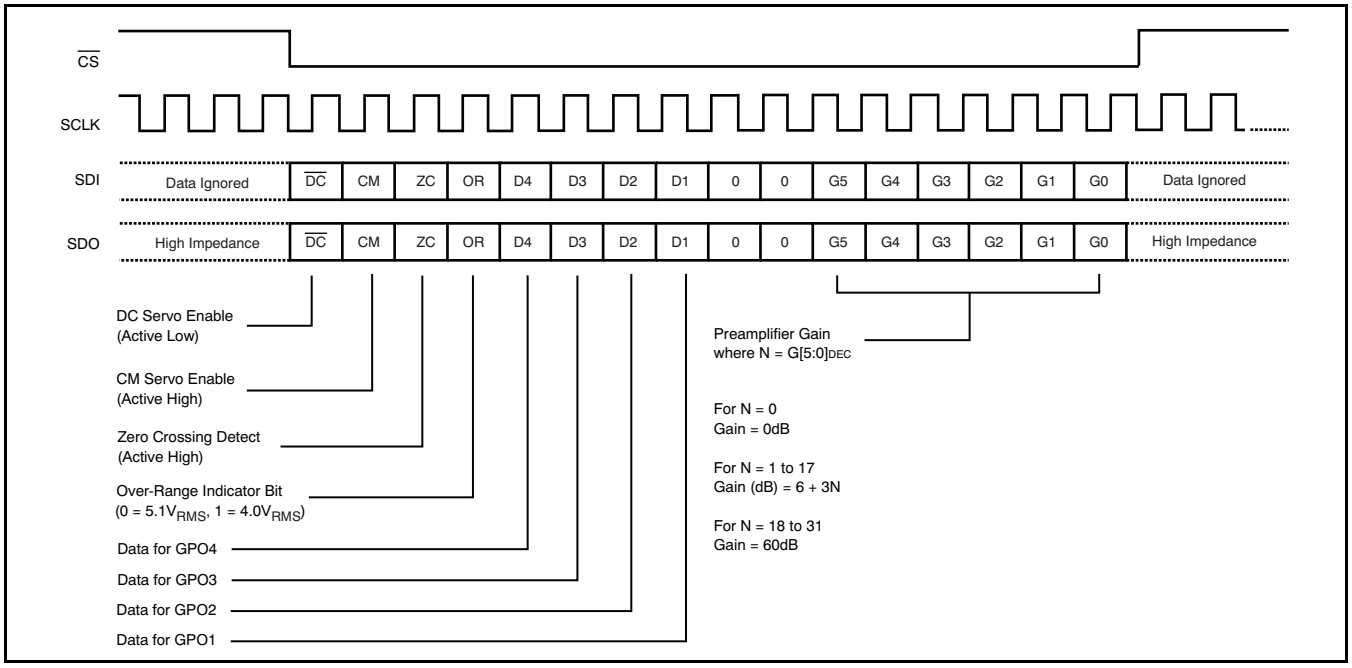


Figure 10. Serial Port Protocol

DAISY-CHAINING MULTIPLE PGA2505 PREAMPLIFIERS

Because the serial port interface may be viewed as a serial in, serial out shift register, multiple PGA2505 preamplifiers may be connected in a cascaded or daisy-chained fashion, as shown in Figure 11. The daisy-chained PGA2505 devices behave as a 16 x *N*-bit shift register, where *N* is the number of cascaded PGA2505 devices.

To program all of the devices, simply force $\overline{CS}$ low for 16 x *N* serial clock periods and clock in 16 x *N* bits of control data. The $\overline{CS}$ input is then forced high to latch in the new settings.

A timing diagram for the daisy-chain application is shown in Figure 12.

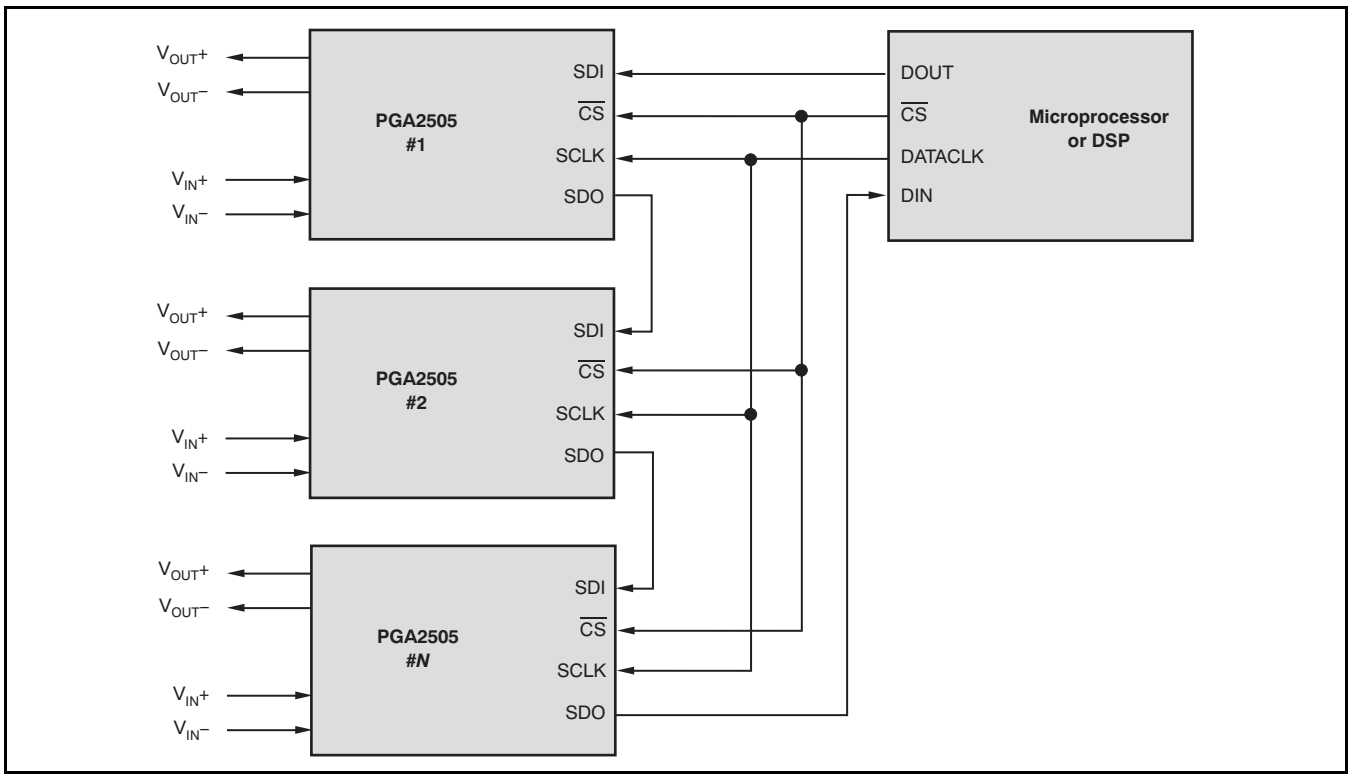


Figure 11. Daisy-Chain Configuration for Multiple PGA2505 Preamplifiers

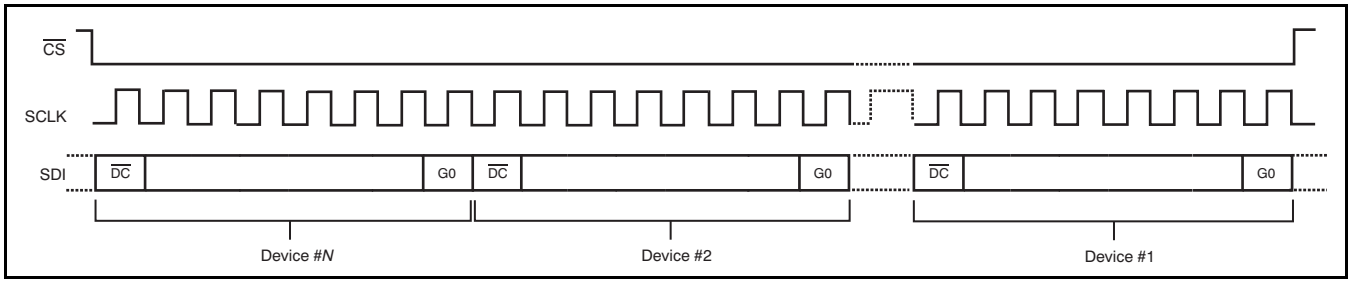


Figure 12. Serial Port Operation for Daisy-Chain Operation

APPLICATION INFORMATION

This section provides practical information for designing the PGA2505 into end applications.

BASIC CIRCUIT CONFIGURATION

A typical application configuration, without the input and output circuitry, is shown in Figure 13. Power-supply bypass and dc servo capacitors are shown with recommended values. All capacitors should be placed as close as possible to the PGA2505 package to limit inductive noise coupling. Surface-mount capacitors are recommended (X7R ceramic for the 0.1µF and 1µF capacitors, and low ESR tantalum for the 4.7µF capacitors).

The PGA2505 can be placed on a split ground plane, with analog and digital pins separated basically down the center of the package. (Note that AGND is on the opposite side.) However, there must be a low impedance connection between the analog and digital grounds at a common return point.

The dc common-mode input, $V_{COM}IN$ (pin 22), can be connected to analog ground or a dc voltage (such as the reference or common voltage output of an audio ADC). When biasing this input to a dc voltage, keep in mind that both the analog output and input pins will be level-shifted by the value of the bias voltage.

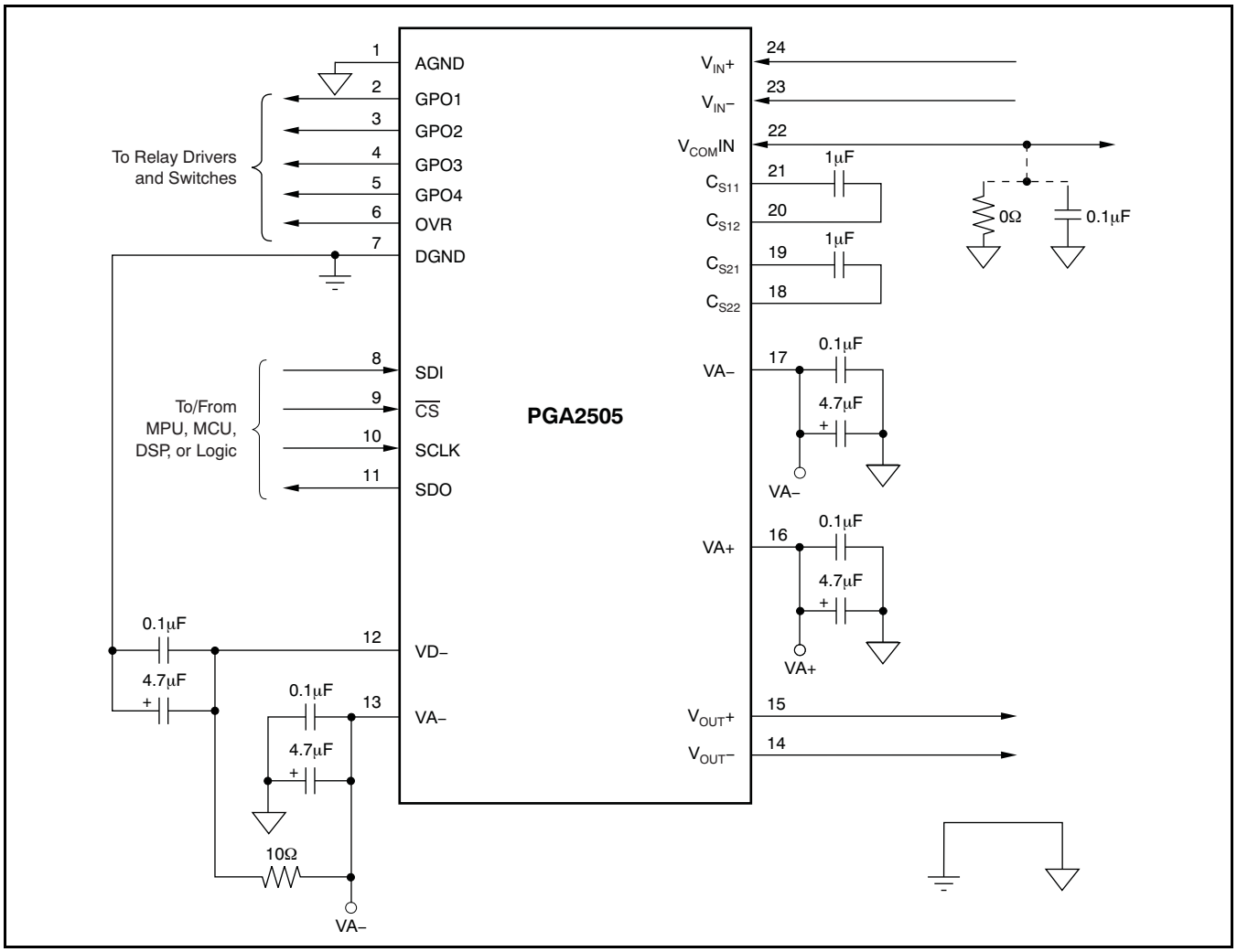


Figure 13. Basic Circuit Configuration for the PGA2505

INPUT CIRCUIT CONSIDERATIONS

For proper operation, the input circuit for the PGA2505 must include several items that are common to most microphone preamplifiers. Figure 14 shows a typical input circuit configuration. Other functions, such as input attenuation (pads), filters, and polarity reversal switches are commonly found in preamplifier circuits, but are not shown here in order to focus on the basic input circuit requirements.

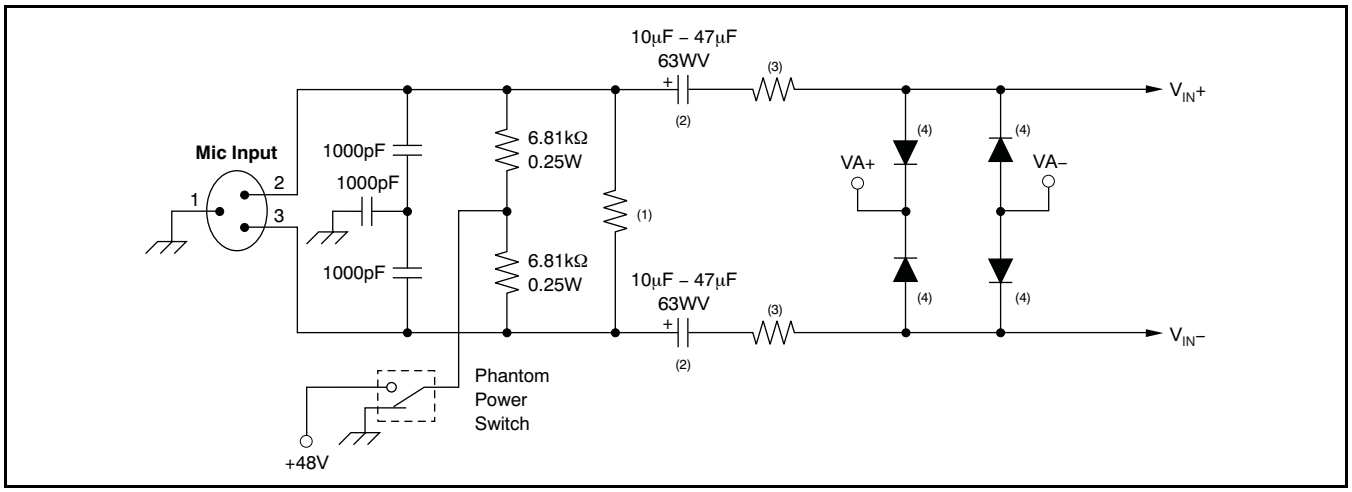
The microphone input is typically taken from a balanced XLR or TRS input connection (XLR shown). Three 1000pF capacitors provide simple EMI filtering for the circuit. Additional filtering for low- or high-frequency noise may be added, depending on the end application environment. A bridging resistor is shown and may be selected to provide the desired overall input impedance required for a given microphone. This resistance is in parallel with the phantom power bias resistors and the PGA2505 input resistance to set the actual impedance seen by the microphone.

Connections for +48V phantom power, required for condenser microphones, are shown in Figure 14. The phantom power requires an On/Off switch, because dynamic microphones do not require phantom power and may be damaged if power is applied. DC-blocking capacitors are required between the phantom power connections and the PGA2505 inputs. The blocking capacitors are selected to have a high working voltage rating, with 50V being the minimum and 63V recommended for long-term reliability.

The blocking capacitors, along with the PGA2505 input resistance, form a high-pass filter circuit. With the typical input resistance of the PGA2505 specified in the Electrical Characteristics table, the value of the capacitor can be chosen to meet the desired low frequency response for the end application. At the same time, the value should be no greater than required, because larger capacitors store more charge and increase the surge current seen at the preamplifier when a short circuit occurs on the microphone input connector.

To protect the PGA2505 from large surge currents, power Schottky diodes are placed on the input pins to both the VA+ and VA– power supplies. Schottky diodes are used because of the lower turn-on voltage compared to standard rectifier diodes. Power devices are required because the surge currents from a large valued blocking capacitor (47µF) can exceed 4.5A for a very short duration of time. It is recommended that the Schottky diode chosen for this application be specified for at least a 10A surge current.

The use of a series current-limiting resistor before the protection diodes aids in handling surge currents, although the resistor adds noise to the circuit. Select a current-liming resistor value that is as high as tolerable for the desired noise performance of the preamplifier circuit.



(1) Bridging resistor; used to set the impedance seen by the microphone.

(2) The blocking capacitor value is selected based upon the desired low frequency response.

(3) Current-limiting resistor. Select the highest value tolerable based upon input noise requirements.

(4) Schottky diode; selected for fast turn-on and rated for a minimum of a 10A surge current. Recommended device is the MBRA120LT3 from ON Semiconductor.

Figure 14. Typical Input Circuit for the PGA2505

OPERATION WITH V_{COM}IN = +2.5V

When interfacing the analog outputs of the PGA2505 with audio ADC inputs, the converter may frequently have a common-mode dc output pin. This pin may be connected to the V_{COM}IN pin of the PGA2505 in order to facilitate a dc-coupled interface between the two devices. The common-mode dc voltage level is typically +2.5V, although some converters may have a slightly lower value, usually between +2.1V and +2.5V. There are several issues that must be considered when operating the PGA2505 in this fashion.

Both the analog input and output pins of the PGA2505 are level-shifted by the V_{COM}IN voltage. The analog outputs are shifted to the V_{COM}IN level, while the analog inputs are shifted to approximately V_{COM}IN – 0.65V, as a result of the offset that normally exists on the input pins. The level-shifting limits the input and output swing of the PGA2505, reducing the overall signal-to-noise ratio and degrading the THD+N performance.

Given V_{COM}IN = +2.5V and gains of 0dB through 60dB, the output swing is limited to less than one-half that specified in the Electrical Characteristics table. The output hard-clips at approximately a diode drop below the VA+ supply rail and a diode drop above analog ground.

Given V_{COM}IN = +2.5V and a gain of 0dB, the practical maximum input or output voltage swing is approximately $1.0V_{RMS}$ differential. Increasing the signal level much beyond this point results in a substantial increase in distortion.

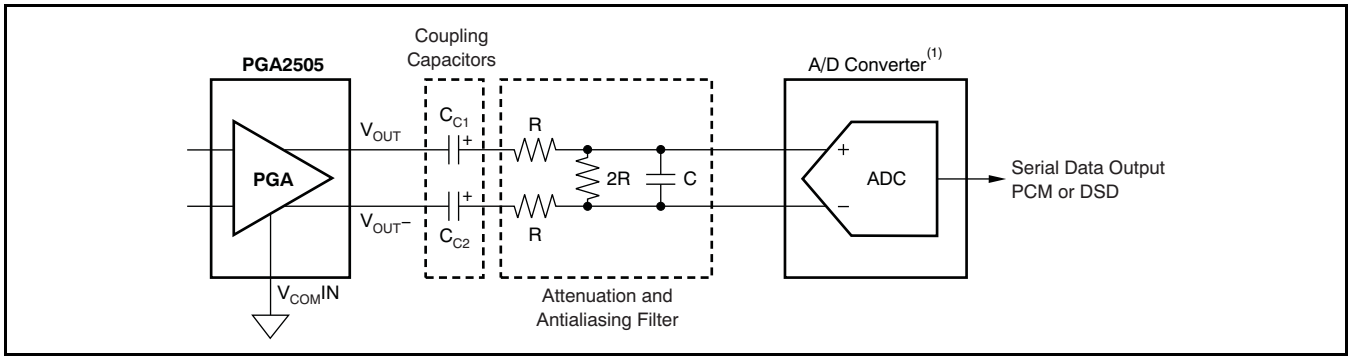
Plots of THD+N vs Frequency are shown in the Typical Characteristics section of this data sheet for both V_{COM}IN = 0V and +2.5V. The performance difference can be seen when comparing the plots. The user must consider whether the difference is acceptable for the end application.

As a suggested alternative, the PGA2505 analog outputs may be ac-coupled to the ADC inputs, allowing the PGA2505 to operate with V_{COM}IN = 0V in order to achieve best performance. The ac-coupling capacitors affect the overall low-frequency response of the preamplifier and converter combination, and the user is advised to choose a value that best suits the application requirements.

Figure 15 illustrates a typical PGA2505 to audio ADC interface using ac-coupling. In addition to the coupling capacitors, a passive RC filter is required as an antialiasing filter for the converter. The vast majority of audio ADCs are of the oversampling delta-sigma variety, with a simple single-pole filter meeting the anti-aliasing requirements for this type of converter. Providing at least 6dB of attenuation also allows the PGA2505 to operate near full signal swing without overdriving the ADC inputs.

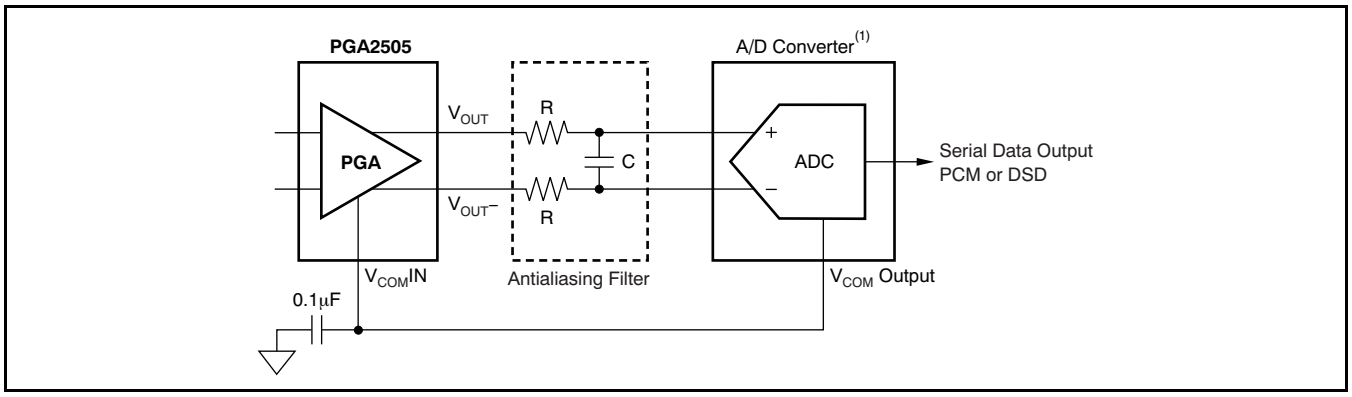
Figure 16 illustrates an application where the V_{COM}IN pin of the PGA2505 is connected to the common-mode dc output of the audio ADC, with a dc-coupled interface between the PGA2505 analog outputs and the ADC analog inputs.

To ensure optimal performance, an output buffer to the PGA2505 is recommended. Figure 17 illustrates the use of an OPA1632 as the buffer. Additionally, the feedback circuitry functions as the antialiasing filter shown in Figure 15 and Figure 16. Having a differential buffer with attenuation of 6dB or greater also allows for the PGA2505 to maximize the output signal swing, while ensuring that the input swing does not exceed the full-scale input range of the ADC. An OPA227 is used to drive the output common-mode of the OPA1632.



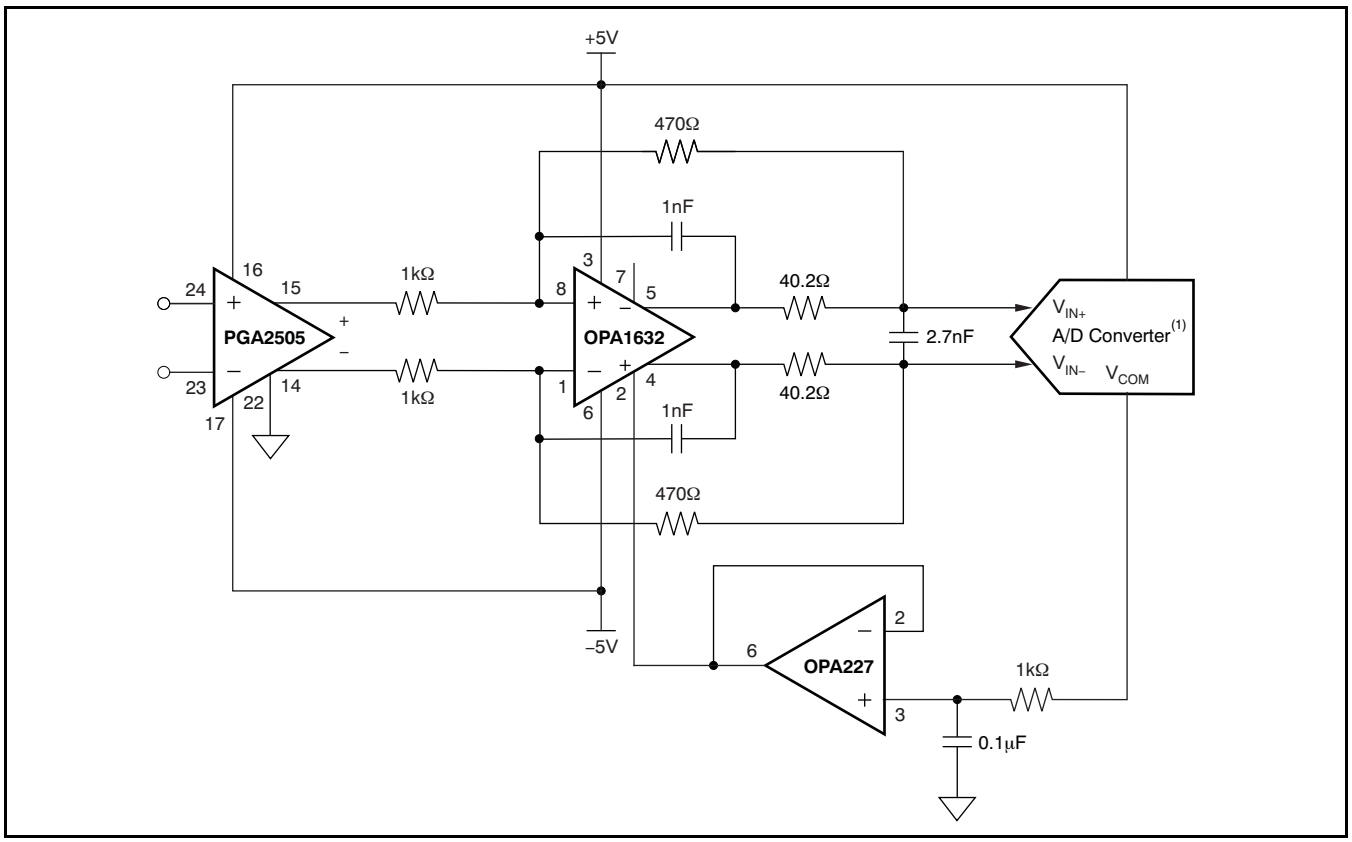
(1) Recommended devices are the PCM1804, PCM4202, PCM4204, PCM4220, or PCM4222.

Figure 15. PGA2505 Analog Output to ADC Analog Input Interface, AC-Coupled



(1) Recommended devices are the PCM1804, PCM4202, PCM4204, PCM4220, or PCM4222.

Figure 16. PGA2505 Analog Output to ADC Analog Input Interface, DC-Coupled



(1) Recommended devices are the PCM1804, PCM4202, PCM4204, PCM4220, or PCM4222.

Figure 17. PGA2505 Using OPA1632 as an Output Buffer

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (May, 2009) to Revision B	Page
• Changed logo on document	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA2505IDB	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2505I	Samples
PGA2505IDBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PGA2505I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

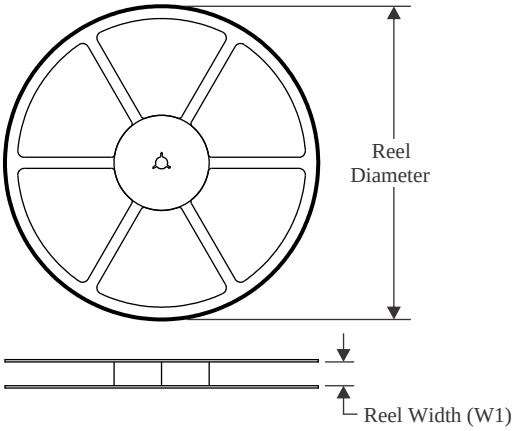
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

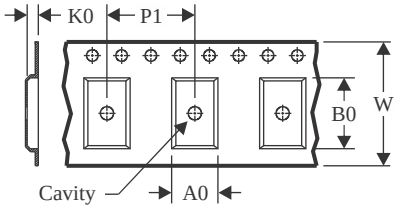
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

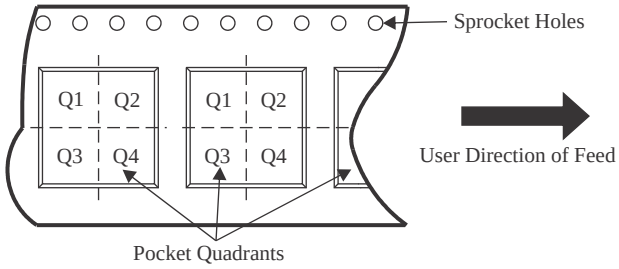


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

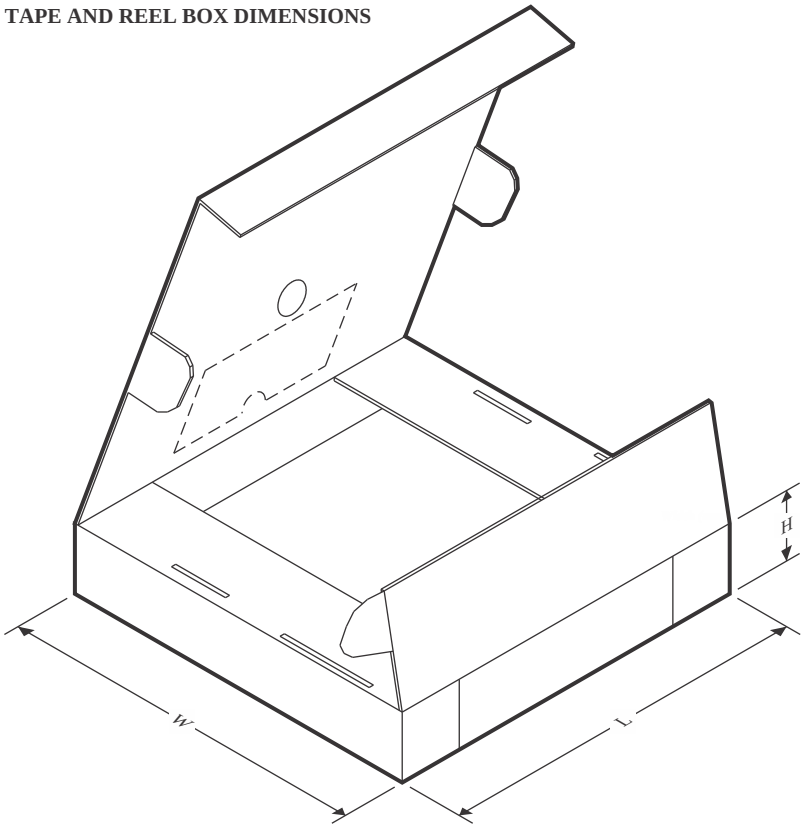
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PGA2505IDBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

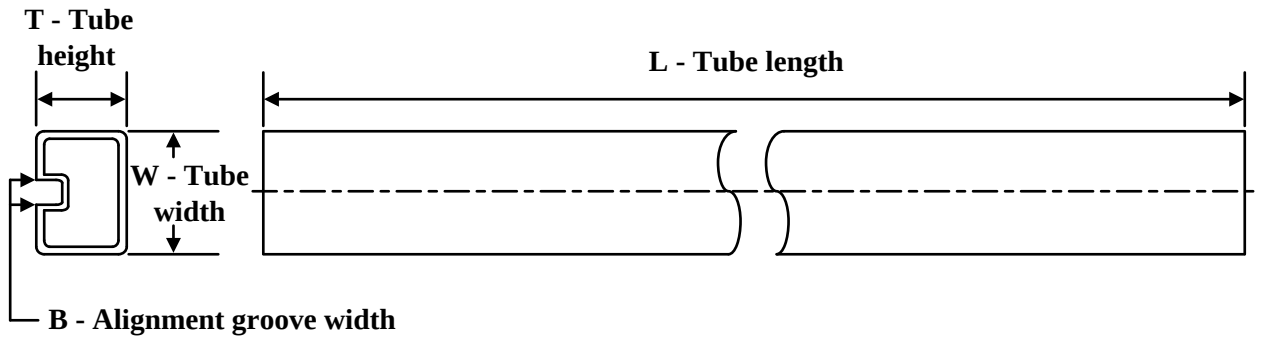
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PGA2505IDBR	SSOP	DB	24	2000	356.0	356.0	35.0

TUBE



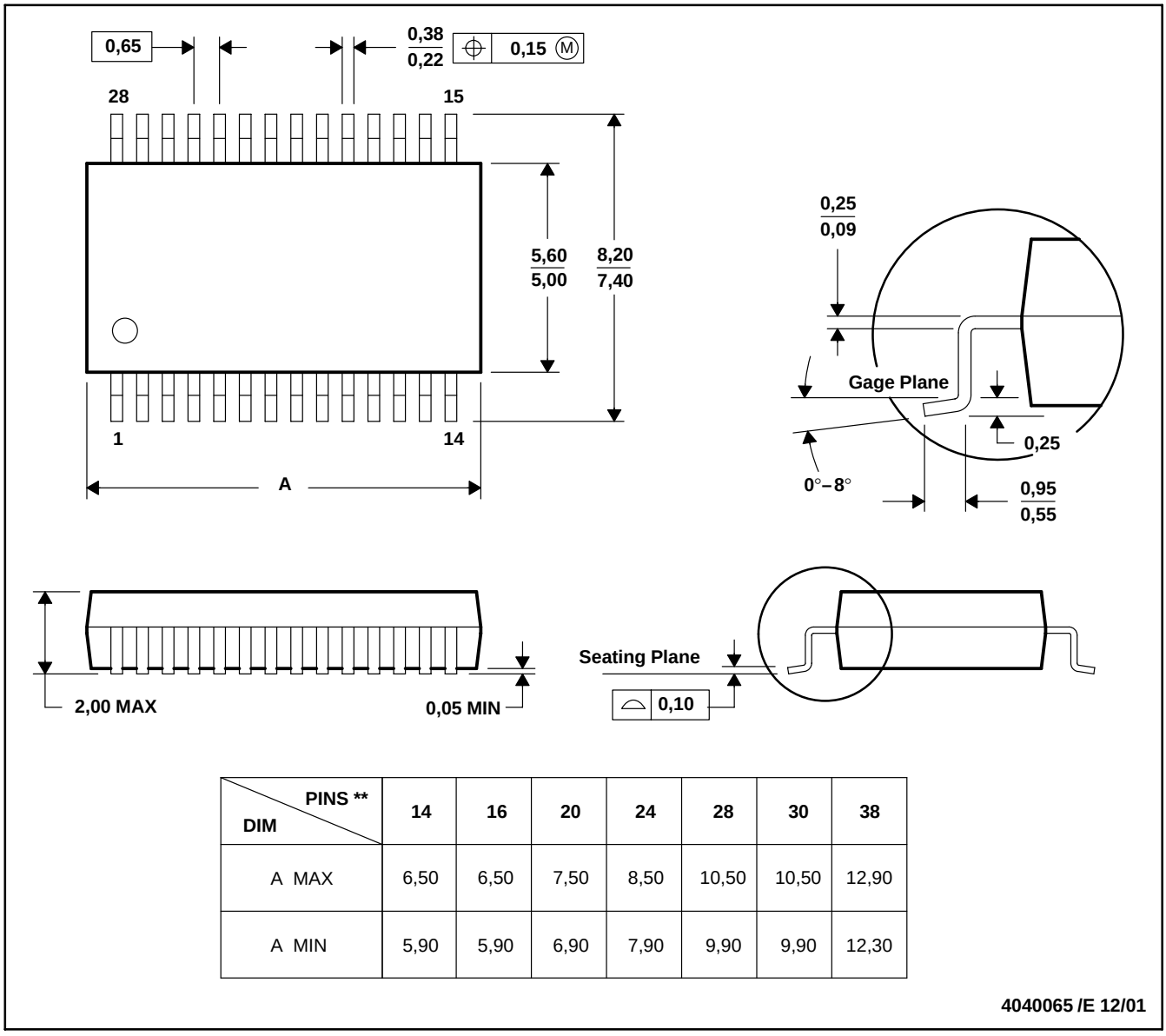
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PGA2505IDB	DB	SSOP	24	60	530	10.5	4000	4.1

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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