

# PGA849 Low-Noise, Wide-Bandwidth, Precision Programmable Gain Instrumentation Amplifier

## 1 Features

- Differential to single-ended conversion
- Eight pin-programmable binary gains
  - $G (V/V) = \frac{1}{8}, \frac{1}{4}, \frac{1}{2}, 1, 2, 4, 8,$  and  $16$
- Low gain error drift:  $2\text{ppm}/^\circ\text{C}$  (max)
- Faster signal processing:
  - Wide bandwidth:  $10\text{MHz}$  at all gains
  - High slew rate:  $35\text{V}/\mu\text{s}$
  - Settling time:
    - 500ns to 0.01%, 950ns to 0.0015%
  - Input stage noise:  $7.8\text{nV}/\sqrt{\text{Hz}}$  at  $G = 16\text{V/V}$
  - Filter option to achieve better SNR
- Input overvoltage protection to  $\pm 40\text{V}$  beyond supplies
- Input-stage supply range:
  - Single supply:  $8\text{V}$  to  $36\text{V}$
  - Dual supply:  $\pm 4\text{V}$  to  $\pm 18\text{V}$
- Independent output power-supply pins
- Output-stage supply range:
  - Single supply:  $4.5\text{V}$  to  $36\text{V}$
  - Dual supply:  $\pm 2.25\text{V}$  to  $\pm 18\text{V}$
- Specified temperature range:  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$
- Small package:  $3\text{mm} \times 3\text{mm}$  QFN

## 2 Applications

- [Factory automation and control](#)
- [Analog input module](#)
- [Data acquisition \(DAQ\)](#)
- [Test and measurement](#)
- [Semiconductor test](#)

## 3 Description

The PGA849 is a wide-bandwidth, low-noise programmable gain instrumentation amplifier for differential-to-single-ended conversion. The PGA849 is equipped with eight binary gain settings, from an attenuating gain of  $0.125\text{V/V}$  to a maximum of  $16\text{V/V}$ , using three digital gain selection pins.

The PGA849 architecture is optimized to drive inputs of high-resolution, precision analog-to-digital converters (ADCs) with sampling rates up to  $1\text{MSPS}$  without the need for an additional ADC driver. The output-stage power supplies are decoupled from the input stage to protect the ADC or downstream device against overdrive damage.

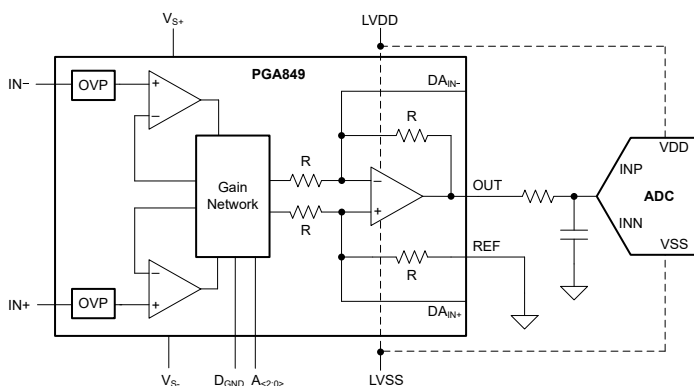
The super-beta input transistors offer an impressively low input bias current, which in turn provides a very low input current noise density of  $0.3\text{pA}/\sqrt{\text{Hz}}$ , making the PGA849 a versatile choice for virtually any sensor type. The low-noise current-feedback front-end architecture offers exceptional gain flatness even at high frequencies, making the PGA849 an excellent high-impedance sensor readout device. Integrated protection circuitry on the input pins handles overvoltages of up to  $\pm 40\text{V}$  beyond the power-supply voltages.

### Package Information

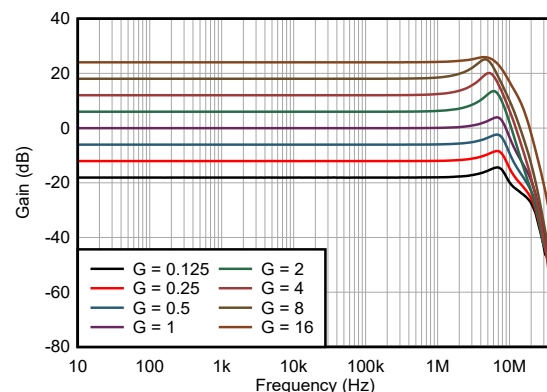
PART NUMBER	PACKAGE <sup>(1)</sup>	PACKAGE SIZE <sup>(2)</sup>
PGA849	RGT (VQFN, 16)	$3\text{mm} \times 3\text{mm}$

(1) For more information, see [Section 11](#).

(2) The package size (length  $\times$  width) is a nominal value and includes pins, where applicable.



**PGA849 Simplified Application**



**Gain vs Frequency**



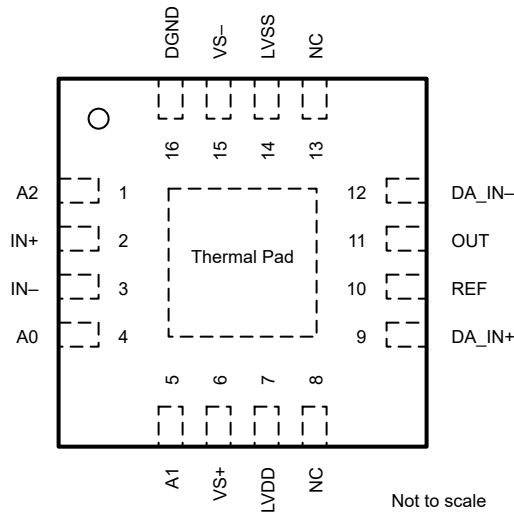
## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>12</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Application Information.....	12
<b>3 Description</b> .....	<b>1</b>	8.2 Typical Applications.....	12
<b>4 Device Comparison Table</b> .....	<b>2</b>	8.3 Power Supply Recommendations.....	15
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	8.4 Layout.....	15
<b>6 Specifications</b> .....	<b>4</b>	<b>9 Device and Documentation Support</b> .....	<b>17</b>
6.1 Absolute Maximum Ratings.....	4	9.1 Device Support.....	17
6.2 ESD Ratings.....	4	9.2 Documentation Support.....	17
6.3 Recommended Operating Conditions.....	4	9.3 Receiving Notification of Documentation Updates....	17
6.4 Thermal Information.....	4	9.4 Support Resources.....	17
6.5 Electrical Characteristics.....	5	9.5 Trademarks.....	17
<b>7 Detailed Description</b> .....	<b>8</b>	9.6 Electrostatic Discharge Caution.....	18
7.1 Overview.....	8	9.7 Glossary.....	18
7.2 Functional Block Diagram.....	8	<b>10 Revision History</b> .....	<b>18</b>
7.3 Feature Description.....	9	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>18</b>
7.4 Device Functional Modes.....	11		

## 4 Device Comparison Table

DEVICE	DESCRIPTION	GAIN EQUATION	RG PINS AT PIN
PGA855	Low-noise, wide-bandwidth, fully-differential-output programmable-gain instrumentation amplifier	Digitally pin-programmable	N/A
INA849	Ultra-low-noise (1nV/√Hz), high-bandwidth instrumentation amplifier	$G = 1 + 6k\Omega / RG$	2, 3
INA851	Low-noise (3.2nV/√Hz), high-speed (22MHz), fully-differential instrumentation amp with overvoltage protection (±40V)	$G = 1 + 6k\Omega / RG$	2, 3
PGA280	20mV to ±10V programmable gain instrumentation amplifier with 3V or 5V differential output; analog supply up to ±18V	Digitally programmable with SPI	N/A
PGA281	Zero-drift, high-voltage programmable gain amplifier	Digitally pin-programmable	N/A

## 5 Pin Configuration and Functions



**Figure 5-1. RGT Package, 16-Pin VQFN (Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NAME	NO.		
A0	4	Input	Gain option pin 0
A1	5	Input	Gain option pin 1
A2	1	Input	Gain option pin 2
DA_IN+	9	Input	Connection to output difference amplifier summing node
DA_IN-	12	Input	Connection to output difference amplifier summing node
DGND	16	Power	Ground reference for digital-logic and gain-setting pins
IN-	3	Input	Negative (inverting) input
IN+	2	Input	Positive (noninverting) input
LVDD	7	Power	Output-driver positive supply
LVSS	14	Power	Output-driver negative supply
NC	8	—	Do not connect
NC	13	—	Do not connect
OUT	11	Output	Output
REF	10	Input	Reference input. This pin must be driven by a low-impedance source
VS+	6	Power	Input-stage positive supply
VS-	15	Power	Input-stage negative supply
Thermal Pad	Thermal pad	—	The thermal pad must be soldered to the printed-circuit board (PCB). Connect thermal pad to a plane or large copper pour that is either floating or electrically connected to VS-, even for applications that have low power dissipation.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>S</sub>	Supply voltage on V <sub>S+</sub> , V <sub>S-</sub> pins; V <sub>S</sub> = (V <sub>S+</sub> ) – (V <sub>S-</sub> )	0	40	V
V <sub>SOUT</sub>	Supply voltage on LVDD, LVSS pins; V <sub>SOUT</sub> = V <sub>LVDD</sub> – V <sub>LVSS</sub>	0	40	V
	Voltage on power pins LVDD, LVSS	(V <sub>S-</sub> ) – 0.5	(V <sub>S+</sub> ) + 0.5	V
V <sub>IN</sub>	Voltage on signal-input pins IN+, IN–	(V <sub>S-</sub> ) – 40	(V <sub>S+</sub> ) + 40	V
	DGND, DA_IN+, DA_IN– pin voltage	(V <sub>S-</sub> ) – 0.5	(V <sub>S+</sub> ) + 0.5	V
	Voltage on gain-select pins A2, A1, A0	V <sub>DGND</sub> – 0.5	(V <sub>S+</sub> ) + 0.5	V
V <sub>O</sub>	Signal output pin maximum voltage	V <sub>LVSS</sub> – 0.5	V <sub>LVDD</sub> + 0.5	V
V <sub>REF</sub>	Reference input voltage	V <sub>LVSS</sub> – 0.5	V <sub>LVDD</sub> + 0.5	V
I <sub>O</sub>	Signal-output pins current	–100	100	mA
I <sub>SC</sub>	Output short-circuit current <sup>(2)</sup>	Continuous		
T <sub>A</sub>	Operating temperature	–50	150	°C

- Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- Short-circuit to V<sub>SOUT</sub> / 2.

### 6.2 ESD Ratings

			VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup>	±1000	

- JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>S</sub>	Input stage supply voltage	Single supply	8	36	V
		Dual supply	±4	±18	
V <sub>SOUT</sub>	Output stage supply voltage	Single supply	4.5	36	V
		Dual supply	±2.25	±18	
T <sub>A</sub>	Specified temperature		–40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		PGA849	UNIT
		RGT (VQFN)	
		16 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	47.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	53.6	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	22.0	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	22.0	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	7.8	°C/W

- For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = 0\text{V}$ ,  $V_{REF} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>INPUT</b>							
$V_{OS}$	Offset voltage (input referred)	G = 1 to 16			±50	±350	μV
		G < 1			±50/G	±350/G	
	Offset voltage drift (input referred)	G = 1 to 16, $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$			±0.2	±1.0	μV/°C
		G < 1, $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$			±0.2/G	±1.0/G	
PSRR	Power-supply rejection ratio	$\pm 4\text{V} \leq V_S \leq \pm 18\text{V}$ , RTI	G = 0.125	95	110	dB	
			G = 0.25	98	114		
			G = 0.5	100	118		
			G = 1	120	134		
			G = 2	120	126		
			G = 4	120	132		
			G = 8	120	136		
			G = 16	120	140		
$Z_{id}$	Differential input impedance			1    1		GΩ    pF	
$Z_{ic}$	Common-mode input impedance			1    7		GΩ    pF	
$V_{ICM}$	Common-mode input voltage	$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$		$(V_{S-}) + 2.5$		$(V_{S+}) - 2$	V
		$V_S = \pm 4\text{V}$ to $\pm 18\text{V}$ , $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		$(V_{S-}) + 3$		$(V_{S+}) - 2.5$	
CMRR	Common-mode rejection ratio	At dc to 60Hz, $V_{ICM} = \pm 10\text{V}$ , $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , RTI	G = 0.125	64	82	dB	
			G = 0.25	70	88		
			G = 0.5	76	94		
			G = 1	82	100		
			G = 2	88	106		
			G = 4	94	112		
			G = 8	100	118		
			G = 16	106	124		
<b>BIAS CURRENT</b>							
$I_B$	Input bias current			0.5	1.8	nA	
		$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		1			
	Input bias current drift	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$				10	pA/°C
$I_{OS}$	Input offset current			0.5	1	nA	
		$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		1			
	Input offset current drift	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$				10	pA/°C

## 6.5 Electrical Characteristics (continued)

at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = 0\text{V}$ ,  $V_{REF} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>NOISE VOLTAGE</b>							
$e_{NI}$	Input-referred voltage noise density	$f = 1\text{kHz}$	$G = 16$		7.8		$\text{nV}/\sqrt{\text{Hz}}$
			$G = 8$		8.0		
			$G = 4$		8.6		
			$G = 2$		12.6		
			$G = 1$		21.6		
			$G = 0.5$		42		
			$G = 0.25$		84		
			$G = 0.125$		168		
	Input-referred voltage noise	$f_B = 0.1\text{Hz to } 10\text{Hz}$	$G = 16$		0.26		$\mu\text{V}_{PP}$
			$G = 8$		0.27		
			$G = 4$		0.29		
			$G = 2$		0.44		
			$G = 1$		0.8		
			$G = 0.5$		1.6		
			$G = 0.25$		3.2		
			$G = 0.125$		6.4		
$i_N$	Input current noise density	$f = 1\text{kHz}$			0.3		$\text{pA}/\sqrt{\text{Hz}}$
	Input current noise	$f_B = 0.1\text{Hz to } 10\text{Hz}$			13		$\text{pA}_{PP}$
<b>GAIN</b>							
	Gain range			0.125		16	$\text{V/V}$
GE	Gain error	$G = 0.125, 0.25, 0.5, 2, 4, 8$			$\pm 0.02$	$\pm 0.05$	%
		$G = 1$			$\pm 0.02$	$\pm 0.03$	%
		$G = 16$			$\pm 0.02$	$\pm 0.07$	%
	Gain drift	$G = 0.125\text{ to } 16, T_A = -40\text{ }^\circ\text{C to } +125\text{ }^\circ\text{C}$			$\pm 1$	$\pm 2$	$\text{ppm}/\text{ }^\circ\text{C}$
	Gain nonlinearity	$G = 0.125\text{ to } 16, V_{OUT} > \pm 5\text{V}$			2	5	ppm
<b>OUTPUT</b>							
$V_{OUT}$	Output voltage	No load	$V_{SOUT} = \pm 2.25\text{V}$	$V_{LVSS} + 0.1$		$V_{LVDD} - 0.1$	V
		$R_L = 10\text{k}\Omega$	$V_{SOUT} = \pm 2.25\text{V}$	$V_{LVSS} + 0.2$		$V_{LVDD} - 0.2$	
			$V_{SOUT} = \pm 18\text{V}$	$V_{LVSS} + 0.4$		$V_{LVDD} - 0.4$	
$C_L$	Load capacitance	Stable operation for capacitive load			100		pF
$I_{SC}$	Short-circuit current	Continuous to $V_{SOUT} / 2$				$\pm 45$	mA
			$T_A = -40\text{ }^\circ\text{C to } +125\text{ }^\circ\text{C}$		$\pm 20$		
<b>FREQUENCY RESPONSE</b>							
BW	Bandwidth, $-3\text{dB}$	$G = 0.125\text{ to } 16$			10		MHz
SR	Slew rate	$G \geq 1, V_{OUT} > 5\text{V}$			35		$\text{V}/\mu\text{s}$
		$G < 1, V_{OUT} > 5\text{V}$			12		$\text{V}/\mu\text{s}$
$t_s$	Settling time	$G = 0.125\text{ to } 16$ $V_{INDIFF} = 10\text{V step or } V_{OUT} = 10\text{V step}$	To 0.01%		0.7		$\mu\text{s}$
			To 0.0015%		0.95		
	Gain switching time				2		$\mu\text{s}$
THD+N	Total harmonic distortion and Noise	Differential input, $f = 10\text{kHz}, V_{OUT} = 10\text{V}_{PP}$			$-110$		dB
		Single-ended input, $f = 10\text{kHz}, V_{OUT} = 10\text{V}_{PP}$			$-105$		
HD2	Second-order harmonic distortion	Differential input, $f = 10\text{kHz}, V_{OUT} = 10\text{V}_{PP}$			$-120$		
		Single-ended input, $f = 10\text{kHz}, V_{OUT} = 10\text{V}_{PP}$			$-110$		
HD3	Third-order harmonic distortion	Differential input, $f = 10\text{kHz}, V_{OUT} = 10\text{V}_{PP}$			$-120$		
		Single-ended input, $f = 10\text{kHz}, V_{OUT} = 10\text{V}_{PP}$			$-110$		

## 6.5 Electrical Characteristics (continued)

at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_S = V_{SOUT} = \pm 15\text{V}$ ,  $V_{ICM} = 0\text{V}$ ,  $V_{REF} = 0\text{V}$ ,  $R_L = 10\text{k}\Omega$  connected to ground, and  $G = 1\text{V/V}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>REFERENCE INPUT</b>						
$R_{IN}$	Reference input impedance			10		k $\Omega$
	Reference input current	$V_{IN} = 0\text{V}$		140		$\mu\text{A}$
	Reference input voltage		$V_{LVSS}$		$V_{LVDD}$	V
	Reference gain to output			1		V/V
	Reference gain error	$V_{OUT} = \pm 10\text{V}$ , inside the voltage swing range		0.01	0.05	%
<b>INPUT STAGE POWER SUPPLY</b>						
$I_{Q\_input}$	Input stage quiescent current $V_{S+}$ , $V_{S-}$	$V_{IN} = 0\text{V}$		3		mA
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$			4.2	
<b>OUTPUT STAGE POWER SUPPLY</b>						
$I_{Q\_output}$	Output stage quiescent current LVDD, LVSS	$V_{IN} = 0\text{V}$ , $V_{REF} = 0\text{V}$		1.3		mA
		$T_A = -40^\circ\text{C}$ to $125^\circ\text{C}$		1.5	1.9	
<b>DIGITAL LOGIC</b>						
$V_{IL}$	Digital input logic low	A0, A1, A2 pins, referred to DGND	$V_{DGND}$		$V_{DGND} + 0.8$	V
$V_{IH}$	Digital input logic high	A0, A1, A2 pins, referred to DGND	$V_{DGND} + 1.8$		$V_{S+}$	V
	Digital input pin current	A0, A1, A2 pins		1.5	3	$\mu\text{A}$
$V_{DGND}$	DGND voltage		$V_{S-}$		$(V_{S+}) - 4$	V
	DGND reference current			4	10	$\mu\text{A}$

## 7 Detailed Description

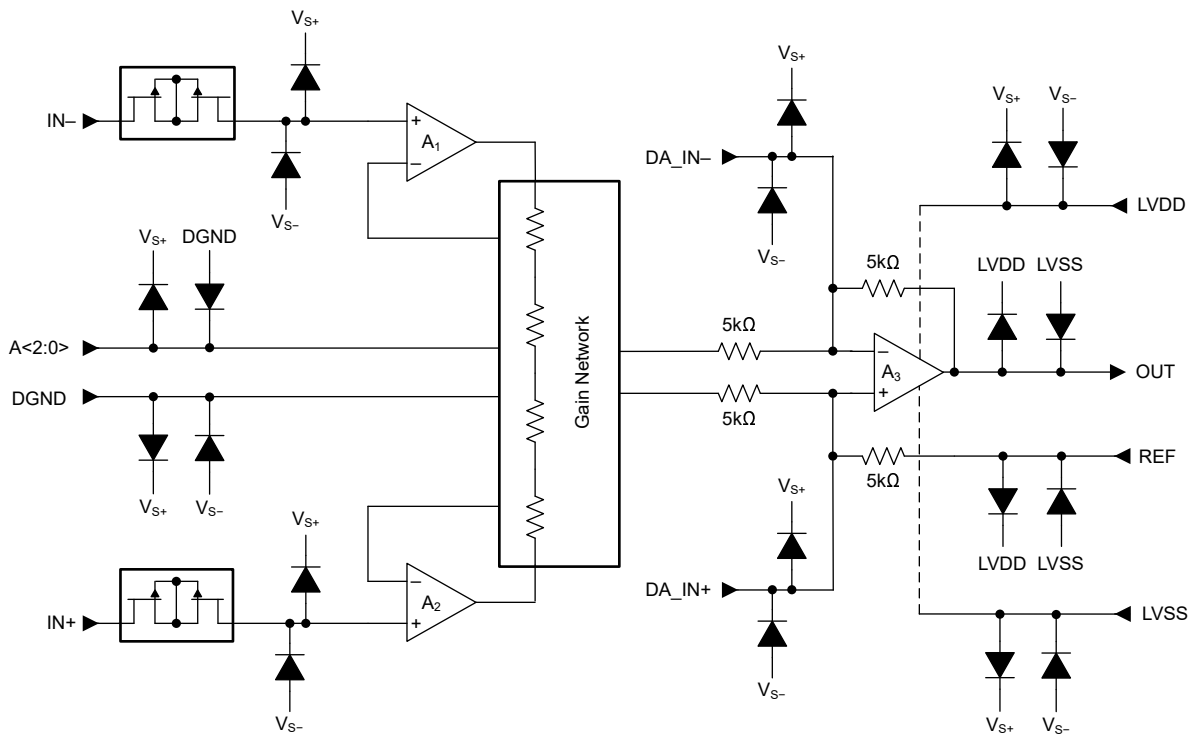
### 7.1 Overview

The PGA849 is a monolithic, high-voltage, precision programmable-gain instrumentation amplifier. The PGA849 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, difference amplifier output stage. Eight preprogrammed binary gains, ranging from 0.125V/V to 16V/V are selectable using gain-select pins A0, A1, and A2.

A functional block diagram for PGA849 is shown in the next section. The differential input voltage is fed into a pair of matched, high-impedance input, current-feedback amplifiers. An integrated precision-matched gain resistor network is used to amplify the differential input voltage. An output difference amplifier, A<sub>3</sub>, rejects the input common-mode component and refers the output signal to the voltage level set by the REF pin.

The PGA849 output amplifier bandwidth is optimized to drive high-performance analog-to-digital converters (ADCs) with sampling rates up to 1MSPS, without the need for an additional ADC driver. The output amplifier uses a separate power supply that is independent of the input-stage power supply. When driving an ADC, use a low-impedance connection from LVDD and LVSS to the ADC power supplies. This configuration protects the ADC inputs from damage due to inadvertent overvoltage conditions.

### 7.2 Functional Block Diagram

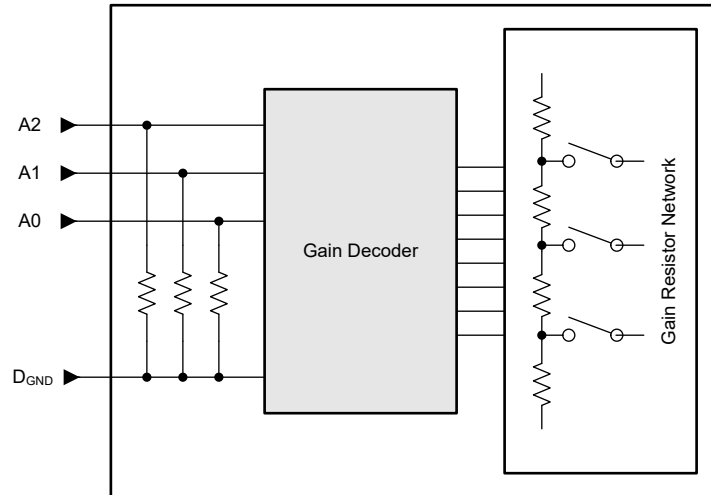




## 7.3 Feature Description

### 7.3.1 Gain Control

The PGA849 uses three pins to set the amplifier gain. These gain select pins are set with respect to DGND. This configuration simplifies design when compared to programmable-gain amplifiers requiring an SPI or other digital interface options for gain changes. [Figure 7-1](#) shows the gain-setting block diagram. [Table 7-1](#) lists the gain options. Any gain select pin that is not driven by an external source is automatically biased at DGND using internal pulldown options.



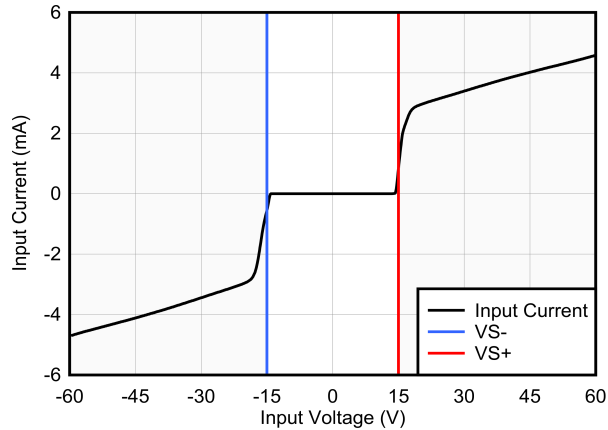
**Figure 7-1. PGA849 Gain Setting Block Diagram**

**Table 7-1. Gain Options**

A2:A0	GAIN
000	0.125
001	0.25
010	0.5
011	1
100	2
101	4
110	8
111	16

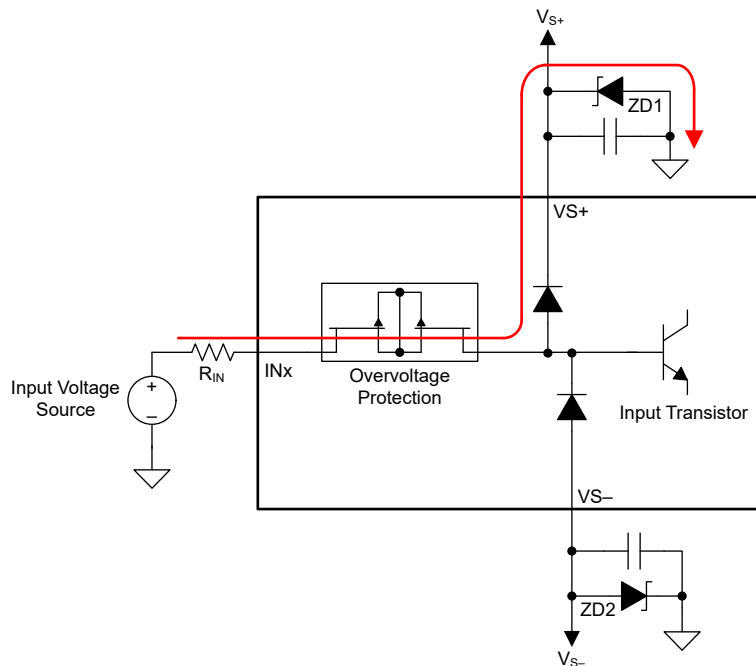
### 7.3.2 Input Protection

The inputs of the PGA849 are individually protected for voltages up to  $\pm 40\text{V}$  beyond either supply. For example, an input common-mode voltage anywhere between  $-55\text{V}$  and  $+55\text{V}$  does not cause damage when powered from  $\pm 15\text{V}$  supplies. Internal circuitry on each input provides low series impedance under normal signal conditions, thus maintaining high performance under normal operating conditions. If the input is overloaded, the protection circuitry limits the input current to a value of approximately  $4.8\text{mA}$ . Figure 7-2 shows the input protection functionality during an overvoltage condition.



**Figure 7-2. Input Current vs Input Overvoltage**

Figure 7-3 shows that during an input overvoltage condition, current flows through the input protection diodes into the power supplies. In applications where the power supplies are unable to sink current, place Zener diode clamps (ZD1 and ZD2) on the power supplies to provide a current pathway to ground.



**Figure 7-3. Input Current Path During an Overvoltage Condition**

### 7.3.3 Using the Output Difference Amplifier to Shape Noise

Section 7.2 shows that the PGA849 output-stage difference amplifier uses a 5k $\Omega$  feedback resistor between the output and the inverting input. External direct access to the inverting and noninverting inputs of the difference amplifier is provided through the DA\_IN– and DA\_IN+ pins, respectively. This option allows circuit designers to add external capacitors in parallel with the internal resistors to implement noise-filtering or noise-shaping techniques. These pins are also used to implement customized attenuating gains for the output stage. Consider the following important factors when designing parallel circuits with the internal resistors:

- The accuracy of the internal resistor network is 0.01% or better. This accuracy results in a common-mode rejection (CMRR) of 80dB or better. Mismatched leakage currents on these pins can cause CMRR degradation.
- The internal resistors have  $\pm 15\%$  absolute resistance variation and must be considered when implementing custom attenuating gains or noise filters.

**CAUTION**

Do not treat these pins as outputs, nor use the pins to source or sink current. Excessive currents through the feedback resistors can cause permanent damage to internal circuitry.

### 7.4 Device Functional Modes

The PGA849 has a single functional mode and operates when the input-stage power supply is greater than  $\pm 4V$  (8V) and the output-stage power supply is greater than  $\pm 2.25V$  (4.5V); see also Section 6.3.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 8.1 Application Information

The PGA849 is a monolithic, high-voltage, high-bandwidth, precision programmable gain instrumentation amplifier with a single-ended output. The PGA849 combines a high-speed current-feedback input stage with an internally matched gain resistor network, followed by a four-resistor, differential amplifier output stage. The PGA849 is equipped with eight binary-gain settings, from 0.125V/V to 16V/V, using three digital gain-selection pins: A0, A1, and A2.

The PGA849 is designed to work with applications such as factory automation and control, analog input modules, data acquisition, test and measurement, and semiconductor test.

### 8.2 Typical Applications

#### 8.2.1 ADS8860 16-Bit, 1MSPS, Single-Ended Input, SAR ADC Driver

Figure 8-1 shows the schematic for the 16-bit, precision, 1MSPS, successive approximation register (SAR), analog-to-digital converter (ADC). This circuit is used to measure the driving capability of the PGA849 with the ADS8860 single-ended input ADC.

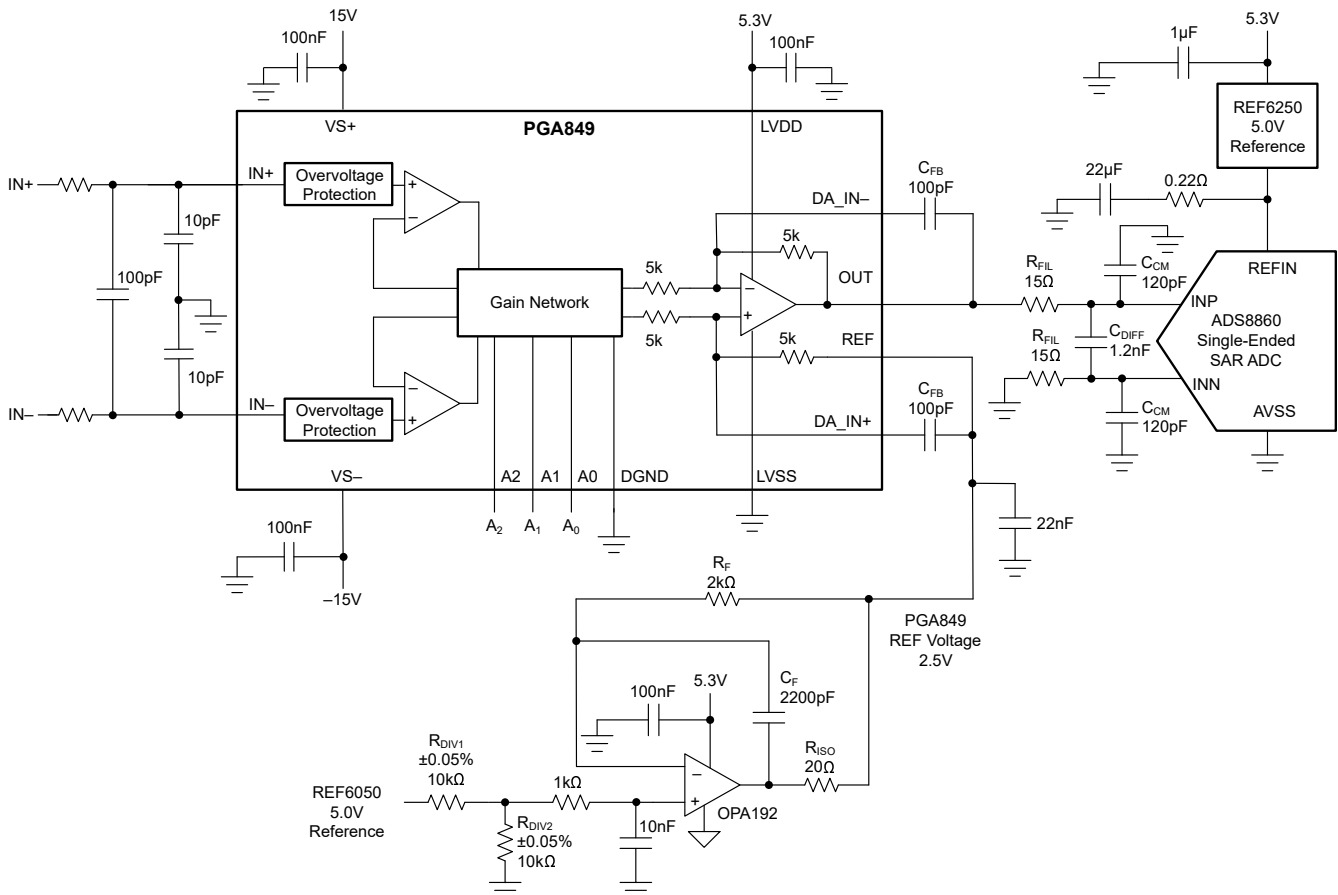


Figure 8-1. Driving the ADS8860 SAR ADC

The circuit accepts single-ended or differential input signals. The PGA849 operates with independent input and output power supplies. In this example,  $\pm 15V$  power supplies are used to power the input-stage, and a unipolar 5.3V supply powers the output-stage. The PGA849 output stage supply is powered by the same 5.3V ADC supply. The 5.3V output supply operation prevents overloading the ADC inputs during PGA overdrive conditions. The [REF6250](#) is selected as the ADC voltage reference. The REF6250 is a low-noise, low-drift, precision, 5V reference connected to the ADS8860 reference input ADC REFIN pin.

The PGA849 output voltage is developed with respect to the REF pin. The REF pin is set to the SAR ADC midscale voltage by dividing the REF6250 ADC reference with a precision resistive voltage divider. The [OPA192](#) buffer drives the PGA849 REF pin. The OPA192 is a precision amplifier with low offset, low drift and 10MHz bandwidth.

### 8.2.1.1 Design Requirements

The design requirements for the application driving the ADS8860 ADC are listed in the following table.

**Table 8-1. Design Parameters**

PARAMETER	VALUE
Supply voltages	$VS_{\pm} = \pm 15V$ , $LVDD = 5.3V$ , $LVSS = GND$ , $ADC\ REFIN = 5V$ , $PGA\ REF = 2.5V$
Full-scale range of ADC	$FSR = 5V$
Sampling rate of ADC	$f_{SAMPLE} = 1MSPS$
PGA gain	0.125, 0.25, 0.5, 1, 2, 4, 8, 16
Input voltages ( $V_{PP}$ , differential)	25V, 16V, 8V, 4V, 2V, 1V, 0.5V, 0.25V
Signal frequency	1kHz
RC kickback filter	$R_{FIL} = 15\Omega$ , $C_{DIFF} = 1.2nF$ , $C_{CM} = 120pF$

### 8.2.1.2 Detailed Design Procedure

The first filter located at the input of the PGA (see [Figure 8-1](#)) helps reduce electromagnetic interference (EMI) and radio frequency interference (RFI), high-frequency, extrinsic noise. This filter can be customized per the application bandwidth and antialiasing requirements.

The second filter is provided by  $C_{FB}$  in parallel with the PGA 5k $\Omega$  feedback resistors. The PGA resistors are  $\pm 15\%$  absolute tolerance, as such, consider the effect of the tolerance on the filter cutoff frequency.  $C_{FB} = 100\text{pF}$  results in a filter cutoff frequency of 318kHz. On the high side of the resistor tolerance, the filter frequency changes to 277kHz. The device allows for the flexibility to modify the  $C_{FB}$  capacitor value to adjust bandwidth, with a trade-off on the broadband noise of the circuit.

The third filter placed at the ADS8860 inputs works as a charge reservoir filter to drive the SAR. The charge kickback filter reduces the instantaneous charge demand of the amplifier, maintaining low distortion that otherwise can degrade because of incomplete ADC sample-and-hold settling. The RC filter combination ( $R_{FIL}$ ,  $C_{DIFF}$ ) is tuned for ADC sample-and-hold settling and total harmonic distortion (THD) performance, while maintaining stability of the PGA. High-grade C0G capacitors are used everywhere in the signal path for the low distortion properties.

The PGA849 front-end, accounting for all three filters, provides a nominal  $f_{-3dB}$  bandwidth of 310kHz. On the high side of the internal 5k $\Omega$  feedback resistor tolerance, the PGA849  $f_{-3dB}$  bandwidth changes to 271kHz and the circuit maintains  $-0.1\text{dB}$  flatness to 41kHz.

The ADS8860 requires a full-scale input in the range of 0V to the 5V ADC reference. The PGA849 REF pin is set to a nominal voltage of 2.5V to shift the signal to the ADC midscale voltage.

The PGA849 REF voltage is generated by feeding the REF6250 5V reference through a 10k $\Omega$ -to-10k $\Omega$  precision voltage divider implemented with  $\pm 0.05\%$  tolerance, low-drift  $\pm 5\text{ppm}/^\circ\text{C}$  resistors. Drive the PGA849 REF pin with a low-impedance source, and use the OPA192 as a buffer to drive the REF pin.

The OPA192 buffer is configured in a dual-feedback configuration to provide stability while driving the REF pin and 22nF bypass capacitor.  $R_{ISO}$  is a 20 $\Omega$  isolation resistor that provides separation of two feedback paths for optimized stability. Feedback path number one is through feedback resistor,  $R_F = 2\text{k}\Omega$ , connected directly to the REF pin. Feedback path number two is through feedback capacitor  $C_F = 2\text{nF}$  connected to the output of the op amp. The circuit provides a loop gain phase margin of  $86^\circ$ . The noninverting input of the OPA192 buffer has a low-pass filter with  $R = 1\text{k}\Omega$ ,  $C = 10\text{nF}$  to reduce the resistive divider thermal noise. Using any other load capacitance requires recalculation of the stability components:  $R_F$ ,  $C_F$ , and  $R_{ISO}$ . If modifying the REF bypass capacitance, verify the circuit is stable with simulation using the OPA192 TINA-TI™ SPICE model, and confirm the circuit provides more than  $60^\circ$  of phase margin.

## 8.3 Power Supply Recommendations

The nominal performance of the PGA849 is specified with input-stage supply and output-stage supply voltages of  $\pm 15\text{V}$ , and  $V_{\text{ICM}}$  and  $V_{\text{REF}}$  at mid-supply. Within the specified limits, custom input common-mode and output reference voltages can be used without compromising performance; see also [Section 6.3](#).

### CAUTION

To prevent damage to internal circuitry, the output-stage power supplies are clamped to stay within the input-stage supply voltage levels; see also [Section 7.2](#).

## 8.4 Layout

### 8.4.1 Layout Guidelines

Attention to good layout practices is always recommended. For best operational performance of the device, use good PCB layout practices, including:

- To avoid converting common-mode signals into differential signals and thermal electromotive forces (EMFs), make sure that both input paths are symmetrical and well-matched for source impedance and capacitance.
- Noise can propagate into analog circuitry through the power pins of the device and of the circuit as a whole. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR,  $0.1\mu\text{F}$  ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from  $V+$  to ground is applicable for single-supply applications.
- To reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better than in parallel with the noisy trace.
- Leakage on the  $\text{DA\_IN+}$  and  $\text{DA\_IN-}$  pins can cause in a dc offset error in the output voltages. Additionally, excessive parasitic capacitance at these pins can result in decreased phase margin and affect the stability of the output stage. If these pins are not used to implement deliberate capacitive feedback, follow best practices to minimize leakage and parasitic capacitance.
- Follow best practices to minimize leakage and parasitic capacitance, which includes implementing *keep-out* areas in any ground planes that lie immediately below the input pins.
- Minimize the number of thermal junctions. If possible, route the signal path using a single layer without vias.
- Keep sufficient distance from major thermal energy sources (circuits with high power dissipation). If not possible, place the device so that the effects of the thermal energy source on the high and low sides of the differential signal path are evenly matched.
- Keep the traces as short as possible.

### 8.4.2 Layout Example

ADVANCE INFORMATION

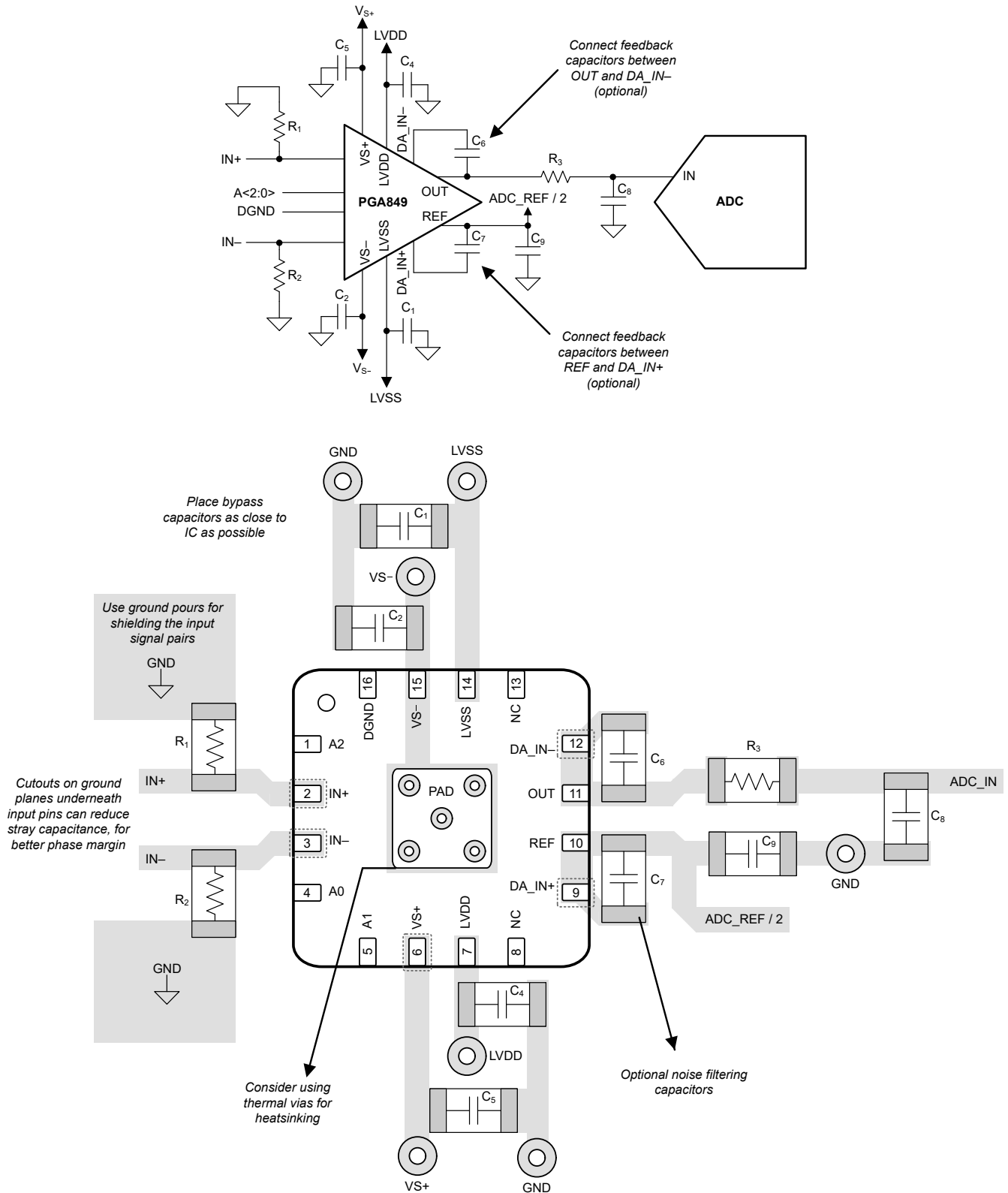


Figure 8-2. Example Schematic and Associated PCB Layout



## 9 Device and Documentation Support

### 9.1 Device Support

#### 9.1.1 Development Support

##### 9.1.1.1 PSpice® for TI

PSpice® for TI is a design and simulation environment that helps evaluate performance of analog circuits. Create subsystem designs and prototype solutions before committing to layout and fabrication, reducing development cost and time to market.

##### 9.1.1.2 TINA-TI™ Simulation Software (Free Download)

TINA-TI™ simulation software is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI simulation software is a free, fully-functional version of the TINA™ software, preloaded with a library of macromodels, in addition to a range of both passive and active models. TINA-TI simulation software provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the [Design tools and simulation](#) web page, TINA-TI simulation software offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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#### Note

These files require that either the TINA software or TINA-TI software be installed. Download the free TINA-TI simulation software from the [TINA-TI™ software folder](#).

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### 9.2 Documentation Support

#### 9.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Comprehensive Error Calculation for Instrumentation Amplifiers application note](#)
- Texas Instruments, [Importance of Input Bias Current Return Paths in Instrumentation Amplifier Applications application note](#)

#### 9.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 9.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

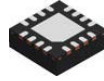
## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
March 2024	*	Initial release

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

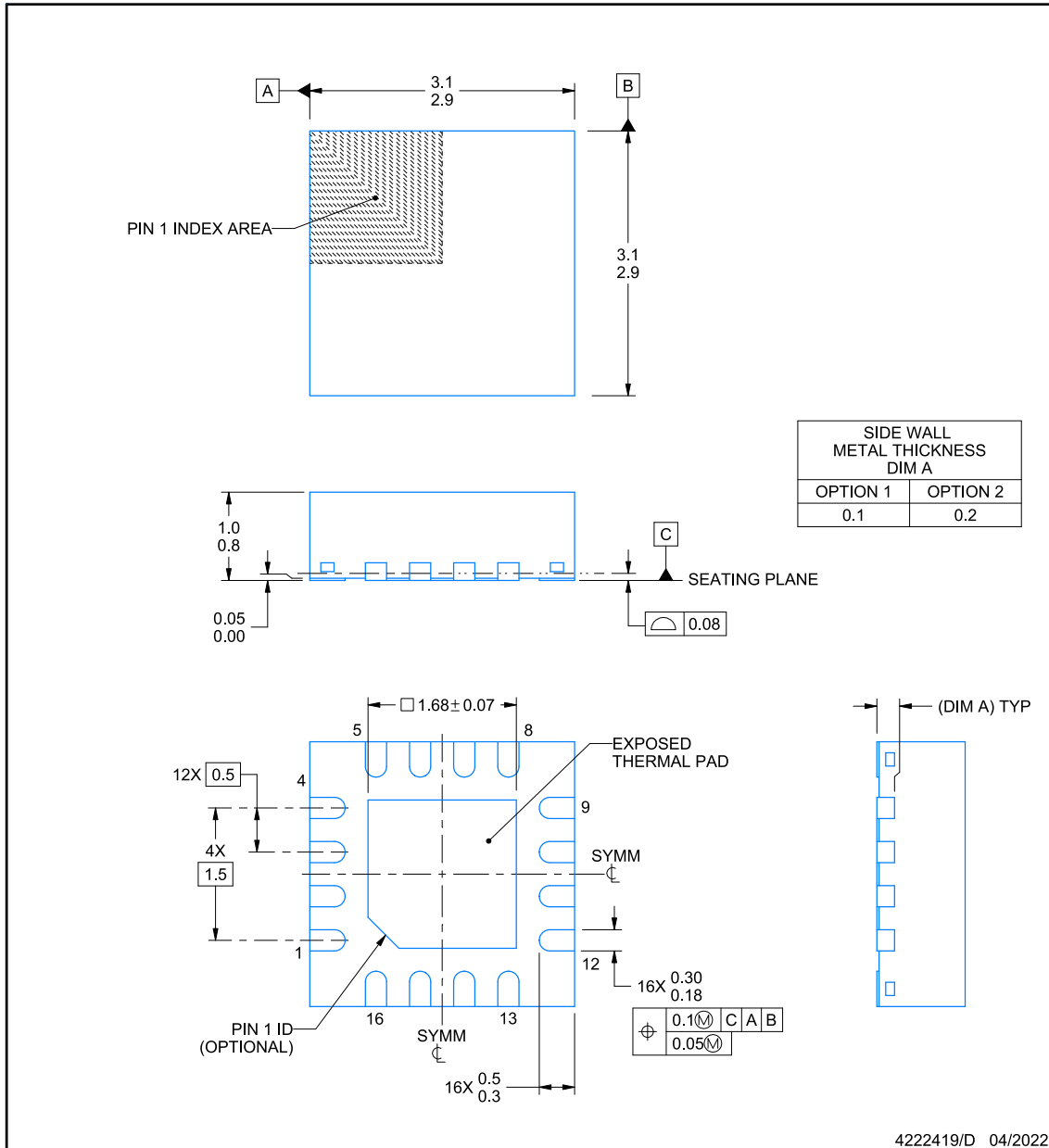


**RGT0016C**

**PACKAGE OUTLINE**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

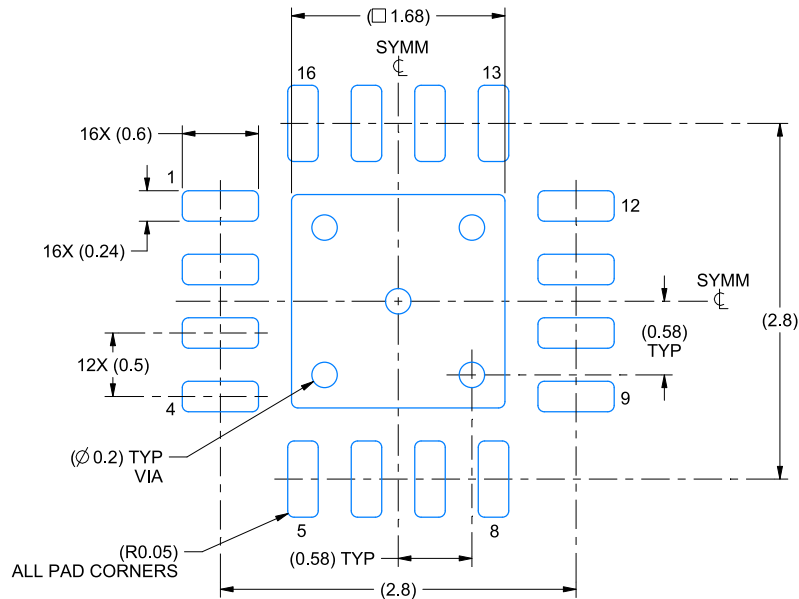
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## EXAMPLE BOARD LAYOUT

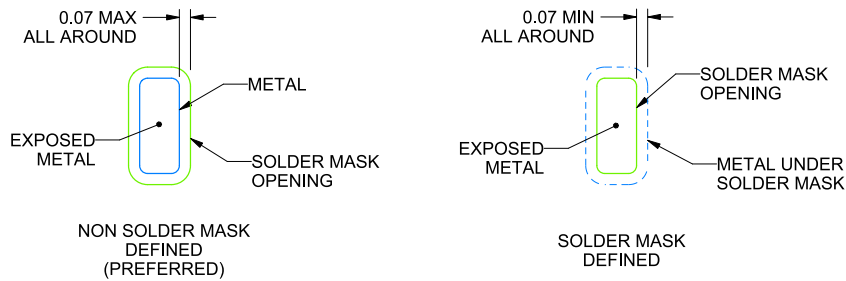
**RGT0016C**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:20X



**SOLDER MASK DETAILS**

4222419/D 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

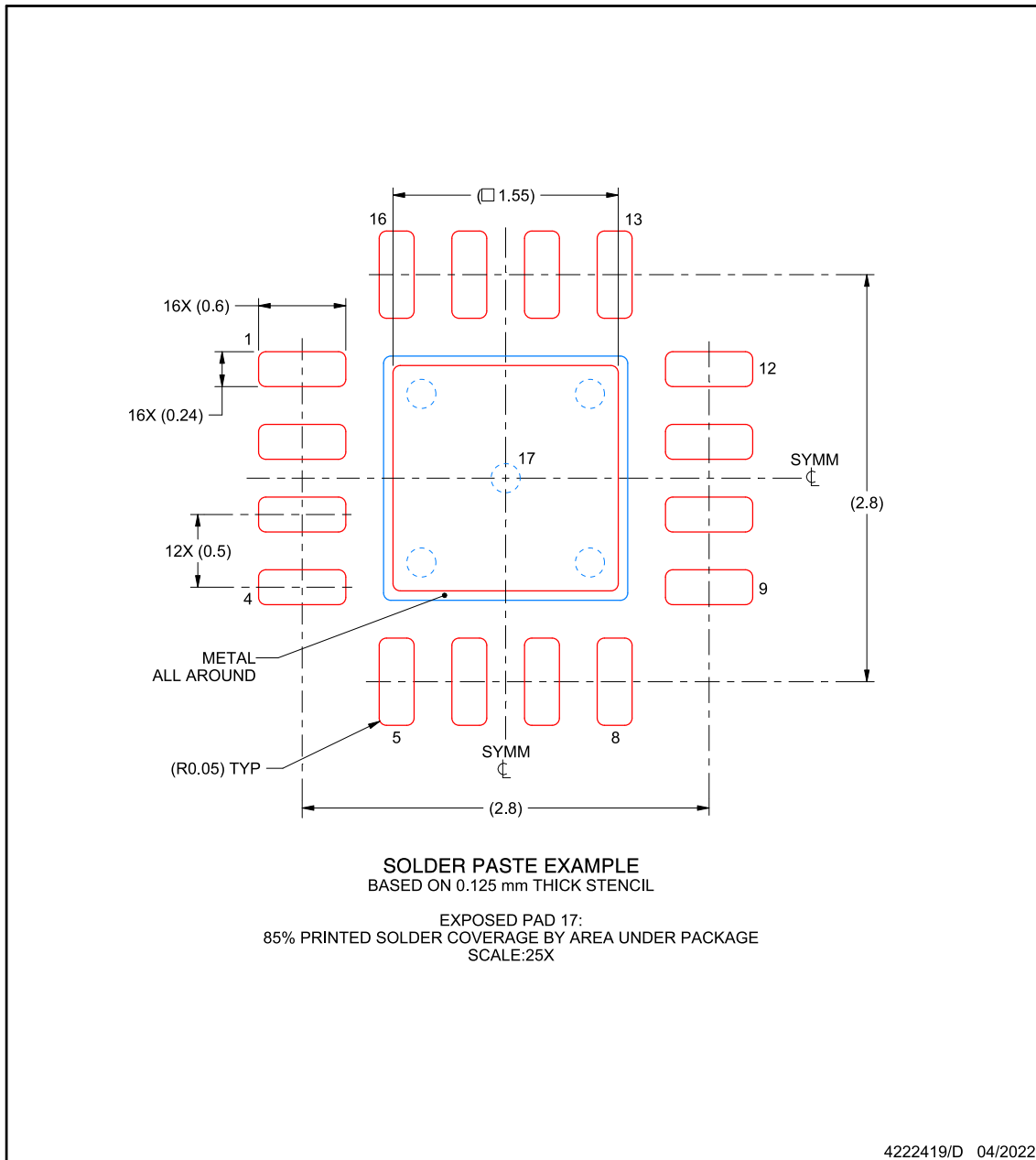
**ADVANCE INFORMATION**

**EXAMPLE STENCIL DESIGN**

**RGT0016C**

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

**ADVANCE INFORMATION**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XPGA849RGTR	ACTIVE	VQFN	RGT	16	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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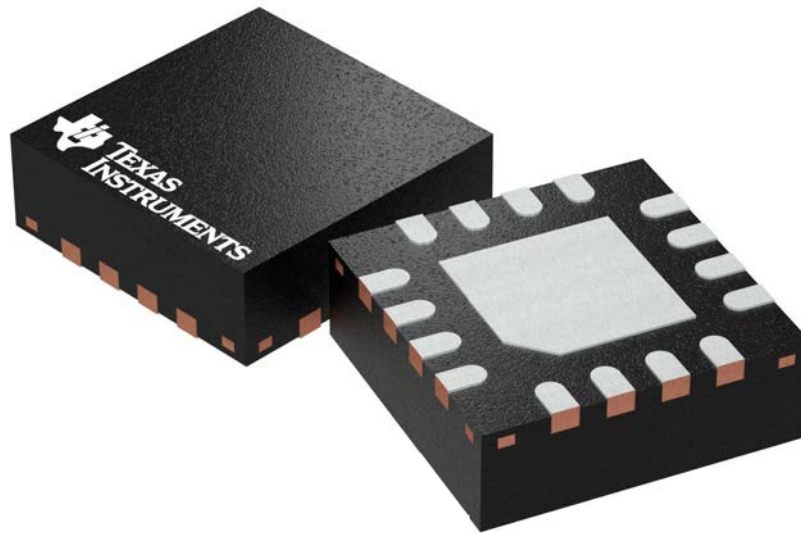
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**RGT 16**

**GENERIC PACKAGE VIEW**

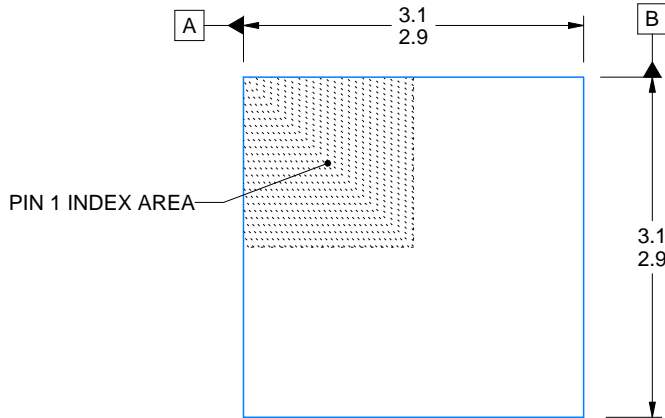
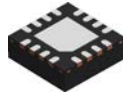
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD

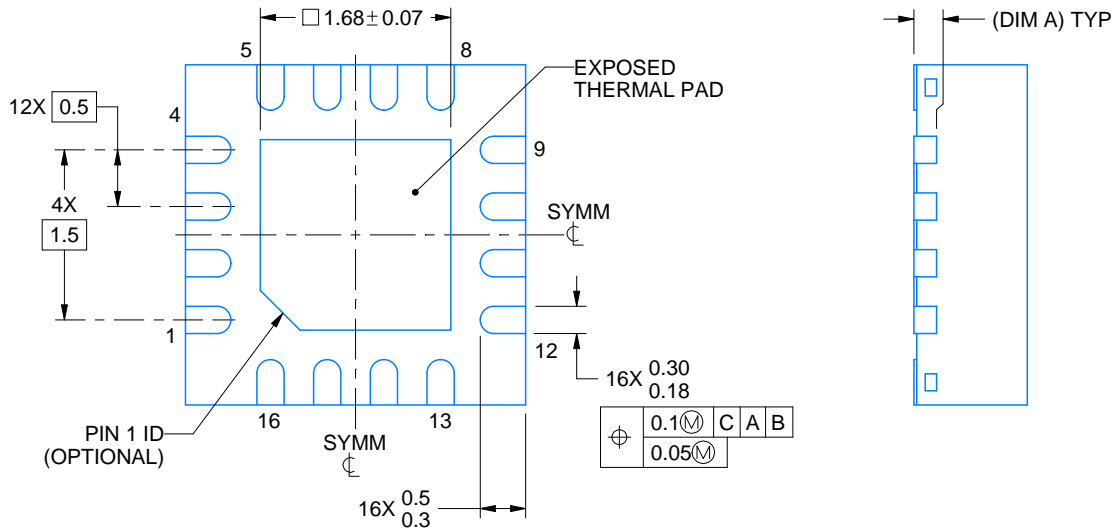
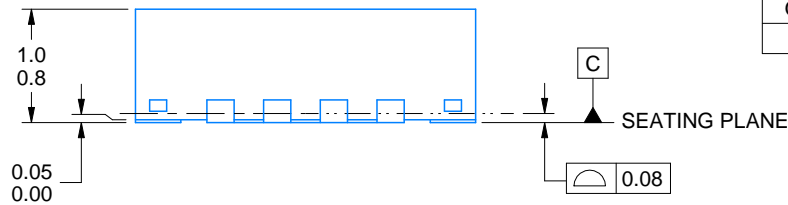


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/D 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



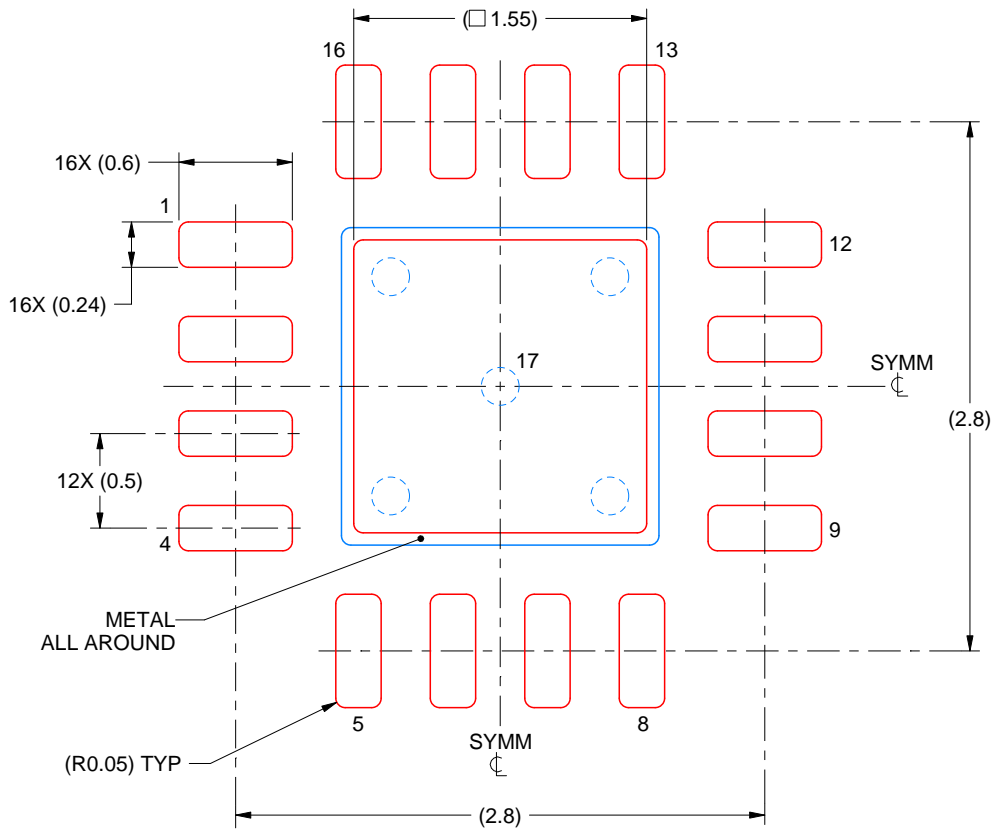


# EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:  
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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