Product Overview

1µV Ultra-Low Noise 12 Vin 3.3 Vout 1-A Power Supply

Design Goals

Table 1. Design Goals

VIN	VOUT	IOUT	Integrated Noise 10Hz-100kHz	Efficiency	PSRR at 100 kHz	Power Dissipation
12 V±1 V	3.3 V ±1.0%	1 A	<10 μV_{RMS}	> 75%	> 50 dB	< 1000 mW

Design Description

Modern digital to analog converters (DACs) and analog to digital converters (ADCs) used in high performance test and measurement equipment such as spectrum analyzer, signal generator, waveform generator, wireless communication tester, oscilloscope and data acquisition system, are sensitive to noise in the power supply, as noise can couple into the signal chain, reducing the quality of the measurement. Low-noise power supplies are essential for noise-sensitive ADCs and DACs to maximize signal integrity system performance.

There are two types of power supplies for DC to DC conversion, switching regulators and linear regulators.

Switching regulators are commonly used to step down an input voltage efficiently. However, the output of a switching regulators contains some switching noise that can adversely affect noise sensitive devices. On the other hand, low dropout linear regulators (LDOs) have low output noise, but due to low efficiency, LDOs are only used with low operating headroom to minimize power dissipation.

This application brief goes over the process of creating a high efficiency (> 75%) and ultra low noise (<10 μV_{RMS}) power supply by combining a switching converter and an LDO. Using switching converter first to efficiently reduce the majority of the input voltage to a lower voltage level that minimizes operating overhead for the LDO. Then the LDO effectively eliminate any remaining noise, providing a low-noise output.

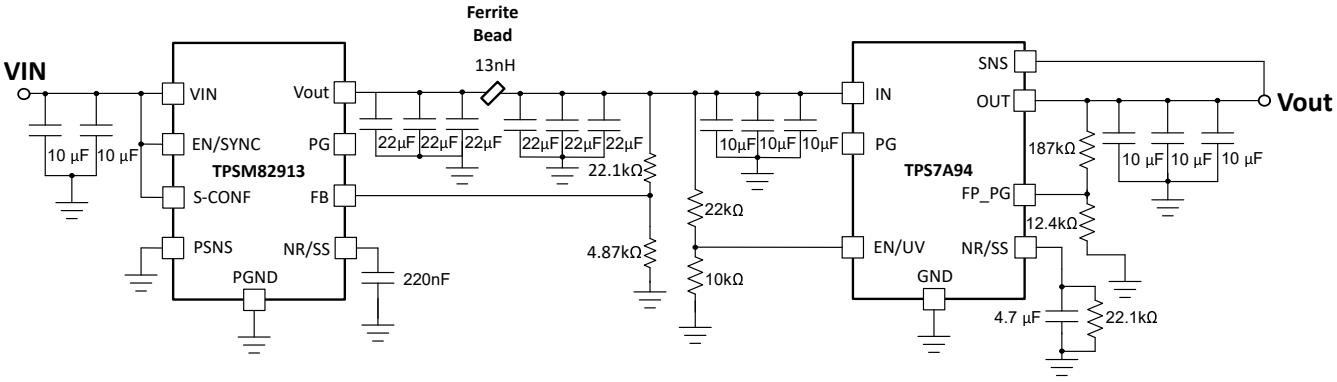

Figure 1. Simplified Schematic

Design Notes

±0.1% resistors are used for switching regulator's feedback network to minimize output voltage variation.

±0.1% resistor is required to set LDO output voltage to meet the ±1% output voltage tolerance requirement.

±1% tolerance resistors are used for EN, UVLO, PG pull up resistors, as those functions do not affect system output voltage precision.

The input bulk capacitor minimizes input voltage ripple, and output capacitors filter noise and transients. A switching regulator requires a minimum amount of input and output capacitance for stability and operation, while a linear regulator needs both input capacitors and output capacitors for best noise performance.

Ceramic capacitors are small, have low equivalent series resistance (ESR) and are used in this design for input and output decoupling. However, capacitance varies due to initial tolerance, temperature and voltage derating.

Capacitors must have ±20% or better tolerance. More initial capacitance is required in the design to account for worst case capacitance and requires more space. Tighter tolerance capacitors reduces the design overhead.

Ceramic capacitor have ratings represent capacitance change over the operating temperature range. X7R (-55°C - 125°C ±15%) and X7S (-55°C - 125°C ±22%) rated capacitors are used for this application brief.

Evaluation modules (EVMs) of TPSM82913 and TPSM7A94 are used for evaluation.

Design Steps

Select LDO

The LDO is selected first for this system, since the LDO must meet or exceed all specifications required by the load.

- VOUT ≥ 3.3 V ±1%
- IOUT ≥ 1 A
- Integrated noise from 10 Hz - 100 kHz < 10 μV_{RMS}
- PSRR at 100 kHz > 50 dB

LDO in this power supply does not need to meet 12 V system input requirement since a switching regulator is used to step down the input voltage to a voltage closer to output voltage.

Table 2 shows a short list of linear regulators that loosely meet requirements

Table 2. LDO Selection

PN	VIN	VOUT max	IOUT	Noise	PSRR at 100 kHz, 1 A, VIN=3.8 V, VOUT=3.3 V	PSRR At 1 MHz	Minimum Drop out Voltage
	V	V	A	μV_{RMS}	dB	dB	mV
TPS7A94	1.7-5.7	5.5	1	0.46	65	48	240
TPS7A96	1.7-5.7	5.5	2	0.46	60	40	250
TPS7A91	1.4-6.5	5.2	1	4.7	40	40	200
TPS7A88	1.4-6.5	5.2	1	3.8	40	40	200
TPS7A20	1.6-6	5.5	0.3	7	60	40	145
TPS7A21	2-6	5.5	0.5	7.7	61	50	175
TPS7A57	0.7-6	5.2	5	2.1	60	30	110

To create a power supply with the best output noise performance, the LDO with the highest PSRR and lowest noise performance is selected. TPS7A94 has output noise of 0.46 μV_{RMS}, while also meeting output voltage range, tolerance and current requirements. TPS7A94 has 3.3 μV_{RMS} less noise compared to the second lowest noise LDO, TPS7A88.

TPS7A96 provides the same low noise performance as TPS7A94 with a higher 2 A output current, which is great for systems that require low noise and more than 1 A current.

TPS7A57, TPS7A91, TPS7A88 are not selected for having lower PSRR than other devices on the list..

TPS7A20 and TPS7A21 do not meet 1 A output current requirement.

Set LDO Output Voltage

Figure 2 shows a simplified regulation circuit, with system output voltage is set by the internal 150 µA current source ($I_{NR/SS}$) and the external resistor ($R_{NR/SS}$).

To set the LDO output voltage to 3.3 V, calculate the required $R_{NR/SS}$ resistance with the following equation:

$$\text{Vout} = R_{NR/SS} \times I_{NR/SS} \quad (1)$$

$$R_{NR/SS} = \frac{V_{OUT}}{I_{NR/SS}} = \frac{3.3\ \text{V}}{150\ \text{uA}} = 22\ \text{k}\Omega \quad (2)$$

22.1 kΩ is used as it's the closest E96 resistor value available, resulting in a nominal VOUT of 3.315 V.

The 150 µA current source has ±1% tolerance, so a high precision ±0.1% resistor is required to minimize tolerance stack up, and to meet the ±1% output voltage tolerance requirement.

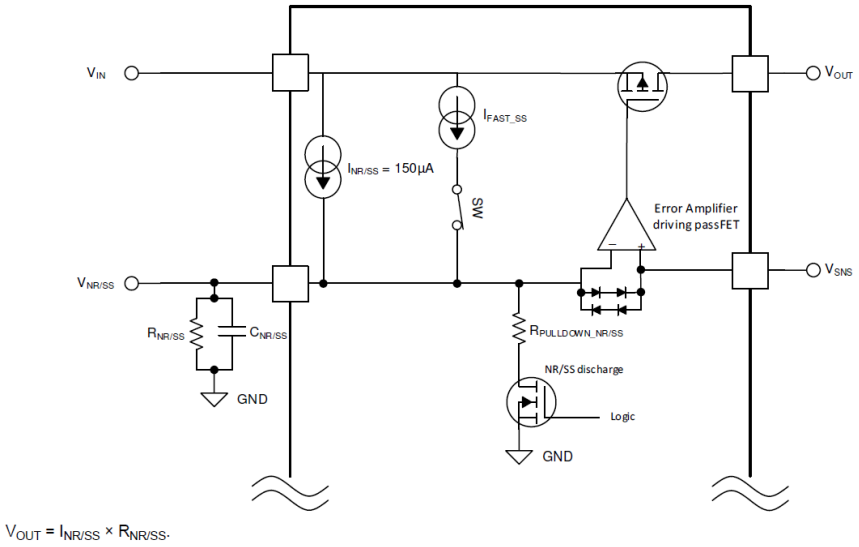

Figure 2. LDO Set VOUT

Select TPS7A94 $C_{NR/SS}$

There is a trade-off between output voltage noise and start-up time. The higher the capacitor value, the longer the start-up takes.Table 3 shows the tradeoff between the two.

Table 3. CNR/SS vs Start-up Time

Noise (μV_{RMS}) 10 Hz to 100 kHz	$C_{NR/SS}$ (µF)	C_{out} (µF)	Start-up Time (ms)
0.98	1	10	3.73
0.62	2.2	10	6.21
0.46	4.7	10	13.97
0.42	10	10	28.21

The goal of the design is to achieve very low noise. While selecting 10 µF for $C_{NR//SS}$ achieves lowest noise, it also has a long start-up time. Choosing a 4.7 µF capacitor for C_NR/SS only adds 0.04 µVrms of noise, while reducing the start-up time by 15ms. Therefore a single 4.7 µF capacitor is selected to strike a balance between low noise and start-up time.

TPS7A94 PSRR vs Operating Headroom

The operating headroom ($V_{Or\ Hr}$) refers to the difference between input and output voltage of the regulator. Based on Figure 3, 500 mV and 360 mV operating headroom have PSRR > 50 dB from 10 Hz to 100 kHz, in contrast, 300 mV and 240 mV operating headroom have PSRR < 50 dB from 10 to 100 kHz. Therefore, the switching regulator's output voltage needs to be 3.675 V or higher to meet the system PSRR requirement.

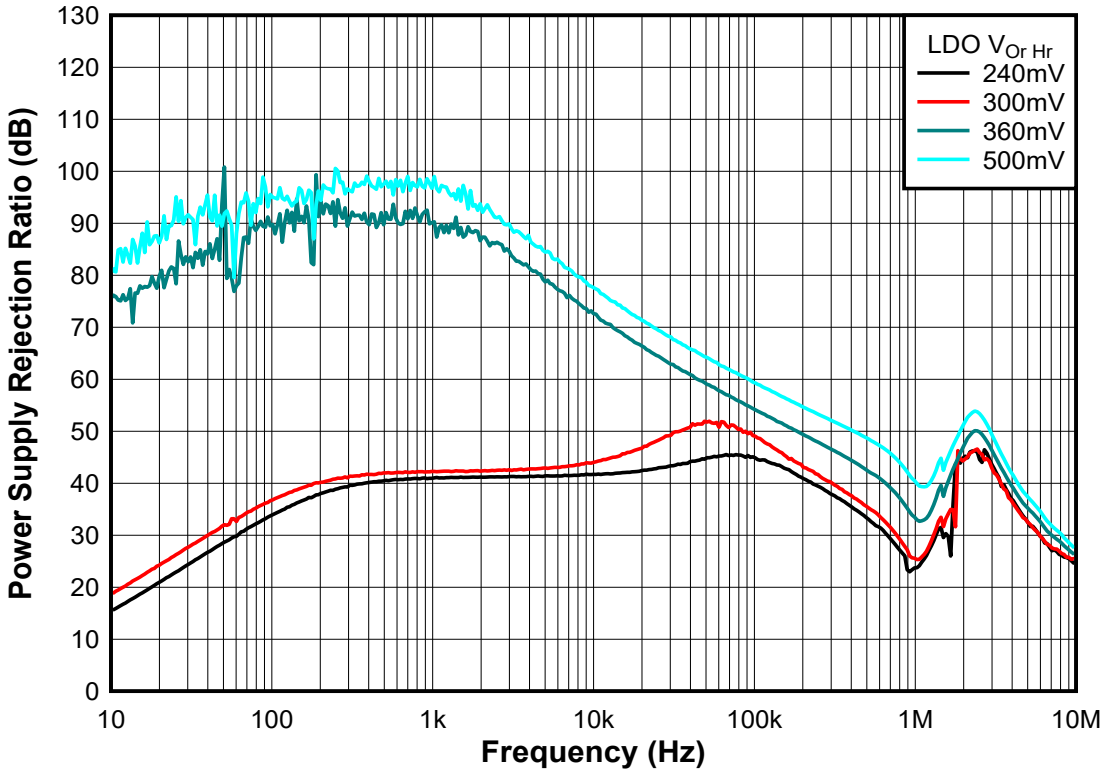

Figure 3. System PSRR

Evaluate LDO Power Dissipation

$R_{\Theta JA}$ for TPS7A94 is 25.6 °C/W. With 500-mW power dissipation when $V_{Or\ Hr}$ = 500 mV and I_{OUT} = 1 A, the resulting temperature increase is only 12.8 °C above ambient.

TPS7A94 EVM Default Setting

Current limit, soft start and UVLO circuits are set to EVM defaults. See TPSM82913 data sheet section 7.3.3 - 7.3.5 for more detail.

Select DC-DC Converter

The DC-DC Converter must meet the following requirements

1. V_{IN} > 13 V
2. VOUT > 3.8 V
3. IOUT ≥ 1 A

A low noise DC-DC converter reduces overall system noise, especially at frequencies where LDO PSRR is low. Most DC-DC converters do not have output noise specified. TPSM82913 was designed as an LDO replacement with much lower noise than a typical buck converter. With a second-stage filter, TPSM82913 has an integrated noise of 22 μV_{RMS} from 10 Hz - 100 kHz. For comparison, the integrated noise of a typical switching converter, TPS543620, is 87 μV_{RMS}.

Set TPSM82913 Output Voltage

To set the output voltage of TPSM82913, feedback resistors R1 and R2 need to be selected.

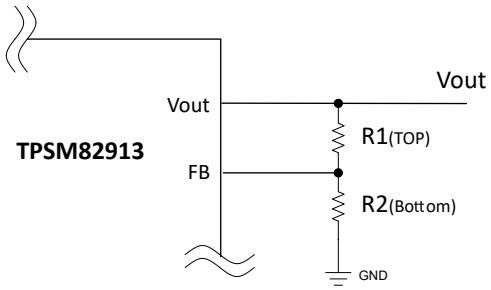

Figure 4. Feedback Resistors

TPSM82913 has 0.8 V internal reference voltage, and with R2 already set to 4.87 kΩ on the EVM, use the following formula to find R1:

$$R1 = R2 \times \left(\frac{V_{OUT}}{0.8V} - 1\right) \quad (3)$$

Table 4. Calculated R1 Values

Operating Head Room (mV)	VOUT (V)	R1 (kΩ)
500	3.8	18.2
360	3.66	17.4
300	3.6	17.2
240	3.54	16.9

TPSM82913 Input Capacitor Selection

TPSM82913 requires 10 µF minimum input capacitance to be stable. Two 10 µF 25 V X7S ceramic capacitors are used to account for tolerance and capacitance change over temperature and voltage. The EVM also contains a 35 V 47 µF electrolytic capacitor to compensate for the long input power wire's inductance.

TPSM82913 Output Capacitor Selection

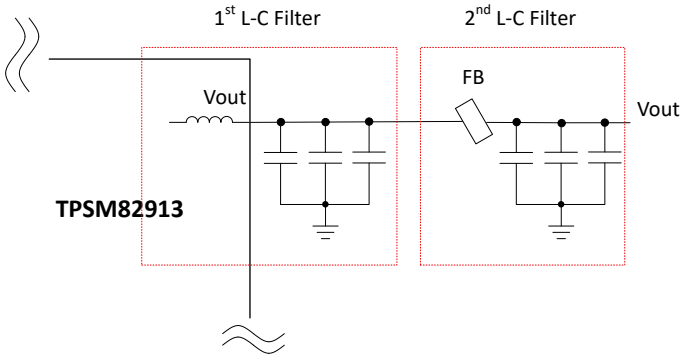

Figure 5. Output Capacitor Diagram

TPSM82913 has the following output capacitor requirements when using a second L-C filter: the first L-C filter must have output capacitance between 40 µF and 80 µF, the second stage L-C filter must have at least 20 µF of capacitance, and the total capacitance for both L-C filters must be less than 200 µF. Three 22 µF, 10 V, X7R Ceramic capacitor are used for the 1st stage and 2nd stage to meet the output stability and capacitance requirements.

Set TPSM82913 S-Config

Switching frequency is selected to be 2.2 MHz, to minimize ripple for relatively high VOUT at 3.3 V-4.3 V. Spread spectrum feature is intended to reduce SW frequency noise and higher harmonics. Since NSD noise is measured at much lower frequencies 10 Hz-100 kHz, Spread Spectrum is turned off and since output discharge and synchronization features are also not required, S-Config pin is tired directly to VIN. See Table 7.1 of data sheet for other S-Config pin configurations.

Select Ferrite Bead

A ferrite bead combined with a second set of output capacitors creates a second stage filter that further damps high frequency noise. The ferrite bead needs to have inductance within the design range for stability, a current rating higher than 1 A and low DC resistance.

The TPSM82913 has internal compensation for a ferrite bead with inductance between 10 nH to 50 nH. Ferrite beads are only specified with impedance at 100 MHz, so inductance L can be calculated with equation below and the impedance at 100 MHz is required to be in between 6.3 Ω and 31 Ω.

$$L = \frac{Z}{2 \times \pi \times f} \tag{4}$$

$$Z = 2 \times \pi \times 100MHz \times 50nH = 31.4\ \Omega \tag{5}$$

- Z is the impedance of the ferrite bead at the specified frequency (Typically 100 MHz)
- F is the frequency at which the impedance is measured

The BL18PS080SN1, which has impedance of 8.5Ω at 100 kHz, 4-mΩ DC resistance, 8-A DC rating, and an 0603 package size, meets the desired requirements for this application. Higher impedance ferrite beads, which are also available in larger package sizes, can be selected depending on application requirements.

Total System PSRR

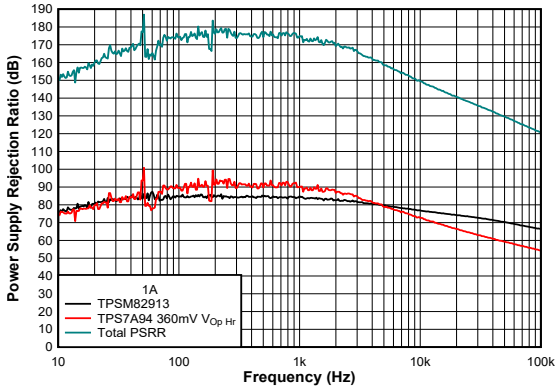

Figure 6. System PSRR

Total system PSRR is the sum of the PSRR of TPSM82913 and TPS7A94. In this case, the PSRR is over 170 dB.

TPSM82913 Thermals

TPSM82913 has, $R_{\Theta JA}$ (junction to ambient resistance) = 25.6 °C/W, at 1 A load, and with 0.5 W power dissipation, resulting temperature increase is only 12.8°C above ambient.

TPSM82913 EN/UVLO

TPSM82913 is enabled when V_{IN} is raised above V_{UVLO} of 2.92 V, and since device synchronization is not needed, EN/SYNC pin is directly tied to VIN.

TPSM82913 Current Limit

TPSM82913 has a current limit of 4.3 A, sufficient for 1 A application. If a different current limit is desired for an application, see section 7.3.9 in TPSM82913 data sheet.

Test Results

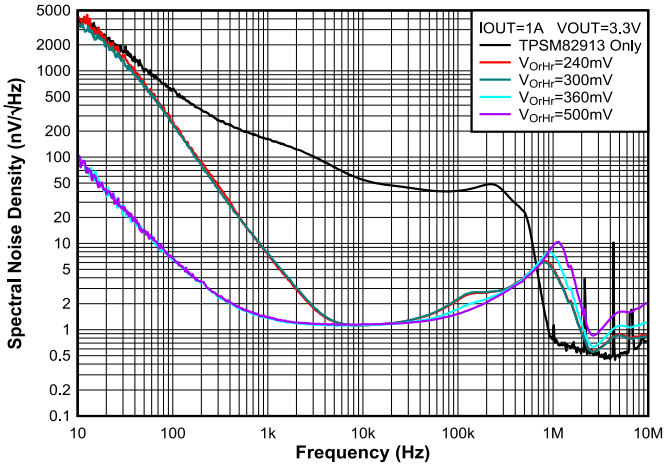

Figure 7. Noise Density Measurement

Several configurations of TPSM82913 and TPS7A94 are tested inside an enclosed RF chamber, and system output noise is measured with E5052B Spectrum Analyzer. As shown by Noise density graph above, only using a switching converter results in the highest noise, 23 μV_{RMS} from 10 Hz - 100 kHz.

When the TPS7A94 has less than 360 mV of operating headroom, the system have 13 μV_{RMS} noise from 10 Hz - 100 kHz.

When TPS7A94 has more than 360 mV of operating headroom, the system have very low noise of 0.5 μV_{RMS} noise from 10 Hz - 100 kHz.

Table 5. System Performance vs. Operating Headroom

			Operating Headroom			
	Integration Bandwidth	**TPSM82913 Only**	**500 mV**	**360 mV**	**300 mV**	**240 mV**
Noise (μVRMS)	10 Hz-100kHz	22.43	0.49	0.51	11.34	12.97
	1 Hz - 100 kHz	29.05	1.44	1.50	20.91	21.14
	1 Hz - 10 MHz	38.5	9.54	7.12	21.88	21.88
Efficiency		87%	76%	79%	81%	82%
Power dissipation (mW)		480	1000	890	770	710

Noise is lowest when $V_{Or\ Hr}$ is at least 360 mV, which is 210 mV above the typical drop out voltage of 150 mV. To maintain the same margin when drop out voltage is at the maximum of 240 mV, 450 mV minimum operating headroom is required.

In conclusion, a low noise DC-DC switching regulator used in conjunction with ultra-low noise LDO TPS7A94 with sufficiently high head room, can achieve ultra-low noise performance and high efficiency.

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