Thin Very Small-Outline Package (TVSOP)

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TEXAS INSTRUMENTS

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Introduction

Development of portable, lightweight, high-performance electronics products is driving the semiconductor industry toward smaller, thinner, and higher-density packages. Pricing pressures are encouraging strong efforts toward cost reduction.

Texas Instruments (TI) always has been a leader in IC packaging and is now introducing a new family of thin very small-outline packages (TVSOP) to support the component miniaturization requirements of the industry. The new TVSOP package family, in 14-, 16-, 20-, 24-, 48-, 56-, 80-, and 100-pin types, features a lead pitch of 0.40 mm (16 mil) and a device height meeting the 1.2-mm Personal Computer Memory Card International Association (PCMCIA) requirement. The TVSOP packages have received Joint Electronics Device Engineering Council (JEDEC) registration under semiconductor package standard MO-194.

This application report presents an overview of the TVSOP package family characteristics, including thermal, electrical, reliability, and moisture-sensitivity performance. Assembly and mounting guidelines for devices with 0.40-mm lead pitch are included.

TVSOP Dimensions

Figure 1 and Table 1 show TVSOP package dimensions.

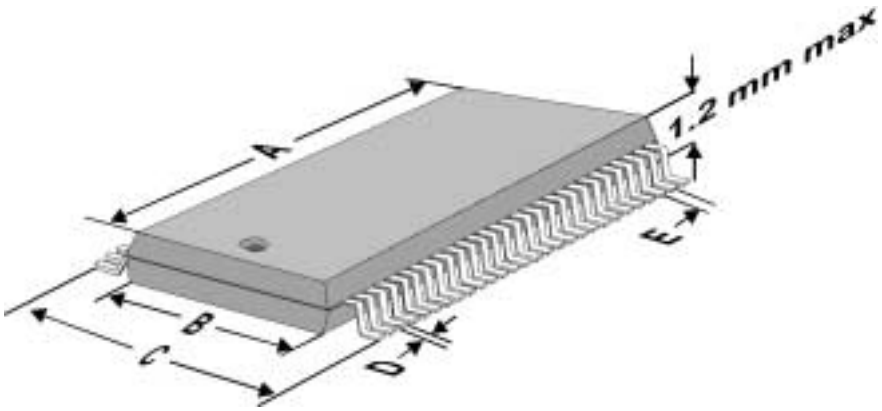


Figure 1. TVSOP Dimensions

Table 1. TVSOP Dimensions by Pin Count

TVSOP PACKAGE	TYPICAL DIMENSIONS (mm)					AREA (mm^2)	PERCENTAGE SMALLER THAN SSOP	PERCENTAGE SMALLER THAN TSSOP	PERCENTAGE SMALLER THAN TQFP
	A	B	C	D	E				
14 pin	3.60	4.40	6.40	0.18	0.40	23.00	52.4	29.3	
16 pin	3.60	4.40	6.40	0.18	0.40	23.00	52.4	29.3	
20 pin	5.00	4.40	6.40	0.18	0.40	32.00	43.0	24.0	
24 pin	5.00	4.40	6.40	0.18	0.40	32.00	50.0	34.0	
48 pin	9.80	4.40	6.40	0.18	0.40	63.00	61.9	38.0	
56 pin	11.3	4.40	6.40	0.18	0.40	72.30	62.2	36.0	
80 pin	17.0	6.10	8.10	0.18	0.40	137.8			30.0
100 pin	20.8	6.10	8.10	0.18	0.40	168.5			35.0

Advanced System Logic (ASL) Packaging Trends

Figure 2 shows how the TVSOP package follows the trend toward smaller and smaller surface-mount packages.

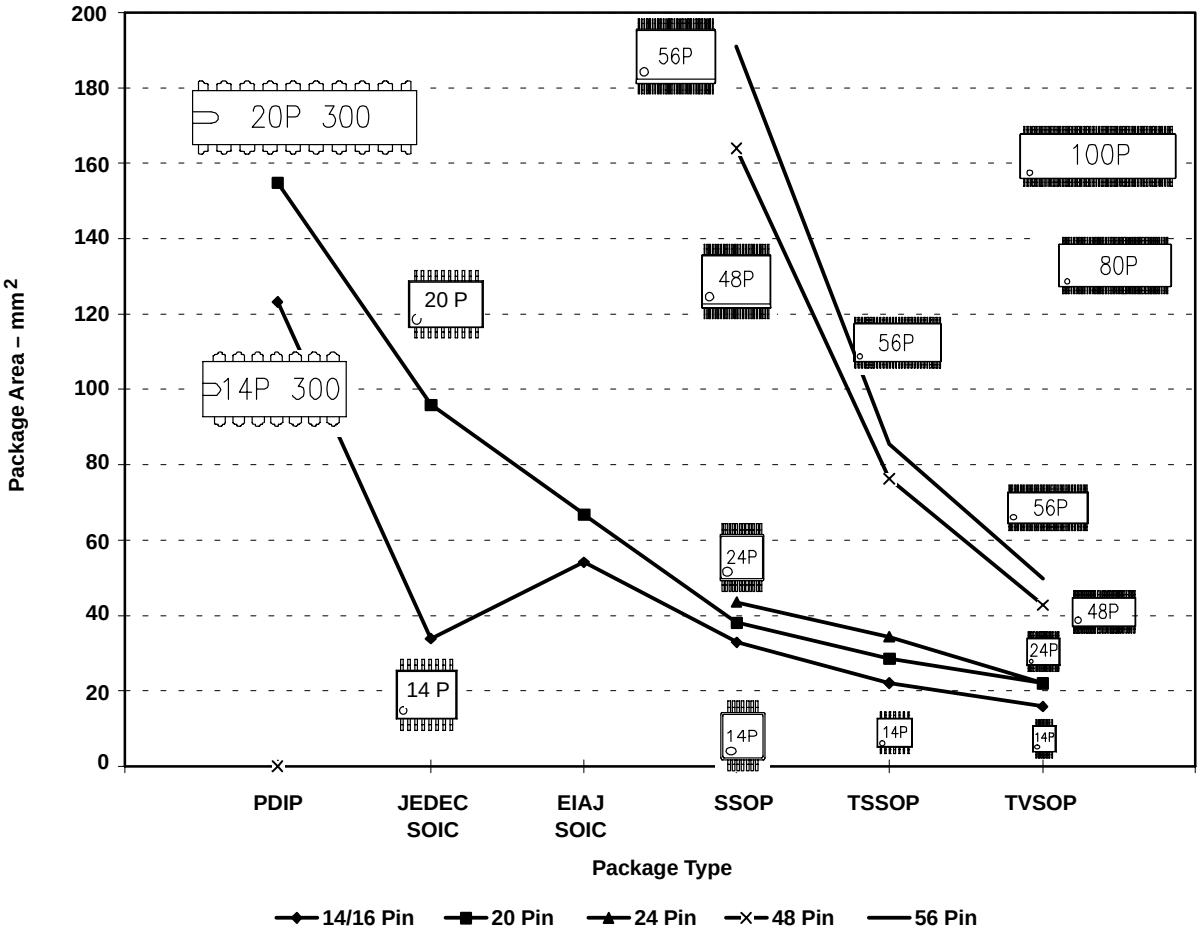
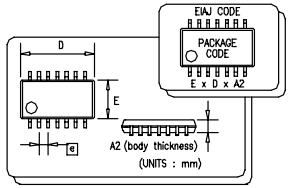
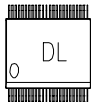


Figure 2. Package Area Comparison

ASL Lineup of Similar Packages

Figure 3 shows TI's SSOP, TSSOP, and TVSOP surface-mount packages with pin pitches of 0.65 mm to 0.40 mm.

PACKAGE TYPE	EIAJ TYPE (mil)	PITCH e	14	16	20	24	48	56	100	80	JEDEC
SSOP	II 300	0.65	 5.3 x 6.2 x 1.8	 5.3 x 6.2 x 1.8	 5.3 x 7.2 x 1.8	 5.3 x 8.2 x 1.8					
	III 375	0.635					 7.5 x 15.9 x 2.3	 7.5x 18.4 x 2.3			
TSSOP	I 225	0.65	 4.4 x 5.0 x 1.0	 4.4 x 5.0 x 1.0	 4.4 x 6.5 x 1.0	 4.4 x 7.8 x 1.0					MO-153
	II 300	0.50					 6.1 x 12.5 x 1.0	 6.1 x 14.0 x 1.0			MO-153
TVSOP	I 225	0.40	 4.4 x 3.6 x 1.0	 4.4 x 3.6 x 1.0	 4.4 x 5.0 x 1.0	 4.4 x 5.0 x 1.0	 4.4 x 9.7 x 1.0	 4.4 x 11.3 x 1.0			MO-194
	II 300	0.40							 6.1 x 17.0 x 1.0	 6.1 x 20.8 x 1.0	MO-194

NOTE: Package outlines are not to scale.

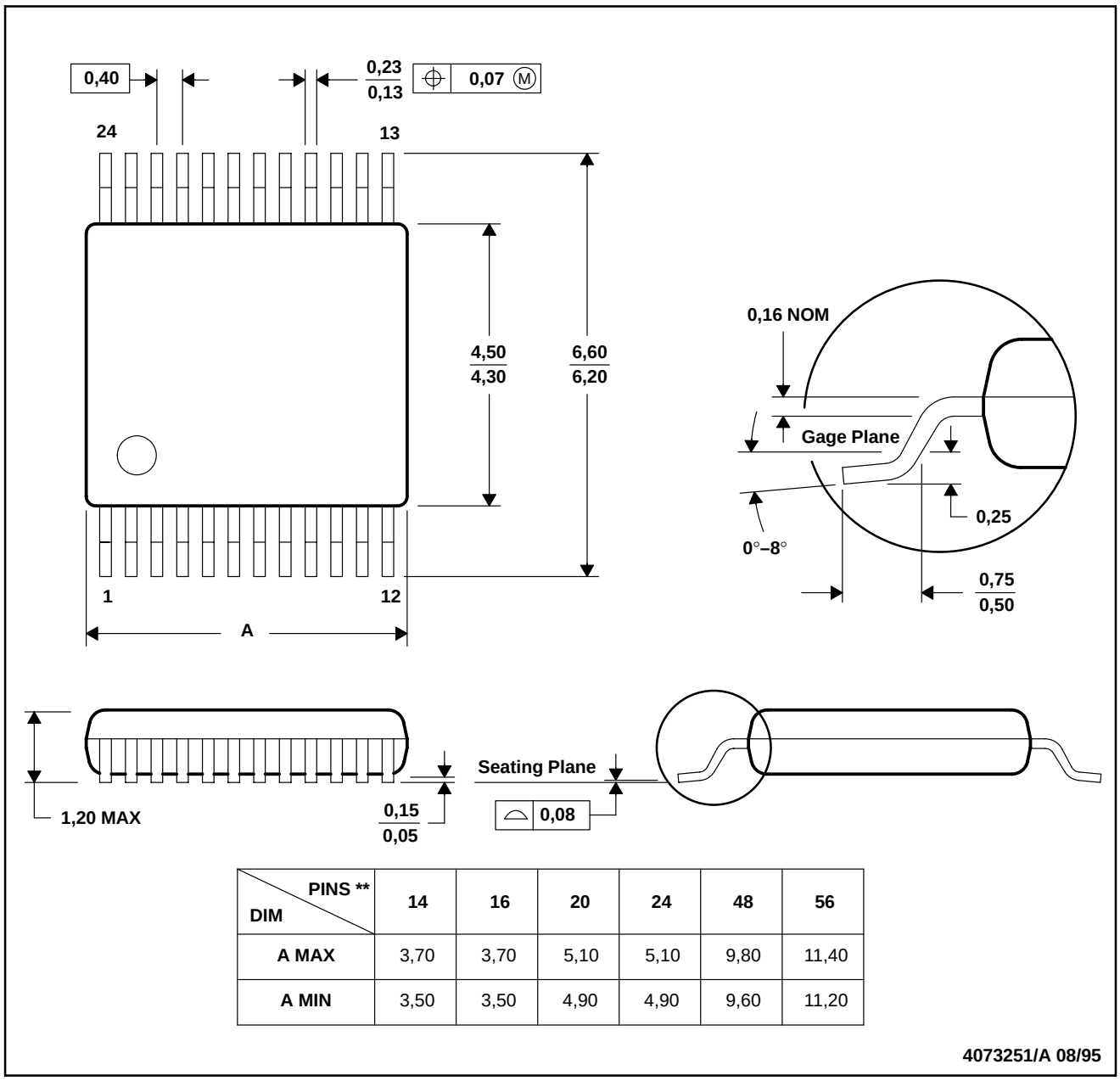
Figure 3. SSOP, TSSOP, and TVSOP Packages

The TVSOP Package and Its Development

Description

Figures 4 and 5 show the basic dimensions of the TVSOP package.

24 PIN SHOWN

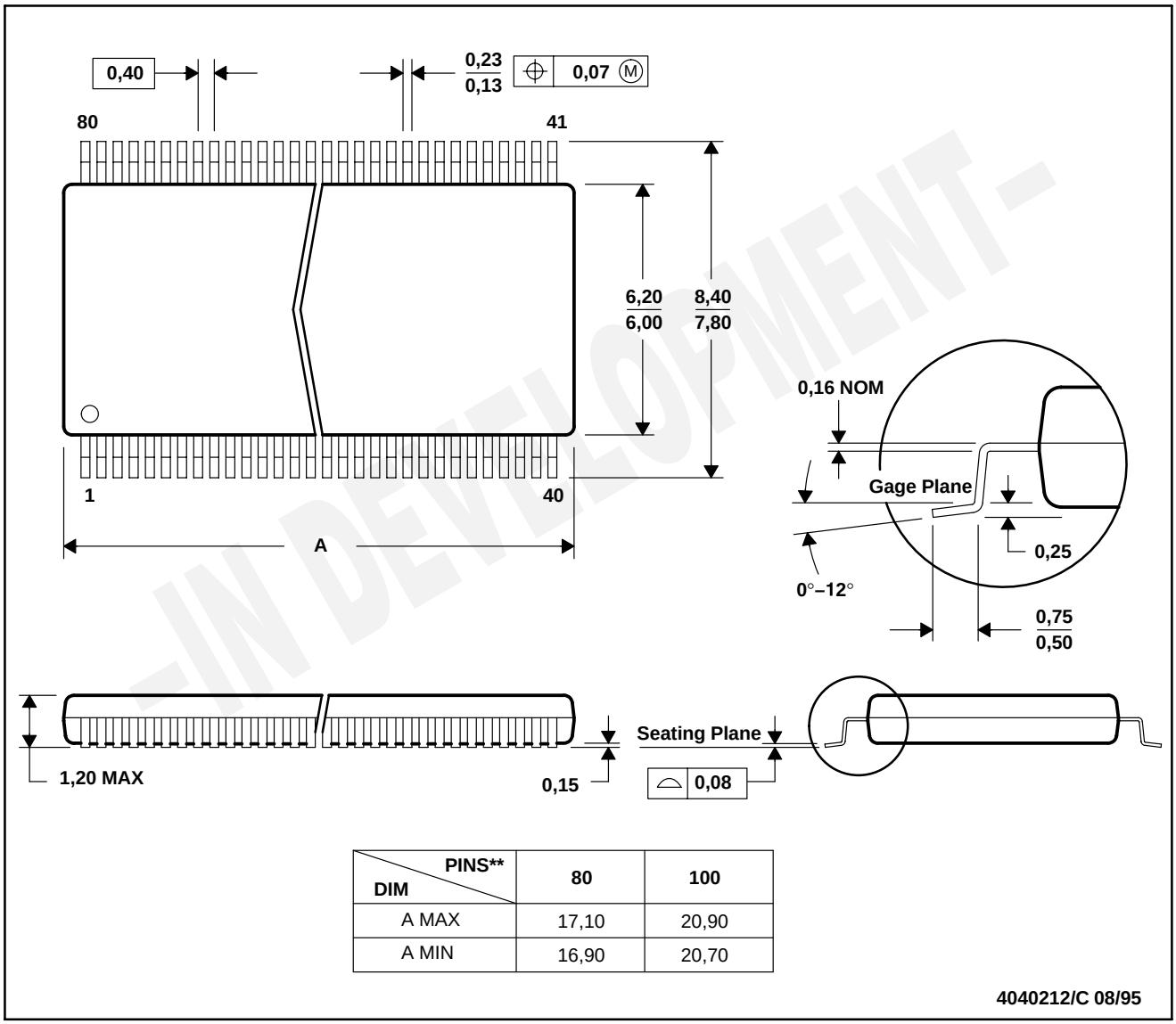


DIM \ PINS **	14	16	20	24	48	56
A MAX	3,70	3,70	5,10	5,10	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	9,60	11,20

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

Figure 4. 14-Pin to 56-Pin TVSOP Package Dimensions

80 PIN SHOWN



DIM \ PINS**	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

Figure 5. 80-Pin and 100-Pin TVSOP Package Dimensions

JEDEC Registration

The TVSOP packages are registered under the JEDEC MO-194 standard for semiconductor packages (see Table 2).

Table 2. JEDEC Registration for TVSOP Packages

PACKAGE	PINS	JEDEC REGISTRATION
DGV	14	MO-194AA
DGV	16	MO-194AB
DGV	20	MO-194AC
DGV	24	MO-194AD
DGV	48	MO-194AE
DGV	56	MO-194AF
DBB	80	MO-194BA
DBB	100	MO-194BB

Symbolization

Symbolization for the TVSOP follows the TI standard. Due to the small size of many of the packages, some characters are omitted or characters are substituted for whole part types. Figure 6 shows the general symbol format and Table 3 lists the character omissions or substitutions. The 14- and 16-pin devices are too small to permit the entire lot-trace code to be symbolized; only characters for the year of the decade and month are included. Complete lot-tracing code information is included on the product packaging labels.

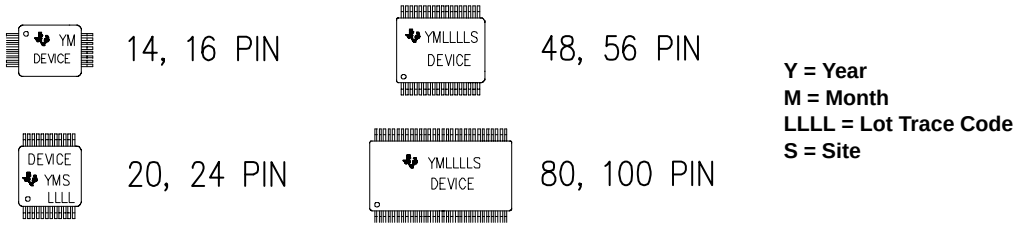


Figure 6. Product Symbolization Format

Table 3. Product Symbolization

FAMILY	DEVICE CODE BY PACKAGE AND PIN COUNT		
	DGV (14, 16, 20, 24)	DGV (48, 56)	DBB (80, 100)
SN74ALVCH16xxx	N/A	VHxxx	ALVCH16xxx
SN74ALVCHG16xxx	N/A	VGxxx	ALVCHG16xxx
SN74ABTxxx	ABxxx	N/A	N/A
SN74ABTHxxx	AKxxx	N/A	N/A
SN74ABT16xxx	N/A	AHxxx	N/A
SN74ABTH16xxx	N/A	AMxxx	N/A
SN74AHCxxx	HAxxx	N/A	N/A
SN74AHCTxxx	HBxxx	N/A	N/A
SN74CBTD3xxx	CCxxx	N/A	N/A
SN74CBT16xxx	N/A	CYxxx	CBT16xxx
SN74LVCxxx	LCxxx	N/A	N/A
SN74LVCHxxx	LCHxxx	N/A	N/A
SN74LVC16xxx	N/A	LDxxx	N/A
SN74LVCH16xxx	N/A	LDHxxx	N/A

NOTE: Please contact your nearest TI sales office or authorized distributor for specific device and type availability.

Printed Circuit Board Manufacture With the TVSOP

Overview of Test Site Results

ASL Packaging Engineering has been working in cooperation with Solectron, Texas (formerly TI Custom Manufacturing Services, Austin) and AVEX Electronics, Inc. to develop printed circuit board (PCB) assembly-process guidelines for ultra-fine-pitch packages in high-volume manufacturing.

The majority of defects encountered in board assembly with fine-pitch packages are caused by solder bridging, open circuits, or improper device placement. Proper lead planarity and the absence of bent leads are essential to minimize assembly-mounting defects. Components with poor coplanarity require more solder paste to obtain a good solder joint. The increased volume of solder paste can cause bridging. All board-mounted components must be selected carefully, based on the lead foot specifications provided by component suppliers. Lead coplanarity data are constantly monitored on TI TVSOP packages to ensure that all units fall within the JEDEC coplanarity specifications of less than 0.08 mm. Inaccurate device placement, the last of the defect issues, is a function of pick-and-place equipment capability.

Two major potential applications for TVSOP 0.40-mm packages were addressed during the assembly process development project: standard PCB boards (8 in. × 16 in.) and standard PCMCIA cards. Many factors can affect board performance (equipment, environment, component and board quality, etc.), therefore, the guidelines presented herein primarily are intended to give manufacturers and designers useful information that resulted from our package-development work.

TVSOP Results From TI Custom Manufacturing Services

TI conducted evaluations to establish the design and processing requirements, along with the limitation in applying the TVSOP series of 0.40-mm- (16-mil) pitch devices. Footprint-geometry, stencil, placement, and surface-mount technology (SMT) processing guidelines are needed to minimize the solder-defect rate of indiscriminate use of 0.40-mm-pitch devices in designs.

Each SMT assembly-process defect rate is unique to the demands of 0.40-mm-pitch devices in the assembly process. Equipment accuracy, repeatability, and process capability all play large roles in the resultant defect rate. Therefore, differences in the magnitudes of the rates achievable through implementation of the recommended guidelines have been quantified.

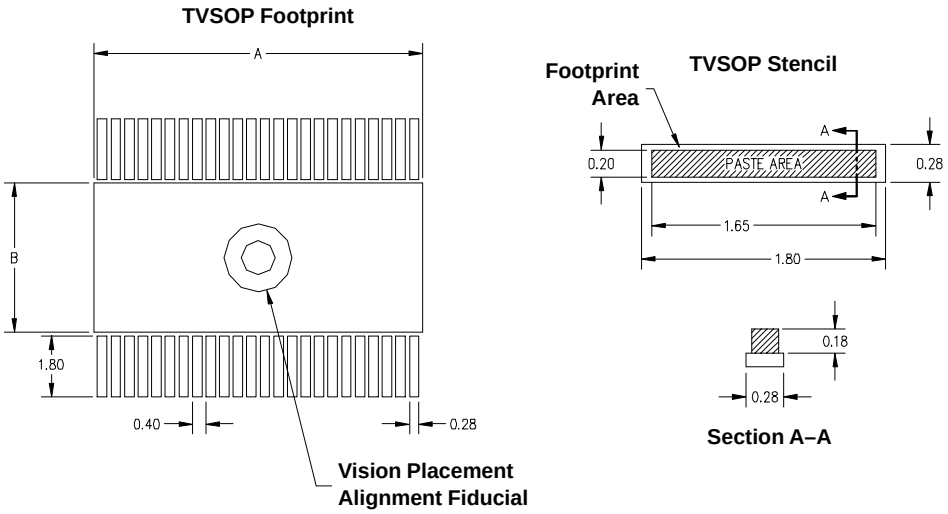
Pad Geometry Requirements

The following dimensional requirements for the 0.40-mm-pitch terminal pad are recommended (see Figure 7):

Terminal pad length	1.8 mm, 0.070 in.
Terminal pad width	0.28 mm, 0.011 in.
Terminal pad pitch	0.4 mm, 0.0157 in.
Gerber Tru Position	2–4 format minimum
Pad finish	ENTEK™

Conclusion: The pad geometry and finish are very important to the assembly-defect rate for widely spaced 0.40-mm-pitch devices.

ENTEK is a trademark of Enthone, Incorporated.



See table below for dimension A and B **All dimensions in mm**

	PIN COUNT					
	14/16	**20/24**	**48**	**56**	**80**	**100**
Dimension A	3.6	5.0	9.8	11.3	17.0	20.8
Dimension B	4.4	4.4	4.4	4.4	6.1	6.1

Figure 7. Pad and Stencil Geometry

Stencil Geometry Requirements

We recommend a single-level, laser-cut, electro-polished stainless steel, 0.006-in.-thick stencil for any product that has both PLCC and 0.40-mm-pitch devices. PCBs without PLCC devices could use a 0.005-in. stencil. However, other 50-mil-pitch devices trend toward insufficient solder volume.

	PLCC AND TVSOP	TVSOP ONLY
Stencil opening length	0.065 in.	0.065 in.
Stencil opening width	0.008 in.	0.008 in.
Stencil thickness	0.006 in.	0.005 in.
Gerber 7 position	2–4 format minimum	

Conclusion: Stencil thickness has the greatest influence on defect rates. Our experience shows that a small increase in the solder-short defect rate of 0.40-mm-pitch devices is preferable to using a thinner stencil that produces opens or solder insufficiencies that are difficult to detect.

Component Placement

All 0.40-mm-pitch device defect rates (shorts) are very sensitive to the lead orientation with respect to the radial distance the devices are from the stencil alignment point (usually the center of the PCB). Defect rates of widely-spaced TVSOP devices can be reduced by orders of magnitude by placing the device with its leads parallel to the raw PCB image-stretch axis. Each PCB and stencil has an image positional accuracy that usually exhibits an inch-per-inches misregistration. Also, stencils have an image-registration accuracy and tend to change dimensionally with the number of print cycles.

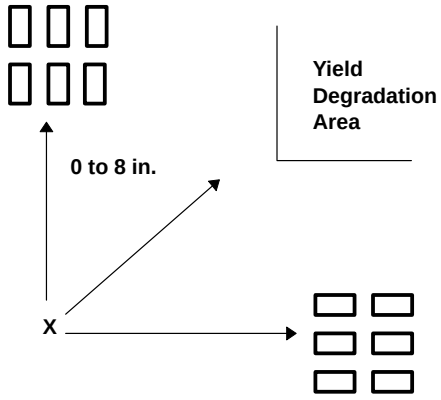
Placement of TVSOP Devices (0.40-mm-Pitch Devices With Leads on Two Sides of the Body)

The previously stated dimensional considerations yield the following optimum placement practices. This information applies to any pin count of a 0.40-mm-pitch small-outline package.

Maximum assembly yields for components placed more than 8 in. from the center of the PCB (stencil alignment point) can be achieved by orienting the leads parallel to the PCB expansion axes, with the longest distance from the center point. In areas where the distance from the alignment point is excessive (yield degradation area), the defect rate climbs rapidly without special placement guidelines.

Devices outside the 8-in. area must have their leads positioned as shown in Figure 8 or assembly yields degrade significantly.

Devices in the yield degradation area of Figure 8 should be avoided. If unavoidable, the leads should be oriented at 45 degrees to the PCB expansion axes to avoid excessive defects.



CORRECTLY ORIENTED DEFECT EXPECTATIONS

Inches from center	1	2	3	4	5	6	7	8	9	10	11
Yield degradation	0	0	0	0	0	0	1×	2×	4×	10×	30×

NOTE: Magnitude of 4× denotes 4 times the defect rate.

Figure 8. TVSOP Placement on PCBs

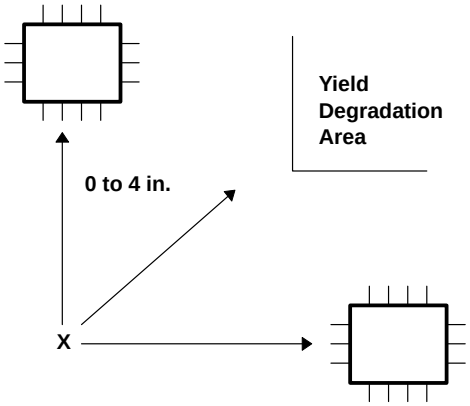
Quad Flatpack (QFP) Devices

This information applies to any pin count 0.40-mm-pitch QFP (leads out all sides) device.

QFP devices cannot avoid defects by changing their lead orientation from 0 to 90 degrees. There is the added complication of stenciling inconsistency with leads in both directions.

Optimum assembly yields of a QFP device are realized when the component is rotated 45 degrees from the PCB expansion axis. Significant defects occurred at all distances more than 4 in. from the stencil alignment point with normally oriented QFPs (see Figure 9).

In summary, placement of any 0.40-mm-pitch device has the second greatest influence over the defect rate.



CORRECTLY ORIENTED 45-DEGREE DEFECT EXPECTATIONS

Inches from center	1	2	3	4	5	6	7	8	9	10	11
0–90° orientation	0	0	0	10×	20×	50×	100×	250×	500×		
45° orientation	0	0	0	0	0	0	0	0	10×	20×	100×

Figure 9. QFP Placement on PCBs

Raw-PCB and Stencil-Image Attributes

The image reproduction accuracy of the raw PCB and stencil are critical in obtaining and sustaining a satisfactory defect rate with widely spaced 0.40-mm-pitch devices. The stencil can be aligned at only one point on the PCB image. Any misregistration approaching a full space between the 0.40-mm-pitch leads (16 mils or 0.006 in.) causes shorts, beginning at tens of thousands of parts per million.

Typical commercial PCB fabrication processes have not comprehended the need for very accurate and repeatable images on the active side of the PCBs. Research indicates that the specifications and requirements for image registration are not well defined. The old *hole true-position registration* plays very little part in the sub-0.50-mm-pitch assembly process. Some points of reference were obtained. One supplier suggests an image registration accuracy of ±0.002 in. (0.00011 in. per inch) over a 24-in. by 18-in. fabrication panel. This experiment substantiated that level of registration misalignment.

PCB Image Misregistration

The following data summarizes the estimated maximum misregistration allowed:

TEST BOARD DIMENSIONS	MEAN X	3 SIGMA X	MEAN Y	3 SIGMA Y	INCH PER INCHES
15 in.	0.0018	0.0024			0.00012
6 in.			0.00136	0.00138	0.00025

Conclusion: Use of widely-spaced 0.40-mm-pitch devices requires an image-registration-tolerance specification and lot testing at the supplier to ensure compliance. Exceeding 0.00015 in. per inch in registration accuracy begins to degrade the defect rate.

The stencil-image registration is just as important as the PCB. It has been our experience that stencil images are as difficult to control as the PCB image. Also, the image moves with the number of print cycles. The movement is of limited predictability.

Conclusion: As with the PCB, every stencil-image registration must be specified and verified when first purchased. Maximum misregistration should be ±0.002 in. over 13 in. (0.00015 in. per inch). If the dimensional registration of the board and stencil are at alignment extremes, it is prudent to rebuild the stencil to more closely match the board-registration trends. The maximum mismatch allowable, including the stencil visual-alignment accuracy, is 0.005 in. before significant defects occur. Compensating a stencil to match board lots is considered counterproductive.

Stencil Process

Equipment capability is critical to the defect rate (see Figures 10 and 11). Characteristics of the stencil equipment and process are:

Stencil printer	MPM UP 3030
Stencil alignment accuracy	±0.0003 in.
Solder paste type	Alpha 609
Solder paste particle size	325 to 500
Stencil thickness	0.006-in. laser-cut 301 stainless steel
Squeegee type	Metal
Paste actual thickness	Mean = 0.0069 in.
Average 9 boards, 3 devices, 10 leads per device	3 sigma = 0.00073
Paste volume	Mean = 3110 mils^3
3 sigma paste volume	3 sigma = 281 mils^3

Component-Placement Process

Characteristics of the placement process are:

Placement equipment	Fuji IPIII Placer
Placement accuracy	±0.0015 in.

The parts were placed on the pads using two local fiducials per device.

Conclusion: The placement was aligned with local fiducials and the devices were placed in the center of the pads. Placement was not considered a significant contributor to the defect rate.

Infrared-Reflow Characteristics

Our standard reflow profile for this type of board was used. Characteristics of the solder-paste-reflow process are:

Infrared reflow oven	Full convection BTU MN: TRS21
Atmosphere	Shop air (no nitrogen)
Chain speed	40 in. per minute
Maximum temperature	215°C
Time over 183°C	90 seconds

Conclusion: The infrared-reflow profile has the least effect on the 0.40-mm-pitch defect rate. A profile is shown in Figure 12.

Overall Conclusion: Special attention to design and the assembly process is critical to assembly of widely spaced 0.40-mm-pitch devices. Closely spaced 0.40-mm-pitch devices offer lower defect rates. With proper design, the most important is placement and lead rotation. Widely spaced 0.40-mm-pitch devices can be assembled with defect rates approaching those of 0.50-mm-pitch devices. Not paying attention to a few basic requirements can make a product unmanufacturable and cost the manufacturer in touch-up costs per board, a truly non-value-added and avoidable expense.

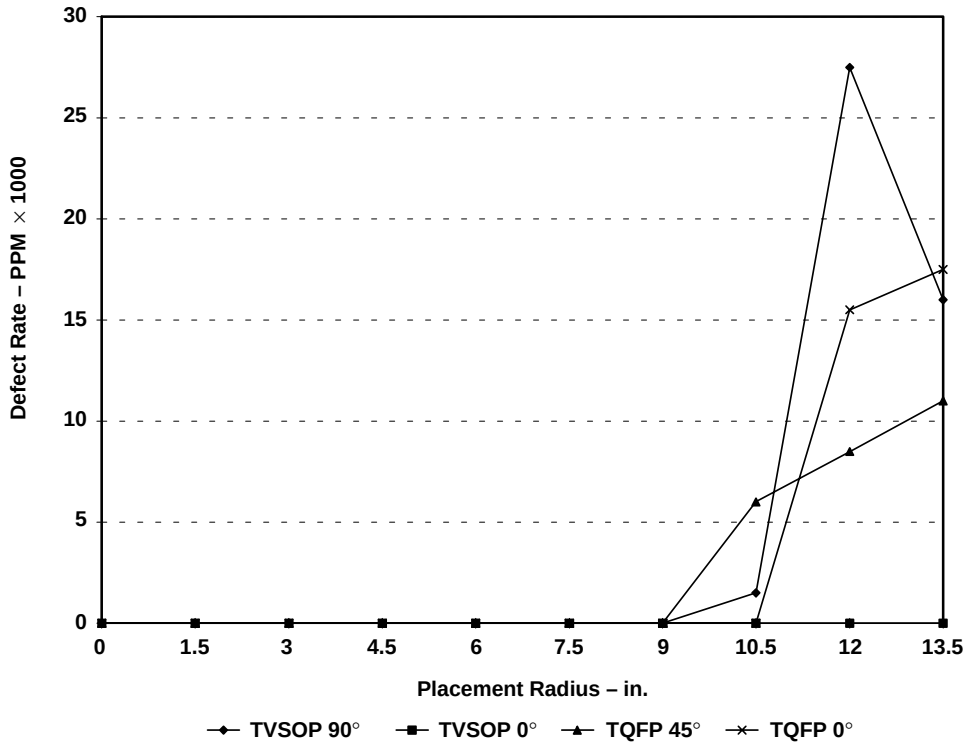


Figure 10. Defect Rate With 5-mil Stencil Thickness

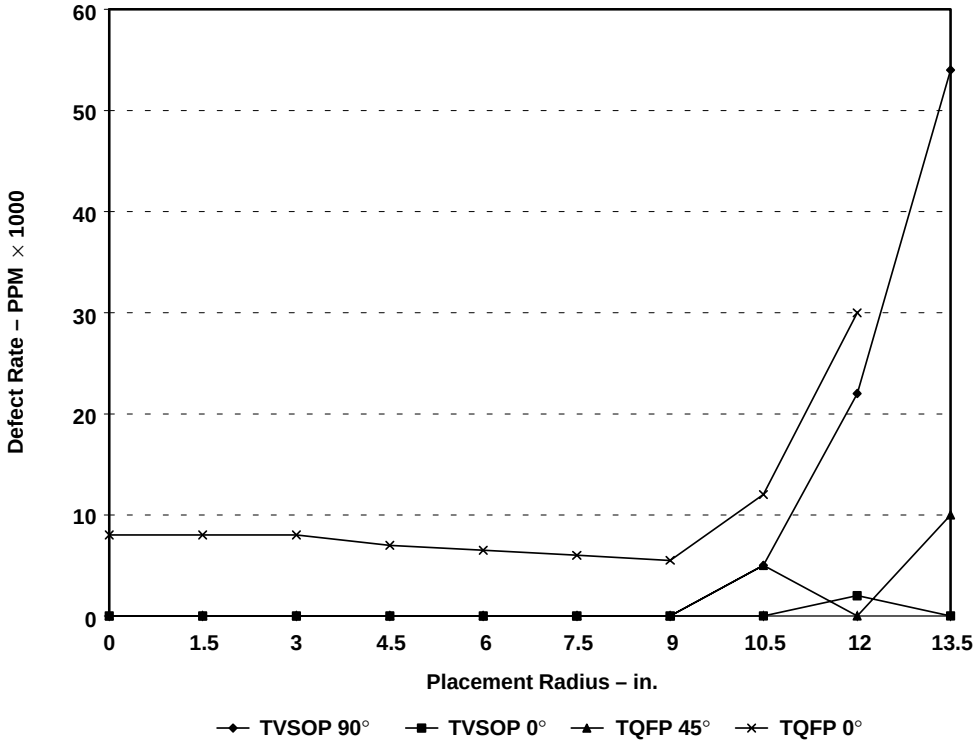
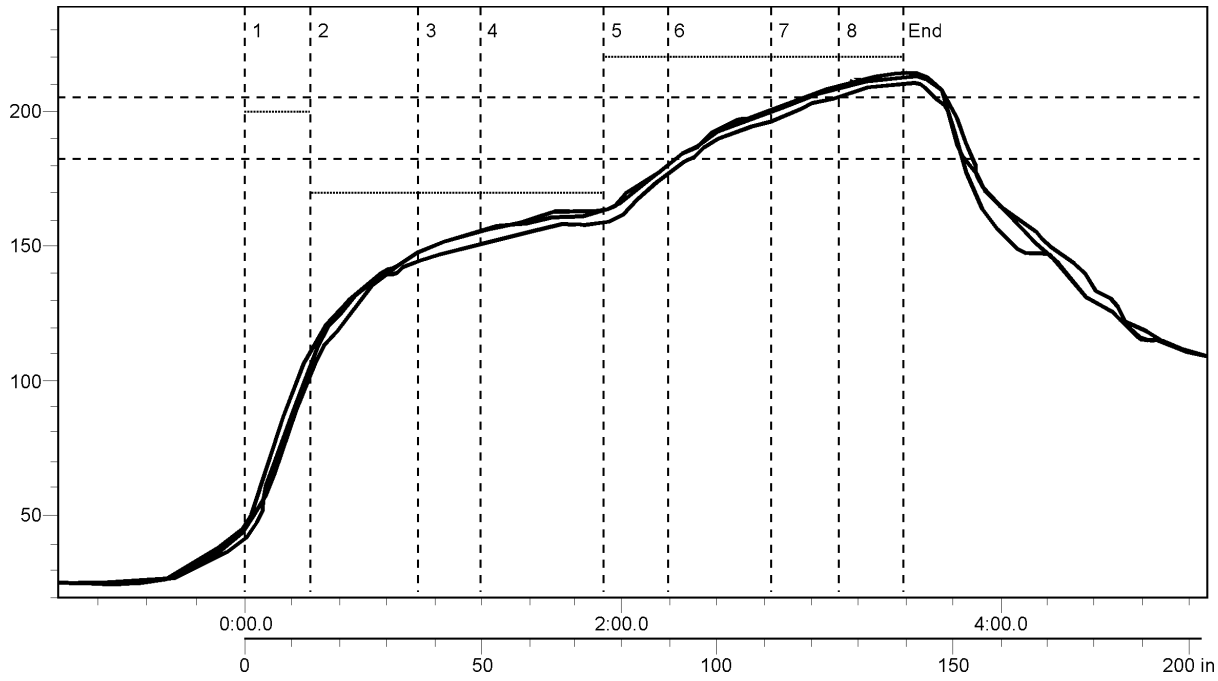


Figure 11. Defect Rate With 6-mil Stencil Thickness



	ZONE	1	2	3	4	5	6	7	8
Speed	Upper	200°	170°	170°	170°	220°	220°	220°	220°
40 (in./min.)	Lower	200°	170°	170°	170°	220°	220°	220°	220°

Figure 12. IR-Reflow Thermal Profile

TVSOP Results From AVEX Electronics

Fifty-six individual double-sided PCMCIA assemblies, eight to a manufacturing panel, for each of two types of plating (gold and ENTEK) were manufactured by AVEX Electronics. Experiments were performed on each of the assemblies to investigate the effect of pad geometry, stencil geometry, and assembly process flow on 0.40-mm (16-mil) lead-pitch devices using high-volume manufacturing equipment.

Pad- and Stencil-Geometry Requirements

The dimensions of the interconnect pad and the stencil aperture have a major effect on the quality of the solder joint. These dimensions must be adhered to during design. The raw card and stencil must maintain these dimensions, otherwise, yields and reliability will be reduced significantly.

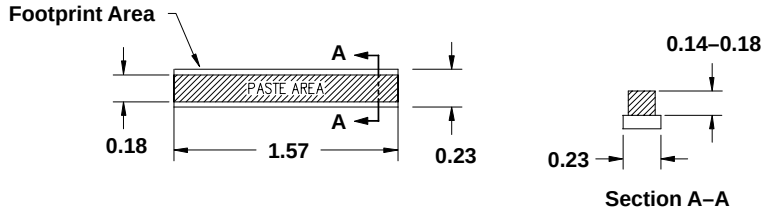
PAD GEOMETRY

Terminal pad length	1.57 mm (0.062 in.)
Terminal pad width	0.23 mm (0.009 in.)
Terminal pad pitch	0.40 mm (0.016 in.)
Pad finish	ENTEK, gold plating

STENCIL GEOMETRY

Stencil opening length	1.57 mm (0.062 in.)
Stencil opening width	0.18 mm (0.007 in.)
Stencil thickness	0.13 mm (0.005 in.)

The dimensions in Figure 13 were used to mount 0.40-mm-pitch devices on PCMCIA cards.



NOTE: All dimensions are in mm.

Figure 13. TVSOP Pad and Stencil Geometry for IR Solder-Reflow Process

Assembly Process

Figure 14 shows the assembly process flow used by AVEX Electronics to mount devices in TVSOP packages on PCMCIA cards.

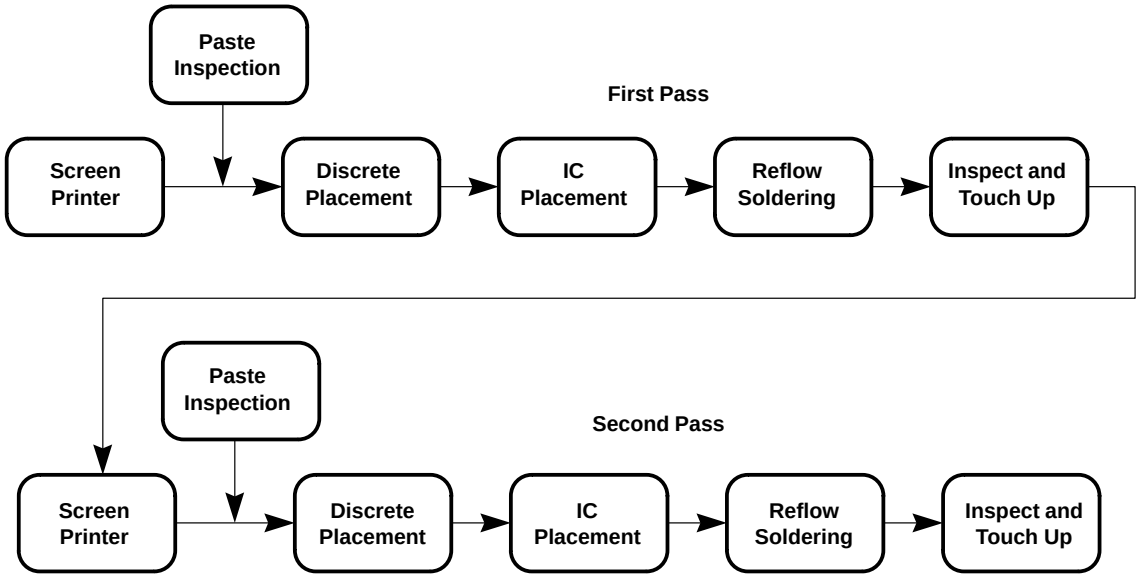


Figure 14. AVEX Process Flow for Mounting TVSOP Devices

The equipment used for the 0.40-mm-lead-pitch mounting evaluation is:

Screen printer	DEK 265GS
Stencil alignment accuracy	±0.0006 in.
Solder paste	Alpha WS609
Solder paste particle size	325–500 (25–45 μm)
Stencil thickness	0.005 in.
Squeegee type	Metal
Paste actual thickness	0.0055 in. to 0.007 in.
Paste inspection	Cyberoptics LSI
Visual placement	KME CM82 (for discrete parts) KME CM92 (for ICs)
Visual accuracy	±0.001 in.
Reflow oven	Heller 1700D

Process Reflow Profile

The recommended and used IR-reflow profile, which is standard for PCMCIA cards, is:

- Preheat: Solder-joint temperature must be gradually increased from ambient to approximately 170°C at a rate not to exceed 2.5°C per second.
- Soak: Solder-joint temperature should be held at approximately 170°C for no more than 50 seconds.
- Reflow: Solder-joint temperature must be increased from 170°C to 210°C at a rate not to exceed 2.5°C per second. Temperature dwell time above 183°C may range from 45 seconds to 65 seconds. Total heating dwell time may be 4 min. to 6 min., depending on thermal inertia and component sensitivity.

Conclusion

Based on the experiments during the qualification run, AVEX Electronics concludes:

- There is no appreciable difference between the gold- and ENTEK-plated PCBs. Choice of PCB plating materials should be based on the solder-paste chemistry.
- Results comparing 7-mil and 8-mil stencil apertures showed that the smaller aperture resulted in a better yield.
- Special consideration must be given to the screen-print process: stencil thickness, aperture size, and PCB support during the second-pass screen-print process.
- Dedicated tooling may be required for machine placement on PCBs less than 0.031 in. thick.
- Component inspection is critical and may require laser-inspection capability on placement equipment.

Solder-Joint Reliability Study

The following photomicrographs are cross sections of leads on TVSOP packages attached to simulated PCMCIA circuit cards.

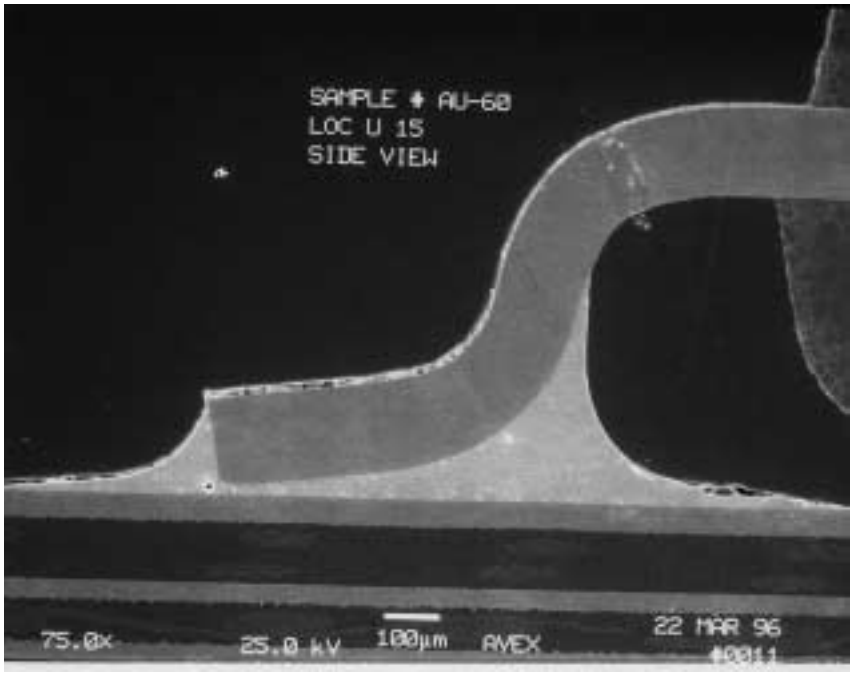


Figure 15. Cross Section of a TVSOP Lead-to-Pad Solder Joint (Side View)

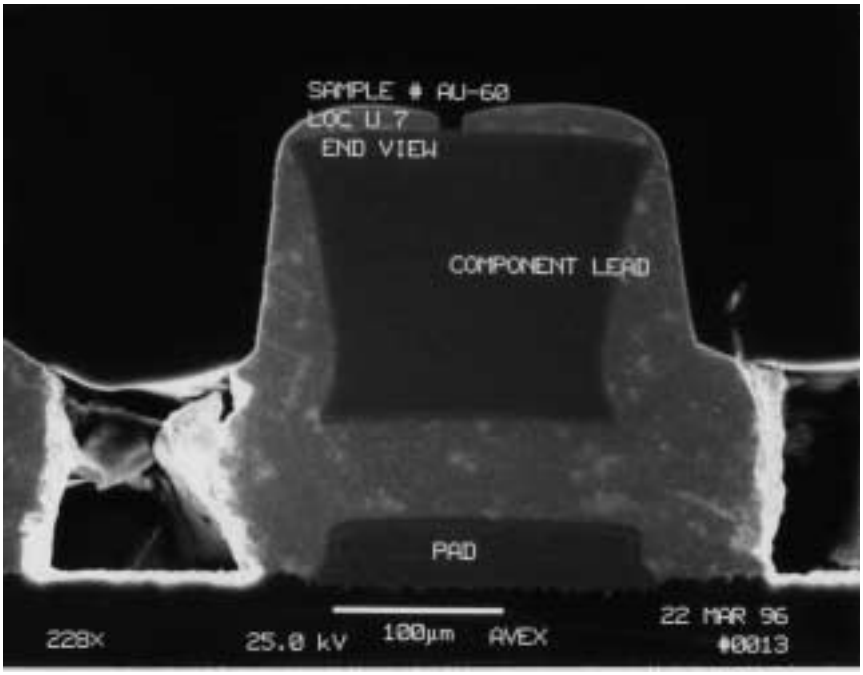


Figure 16. Cross Section of a TVSOP Lead-to-Pad Solder Joint (End View)

Temperature-Cycle Test

This experiment was designed to determine the reliability of TVSOP solder joints after thermal cycling.

No failures were obtained after 1200 thermal cycles between 0°C and 100°C. The following describes the AVEX Electronics thermal cycling test procedure and requirements for the TI PCMCIA environmental stress screening (ESS):

- Support testing of 48 PCBs (12 panels) per run
- 300 cycles (0°C–100°C temperature profile, 15-min. dwell time, 15-min. ramp)
- 900 cycles (0°C–100°C temperature profile, 7.5-min. dwell time, 7.5-min. ramp)
- No power source is required for the unit under test (UUT).
- UUT continuity test requires monitoring of two circuits per UUT.
- No current load required on UUT traces
- Continuous monitoring of UUT status, sample rate of at least one sample per second
- Failures to be removed after return to 25°C

Test Implementation

The PCMCIA panel assemblies were loaded onto an AVEX Electronics standard ESS tray. The tray was modified to hold five panels per tray on metal screws with nylon standoffs. The standard ESS frame wiring was used to provide the I/O interface from the ESS chamber to a monitoring PC system. The PC system monitored the continuity of the UUT traces through a standard digital I/O interface card.

Equipment List

The following equipment was used to perform the TI PCMCIA ESS test:

- ESS chamber, model ESS5-7RWC
- AVEX Electronics ESS frame
- Five AVEX Electronics tray assemblies
- Dell 486/33 PC system
- Metrabyte: PIO96 digital I/O card
- Application-specific chamber-to-PC controller-interface card assembly
- Application-specific test software written in Borland C

Chamber Profile

Table 4 lists the essential characteristics of the ESS5-7RWC test chamber.

Table 4. Characteristics of the ESS5-7RWC Test Chamber

ACTIVITY	TEMPERATURE RANGE	
	0°C–100°C	0°C–100°C
Negative ramp time	15 min.	7.5 min.
Lower dwell time	15 min.	7.5 min.
Positive ramp time	15 min.	7.5 min.
Upper dwell time	15 min.	7.5 min.
Total cycle length	60 min.	30 min.
Number of cycles	300 cycles	900 cycles
Total continuous cycles		1200 cycles

Test Data

The ESS profile was run from February 27, 1996 to April 8, 1996. No test failures were observed. The PC test-data log contained no entries for state changes of the PIO96 digital I/O inputs.

Definitions

UUT Unit under test. A single board assembly that is subjected to testing.

I/O Input/output. Signal lines for stimulus and monitoring of a system or board assembly.

PC system IBM-compatible personal computer system. Used as test controllers and monitoring units.

References

AVEX Electronics, In-Line ESS Lab Setup Wiring Diagram, document no. 4000-14-0159.

AVEX Electronics, ESS Drawer Block Diagram, document no. 4978-08-2034.

TI Reference Information

Thermal Characteristics

Heat is transferred from packages in three ways: conduction, convection, and radiation.

Conduction, the simplest heat-transfer mechanism, is the transfer of kinetic energy from a more excited electron to a nearby electron by vibrations and collisions. It is the primary mode of heat transfer within or between solids. Metals are good conductors because they have a large number of free electrons to encourage collisions. This ability to conduct heat is quantified by a proportionality constant (k), also known as thermal conductivity. The higher the thermal conductivity, the better the material conducts heat. Mold compounds play a role in conduction, but do not contribute as much as copper leadframes.

The second method of heat transfer is convection. This transfer involves the movement of the heated substance. Convection is the primary mode of transfer between solids, liquids, or gases. The rate of convection is dependent on the surface area of the package and on the velocity and physical properties of air. Natural convection is heat transfer caused by induced differences in density that result from the expansion and contraction of air subjected to temperature changes. Forced convection is heat transfer caused by moving a cooling medium across a heat source. Forced airflow increases the rate of heat transfer.

The third mode of heat transfer is radiation. Radiated heat transfers occur due to thermal emission, primarily in the infrared spectrum. Though radiation always exists, it is the only mode of heat transfer between objects separated in a vacuum. Most of the heat transfer will take the form of conduction or convection.

Thermal Parameters

The thermal impedance (k-factor) of a package is defined as the increase in junction temperature above the ambient temperature due to the power dissipated by the device. Thermal impedance is measured in degrees Celsius per watt (°C/W). Two indices are commonly used to describe the thermal characteristics of an integrated-circuit package, θ_{JA} (junction to ambient) and θ_{JC} (junction to case).

Junction temperature Temperature of the die inside the package. Maintaining the junction temperature within a given range is necessary for proper device functionality and for long-term reliability. A lower junction temperature results in increased component reliability due to the reduced possibility of electro-migration or ball-bond intermetallic failure. Table 5 shows this relationship.

Table 5. Junction Temperature Versus Long-Term Reliability Comparison

JUNCTION TEMPERATURE	FAILURE RATE† (%)
100°C	0.02
110°C	1
120°C	11
130°C	46
140°C	80
150°C	96

† Failure rate at 100,000 hours

Case temperature Temperature on the package surface measured at the center of the top of the package by an attached K-type thermocouple.

Ambient temperature Temperature of the surrounding air. It is used usually as a reference point to calculate the junction or case temperature. It is measured at some distance away from the device.

Thermal Measurements

In making comparisons among parameters, it is important to understand how the parameters are measured and under what test conditions. Thermal measurement standards that have been developed by JEDEC will lead to a more consistent correlation of thermal performance among IC vendors. The JC15 JEDEC committee was formed to develop standards for the thermal measurement and modeling of IC packages. Perhaps the most important factor regarding variability in thermal measurements is the design of the thermal test board. Table 6 provides the JEDEC dimensions of dual-in-line packages with body length less than 28 mm and external lead pitch equal to or less than 0.40 mm.

Table 6. JEDEC Thermal Test Board Specifications

DIMENSION	SPECIFICATION
Board thickness	1.57 mm (0.062 in.)
Board dimension (package length < 28 mm)	76.2 mm × 114.3 mm (3.0 in. × 4.5 in.)
Board material	FR-4 epoxy glass
Fan-out trace length (minimum)	25 mm (0.98 in.)
Fan-out trace position	Centered in 76.2 mm × 76.2 mm
Trace thickness	0.071 mm (0.0028 in.) ±20%
Trace width for 0.40-mm lead pitch	0.40 mm (0.016 in.)

Thermal modeling at TI uses an internally developed software package, ThermCAL. The software divides the package into a large number of small elements (meshing), then calculates temperature for each element based on temperatures of the surrounding elements.

TVSOP Power Dissipation and Thermal-Impedance Characteristics

Device junction temperature is determined mainly by the IC power consumption, the surrounding temperature, and the thermal impedance between the junction and the atmosphere. The relationship is expressed by equation 1.

$$T_J = T_A + (\theta_{JA})P \quad \textbf{(1)}$$

Where:

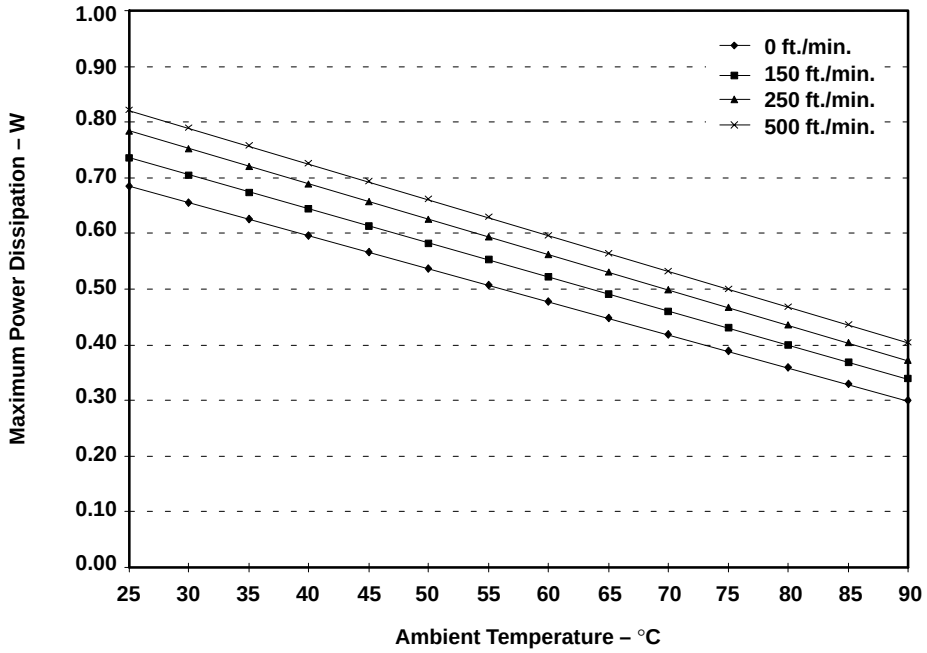
T_J = junction temperature
T_A = ambient temperature
P = power
θ_{JA} = thermal impedance

Thermal impedance is the package's resistance to heat dissipation and is related inversely to thermal conductivity (k). When a device reaches a state of equilibrium, the electrical power delivered is equal to the thermal heat dissipated. This thermal energy is in the form of heat and is given off to the surroundings. The maximum allowable power consumption at a given surrounding temperature is computed using the maximum junction temperature for the chip given in equation 2.

$$P = \frac{(T_J - T_A)}{\theta_{JA}} \quad \textbf{(2)}$$

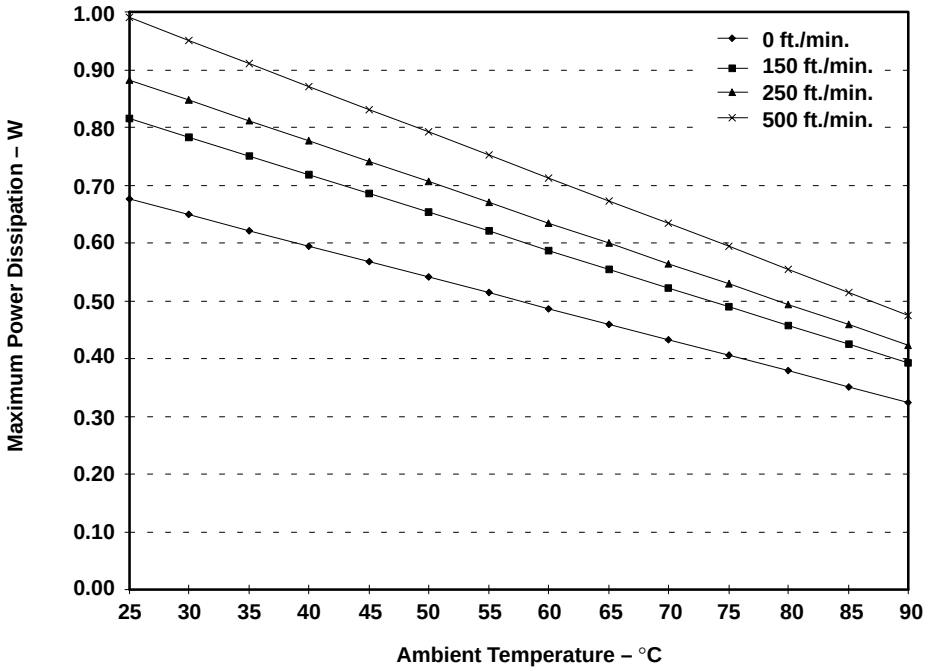
Figures 17 through 24 show the derating curves that were obtained from equation 2 using thermal-impedance values determined by using JEDEC-standard boards with 1000-mil trace length and a maximum junction temperature of 150°C. The main factors affecting thermal impedance are material selection, package geometry, airflow, and length and width of the traces on the board.

Natural convection, in many cases, does not adequately dissipate heat. The solution is to induce airflow across a device. The data for a TVSOP 48-pin package shows that changing from natural convection to forced convection can decrease thermal impedance by as much as 25%.



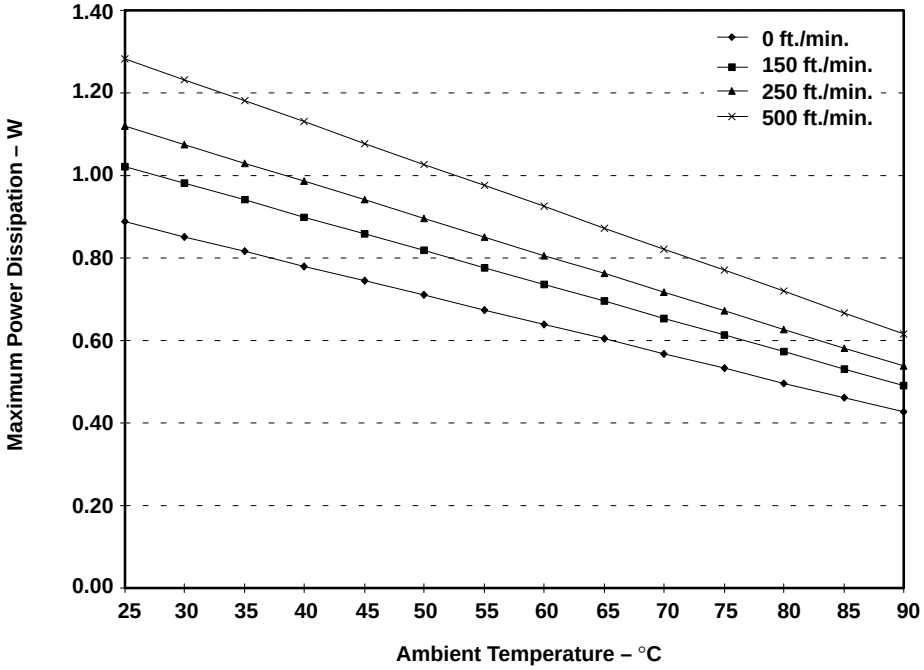
Air velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	182	166	160	150

Figure 17. 14-Pin TVSOP Derating Curves



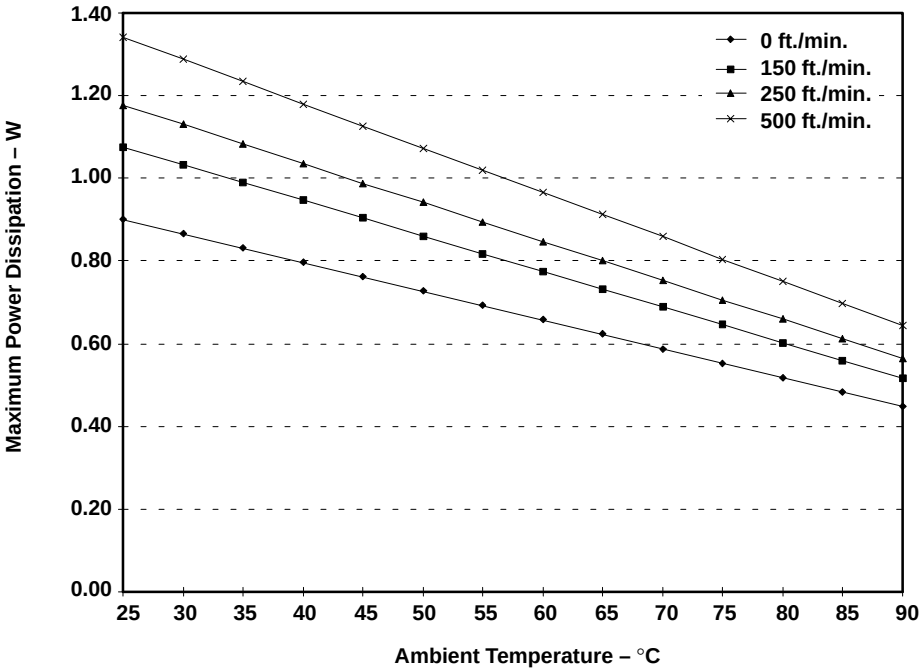
Air velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	182	153	142	126

Figure 18. 16-Pin TVSOP Derating Curves



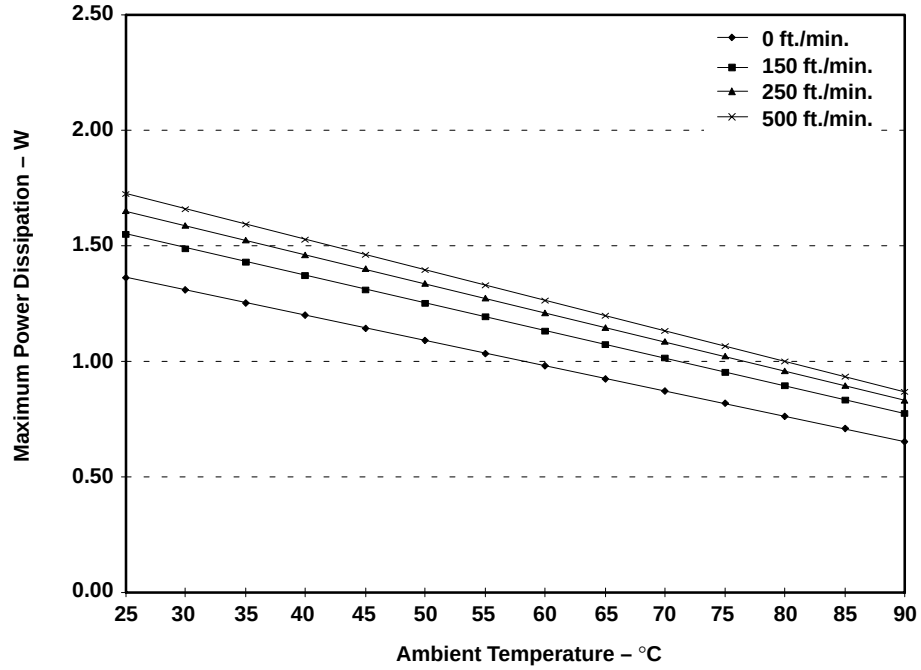
Air velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	146	122	112	97

Figure 19. 20-Pin TVSOP Derating Curves



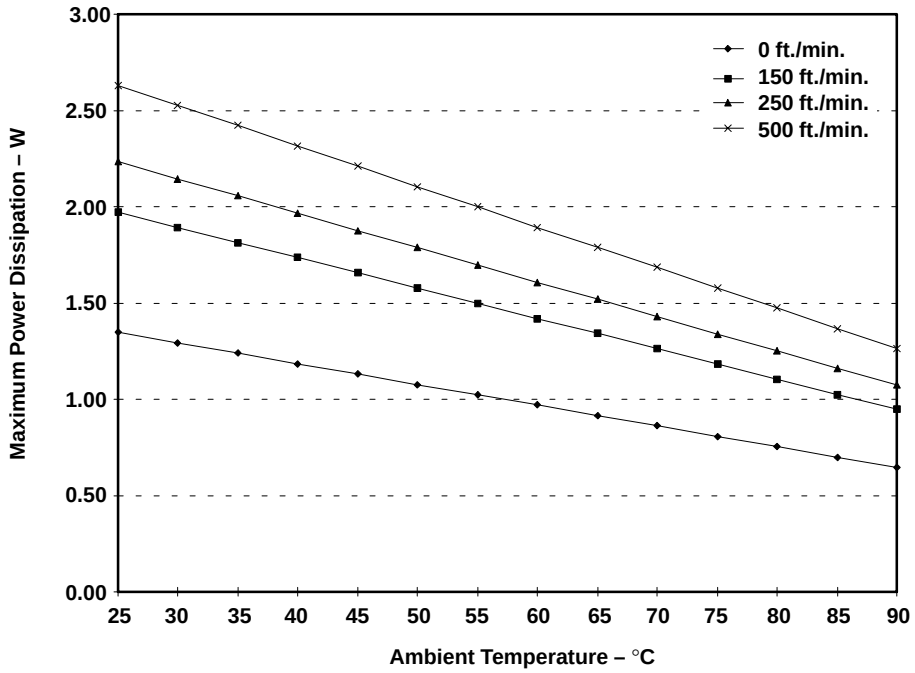
Air velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	139	116	106	93

Figure 20. 24-Pin TVSOP Derating Curves



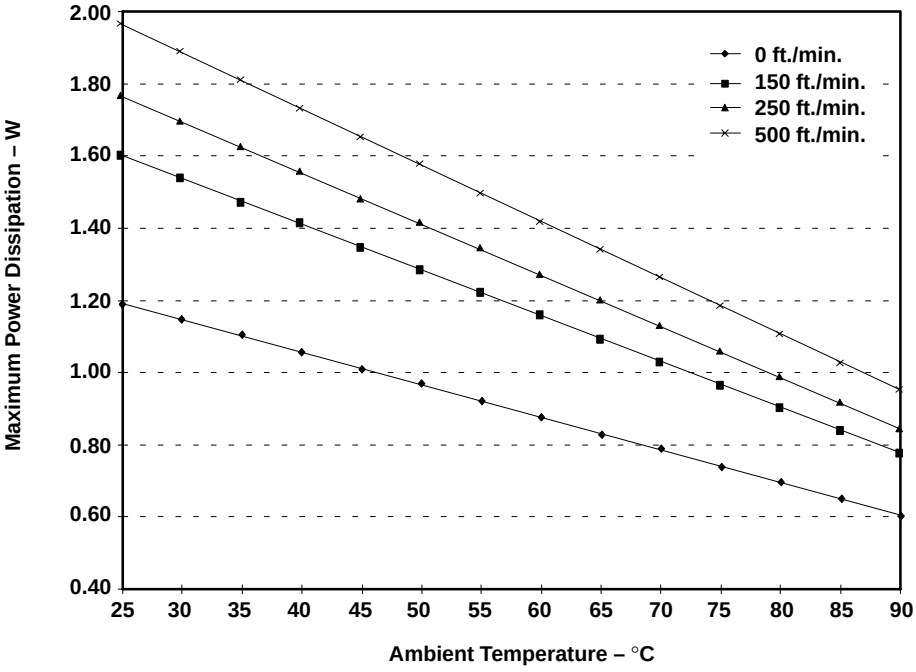
Air velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	93	81	77	71

Figure 21. 48-Pin TVSOP Derating Curves



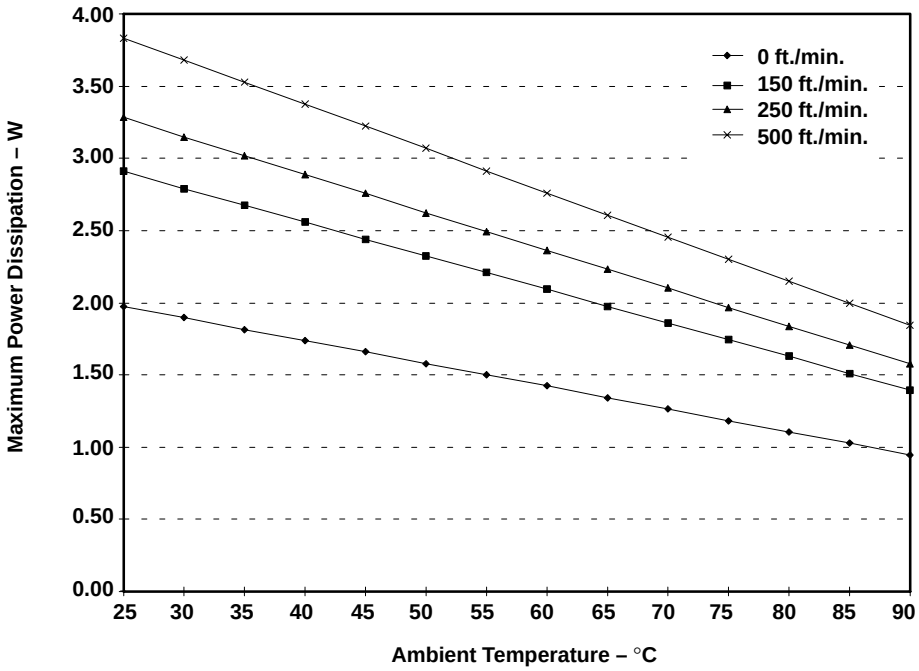
Air velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	86	65	57	48

Figure 22. 56-Pin TVSOP Derating Curves



Air velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	106	78	72	64
θ_{JC} (°C/W)	23			

Figure 23. 80-Pin TVSOP Derating Curves



Air velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	63	43	38	33

Figure 24. 100-Pin TVSOP Derating Curves

Power Calculation[1]

When calculating the total power consumption of a circuit, both static and dynamic currents must be taken into account. Bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL}, I_{CCH}, or I_{CCZ}), while a CMOS device has a single value for I_{CC}. These values can be found in the data sheets. TTL-compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not switched off completely. This value, known as ΔI_{CC}, also is provided in the data sheet.

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is C_{pd}, which is listed in the data sheet and obtained using equations 3 and 4:

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad \textbf{(3)}$$

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I} \quad \textbf{(4)}$$

[1] The information presented in this section is a modified form of the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application report, literature number SCZA005.

To explain the C_{pd} and the method of calculating dynamic power calculation, see Table 7, which indicates the C_{pd} test conditions for AHC devices. The symbols used in Table 7 are:

V = V_{CC} (5 V)
G = ground (0 V)
1 = high logic level = V_{CC} (5 V)
0 = low logic level = ground (0 V)
X = don't care: 1 or 0, but not switching
C = 50% duty-cycle input pulse (1 MHz) (see Figure 25)
D = 50% duty-cycle input (1/2 frequency) out-of-phase input pulse (see Figure 25)
S = standard ac output load (50 pF to GND)

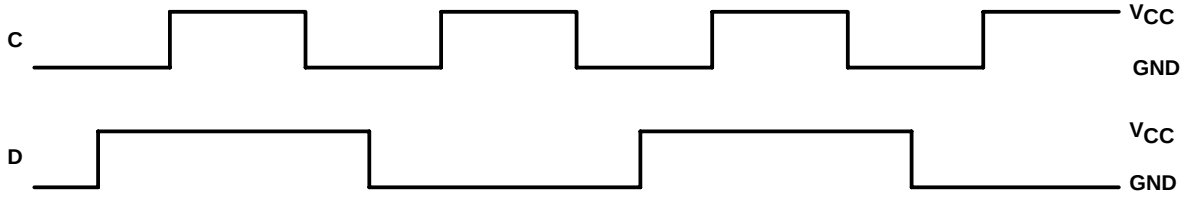


Figure 25. Input Waveform

Table 7 shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations explained in the following sections.

Table 7. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN NO.																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switching, but with no active clock signal
‡ All bits switching

CMOS

CMOS-Level Inputs

Static-power consumption can be calculated using equation 5.

$$P_S = V_{CC} \times I_{CC} \quad \textbf{(5)}$$

The dynamic-power consumption of a CMOS device is calculated by adding the transient-power consumption and capacitive-load power consumption.

Transient-Power Consumption

The transient power is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This power is a result of the current required to charge the internal nodes (*switching current*), plus the current that flows from V_{CC} to GND when the p-channel and n-channel transistors turn on briefly at the same time during the logic transition (*through current*). The frequency at which the device is switching, plus the rise and fall time of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible in comparison to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the device and the charge and discharge current of the load capacitance. The transient-power consumption can be calculated using equation 6.

$$P_T = C_{pd} \times {V_{CC}}^2 \times f_I \times N_{SW} \quad \textbf{(6)}$$

In case of single-bit switching, N_{SW} in equation 6 becomes 1.

Capacitive-Load Power Consumption

Additional power is consumed in charging of external load capacitance and is dependent on switching frequency. Equation 7 can be used to calculate this power while all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times {V_{CC}}^2 \times f_O \times N_{SW} \text{ } (C_L \text{ is the load per output}) \quad \textbf{(7)}$$

In case of different loads and different output frequencies at all outputs, equation 8 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times {V_{CC}}^2 \quad \textbf{(8)}$$

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions, and is expressed in equation 9 (single-bit-switching case) and 10 (multiple-bit switching with variable load and variable output frequencies).

$$P_D = \left(C_{pd} \times f_I \times {V_{CC}}^2\right) + \left(C_L \times f_O \times {V_{CC}}^2\right) \quad \textbf{(9)}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma\left(C_{Ln} \times f_{On}\right)\right]{V_{CC}}^2 \quad \textbf{(10)}$$

Total power consumption with a CMOS-level input is the sum of static and dynamic-power consumption.

TTL-Level Inputs

Similarly, with TTL-level inputs, both static- and dynamic-power consumption can be calculated using equations 11, 12, and 13.

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad \textbf{(11)}$$

$$P_D = \left(C_{pd} \times f_I \times {V_{CC}}^2\right) + \left(C_L \times f_O \times {V_{CC}}^2\right) \text{ (single bit switching)} \quad \textbf{(12)}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma(C_{Ln} \times f_{On})\right]{V_{CC}}^2 \quad \textbf{(13)}$$

(multiple bits switching with variable load and frequency)

BiCMOS

Static Power

$$P_S = V_{CC}\left\{DC_{en}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\right\} \quad \textbf{(14)}$$

Where:

ΔI_{CC} = 0 for bipolar devices

NOTE:
For a continuous waveform at 50% duty cycle, DC_{en} = 1.

Equation 14 becomes:

$$P_S = V_{CC}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] \quad \textbf{(15)}$$

NOTE:
If half of the time the waveform is high and half of the time the waveform is low and the waveform is switching continuously, $\Rightarrow (N_H = N_L = 1/2\ N_T)$, P_S becomes:

$$P_S = \left(\frac{V_{CC}}{2}\right)(I_{CCH} + I_{CCL}) \quad \textbf{(16)}$$

Dynamic Power

$$P_D = (DC_{em} \times N_{SW} \times V_{CC} \times f \times I_{CCD})\ \text{Condition is } 50\ \text{pF} \parallel 500\ \Omega \quad \textbf{(17)}$$

I_{CCD} is calculated with 50 pF || 500 Ω and with a given number of outputs switching.

NOTE:
For a continuous waveform at 50% duty cycle, DC_{en} = 1.

Dynamic power with external capacitance:

$$P_D = DC_{en} \times N_{SW} \times V_{CC} \times f \times (V_{OH} - V_{OL}) \times (C_L - 50\ \text{pF}) + DC_{en} \times N_{SW} \times V_{CC} \times f \times I_{CCD} \quad \textbf{(18)}$$

I_{CCD} is calculated with 50 pF || 500 Ω and with a given number of outputs switching.

Power also is consumed by the upper output driver due to the output resistor (500 Ω in most load circuits for outputs in the data sheet). This power is very small, but needs to be included in the dynamic power-consumption calculation. Equation 19 is used to calculate this power consumption.

$$P_{\_Res} = (V_{CC} - V_{OH}) \times \frac{V_{OH}}{R} \quad \textbf{(19)}$$

NOTE:
Assume that the output waveform always is at logic high and is not frequency dependent.

Therefore, total dynamic-power consumption is:

$$P_{D\_TOT} = P_D + P_{\_Res} \quad \textbf{(20)}$$

Finally, total power consumption can be calculated as:

$$P_{\_Total} = P_{D\_TOT} + P_S \quad \textbf{(21)}$$

Where:

V_{CC} = supply voltage (V)
I_{CC} = power-supply current (A) (from the data sheet)
I_{CCL} = power-supply current when outputs are in low state (A) (from the data sheet)
I_{CCH} = power-supply current when outputs are in high state (A) (from the data sheet)
I_{CCZ} = power-supply current when outputs are in high-impedance state (A) (from the data sheet)
ΔI_{CC} = power-supply current when one input is at a TTL level (A) (from the data sheet)
DC_{en} = % duty cycle enabled (50% = 0.5)

DC_d = % duty cycle of the data (50% = 0.5)
N_H = number of outputs in high state
N_L = number of outputs in low state
N_{sw} = total number of outputs switching
N_T = total number of outputs
N_{TTL} = number of inputs driven at TTL levels

fi = input frequency (Hz)
f_O = output frequency (Hz)
f = operating frequency (Hz)
V_{OH} = output voltage in high state (V)
V_{OL} = output voltage in low state (V)
C_L = external load capacitance (F)
I_{CCD} = slope of the I_{CC} versus frequency curve (A/Hz × bit)

$C_{L(eff)}$ = effective load capacitance (F)
f_O/f_I = ratio of output and input frequency (Hz)
P_T = transient-power consumption
P_D = dynamic-power consumption
P_S = static-power consumption
$P_{\_Res}$ = power consumption due to output resistance
P_{D_TOT} = total dynamic-power consumption
$P_{\_Total}$ = total power consumption

C_{PD} = dynamic power-dissipation capacitance (F)
P_L = capacitive-load power consumption
Σ = sum of n different frequencies and loads at n different outputs
f_{On} = all different output frequencies at each output numbered 1 through n (Hz)
C_{Ln} = all different load capacitances at each output numbered 1 through n

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

The total power calculated using these equations should be less than the package power dissipation mentioned in the data sheets. Otherwise, the device may not function properly.

Electrical Characteristics

Electrical characteristics of the IC packages used at TI normally are determined by computer-modeling programs developed in-house (PACED)[2] or by using commercially available software. Electrical parameters are measured in our laboratories to verify the modeling data. The measurement methods follow the EIA/JEDEC Guideline EIA/JEP123, and include the use of impedance meters, time-domain reflectometers (TDRs), and network analyzers.

The electrical modeling program calculates the following parameters:

- Resistance (R) - dc or with high-frequency effects
- Capacitance (C) - includes loading and coupling capacitance
- Inductance (L) - includes mutual and self inductance

The RLC parameters are available for each pin of the package being modeled or reported in tabular form as a range of values for the longest to the shortest leads. A SPICE input file for the package also is created by the modeling program. The SPICE file is produced in two formats: a lumped-parameter file, where each lead and bond wire is represented by one RLC element, or a distributed-parameter file, where the lead and bond wire is represented by many RLC elements. The distributed-parameter version represents varying sections of the lead more accurately and is used for higher-frequency simulations.

The characteristic impedance (Z_O) is calculated for each section of the lead and bond wire. This may be important if impedance matching is a consideration in the design for high-speed applications.

Electrical Parameters

Resistance

The resistance of an IC package conductor can be significant as a source of IR voltage drop in certain package families. In molded packages with copper lead frames (ρ = 1.7 $\mu\Omega$-cm)[3], most of the resistance is due to the bond wire because of the very small cross section (100 mΩ/0.1 in.). If Alloy 42 lead frames (ρ = 48.8 $\mu\Omega$-cm) are used, the resistance of the lead can be several-hundred mΩ and, therefore, much higher than the wire bonds. Cofired ceramic packages tend to have higher conductor resistance because the material used is a tungsten/glass mixture (ρ = 25 $\mu\Omega$-cm). Other families that may have significant trace resistance include the thin-film processed interconnects, as in some multiple-chip modules, due to the low thickness of the conductors.

Capacitance

Capacitance is a function of lead-surface proximity and the dielectric constant of the insulating material. These surfaces include the conductor leads, power and ground planes (if any), and the presence of floating metal, such as heat spreaders. The electrical models for molded-lead-frame packages assume a ground plane exists in the PC board on which it is mounted. The capacitance to ground usually is very small for these style packages and most of the loading capacitance is due to interlead coupling. This coupling capacitance can be a source of crosstalk noise from lead to lead.

The relative dielectric constant can vary widely among package families. Mold compounds have relative dielectric constants of 4 to 5, alumina ceramic packages range from 9 to 10, and some lead-zinc-borate solder glass materials can be as high as 33.

Changing the proximity of one conductor to another can affect the coupling capacitance to a third conductor. This is exploited in some designs by moving the ground plane closer to the conductor leads to reduce the interlead coupling.

Inductance

Inductance is a function of the current distribution in the package and the relative permeability of the conductor material. Because of the dependence on current distribution, the effective inductance of a lead depends on the ground return path in the system. Moving a ground plane closer to the conductor lead decreases the magnetic field around the lead and reduces the mutual and self-inductance to the other leads. The lead width also significantly influences self inductance. Minimum inductance is achieved when the ratio of the lead width to the height of lead from ground plane is maximized. Bond wires are a significant source of inductance because of their very narrow effective width.

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2 PACED: Process Automation Center Electrical Design software

3 ρ (rho): Electrical resistivity

The proximity of floating, nonferrous metal (as in heat spreaders) also decreases the effective inductance due to eddy currents flowing in these structures. The eddy currents flow in the opposite direction from the lead currents, reducing the total magnetic field.

As frequency increases, the self inductance of the package lead decreases. This is caused by the reduction of the magnetic field internal to the lead by the skin effect (current density greater near the surface of the conductor and less in the center). For copper lead frames, this effect is very small and usually can be ignored. For magnetic lead frame materials with higher relative permeability, such as Alloy 42, the frequency dependence is large. However, the fast rise times of modern devices dictate a high-frequency bandwidth for the package and the Alloy 42 self-inductance approaches that of copper.

Solutions for reducing the effective inductance, especially for ground and power leads, include increasing the number of lead paths for that function and multiple-wire bonding to the same package pin. Doubling the conductors, however, does not reduce the inductance by half. The mutual inductance between the leads prevents this from happening and, if the leads are tightly coupled, the inductance may only decrease by 20 percent or so. To maximize the reduction of the effective inductance, the leads serving the same function, such as ground or power, should be as far apart as possible.

TVSOP Electrical Data

Figures 26 through 29 show the minimum and maximum range of capacitance (C) and inductance (L) for 14-pin to 56-pin narrow-body TVSOP packages and 80-pin and 100-pin wide-body TVSOP packages. Table 8 summarizes TVSOP electrical data.

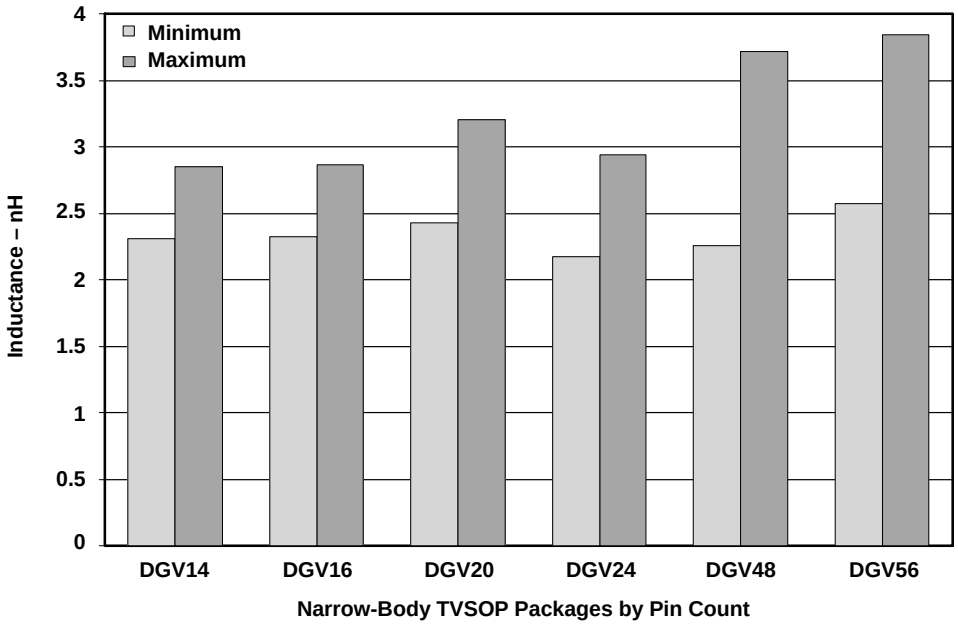


Figure 26. TVSOP Package Inductance (14, 16, 20, 24, 48, and 56 Pins)

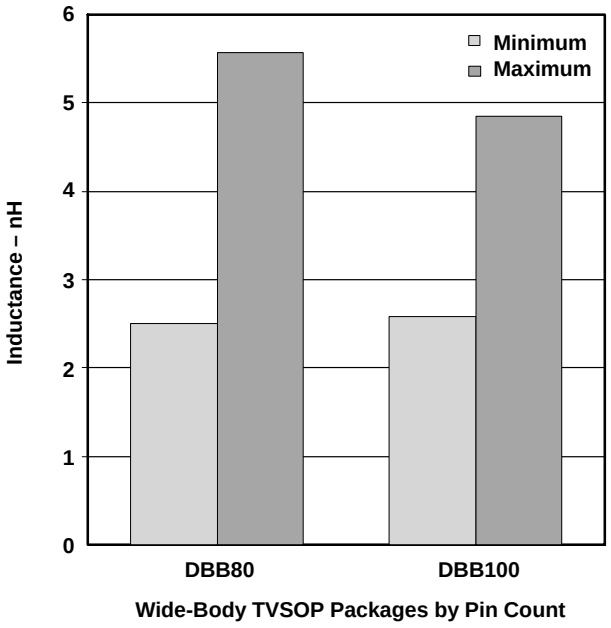


Figure 27. TVSOP Package Inductance (80 and 100 Pins)

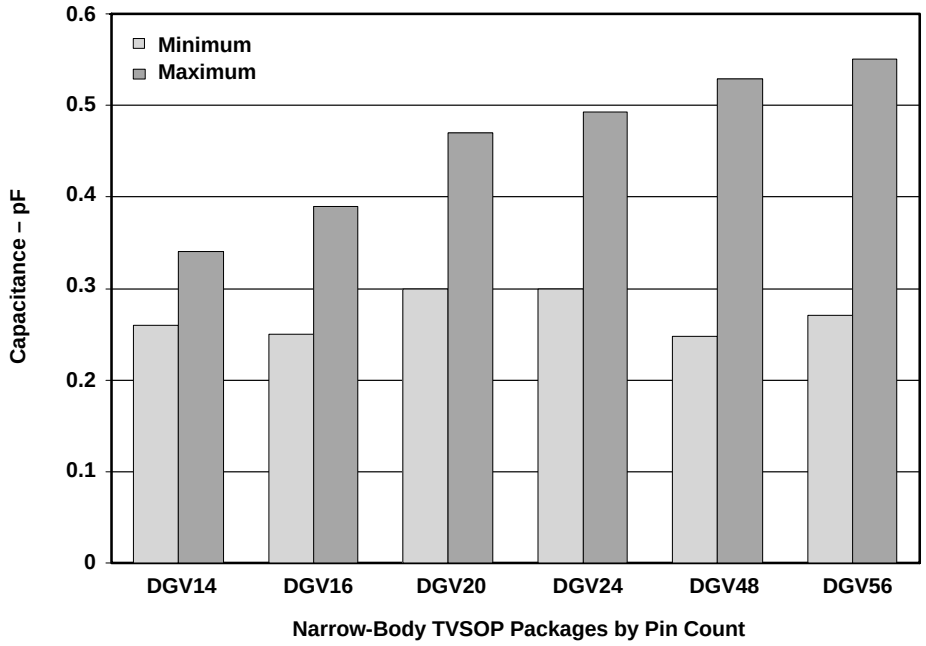


Figure 28. TVSOP Package Capacitance (14, 16, 20, 24, 48, and 56 Pins)

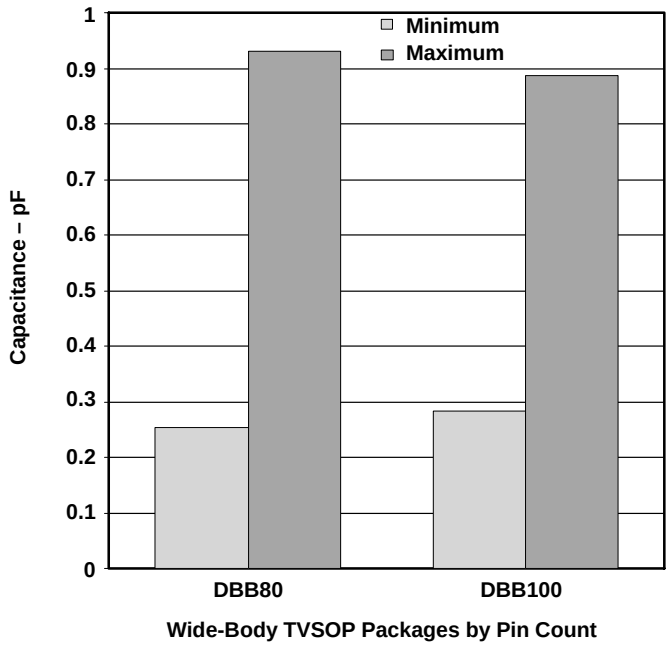


Figure 29. TVSOP Package Capacitance (80 and 100 Pins)

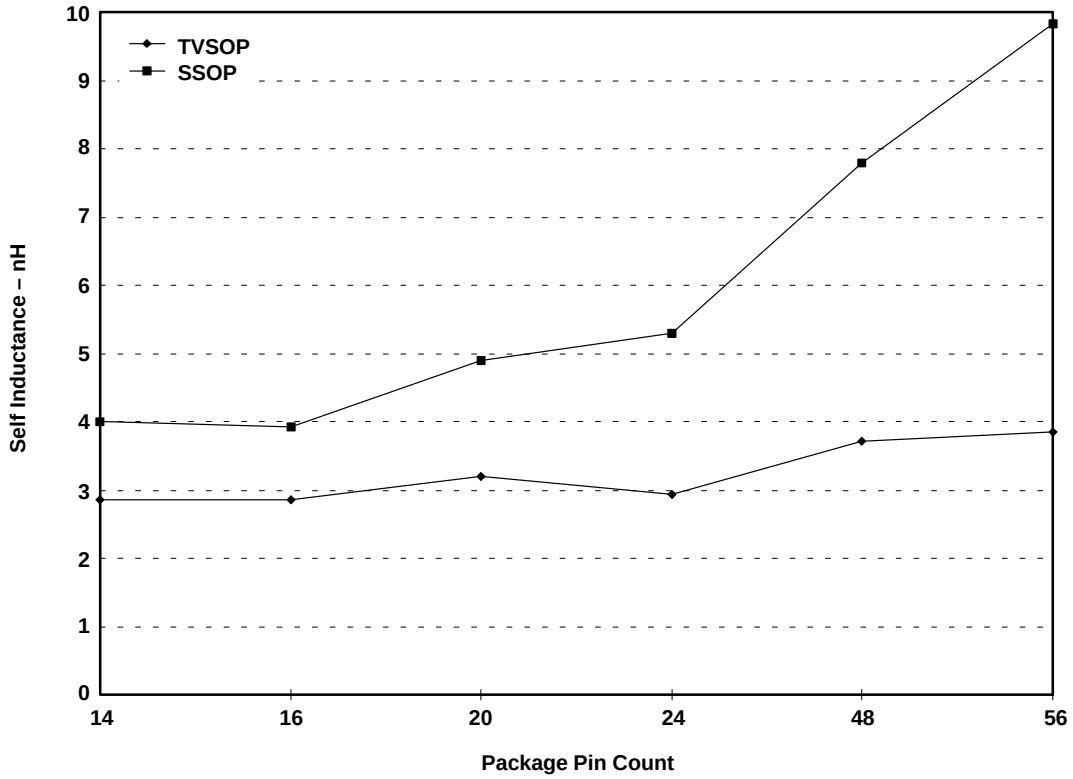


Figure 30. TVSOP and SSOP Self-Inductance Comparison

Table 8. Summary of TVSOP Electrical Data

TVSOP PACKAGE	RESISTANCE (Ω)	INDUCTANCE L_S (nH)	CAPACITANCE C_L (pF)
DGV 14	0.037–0.040	2.31–2.85	0.26–0.34
DGV 16	0.029–0.040	2.32–2.86	0.25–0.39
DGV 20	0.039–0.041	2.43–3.21	0.30–0.47
DGV 24	0.035–0.040	2.17–2.94	0.30–0.49
DGV 48	0.027–0.045	2.26–3.71	0.28–0.53
DGV 56	0.050–0.062	2.57–3.84	0.27–0.55
DBB 80	0.042–0.083	2.50–5.57	0.25–0.93
DBB 100	0.046–0.066	2.58–4.9	0.28–0.89

NOTES: 1. Copper-based leadframe and gold bond wire
2. Electrical values based on maximum die fit on packages
3. Ground plane is a single layer (no power or ground planes) on top of the PCB.

L_S = self-inductance, C_L = load capacitance

Table 9. 14-Pin TVSOP Package Reliability Results

	REQUIRED SS PER NUMBER OF FAILURES	AABT126DGV ACTUAL SS PER NUMBER OF FAILURES
Operating life static test† (125°C, 1000 hours)	116/0	116/0
Biased humidity† (85°C/85% RH, 1000 hours)	116/0	116/0
Temperature cycle test† (–65°C to 150°C, 1000 cycles)	116/0	116/0
Autoclave† (121°C, 15 psi, 240 hours)	76/0	76/0
Solderability	22/0	22/0
Solder heat	22/0	22/0
Lead fatigue	22/0	22/0
Lead pull to destruction	22/0	22/0
Lead finish adhesion	15/0	15/0
Flammability (UL)	5/0	5/0
Flammability (IEC)	5/0	5/0
Salt atmosphere	22/0	22/0
X-ray (top view only)	5/0	5/0
Manufacturability	Pass/fail	Pass
Physical dimensions	5/0	5/0
Moisture sensitivity (level 1)	12/0	12/0

† Condition level 1 preconditioning sequence:
1. 85°C at 85% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a 1-hr. 25°C drying period

Table 10. 20-Pin TVSOP Package Reliability Results

	REQUIRED SS PER NUMBER OF FAILURES	AABT126DGV ACTUAL SS PER NUMBER OF FAILURES
Operating life static test† (125°C, 1000 hours)	116/0	116/0
Biased humidity† (85°C/85% RH, 1000 hours)	116/0	116/0
Temperature cycle test† (–65°C to 150°C, 1000 cycles)	116/0	116/0
Autoclave† (121°C, 15 psi, 240 hours)	76/0	76/0
Solderability	22/0	22/0
Solder heat	22/0	22/0
Lead fatigue	22/0	22/0
Lead pull to destruction	22/0	22/0
Lead finish adhesion	15/0	15/0
Flammability (UL)	5/0	5/0
Flammability (IEC)	5/0	5/0
Salt atmosphere	22/0	22/0
X-ray (top view only)	5/0	5/0
Manufacturability	Pass/fail	Pass
Physical dimensions	5/0	5/0
Moisture sensitivity (level 1)	20/0	20/0

† Condition level 2 preconditioning sequence:
1. 85°C at 85% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a 1-hr. 25°C drying period

Table 11. 48-Pin TVSOP Package Reliability Results

	REQUIRED SS PER NUMBER OF FAILURES	ABT16640DGV ACTUAL SS PER NUMBER OF FAILURES
Operating life static test† (125°C, 1000 hours)	116/0	116/0
Biased humidity† (85°C/85% RH, 1000 hours)	116/0	116/0
Storage life test† (150°C, 1000 hours)	90/0	90/0
Temperature cycle test† (–65°C to 150°C, 1000 cycles)	116/0	116/0
Autoclave† (121°C, 15 psi, 240 hours)	76/0	76/0
Solderability	44/0	44/0
Solder heat	44/0	44/0
Lead fatigue	6/0	6/0
Lead pull to destruction	6/0	6/0
Lead finish adhesion	6/0	6/0
Flammability (UL)	10/0	10/0
Flammability (IEC)	10/0	10/0
Salt atmosphere	44/0	44/0
Resist solvent	24/0	24/0
X-ray (top view only)	10/0	10/0
Manufacturability	Pass/fail	Pass
Physical dimensions	10/0	10/0
Moisture sensitivity (level 1)	20/0	20/0

† Condition level 2 preconditioning sequence:
1. 85°C at 85% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a 1-hr. 25°C drying period

Table 12. 80-Pin TVSOP Package Reliability Results

	REQUIRED SS PER NUMBER OF FAILURES	ALVC16901DBB ACTUAL SS PER NUMBER OF FAILURES
Operating life static test† (125°C, 1000 hours)	120/0	120/0
Biased humidity† (85°C/85% RH, 1000 hours)	116/0	116/0
Storage life test† (150°C, 1000 hours)	45/0	45/0
Temperature cycle test† (–65°C to 150°C, 1000 cycles)	120/0	120/0
Autoclave† (121°C, 15 psi, 240 hours)	78/0	78/0
Lead fatigue	66/0	66/0
Lead pull to destruction	3/0	3/0
Lead finish adhesion	5/0	5/0
Salt atmosphere	24/0	24/0
X-ray (top view only)	6/0	6/0
Manufacturability	Pass/fail	Pass
Physical dimensions	6/0	6/0
Moisture sensitivity (level 1)	12/0	12/0

† Condition level 1 preconditioning sequence:
1. 85°C at 85% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a 1-hr. 25°C drying period

Delivery of the TVSOP to TI Customers

Moisture Sensitivity of the TVSOP

Moisture sensitivity describes the characteristic of some plastic surface-mount packages to absorb sufficient moisture from their environment to cause the package to crack when exposed to the extreme temperature of reflow soldering. During solder reflow (IR, VPR, or wave solder), flash vaporization of the absorbed moisture causes high stress, resulting in internal cracking or delamination between the chip and the leadframe chip pad. Packages are tested for moisture sensitivity in accordance with JESD A112. Those packages that fail to meet Level 1 are designated as moisture sensitive and are dry packed. Table 13 describes the recommended floor life of the package after it is removed from the sealed dry-pack bag prior to soldering. The floor life can be extended by sealing the dry-pack bag as soon as possible after removing the components to be used.

Table 13. TVSOP Floor Life

LEVEL	FLOOR LIFE	
	CONDITIONS	DURATION
1	≤30°C at 90% RH	Unlimited
2	≤30°C at 60% RH	1 year
3	≤30°C at 60% RH	168 hours
4	≤30°C at 60% RH	72 hours
5	≤30°C at 60% RH	24 hours
6	≤30°C at 60% RH	6 hours

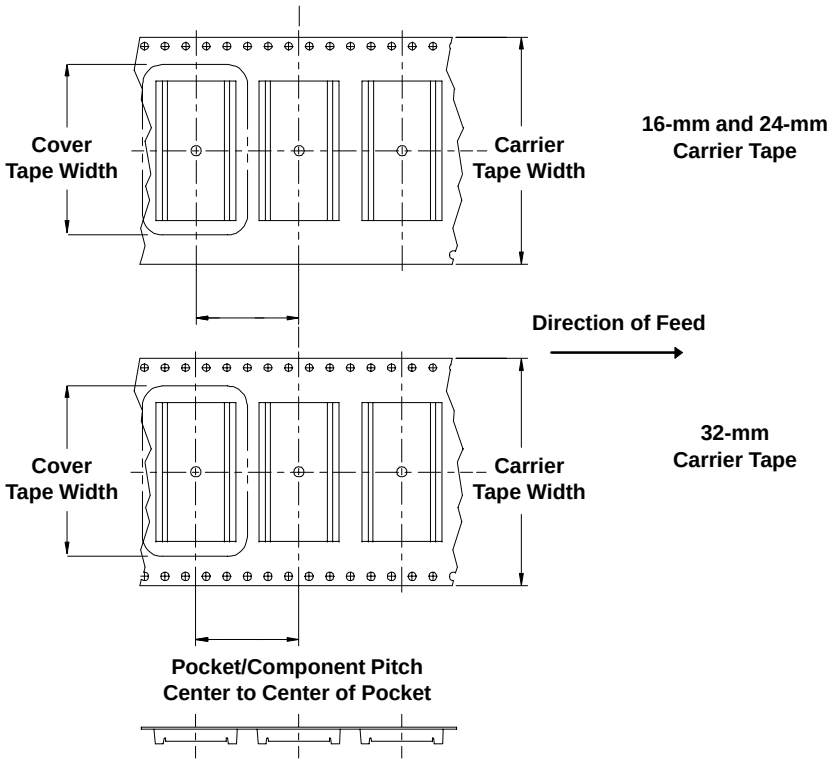
Dry pack is a method that protects moisture-sensitive plastic surface-mount devices from moisture during shipment and storage. The parts initially are baked, then placed inside a moisture- and vapor-barrier bag with a desiccant. The desiccant absorbs moisture and keeps the humidity inside the bag at a safe level. The moisture- and vapor-barrier bag used in dry pack has a maximum transmission rate of 0.02g/100 square in. in 24 hours. The desiccant used can absorb up to 3 grams of water per unit at 20% relative humidity (RH). The actual shelf life will vary, based on the storage conditions, the quality of moisture barrier the bag provides, the number of desiccants used, and the size of the package. A humidity-indicator card also is added to the bag, which shows the internal humidity of the bag in 10% increments. This card can be used to verify that the humidity level inside the bag has not exceeded the safe level. If the humidity inside the dry-pack bag exceeds the recommended RH limit shown on the dry-pack label, the parts must be baked dry before soldering.

Baking conditions and duration are described on the dry-pack labels along with an outline of necessary precautions and seal date for products. TI uses this dry-pack method, regardless of whether the parts are shipped in tubes or tape and reel.

Tape and Reel

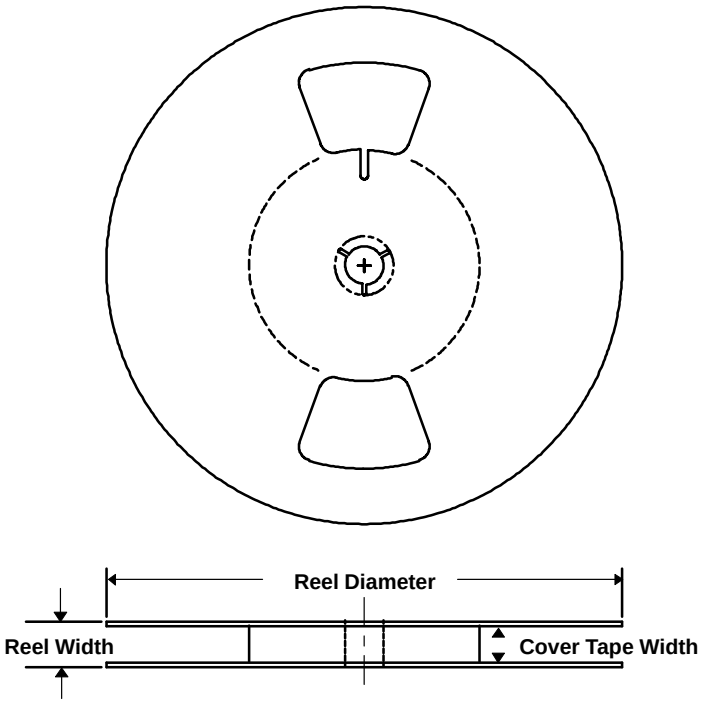
The purpose of tape-and-reel packaging is to position components so they can be placed on circuit boards using automated equipment. Components such as, but not limited to, diodes, capacitors, resistors, transistors, inductors, and ICs can be packed in this manner.

The packing materials used normally include a carrier tape, cover tape, and a reel. All material used meets industry guidelines for ESD protection. Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1, EIA-481-2, and EIA-481-3. The dimensions that are of particular interest to the end user are tape width, pocket pitch, and quantity per reel. Figures 31 and 32 illustrate typical designs for carrier tape and reels for TVSOP packages.



PACKAGE	PINS	CARRIER TAPE WIDTH (mm)	COVER TAPE WIDTH (mm)	POCKET PITCH (mm)	QUANTITY PER REEL
DGV	14–48	16.00	13.3	8.00	2000
DGV	56	24.00	21.0	8.00	2000
DBB	80	24.00	21.0	12.00	2000
DBB	100	32.00	25.5	16.00	2000

Figure 31. Carrier and Cover-Tape Information for Reeled TVSOP Packages



PACKAGE TYPE (NUMBER OF PINS)	CARRIER TAPE WIDTH (mm)	COVER TAPE WIDTH (mm)	REEL WIDTH (mm)	REEL DIAMETER (mm)
DGV (14–48)	16.00	13.3	16.4	330
DGV (56), DBB (80)	24.00	21.0	24.4	330
DBB (100)	32.00	25.5	32.4	330

Figure 32. Reel Dimensions

Test Sockets

Table 14 lists available test sockets from Yamaichi and Enplas. The sockets are closed tooling.

Table 14. Available TVSOP Test Sockets

VENDOR	PIN COUNT	SOCKET WITH FLANGE	SOCKET WITHOUT FLANGE
Yamaichi	14	IC51-0142-2074-MF	IC51-0142-2074
Yamaichi	16	IC51-0162-2073-MF	IC51-0162-2073
Yamaichi	20	IC51-0202-2072-MF	IC51-0202-2072
Yamaichi	24	IC51-0242-2071-MF	IC51-0242-2071
Yamaichi	48	IC51-0482-2069-MF	IC51-0482-2069
Yamaichi	56	IC51-0562-2067-MF	IC51-0562-2067
Yamaichi	80	IC51-0802-2077-MF	IC51-0802-2077
Enplas	80		FP-80-0.4-01
Yamaichi	100	IC51-1002-2076-MF	IC51-1002-2076

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