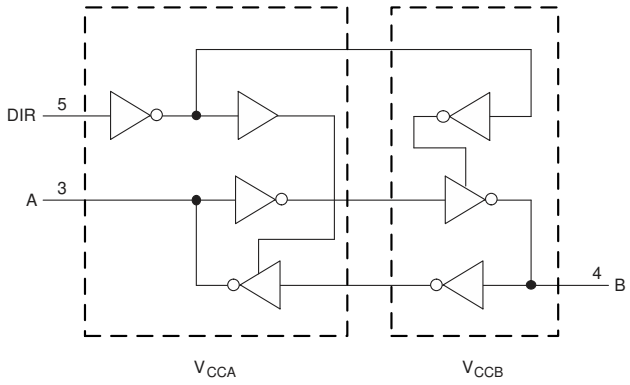
SN74AXC1T45-Q1 Automotive Qualified Single-Bit Dual-Supply Bus Transceiver with Configurable Voltage Translation, Tri-State Outputs

1 Features

- AEC-Q100 qualified for automotive applications
- Fully configurable dual-rail design allows each port to operate with a power supply range from 0.65V to 3.6V
- Operating temperature: –40°C to +125°C
- Glitch-free power supply sequencing
- Maximum quiescent current (I_{CCA} + I_{CCB}) of 10µA (85°C maximum) and 16µA (125°C maximum)
- Up to 500Mbps support when translating from 1.8 to 3.3V
- V_{CC} isolation feature
  - If Either V_{CC} input is below 100mV, all I/O outputs are disabled and become high-impedance
- I_{off} supports partial-power-down mode operation
- Latch-up performance exceeds 100mA per JESD 78, Class II
- ESD protection exceeds JESD 22:
  - 8000-V Human body model
  - 1000-V Charged-device model

2 Applications

- ADAS fusion
- ADAS front camera
- HEV battery management system
- Infotainment head unit



Functional Block Diagram

3 Description

The SN74AXC1T45-Q1 is AEC-Q100 qualified single-bit non-inverting bus transceiver that uses two individually configurable power-supply rails. The device is operational with both V_{CCA} and V_{CCB} supplies as low as 0.65V. The A port is designed to track V_{CCA}, which accepts any supply voltage from 0.65V to 3.6V. The B port is designed to track V_{CCB}, which also accepts any supply voltage from 0.65V to 3.6V. Additionally, the SN74AXC1T45-Q1 is compatible with a single-supply system.

The DIR pin determines the direction of signal propagation. With the DIR pin configured HIGH, translation is from Port A to Port B. With DIR configured LOW, translation is from Port B to Port A. The DIR pin is referenced to V_{CCA}, meaning that its logic-high and logic-low thresholds track with V_{CCA}.

This device is fully specified for partial-power-down applications using the I_{off} current. The I_{off} protection circuitry is designed so that no excessive current is drawn from or to an input, output, or combined I/O that is biased to a specific voltage while the device is powered down.

The V_{CC} isolation feature is designed so that if either V_{CCA} or V_{CCB} is less than 100mV, both I/O ports enter a high-impedance state by disabling their outputs.

Glitch-free power supply sequencing allows either supply rail to be powered on or off in any order while providing robust power sequencing performance.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
SN74AXC1T45-Q1	DCK (SC70, 6)	2mm × 2.1mm
	DRY (SON, 6)	1.45mm × 1mm

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Pin Configuration and Functions

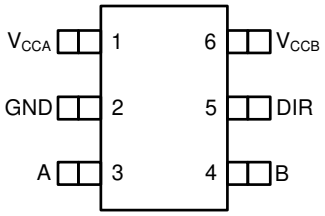

Figure 4-1. DCK Package, 6-Pin SC70 (Top View)

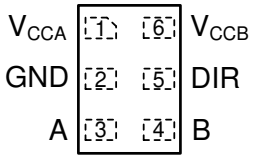

Figure 4-2. DRY Package, 6-Pin SON Transparent (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{CCA}	1	—	A-port supply voltage. 0.65V ≤ V_{CCA} ≤ 3.6V
GND	2	—	Ground
A	3	I/O	Input/output A. This pin is referenced to V_{CCA}.
B	4	I/O	Input/output B. This pin is referenced to V_{CCB}.
DIR	5	I	Direction control signal. See *Device Functional Modes* for functionality
V_{CCB}	6	—	B-port supply voltage. 0.65V ≤ V_{CCB} ≤ 3.6V.

(1) I = input, O = output

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage A		–0.5	4.2	V
V_{CCB}	Supply voltage B		–0.5	4.2	V
V_I	Input Voltage(2)	I/O Ports (A Port)	–0.5	4.2	V
		I/O Ports (B Port)	–0.5	4.2	
		Control Inputs	–0.5	4.2	
V_O	Voltage applied to any output in the high-impedance or power-off state(2)	A Port	–0.5	4.2	V
		B Port	–0.5	4.2	
V_O	Voltage applied to any output in the high or low state(2) (3)	A Port	–0.5	V_{CCA} + 0.2	V
		B Port	–0.5	V_{CCB} + 0.2	
I_{IK}	Input clamp current	V_I < 0	–50		mA
I_{OK}	Output clamp current	V_O < 0	–50		mA
I_O	Continuous output current		–50	50	mA
	Continuous current through V_{CC} or GND		–100	100	mA
T_J	Junction Temperature			150	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.2V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±8000	V
		Charged device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

				MIN	MAX	UNIT
V_{CCA}	Supply voltage A			0.65	3.6	V
V_{CCB}	Supply voltage B			0.65	3.6	V
V_{IH}	High-level input voltage	Data Inputs	V_{CCI} = 0.65V - 0.75V	V_{CCI} x 0.70		V
			V_{CCI} = 0.76V - 1 V	V_{CCI} x 0.70		
			V_{CCI} = 1.1 V - 1.95V	V_{CCI} x 0.65		
			V_{CCI} = 2.3V - 2.7V	1.6		
			V_{CCI} = 3V - 3.6V	2		
		Control Input (DIR) Referenced to V_{CCA}	V_{CCA} = 0.65V - 0.75V	V_{CCA} x 0.70		
			V_{CCA} = 0.76V - 1 V	V_{CCA} x 0.70		
			V_{CCA} = 1.1 V - 1.95V	V_{CCA} x 0.65		
			V_{CCA} = 2.3V - 2.7V	1.6		
			V_{CCA} = 3V - 3.6V	2		
V_{IL}	Low-level input voltage	Data Inputs	V_{CCI} = 0.65V - 0.75V		V_{CCI} x 0.30	V
			V_{CCI} = 0.76V - 1 V		V_{CCI} x 0.30	
			V_{CCI} = 1.1 V - 1.95V		V_{CCI} x 0.35	
			V_{CCI} = 2.3V - 2.7V		0.7	
			V_{CCI} = 3V - 3.6V		0.8	
		Control Input (DIR) Referenced to V_{CCA}	V_{CCA} = 0.65V - 0.75V		V_{CCA} x 0.30	
			V_{CCA} = 0.76V - 1 V		V_{CCA} x 0.30	
			V_{CCA} = 1.1 V - 1.95V		V_{CCA} x 0.35	
			V_{CCA} = 2.3V - 2.7V		0.7	
			V_{CCA} = 3V - 3.6V		0.8	
V_I	Input voltage (3)			0	3.6	V
V_O	Output voltage	Active State		0	V_{CCO}	V
		Tri-State		0	3.6	
$\Delta t/\Delta v$	Input transition rate				100	ns/V
T_A	Operating free-air temperature			–40	125	°C

(1) VCCI is the VCC associated with the input port.
(2) VCCO is the VCC associated with the output port.
(3) All unused inputs of the device must be held at VCC or GND for proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.

5.4 Thermal Information

THERMAL METRIC(1)		SN74AXC1T45-Q1		UNIT
		DCK (SC70)	DRY (SON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	235.3	305.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	160.5	202.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	76.9	181.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	59.7	41.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	77.1	180.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted) (1) (2)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	Operating free-air temperature (T_A)						UNIT
						–40°C to 85°C			–40°C to 125°C			
						MIN	TYP(3)	MAX	MIN	TYP	MAX	
V_{OH}	High-level output voltage	$V_I = V_{IH}$	I_{OH} = -100µA	0.7V - 3.6V	0.7V - 3.6V	V_{CCO} – 0.1			V_{CCO} – 0.1			V
			I_{OH} = -50µA	0.65V	0.65V	0.55			0.55			
			I_{OH} = -200µA	0.76V	0.76V	0.58			0.58			
			I_{OH} = -500µA	0.85V	0.85V	0.65			0.65			
			I_{OH} = -3mA	1.1V	1.1V	0.85			0.85			
			I_{OH} = -6mA	1.4V	1.4V	1.05			1.05			
			I_{OH} = -8mA	1.65V	1.65V	1.2			1.2			
			I_{OH} = -9mA	2.3V	2.3V	1.75			1.75			
			I_{OH} = -12mA	3V	3V	2.3			2.3			
V_{OL}	Low-level output voltage	$V_I = V_{IL}$	I_{OL} = 100µA	0.7V - 3.6V	0.7V - 3.6V			0.1			0.1	V
			I_{OL} = 50µA	0.65V	0.65V			0.1			0.1	
			I_{OL} = 200µA	0.76V	0.76V			0.18			0.18	
			I_{OL} = 500µA	0.85V	0.85V			0.2			0.2	
			I_{OL} = 3mA	1.1V	1.1V			0.25			0.25	
			I_{OL} = 6mA	1.4V	1.4V			0.35			0.35	
			I_{OL} = 8mA	1.65V	1.65V			0.45			0.45	
			I_{OL} = 9mA	2.3V	2.3V			0.55			0.55	
			I_{OL} = 12mA	3V	3V			0.7			0.7	
I_I	Input leakage current	Control input (DIR): V_I = V_{CCA} or GND		0.65V- 3.6V	0.65V- 3.6V	–1		1	–1.5		1.5	µA
		A or B Port: Vi = V_{CCI} or GND		0.65V- 3.6V	0.65V- 3.6V	–4		4	–8		8	
I_{off}	Partial power down current	A or B Port: Vi or Vo = 0V - 3.6V		0V	0V - 3.6V	–5		5	–7.5		7.5	µA
				0V - 3.6V	0V	–5		5	–7.5		7.5	
I_{CCA}	V_{CCA} supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65V- 3.6V	0.65V- 3.6V			8			12	µA
				0V	3.6V	–2			–8			
				3.6V	0V			2			8	
I_{CCB}	V_{CCB} supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65V- 3.6V	0.65V- 3.6V			8			12	µA
				0V	3.6V			2			8	
				3.6V	0V	–2			–8			
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND	I_O = 0	0.65V- 3.6V	0.65V- 3.6V			10			16	µA
C_I	Control input capacitance	V_I = 3.3V or GND		3.3V	3.3V		4.4			4.4		pF
C_{IO}	Data I/O capacitance, A Port	V_O = 1.65V DC +1MHz -16 dBm sine wave		3.3V	0V		5			5		pF
C_{IO}	Data I/O capacitance, B Port	V_O = 1.65V DC +1MHz -16 dBm sine wave		0V	3.3V		5			5		pF

(1) VCCI is the VCC associated with the input port.
(2) VCCO is the VCC associated with the output port.
(3) All typical data is taken at 25°C.

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5.6 Operating Characteristics: T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	MIN	TYP	MAX	UNIT
C_{pdA}	Power Dissipation Capacitance per transceiver (A to B)	C_L = 0, R_L = Open f = 1MHz, t_r = t_f = 1 ns	0.7V	0.7V		1.3		pF
			0.8V	0.8V		1.3		
			0.9V	0.9V		1.3		
			1.2V	1.2V		1.3		
			1.5V	1.5V		1.3		
			1.8V	1.8V		1.4		
			2.5V	2.5V		1.7		
			3.3V	3.3V		2.1		
	Power Dissipation Capacitance per transceiver (B to A)	C_L = 0, R_L = Open f = 1MHz, t_r = t_f = 1 ns	0.7V	0.7V		9.2		pF
			0.8V	0.8V		9.4		
			0.9V	0.9V		9.4		
			1.2V	1.2V		9.8		
			1.5V	1.5V		10.1		
			1.8V	1.8V		11.0		
			2.5V	2.5V		14.4		
			3.3V	3.3V		18.6		
C_{pdB}	Power Dissipation Capacitance per transceiver (A to B)	C_L = 0, R_L = Open f = 1MHz, t_r = t_f = 1 ns	0.7V	0.7V		9.2		pF
			0.8V	0.8V		9.3		
			0.9V	0.9V		9.4		
			1.2V	1.2V		9.7		
			1.5V	1.5V		10.1		
			1.8V	1.8V		11.0		
			2.5V	2.5V		14.4		
			3.3V	3.3V		18.3		
	Power Dissipation Capacitance per transceiver (B to A)	C_L = 0, R_L = Open f = 1MHz, t_r = t_f = 1 ns	0.7V	0.7V		1.3		pF
			0.8V	0.8V		1.3		
			0.9V	0.9V		1.3		
			1.2V	1.2V		1.3		
			1.5V	1.5V		1.3		
			1.8V	1.8V		1.4		
			2.5V	2.5V		1.7		
			3.3V	3.3V		2.1		

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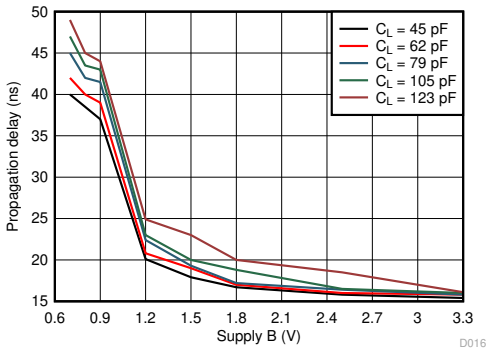
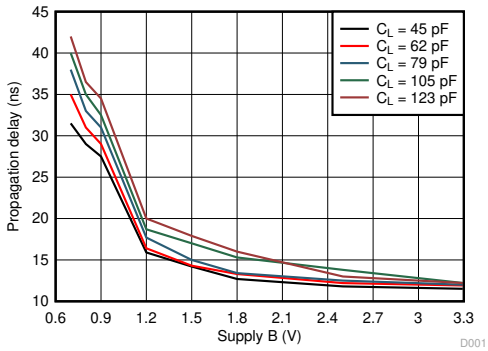
5.7 Typical Characteristics



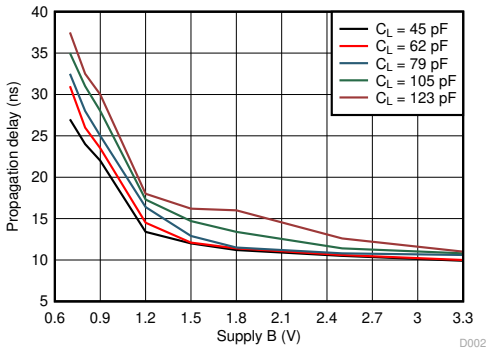
T_A = 25°C V_{CCA} = 0.7V

Figure 5-1. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



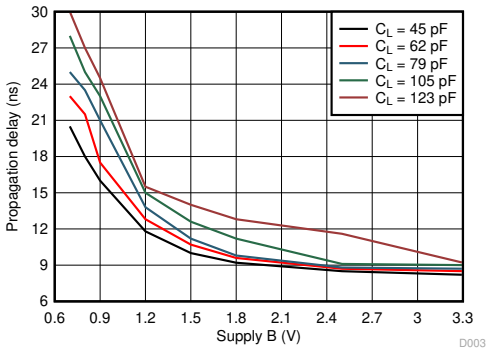
T_A = 25°C V_{CCA} = 0.8V

Figure 5-2. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



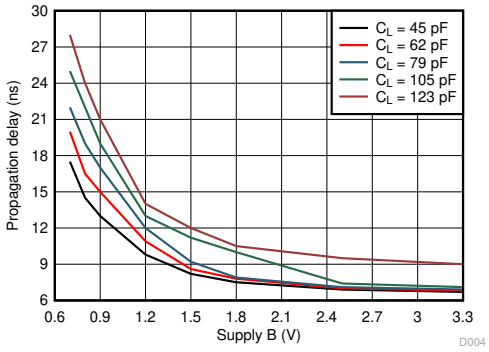
T_A = 25°C V_{CCA} = 0.9V

Figure 5-3. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



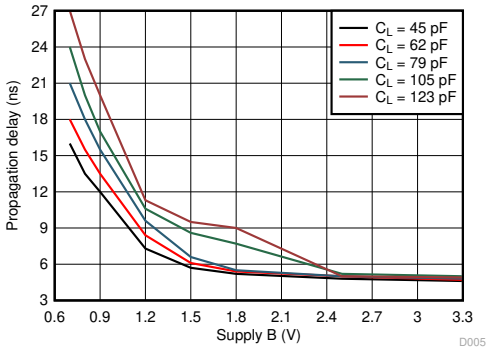
T_A = 25°C V_{CCA} = 1.2V

Figure 5-4. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



T_A = 25°C V_{CCA} = 1.5V

Figure 5-5. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



T_A = 25°C V_{CCA} = 1.8V

Figure 5-6. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance

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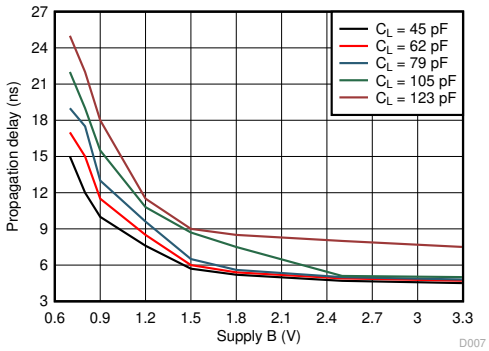
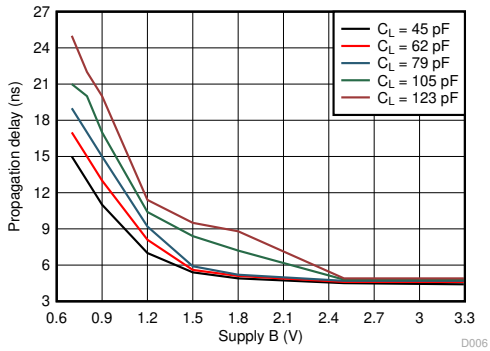
5.7 Typical Characteristics (continued)



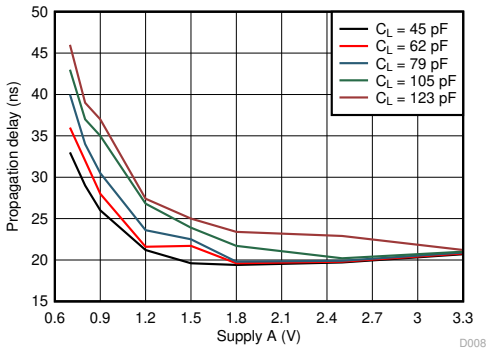
T_A = 25°C V_{CCA} = 3.3V

Figure 5-7. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



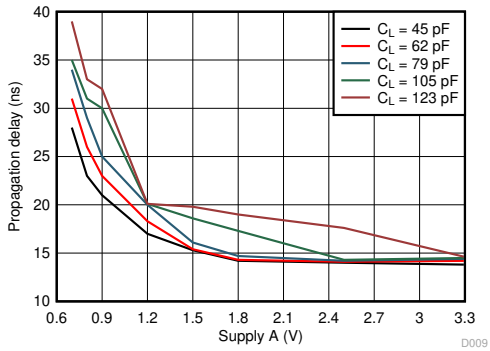
T_A = 25°C V_{CCA} = 2.5V

Figure 5-8. Typical Propagation Delay of Low-to-High (A to B) vs Load Capacitance



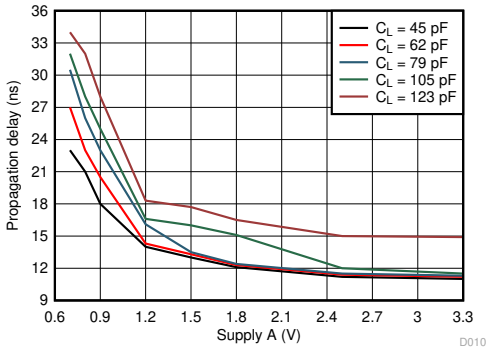
T_A = 25°C V_{CCA} = 0.7V

Figure 5-9. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



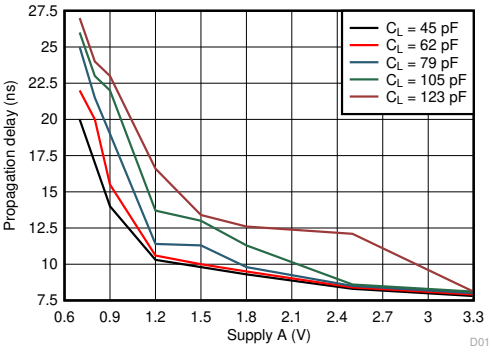
T_A = 25°C V_{CCA} = 0.8V

Figure 5-10. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



T_A = 25°C V_{CCA} = 0.9V

Figure 5-11. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



T_A = 25°C V_{CCA} = 1.2V

Figure 5-12. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance

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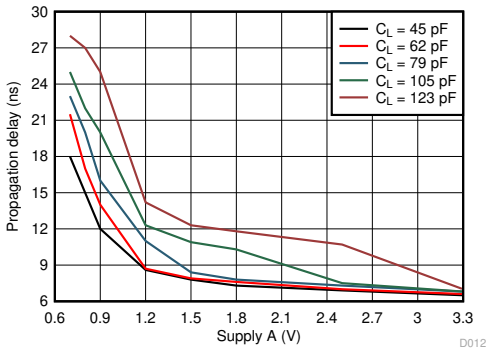
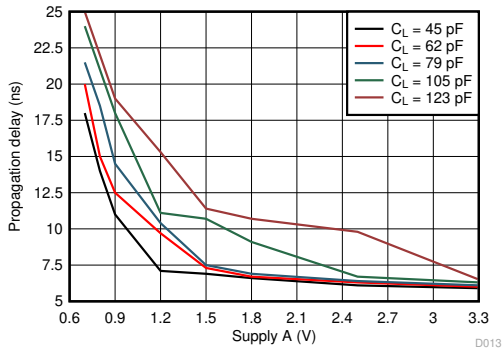
5.7 Typical Characteristics (continued)



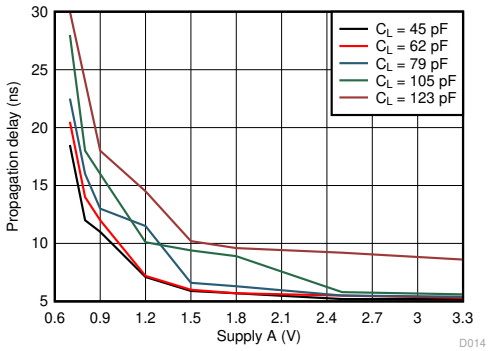
T_A = 25°C V_{CCA} = 1.5V

Figure 5-13. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



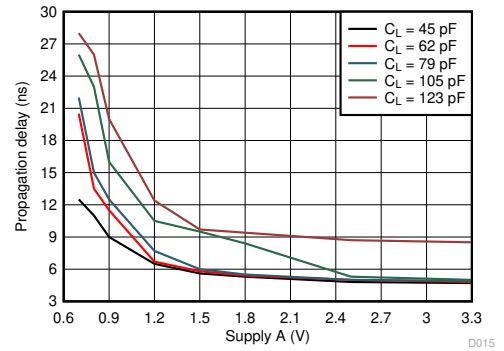
T_A = 25°C V_{CCA} = 1.8V

Figure 5-14. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



T_A = 25°C V_{CCA} = 2.5V

Figure 5-15. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance



T_A = 25°C V_{CCA} = 3.3V

Figure 5-16. Typical Propagation Delay of Low-to-High (B to A) vs Load Capacitance

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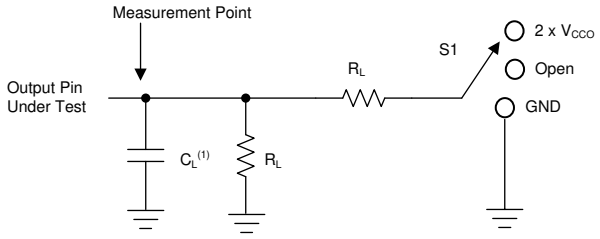
6 Parameter Measurement Information

6.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 1MHz
- Z_O = 50Ω
- dv/dt ≤ 1 ns/V

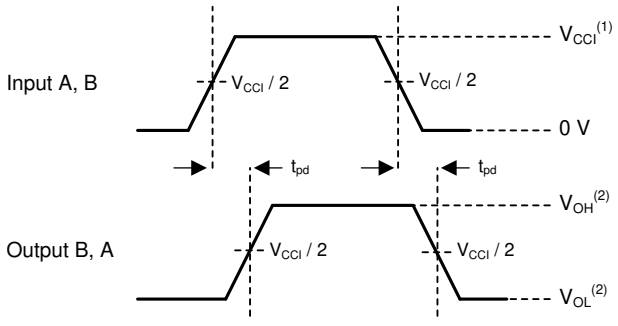


A. C_L includes probe and jig capacitance.

Figure 6-1. Load Circuit

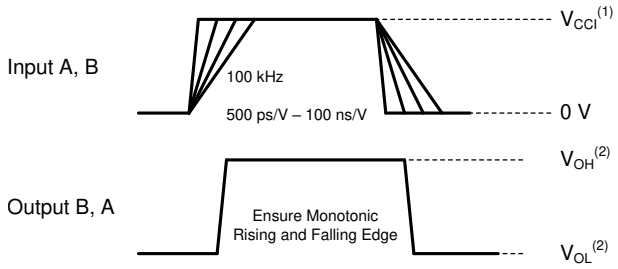
Table 6-1. Load Circuit Conditions

Parameter		V_{CCO}	R_L	C_L	S_1	V_{TP}
Δt/Δv	Input transition rise or fall rate	0.65V – 3.6V	1MΩ	15pF	Open	N/A
t_{pd}	Propagation (delay) time	1.1 V – 3.6V	2kΩ	15pF	Open	N/A
		0.65V – 0.95V	20kΩ	15pF	Open	N/A
t_{en}, t_{dis}	Enable time, disable time	3V – 3.6V	2kΩ	15pF	2 × V_{CCO}	0.3V
		1.65V – 2.7V	2kΩ	15pF	2 × V_{CCO}	0.15V
		1.1 V – 1.6V	2kΩ	15pF	2 × V_{CCO}	0.1V
		0.65V – 0.95V	20kΩ	15pF	2 × V_{CCO}	0.1V
t_{en}, t_{dis}	Enable time, disable time	3V – 3.6V	2kΩ	15pF	GND	0.3V
		1.65V – 2.7V	2kΩ	15pF	GND	0.15V
		1.1 V – 1.6V	2kΩ	15pF	GND	0.1V
		0.65V – 0.95V	20kΩ	15pF	GND	0.1V



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-3. Input Transition Rise or Fall Rate

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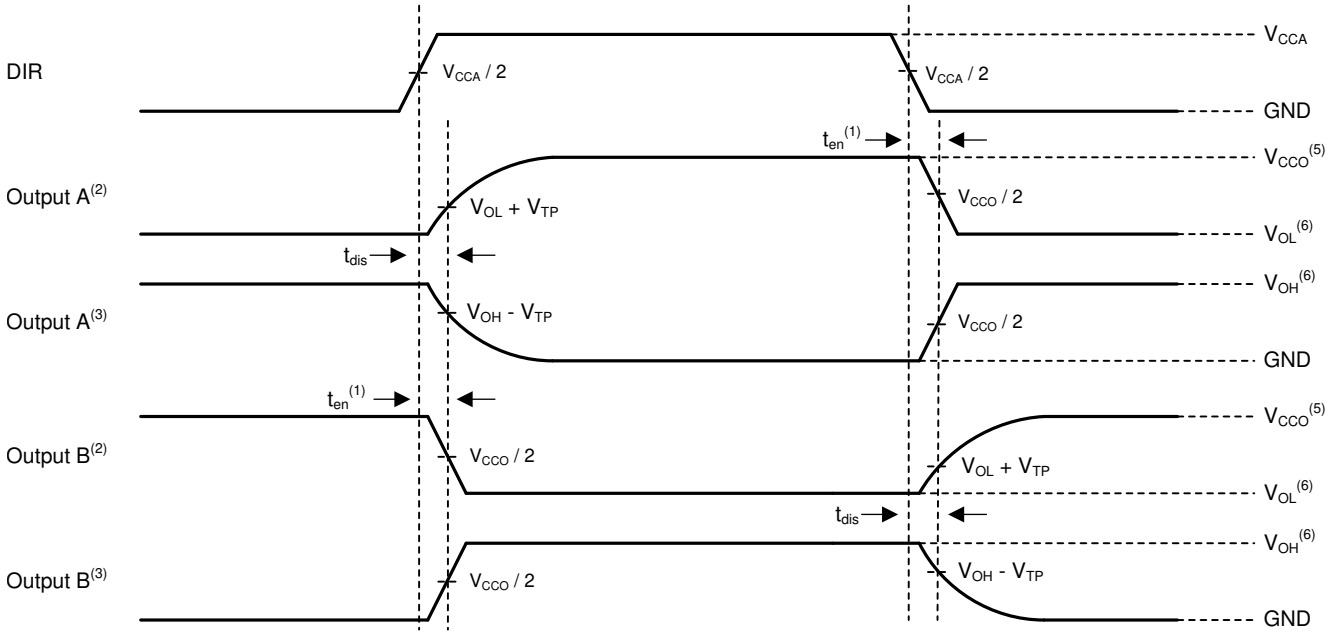

1. Illustrative purposes only. Enable Time is a calculation as described in the data sheet.
2. Output waveform on the condition that input is driven to a valid Logic Low.
3. Output waveform on the condition that input is driven to a valid Logic High.
4. V_{CCI} is the supply pin associated with the input port
5. V_{CCO} is the supply pin associated with the output port.
6. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1

Figure 6-4. Disable and Enable Time

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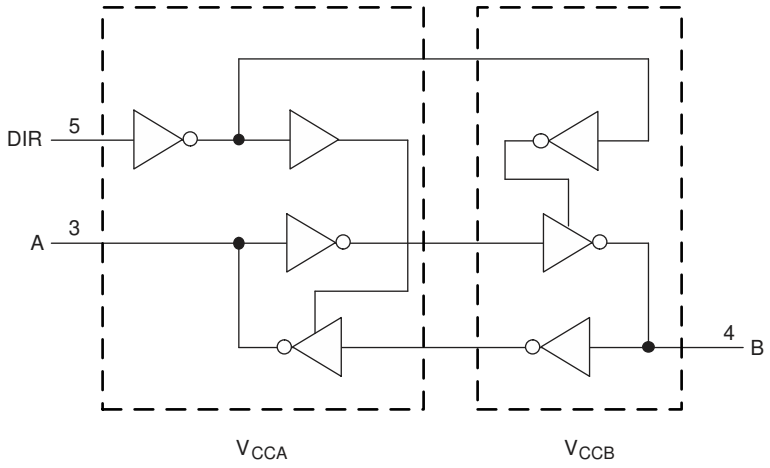
7 Detailed Description

7.1 Overview

The SN74AXC1T45-Q1 is AEC-Q100 qualified single-bit, dual-supply, non-inverting voltage level translator. Pin A and the direction control pin are referenced to V_{CCA} logic levels and pin B is referenced to V_{CCB} logic levels, as depicted in the *Functional Block Diagram*. The A port can accept I/O voltages ranging from 0.65V to 3.6V, and the B port can accept I/O voltages from 0.65V to 3.6V. A logic high on the DIR pin enables data transmission from A to B and a logic low on the DIR pin enables data transmission from B to A.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by Δt/Δv in *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.2 Balanced High-Drive CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The high drive capability of this device creates fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

7.3.3 Partial Power Down (I_{off})

The inputs and outputs for this device enter a high-impedance state when the device is powered down, inhibiting current backflow into the device. The maximum leakage into or out of any input or output pin on the device is specified by I_{off} in the *Electrical Characteristics*.

7.3.4 V_{CC} Isolation

The inputs and outputs for this device enter a high-impedance state when either supply is <100mV.

7.3.5 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the *Recommended Operating Conditions*.

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7.3.6 Negative Clamping Diodes

The inputs and outputs to this device have negative clamping diodes as depicted in Figure 7-1.

CAUTION

Voltages beyond the values specified in the Absolute Maximum Ratings table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

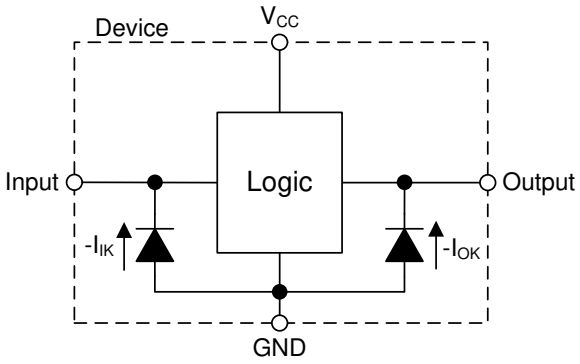

Figure 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.3.7 Fully Configurable Dual-Rail Design

Both the V_{CCA} and V_{CCB} pins can be supplied at any voltage from 0.65V to 3.6V, making the device suitable for translating between any of the voltage nodes (0.7V, 0.8V, 0.9V, 1.2V, 1.8V, 2.5V and 3.3V).

7.3.8 I/Os with Integrated Static Pull-Down Resistors

To help avoid floating inputs on the I/Os, this device has 288kΩ typical integrated weak pull-downs on all data I/Os. This feature allows all inputs to be left floating without the concern for unstable outputs or increased current consumption. This also helps to reduce external component count for applications where not all channels are used or need to be fixed low. If an external pull-up is required, it should be no larger than 30kΩ to avoid contention with the 288kΩ internal pull-down.

7.3.9 Supports High-Speed Translation

The SN74AXC1T45-Q1 device can support high data-rate applications. The translated signal data rate can be up to 500Mbps when the signal is translated from 1.8V to 3.3V.

7.4 Device Functional Modes

Table 7-1 lists the device functions for the DIR input.

Table 7-1. Function Table

INPUT(1) DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The SN74AXC1T45-Q1 device can be used in level-translation applications for interfacing devices or systems with one another when they are operating at different interface voltages. The maximum data rate can be up to 500Mbps when the device translate signals from 1.8V to 3.3V.

8.1.1 Enable Times

Calculate the enable times for the SN74AXC1T45-Q1 using the following formulas:

$$t_{PZH}\text{ (DIR to A)} = t_{PLZ}\text{ (DIR to B)} + t_{PLH}\text{ (B to A)} \quad (1)$$

$$t_{PZL}\text{ (DIR to A)} = t_{PHZ}\text{ (DIR to B)} + t_{PHL}\text{ (B to A)} \quad (2)$$

$$t_{PZH}\text{ (DIR to B)} = t_{PLZ}\text{ (DIR to A)} + t_{PLH}\text{ (A to B)} \quad (3)$$

$$t_{PZL}\text{ (DIR to B)} = t_{PHZ}\text{ (DIR to A)} + t_{PHL}\text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay time from the time the DIR bit is switched until an output is expected. For example, if the SN74AXC1T45-Q1 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

8.2 Typical Applications

8.2.1 Interrupt Request Application

Figure 8-1 shows an example of the SN74AXC1T45-Q1 being used in an application where a system controller flags an interrupt request (IRQ) to the CPU. The system controller determines the direction of the IRQ line to either flag an interrupt to the CPU or allow the CPU to drive data on the line. In this application the controller is operating at 3.3V while the CPU can operate as low as 0.65V.

The SN74AXC1T45-Q1 device is used to allow these devices to communicate at the appropriate voltage levels. Because the SN74AXC1T45-Q1 does not have an output-enable ($\overline{OE}$) pin, the system designer should take precautions to avoid bus contention between the CPU and controller when changing directions.

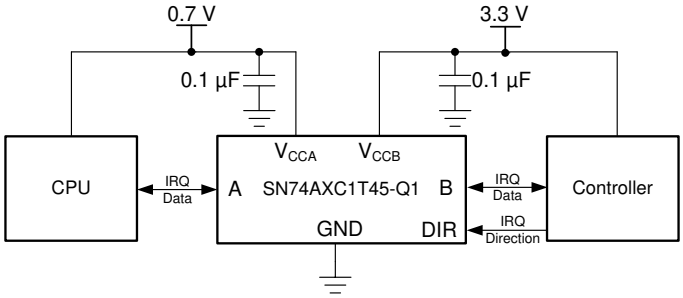

Figure 8-1. Interrupt Request Application

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8.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 8-1.

Table 8-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input voltage range	0.65V to 3.6V
Output voltage range	0.65V to 3.6V

8.2.1.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AXC1T45-Q1 device to determine the input voltage range. For a valid logic-high, the value must exceed the high-level input voltage (V_{IH}) of the input port. For a valid logic low the value must be less than the low-level input voltage (V_{IL}) of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AXC1T45-Q1 device is driving to determine the output voltage range.

8.2.1.3 Application Curve

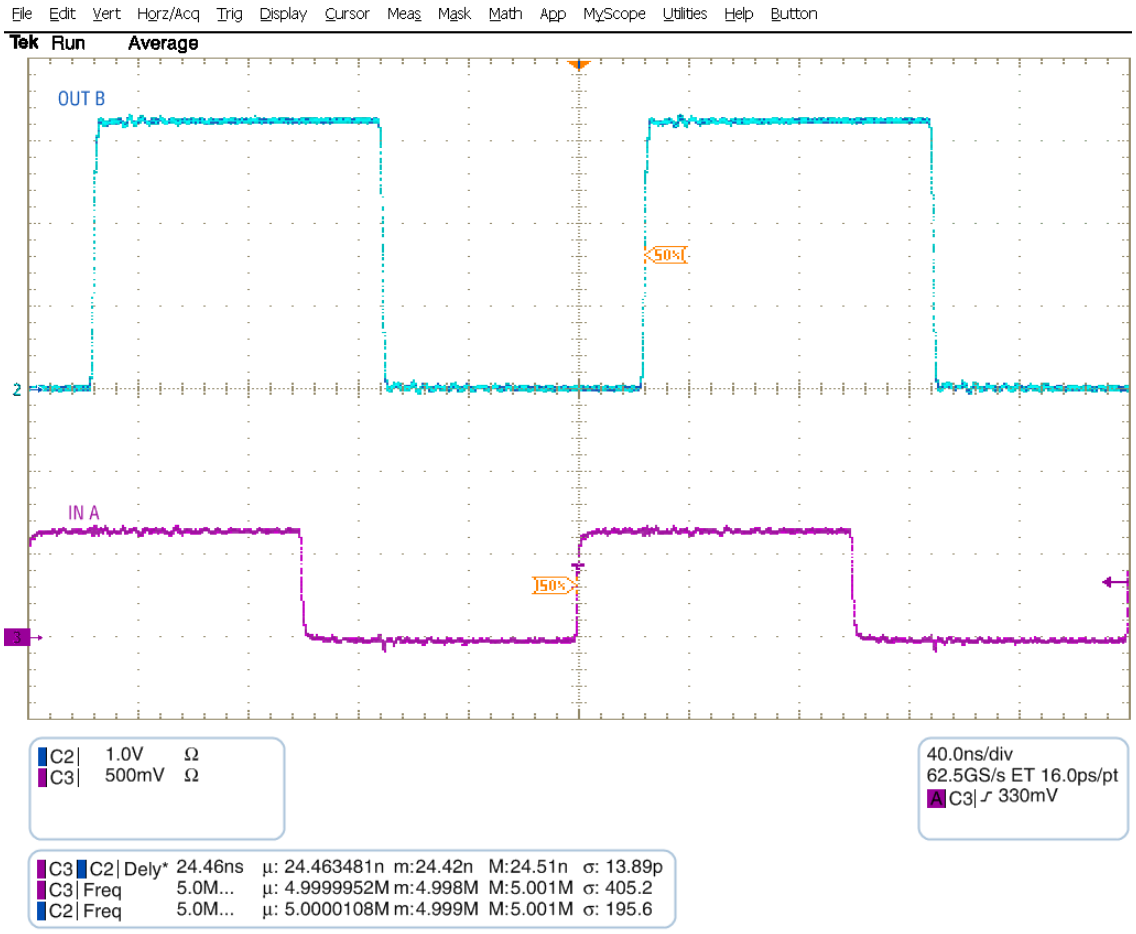

Figure 8-2. Up Translation at 2.5MHz (0.7V to 3.3V)

8.2.2 Universal Asynchronous Receiver-Transmitter (UART) Interface Application

Figure 8-3 shows the SN74AXC1T45-Q1 being used for the two-bit UART interface application. One SN74AXC1T45-Q1 device is used to level shift the voltage and drive the TX from the processor to the GPS Module while a second SN74AXC1T45-Q1 device is used to drive the TX Data line from the GPS Module to the Processor.

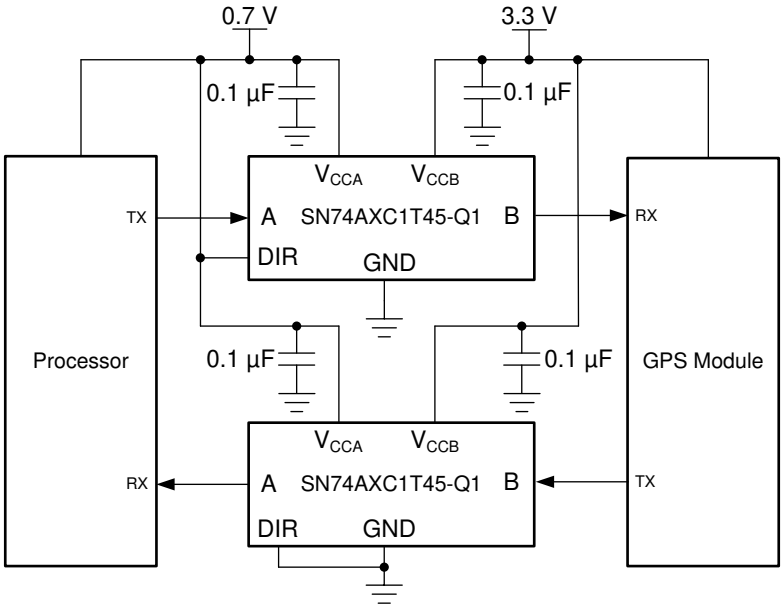

Figure 8-3. UART Interface Application

8.2.2.1 Design Requirements

Refer to *Section 8.2.1.1*.

8.2.2.2 Detailed Design Procedure

Refer to *Section 8.2.1.2*.

8.3 Power Supply Recommendations

Always apply a ground reference to the GND pins first. This device is designed for glitch free power sequencing without any supply sequencing requirements such as ramp order or ramp rate.

This device was designed with various power supply sequencing methods in mind to help prevent unintended triggering of downstream devices. For more information regarding the power up glitch performance of the AXC family of level translators, see the *Power Sequencing for AXC Family of Devices* application report

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, following common printed-circuit board layout guidelines are recommended:

- Use bypass capacitors on the power supply pins and place them as close to the device as possible.
- Use short trace lengths to avoid excessive loading.

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8.4.2 Layout Example

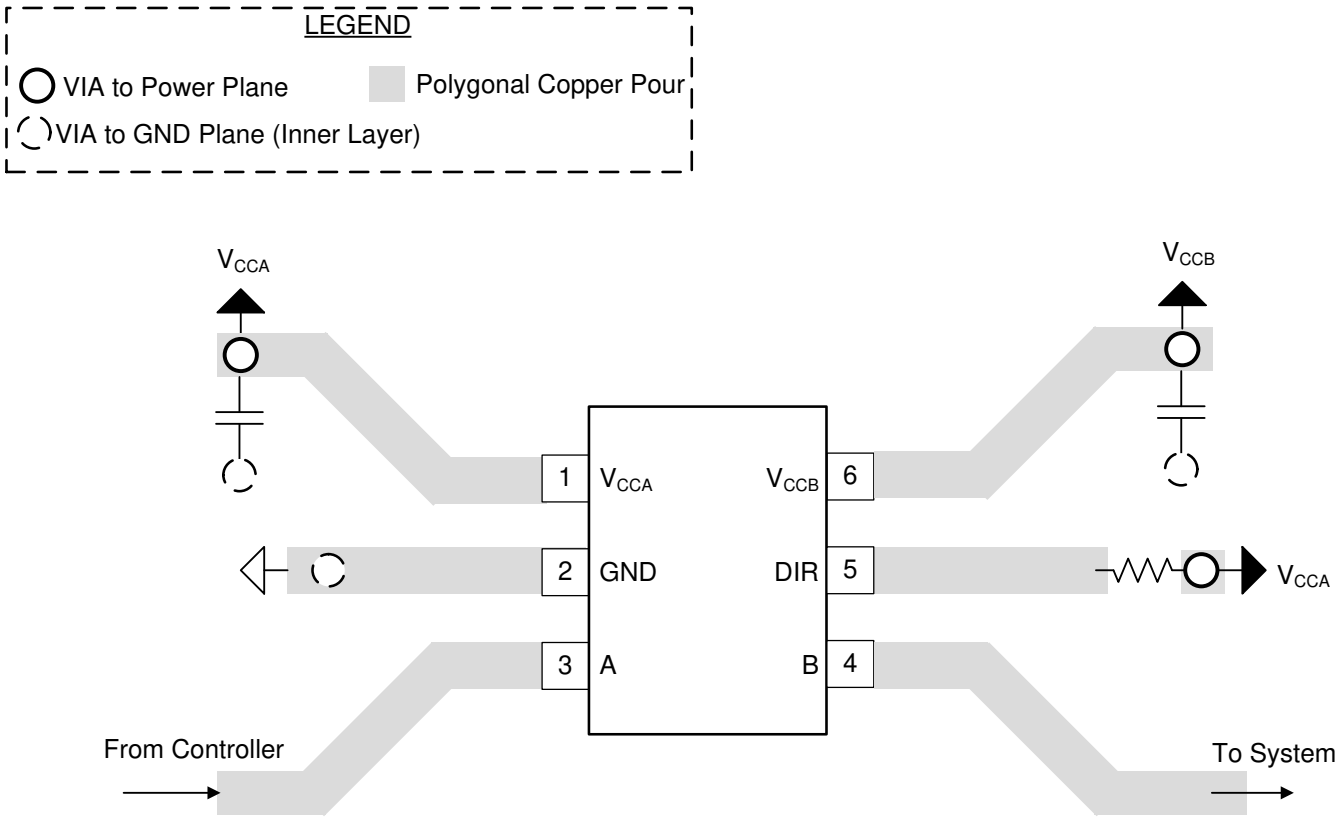

Figure 8-4. PCB Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Evaluate SN74AXC1T45DRL Using a Generic EVM* application report
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application report
- Texas Instruments, *Power Sequencing for the AXC Family of Devices* application report

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

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All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (January 2020) to Revision D (January 2024)	Page
• Added the *I/Os with Integrated Static Pull-Down Resistors* section	13

Changes from Revision B (September 2019) to Revision C (January 2020)	Page
• Device with DRY package is now Active status	2
• Updated I_{CCA}, I_{CCB}, and I_{CCA} + I_{CCB} to reflect updated performance of device	5

Changes from Revision A (July 2019) to Revision B (September 2019)	Page
• Device with DCK package is now Active status	2

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Changes from Revision * (February 2019) to Revision A (July 2019)	Page
• Added DRY package to Device Information table	1
• Added DRY package to Pin Configurations	2
• Added DRY package to Section 5.4 table	4

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AXC1T45QDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1E1	Samples
SN74AXC1T45QDRYRQ1	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	G2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AXC1T45-Q1 :

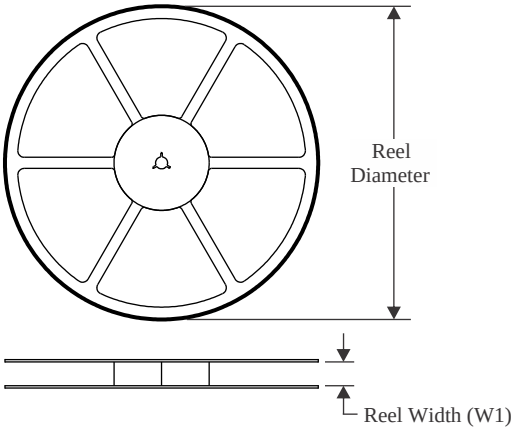
- Catalog : SN74AXC1T45

NOTE: Qualified Version Definitions:

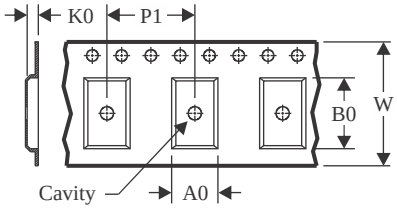
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

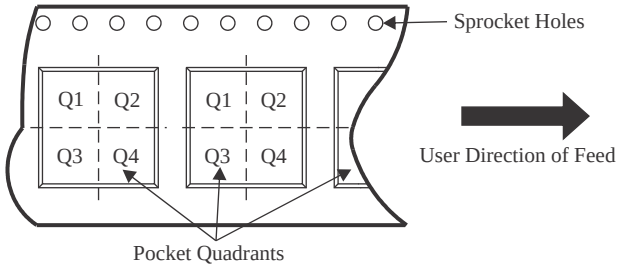


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

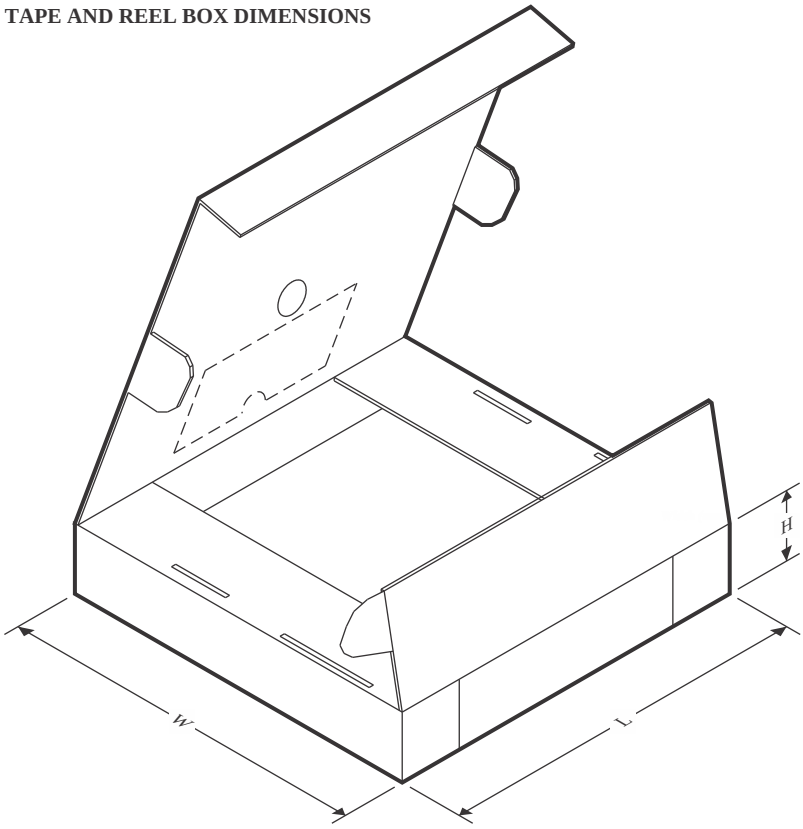
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AXC1T45QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74AXC1T45QDRYRQ1	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

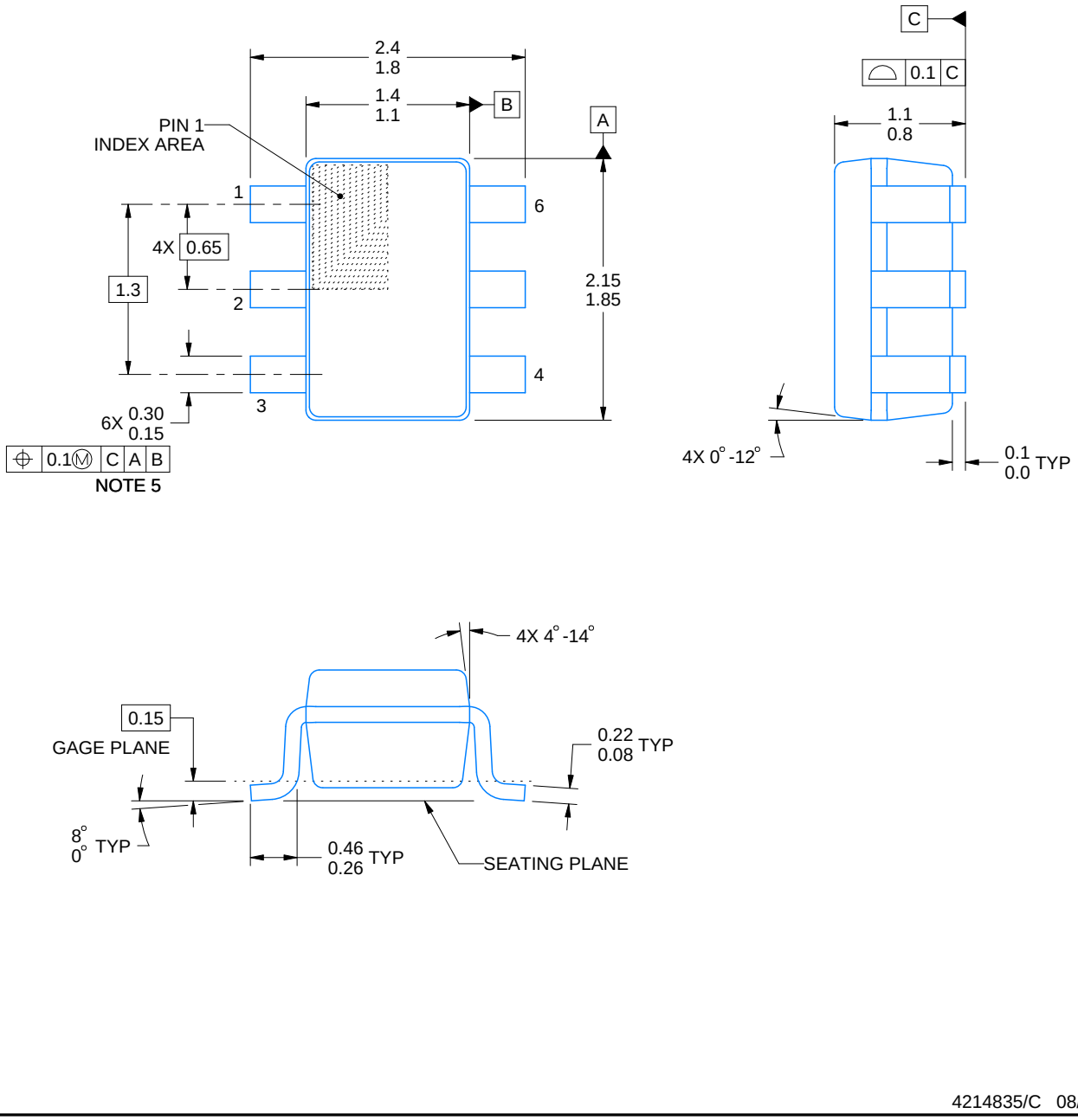
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AXC1T45QDCKRQ1	SC70	DCK	6	3000	190.0	190.0	30.0
SN74AXC1T45QDRYRQ1	SON	DRY	6	5000	189.0	185.0	36.0

PACKAGE OUTLINE

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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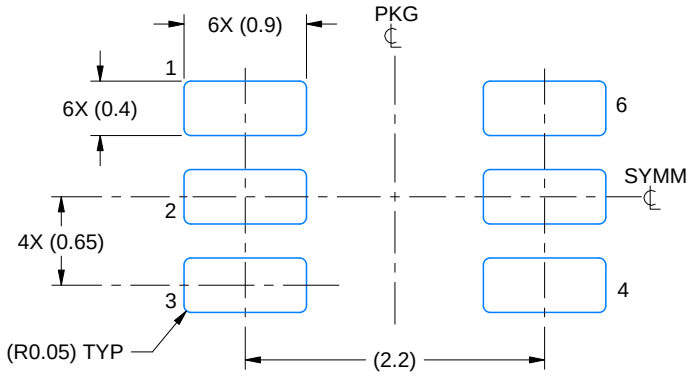
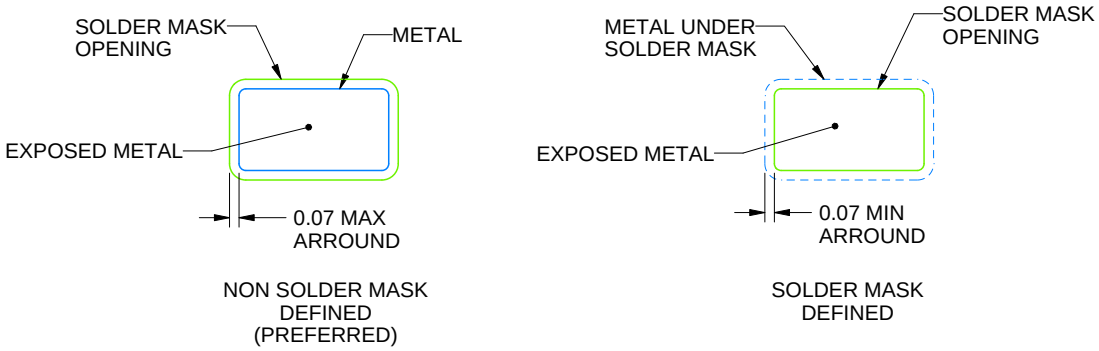
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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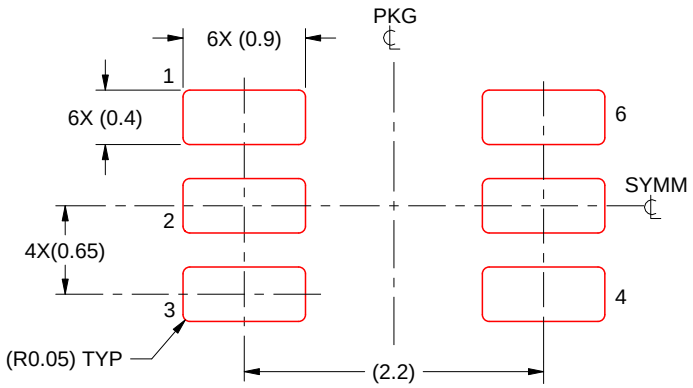
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRY 6 USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

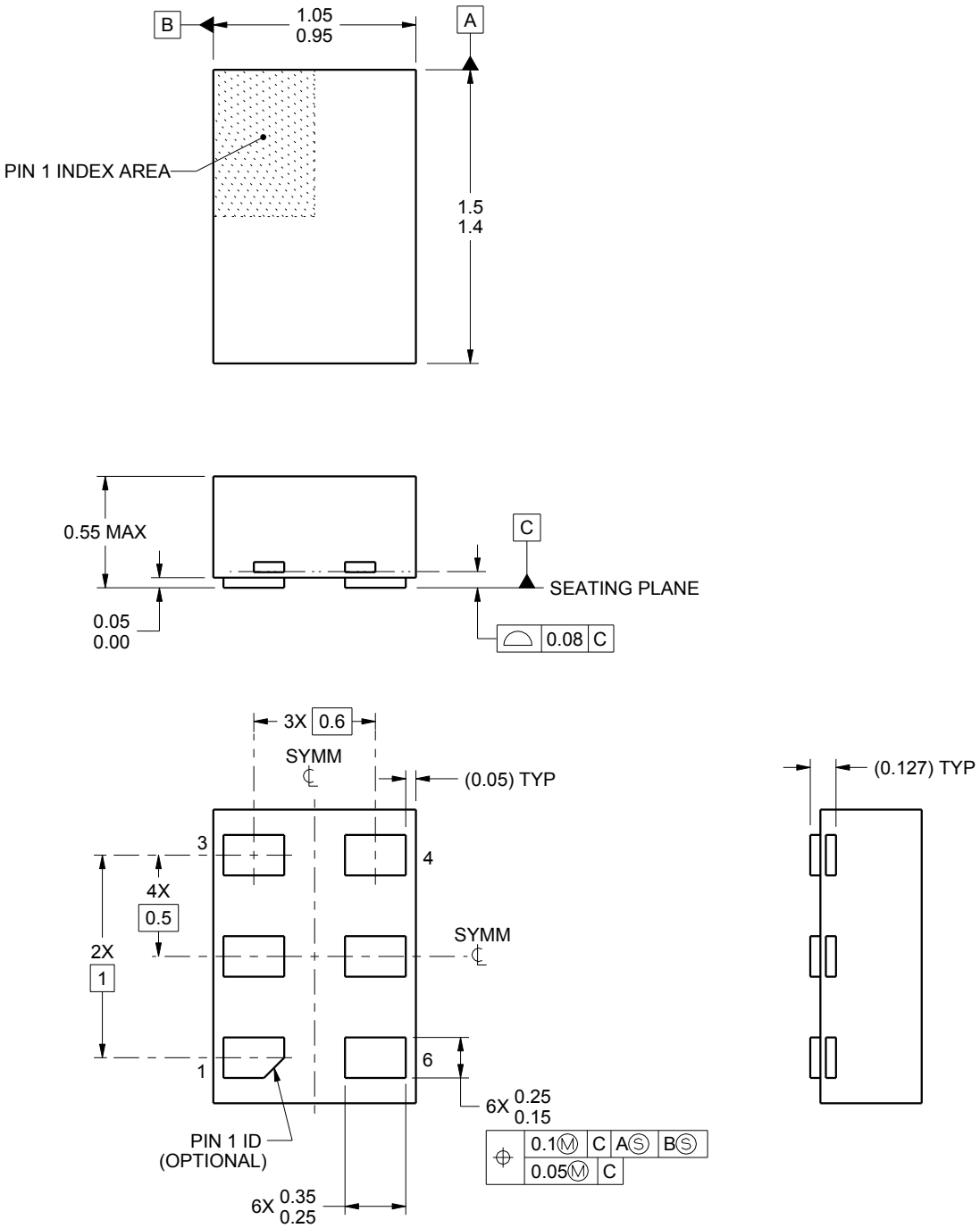
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DRY0006B

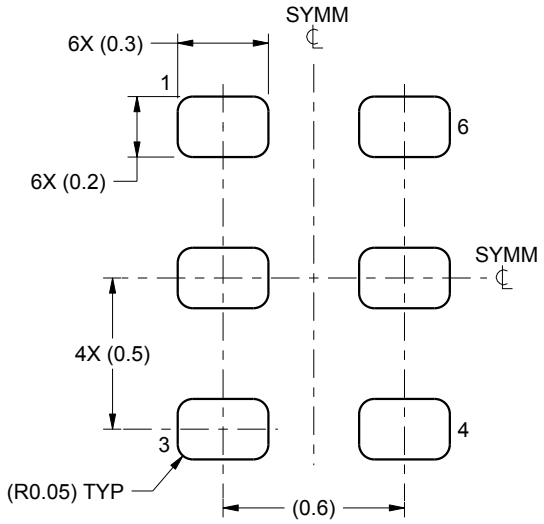
USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

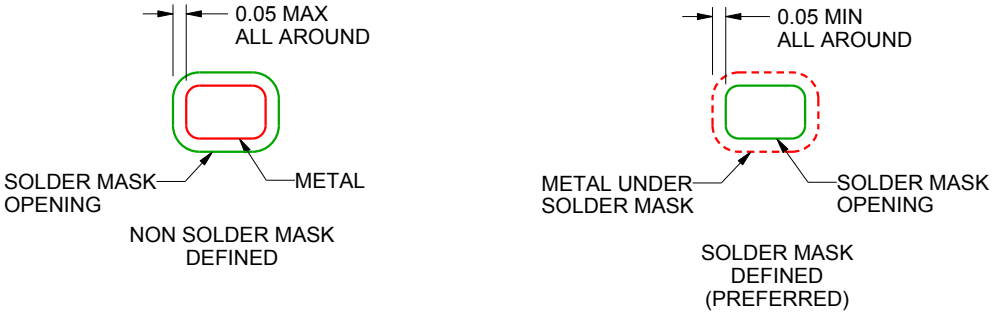


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
SCALE:40X



SOLDER MASK DETAILS

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NOTES: (continued)

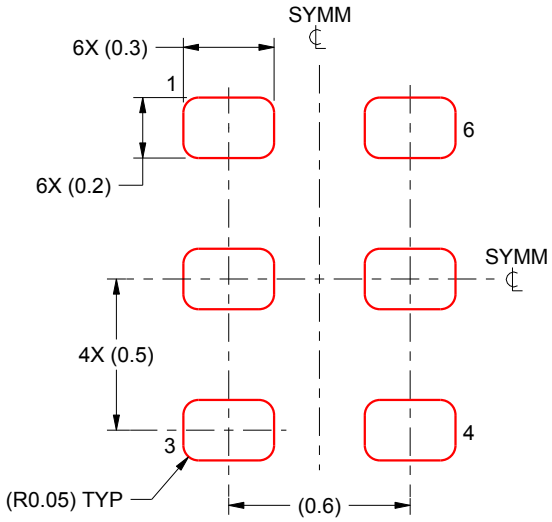
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DRY0006B

USON - 0.55 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222207/B 02/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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