Functional Safety Information

TPSF12C1
Functional Safety FIT Rate, FMD and Pin FMA

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Trademarks

1 Overview

This document contains information for the TPSF12C1 (SOT-23-THIN package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

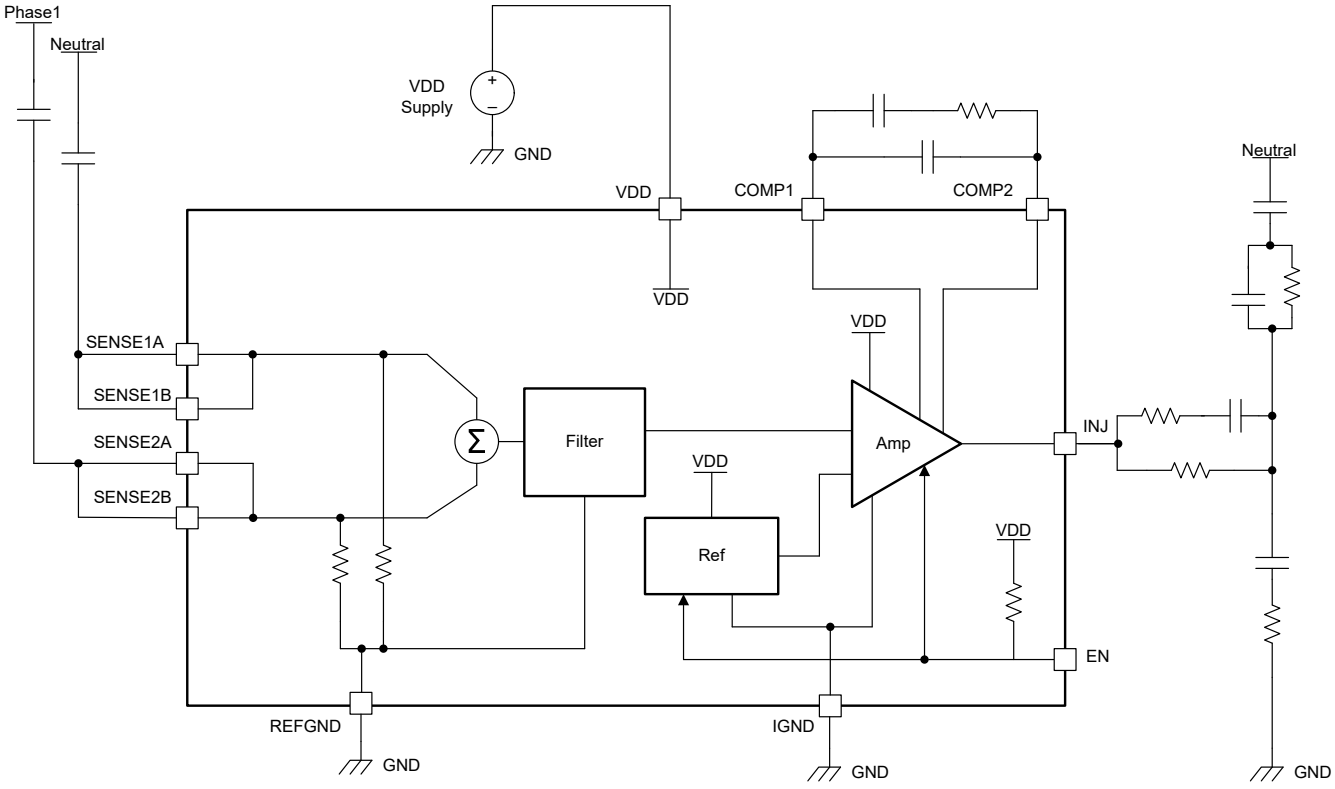

Figure 1-1. Functional Block Diagram

TPSF12C1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for the TPSF12C1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	13
Die FIT Rate	6
Package FIT Rate	7

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 270 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed signal less than 50 V supply	25 FIT	55°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for the TPSF12C1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution
INJ open (high impedance)	32%
INJ saturated high	6%
INJ saturated low	7%
INJ functional but not in specification	55%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TPSF12C1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2)
- Pin open-circuited (see Table 4-3)
- Pin short-circuited to an adjacent pin (see Table 4-4)
- Pin short-circuited to supply (see Table 4-5)

Table 4-2 through Table 4-5 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Figure 4-1 shows the TPSF12C1 pin diagram. For a detailed description of the device pins, please refer to the *Pin Configuration and Functions* section in the TPSF12C1 data sheet.

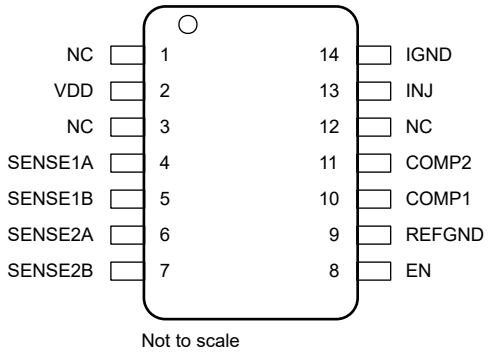

Figure 4-1. Pin Diagram

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- Application circuit, as per the *TPSF12C1 data sheet* is used.

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1, 3, 12	No impact	D
VDD	2	AEF disabled	B
SENSE1A	4	AEF degradation	B
SENSE1B	5	AEF degradation	B
SENSE2A	6	AEF degradation	B
SENSE2B	7	AEF degradation	B
EN	8	AEF disabled	B
REFGND	9	Normal operation	D
COMP1	10	No EMI filtering	B
COMP2	11	No EMI filtering; damage to gain stage	A
INJ	13	No EMI filtering; damage to gain stage	A
IGND	14	Normal operation	D

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1, 3, 12	No effect (normal operation)	D
VDD	2	No EMI filtering	B
SENSE1A	4	AEF degradation	B
SENSE1B	5	AEF degradation	B
SENSE2A	6	AEF degradation	B
SENSE2B	7	AEF degradation	B
EN	8	No effect (normal operation)	B
REFGND	9	AEF degradation	B
COMP1	10	No EMI filtering	B
COMP2	11	No EMI filtering	B
INJ	13	No EMI filtering	B
IGND	14	AEF degradation	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1	VDD	No effect (normal operation)	D
VDD	2	NC	No effect (normal operation)	D
NC	3	SENSE1	No effect (normal operation)	B
SENSE1A	4	SENSE1B	No effect (normal operation)	B
SENSE1B	5	SENSE2A	AEF degradation	B
SENSE2A	6	SENSE2B	No effect (normal operation)	B
SENSE2B	7	EN	N/A	D
EN	8	REFGND	No EMI filtering	B
REFGND	9	COMP1	No EMI filtering	B
COMP1	10	COMP2	No EMI filtering	B
COMP2	11	NC	No effect (normal operation)	D
NC	12	INJ	No effect (normal operation)	D
INJ	13	IGND	No EMI filtering; damage to gain stage	A
IGND	14	NC	No effect (normal operation)	D

Table 4-5. Pin FMA for Device Pins Short-Circuited to VDD

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
NC	1, 3, 12	No effect (normal operation)	D
VDD	2	No effect (normal operation)	D
SENSE1A	4	AEF degradation; damage to sensing stage	A
SENSE1B	5	AEF degradation; damage to sensing stage	A
SENSE2A	6	AEF degradation; damage to sensing stage	A
SENSE2B	7	AEF degradation; damage to sensing stage	A
EN	8	AEF normal	B
REFGND	9	AEF disabled	B
COMP1	10	No EMI filtering; damage to COMP1 if V_{VDD} > 5.5 V	A
COMP2	11	No EMI filtering; damage to COMP2 if V_{VDD} > 15 V	A
INJ	13	No EMI filtering; damage to gain stage	A
IGND	14	AEF disabled	B

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265