Application Note

TAx5xxx-Q1 Fault Diagnostic Features

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ABSTRACT

The TAx5xxx-Q1 family of devices are multichannel, high performance, analog-to-digital converters, and codecs intended for automotive audio applications. This application note details the integrated fault diagnostic features of this family and how the family of devices can be used for robust system design.

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1 Introduction

Automotive systems are designed to operate in a wide range of harsh environments. As greater amounts of electronics are integrated into automotive systems, the system complexity and potential for faults also increase. Multiple microphones are typically used for automotive audio systems that rely on algorithms like beamforming, active noise cancellation, or speech recognition. These algorithms depend on reliable data from microphones, and if one or more microphones in the system fail, the processing of unreliable data leads to erroneous calculations. In these automotive audio applications, microphones can be placed in remote locations far away from the PCB, such as in a wheel well, close to the engine, or at different positions in the passenger cabin. The remote placement of the microphone makes a wire harness to interface with the rest of the electronics necessary. Although extreme care is taken to prevent failure, over time these harnesses can degrade, resulting in faulty microphone connections. The new family of automotive audio data converters from Texas Instruments helps to address this challenge by providing integrated diagnostic monitoring features that determine when an input fault condition has occurred. With this information, the system can select how to respond and adjust system algorithms to handle the error.

2 Diagnostic Monitoring Architecture

Typical automotive audio applications favor the use of electret condenser microphones (ECM) for ease of mounting, interfacing, pickup directionality, moisture, and dust protection. These ECM microphones operate between 2 V to 10 V and can have large voltage swings. For accurate fault detection the ADC is required to interface directly with the microphone pins. For an AC-coupled application, designs require doubling the number of input pins as shown in Figure 2-1.

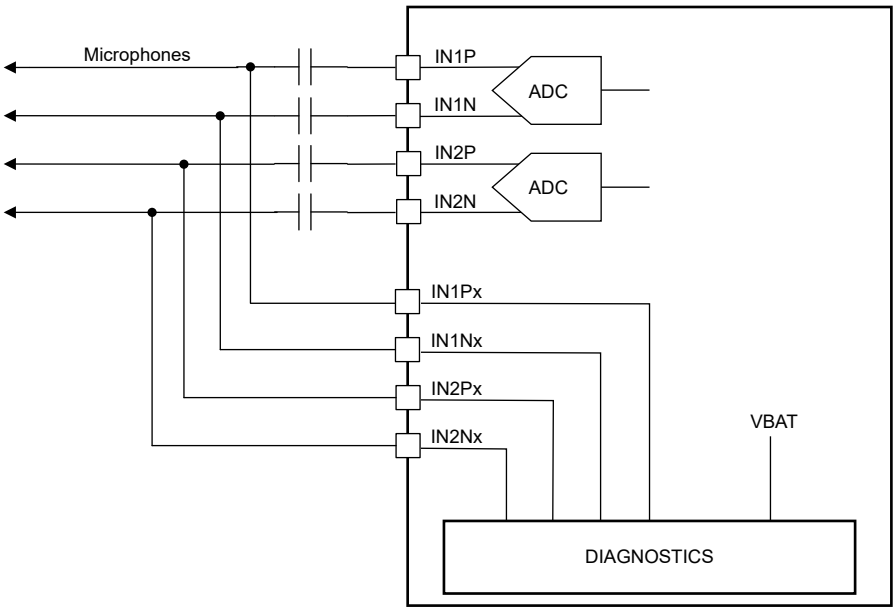


Figure 2-1. AC-coupled Diagnostics

This configuration also requires that the inputs use high-voltage transistors to handle the 10-VRMS swing directly. Together, these two factors lead to a very large solution size. Because of the doubling of input pin and added transistors, the TAx5xxx-Q1 family uses DC coupling for fault diagnostics with an attenuator on the front end of the signal chain to allow the input and the diagnostics to operate using a single pin. This design is shown in Figure 2-2.

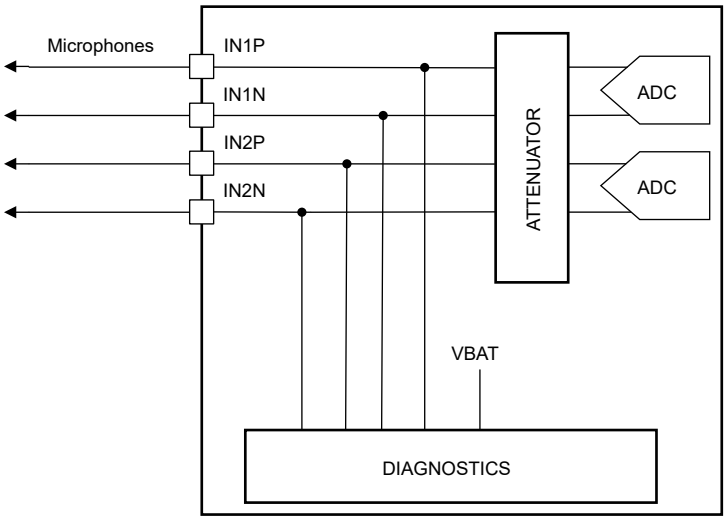


Figure 2-2. DC-coupled Diagnostics

AC coupling has benefits as well, such as higher input swing and more filtering flexibility. For applications that desire AC coupling with fault diagnostics, using a channel for AC-coupled analog inputs and dedicating the other channel to the DC-coupled diagnostics is possible. Figure 2-3 shows an example of channel 1 with AC-coupled microphone inputs and channel 2 is being used for microphone diagnostics. In this configuration, faults on channels 1 are recorded in the diagnostic registers for channel 2. Enabling the primary ADC for channel 2 is not necessary and is used only for diagnostics.

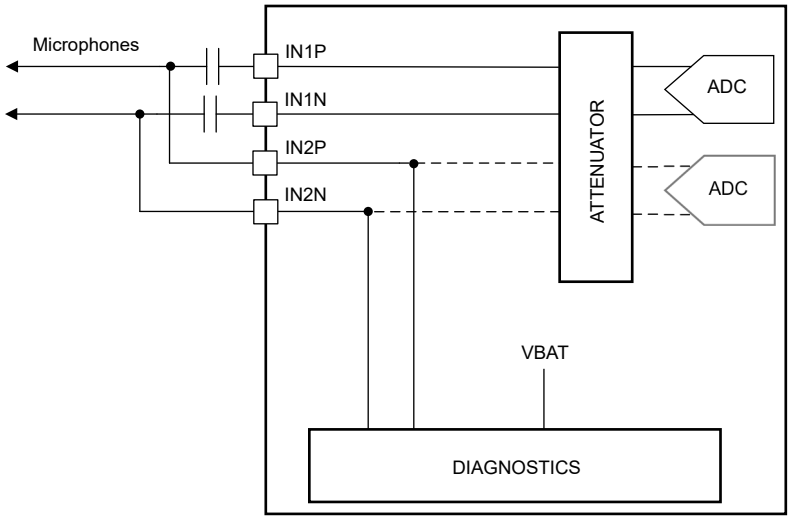


Figure 2-3. AC-coupled Inputs With DC Diagnostics

Figure 2-3 depicts a TAx5xxx diagnostic monitoring architecture for a fault monitoring signal chain.

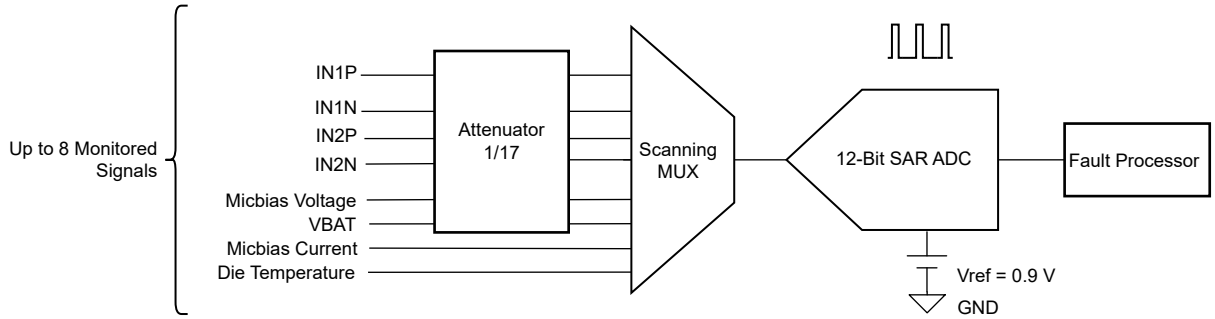


Figure 2-4. Diagnostics Monitoring Architecture

All of the input pins are monitored (4 pins for the 2-channel devices) along with the MICBIAS pin voltage, MICBIAS load current, VBAT_IN input, and internal die temperature. The input pins first pass through an attenuator, which scales the signal down by a factor of 17 before reaching the scanning multiplexer (MUX). The MUX automatically scans all inputs where diagnostics are enabled in a consecutive manner. The scan rate is adjustable in the DIAG_CFG3 register (Page 1, address 0x49). Once an input is selected by the scanning MUX, eight consecutive samples of the input are collected and averaged to improve the noise performance. Note that disabling the diagnostics for a channel is independent of disabling the channel, and diagnostics can still be read on inactive channels.

3 Monitored Faults

3.1 Microphone Faults

There are several ways that the microphone or the connections to the microphone can fail depending on the system implementation. For example, microphones themselves can degrade after prolonged exposure to extreme environmental conditions, excessive vibration or impact. Over time, cables connecting microphones to other electronics in the system can also degrade due to vibration, shock, or extreme temperature.

For robust detection, the Tax5xxx-Q1 monitors the input pins for the following faults:

- Inputs shorted to ground
- Inputs shorted to MICBIAS
- Input open circuit
- Input pins shorted together
- Input overvoltage detection
- Inputs shorted to VBAT

The input diagnostics of the TAx5xxx-Q1 family are designed with microphone inputs in mind, but can also be used for DC-coupled line inputs.

Most faults support user-programmable thresholds for detection. Faults can be individually enabled or disabled or masked. For the diagnostic monitoring to be active, MICBIAS must be turned on (even if MCBIAS is not actively used) since a number of faults rely on the measured value. Waiting at least 10 ms is recommended after powering up MICBIAS and the PLL before enabling fault diagnostic monitoring. Each fault reading is trimmed to an 8-bit accuracy to match the threshold programmability. Once detected, faults can be set to trigger interrupts on the GPIO pins or force channels to power down automatically. Each of the previously noted faults is described in the following sections.

3.1.1 Inputs Shorted to Ground

This fault triggers if the measured input pin voltage is less than the programmed threshold. This fault is programmable from 0 V to 900 mV with a programming resolution of 60 mV.

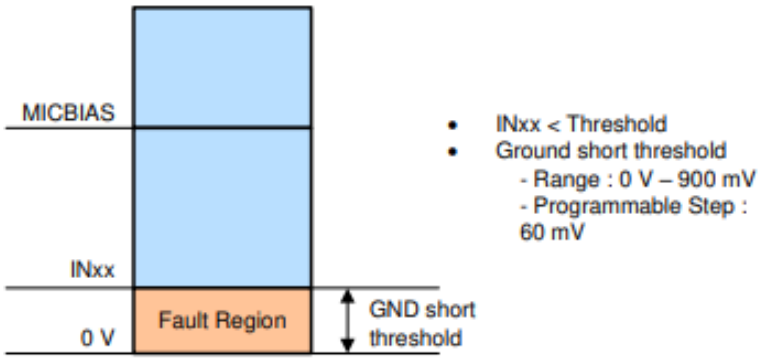


Figure 3-1. Input Short to GND Conditions

3.1.2 Inputs Shorted to MICBIAS

This fault is triggered if the difference between the voltage measured at the input pin and the voltage measured at the MICBIAS pin is greater than 0 V and less than the programmed threshold. This fault is programmable from 0 V to 450 mV with a programming step size of 30 mV. This fault uses the actual voltage measured at the MICBIAS pin, which can differ slightly from the programmed MICBIAS value.

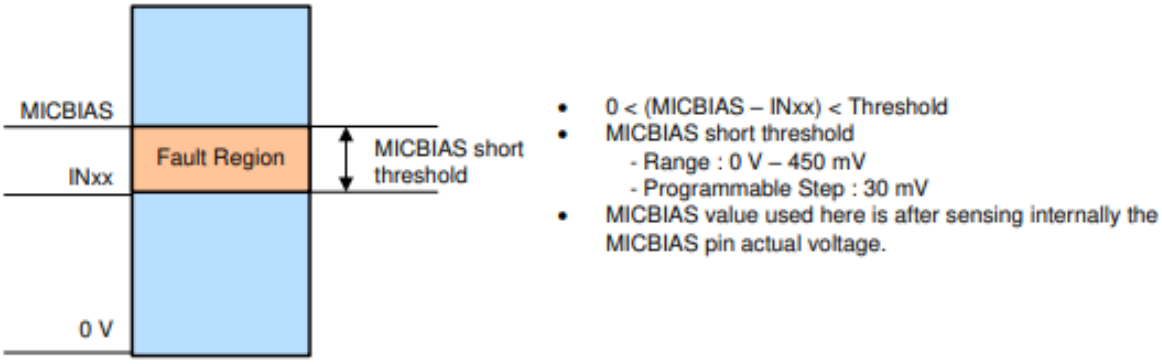


Figure 3-2. Input Short to MICBIAS Conditions

3.1.3 Input Open Circuit

This fault triggers when an open circuit condition is detected, which occurs from a combination of the previous two faults. This fault can trigger in two ways:

1. INxP is shorted to MICBIAS AND INxM is shorted to GND
2. INxP is shorted GND and INxM is shorted to MICBIAS

This fault relies on the thresholds programmed for these two respective faults.

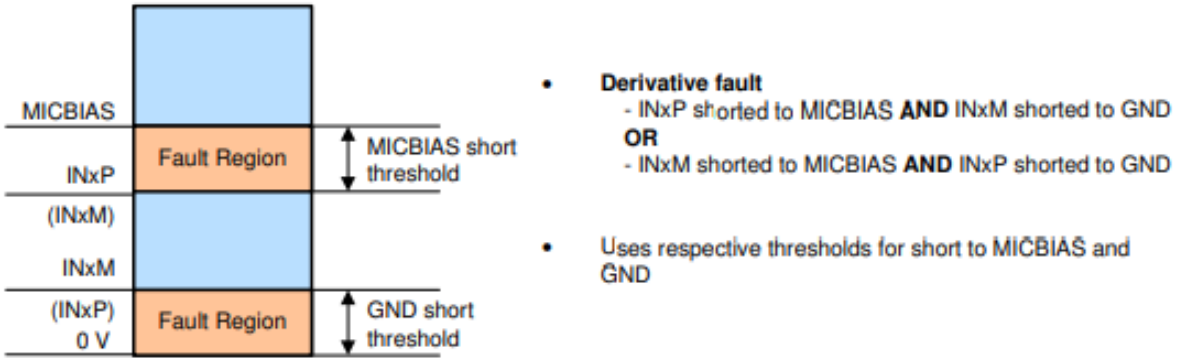


Figure 3-3. Input Open Circuit Conditions

3.1.4 Input Pins Shorted Together

This fault triggers when the absolute value of the difference between the input pins falls under the programmed threshold. This fault is programmable from 0 V to 450 mV in steps of 30 mV. In a typical DC-coupled application, there is a differential DC offset between the input pins from the microphone. This fault can trigger inadvertently in the application if the DC differential is kept below the programmed threshold.

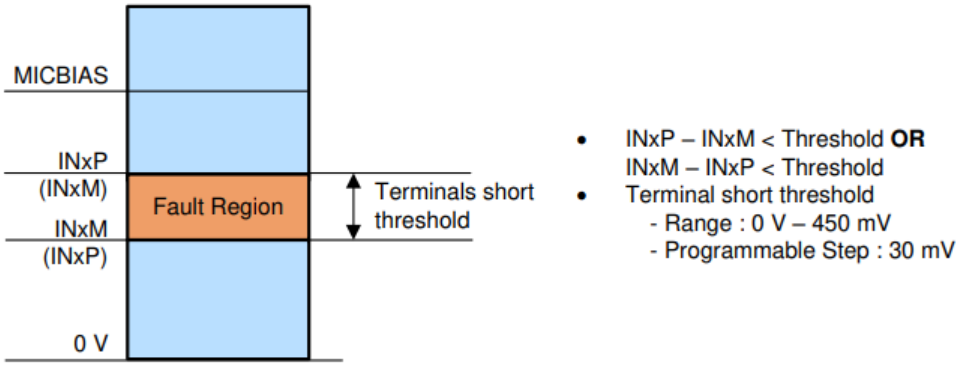


Figure 3-4. Inputs Shorted Conditions

3.1.5 Input Overvoltage Detection

This fault triggers when the measured input pin voltage is greater than the measured MICBIAS voltage. This threshold is not user programmable.

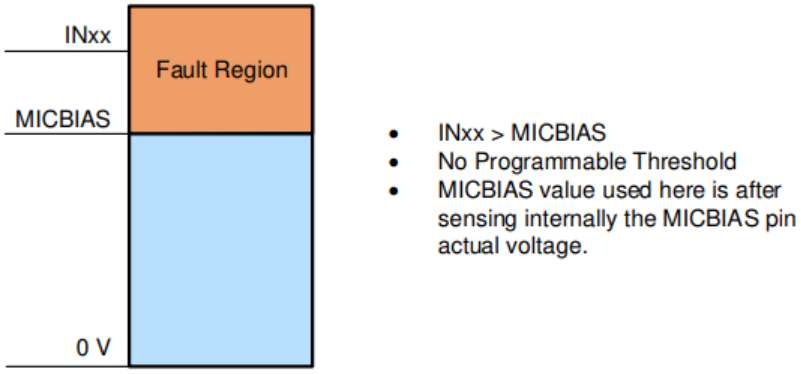
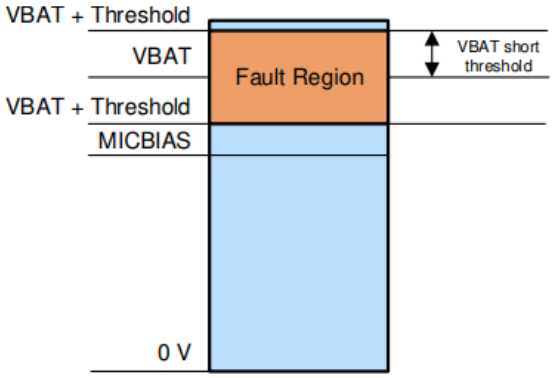


Figure 3-5. Input Overvoltage Conditions

3.1.6 Inputs Shorted to VBAT

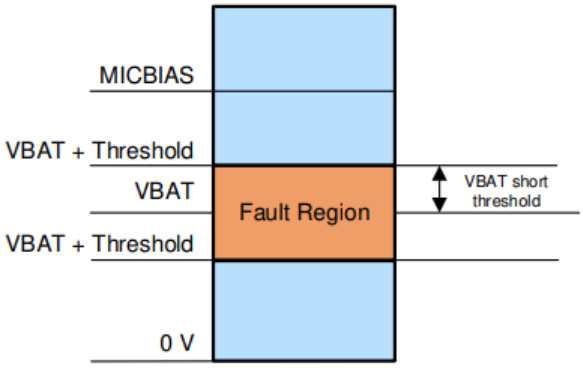
This fault triggers when the absolute value of the difference between the voltage applied to the VBAT pin and the input pin is less than the programmed threshold. The programmable range is 0 V to 450 mV in steps of 30 mV.



- |VBAT – INxx| < Threshold
- VBAT short threshold
  - Range : 0 V – 450 mV
  - Programmable Step : 30 mV
- MICBIAS value used here is after sensing internally the MICBIAS pin actual voltage.
- Max readable voltage is ~11.7 V therefore VBAT and/or INxx pins voltage above this will be detected as short.

Figure 3-6. Input Short to VBAT Conditions When VBAT > MICBIAS

In most automotive applications, the battery voltage is not expected to dip below MICBIAS, which has a maximum programmable value of 10 V. As long as VBAT is greater than MICBIAS, then a short to VBAT fault also produces an overvoltage fault. In rare cases, VBAT can be less than MICBIAS. This scenario can occur if the battery is heavily loaded or a voltage divider is used prior to VBAT_IN. In these cases, the fault can falsely trigger based on the signal level on the INxx pin. To avoid or minimize false detections, using the debounce and averaging features described in Section 6.3 are recommended. The debounce for this specific condition can be programmed independently from the other faults, or detection of this fault can be disabled altogether.



- VBAT < MICBIAS **AND**
- |VBAT – INxx| < Threshold
- VBAT short threshold
  - - Range : 0 V – 450 mV
  - - Programmable Step : 30 mV
- MICBIAS value used here is after sensing internally the MICBIAS pin actual voltage

Figure 3-7. Input Short to VBAT Conditions When VBAT < MICBIAS

3.2 Line Out Faults

Having robust line out fault diagnostics is of paramount importance for providing optimal audio quality and system reliability. Various factors such as electromagnetic interference (EMI), power supply fluctuations, and mechanical stresses can jeopardize the integrity of connections. For instance, EMI generated by the electrical systems of the vehicle or nearby devices can induce noise in audio connections. Furthermore, temperature variations and vibrations can lead to wear and tear on connectors, potentially resulting in intermittent or faulty connections. The diagnostics within the TAC5(3/4)1x-Q1 CODEC monitor the output pins for the following faults.

- Overcurrent
- Virtual ground

3.2.1 Output Overcurrent

This fault triggers when the current draw of OUTx is greater than 160 mA, shorts to supply, or if there is a short to ground.

3.2.2 Virtual Ground

Preceding the output pins is an amplifier operating at AVDD that creates a midpoint voltage to serve as a reference point for the analog input signal. This midpoint voltage, shown as V_ICM (which stands for "internal common-mode") in Figure 3-8, is referred to as the virtual ground. A fault is triggered if there is a short at OUTx that brings the virtual ground to unintended high voltages. Furthermore, a fault can be triggered under the following conditions:

- If the analog input signal common mode is higher than 100 mV, thus breaking the limitation of R_{BYP} and bringing the virtual ground to unintended high voltages. This is only applicable when the device output configuration is fully-differential.
- If the device is configured to have a 6-db or 12-dB gain in bypass and the input signal is greater than -6-dB or -12-dB respectively. This is applicable to single-ended or fully-differential output configurations.
- If the analog input level exceeds the full scale input signal range for the respective input configuration.

Correct configuration of the output registers for channel 1 (P0_R100-R102) and channel 2 (P0_R107-R109) is essential to prevent unintended virtual ground fault detection. In the event a virtual ground fault is detected, the user must check the output configuration registers and verify compliance with the input signal and voltages.

In addition, the DAC output stage is shown in Figure 3-8 and if the voltage measured at OUTx exceeds the design limits of the device, this fault triggers. The user has the ability to program the device in DAC_FLT_CFG (P0_R67) to power down the playback path of the DAC upon fault detection.

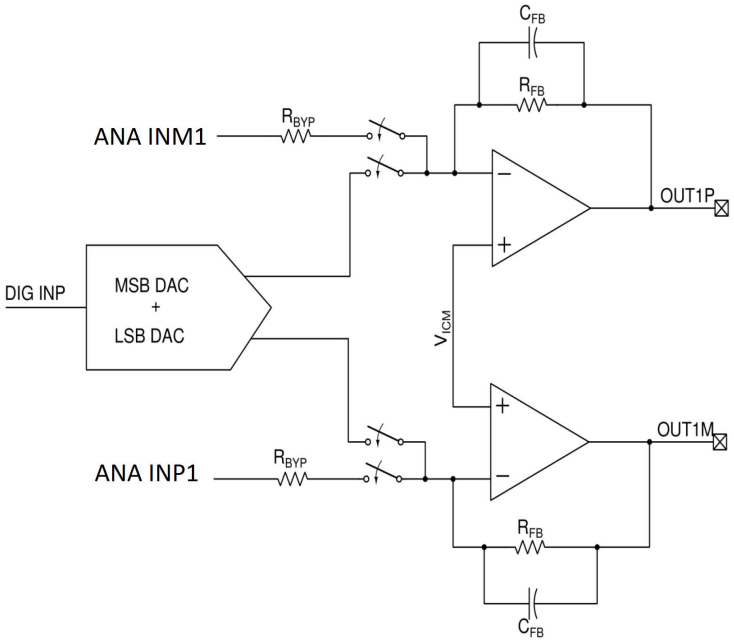


Figure 3-8. Virtual Ground Output Configuration

3.3 Other Faults

3.3.1 MICBIAS Overvoltage

If the MICBIAS pin is pulled to a voltage higher than what is set in the MICBIAS_CFG register (P0_R115), then a MICBIAS overvoltage fault triggers. This can occur, for instance, if MICBIAS is shorted to VBAT. When this fault is triggered the device sets the overvoltage status flag in the INT_LTCH2 (P0_R59_D0) and INT_LIVE2 register. The threshold for overvoltage detection can be adjusted in the DIAG_CFG11 register (P1_R81).

3.3.1.1 DIAG_CFG11 Register (page = 0x01, address = 0x51) [Reset = 0x40]

This register is the MICBIAS overvoltage configuration register.

Table 3-1. DIAG_CFG11 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7-5	SAFEBAND_MBIAS_OV_FLT[2:0]	R/W	010b	Safeband configuration for lower boundary of MBIAS overvoltage fault 0 = No safeband 1 = 30-mV safeband (1 LSB at 9b lvl) 2 = 60-mV safeband (2 LSB at 9b lvl) 3-7 = N × 30 mV
4-0	RESERVED	R	00000b	Reserved bits; Write only reset values

(1) R/W = Read and Write; R = Read

3.3.2 MICBIAS Overcurrent

The MICBIAS pin has an integrated overcurrent protection circuit that protects the device from damage due to excessive current draw. The MICBIAS pin is specified up to 30-mA continuous current draw. Though the exact current that triggers an overcurrent protection fault varies device-to-device, the minimum threshold that the fault can trigger at is 45 mA. Once the overcurrent protection has been triggered, the device sets the overcurrent status flag in the INT_LTCH2 (P1_R59_D3 bit) register and limits the output current of the MICBIAS pin.

3.3.3 MICBIAS Load Current

Separate from the overcurrent protection, an internal current sensor monitors the loading on the MICBIAS pin of the device. This feature can be programmed to trigger a fault if the current exceeds the maximum programmed value or falls under the minimum expected load. Note that the programmed threshold is only used for fault detection and does not limit the current supplied by the MICBIAS pin. The high- and low-current thresholds can be programmed from 0 mA to 30 mA (default lower and upper thresholds are 2.6 mA and 18 mA, respectively) with a resolution of 0.117 mA. These thresholds are programmed in DIAG_CFG6 (Page 1, address 0x4C) and DIAG_CFG7 (Page 1, address 0x4D). Since the device is only specified up to 30 mA, the device is not recommended to set the high load current threshold greater than 30 mA.

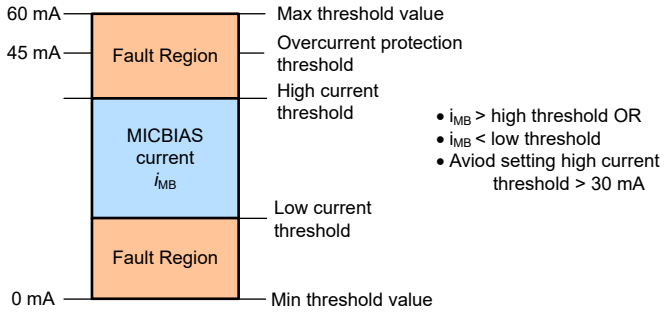


Figure 3-9. MICBIAS Load Current Conditions

3.3.3.1 DIAG_CFG6 Register (page = 0x01, address = 0x4C) [Reset = 0xA2]

This is the MICBIAS diagnostic configuration register for setting the high current threshold.

Table 3-2. DIAG_CFG6 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7-0	MBIAS_HIGH_CURR_THRS[7:0]	R/W	10100010b	Threshold for MICBIAS high-current fault diagnostics Default ≅ 18 mA Nd = ((0.9×(N×16)/4095)-0·2)×48.46154 (mA)

(1) R/W = Read or Write

3.3.3.2 DIAG_CFG7 Register

This is the MICBIAS diagnostic configuration register for setting the low current threshold.

Table 3-3. DIAG_CFG7 Register Field Descriptions

Bit	Field	Type(1)	Reset	Description
7-0	MBIAS_LOW_CURR_THRS[7:0]	R/W	01001000b	Threshold for MICBIAS low-current fault diagnostics Default ≅ 2.6 mA Nd = ((0.9×(N×16)/4095)-0·2)×48.46154 (mA)

(1) R/W = Read or Write

3.3.4 Overtemperature Fault

An overtemperature protection circuit monitors the die temperature and sets the status flag in the INT_LTCH0 (P1_R52_D5) register whenever the die junction temperature exceeds the supported level. The exact level at which this fault triggers varies device-to-device, but does not occur within the specified operating range and is intended to protect the IC from damage.

3.3.5 Supply Back Pumping

Due to the complex nature of circuits within automotive systems, connections can easily be shorted to one another, jeopardizing the integrity of audio system. As an example, the MICBIAS pin can potentially short to the primary battery supply, VBAT, and drive the MICBIAS to a higher voltage thus unintentionally pumping current back through the MICBIAS pin. A traditional MICBIAS does not have the ability to synchronize current if unintentionally shorted to another power supply source, so this hazard induces a reliability issue in the system. The TAx5x1x-Q1 integrates important protective features within the audio device to prevent back-pumping from damaging the integrity of the device.

As shown in Figure 3-10, the MICBIAS pin monitors any variations in the bias voltage and has integrated circuitry to synchronize current with a higher voltage in the case of back-pumping. Back-pumping or a sudden change in the power supply voltage (for example, a voltage spike or dip) can propagate through the MICBIAS pin, boost, HVDD, and the microphone. These pins are protected from reverse current and a short to a voltage higher than the programmed maximum threshold to provide a stable bias voltage for the microphone and a clean power supply for TAx5xxx-Q1.

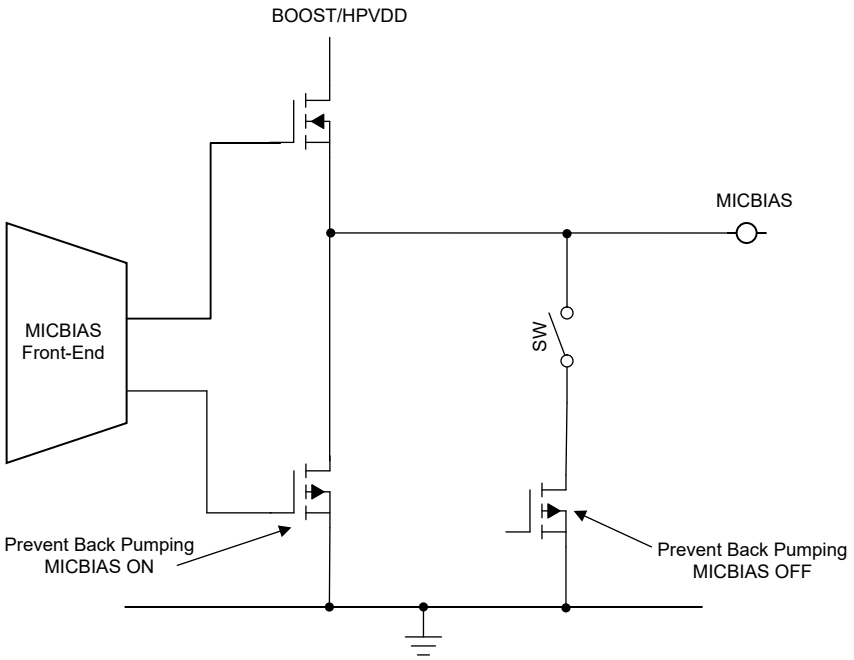


Figure 3-10. Supply Back Pumping Diagram

4 Enabling Diagnostics and Programming Thresholds

The primary diagnostic configuration registers are registers 70 through 74. These registers control which channels are scanned for faults and the thresholds for each of the faults. The first of these registers, DIAG_CFG0 (P1_R70), allows the user to enable or disable diagnostic monitoring on each of the input channels, respectively. Bit 4 of DIAG_CFG0 controls diagnostic monitoring on AC-coupled channels. Although the microphone connectivity can not be diagnosed when using AC coupling, the diagnostics does provide pin-level monitoring of the ADC to determine if any shorts have occurred at the PCB level. Bit 5 of DIAG_CFG0 controls whether the INxM pins are monitored for single-ended input channels. This feature can be useful in pseudo-differential input configurations where INxM is held at a constant voltage but is not grounded. This functionality also can be used if the ground connection is located away from the board or for detecting a loss of ground condition.

4.1 DIAG_CFG0 Register (page = 0x01, Address = 0x46) [Reset = 0x00]

This register is configuration register 0 for input fault diagnostics setting.

Table 4-1. DIAG_CFG0 Register Field Descriptions

Bit	Field	Type(1)	Reset	Description
7	IN_CH1_DIAG_EN	R/W	0b	Channel-1 Input (IN1P and IN1M) Scan for diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled
6	IN_CH2_DIAG_EN	R/W	0b	Channel-2 Input (IN2P and IN2M) Scan for diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled
5	INCL_SE_INM	R/W	0b	INxM pin Diagnostics scan selection for single-ended configuration 0b = INxM pins of single-ended channels are excluded for diagnosis 1b = INxM pins of single-ended channels are included for diagnosis
4	INCL_AC_COUP	R/W	0b	AC-coupled channels pins Scan selection for diagnostics 0b = INxP and INxM pins of AC-coupled channels are excluded for diagnosis 1b = INxP and INxM pins of AC-coupled channels are included for diagnosis
3	RESERVED	R/W	0b	Reserved bit; Write only reset value
2	RESERVED	R/W	0b	Reserved bit; Write only reset value
1	RESERVED	R/W	0b	Reserved bit; Write only reset value
0	RESERVED	R/W	0b	Reserved bit; Write only reset value

(1) R/W = Read or Write

Applications differ in expected signal levels because of DC-coupled inputs, a broad selection of microphones to choose from, and flexibility in how those microphones are biased. Threshold programmability allows each fault to be set at a reasonable level and tailored to the application. The default values for these thresholds are set to be the most commonly used values. DIAG_CFG1 allows the user to configure the thresholds used for the INxP to INxM terminal short detection and the short to VBAT_IN detection.

4.2 DIAG_CFG1 Register (page = 0x01, Address = 0x47) [Reset = 0x37]

This register is configuration register 1 for input fault diagnostics setting.

Table 4-2. DIAG_CFG1 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7-4	DIAG_SHT_TERM[3:0]	R/W	0011b	INxP and INxM Terminal Short Detect Threshold 0d = INxP and INxM Terminal Short Detect Threshold Value is 0 mV 1d = INxP and INxM Terminal Short Detect Threshold Value is 30 mV 2d = INxP and INxM Terminal Short Detect Threshold Value is 60 mV 10d to 13d = INxP and INxM Terminal Short Detect Threshold Value is as per configuration 14d = INxP and INxM Terminal Short Detect Threshold Value is 420 mV 15d = INxP and INxM Terminal Short Detect Threshold Value is 450 mV
3-0	DIAG_SHT_VBAT_IN[3:0]	R/W	0111b	Short to VBAT_IN Detect Threshold 0d = Short to VBAT_IN Detect Threshold Value is 0 mV 1d = Short to VBAT_IN Detect Threshold Value is 30 mV 2d = Short to VBAT_IN Detect Threshold Value is 60 mV 10d to 13d = Short to VBAT_IN Detect Threshold Value is as per configuration 14d = Short to VBAT_IN Detect Threshold Value is 420 mV 15d = Short to VBAT_IN Detect Threshold Value is 450 mV

(1) R/W = Read or Write

DIAG_CFG2 similarly allows the user to configure the thresholds used for short to ground detection and short to MICBIAS.

4.3 DIAG_CFG2 Register (page = 0x01, Address = 0x48) [Reset = 0x87]

This register is configuration register 2 for input fault diagnostics setting.

Table 4-3. DIAG_CFG2 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7-4	DIAG_SHT_GND[3:0]	R/W	1000b	Short to GND Detect Threshold 0d = Short to GND Detect Threshold Value is 0 mV 1d = Short to GND Detect Threshold Value is 60 mV 2d = Short to GND Detect Threshold Value is 120 mV 10d to 13d = Short to GND Detect Threshold Value is as per configuration 14d = Short to GND Detect Threshold Value is 840 mV 15d = Short to GND Detect Threshold Value is 900 mV
3-0	DIAG_SHT_MICBIAS[3:0]	R/W	0111b	Short to MICBIAS Detect Threshold 0d = Short to MICBIAS Detect Threshold Value is 0 mV 1d = Short to MICBIAS Detect Threshold Value is 30 mV 2d = Short to MICBIAS Detect Threshold Value is 60 mV 10d to 13d = Short to MICBIAS Detect Threshold Value is as per configuration 14d = Short to MICBIAS Detect Threshold Value is 420 mV 15d = Short to MICBIAS Detect Threshold Value is 450 mV

(1) R/W = Read or Write

DIAG_CFG4 contains advanced monitoring feature settings. Bit 0 controls threshold scaling. Setting Bit 0 high doubles the value of the configured thresholds, effectively expanding the range of a 450-mV threshold to 900 mV. This setting applies to all diagnostic thresholds. See Section 6.3.2.1 for the DIAG_CFG4 register definition.

5 Fault Diagnostic Setup Procedure

Figure 5-1 shows the suggested flow for setting up fault diagnostics. Each feature is described in more detail in the following sections. Some applications do not use all features or rely on the default values in the configuration registers. At a minimum, the user must power up MICBIAS and enable the channel diagnostics.

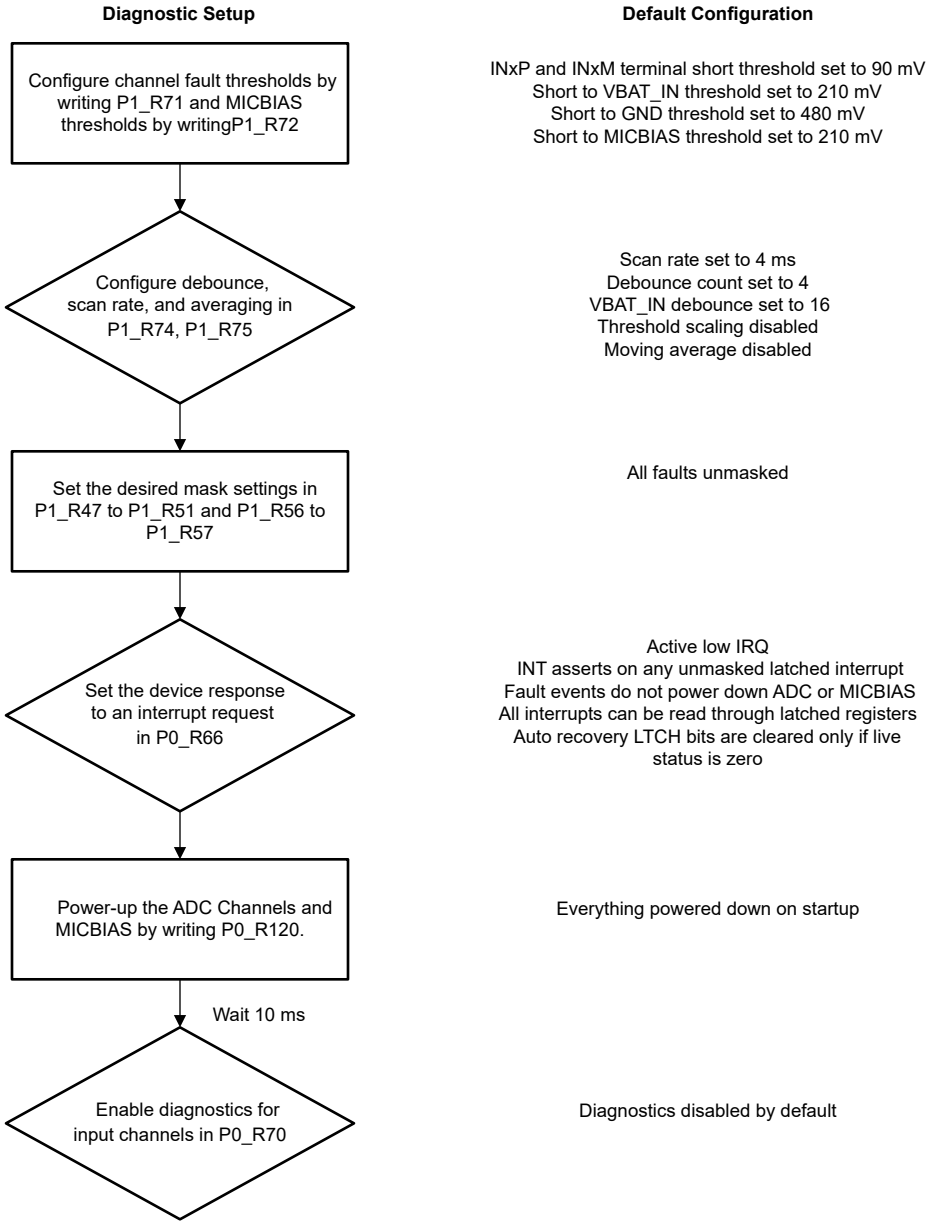


Figure 5-1. Diagnostic Setup Procedure

6 Fault Reporting

Faults are reported in live and latched status registers based on the settings used for fault detection.

6.1 Live Registers

The live registers, P1_R61 to P1_R67, are updated continuously with each new scan and report the most recent measurements recorded by the diagnostics processor. The CHx_LIVE register (P1_R61) contains a summary of present faults allowing the user to determine which channels have active faults.

6.1.1 CHx_LIVE Register (page = 0x01, address = 0x3D) [Reset = 0b]

This register is the live Interrupt status register for channel level diagnostic summary.

Table 6-1. CHx_LIVE Register Field Descriptions

Bit	Field	Type(1)	Reset	Description
7	STS_CHx_LIVE	R	0b	Status of Input CH1_LIVE 0b = No faults occurred in input channel 1 1b = Fault or faults have occurred in input channel 1
6	STS_CHx_LIVE	R	0b	Status of Input CH2_LIVE 0b = No faults occurred in input channel 2 1b = Fault or faults have occurred in input channel 2
5	STS_CHx_LIVE	R	0b	Status of Output CH1_LIVE 0b = No faults occurred in output channel 1 1b = Fault or faults have occurred in output channel 1
4	STS_CHx_LIVE	R	0b	Status of Output CH2_LIVE 0b = No faults occurred in output channel 2 1b = Fault or faults have occurred in output channel 2
3	STS_CHx_LIVE	R	0b	Status on fault due to "Short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS" 0b = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS did NOT occur in any channel 1b = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in at least one channel
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

(1) R = Read

The respective CH_LIVE registers P0_R63 and P0_R64 contain the details of exactly which faults occurred on a given channel. Section 6.1.2 shows CH1_LIVE register for reference.

6.1.2 CH1_LIVE Register (page = 0x01, address = 0x3E) [Reset = 0h]

This register is the live Interrupt status register for channel 1 fault diagnostic

Table 6-2. IN_CH1_LIVE Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7	IN_CH1_LIVE	R	0b	Input Channel-1 Open Inputs 0b = No Open Inputs 1b = Open Inputs
6	IN_CH1_LIVE	R	0b	Input Channel-1 Inputs Shorted 0b = No Input Shorted 1b = Input Shorted to each other
5	IN_CH1_LIVE	R	0b	Input Channel-1 INP Shorted to GND 0b = INP not shorted to GND 1b = INP shorted to GND
4	IN_CH1_LIVE	R	0b	Input Channel-1 INM Shorted to GND 0b = INM not shorted to GND 1b = INM shorted to GND
3	IN_CH1_LIVE	R	0b	Input Channel-1 INP Shorted to MICBIAS 0b = INP not shorted to MICBIAS 1b = INP shorted to MICBIAS
2	IN_CH1_LIVE	R	0b	Input Channel-1 INM Shorted to MICBIAS 0b = INM not shorted to MICBIAS 1b = INM shorted to MICBIAS
1	IN_CH1_LIVE	R	0b	Input Channel-1 INP Shorted to VBAT_IN 0b = INP not shorted to VBAT_IN 1b = INP shorted to VBAT_IN
0	IN_CH1_LIVE	R	0b	Input Channel-1 INM Shorted to VBAT_IN 0b = INM not shorted to VBAT_IN 1b = INM shorted to VBAT_IN

(1) R = Read

In addition to the channel registers, there are also interrupt registers that contain various faults. The first of these registers, INT_LIVE0 (P1_R60), contains the boost-protection fault flags as well as the ASI bus clock error and PLL lock status. The PLL lock status is not a fault, but provides a method to monitor when the state of the PLL changes. For more information on ASI bus clock errors, see the device data sheet.

6.1.3 INT_LIVE0 Register (page = 0x01, address = 0x3C) [Reset = 00]

This register is the live Interrupt readback register 0.

Table 6-3. INT_LIVE0 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7	INT_LIVE0	R	0b	Interrupt due to clock error 0b = No interrupt 1b = Interrupt
6	INT_LIVE0	R	0b	Interrupt due to PLL Lock 0b = No interrupt 1b = Interrupt
5	INT_LIVE0	R	0b	Interrupt due to Boost Over Temperature 0b = No interrupt 1b = Interrupt
4	INT_LIVE0	R	0b	Interrupt due to Boost Over Current 0b = No interrupt 1b = Interrupt
3	INT_LIVE0	R	0b	Interrupt due to Boost MO 0b = No interrupt 1b = Interrupt
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	Reserved bit; Write only reset value

(1) R = Read

INT_LIVE1 (P1_R66) contains the overvoltage fault status for each of the INxP pins of the device. Similarly, INT_LIVE2 (P1_R67) contains the MICBIAS faults that do not pertain to the device's self-protection features.

6.1.4 INT_LIVE1 Register (page = 0x00, address = 0x42) [reset = 0x00]

This register is the live interrupt readback register 1.

Table 6-4. INT_LIVE1 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7	INT_LIVE1	R	0b	Channel-1 INP Over Voltage 0b = No INP Over Voltage fault 1b = INP Over Voltage fault has occurred
6	INT_LIVE1	R	0b	Channel-1 INM Over Voltage 0b = No INM Over Voltage fault 1b = INM Over Voltage fault has occurred
5	INT_LIVE1	R	0b	Channel-2 INP Over Voltage 0b = No INP Over Voltage fault 1b = INP Over Voltage fault has occurred
4	INT_LIVE1	R	0b	Channel-2 INM Over Voltage 0b = No INM Over Voltage fault 1b = INM Over Voltage fault has occurred
3	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
2	RESERVED	R	0b	Reserved bit; Write only reset value
1	RESERVED	R	0b	Reserved bit; Write only reset value
0	RESERVED	R	0b	

(1) R = Read

6.1.5 INT_LIVE2 Register (page = 0x00, address = 0x43) [reset = 0x00]

Table 6-5. INT_LIVE2 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7	INT_LIVE2	R	0b	Interrupt due to GPA up threshold fault 0b = No interrupt 1b = Interrupt
6	INT_LIVE2	R	0b	Interrupt due to GPA low threshold fault 0b = No interrupt 1b = Interrupt
5	INT_LIVE2	R	0b	Interrupt due to VAD power up detect 0b = No interrupt 1b = Interrupt
4	INT_LIVE2	R	0b	Interrupt due to VAD power down detect 0b = No interrupt 1b = Interrupt
3	INT_LIVE2	R	0b	Interrupt due to MICBIAS short circuit condition 0b = No interrupt 1b = Interrupt
2	INT_LIVE2	R	0b	Interrupt due to MICBIAS High current fault 0b = No interrupt 1b = Interrupt
1	INT_LIVE2	R	0b	Interrupt due to MICBIAS Low current fault 0b = No interrupt 1b = Interrupt
0	INT_LIVE2	R	0b	Interrupt due to MICBIAS Over voltage fault 0b = No interrupt 1b = Interrupt

(1) R = Read

6.2 Latched Registers

The latched registers are set up to mirror the live registers. The latched status of each diagnostic fault is reported by the channel in P1_R54 to P1_R57, and a latched summary of all channels is reported in CHx_LTCH, P1_R53. The latched registers are latched when the associated bit in the live fault registers transitions from a 0 to a 1 and the conditions set in the fault filtering registers are met. A transition of any bit in the latched register from a 0 to 1 triggers an interrupt request. By default, latched registers are cleared after reading only if the fault is no longer present and the associated live register reports 0, otherwise the register remains latched. There is an additional mode in which the latched registers clears, regardless of the status of the associated live registers. This feature is useful for identifying unique faults as only one interrupt is generated per fault. This feature can be enabled by setting the LTCH_CLR_ON_READ bit to 1 in the INT_CFG register.

6.2.1 Clearing Latched Registers

Most of the latched registers in the device are self-clearing and reset upon reading as previously described. However, the mapping of some registers causes the registers to clear only when another latched register is read. Registers that exhibit this behavior include a description in the register map stating which register needs to be read for the bit to clear. This behavior applies to the INxM short to VBAT_IN faults in the channel latch registers as well as the INxP and INxM overvoltage status bits in INT_LTCH1. Reading all latched registers any time a fault is detected is recommended to verify all bits are cleared. To verify no faults are missed, a recommended read sequence is provided in Section 7.3.

6.3 Fault Filtering and Response Time

The DIAG_CFG4 and DIAG_CFG5 registers contain several settings that allow the user to adjust the response time of the device to a fault condition. These settings control how often the MUX switches to check for faults and how long a fault must be present before being latched in the associated latched register.

6.3.1 Debounce

A debounce filter can be applied to diagnostic measurements. This debounce is analogous to the switch debounce often used in analog circuitry. Once a fault condition occurs, with debounce enabled, the device does not trigger a fault until it counts the programmed number of consecutive values within fault thresholds. The debounce can be programmed for 4, 8, or 16 counts to filter out transient events. All faults share the same debounce setting with the exception of VBAT_IN short when VBAT_IN is less than MICBIAS. Since in this circumstance false triggers are more likely to occur under normal operating conditions, the debounce setting for this fault can be programmed independently to 8 or 16 counts. The debounce settings are contained in the DIAG_CFG4 register (Page 1, address 0x4A).

6.3.2 Scan Rate

When diagnostics are enabled, the fault diagnostic signal chain is constantly scanning the input channels. This multiplexing occurs automatically, but the rate at which the channels are scanned can be adjusted in DIAG_CFG4. The repetition rate can be set to 1 ms, 4 ms, 8 ms, or set to continuously scan as fast as possible. The default scan rate is 4 ms. The scan rate is the time between the end of one scan cycle and the beginning of the next. Since the sample rate of the diagnostic ADC is typically much faster than the scan rate, the scan rate is effectively the time between fault readings. Using the continuous back-to-back scan mode is recommended for the fastest response time and greatest signal integrity for the record channel. This selection causes the diagnostic ADC to sample at the same rate as the audio ADC and eliminates the small amount of coupling distortion that can arise from discontinuities in the diagnostic sampling. The power consumption of the diagnostic signal chain scales with the scan repetition rate. In back-to-back continuous scanning, the AVDD current can be expected to increase by approximately 2.5 mA compared to the 4-ms scan rate setting. For this reason, continuously scanning in power-sensitive applications is not recommended unless a system is particularly prone to faults and fast response time is needed.

6.3.2.1 DIAG_CFG4 Register (page = 0x01, address = 0x4A) [reset = 0xB8]

This register is configuration register 4 for input fault diagnostics setting.

Table 6-6. DIAG_CFG4 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7-6	REP_RATE[1:0]	R/W	10b	Fault monitoring scan repetition rate 0d = Continuous back to back scanning of selected channels input pins without any idle time 1d = Fault monitoring repetition rate of 1 ms for selected channels input pins scanning 2d = Fault monitoring repetition rate of 4 ms for selected channels input pins scanning 3d = Fault monitoring repetition rate of 8 ms for selected channels input pins scanning
5-4	RESERVED	R/W	11b	Reserved bits; Write only reset values
3-2	FAULT_DBNCE_SEL[1:0]	R/W	10b	Debounce count for all the faults (except VBAT_IN short when VBAT_IN < MICBIAS) 0b = 16 counts for debounce to filter-out false faults detection 1b = 8 counts for debounce to filter-out false faults detection 2b = 4 counts for debounce to filter-out false faults detection 3b = No debounce count
1	VSHORT_DBNCE	R/W	0b	VBAT_IN short debounce count 0b = 16 counts for debounce to filter-out false faults detection 1b = 8 counts for debounce to filter-out false faults detection
0	DIAG_2X_THRES	R/W	0b	Diagnostic thresholds range scale 0d = Thresholds same as configured 1d = All the configuration thresholds gets scale by 2 times

(1) R/W = Read or Write

6.3.3 Moving Average

For more robust detection, the fault monitoring can be based on the moving average of the diagnostic signal. With this setting enabled, each new sample is averaged with the previous set of samples and if a fault occurs, the latched registers does not latch until the average of the samples crosses the programmed threshold. This

setup acts as a simple FIR filter and avoids triggering faults from transient events in the system. If debounce and moving average are used together, then the latched register does not latch until the moving average of consecutive samples crosses the programmed threshold and remains there for the programmed debounce count. The moving average can be set to weigh new and old data equally, or skewed to give old data 0.75 weight and new data a 0.25 weight to further improve transient immunity. The moving average setting is common to all input channels, but can be enabled or disabled independently for the MICBIAS load current and overtemperature faults to achieve faster response times for these faults. Moving average settings are contained in the DIAG_CFG5 register (Page 1, address 0x4B).

6.3.3.1 DIAG_CFG5 Register (page = 0x01, address = 0x4B) [reset = 0h]

This register is configuration register 5 for input fault diagnostics setting.

Table 6-7. DIAG_CFG5 Register Field Descriptions

Bit	Field	Type[1]	Reset	Description
7-6	DIAG_MOV_AVG_CFG[1:0]	R/W	00b	Moving average configuration 0d = Moving average disabled 1d = Moving average enabled with 0.5 weightage for new and old data 2d = Moving average enabled with 0.75 weightage for old data and 0.25 weightage for new data 3d = Reserved
5	MOV_AVG_DIS_MBIAS_LOAD	R/W	0b	Moving average configuration for MICBIAS Load channel 0b = Moving average is enabled for MICBIAS Load channel 1b = Moving average is disabled for MICBIAS Load channel
4	MOV_AVG_DIS_TEMP_SENS	R/W	0b	Moving average configuration for Temp Sense channel 0b = Moving average is enabled for Temp Sense channel 1b = Moving average is disabled for Temp Sense channel
3	MOV_AVG_DIS_GPA	R/W	0b	Moving average configuration for GPA channel 0b = Moving average is enabled for GPA channel 1b = Moving average is disabled for GPA channel
2-0	RESERVED	R	000b	Reserved bits; Write only reset values

(1) R/W = Read or Write; R = Read

If the moving average feature is not used, the fault response time can be calculated as the scan rate multiplied by the debounce setting. For example, a debounce of 8 and scan rate of 4 ms requires a fault to be present for 32 ms before latching the corresponding fault register. This behavior is useful for filtering out transient behaviors, such as the start-up response of a microphone. If the moving average feature is used, then the exact response time depends on the nature of the fault and the amplitude of the input signal causing the fault. This setting can be useful in particularly noisy applications in which the microphone is prone to saturate for a portion of the time. Setting the scan rate to continuous provides the fastest response. The exact response time depends on many factors. To simplify calculation, the following equation shows how to calculate the effective response time in back-to-back scan mode.

$$Response\ \ Time\ \ = \ \ (450\ \times N + 1000) \times DIAG\_CLK\_PERIOD \quad (1)$$

Where

- *N* is the number of channels (1 to 2) enabled for diagnostics scan using page-0, register-70d
- And *DIAG_CLK_PERIOD* is the period of the clock used for the diagnostic state-machine

The diagnostic clock period depends on whether valid clocks are present and the sample rate. The diagnostic clock frequency is 6.144 MHz for all ASI sample rate multiples and sub-multiples of 48 kHz. Similarly, the frequency is 5.644 MHz for all ASI sample rate multiples and sub-multiples of 44.1 kHz. If no clocks are present or there is an error in the clocks, then the diagnostic clock defaults to the 5-MHz (typical) clock generated using the internal on-chip oscillator.

Live registers always report the most recent reading and are not influenced by the debounce or moving average settings. The faults in INT_LTCH0 are also not affected by these filter settings.

7 Responding to a Fault

By default, once a fault is detected, an internal interrupt request (IRQ) is generated. The user can control which faults generate interrupts using the INT_MASKx registers. Setting a mask bit to 1 means the corresponding fault is masked and no longer triggers an interrupt, though the fault is still recorded in the latched registers as long as the LTCH_READ_CFG bit in the INT_CFG register is set to 0. Settings in INT_CFG apply to faults for all channels.

The internal IRQ signal can be an output on any of the GPIO pins and used to alert the host processor to a fault condition. If the GPIO pins on the TAx5xxx-Q1 are used for another function or there is not an available GPI pin on the host processor, then the user can also choose to periodically poll the fault registers.

The settings in the INT_CFG, P0_R66 register dictate how the device handles interrupts. The user can program the polarity of the interrupt for output on a GPIO with the INT_POL bit. The INT_EVENT bits set how often an interrupt asserts for a given event. The PD_ON_FLT_CFG bits control whether faults automatically power down MICBIAS and the affected ADC channels. The user can choose to power down from unmasked faults only, or from any detected fault regardless of mask settings. The PD_ON_FLT_RCV_CFG bit sets whether the device automatically re-powers once the interrupt is no longer asserted, or waits for manual programming from the host. For more information on manual recovery mode, see Section 7.2. Note, that ASI bus clock errors always power down the ADC channels and the device recovers as soon as the error is resolved.

7.1 INT_CFG Register (page = 0x00, address = 0x42) [reset = 0b]

This register is the interrupt configuration register.

Table 7-1. INT_CFG Register Field Descriptions

Bit	Field	Type(1)	Reset	Description
7	INT_POL	R/W	0b	Interrupt polarity 0b = Active low (IRQZ) 1b = Active high (IRQ)
6-5	INT_EVENT[1:0]	R/W	00b	Interrupt event configuration 0d = INT asserts on any unmasked latched interrupts event 1d = INT asserts on any unmasked live interrupts event 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event
4-3	PD_ON_FLT_CFG[1:0]	R/W	00b	Power down configuration during fault for CHx and MCBIAS 0d = Faults are not considered for power down 1d = Only unmasked faults are considered for power down 2d = All faults are considered for power down 3d = Reserved
2	LTCH_READ_CFG	R/W	0b	Interrupt latch registers readback configuration 0b = All interrupts can be read through the LTCH registers 1b = Only unmasked interrupts can be read through the LTCH registers
1	PD_ON_FLT_RCV_CFG	R/W	0b	Configuration for power down ADC channels on fault 0b = Auto recovery, ADC channels are powered-up again when fault goes away 1b = Manual recovery, ADC channels are not powered up again when fault goes away
0	LTCH_CLR_ON_READ	R/W	0b	Configuration for clearing LTCH register bits 0 = LTCH register bits are cleared on register read only if live status is zero 1 = LTCH register bits are cleared on register read irrespective of live status

(1) R/W = Read or Write

In addition to the mask settings, DIAG_CFG10, P1_R80 allows the user to select which MICBIAS faults are used for the power down of MICBIAS and all ADC channels.

7.1.1 DIAG_CFG10 Register (page = 0x01, address = 0x50) [Reset = 0x88]

This register is the MICBIAS diagnostic configuration register 10.

Table 7-2. DIAG_CFG10 Register Field Descriptions

Bit	Field	Type(1)	Reset	Description
7	PD_MBIAS_SHRT_CKT_ FLT	R/W	1b	Power down configuration of MICBIAS during Short Circuit fault 0b = No change when fault occurs 1b = MICBIAS is disabled when fault occurs
6	PD_MBIAS_HIGH_CURR _FLT	R/W	0b	Power down configuration of MICBIAS during High current fault 0b = No change when fault occurs 1b = MICBIAS is disabled when fault occurs
5	PD_MBIAS_LOW_CURR_ FLT	R/W	0b	Power down configuration of MICBIAS during Low current fault 0b = No change when fault occurs 1b = MICBIAS is disabled when fault occurs
4	PD_MBIAS_OV_FLT	R/W	0b	Power down configuration of MICBIAS during high voltage fault 0b = No change when fault occurs 1b = MICBIAS is disabled when fault occurs
3	PD_MBIAS_OT_FLT	R/W	1b	Power down configuration of MICBIAS during over temperature fault 0b = No change when fault occurs 1b = MICBIAS is disabled when fault occurs
2	MAN_RCV_PD_FLT_CHK	R/W	0b	Manual Recovery (self clear bit) 0b = No effect 1b = Re-check fault status and power up channels again if channels do not have any faults.
1	MBIAS_FLT_AUTO_REC_ EN	R/W	0b	MICBIAS power down on faults Auto-Recovery Enable 0d = Auto-recovery from MICBIAS faults disabled 1d = Auto recovery enabled
0	MICBIAS_SHRT_CKT_DE T_DIS	R/W	0b	MICBIAS Short Circuit fault detect configuration 0b = enable 1b = disable

(1) R/W = Read or Write

7.2 Manual Recovery Sequence

In some applications, waiting for the input from the host processor is desired before powering back up after a fault occurs and MICBIAS and ADC channels are shut down. For this purpose, the PD_ON_FLT_RCV_CFG bit in INT_CFG, P0_R66 can be set to 1 to enable manual recovery mode. In this mode, the device waits for a write of 1 to the MAN_RCV_PD_FLT_CHK bit in the DIAG_CFG10, P1_R80 register before initiating the start-up sequence. The proper sequence for initiating a manual recovery is as follows:

1. Remove all the triggers or events in the system which caused the MICBIAS fault.
2. Reset PD_MBIAS_HIGH_CURR_FLT and PD_MBIAS_LOW_CURR_FLT bits in P1_80.
3. Set MAN_RCV_PD_FLT_CHK (P1_R80).
4. Wait for at least 10 ms.
5. Set PD_MBIAS_HIGH_CURR_FLT and PD_MBIAS_LOW_CURR_FLT bits in P0_R58 as required.

Do not skip step 2 in this sequence, otherwise the device can fail to start up properly, even if faults are no longer present.

7.3 Recommended Fault Register Read Sequence

Once a fault has occurred and an interrupt is generated, the diagnostic registers can be used to determine present faults. For most applications, the latched registers is used to identify faults since these register can be transient and are no longer reflected in the live registers. When reading latched registers, reading each of the latched fault registers is recommended to verify that all errors are detected and that the latches are reset accordingly. The exact sequence of register reads occurring depends on the application and mask settings. The following is provided as a default recommended sequence to avoid missing faults.

1. Read INT_LTCH0 register to determine if any clock, PLL, overtemperature, or overcurrent faults have occurred.
2. Read the CHx_LTCH register to determine which input channels, if any, experienced faults.
3. If a channel has experienced a fault, read the INT_LTCH1 register first to determine if an overvoltage fault has occurred.
4. Read the associated IN_CH_LTCH register for the channels identified in step 1 to determine which other faults have occurred.

Since reading the overvoltage register in INT_LTCH1 clears the short to VBAT_IN bits in the IN_CHx_LTCH registers, not detecting a short to VBAT_IN is possible if the short is a transient short. Detecting an overvoltage is preferred since any short to VBAT_IN also triggers an overvoltage fault as long as VBAT_IN > MICBIAS (as is the case in most applications). Furthermore, a short to VBAT_IN is less likely to be transient in nature, and is still readable in the respective latched or live register depending on the LTCH_CLR_ON_READ setting.

8 Using PurePath™ Console

The input fault diagnostic features are easily configured when using the TAx5x1x-Q1 evaluation module (EVM) and PurePath™ Console 3 graphical user interface (GUI). PurePath Console 3 allows the user to configure the diagnostics programming thresholds, debounce, enable or mask a fault, and automatically monitors the status of input and MICBIAS faults while the EVM has integrated circuitry to trigger these input channels directly.

The TAx5x1xQ15B5EVM-K Evaluation Module EVM user's guide has instructions for testing various diagnostic setups.

8.1 Advanced Tab

After downloading the GUI and TAx5x1x-Q1 application from ti.com/mysecuresoftware, navigate to the *Advanced* tab at the top right of the page. Enable the *Diagnostics* advanced mode tab and click *Apply*.

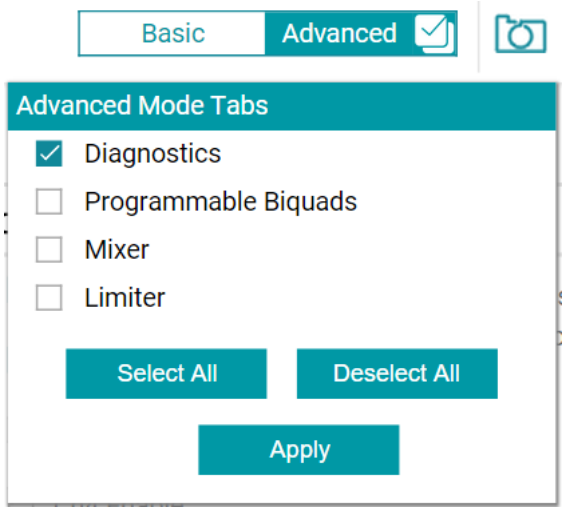


Figure 8-1. Advanced Mode Tab

8.2 Diagnostics Walk-through

8.2.1 Diagnostics Configuration

Figure 8-2 shows a section of the *Advanced Mode Tab* that allows the user to adjust the monitored input faults with a programmable threshold from 0 to 450 mV. The single point sliders are set to the default threshold for each fault at initialization.

1. The *Threshold Range Scale* check box allows the user to scale all of the configuration thresholds by two times.
2. The *INxM pins of Single Ended Configuration* check box excludes the INxM pins from being scanned for diagnostics.
3. The *AC Coupled channel pins* check box configures the device to include the AC coupled channels in the scan for diagnostics. Enabling this box coincides with using one channel for DC diagnostics while the other channel has an AC-coupled MIC input as shown in Figure 2-3.

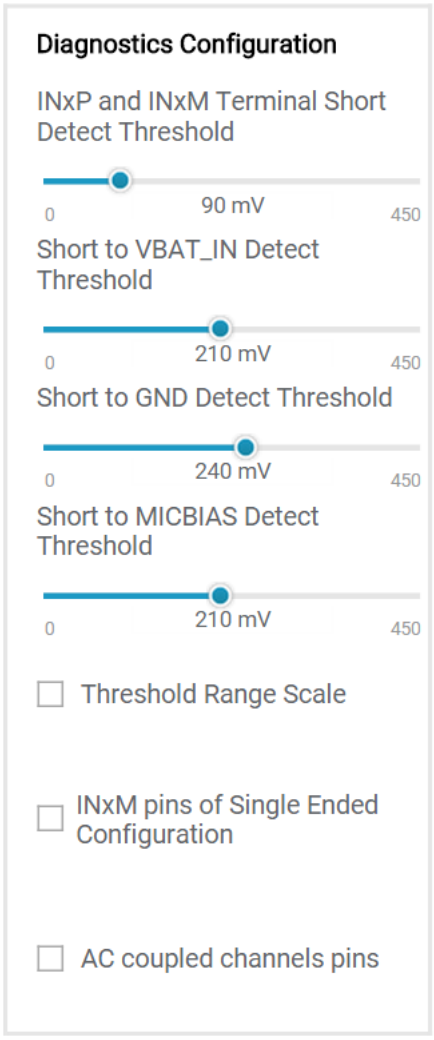


Figure 8-2. Diagnostics Configuration Pane

8.2.2 Debounce Configuration

Figure 8-3 shows a section of the *Advanced Mode Tab* that allows the user to program debounce for 0, 4, 8, or 16 counts to filter out transient events. This setting configures debounce for all faults except the VBAT_IN short, which can be programmed independently to 8 or 16 counts.

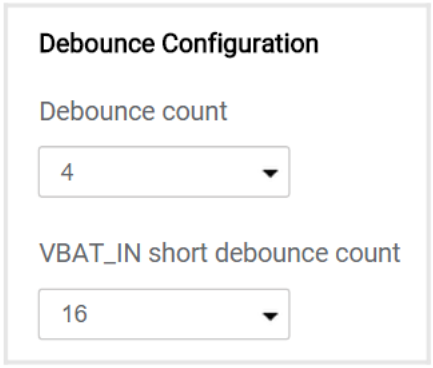


Figure 8-3. Debounce Configuration Pane

8.2.3 Latched Fault Status

The TAx5x1xQ1 GUI features a comprehensive summary of input and microphone faults. The GUI features options that allow the user to choose which fault interrupts or channels to mask diagnostics for and whether to update automatically or manually.

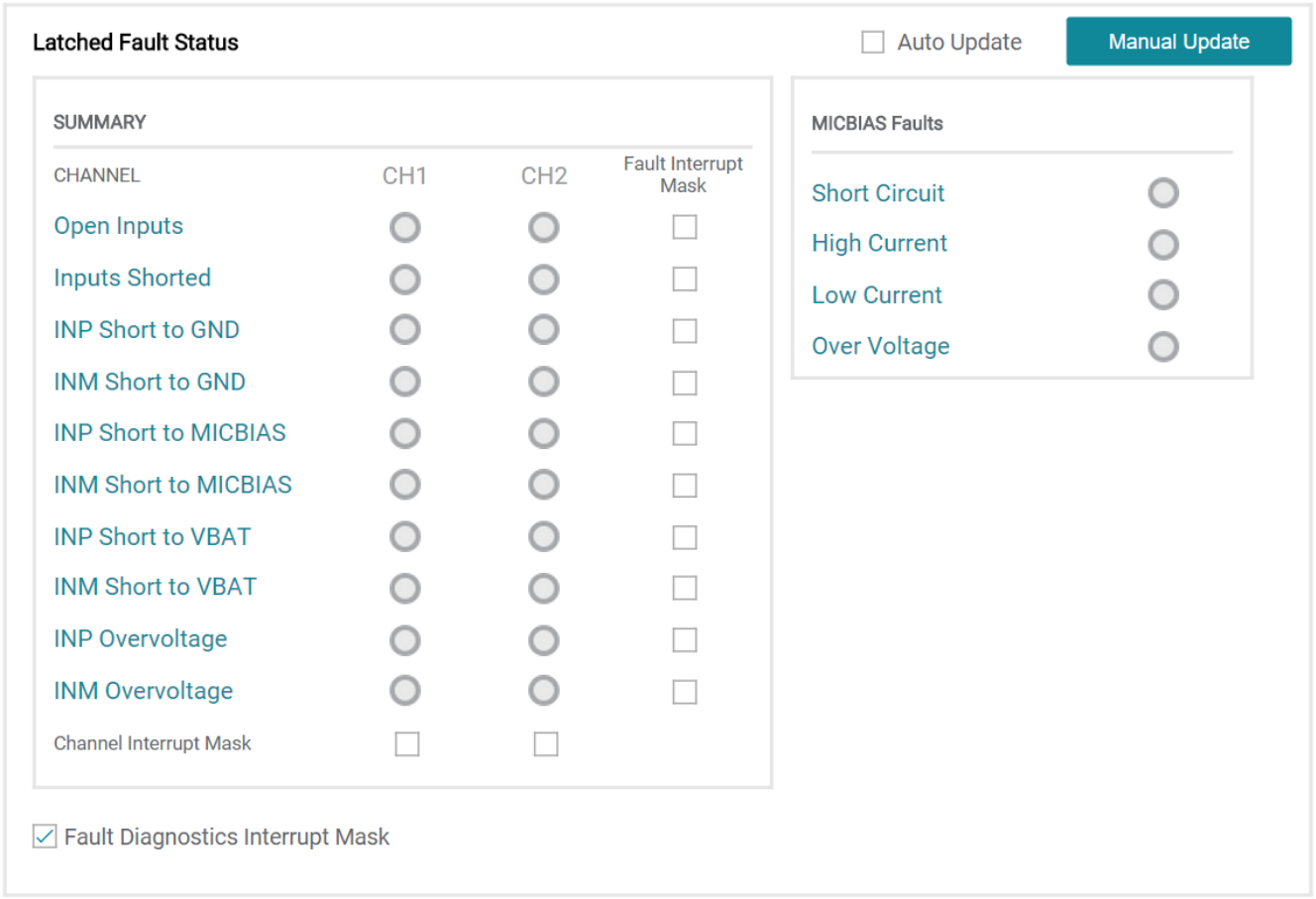


Figure 8-4. Latched Fault Status Pane

9 Diagnostic Monitoring Registers

In addition to the latched and live fault registers, the raw data used for fault calculation is stored in diagnostic monitoring registers (P1_R86 to P1_R113). These registers provide voltage readings for each of the input channels, VBAT_IN, and MICBIAS as well as the MICBIAS load and internal die temperature. The MICBIAS load and die temperature registers have unique transfer functions detailed in the following sections. These registers can be used to bypass the on-chip fault processing and develop unique fault algorithms from the raw data. The registers are also useful during system debug.

9.1 Voltage Measurements

The raw channel voltage data used for fault calculation is stored as a 12-bit SAR ADC code in binary format and can be read from the associated page-1 registers. Data is packed as first MSB byte in one register and then LSB nibble in a second register and is appended with a 4-bit channel-ID. The following equation is used to convert the raw data to input source voltage.

$$VIN(V) = \left(\left(0.9 \times \frac{READ\_DATA}{4095}\right) - 0 \cdot 211764\right) \times 17 \quad (2)$$

The DIAGDATA_CFG register (page 1: 0x55) allows the user to select whether the SAR data registers are updated continuously or held during register read back. By default, data update is held while registers are read. If the moving average feature is used, then data must be updated continuously.

9.2 MICBIAS Load Current

The MICBIAS load data is divided into two page 1 registers. DIAG_MON_MSB_MBIAS (Page 1, address 0x58) contains the MSB data byte of the MICBIAS load current. DIAG_MON_LSB_MBLOAD (Page 1, address 0x57) contains the LSB data nibble of the MICBIAS load current. The supported monitoring range is from 0 mA to 50 mA. The following equation shows how to convert this raw binary data to the MICBIAS load current.

$$MICBIAS\ Load\ Current\ (mA) = \left(\left(0.9 \times \frac{READ\_DATA}{4095}\right) - 0 \cdot 2\right) \times 48.46154 \quad (3)$$

The MICBIAS load current measurement is not trimmed for gain and offset error and is intended only as an auxiliary feature for applications that want a rough estimate of the load conditions. The accuracy is approximately the same as the threshold step size of 0.117 mA. If precision load monitoring is required, using an external sensor is recommended.

9.3 Internal Die Temperature

An internal diode provides a rough measure of the device die temperature. This temperature monitor is not the same as that used by the over-temperature fault detect circuitry. The supported monitoring range is from –40°C to 150°C and the temperature can be calculated using the following equation.

$$Temperature(°C) = 0.1141 \times (3565 - READ\_DATA) - 40 \quad (4)$$

The die temperature measurement is not trimmed for gain and offset error and is intended only as an auxiliary feature for applications that want a rough estimate of the die temperature. The accuracy of the die temperature sensor is not specified and varies depending on board layout. However, a rough characterization of the sensor typically shows accuracy around ±5°C. If precision temperature readings are required, using an external sensor is recommended.

10 Summary

The TAx5xxx-Q1 family of devices have embedded advanced diagnostic capabilities that are designed to enhance the reliability and performance of automotive audio systems. This application note delves into the key aspects of the device, including the various input and output faults, virtual ground fault, and supply back pumping protection methods. Additionally, this document outlines how to configure the registers of the device family, how to properly detect and respond to various faults, and how to interact with the PurePath™ Console graphical user interface (GUI), to serve as a comprehensive guide for engineers and designers.

11 References

- Texas Instruments, *TAA5412-Q1 Automotive, 2-Channel, 768-kHz, Audio ADC With Integrated Microphone Bias and Input Fault Diagnostics*, data sheet
- Texas Instruments, *TAx5x1xQ15B5EVM-K Evaluation Module*, EVM user's guide
- Texas Instruments, *PCM6xx0-Q1 Fault Diagnostic Features*, application note

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