

# TAC5142 Hardware-control stereo audio codec with 103dB dynamic range ADC and 110dB dynamic range DAC

## 1 Features

- Stereo audio ADC Channels
  - Performance:
    - Line/Microphone differential input dynamic range: 103dB
    - Differential input THD+N: –91dB
  - Input voltage:
    - Differential,  $2V_{RMS}$  full-scale inputs
    - Single-ended,  $1V_{RMS}$  full-scale inputs
  - ADC sample rates ( $f_s$ ) = 8kHz to 192kHz
  - Digital HPF with configurable cut-off frequency:
    - 1Hz or 12Hz, at 48kHz sampling rate
  - Low noise microphone bias
- Stereo audio DAC Channels
  - Performance:
    - DAC to differential line-out dynamic range: 110 dB
    - DAC to pseudo-differential headphone-out dynamic range: 107 dB
    - THD+N: –100 dB
  - Output voltage:
    - Differential line-out/receiver,  $2V_{RMS}$  full-scale
    - Pseudo-differential headphone,  $1V_{RMS}$  full-scale
    - Single-ended line-out,  $1V_{RMS}$  full-scale
  - DAC sample rates ( $f_s$ ) = 8kHz to 192kHz
- Common Features
  - Pin or Hardware Control
  - Audio Serial Interface
    - Format: TDM, I<sup>2</sup>S, or Left-justified (LJ)
    - Bus Controller and Target Modes
    - Configurable TDM Slots
    - Word Length: Selectable 24 or 32 Bits
  - Pin-selectable digital decimation/interpolation filter options:
    - Linear-phase or Low-latency
  - Integrated PLL
  - Auto clock & sample rate detection
  - Interrupt output on clock error
  - Single Supply Operation AVDD: 1.8V or 3.3V
  - I/O Supply Operation: 1.8V or 3.3V
  - Temperature grade 1:  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$

## 2 Applications

- [Video Conference System](#)
- [IP Network Camera](#)
- [IP Telephone](#)
- [Smart Speakers](#)
- [Professional audio mixer/control surface](#)

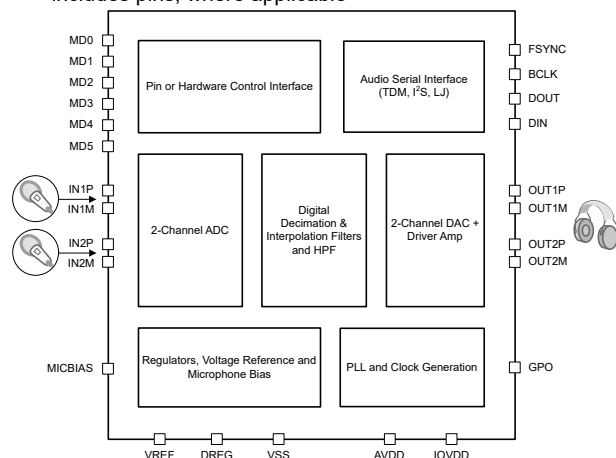
## 3 Description

The TAC5142 is a stereo audio codec with  $2V_{RMS}$  differential input, 103dB dynamic range ADC and  $2V_{RMS}$  differential output, 110dB dynamic range DAC. The TAC5142 supports both differential and single-ended inputs and outputs. The ADC supports both line/microphone input signals with options for AC or DC coupling configurations and the DAC output can be configured for either line-output or headphone loads. The DAC can drive up to 62.5mW into a  $16\Omega$  headphone load. The device integrates a phase-locked loop (PLL) and supports sample rates up to 192kHz for both the ADC and DAC signal chains. The device also integrates a DC-removal digital high-pass filter (HPF) with configurable cut-off for the ADC signal chain. The TAC5142 supports time-division multiplexing (TDM), left-justified (LJ), or I<sup>2</sup>S audio formats in controller and target modes, and is pin or hardware controlled. These integrated high-performance features, pin control along with a single supply operation, make TAC5142 an excellent choice for space-constrained audio applications.

### Device Information

| PART NUMBER | PACKAGE <sup>(1)</sup> | PACKAGE SIZE (NOM) <sup>(2)</sup> |
|-------------|------------------------|-----------------------------------|
| TAC5142     | VQFN (24)              | 4mm x 4mm with 0.5mm pitch        |

- (1) For all available packages, see the orderable addendum at the end of the data sheet.
- (2) The package size (length × width) is a nominal value and includes pins, where applicable



**Simplified Block Diagram**

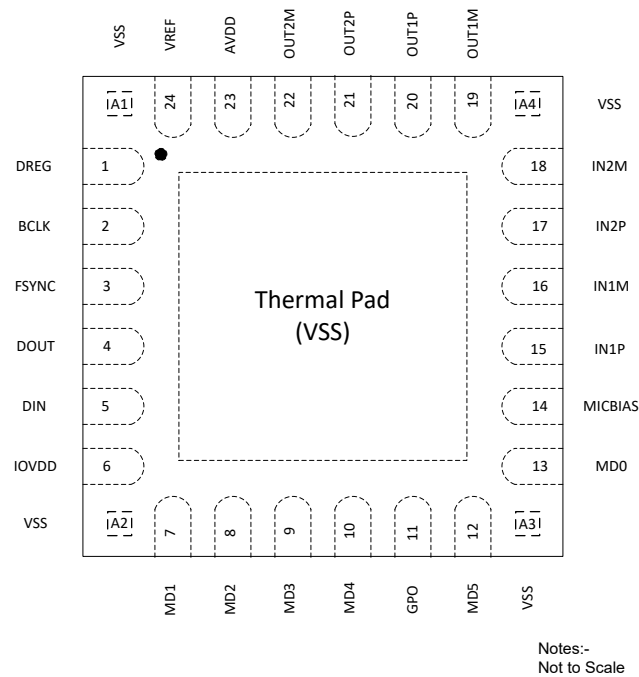
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## 4 Device Comparison Table

| FEATURE                        | TAC5242   | TAC5142 | TAC5212   | TAC5112 | TAC5211   | TAC5111 |
|--------------------------------|---|---------|---|---------|---|---------|
| Control interface              | Pin or Hardware control   |         | I <sup>2</sup> C or SPI   |         |   |         |
| Digital audio serial interface | TDM or I <sup>2</sup> S or left-justified (LJ)  |         |   |         |   |         |
| Audio ADC channel              | 2   |         | 2   |         | 1   |         |
| Digital microphone channel     | Not available (N/A)   |         | 4   |         | 2   |         |
| Microphone bias                | Yes (Fixed Voltage)   |         | Yes (Programmable Voltage)  |         |   |         |
| ADC dynamic range              | 119dB   | 103dB   | 119dB   | 105dB   | 119dB   | 105dB   |
| Audio DAC channel              | 2   |         | 2   |         | 1   |         |
| DAC dynamic range              | 120dB   | 110dB   | 120dB   | 114dB   | 120dB   | 114dB   |
| Compatibility                  | Pin-to-pin, package, and control configuration compatible; drop-in replacements of each other |         | Pin-to-pin, package, and control registers compatible; drop-in replacements of each other |         | Pin-to-pin, package, and control registers compatible; drop-in replacements of each other |         |
| Package                        | VQFN, 24-pins, 4.00mm × 4.00mm with 0.5mm pitch   |         |   |         |   |         |

## 5 Pin Configuration and Functions



**Figure 5-1. 24-Pin QFN Package with Exposed Thermal Pad and Corner Pins, Top View**

**Table 5-1. Pin Functions**

| PIN   |     | TYPE           | DESCRIPTION   |
|-------|-----|----------------|---|
| NAME  | NO. |                |   |
| VSS   | A1  | Ground         | Ground pin. Short directly to board ground plane.   |
| DREG  | 1   | Digital Supply | Digital on-chip regulator output voltage for digital supply (1.55V, nominal)                                  |
| BCLK  | 2   | Digital I/O    | Audio serial data interface bus bit clock   |
| FSYNC | 3   | Digital I/O    | Audio serial data interface bus frame synchronization signal  |
| DOUT  | 4   | Digital Output | Audio serial data interface bus output  |
| DIN   | 5   | Digital Input  | Audio serial data interface bus input   |
| IOVDD | 6   | Digital Supply | Digital I/O power supply (1.8V or 3.3V, nominal)  |
| VSS   | A2  | Ground         | Ground pin. Short directly to board ground plane.   |
| MD1   | 7   | Digital Input  | Controller Mode: Frame rate and BCLK frequency selection  |
|       |     |                | Target Mode: AVDD supply, word length, and decimation/interpolation filter type selection                     |
| MD2   | 8   | Digital Input  | Controller Mode: Frame rate and BCLK frequency selection  |
|       |     |                | Target Mode: AVDD supply, word length, and decimation/interpolation filter type selection                     |
| MD3   | 9   | Digital Input  | Controller Mode: Controller clock input   |
|       |     |                | TDM Target Mode: Data slot selection  |
|       |     |                | I <sup>2</sup> S/LJ Target Mode: Digital HPF cut-off frequency and input cap quick charge setting for the ADC |
| MD4   | 10  | Digital Input  | ADC/DAC input/output configuration selection  |

**Table 5-1. Pin Functions (continued)**

| PIN     |             | TYPE           | DESCRIPTION   |
|---------|-------------|----------------|---|
| NAME    | NO.         |                |   |
| GPO     | 11          | Digital Output | Interrupt output (latched)  |
| MD5     | 12          | Digital Input  | ADC/DAC input/output configuration selection  |
| VSS     | A3          | Ground         | Ground pin. Short directly to board ground plane.   |
| MD0     | 13          | Analog Input   | Multi-level analog input for Controller/Target and I <sup>2</sup> S/TDM/LJ mode selection |
| MICBIAS | 14          | Analog         | Microphone bias output  |
| IN1P    | 15          | Analog Input   | Analog input 1P pin   |
| IN1M    | 16          | Analog Input   | Analog input 1M pin   |
| IN2P    | 17          | Analog Input   | Analog input 2P pin   |
| IN2M    | 18          | Analog Input   | Analo input 2M pin  |
| VSS     | A4          | Ground         | Ground pin. Short directly to board ground plane.   |
| OUT1M   | 19          | Analog Output  | Analog output 1M pin  |
| OUT1P   | 20          | Analog Output  | Analog output 1P pin  |
| OUT2P   | 21          | Analog Output  | Analog output 2P pin  |
| OUT2M   | 22          | Analog Output  | Analog output 2M pin  |
| AVDD    | 23          | Analog Supply  | Analog power supply (1.8V or 3.3V, nominal)   |
| VREF    | 24          | Analog         | Analog reference voltage filter output  |
| VSS     | Thermal pad | Ground         | Thermal pad shorted to internal device ground. Short directly to board ground plane.      |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                            |   | MIN  | MAX         | UNIT |
|----------------------------|---|------|-------------|------|
| Supply voltage             | AVDD to VSS (thermal pad)                       | -0.3 | 3.9         | V    |
| Supply voltage             | IOVDD to VSS (thermal pad)                      | -0.3 | 3.9         | V    |
| Ground voltage differences | VSS to VSS (thermal pad)                        | -0.3 | 0.3         | V    |
| Analog input voltage       | Analog input pins voltage to VSS (thermal pad)  | -0.3 | AVDD + 0.3  | V    |
| Digital input voltage      | Digital input pins voltage to VSS (thermal pad) | -0.3 | IOVDD + 0.3 | V    |
| Temperature                | Functional ambient, T <sub>A</sub>              | -55  | 125         | °C   |
|                            | Operating ambient, T <sub>A</sub>               | -40  | 125         |      |
|                            | Junction, T <sub>J</sub>                        | -40  | 150         |      |
|                            | Storage, T <sub>stg</sub>                       | -65  | 150         |      |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

### 6.2 ESD Ratings

|                    |                         |   | VALUE | UNIT |
|--------------------|-------------------------|---|-------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>     | ±2000 | V    |
| V <sub>(ESD)</sub> | Electrostatic discharge | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

|                     |  | MIN  | NOM | MAX   | UNIT |
|---------------------|--|------|-----|-------|------|
| <b>POWER</b>        |  |      |     |       |      |
| AVDD <sup>(1)</sup> | Analog supply voltage to VSS (thermal pad) - AVDD 3.3V operation | 3.0  | 3.3 | 3.6   | V    |
|                     | Analog supply voltage to VSS (thermal pad) - AVDD 1.8V operation | 1.65 | 1.8 | 1.95  |      |
| IOVDD               | IO supply voltage to VSS (thermal pad) - IOVDD 3.3V operation    | 3.0  | 3.3 | 3.6   | V    |
|                     | IO supply voltage to VSS (thermal pad) - IOVDD 1.8V operation    | 1.65 | 1.8 | 1.95  |      |
| <b>INPUTS</b>       |  |      |     |       |      |
| INxx                | Analog input pins voltage to VSS (thermal pad)                   | 0    |     | AVDD  | V    |
| IO                  | Digital input pins (MD1 to MD5) voltage to VSS (thermal pad)     | 0    |     | IOVDD | V    |
| MD0                 | MD0 pin w.r.t VSS (thermal pad)                                  | 0    |     | AVDD  | V    |
| <b>TEMPERATURE</b>  |  |      |     |       |      |
| T <sub>A</sub>      | Operating ambient temperature                                    | -40  |     | 125   | °C   |

|                |   | MIN | NOM | MAX                   | UNIT |
|----------------|---|-----|-----|-----------------------|------|
| <b>OTHERS</b>  |   |     |     |                       |      |
| CCLK           | MD3 controller mode clock frequency (CCLK) - IOVDD 3.3V operation |     |     | 36.864 <sup>(2)</sup> | MHz  |
|                | MD3 controller mode clock frequency (CCLK) - IOVDD 1.8V operation |     |     | 24.576 <sup>(2)</sup> |      |
| C <sub>L</sub> | Digital output load capacitance                                   |     | 20  | 50                    | pF   |

- (1) VSS and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2V.  
(2) CCLK input rise time (V<sub>IL</sub> to V<sub>IH</sub>) and fall time (V<sub>IH</sub> to V<sub>IL</sub>) must be less than 5ns. For better audio noise performance, CCLK input must be used with low jitter.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | TAC5142    | UNIT |
|-------------------------------|--|------------|------|
|                               |  | RGE (VQFN) |      |
|                               |  | 24 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 38.4       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 26.3       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 15.9       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.5        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 15.8       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 13.8       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

## 6.5 Electrical Characteristics

At T<sub>A</sub> = 25°C, AVDD = 3.3V, IOVDD = 3.3V, f<sub>IN</sub> = 1kHz sinusoidal signal, f<sub>S</sub> = 48kHz, 32-bit audio data, BCLK = 256×f<sub>S</sub>, TDM target mode, and linear-phase decimation/interpolation filters, with 1200Ω/600Ω line-out load in differential/single-ended configuration or 32Ω receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

| PARAMETER                                  | TEST CONDITIONS                                      | MIN   | NOM | MAX | UNIT             |
|--|--|---|-----|-----|------------------|
| <b>ADC PERFORMANCE FOR INPUT RECORDING</b> |  |   |     |     |                  |
|  | Differential input full-scale AC signal voltage      | AC-coupled input  | 2   |     | V <sub>RMS</sub> |
|  | Single-ended input full-scale AC signal voltage      | AC-coupled input  | 1   |     | V <sub>RMS</sub> |
| SNR  | Signal-to-noise ratio, A-weighted <sup>(1) (2)</sup> | INxx differential AC-coupled input and AC signal shorted to ground  | 104 |     | dB               |
|  |  | INxx differential DC-coupled input and AC signal shorted to ground, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)              | 101 |     |                  |
| SNR  | Signal-to-noise ratio, A-weighted <sup>(1) (2)</sup> | INxx differential AC-coupled input and AC signal shorted to ground, AVDD = 1.8V   | 99  |     | dB               |
|  |  | INxx differential DC-coupled input and AC signal shorted to ground, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01), AVDD = 1.8V | 95  |     |                  |
| SNR  | Signal-to-noise ratio, A-weighted <sup>(1) (2)</sup> | INxx single-ended AC-coupled input and AC signal shorted to ground  | 97  |     | dB               |
|  |  | INxx single-ended AC-coupled input and AC signal shorted to ground, AVDD = 1.8V   | 92  |     |                  |
| DR   | Dynamic range, A-weighted <sup>(2)</sup>             | INxx differential AC-coupled input and -60dBFS AC signal input  | 103 |     | dB               |
|  |  | INxx differential DC-coupled input and -60dBFS dB AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)               | 101 |     |                  |

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At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{V}$ ,  $IOVDD = 3.3\text{V}$ ,  $f_{IN} = 1\text{kHz}$  sinusoidal signal,  $f_S = 48\text{kHz}$ , 32-bit audio data,  $BCLK = 256 \times f_S$ , TDM target mode, and linear-phase decimation/interpolation filters, with  $1200\Omega/600\Omega$  line-out load in differential/single-ended configuration or  $32\Omega$  receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

| PARAMETER                   |   | TEST CONDITIONS   | MIN | NOM        | MAX | UNIT                       |
|-----------------------------|---|---|-----|------------|-----|----------------------------|
| DR                          | Dynamic range, A-weighted <sup>(2)</sup>  | INxx differential AC-coupled input and –60dBFS AC signal input, $AVDD = 1.8\text{V}$  |     | 98         |     | dB                         |
|                             |   | INxx differential DC-coupled input and –60dBFS dB AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01), $AVDD = 1.8\text{V}$ |     | 95         |     |                            |
| DR                          | Dynamic range, A-weighted <sup>(2)</sup>  | INxx single-ended AC-coupled input and –60dBFS AC signal input  |     | 97         |     | dB                         |
|                             |   | INxx single-ended AC-coupled input and –60dBFS AC signal input, $AVDD = 1.8\text{V}$  |     | 91         |     |                            |
| THD+N                       | Total harmonic distortion <sup>(2)</sup>  | INxx differential AC-coupled input and –1dBFS AC signal input   |     | –91        |     | dB                         |
|                             |   | INxx differential DC-coupled input and –1dBFS AC signal input, in High Common Mode Tolerance Mode (MD5-MD4 = 2'b01)                           |     | –90        |     |                            |
| <b>ADC OTHER PARAMETERS</b> |   |   |     |            |     |                            |
|                             | AC Input impedance                        | Input pins INxP or INxM   |     | 42         |     | k $\Omega$                 |
|                             | Output data word length                   | Pin Selectable, based on MD1/MD2 Configuration  | 24  |            | 32  | Bits                       |
|                             | Digital high-pass filter cutoff frequency | First-order IIR filter, –3dB point (Pin Selectable)   | 1   |            | 12  | Hz                         |
|                             | Interchannel isolation                    | –1dBFS AC signal line-in differential input to non-measurement channel  |     | –134       |     | dB                         |
|                             | Interchannel gain mismatch                | –6dBFS AC signal line-in differential input, 1kHz sinusoidal signal   |     | $\pm 0.1$  |     | dB                         |
|                             | Interchannel phase mismatch               | –6dBFS AC signal line-in differential input, 1kHz sinusoidal signal   |     | $\pm 0.01$ |     | Degrees                    |
| PSRR                        | Power-supply rejection ratio              | 100mV <sub>PP</sub> , 1kHz sinusoidal signal on $AVDD$ , differential input   |     | 120        |     | dB                         |
| <b>MICROPHONE BIAS</b>      |   |   |     |            |     |                            |
|                             | MICBIAS noise                             | Bandwidth = 20Hz to 20kHz, A-weighted, 1 $\mu\text{F}$ capacitor between MICBIAS and VSS (thermal pad)  |     | 2          |     | $\mu\text{V}_{\text{RMS}}$ |
|                             | MICBIAS voltage                           | $AVDD = 1.8\text{V}$  |     | 1.375      |     | V                          |
|                             |   | $AVDD = 3.3\text{V}$  |     | 2.75       |     |                            |



At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{V}$ ,  $IOVDD = 3.3\text{V}$ ,  $f_{IN} = 1\text{kHz}$  sinusoidal signal,  $f_S = 48\text{kHz}$ , 32-bit audio data,  $BCLK = 256 \times f_S$ , TDM target mode, and linear-phase decimation/interpolation filters, with  $1200\Omega/600\Omega$  line-out load in differential/single-ended configuration or  $32\Omega$  receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

| PARAMETER  |  | TEST CONDITIONS   | MIN | NOM       | MAX | UNIT      |
|--|--|---|-----|-----------|-----|-----------|
| <b>DAC Performance for Line Output/Head Phone Playback</b> |  |   |     |           |     |           |
|  | Full Scale Output Voltage                            | Differential output between OUTxP and OUTxM, AVDD = 3.3V  |     | 2         |     | $V_{RMS}$ |
|  |  | Differential output between OUTxP and OUTxM, AVDD = 1.8V  |     | 1         |     |           |
|  |  | Single-ended output, AVDD = 3.3V  |     | 1         |     |           |
|  |  | Single-ended output, AVDD = 1.8V  |     | 0.5       |     |           |
|  |  | Pseudo-differential output between OUTxP and OUT1M with external common-mode sense, AVDD = 3.3V |     | 1         |     |           |
|  |  | Pseudo-differential output between OUTxP and OUT1M with external common-mode sense, AVDD = 1.8V |     | 0.5       |     |           |
| SNR  | Signal-to-noise ratio, A-weighted <sup>(1) (2)</sup> | Differential output, 0dBFS signal, AVDD = 3.3V  |     | 110       |     | dB        |
|  |  | Single-ended output, 0dBFS signal, AVDD = 3.3V  |     | 107       |     |           |
|  |  | Pseudo-differential output, 0dBFS signal, AVDD = 3.3V   |     | 107       |     |           |
|  |  | Differential output, 0dBFS signal, AVDD = 1.8V  |     | 109       |     |           |
|  |  | Single-ended output, 0dBFS signal, AVDD = 1.8V  |     | 104       |     |           |
|  |  | Pseudo-differential output, 0dBFS signal, AVDD = 1.8V   |     | 103       |     |           |
| DR   | Dynamic range, A-weighted <sup>(2)</sup>             | Differential output, -60dBFS signal, AVDD = 3.3V  |     | 110       |     | dB        |
|  |  | Single-ended output, -60dBFS signal, AVDD = 3.3V  |     | 107       |     |           |
|  |  | Pseudo-differential output, -60dBFS signal, AVDD = 3.3V   |     | 107       |     |           |
|  |  | Differential output, -60dBFS signal, AVDD = 1.8V  |     | 109       |     |           |
|  |  | Single-ended output, -60dBFS signal, AVDD = 1.8V  |     | 104       |     |           |
|  |  | Pseudo-differential output, -60dBFS signal, AVDD = 1.8V   |     | 103       |     |           |
| THD+N  | Total harmonic distortion <sup>(2)</sup>             | Differential output, -1dBFS Signal, AVDD = 3.3V   |     | -100      |     | dB        |
|  |  | Single-ended output, -1dBFS Signal, AVDD = 3.3V   |     | -96       |     |           |
|  | Headphone Load Range                                 |   | 8   | 16        | 300 | $\Omega$  |
|  | Headphone/Line-out Cap Load                          |   | 0   | 100       | 550 | pF        |
|  | Line-out Load Range                                  |   | 600 |           |     | $\Omega$  |
| <b>DAC Channel OTHER PARAMETERS</b>                        |  |   |     |           |     |           |
|  | Output Offset  | 0 Input, Differential Line-output   |     | $\pm 0.5$ |     | mV        |
|  | Output Common Mode                                   | Common Mode Level for OUTxP and OUTxM, AVDD = 1.8V  |     | 0.9       |     | V         |
|  |  | Common Mode Level for OUTxP and OUTxM, AVDD = 3.3V  |     | 1.65      |     |           |
|  | Common Mode Error                                    | DC Error in Common Mode Voltage   |     | $\pm 10$  |     | mV        |
|  | Output Signal Bandwidth                              |   |     | 20        |     | kHz       |
|  | Input data word length                               | Pin Selectable, based on MD1/MD2 Configuration  | 24  |           | 32  | Bits      |

**TAC5142**

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At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{V}$ ,  $IOVDD = 3.3\text{V}$ ,  $f_{IN} = 1\text{kHz}$  sinusoidal signal,  $f_S = 48\text{kHz}$ , 32-bit audio data,  $BCLK = 256 \times f_S$ , TDM target mode, and linear-phase decimation/interpolation filters, with  $1200\Omega/600\Omega$  line-out load in differential/single-ended configuration or  $32\Omega$  receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

| PARAMETER                                 |  | TEST CONDITIONS  | MIN                        | NOM        | MAX                        | UNIT          |
|---|--|--|----------------------------|------------|----------------------------|---------------|
|   | Interchannel isolation   | Differential output, $-1\text{dBFS}$ input signal on non-measurement channel                 |                            | $-120$     |                            | dB            |
|   | Gain Error   | Differential output, $-6\text{dBFS}$ Input signal  |                            | $\pm 0.1$  |                            |               |
|   | Interchannel gain mismatch   | Differential output, $-6\text{dBFS}$ Input signal  |                            | $\pm 0.1$  |                            | dB            |
|   | Interchannel phase mismatch  | Differential output, $-6\text{dBFS}$ Input signal  |                            | $\pm 0.01$ |                            | Degrees       |
| PSRR                                      | Power-supply rejection ratio   | $100\text{mV}_{PP}$ , 1kHz sinusoidal signal on AVDD, differential input, 0dB channel gain   |                            | 110        |                            | dB            |
| $P_{out}$                                 | Output Power Delivery  | Receiver/Headphone $R_L = 16\Omega$ , THD+N < 1% in Differential or Pseudo-differential mode |                            | 62.5       |                            | mW            |
| <b>DIGITAL I/O</b>                        |  |  |                            |            |                            |               |
| $V_{IL}$                                  | Low-level digital input logic voltage threshold  | All digital pins, IOVDD 1.8V operation   | $-0.3$                     |            | $0.35 \times \text{IOVDD}$ | V             |
|   |  | All digital pins, IOVDD 3.3V operation   | $-0.3$                     |            | 0.8                        |               |
| $V_{IH}$                                  | High-level digital input logic voltage threshold   | All digital pins, IOVDD 1.8V operation   | $0.65 \times \text{IOVDD}$ |            | $\text{IOVDD} + 0.3$       | V             |
|   |  | All digital pins, IOVDD 3.3V operation   | 2                          |            | $\text{IOVDD} + 0.3$       |               |
| $V_{OL}$                                  | Low-level digital output voltage   | All digital pins, $I_{OL} = -2\text{mA}$ , IOVDD 1.8V operation                              |                            |            | 0.45                       | V             |
|   |  | All digital pins, $I_{OL} = -2\text{mA}$ , IOVDD 3.3V operation                              |                            |            | 0.4                        |               |
| $V_{OH}$                                  | High-level digital output voltage  | All digital pins, $I_{OH} = 2\text{mA}$ , IOVDD 1.8V operation                               | $\text{IOVDD} - 0.45$      |            |                            | V             |
|   |  | All digital pins, $I_{OH} = 2\text{mA}$ , IOVDD 3.3V operation                               | 2.4                        |            |                            |               |
| $I_{IL}$                                  | Input logic-low leakage for digital inputs   | All digital pins, input = 0V   | $-5$                       | 0.1        | 5                          | $\mu\text{A}$ |
| $I_{IH}$                                  | Input logic-high leakage for digital inputs  | All digital pins, input = IOVDD  | $-5$                       | 0.1        | 5                          | $\mu\text{A}$ |
| $C_{IN}$                                  | Input capacitance for digital inputs   | All digital pins   |                            | 5          |                            | pF            |
| $R_{PD}$                                  | Pulldown resistance for digital I/O pins when asserted on  |  |                            | 20         |                            | k $\Omega$    |
| <b>TYPICAL SUPPLY CURRENT CONSUMPTION</b> |  |  |                            |            |                            |               |
| $I_{AVDD}$                                | Current consumption in sleep mode or low power mode  | All external clocks stopped, AVDD = 3.3V   |                            | 1.35       |                            | mA            |
| $I_{IOVDD}$                               |  | All external clocks stopped, IOVDD = 3.3V  |                            | 0.6        |                            | $\mu\text{A}$ |
| $I_{IOVDD}$                               |  | All external clocks stopped, IOVDD = 1.8V  |                            | 0.2        |                            |               |
| $I_{AVDD}$                                | Current consumption with ADC 2-channel and DAC to Line-out 2-channel, operating at $f_S$ 16kHz, I <sup>2</sup> S Target Mode, BCLK = $64 \times f_S$ | AVDD = 3.3V  |                            | 22.7       |                            | mA            |
| $I_{IOVDD}$                               |  | IOVDD = 3.3V   |                            | 0.05       |                            |               |
| $I_{IOVDD}$                               |  | IOVDD = 1.8V   |                            | 0.02       |                            |               |

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{V}$ ,  $IOVDD = 3.3\text{V}$ ,  $f_{IN} = 1\text{kHz}$  sinusoidal signal,  $f_S = 48\text{kHz}$ , 32-bit audio data,  $BCLK = 256 \times f_S$ , TDM target mode, and linear-phase decimation/interpolation filters, with  $1200\Omega/600\Omega$  line-out load in differential/single-ended configuration or  $32\Omega$  receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted

| PARAMETER   |   | TEST CONDITIONS       | MIN | NOM  | MAX | UNIT |
|-------------|---|-----------------------|-----|------|-----|------|
| $I_{AVDD}$  | Current consumption with ADC 2-channel and DAC to Line-out 2-channel, operating at $f_S 48\text{kHz}$ , I <sup>2</sup> S Target Mode, $BCLK = 64 \times f_S$  | $AVDD = 3.3\text{V}$  |     | 26.6 |     | mA   |
| $I_{IOVDD}$ |   | $IOVDD = 3.3\text{V}$ |     | 0.1  |     |      |
| $I_{IOVDD}$ |   | $IOVDD = 1.8\text{V}$ |     | 0.05 |     |      |
| $I_{AVDD}$  | Current consumption with ADC 2-channel and DAC to Headphone 2-channel, operating at $f_S 16\text{kHz}$ , I <sup>2</sup> S Target Mode, $BCLK = 64 \times f_S$ | $AVDD = 3.3\text{V}$  |     | 21.5 |     | mA   |
| $I_{IOVDD}$ |   | $IOVDD = 3.3\text{V}$ |     | 0.06 |     |      |
| $I_{IOVDD}$ |   | $IOVDD = 1.8\text{V}$ |     | 0.03 |     |      |
| $I_{AVDD}$  | Current consumption with ADC 2-channel and DAC to Headphone 2-channel, operating at $f_S 48\text{kHz}$ , I <sup>2</sup> S Target Mode, $BCLK = 64 \times f_S$ | $AVDD = 3.3\text{V}$  |     | 25.5 |     | mA   |
| $I_{IOVDD}$ |   | $IOVDD = 3.3\text{V}$ |     | 0.06 |     |      |
| $I_{IOVDD}$ |   | $IOVDD = 1.8\text{V}$ |     | 0.03 |     |      |

- (1) Ratio of output level with 1kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground or no generator input signal, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
- (2) All performance measurements done with a 20kHz low-pass filter and, where noted, an A-weighted filter. Failure to use such a filter can result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

## 6.6 Timing Requirements: TDM, I<sup>2</sup>S or LJ Interface

at  $T_A = 25^\circ\text{C}$ ,  $IOVDD = 3.3\text{V}$  or  $1.8\text{V}$  and 20pF load on all outputs (unless otherwise noted); see Figure 6-1 for timing diagram

|                  |   |  | MIN | NOM | MAX | UNIT |
|------------------|---|--|-----|-----|-----|------|
| $t_{(BCLK)}$     | BCLK period                             | $IOVDD = 1.8\text{V}$                      | 80  |     |     | ns   |
|                  |   | $IOVDD = 3.3\text{V}$                      | 40  |     |     |      |
| $t_{H(BCLK)}$    | BCLK high pulse duration <sup>(1)</sup> | $IOVDD = 1.8\text{V}$                      | 36  |     |     | ns   |
|                  |   | $IOVDD = 3.3\text{V}$                      | 18  |     |     |      |
| $t_{L(BCLK)}$    | BCLK low pulse duration <sup>(1)</sup>  | $IOVDD = 1.8\text{V}$                      | 36  |     |     | ns   |
|                  |   | $IOVDD = 3.3\text{V}$                      | 18  |     |     |      |
| $t_{SU(FSYNC)}$  | FSYNC setup time                        | $IOVDD = 1.8\text{V}$                      | 8   |     |     | ns   |
|                  |   | $IOVDD = 3.3\text{V}$                      | 8   |     |     |      |
| $t_{HLD(FSYNC)}$ | FSYNC hold time                         | $IOVDD = 1.8\text{V}$                      | 8   |     |     | ns   |
|                  |   | $IOVDD = 3.3\text{V}$                      | 8   |     |     |      |
| $t_{SU(DIN)}$    | DIN setup time                          | $IOVDD = 1.8\text{V}$                      | 8   |     |     | ns   |
|                  |   | $IOVDD = 3.3\text{V}$                      | 8   |     |     |      |
| $t_{HLD(DIN)}$   | DIN hold time                           | $IOVDD = 1.8\text{V}$                      | 16  |     |     | ns   |
|                  |   | $IOVDD = 3.3\text{V}$                      | 8   |     |     |      |
| $t_{r(BCLK)}$    | BCLK rise time                          | 10% - 90% rise time, $IOVDD = 1.8\text{V}$ |     |     | 10  | ns   |
|                  |   | 10% - 90% rise time, $IOVDD = 3.3\text{V}$ |     |     | 10  |      |
| $t_{f(BCLK)}$    | BCLK fall time                          | 90% - 10% fall time, $IOVDD = 1.8\text{V}$ |     |     | 10  | ns   |
|                  |   | 90% - 10% fall time, $IOVDD = 3.3\text{V}$ |     |     | 10  |      |

- (1) To meet the timing specifications, the BCLK minimum high or low pulse duration must be higher than 25ns, if the DOUT data line is latched on the opposite BCLK edge polarity from the one used by the device to transmit the DOUT data at  $IOVDD = 3.3\text{V}$ .

## 6.7 Switching Characteristics: TDM, I<sup>2</sup>S or LJ Interface

at  $T_A = 25^\circ\text{C}$ , IOVDD = 3.3V or 1.8V and 20pF load on all outputs (unless otherwise noted); see Figure 6-1 for timing diagram

| PARAMETER                  | TEST CONDITIONS   | MIN                                       | TYP | MAX    | UNIT |
|----------------------------|---|---|-----|--------|------|
| $t_{d(\text{DOUT-BCLK})}$  | BCLK to DOUT delay  | 50% of BCLK to 50% of DOUT, IOVDD = 1.8V  |     | 26     | ns   |
|                            |   | 50% of BCLK to 50% of DOUT, IOVDD = 3.3V  |     | 19     |      |
| $t_{d(\text{DOUT-FSYNC})}$ | FSYNC to DOUT delay in TDM or LJ mode                       | 50% of FSYNC to 50% of DOUT, IOVDD = 1.8V |     | 26     | ns   |
|                            |   | 50% of FSYNC to 50% of DOUT, IOVDD = 3.3V |     | 19     |      |
| $f_{(\text{BCLK})}$        | BCLK output clock frequency; controller mode <sup>(1)</sup> | IOVDD = 1.8V                              |     | 12.288 | MHz  |
|                            |   | IOVDD = 3.3V                              |     | 24.576 |      |
| $t_{d(\text{FSYNC})}$      | BCLK to FSYNC delay; controller mode                        | 50% of BCLK to 50% of FSYNC, IOVDD = 1.8V |     | 26     | ns   |
|                            |   | 50% of BCLK to 50% of FSYNC, IOVDD = 3.3V |     | 19     |      |
| $t_{H(\text{BCLK})}$       | BCLK high pulse duration; controller mode                   | IOVDD = 1.8V                              | 36  |        | ns   |
|                            |   | IOVDD = 3.3V                              | 18  |        |      |
| $t_{L(\text{BCLK})}$       | BCLK low pulse duration; controller mode                    | IOVDD = 1.8V                              | 36  |        | ns   |
|                            |   | IOVDD = 3.3V                              | 18  |        |      |
| $t_{r(\text{BCLK})}$       | BCLK rise time; controller mode                             | 10% - 90% rise time, IOVDD = 1.8V         |     | 10     | ns   |
|                            |   | 10% - 90% rise time, IOVDD = 3.3V         |     | 10     |      |
| $t_{f(\text{BCLK})}$       | BCLK fall time; controller mode                             | 90% - 10% fall time, IOVDD = 1.8V         |     | 10     | ns   |
|                            |   | 90% - 10% fall time, IOVDD = 3.3V         |     | 10     |      |

(1) To meet the timing specifications, the BCLK output clock frequency must be lower than 18.5MHz, if the DOUT data line is latched on the opposite BCLK edge polarity from the one used by the device to transmit DOUT data at IOVDD = 3.3V.

## 6.8 Timing Diagrams

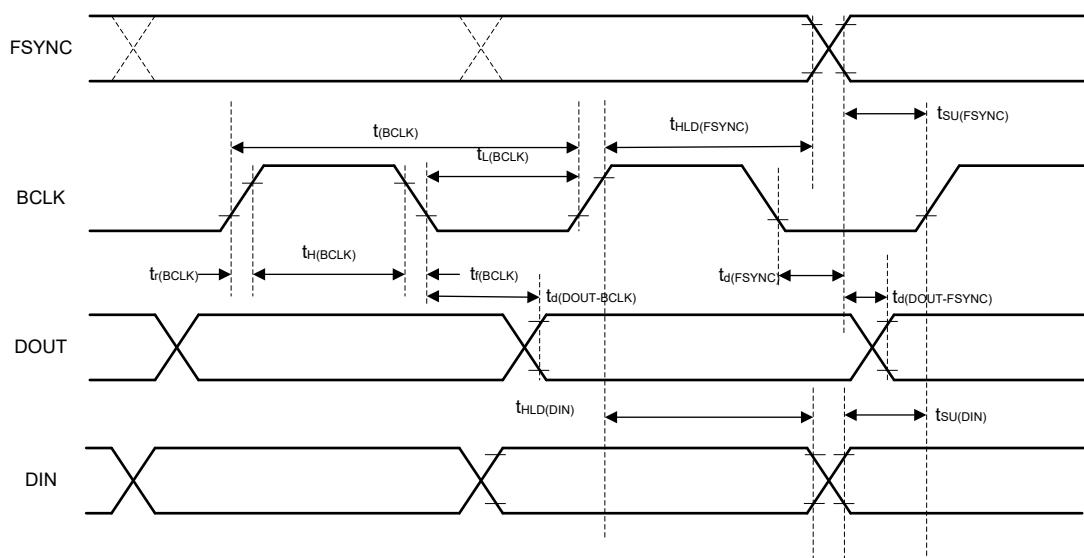
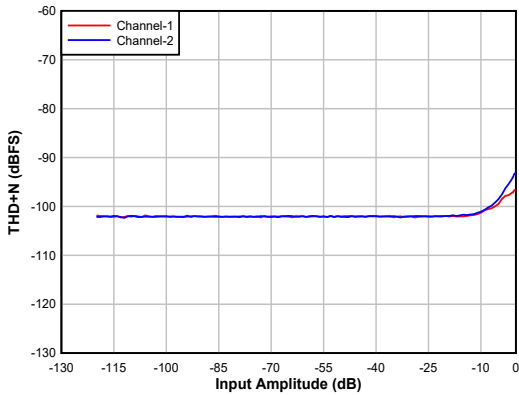


Figure 6-1. TDM, I<sup>2</sup>S, and LJ Interface Timing Diagram

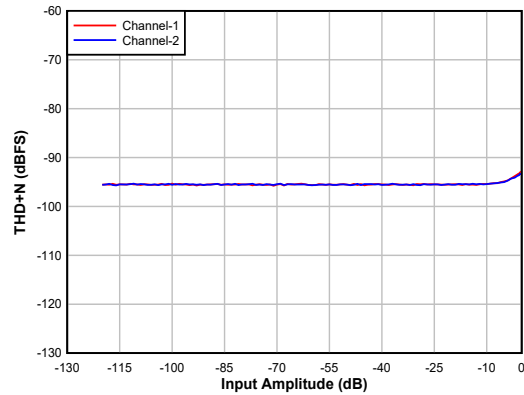
### 6.9 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $AVDD = 3.3\text{V}$ ,  $IOVDD = 3.3\text{V}$ ,  $f_{IN} = 1\text{kHz}$  sinusoidal signal,  $f_S = 48\text{kHz}$ , 32-bit audio data,  $BCLK = 256 \times f_S$ , TDM target mode, and linear phase decimation/interpolation filter, with AC-coupled line-input in differential configuration and  $1200\Omega/600\Omega$  line-out load in differential/single-ended configuration or  $32\Omega$  receiver differential load as applicable; measured filter free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted



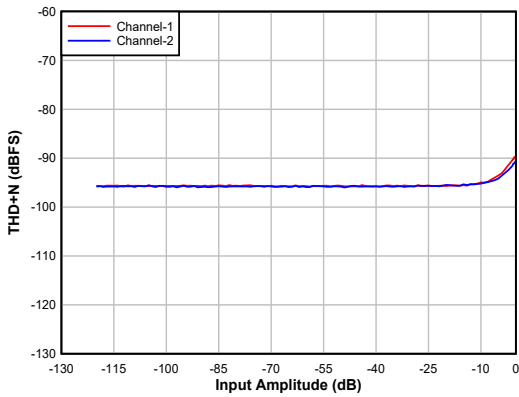
AC-coupled differential line input

**Figure 6-2. ADC THD+N Level vs Input**



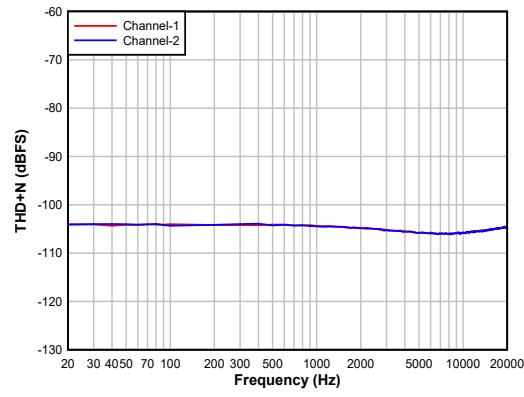
AC-coupled single-ended line input

**Figure 6-3. ADC THD+N Level vs Input**



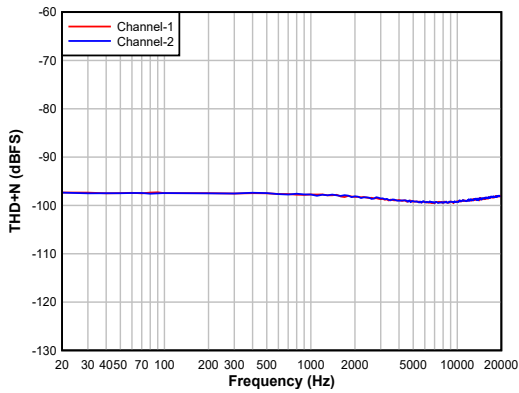
AC-coupled differential line input, AVDD=1.8V

**Figure 6-4. ADC THD+N Level vs Input**



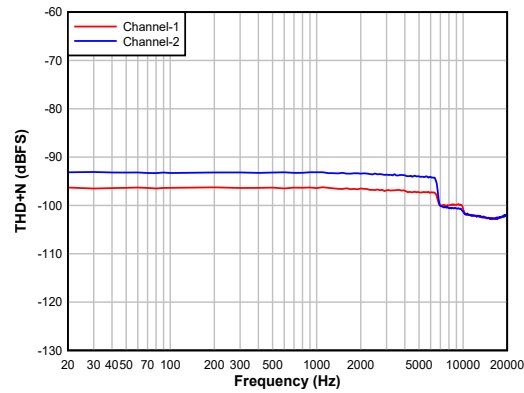
AC-coupled differential line input (-60dBFS)

**Figure 6-5. ADC A-weighted DR vs Frequency**



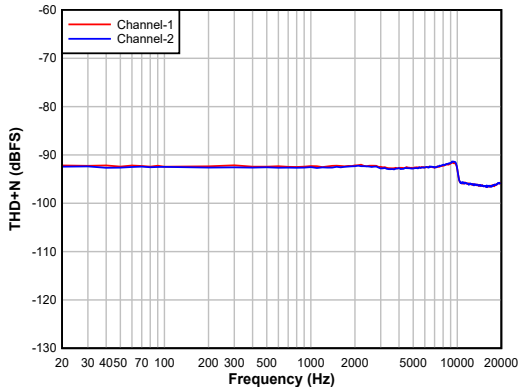
AC-coupled single-ended line input (-60dBFS)

**Figure 6-6. ADC A-weighted DR vs Frequency**



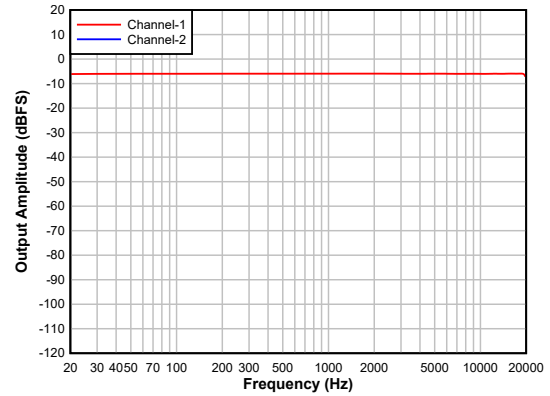
AC-coupled differential line input (-1dBFS)

**Figure 6-7. ADC THD+N vs Frequency**



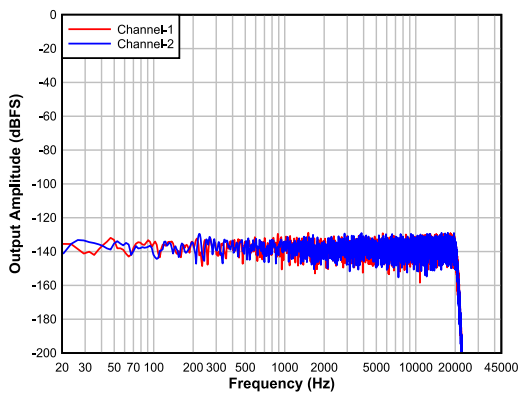
AC-coupled single-ended line input (-1dBFS)

**Figure 6-8. ADC THD+N vs Frequency**



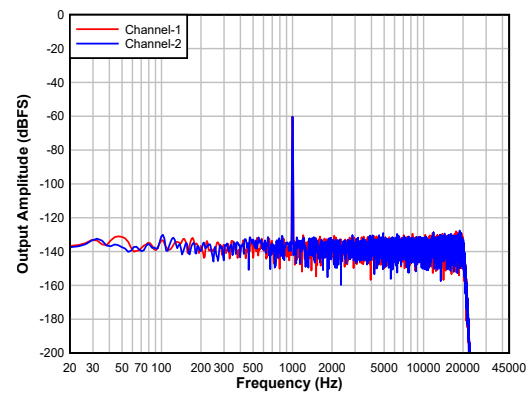
AC-coupled differential line input (-6dBFS)

**Figure 6-9. ADC Frequency Response**



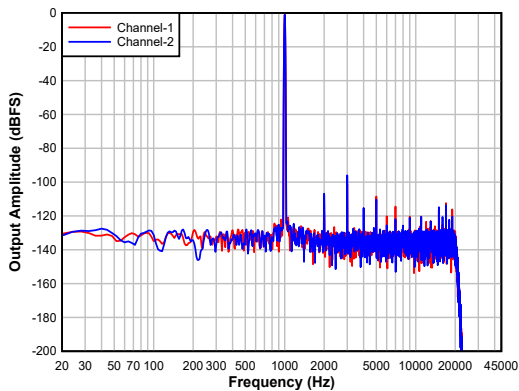
AC-coupled differential line input

**Figure 6-10. ADC FFT with Idle Channel Input**



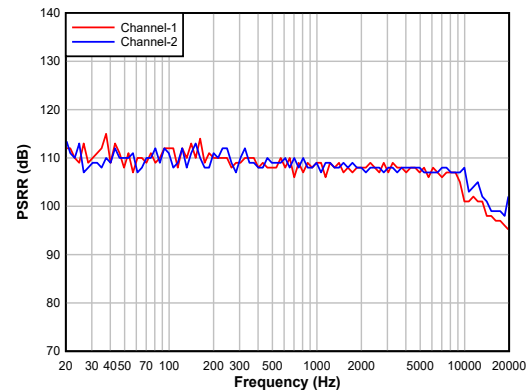
AC-coupled differential line input

**Figure 6-11. ADC FFT with -60dBFS Input**



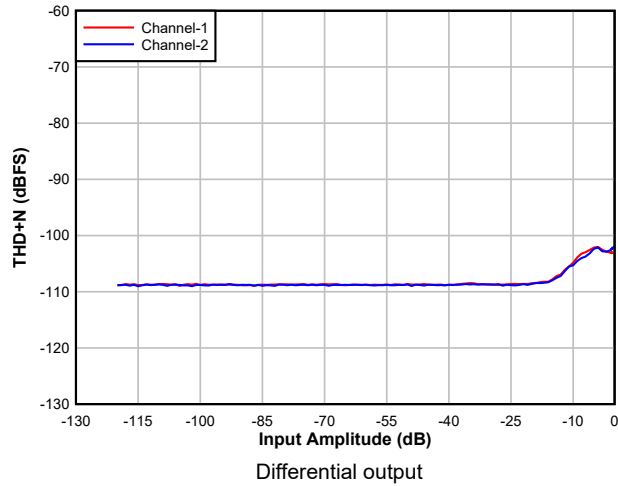
AC-coupled differential line input

**Figure 6-12. ADC FFT with -1dBFS Input**

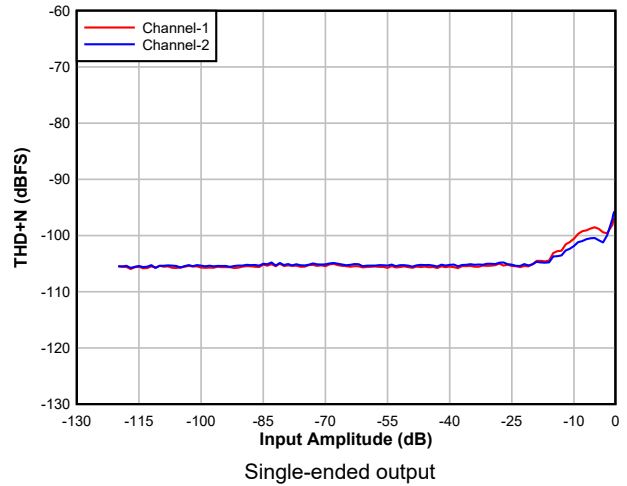


AC-coupled differential line input

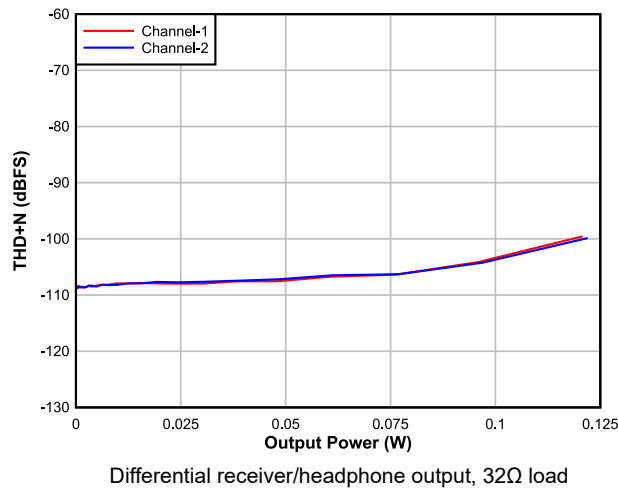
**Figure 6-13. ADC PSRR vs Frequency**



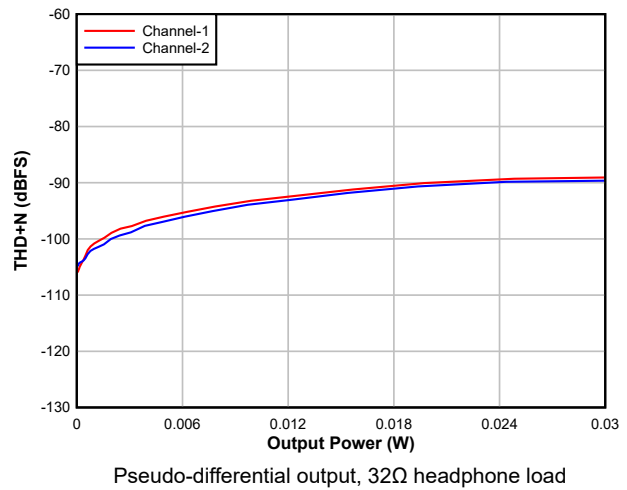
**Figure 6-14. DAC THD+N Level vs Input**



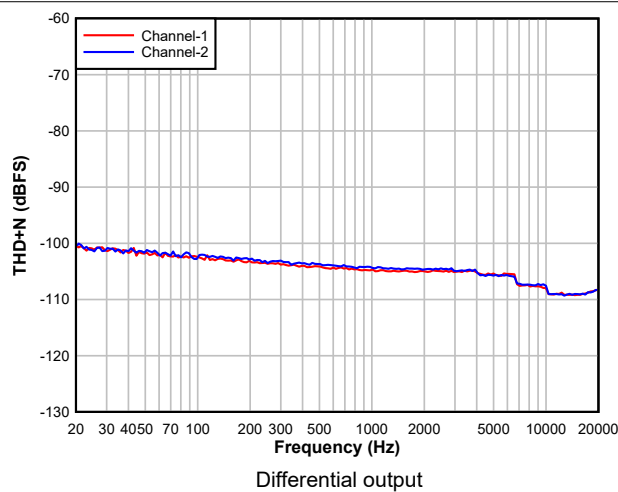
**Figure 6-15. DAC THD+N Level vs Input**



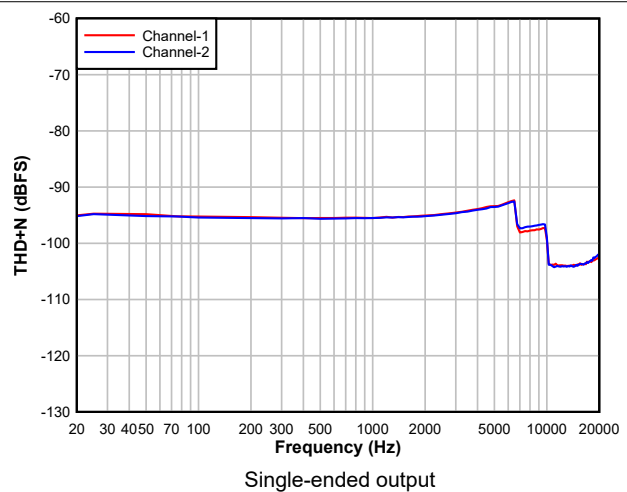
**Figure 6-16. DAC THD+N Level vs Output Power**



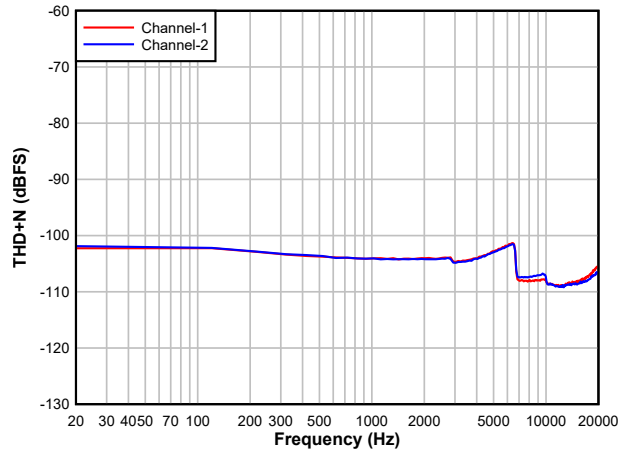
**Figure 6-17. DAC THD+N Level vs Output Power**



**Figure 6-18. DAC THD+N Level vs Frequency**

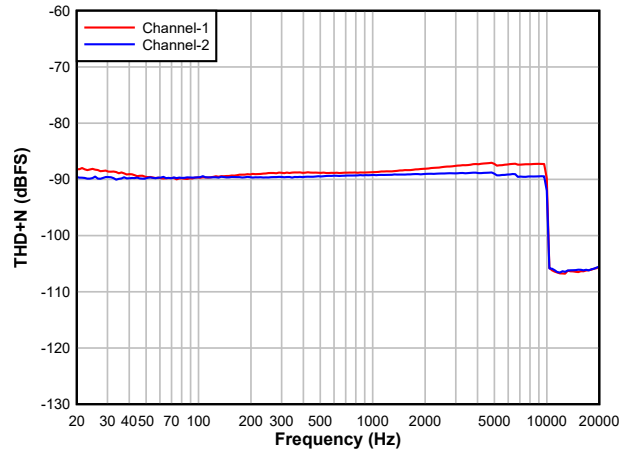


**Figure 6-19. DAC THD+N Level vs Frequency**



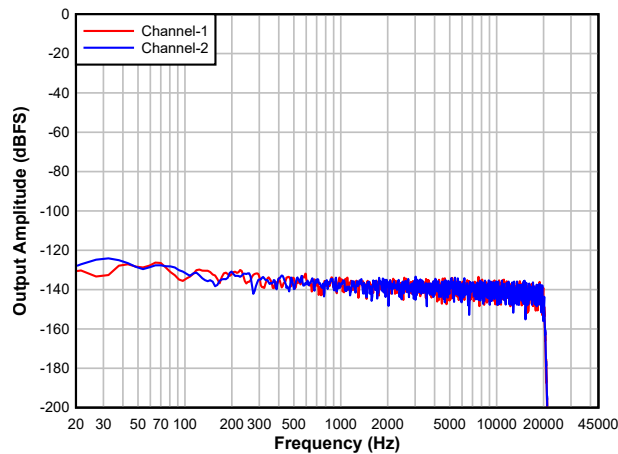
Differential receiver/headphone output, 32Ω load

**Figure 6-20. DAC THD+N Level vs Frequency**



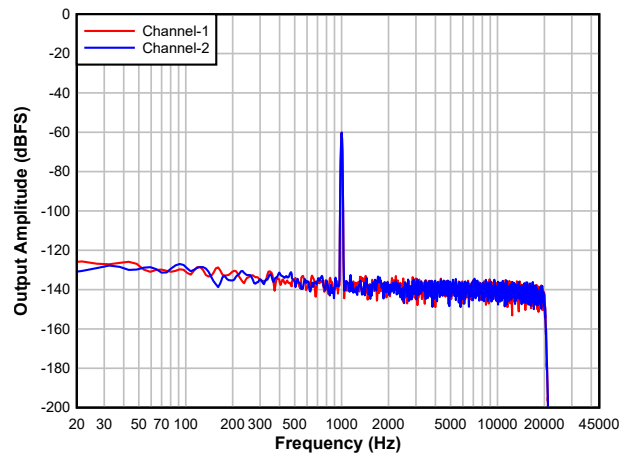
Pseudo-differential output, 32Ω headphone load

**Figure 6-21. DAC THD+N Level vs Frequency**



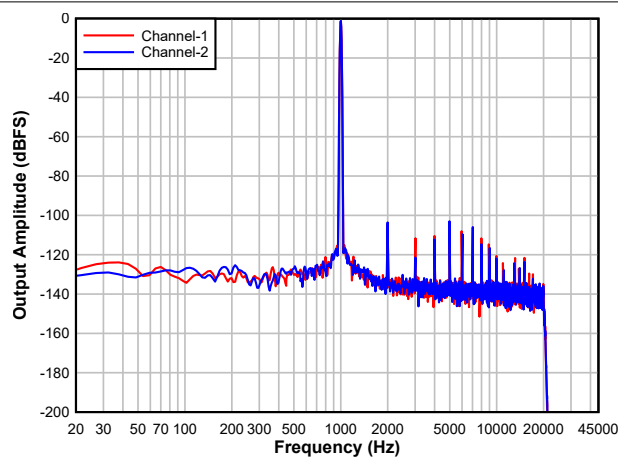
Differential output, idle-channel input

**Figure 6-22. DAC FFT**



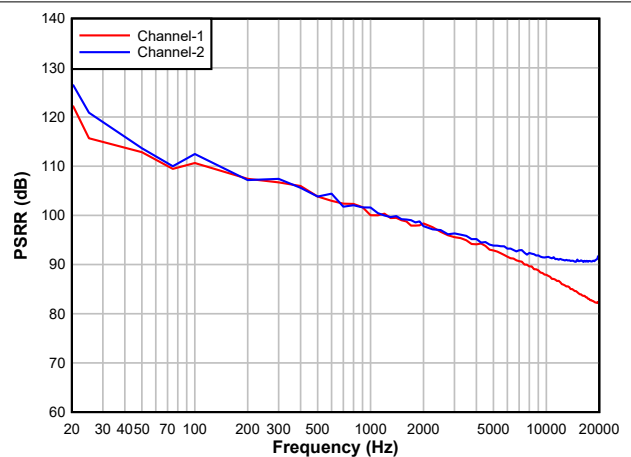
Differential output, -60dBFS input

**Figure 6-23. DAC FFT**



Differential output, -1dBFS input

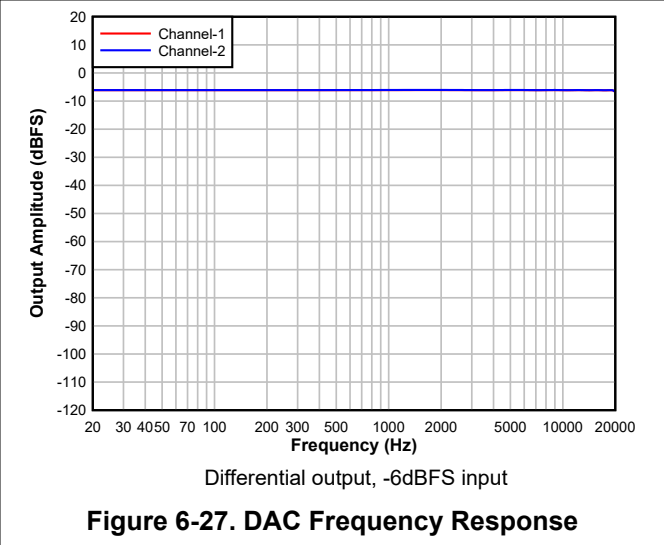
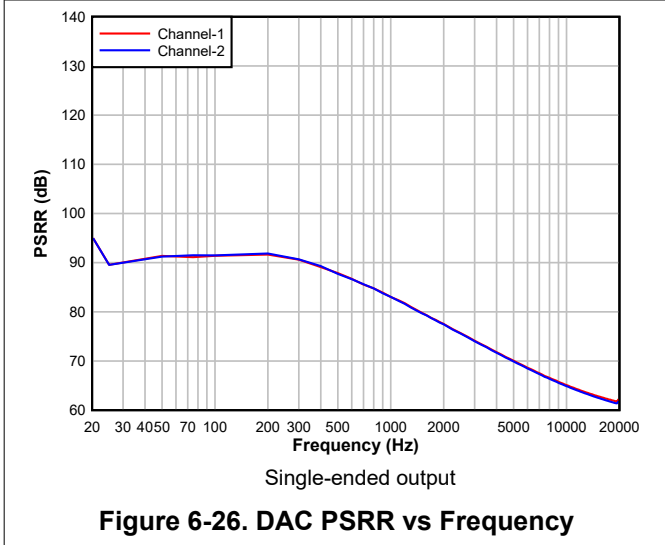
**Figure 6-24. DAC FFT**



Differential output

**Figure 6-25. DAC PSRR vs Frequency**





## 7 Detailed Description

### 7.1 Overview

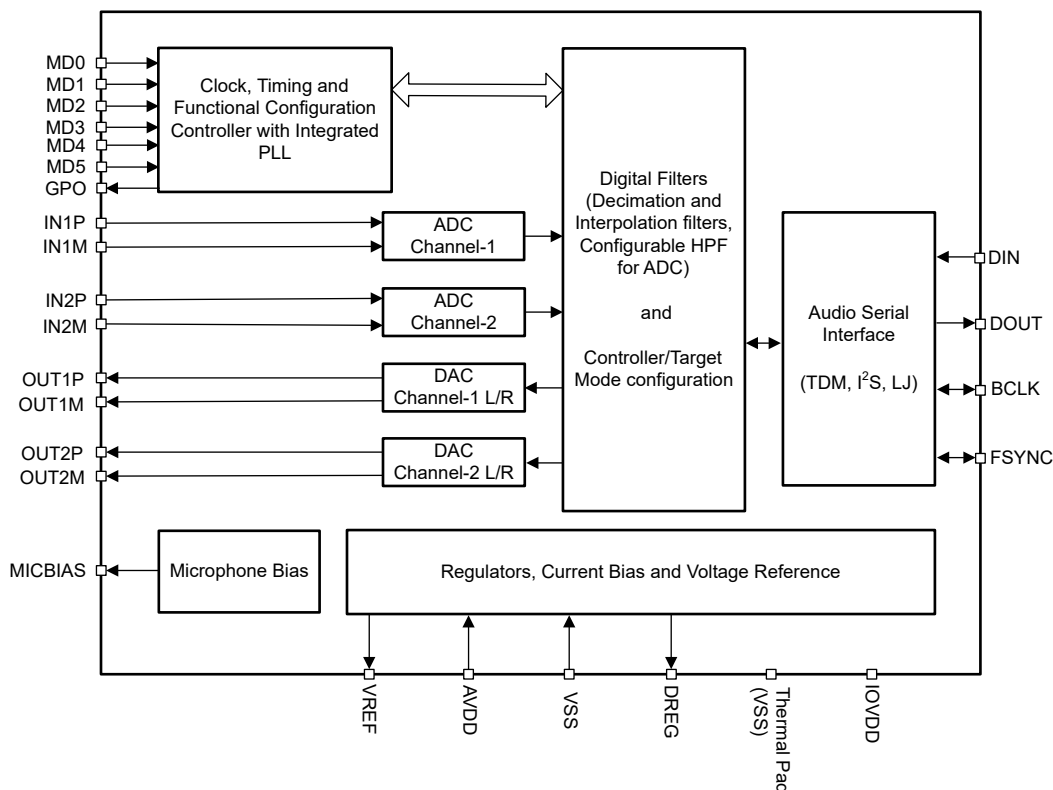
The TAC5142 is from a scalable family of devices. As part of the extended family of devices, the TAC5142 consists of a low-power, stereo, audio analog-to-digital converter (ADC) and audio digital-to-analog converter (DAC) with extensive feature integration. This device is optimized for various end-equipments and applications that require low-noise multichannel audio recording and playback and is intended for broad market applications such as ruggedized communication equipment, IP network cameras, professional audio, and multimedia applications. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained system designs. Package, performance, and compatible configuration across extended families make this device well-suited for scalable system designs.

The TAC5142 consists of the following blocks:

- Pin or Hardware controlled device configurations
- 2-channel, multi-bit, high-performance delta-sigma ( $\Delta\Sigma$ ) ADCs
- Configurable single-ended or differential audio inputs
- Low-noise microphone bias output
- High-pass filter (HPF) with selectable cut-off frequency options on ADC signal path
- 2-channel, multibit, high-performance delta-sigma ( $\Delta\Sigma$ ) DACs
- Configurable single-ended, differential, or pseudo-differential audio outputs
- Linear-phase or Low-latency digital decimation and interpolation filters
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

The device supports a flexible audio serial interface [time-division multiplexing (TDM), I<sup>2</sup>S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

### 7.3.1 Hardware Control

The device supports simple hardware-pin-controlled options to select a specific mode of operation and audio interface for a given system as summarized in [Table 7-1](#). The device is controlled through the MD0 to MD5 pins. MD1 to MD5 pins are connected to either logic low (VSS) or logic high (IOVDD), and the MD0 pin can be connected to AVDD or VSS through different pull-up or pull-down resistors.

**Table 7-1. Pin Selectable Configurations Summary**

| PIN | TARGET MODE   | CONTROLLER MODE                         |
|-----|---|---|
| MD0 | Multi-level analog input for controller/target mode and I <sup>2</sup> S/TDM/LJ mode selection  |   |
| MD1 | AVDD supply, word length, and decimation/interpolation filter type selection  | Frame rate and BCLK frequency selection |
| MD2 |   |   |
| MD3 | I <sup>2</sup> S/LJ Mode: Digital HPF cut-off frequency and input cap quick charge selection for the ADC<br>TDM Mode: Data slot selection   | Controller clock input                  |
| MD4 | ADC input configuration (Differential/Single-ended, AC/DC Coupled) and DAC output configuration (Differential Line-out/ Differential Receiver or Headphone/ Single-ended Line-out/ Pseudo-differential Headphone) |   |
| MD5 |   |   |

### 7.3.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAC5142 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus can be operated in target or controller mode through pin control. The ASI supports TDM mode for multi-channel operation, I<sup>2</sup>S, and Left-Justified (LJ) bus protocols. The data is in MSB-first, two's-complement pulse code modulation (PCM) format, with pin-selectable word-length configuration.

The device supports an audio bus controller or target mode of operation using the hardware pin MD0. In target mode, FSYNC and BCLK work as input pins whereas in controller mode, FSYNC and BCLK work as output pins generated by the device. [Table 7-2](#) shows the controller and target mode selection using the MD0 pin.

**Table 7-2. Controller and Target Mode Selection**

| MD0                            | CONTROLLER AND TARGET SELECTION  |
|--------------------------------|----------------------------------|
| Short to Ground                | Target I <sup>2</sup> S Mode     |
| Short to Ground with 4.7K Ohms | Target TDM Mode                  |
| Short to AVDD                  | Controller I <sup>2</sup> S Mode |
| Short to AVDD with 4.7K Ohms   | Controller TDM Mode              |
| Short to AVDD with 22K Ohms    | Target LJ Mode                   |

In Target mode of operation, the word length for the audio serial interface (ASI) in TAC5142 can be selected through MD1 and MD2 Pins. The TAC5142 also supports 1.8V AVDD operation in target mode with 32-bit word length. [Table 7-3](#) shows the configuration table for setting the word length, AVDD supply voltage, and decimation/interpolation filter type applicable in Target Mode. In controller mode, a fixed word length of 32-bits is supported, the decimation/interpolation filters are configured in the linear phase and the MD1 and MD2 Pins control the system clock configuration described in [Table 7-9](#).

**Table 7-3. Word Length, Supply Mode, and Decimation/Interpolation Filter Selection**

| MD2  | MD1  | WORD LENGTH, SUPPLY MODE, AND DECIMATION/INTERPOLATION FILTER SELECTION (Valid for Target Mode only) |
|------|------|--|
| Low  | Low  | AVDD=3.3V, Word Length=32, Linear-phase Filter   |
| Low  | High | AVDD=1.8V, Word Length=32, Linear-phase Filter   |
| High | Low  | AVDD=3.3V, Word Length=24, Linear-phase Filter   |
| High | High | AVDD=3.3V, Word Length=32, Low-latency phase Filter  |

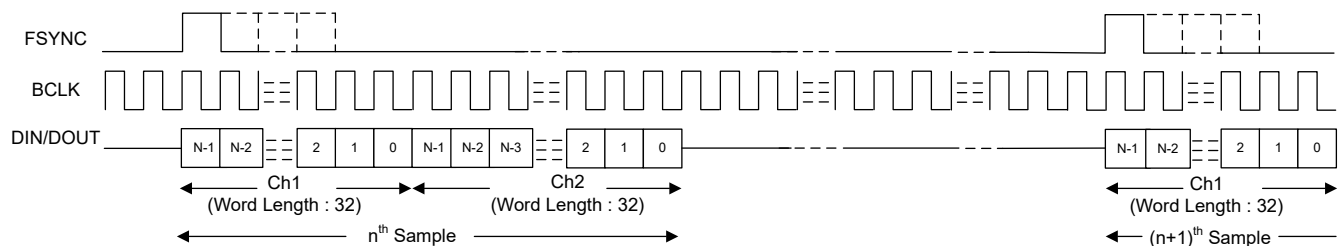
The TAC5142 offers slot configuration for target TDM mode of operation. This can be selected through MD3 pin when MD0 is configured in target TDM mode. Table 7-4 shows the slots selected in Target TDM mode of operation based on the MD3 pin. For options on MD3 in other modes of operation, refer to Table 7-1.

**Table 7-4. Data Slot Selection for TDM Target Mode**

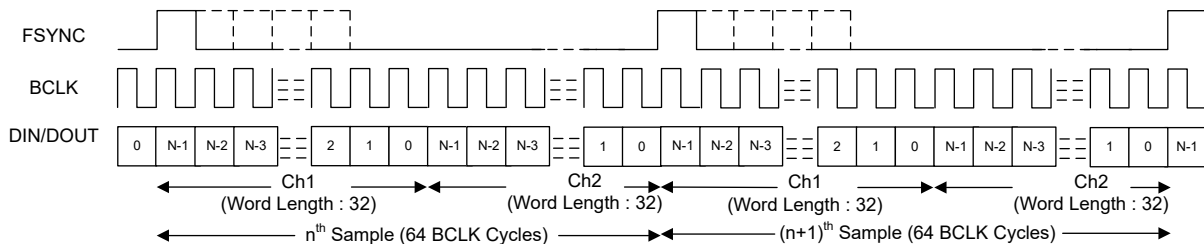
| MD3  | ADC SLOTS                | DAC SLOTS                |
|------|--------------------------|--------------------------|
| Low  | ADC Data on Slot 0 and 1 | DAC Data on Slot 0 and 1 |
| High | ADC Data on Slot 2 and 3 | DAC Data on Slot 2 and 3 |

### 7.3.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit is transmitted on the rising edge of BCLK and received on the falling edge of the BCLK. Figure 7-1 and Figure 7-2 show the protocol timing for TDM operation with various configurations.



**Figure 7-1. TDM Mode Protocol Timing (MD0 shorted to ground with 4.7KOhms) In Target Mode**



**Figure 7-2. TDM Mode Protocol Timing (MD0 shorted to AVDD with 4.7KOhms) In Controller Mode**

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active input and output channels times the configured word length of the input and output channel data. The DOUT pin is in a Hi-Z state for the extra unused bit clock cycles. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock but also supports multiples.

### 7.3.2.2 Inter IC Sound (I<sup>2</sup>S) Interface

The standard I<sup>2</sup>S protocol is defined for only two channels: left and right. In I<sup>2</sup>S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK and received on the rising edge of BCLK, in the second cycle after the *falling* edge of FSYNC. The MSB of the right slot 0 is transmitted on the falling edge of BCLK and received on the rising edge of BCLK in the second cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK and received on the rising edge of BCLK. In controller mode, FSYNC is transmitted on the rising edge of BCLK. Figure 7-3 and Figure 7-4 show the protocol timing for I<sup>2</sup>S operation in target and controller mode of operation.

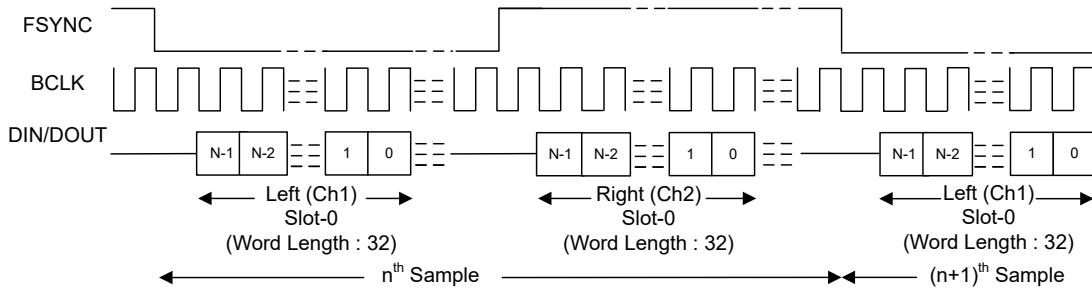


Figure 7-3. I<sup>2</sup>S Mode Protocol Timing (MD0 shorted to ground) in Target Mode

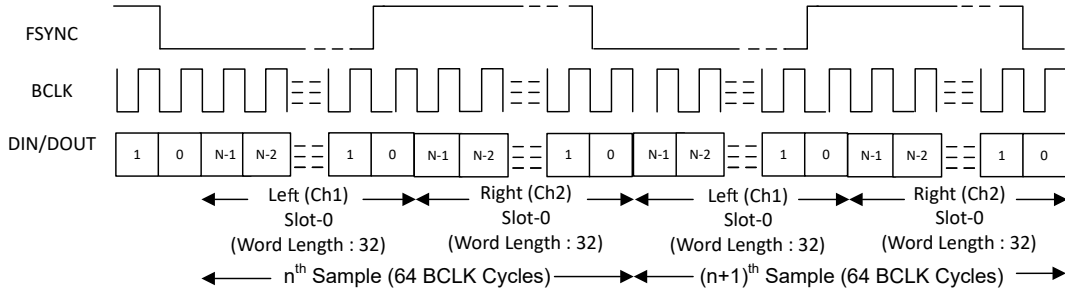


Figure 7-4. I<sup>2</sup>S Protocol Timing (MD0 shorted to AVDD) In Controller Mode

For proper operation of the audio bus in I<sup>2</sup>S mode, the number of bit clocks per frame must be greater than or equal to the number of active input and output channels (including left and right slots) times the configured word length of the input and output channel data.

### 7.3.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. In LJ mode, the MSB of the left slot 0 is transmitted and received in the same BCLK cycle after the *rising* edge of FSYNC. The MSB of the right slot 0 is transmitted and received in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK and received on the rising edge of BCLK. Figure 7-5 illustrates the protocol timing for LJ operation in the target mode of operation.

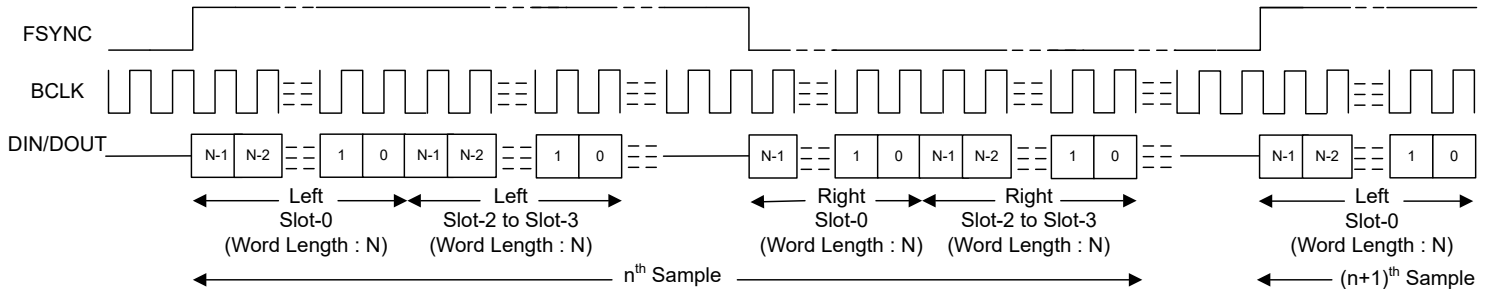


Figure 7-5. LJ Mode Standard Protocol Timing (MD0 shorted to AVDD with 22 kOhm) in Target Mode

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active input and output channels (including left and right slots) times the configured word length of the input and output channel data.

### 7.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the ADC and DAC modulators and digital filter engine, as well as other control blocks.

In the target mode of operation, the device supports the various output data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 7-5 to Table 7-8 list the supported FSYNC and BCLK frequencies depending on the IOVDD Supply.

**Table 7-5. Supported FSYNC (Multiples or Submultiples of 48kHz) and BCLK Frequencies (IOVDD - 3.3V Operation)**

| BCLK TO FSYNC RATIO | BCLK (MHz)    |                |                |                |                |                |                 |
|---------------------|---------------|----------------|----------------|----------------|----------------|----------------|-----------------|
|                     | FSYNC (8 kHz) | FSYNC (16 kHz) | FSYNC (24 kHz) | FSYNC (32 kHz) | FSYNC (48 kHz) | FSYNC (96 kHz) | FSYNC (192 kHz) |
| 16                  | Reserved      | 0.256          | 0.384          | 0.512          | 0.768          | 1.536          | 3.072           |
| 24                  | Reserved      | 0.384          | 0.576          | 0.768          | 1.152          | 2.304          | 4.608           |
| 32                  | 0.256         | 0.512          | 0.768          | 1.024          | 1.536          | 3.072          | 6.144           |
| 48                  | 0.384         | 0.768          | 1.152          | 1.536          | 2.304          | 4.608          | 9.216           |
| 64                  | 0.512         | 1.024          | 1.536          | 2.048          | 3.072          | 6.144          | 12.288          |
| 96                  | 0.768         | 1.536          | 2.304          | 3.072          | 4.608          | 9.216          | 18.432          |
| 128                 | 1.024         | 2.048          | 3.072          | 4.096          | 6.144          | 12.288         | 24.576          |
| 192                 | 1.536         | 3.072          | 4.608          | 6.144          | 9.216          | 18.432         | Reserved        |
| 256                 | 2.048         | 4.096          | 6.144          | 8.192          | 12.288         | 24.576         | Reserved        |
| 384                 | 3.072         | 6.144          | 9.216          | 12.288         | 18.432         | Reserved       | Reserved        |
| 512                 | 4.096         | 8.192          | 12.288         | 16.384         | 24.576         | Reserved       | Reserved        |

**Table 7-6. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies (IOVDD - 3.3V Operation)**

| BCLK TO FSYNC RATIO | BCLK (MHz)       |                  |                   |                  |                  |                  |                   |
|---------------------|------------------|------------------|-------------------|------------------|------------------|------------------|-------------------|
|                     | FSYNC (7.35 kHz) | FSYNC (14.7 kHz) | FSYNC (22.05 kHz) | FSYNC (29.4 kHz) | FSYNC (44.1 kHz) | FSYNC (88.2 kHz) | FSYNC (176.4 kHz) |
| 16                  | Reserved         | Reserved         | 0.3528            | 0.4704           | 0.7056           | 1.4112           | 2.8224            |
| 24                  | Reserved         | 0.3528           | 0.5292            | 0.7056           | 1.0584           | 2.1168           | 4.2336            |
| 32                  | Reserved         | 0.4704           | 0.7056            | 0.9408           | 1.4112           | 2.8224           | 5.6448            |
| 48                  | 0.3528           | 0.7056           | 1.0584            | 1.4112           | 2.1168           | 4.2336           | 8.4672            |
| 64                  | 0.4704           | 0.9408           | 1.4112            | 1.8816           | 2.8224           | 5.6448           | 11.2896           |
| 96                  | 0.7056           | 1.4112           | 2.1168            | 2.8224           | 4.2336           | 8.4672           | 16.9344           |
| 128                 | 0.9408           | 1.8816           | 2.8224            | 3.7632           | 5.6448           | 11.2896          | 22.5792           |
| 192                 | 1.4112           | 2.8224           | 4.2336            | 5.6448           | 8.4672           | 16.9344          | Reserved          |
| 256                 | 1.8816           | 3.7632           | 5.6448            | 7.5264           | 11.2896          | 22.5792          | Reserved          |
| 384                 | 2.8224           | 5.6448           | 8.4672            | 11.2896          | 16.9344          | Reserved         | Reserved          |
| 512                 | 3.7632           | 7.5264           | 11.2896           | 15.0528          | 22.5792          | Reserved         | Reserved          |

**Table 7-7. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies (IOVDD - 1.8V Operation)**

| BCLK TO FSYNC RATIO | BCLK (MHz)    |                |                |                |                |                |                 |
|---------------------|---------------|----------------|----------------|----------------|----------------|----------------|-----------------|
|                     | FSYNC (8 kHz) | FSYNC (16 kHz) | FSYNC (24 kHz) | FSYNC (32 kHz) | FSYNC (48 kHz) | FSYNC (96 kHz) | FSYNC (192 kHz) |
| 16                  | Reserved      | 0.256          | 0.384          | 0.512          | 0.768          | 1.536          | 3.072           |
| 24                  | Reserved      | 0.384          | 0.576          | 0.768          | 1.152          | 2.304          | 4.608           |
| 32                  | 0.256         | 0.512          | 0.768          | 1.024          | 1.536          | 3.072          | 6.144           |

**Table 7-7. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies (IOVDD - 1.8V Operation) (continued)**

| BCLK TO FSYNC RATIO | BCLK (MHz)    |                |                |                |                |                |                 |
|---------------------|---------------|----------------|----------------|----------------|----------------|----------------|-----------------|
|                     | FSYNC (8 kHz) | FSYNC (16 kHz) | FSYNC (24 kHz) | FSYNC (32 kHz) | FSYNC (48 kHz) | FSYNC (96 kHz) | FSYNC (192 kHz) |
| 48                  | 0.384         | 0.768          | 1.152          | 1.536          | 2.304          | 4.608          | 9.216           |
| 64                  | 0.512         | 1.024          | 1.536          | 2.048          | 3.072          | 6.144          | 12.288          |
| 96                  | 0.768         | 1.536          | 2.304          | 3.072          | 4.608          | 9.216          | Reserved        |
| 128                 | 1.024         | 2.048          | 3.072          | 4.096          | 6.144          | 12.288         | Reserved        |
| 192                 | 1.536         | 3.072          | 4.608          | 6.144          | 9.216          | Reserved       | Reserved        |
| 256                 | 2.048         | 4.096          | 6.144          | 8.192          | 12.288         | Reserved       | Reserved        |
| 384                 | 3.072         | 6.144          | 9.216          | 12.288         | Reserved       | Reserved       | Reserved        |
| 512                 | 4.096         | 8.192          | 12.288         | Reserved       | Reserved       | Reserved       | Reserved        |

**Table 7-8. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies (IOVDD - 1.8V Operation)**

| BCLK TO FSYNC RATIO | BCLK (MHz)       |                  |                   |                  |                  |                  |                   |
|---------------------|------------------|------------------|-------------------|------------------|------------------|------------------|-------------------|
|                     | FSYNC (7.35 kHz) | FSYNC (14.7 kHz) | FSYNC (22.05 kHz) | FSYNC (29.4 kHz) | FSYNC (44.1 kHz) | FSYNC (88.2 kHz) | FSYNC (176.4 kHz) |
| 16                  | Reserved         | Reserved         | 0.3528            | 0.4704           | 0.7056           | 1.4112           | 2.8224            |
| 24                  | Reserved         | 0.3528           | 0.5292            | 0.7056           | 1.0584           | 2.1168           | 4.2336            |
| 32                  | Reserved         | 0.4704           | 0.7056            | 0.9408           | 1.4112           | 2.8224           | 5.6448            |
| 48                  | 0.3528           | 0.7056           | 1.0584            | 1.4112           | 2.1168           | 4.2336           | 8.4672            |
| 64                  | 0.4704           | 0.9408           | 1.4112            | 1.8816           | 2.8224           | 5.6448           | 11.2896           |
| 96                  | 0.7056           | 1.4112           | 2.1168            | 2.8224           | 4.2336           | 8.4672           | Reserved          |
| 128                 | 0.9408           | 1.8816           | 2.8224            | 3.7632           | 5.6448           | 11.2896          | Reserved          |
| 192                 | 1.4112           | 2.8224           | 4.2336            | 5.6448           | 8.4672           | Reserved         | Reserved          |
| 256                 | 1.8816           | 3.7632           | 5.6448            | 7.5264           | 11.2896          | Reserved         | Reserved          |
| 384                 | 2.8224           | 5.6448           | 8.4672            | 11.2896          | Reserved         | Reserved         | Reserved          |
| 512                 | 3.7632           | 7.5264           | 11.2896           | Reserved         | Reserved         | Reserved         | Reserved          |

In the controller mode of operation, the device uses the MD3 pin, as the system clock, and CCLK as the reference input clock source. In target mode of operation, the MD3 pin function is described in [Table 7-4](#) and [Table 7-11](#).

The device provides flexibility in FSYNC selection with a supported system clock frequency option of either  $256 \times f_S$  or  $128 \times f_S$  or a fixed 48/44.1kHz or 96/88.2kHz as configured using the MD1 and MD2 pins. [Table 7-9](#) shows the FSYNC and BCLK selection for the controller mode using the MD1 and MD2 pins.

**Table 7-9. System Clock Selection for the Controller Mode**

| MD2  | MD1  | SYSTEM CLOCK SELECTION (Valid for Controller Mode Only) |                       |  |
|------|------|---|-----------------------|--|
|      |      | FSYNC   | BCLK TO FSYNC RATIO   |  |
|      |      |   | I <sup>2</sup> S MODE | TDM MODE   |
| LOW  | LOW  | CCLK/256  | 64                    | 256 for FSYNC ≤ 48kHz,<br>128 for 48kHz < FSYNC ≤ 96kHz, and<br>64 for FSYNC > 96kHz |
| LOW  | HIGH | CCLK/128  |                       |  |
| HIGH | LOW  | 96/88.2kHz  |                       |  |
| HIGH | HIGH | 48/44.1kHz  |                       |  |

See [Table 7-3](#) for the MD1 and MD2 pin functions in the target mode of operation. In the controller mode of operation, AVDD = 3.3V and Word-Length = 32 and a linear-phase decimation/interpolation filter is applicable.

### 7.3.4 Analog Input and Output Configurations

The device supports simultaneous recording of up to two channels using the high-performance stereo ADC. The device consists of two pairs of analog input pins (INxP and INxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for the analog pins can be from electret-condenser analog microphones, micro electrical-mechanical system (MEMS) analog microphones, or line-in (auxiliary) inputs from the system board.

The voice or audio signal inputs can be capacitively coupled (AC-coupled) or DC-coupled to the device. For best distortion performance, use of low-voltage coefficient capacitors for AC-coupling is recommended. The typical input impedance for the TAC5142 is 42k $\Omega$  for the INxP or INxM pins with  $\pm 20\%$  variation. The value of the coupling capacitor in AC-coupled mode must be chosen so that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. Before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage at power-up. To enable quick charging, the device has a quick charge scheme to speed up the charging of the coupling capacitor at power-up when operating in the I<sup>2</sup>S/LJ target mode. This input cap quick charge setting can be enabled by configuring the MD3 pin. The MD3 pin also configures the digital HPF cut-off frequency of the ADC signal path when the device is operating in I<sup>2</sup>S/LJ target mode as described in [Table 7-11](#).

For optimal performance, the common-mode variation at the device input should be limited to less than 100mVpp for AC-coupled settings. For applications that cannot avoid large common-mode fluctuations, the device offers the modes to configure the device for higher common-mode tolerance for both single-ended and differential applications.

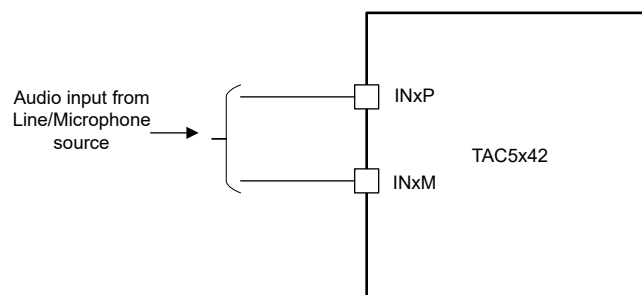
The device supports playback of two channels using the high-performance stereo DAC. The device consists of two pairs of analog output pins (OUTxP and OUTxM) which can be configured in single-ended or differential input mode by setting MD4 and MD5 pins. The input source for these channels is from TDM/I<sup>2</sup>S/LJ interface.

[Table 7-10](#) shows the analog input output configuration modes available with MD4 and MD5 configuration.

**Table 7-10. Analog Input and Output Configurations**

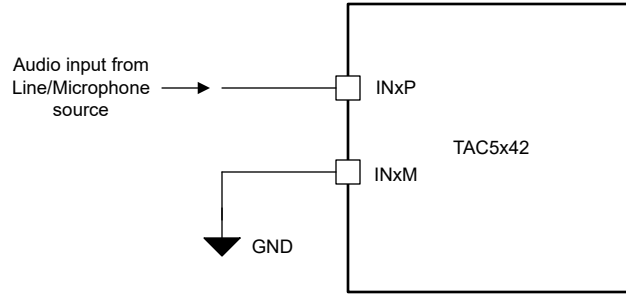
| MD5  | MD4  | ANALOG INPUT CONFIGURATION   | ANALOG OUTPUT CONFIGURATION   |
|------|------|--|---|
| Low  | Low  | Differential input; AC-Coupled only  | Differential Output; Line-out only  |
| Low  | High | Differential input; AC or DC-Coupled with High Common Mode Tolerance         | Differential Output; Receiver/Headphone load or Line-out                        |
| High | Low  | Single Ended Input on INxP; AC-Coupled only                                  | Single-ended output; Line-out only  |
| High | High | Single Ended Input on INxP; AC or DC-Coupled with High Common Mode Tolerance | Pseudo-differential output with external common-mode sense; Headphone load only |

[Figure 7-6](#) to [Figure 7-9](#) show the typical configuration diagrams for the various input configuration modes and [Figure 7-10](#) to [Figure 7-12](#) show the typical configuration diagrams for the various output modes.

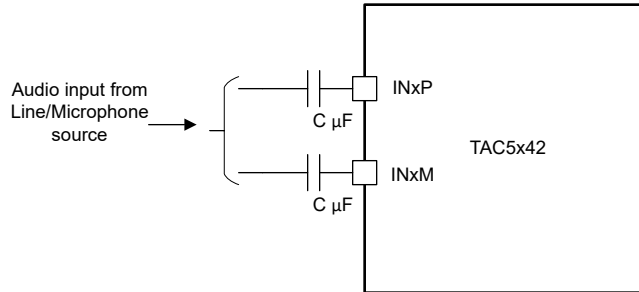


**Figure 7-6. DC-Coupled Microphone or Line Differential Input Connection**

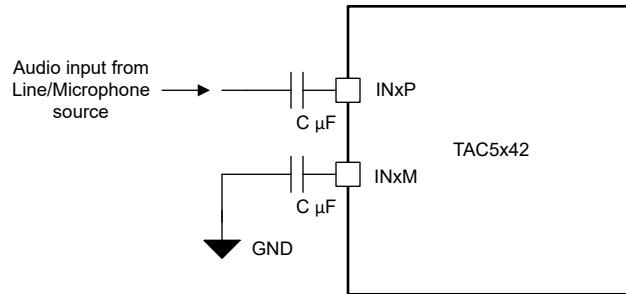




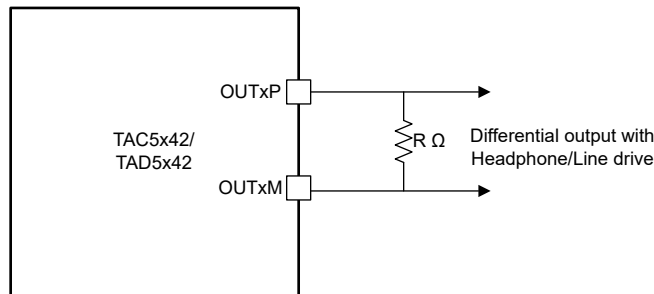
**Figure 7-7. DC-Coupled Microphone or Line Single-Ended Input Connection**



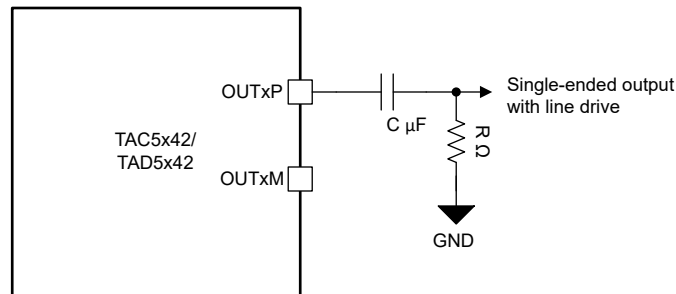
**Figure 7-8. AC-Coupled Microphone or Line Differential Input Connection**



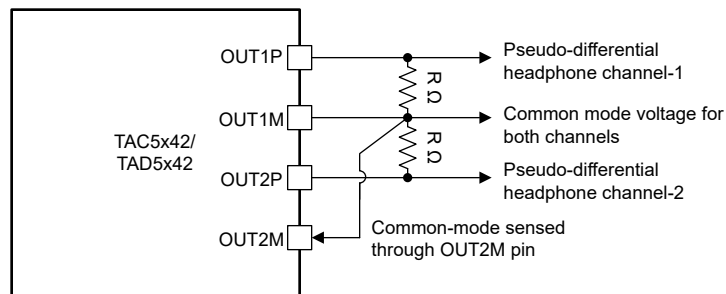
**Figure 7-9. AC-Coupled Microphone or Line Single-Ended Input Connection**



**Figure 7-10. Differential Output Connection**



**Figure 7-11. Single-ended Output Connection**



**Figure 7-12. Pseudo-differential Output Connection with External Common-Mode Sense**

### 7.3.5 Reference Voltage

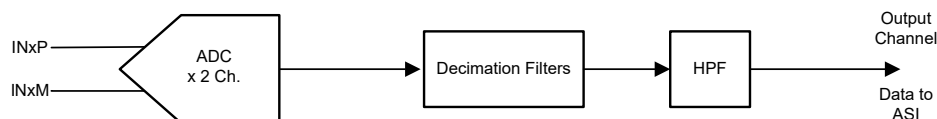
All audio data converters require a DC reference voltage. The TAC5142 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1 $\mu$ F capacitor connected from the VREF pin to the analog ground (VSS). The value of this reference voltage, VREF, is set to 2.75V, which in turn supports a 2V<sub>RMS</sub> differential full-scale input and 2V<sub>RMS</sub> differential full-scale output to the device. The required minimum AVDD voltage for this VREF voltage is 3V. When the device is configured for 1.8V AVDD supply voltage, the voltage on the VREF pin is 1.375V, which in turn supports a 1V<sub>RMS</sub> differential full-scale input to the device. Do not connect any external load to a VREF pin.

### 7.3.6 Integrated Microphone Bias

The device integrates a built-in, low-noise microphone bias pin that outputs a high PSRR, low noise output voltage equal to VREF that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphones. The integrated bias amplifier supports up to 5mA of load current that can be used for multiple microphones. When using this MICBIAS pin for biasing or supplying various microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones.

### 7.3.7 ADC Signal-Chain

The TAC5142 ADC signal chain is comprised of very low-noise, high-performance, and low-power analog blocks and configurable digital processing blocks. Figure 7-13 shows a conceptual block diagram for the TAC5142 that highlights the key components of the record-path signal chain.



**Figure 7-13. ADC Signal-Chain Processing Flowchart**

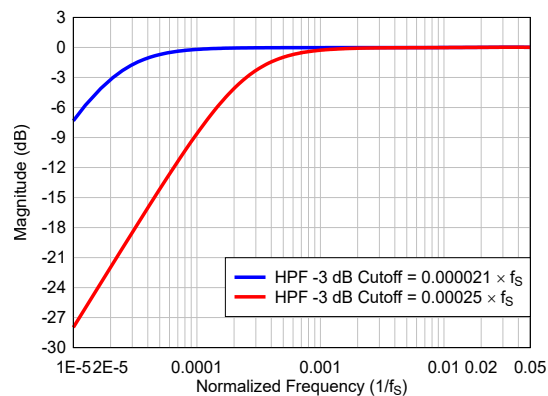
The high performance and flexibility combined with a compact package make the device optimized for a variety of end-equipments and applications that require multichannel audio capture. The ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multi-stage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation followed by a high-pass filter (HPF) with configurable cut-off frequency described further. The TAC5142 supports sample rates of up to 192kHz in both controller and target mode of operation.

### 7.3.7.1 Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a configurable high-pass filter (HPF) with a  $-3\text{dB}$  cut-off frequency of  $0.000021 \times f_s$  or  $0.00025 \times f_s$ . The HPF is not a channel-independent filter but is globally applicable for all the ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter and is efficient enough to filter out possible DC components of the signal. This configuration is only available in Target I<sup>2</sup>S or LJ modes of operation. In the Target TDM Mode of operation, MD3 is used to set slots for input and output data streams as described in Table 7-4 and in Controller Mode, MD3 is used as CCLK input as described in Table 7-9, and in these modes, the HPF is by default set to  $0.000021 \times f_s$ . Additionally, as a lower frequency filter in digital requires a higher value capacitor as well for low droop at the cutoff frequency, the device also adjusts the input cap quick charge time along with the HPF cut-off with this configuration. Table 7-11 shows the MD3 configuration and  $-3\text{dB}$  cutoff frequency value and input cap quick charge setting. Figure 7-14 shows a frequency response plot for the HPF filter.

**Table 7-11. Input Cap Quick-Charge and HPF HPF Cutoff Frequency Selections for ADC in Target I<sup>2</sup>S/LJ Mode**

| MD3  | INPUT CAP QUICK CHARGE | HPF $-3\text{dB}$ CUT-OFF FREQUENCY | HPF $-3\text{dB}$ CUTT-OFF FREQUENCY @ 48 kHz SAMPLE RATE |
|------|------------------------|-------------------------------------|---|
| Low  | Disabled (50ms time)   | $0.000021 \times f_s$               | 1Hz   |
| High | Enabled (12.5ms time)  | $0.00025 \times f_s$                | 12Hz  |



**Figure 7-14. HPF Filter Frequency Response Plot**

### 7.3.7.2 Configurable Digital Decimation Filters

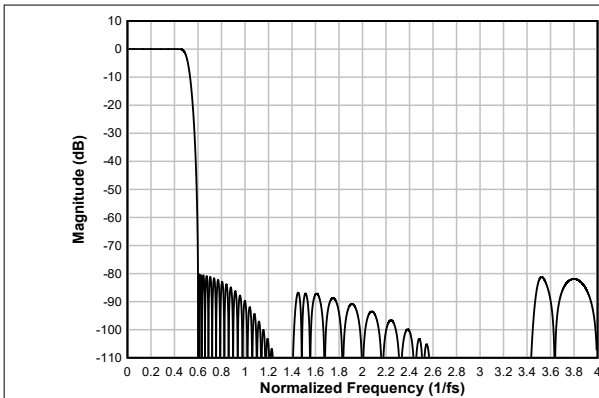
The device record channel includes a high dynamic range, built-in digital decimation filter to process the oversampled data from the multibit delta-sigma ( $\Delta\Sigma$ ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. The decimation filters in the device can be selected to linear-phase or low-latency filters based on the state of the MD2 and MD1 pins according to [Table 7-3](#). This makes the device suitable for a wide variety of audio applications. Following section describes the filter response for different samples rates.

#### 7.3.7.2.1 Linear-phase filters

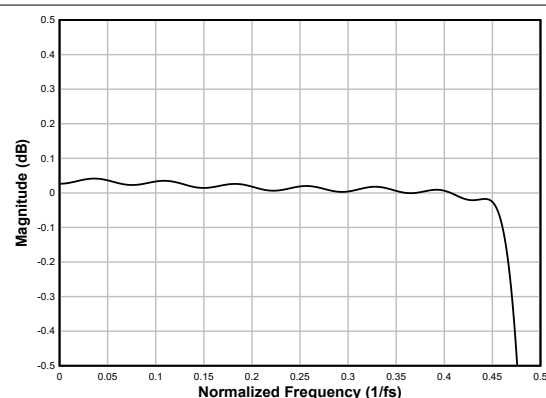
The linear-phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

##### 7.3.7.2.1.1 Sampling Rate: 8kHz or 7.35kHz

[Figure 7-15](#) and [Figure 7-16](#) respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 8kHz or 7.35kHz, and [Table 7-12](#) lists its specifications.



**Figure 7-15. Linear-phase Decimation Filter Magnitude Response**



**Figure 7-16. Linear-phase Decimation Filter Pass-Band Ripple**

**Table 7-12. Linear-phase Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                                       | MIN   | TYP  | MAX  | UNIT    |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.454 \times f_S$            | -0.04 |      | 0.04 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ to $4 \times f_S$ | 80.2  |      |      | dB      |
|                        | Frequency range is $4 \times f_S$ onwards             | 84.7  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$            |       | 16.1 |      | $1/f_S$ |

### 7.3.7.2.1.2 Sampling Rate: 16kHz or 14.7kHz

Figure 7-17 and Figure 7-18 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 16kHz or 14.7kHz, and Table 7-13 lists its specifications.

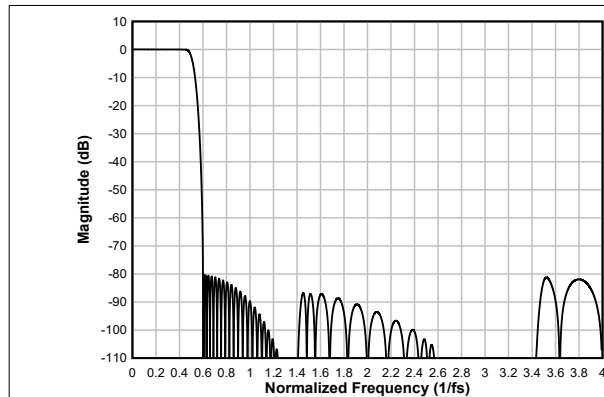


Figure 7-17. Linear-phase Decimation Filter Magnitude Response

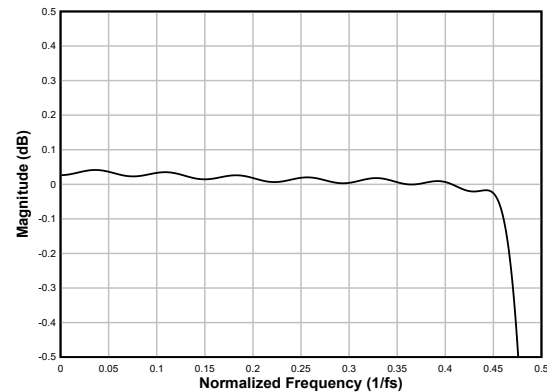


Figure 7-18. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-13. Linear-phase Decimation Filter Specifications

| PARAMETER              | TEST CONDITIONS                                       | MIN   | TYP  | MAX  | UNIT    |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.454 \times f_S$            | -0.04 |      | 0.04 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ to $4 \times f_S$ | 80.2  |      |      | dB      |
|                        | Frequency range is $4 \times f_S$ onwards             | 84.7  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$            |       | 16.1 |      | $1/f_S$ |

### 7.3.7.2.1.3 Sampling Rate: 24kHz or 22.05kHz

Figure 7-19 and Figure 7-20 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 24kHz or 22.05kHz, and Table 7-14 lists its specifications.

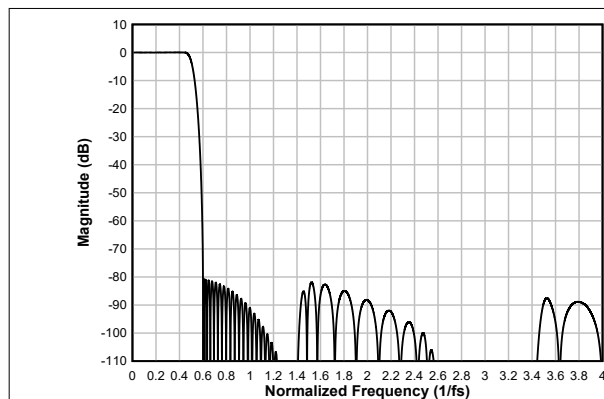


Figure 7-19. Linear-phase Decimation Filter Magnitude Response

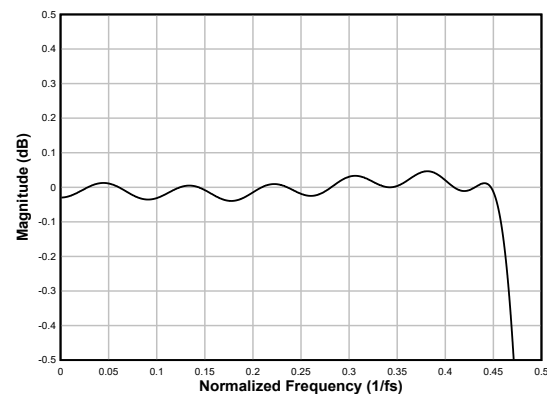


Figure 7-20. Linear-phase Decimation Filter Pass-Band Ripple

Table 7-14. Linear-phase Decimation Filter Specifications

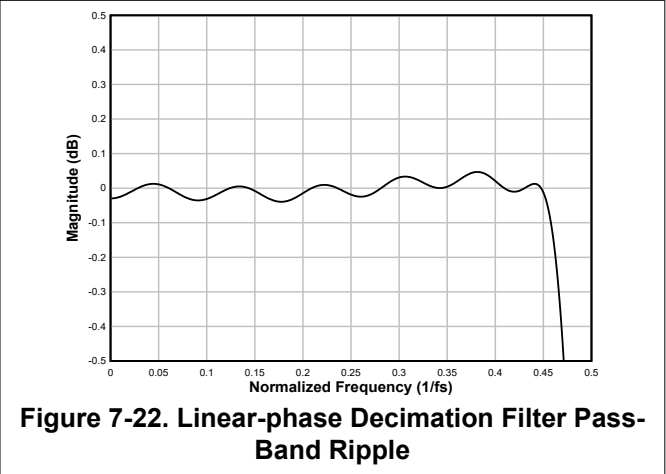
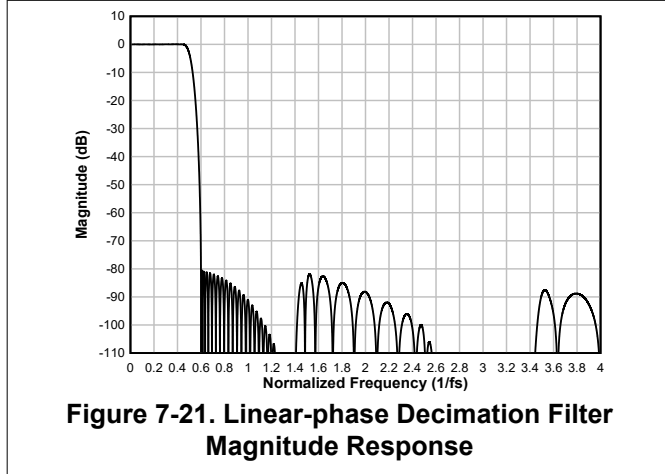
| PARAMETER             | TEST CONDITIONS                                       | MIN   | TYP | MAX  | UNIT |
|-----------------------|---|-------|-----|------|------|
| Pass-band ripple      | Frequency range is 0 to $0.455 \times f_S$            | -0.05 |     | 0.05 | dB   |
| Stop-band attenuation | Frequency range is $0.6 \times f_S$ to $4 \times f_S$ | 80.6  |     |      | dB   |
|                       | Frequency range is $4 \times f_S$ onwards             | 93    |     |      |      |

**Table 7-14. Linear-phase Decimation Filter Specifications (continued)**

| PARAMETER              | TEST CONDITIONS                            | MIN | TYP  | MAX | UNIT    |
|------------------------|--|-----|------|-----|---------|
| Group delay or latency | Frequency range is 0 to $0.455 \times f_s$ |     | 14.7 |     | $1/f_s$ |

**7.3.7.2.1.4 Sampling Rate: 32kHz or 29.4kHz**

Figure 7-21 and Figure 7-22 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 32kHz or 29.4kHz, and Table 7-15 lists its specifications.

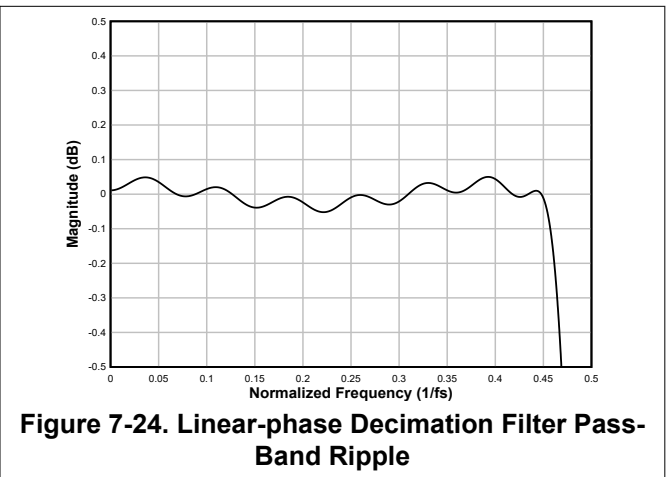
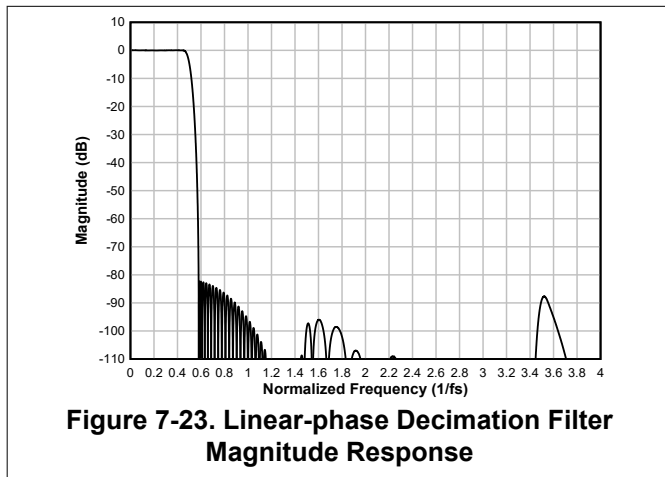


**Table 7-15. Linear-phase Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                                       | MIN   | TYP  | MAX  | UNIT    |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_s$            | -0.05 |      | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_s$ to $4 \times f_s$ | 80.6  |      |      | dB      |
|                        | Frequency range is $4 \times f_s$ onwards             | 92.9  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.455 \times f_s$            |       | 14.7 |      | $1/f_s$ |

**7.3.7.2.1.5 Sampling Rate: 48kHz or 44.1kHz**

Figure 7-23 and Figure 7-24 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 48kHz or 44.1kHz, and Table 7-16 lists its specifications.

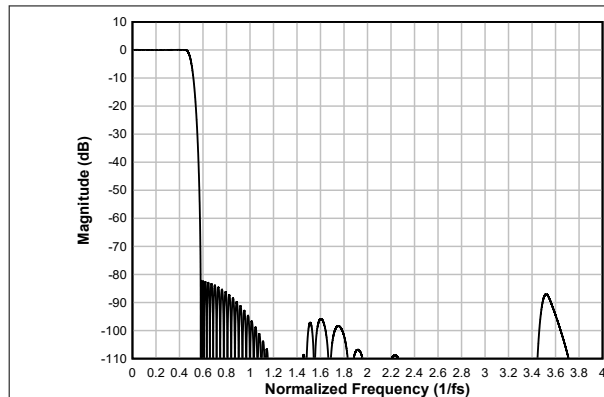
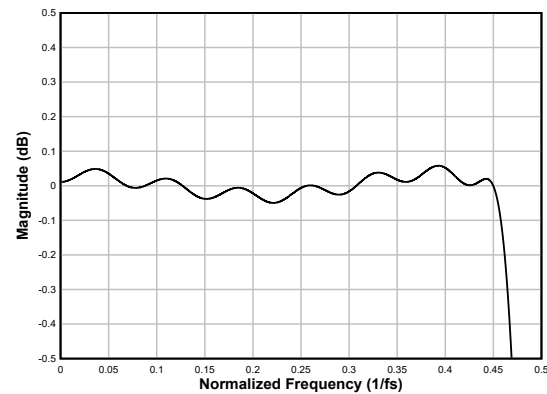


**Table 7-16. Linear-phase Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS  | MIN   | TYP | MAX  | UNIT    |
|------------------------|--|-------|-----|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.454 \times f_S$             | -0.05 |     | 0.05 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_S$ to $4 \times f_S$ | 82.2  |     |      | dB      |
|                        | Frequency range is $4 \times f_S$ onwards              | 98    |     |      |         |
| Group delay or latency | Frequency range is 0 to $0.454 \times f_S$             |       | 17  |      | $1/f_S$ |

**7.3.7.2.1.6 Sampling Rate: 96kHz or 88.2kHz**

Figure 7-25 and Figure 7-26 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 96kHz or 88.2kHz, and Table 7-17 lists its specifications.

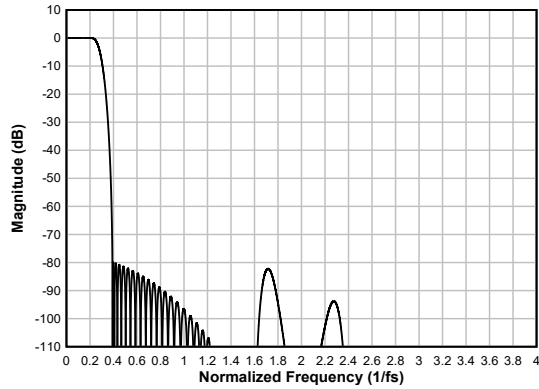
**Figure 7-25. Linear-phase Decimation Filter Magnitude Response****Figure 7-26. Linear-phase Decimation Filter Pass-Band Ripple****Table 7-17. Linear-phase Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS  | MIN   | TYP  | MAX  | UNIT    |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_S$             | -0.05 |      | 0.06 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_S$ to $4 \times f_S$ | 82.2  |      |      | dB      |
|                        | Frequency range is $4 \times f_S$ onwards              | 87    |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.455 \times f_S$             |       | 16.9 |      | $1/f_S$ |

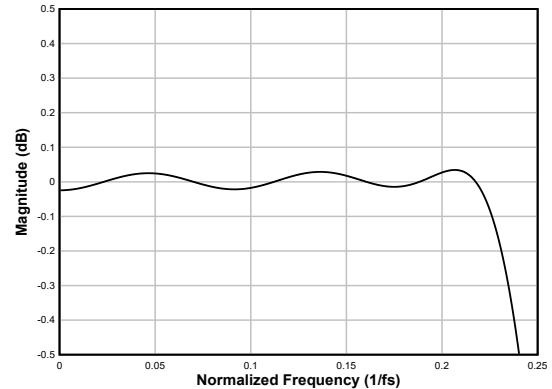
**7.3.7.2.1.7 Sampling Rate: 192kHz or 176.4kHz**

Figure 7-27 and Figure 7-28 respectively show the magnitude response and the pass-band ripple for this decimation filter with a sampling rate of 192kHz or 176.4kHz, and Table 7-18 lists its specifications.





**Figure 7-27. Linear-phase Decimation Filter Magnitude Response**



**Figure 7-28. Linear-phase Decimation Filter Pass-Band Ripple**

**Table 7-18. Linear-phase Decimation Filter Specifications**

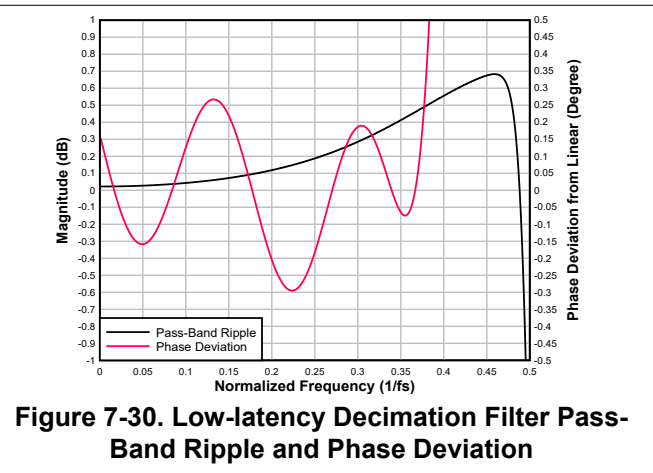
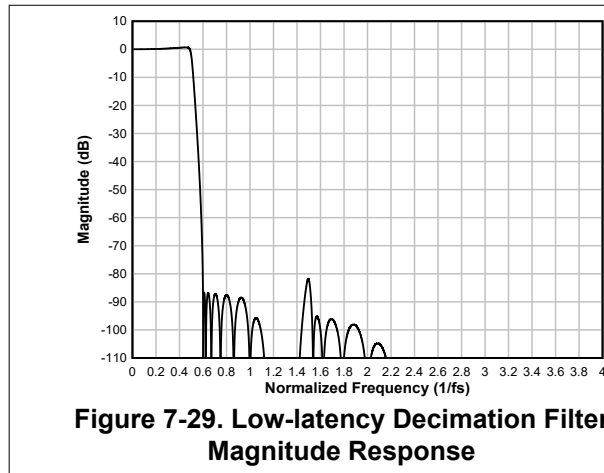
| PARAMETER              | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT    |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.223 \times f_S$              | -0.04 |      | 0.04 | dB      |
| Stop-band attenuation  | Frequency range is $0.391 \times f_S$ to $4 \times f_S$ | 80    |      |      |         |
|                        | Frequency range is $4 \times f_S$ onwards               | 82.2  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.258 \times f_S$              |       | 11.6 |      | $1/f_S$ |

### 7.3.7.2.2 Low-latency Filters

For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency decimation filters on the TAC5142 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the  $0.376 \times f_S$  frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

#### 7.3.7.2.2.1 Sampling Rate: 24kHz or 22.05kHz

Figure 7-29 shows the magnitude response and Figure 7-30 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 24kHz or 22.05kHz. Table 7-19 lists its specifications.

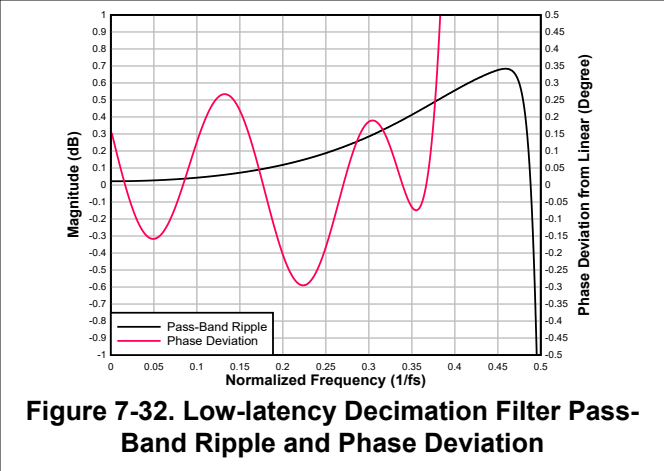
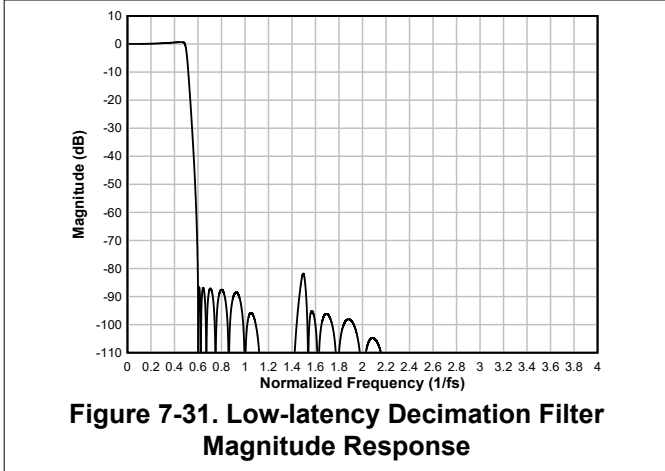


**Table 7-19. Low-latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                                       | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.492 \times f_S$            | -0.67  |     | -0.67 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ to $4 \times f_S$ | 81.8   |     |       | dB      |
|                        | Frequency range is $4 \times f_S$ onwards             | 115    |     |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$            |        | 6.5 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$            | -0.092 |     | 0.029 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.376 \times f_S$            | -0.3   |     | 0.27  | Degrees |

#### 7.3.7.2.2.2 Sampling Rate: 32kHz or 29.4kHz

Figure 7-31 shows the magnitude response and Figure 7-32 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 32kHz or 29.4kHz. Table 7-20 lists its specifications.

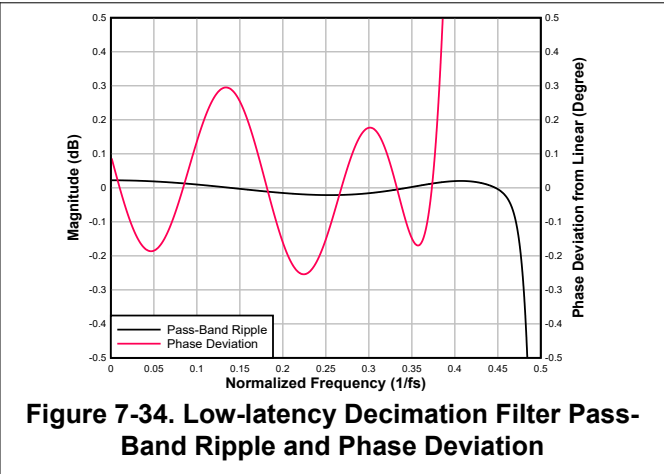
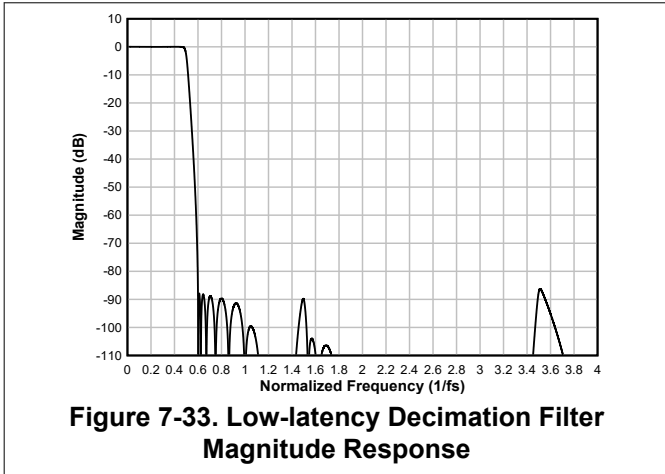


**Table 7-20. Low-latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS                                       | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.492 \times f_S$            | -0.67  |     | -0.67 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ to $4 \times f_S$ | 81.8   |     |       | dB      |
|                        | Frequency range is $4 \times f_S$ onwards             | 115    |     |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$            |        | 6.5 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$            | -0.092 |     | 0.029 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.376 \times f_S$            | -0.3   |     | 0.27  | Degrees |

**7.3.7.2.2.3 Sampling Rate: 48kHz or 44.1kHz**

Figure 7-33 shows the magnitude response and Figure 7-34 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 48kHz or 44.1kHz. Table 7-21 lists its specifications.



**Table 7-21. Low-latency Decimation Filter Specifications**

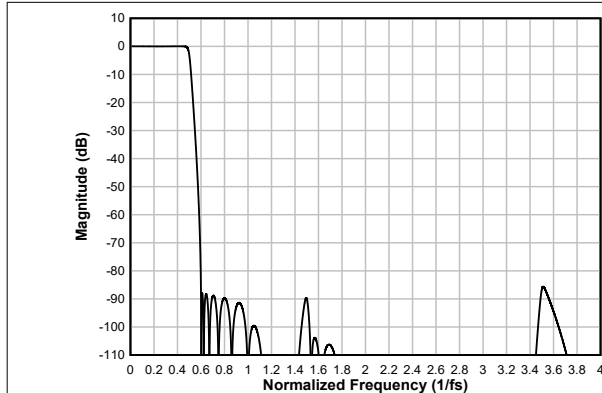
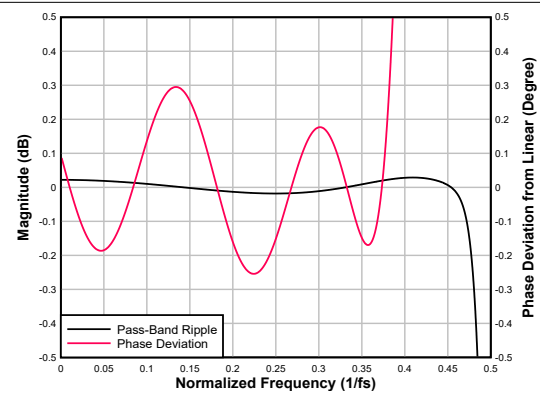
| PARAMETER              | TEST CONDITIONS                                       | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.456 \times f_S$            | -0.02  |     | -0.02 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ to $4 \times f_S$ | 86.3   |     |       | dB      |
|                        | Frequency range is $4 \times f_S$ onwards             | 96.8   |     |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$            |        | 6.6 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$            | -0.086 |     | 0.027 | $1/f_S$ |

**Table 7-21. Low-latency Decimation Filter Specifications (continued)**

| PARAMETER       | TEST CONDITIONS                            | MIN   | TYP | MAX | UNIT    |
|-----------------|--|-------|-----|-----|---------|
| Phase deviation | Frequency range is 0 to $0.376 \times f_S$ | -0.25 |     | 0.3 | Degrees |

**7.3.7.2.2.4 Sampling Rate: 96kHz or 88.2kHz**

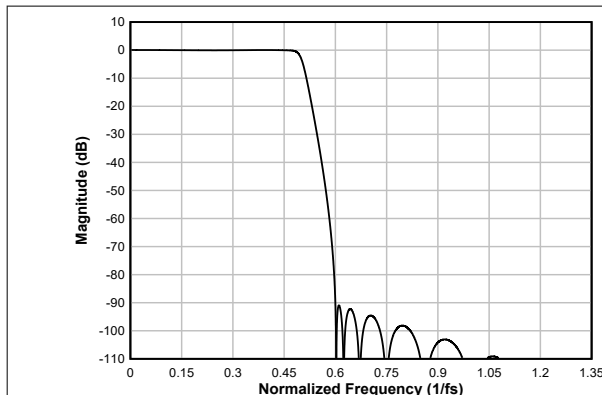
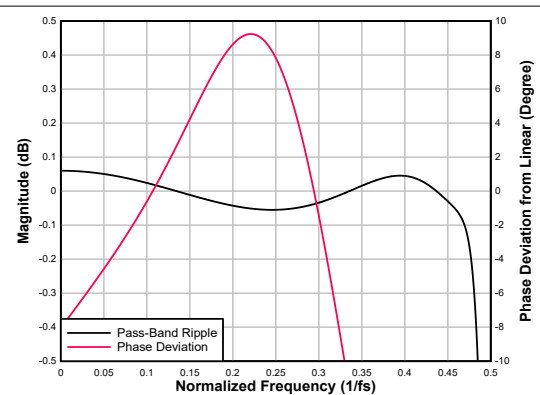
Figure 7-35 shows the magnitude response and Figure 7-36 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 96kHz or 88.2kHz. Table 7-22 lists its specifications.

**Figure 7-35. Low-latency Decimation Filter Magnitude Response****Figure 7-36. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation****Table 7-22. Low-latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS   | MIN    | TYP | MAX   | UNIT    |
|------------------------|---|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.456 \times f_S$              | -0.02  |     | 0.03  | dB      |
| Stop-band attenuation  | Frequency range is $0.599 \times f_S$ to $4 \times f_S$ | 85.6   |     |       |         |
|                        | Frequency range is $4 \times f_S$ onwards               | 95.7   |     |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$              |        | 6.6 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$              | -0.086 |     | 0.022 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.376 \times f_S$              | -0.25  |     | 0.022 | Degrees |

**7.3.7.2.2.5 Sampling Rate: 192kHz or 176.4kHz**

Figure 7-37 shows the magnitude response and Figure 7-38 shows the pass-band ripple and phase deviation for this decimation filter with a sampling rate of 192kHz or 176.4kHz. Table 7-23 lists its specifications.

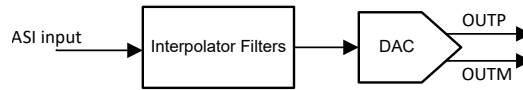
**Figure 7-37. Low-latency Decimation Filter Magnitude Response****Figure 7-38. Low-latency Decimation Filter Pass-Band Ripple and Phase Deviation**

**Table 7-23. Low-latency Decimation Filter Specifications**

| PARAMETER              | TEST CONDITIONS  | MIN    | TYP | MAX   | UNIT    |
|------------------------|--|--------|-----|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.456 \times f_S$                 | -0.06  |     | 0.06  | dB      |
| Stop-band attenuation  | Frequency range is $0.571 \times f_S$ to $1.35 \times f_S$ | 90.5   |     |       | dB      |
|                        | Frequency range is $1 \times f_S$ onwards                  | 86.9   |     |       |         |
| Group delay or latency | Frequency range is 0 to $0.327 \times f_S$                 |        | 6.8 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.327 \times f_S$                 | -0.296 |     | 0.829 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.327 \times f_S$                 | -9.24  |     | 9.24  | Degrees |

### 7.3.8 DAC Signal-Chain

Figure 7-39 shows the key components of the playback signal chain.



**Figure 7-39. DAC Signal-Chain Processing Flowchart**

The DAC signal chain offers a highly flexible low-noise playback path for low-noise and high-fidelity audio applications. This low-noise and low-distortion, multi-bit, delta-sigma DAC enables the TAC5142 to achieve a high dynamic range in very low power. Moreover, the DAC architecture has inherent anti-alias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band. The TAC5142 also integrates a high-performance multi-stage digital interpolation filter that sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

### 7.3.8.1 Digital Interpolation Filters

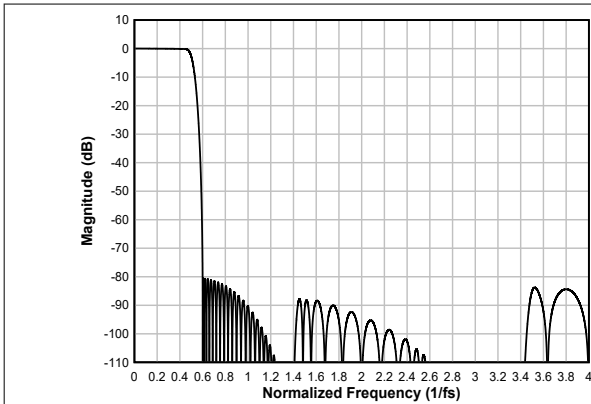
The device playback channel includes a high dynamic range and a built-in digital interpolation filter to process the input data stream to generate a digital data stream for a multibit delta-sigma ( $\Delta\Sigma$ ) modulator. The interpolation filters in the device can be selected to linear phase or low-latency filters based on the state of the MD2 and MD1 pins according to [Table 7-3](#). This makes them suitable for a wide variety of audio applications. The following section describes the filter response for different sample rates.

#### 7.3.8.1.1 Linear-phase filters

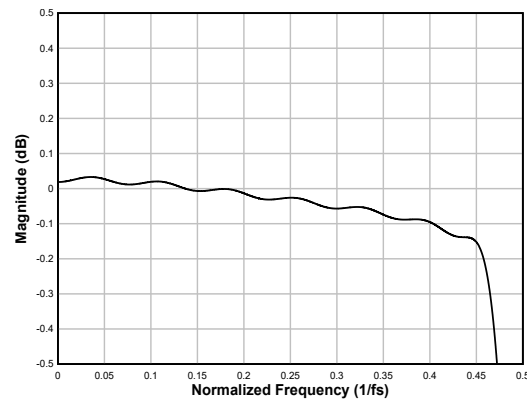
The linear-phase interpolation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

##### 7.3.8.1.1.1 Sampling Rate: 8kHz or 7.35kHz

[Figure 7-40](#) and [Figure 7-41](#) respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 8kHz or 7.35kHz, and [Table 7-24](#) lists its specifications.



**Figure 7-40. Linear-phase Interpolation Filter Magnitude Response**



**Figure 7-41. Linear-phase Interpolation Filter Pass-Band Ripple**

**Table 7-24. Linear-phase Interpolation Filter Specifications**

| PARAMETER              | TEST CONDITIONS   | MIN   | TYP | MAX  | UNIT    |
|------------------------|---|-------|-----|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_s$              | -0.17 |     | 0.03 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_s$ to $4 \times f_s$   | 80.4  |     |      | dB      |
|                        | Frequency range is $4 \times f_s$ to $7.431 \times f_s$ | 86.9  |     |      |         |
| Group delay or latency | Frequency range is 0 to $0.455 \times f_s$              |       | 16  |      | $1/f_s$ |

7.3.8.1.1.2 Sampling Rate: 16kHz or 14.7kHz

Figure 7-42 and Figure 7-43 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 16kHz or 14.7kHz, and Table 7-25 lists its specifications.

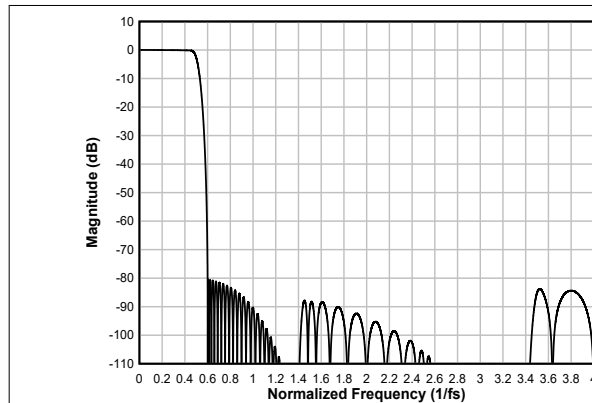


Figure 7-42. Linear-phase Interpolation Filter Magnitude Response

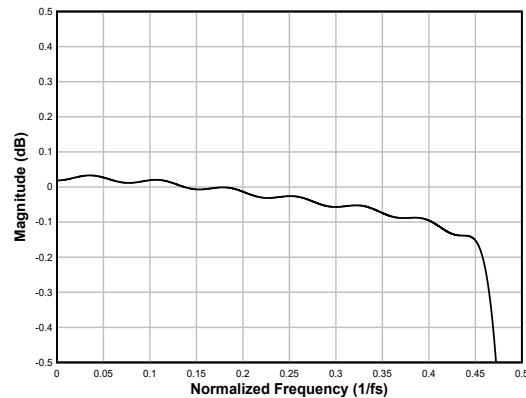


Figure 7-43. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-25. Linear-phase Interpolation Filter Specifications

| PARAMETER              | TEST CONDITIONS   | MIN   | TYP | MAX  | UNIT    |
|------------------------|---|-------|-----|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_s$              | -0.17 |     | 0.03 | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_s$ to $4 \times f_s$   | 80.4  |     |      | dB      |
|                        | Frequency range is $4 \times f_s$ to $7.431 \times f_s$ | 86.9  |     |      |         |
| Group delay or latency | Frequency range is 0 to $0.455 \times f_s$              |       | 16  |      | $1/f_s$ |

7.3.8.1.1.3 Sampling Rate: 24kHz or 22.05kHz

Figure 7-44 and Figure 7-45 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 24kHz or 22.05kHz, and Table 7-26 lists its specifications.

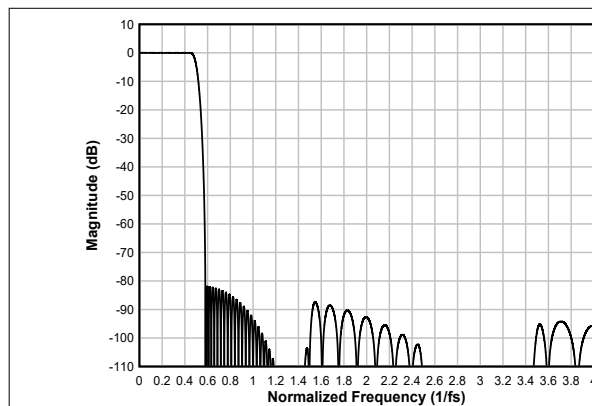


Figure 7-44. Linear-phase Interpolation Filter Magnitude Response

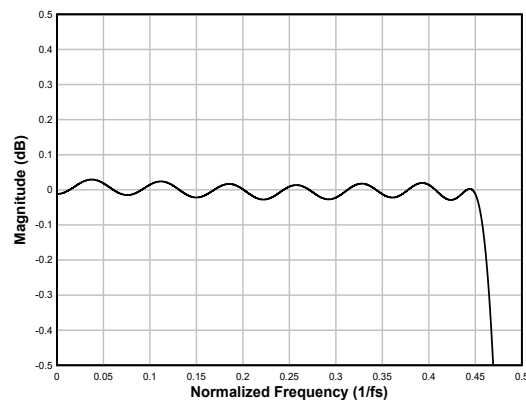


Figure 7-45. Linear-phase Interpolation Filter Pass-Band Ripple

Table 7-26. Linear-phase Interpolation Filter Specifications

| PARAMETER             | TEST CONDITIONS  | MIN   | TYP | MAX  | UNIT |
|-----------------------|--|-------|-----|------|------|
| Pass-band ripple      | Frequency range is 0 to $0.455 \times f_s$             | -0.05 |     | 0.03 | dB   |
| Stop-band attenuation | Frequency range is $0.58 \times f_s$ to $4 \times f_s$ | 81.9  |     |      | dB   |
|                       | Frequency range is $4 \times f_s$ to $8 \times f_s$    | 87.7  |     |      |      |

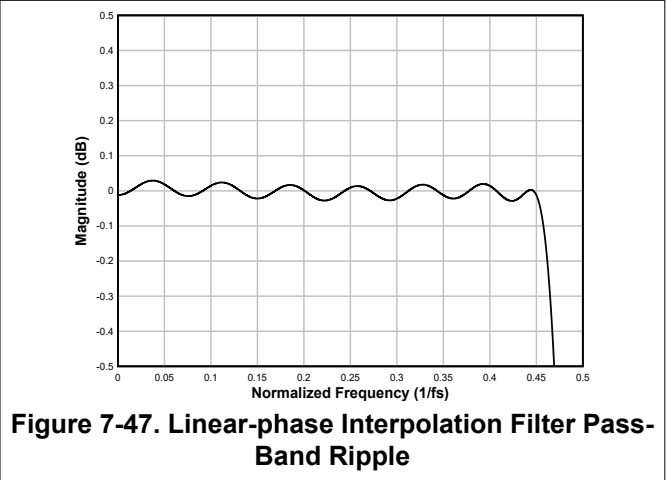
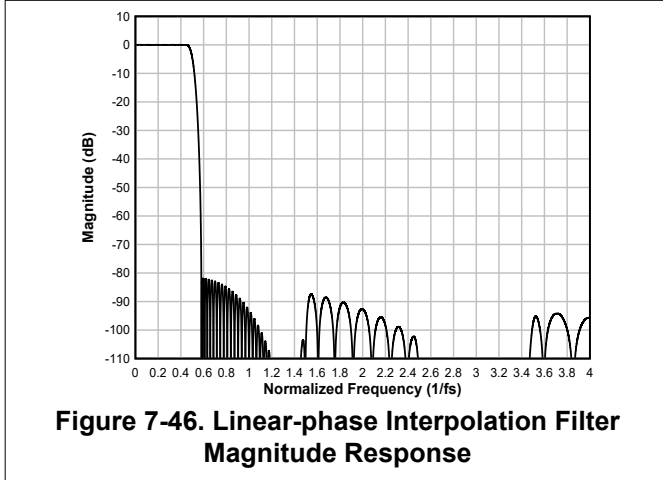


**Table 7-26. Linear-phase Interpolation Filter Specifications (continued)**

| PARAMETER              | TEST CONDITIONS                            | MIN | TYP  | MAX | UNIT    |
|------------------------|--|-----|------|-----|---------|
| Group delay or latency | Frequency range is 0 to $0.455 \times f_S$ |     | 17.6 |     | $1/f_S$ |

**7.3.8.1.1.4 Sampling Rate: 32kHz or 29.4kHz**

Figure 7-46 and Figure 7-47 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 32kHz or 29.4kHz, and Table 7-27 lists its specifications.

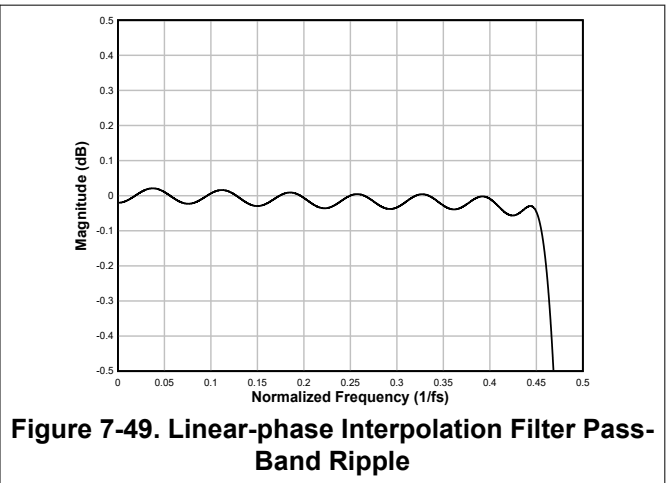
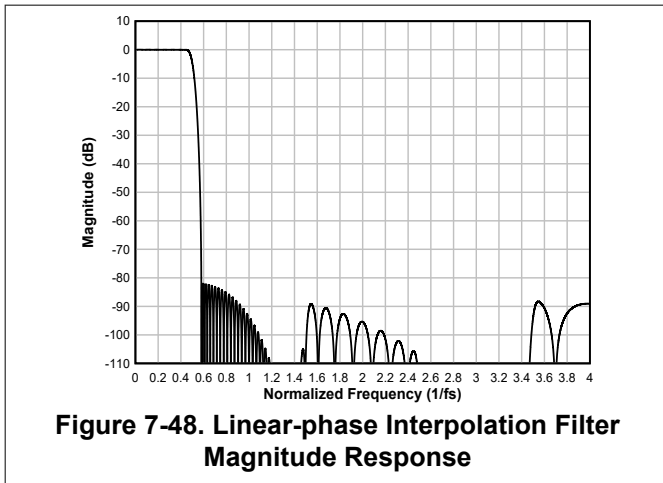


**Table 7-27. Linear-phase Interpolation Filter Specifications**

| PARAMETER              | TEST CONDITIONS  | MIN   | TYP  | MAX  | UNIT    |
|------------------------|--|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_S$             | -0.05 |      | 0.03 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_S$ to $4 \times f_S$ | 81.9  |      |      |         |
|                        | Frequency range is $4 \times f_S$ to $8 \times f_S$    | 87.6  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.455 \times f_S$             |       | 17.6 |      | $1/f_S$ |

**7.3.8.1.1.5 Sampling Rate: 48kHz or 44.1kHz**

Figure 7-48 and Figure 7-49 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 48kHz or 44.1kHz, and Table 7-28 lists its specifications.

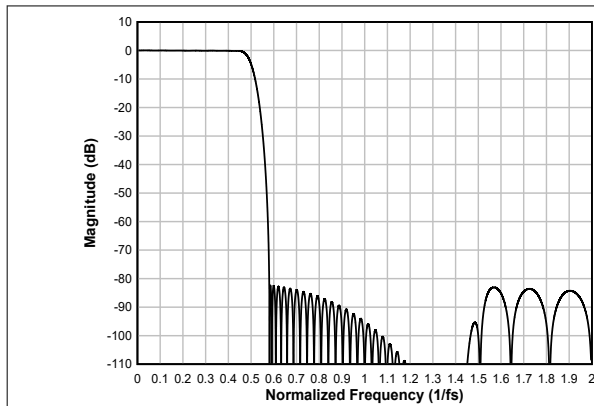
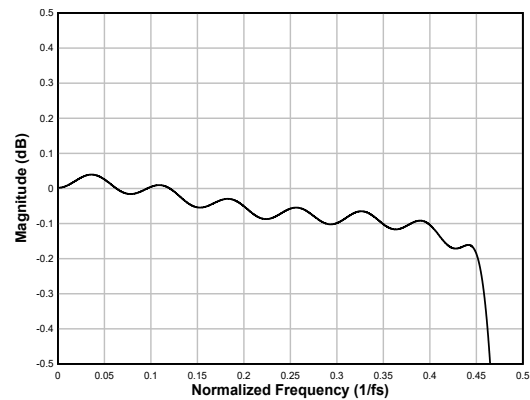


**Table 7-28. Linear-phase Interpolation Filter Specifications**

| PARAMETER              | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT    |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_S$              | -0.09 |      | 0.02 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_S$ to $4 \times f_S$  | 82    |      |      | dB      |
|                        | Frequency range is $4 \times f_S$ to $7.423 \times f_S$ | 89.1  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.455 \times f_S$              |       | 17.3 |      | $1/f_S$ |

**7.3.8.1.1.6 Sampling Rate: 96kHz or 88.2kHz**

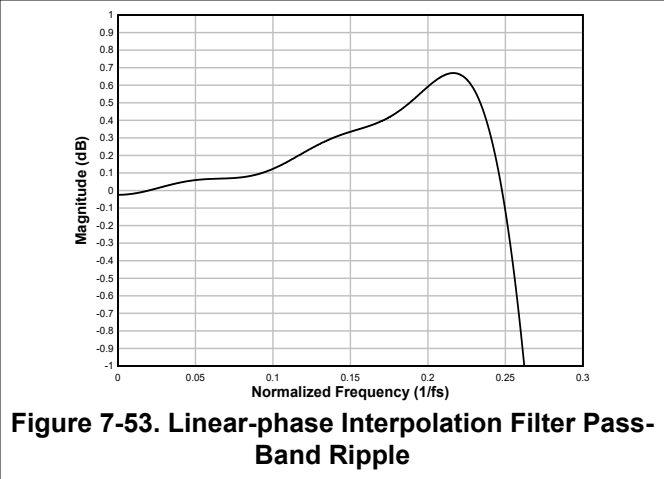
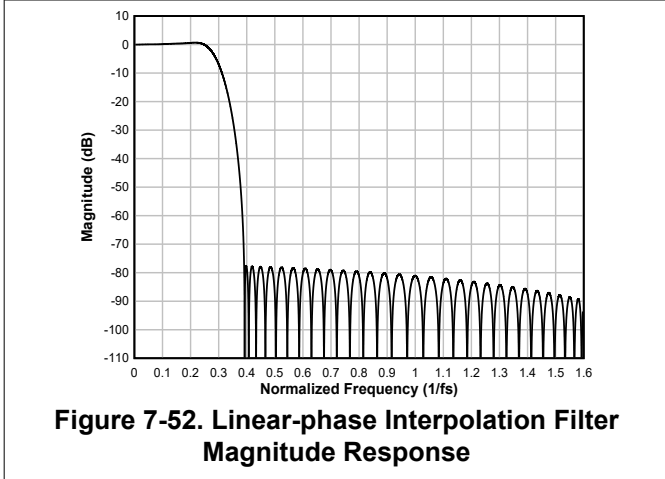
Figure 7-50 and Figure 7-51 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 96kHz or 88.2kHz, and Table 7-29 lists its specifications.

**Figure 7-50. Linear-phase Interpolation Filter Magnitude Response****Figure 7-51. Linear-phase Interpolation Filter Pass-Band Ripple****Table 7-29. Linear-phase Interpolation Filter Specifications**

| PARAMETER              | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT    |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_S$              | -0.23 |      | 0.04 | dB      |
| Stop-band attenuation  | Frequency range is $0.58 \times f_S$ to $2 \times f_S$  | 82.4  |      |      | dB      |
|                        | Frequency range is $2 \times f_S$ to $3.422 \times f_S$ | 85.1  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.455 \times f_S$              |       | 16.7 |      | $1/f_S$ |

**7.3.8.1.1.7 Sampling Rate: 192kHz or 176.4kHz**

Figure 7-52 and Figure 7-53 respectively show the magnitude response and the pass-band ripple for this interpolation filter with a sampling rate of 192kHz or 176.4kHz, and Table 7-30 lists its specifications.



**Table 7-30. Linear-phase Interpolation Filter Specifications**

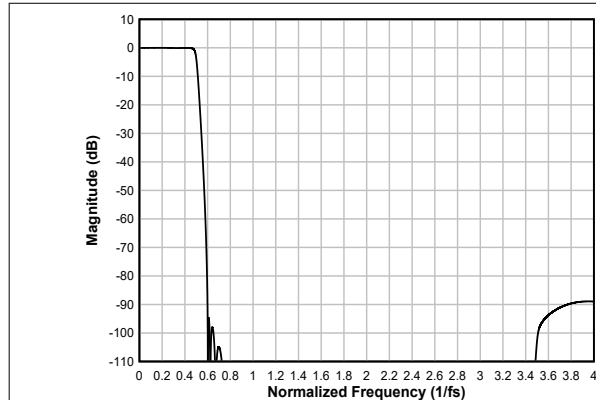
| PARAMETER              | TEST CONDITIONS   | MIN   | TYP  | MAX  | UNIT    |
|------------------------|---|-------|------|------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.258 \times f_S$              | -0.67 |      | 0.67 | dB      |
| Stop-band attenuation  | Frequency range is $0.391 \times f_S$ to $1 \times f_S$ | 77.7  |      |      |         |
|                        | Frequency range is $1 \times f_S$ to $1.612 \times f_S$ | 81.1  |      |      |         |
| Group delay or latency | Frequency range is 0 to $0.258 \times f_S$              |       | 10.7 |      | $1/f_S$ |

### 7.3.8.1.2 Low-latency Filters

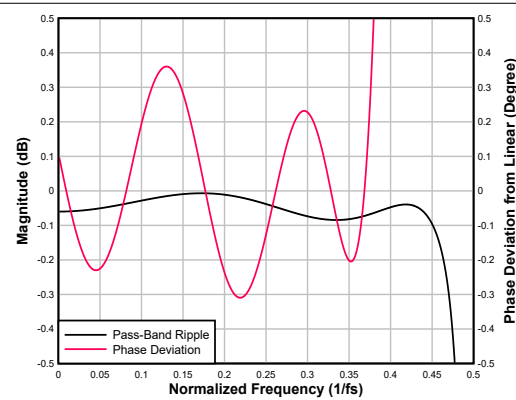
For applications where low latency with minimal phase deviation (within the audio band) is critical, the low-latency interpolation filters on the TAC5142 can be used. The device supports these filters with a group delay of approximately seven samples with an almost linear phase response within the  $0.376 \times f_S$  frequency band. This section provides the filter performance specifications and various plots for all supported output sampling rates for the low-latency filters.

#### 7.3.8.1.2.1 Sampling Rate: 24kHz or 22.05kHz

Figure 7-54 shows the magnitude response and Figure 7-55 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 24kHz or 22.05kHz. Table 7-31 lists its specifications.



**Figure 7-54. Low-latency Interpolation Filter Magnitude Response**



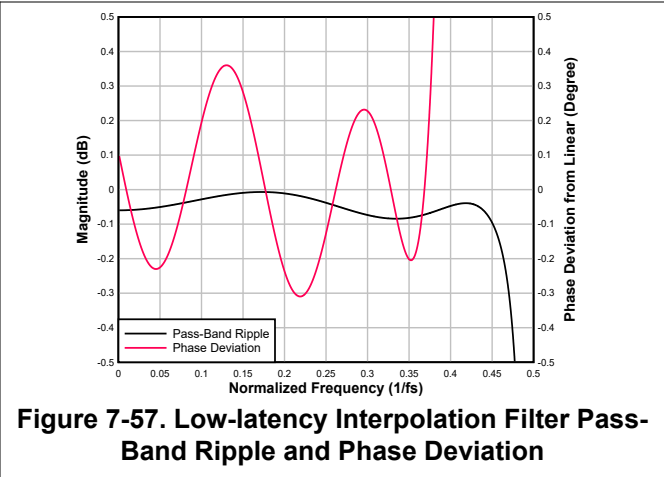
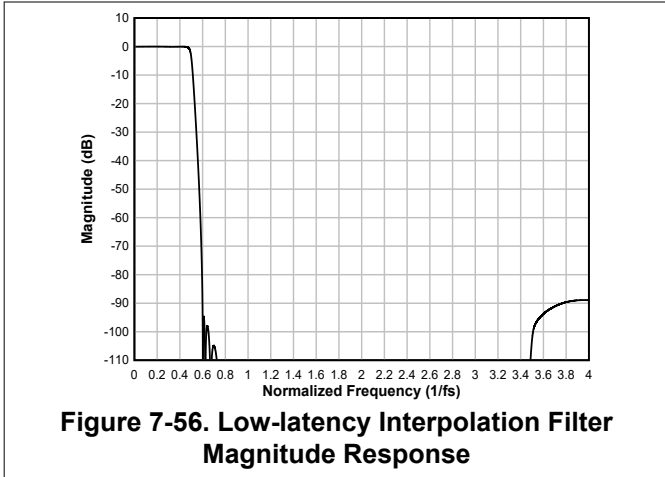
**Figure 7-55. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation**

**Table 7-31. Low-latency Interpolation Filter Specifications**

| PARAMETER              | TEST CONDITIONS   | MIN    | TYP  | MAX   | UNIT    |
|------------------------|---|--------|------|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_S$              | -0.12  |      | -0.01 | dB      |
| Stop-band attenuation  | Frequency range is $0.599 \times f_S$ to $4 \times f_S$ | 88.9   |      |       | dB      |
|                        | Frequency range is $4 \times f_S$ to $7.414 \times f_S$ | 89     |      |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$              |        | 7.19 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$              | -0.088 |      | 0.088 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.376 \times f_S$              | -0.31  |      | 0.36  | Degrees |

#### 7.3.8.1.2.2 Sampling Rate: 32kHz or 29.4kHz

Figure 7-56 shows the magnitude response and Figure 7-57 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 32kHz or 29.4kHz. Table 7-32 lists its specifications.

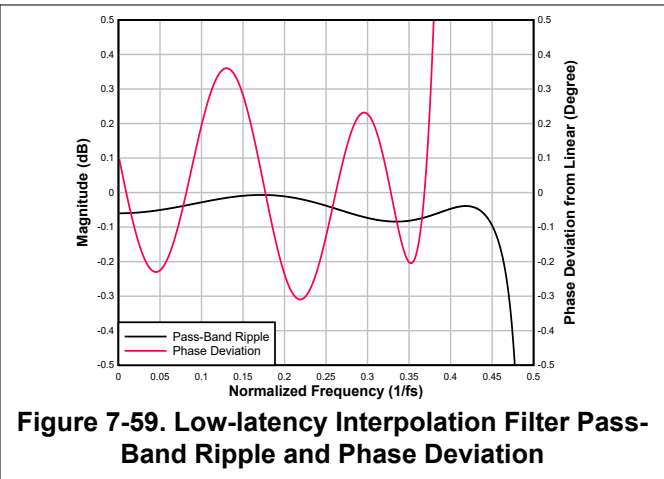
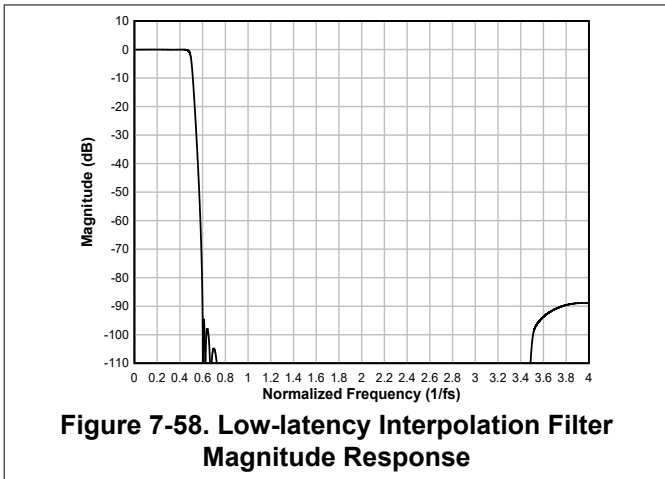


**Table 7-32. Low-latency Interpolation Filter Specifications**

| PARAMETER              | TEST CONDITIONS   | MIN    | TYP  | MAX   | UNIT    |
|------------------------|---|--------|------|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_S$              | -0.12  |      | -0.01 | dB      |
| Stop-band attenuation  | Frequency range is $0.599 \times f_S$ to $4 \times f_S$ | 88.9   |      |       | dB      |
|                        | Frequency range is $4 \times f_S$ to $7.414 \times f_S$ | 89     |      |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$              |        | 7.19 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$              | -0.088 |      | 0.088 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.376 \times f_S$              | -0.31  |      | 0.36  | Degrees |

**7.3.8.1.2.3 Sampling Rate: 48kHz or 44.1kHz**

Figure 7-58 shows the magnitude response and Figure 7-59 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 48kHz or 44.1kHz. Table 7-33 lists its specifications.



**Table 7-33. Low-latency Interpolation Filter Specifications**

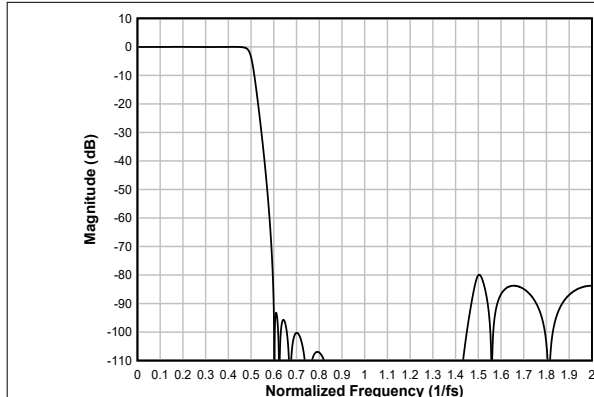
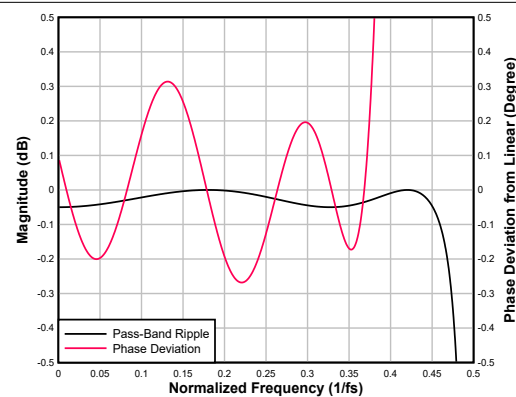
| PARAMETER              | TEST CONDITIONS   | MIN    | TYP  | MAX   | UNIT    |
|------------------------|---|--------|------|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.455 \times f_S$              | -0.12  |      | -0.01 | dB      |
| Stop-band attenuation  | Frequency range is $0.599 \times f_S$ to $4 \times f_S$ | 88.9   |      |       | dB      |
|                        | Frequency range is $4 \times f_S$ to $7.414 \times f_S$ | 89     |      |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$              |        | 7.19 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$              | -0.088 |      | 0.088 | $1/f_S$ |

**Table 7-33. Low-latency Interpolation Filter Specifications (continued)**

| PARAMETER       | TEST CONDITIONS                            | MIN   | TYP | MAX  | UNIT    |
|-----------------|--|-------|-----|------|---------|
| Phase deviation | Frequency range is 0 to $0.376 \times f_S$ | -0.31 |     | 0.36 | Degrees |

**7.3.8.1.2.4 Sampling Rate: 96kHz or 88.2kHz**

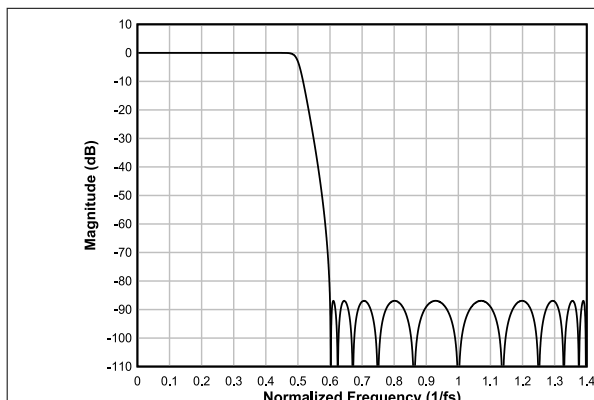
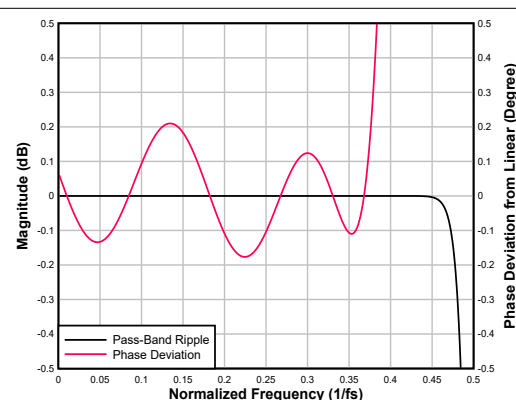
Figure 7-60 shows the magnitude response and Figure 7-61 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 96kHz or 88.2kHz. Table 7-34 lists its specifications.

**Figure 7-60. Low-latency Interpolation Filter Magnitude Response****Figure 7-61. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation****Table 7-34. Low-latency Interpolation Filter Specifications**

| PARAMETER              | TEST CONDITIONS   | MIN    | TYP  | MAX   | UNIT    |
|------------------------|---|--------|------|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.456 \times f_S$              | -0.07  |      | 0     | dB      |
| Stop-band attenuation  | Frequency range is $0.595 \times f_S$ to $2 \times f_S$ | 79.9   |      |       | dB      |
|                        | Frequency range is $2 \times f_S$ to $3.405 \times f_S$ | 79.9   |      |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$              |        | 6.39 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$              | -0.078 |      | 0.022 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.376 \times f_S$              | -0.268 |      | 0.022 | Degrees |

**7.3.8.1.2.5 Sampling Rate: 192kHz or 176.4kHz**

Figure 7-62 shows the magnitude response and Figure 7-63 shows the pass-band ripple and phase deviation for this interpolation filter with a sampling rate of 192kHz or 176.4kHz. Table 7-35 lists its specifications.

**Figure 7-62. Low-latency Interpolation Filter Magnitude Response****Figure 7-63. Low-latency Interpolation Filter Pass-Band Ripple and Phase Deviation**

**Table 7-35. Low-latency Interpolation Filter Specifications**

| PARAMETER              | TEST CONDITIONS   | MIN    | TYP  | MAX   | UNIT    |
|------------------------|---|--------|------|-------|---------|
| Pass-band ripple       | Frequency range is 0 to $0.452 \times f_S$              | -0.005 |      | 0     | dB      |
| Stop-band attenuation  | Frequency range is $0.6 \times f_S$ to $1 \times f_S$   | 86.9   |      |       | dB      |
|                        | Frequency range is $1 \times f_S$ to $1.401 \times f_S$ | 86.9   |      |       |         |
| Group delay or latency | Frequency range is 0 to $0.376 \times f_S$              |        | 5.41 |       | $1/f_S$ |
| Group delay deviation  | Frequency range is 0 to $0.376 \times f_S$              | -0.055 |      | 0.055 | $1/f_S$ |
| Phase deviation        | Frequency range is 0 to $0.376 \times f_S$              | -0.177 |      | 0.21  | Degrees |

## 7.4 Device Functional Modes

### 7.4.1 Active Mode

The device wakes up in active mode when AVDD and IOVDD are available. MD0 pin sets the type of audio serial interface and should be configured along with the supplies. Further, configure all other hardware control mode pins (MD1, MD2, MD3, MD4, and MD5) for the desired mode of operation before enabling the clocks for the device.

In active mode, when the audio clocks are available, the device automatically powers up all the ADC and DAC channels and starts receiving and transmitting data over the audio serial interface as per the configurations. If the clocks are stopped, then the device auto-powers down the ADC and DAC channels.

Stopping the clocks or clock error triggers an interrupt on the GPO pin. This is a latched interrupt that can be cleared by power-cycling the device supplies.

## 8 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

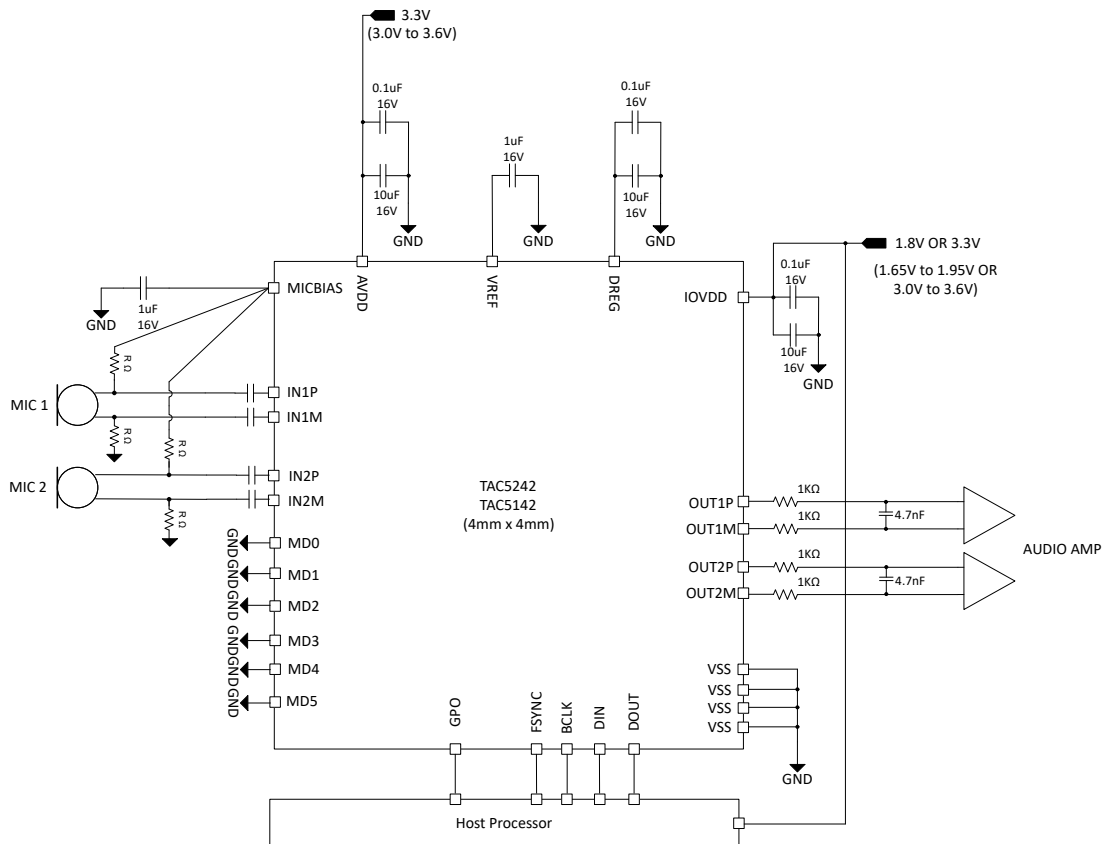
### 8.1 Application Information

The TAC5142 is a pin or hardware-controlled, low-power stereo audio codec that supports sample rates of up to 192kHz on both the record and playback paths. The device can be configured by controlling the Mode pins MD0 to MD5 and can support 1.8V or 3.3V AVDD analog power supply along with flexible digital audio interfaces of I<sup>2</sup>S/TDM/LJ. The ADC has differential and single-ended input capabilities and can support both line-in and microphone inputs for stereo recording with high dynamic range, and the DAC supports various output configurations like 2-channel differential, single-ended or pseudo-differential with external common-mode sense outputs with options for headphone and line-out drive capabilities.

### 8.2 Typical Application

#### 8.2.1 Application

Figure 8-1 shows a typical configuration of the TAC5142 for an application using a 2-channel differential AC-coupled microphone operation and a 2-channel differential line-out operation with a Target Mode I<sup>2</sup>S audio serial data interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.



**Figure 8-1. Stereo Differential AC-Coupled Microphone with Stereo Differential Line-out in Target I<sup>2</sup>S Mode, Block Diagram**



## 8.2.2 Design Requirements

Table 8-1 lists the design parameters for this application.

**Table 8-1. Design Parameters**

| PARAMETER                          | VALUE                    |
|------------------------------------|--------------------------|
| AVDD                               | 3.3V                     |
| IOVDD                              | 1.8V or 3.3V             |
| AVDD supply current consumption    | 27mA, with AVDD = 3.3V   |
| IOVDD supply current consumption   | 0.1mA, with IOVDD = 3.3V |
| Maximum MICBIAS current            | 5mA                      |
| Load on OUT1M, OUT1P, OUT2M, OUT2P | >600 ohms                |

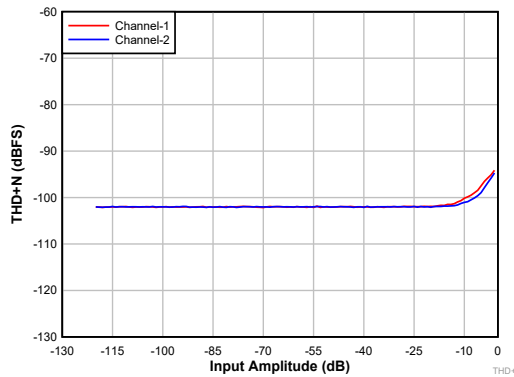
## 8.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAC5142 for this specific application.

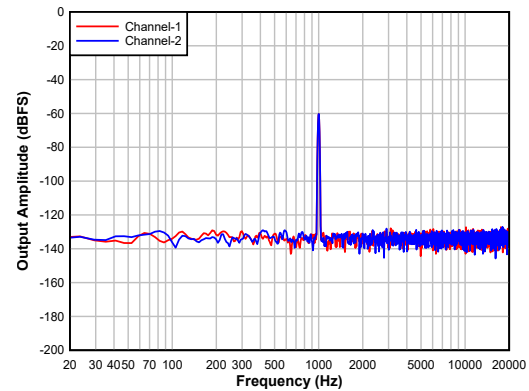
- Audio Serial Interface (ASI) Mode is configured based on the MD0 pin setting which needs to be provided along with the power supplies. Configure MD0 to be either pulled up to AVDD or down to VSS with appropriate resistor values. MD0 is to be grounded for this application case.
- Apply power to the device:
  - Power up the IOVDD and AVDD power supplies.
  - Ensure that the MD0 pin setting is stable as soon as power supplies are up and wait for at least 2ms to allow the device to initialize for this mode of operation.
  - The device now goes into sleep mode (low-power mode <1.5mA)
- Configure the Mode pins MD1 to MD5 as per the system requirements:
  - Pull up to IOVDD or pull down to VSS on MD1 to MD5 pins as per the required configuration. The MD1 to MD5 pins are grounded for this application's use-case.
- Apply the ASI clocks (BCLK and FSYNC) to wake up the device.
- To put the device back in sleep mode, stop the clocks:
  - Wait at least 100ms to allow the device to complete the shutdown sequence.
  - Change the device configurations by changing MD1 to MD5 pin settings as per requirement.
- To change the ASI mode, re-configure the MD0 pin and power-cycle the device.
- Repeat steps 1-6 as required for mode transitions.

## 8.2.4 Application Performance Plots

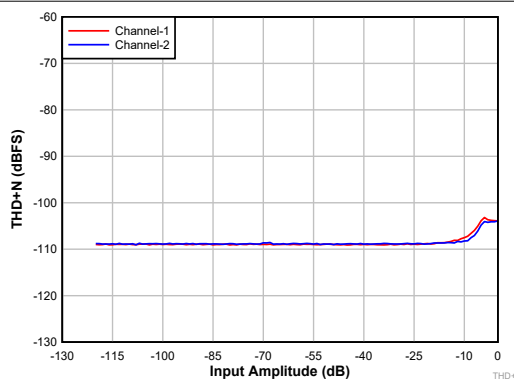
At  $T_A = 25^\circ\text{C}$ , AVDD = 3.3V, IOVDD = 3.3V,  $f_{IN} = 1\text{kHz}$  sinusoidal signal,  $f_S = 48\text{kHz}$ , 32-bit audio data, BCLK =  $256 \times f_S$ , TDM target mode, and linear-phase decimation and interpolation filters, with differential AC-coupled line-input configuration and  $1200\Omega$  line-out load in differential configuration; measured filter-free with an Audio Precision with a 20Hz to 20kHz un-weighted bandwidth, unless otherwise noted



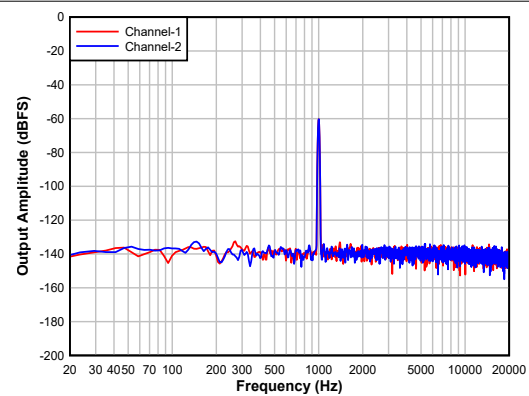
AC-coupled differential line input

**Figure 8-2. ADC THD+N Level vs Input**

AC-coupled differential line input (-60dBFS)

**Figure 8-3. ADC FFT with -60dBFS Input**

Differential output

**Figure 8-4. DAC THD+N Level vs Input**

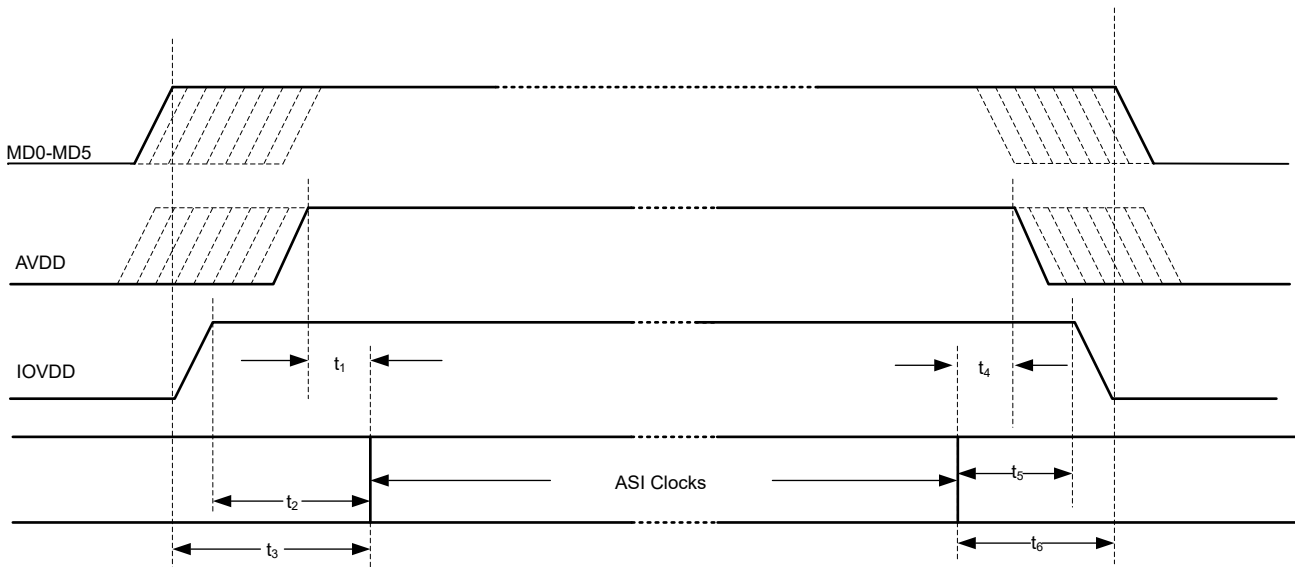
Differential output (-60dBFS input)

**Figure 8-5. DAC FFT with -60dBFS Input**

### 8.3 Power Supply Recommendations

The power supply sequence between the IOVDD and AVDD rails can be applied in any order. MD0 pin should be provided along with the power supplies and should be stable as soon as the supplies are settled to the recommended operating voltage levels. Only initiate the clocks to initialize the device after all the other Mode pins (MD1 to MD5) are also stable.

For the supply power-up requirement,  $t_1$ ,  $t_2$  and  $t_3$  must be at least 2ms to allow the device to initialize the internal settings. See the [Section 7.3.1](#) for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement,  $t_4$ ,  $t_5$  and  $t_6$  must be at least 10ms. This timing (as shown in [Figure 8-6](#)) allows the device to ramp down the volume on the record and playback data, power down the analog and digital blocks, and put the device into a low power mode.



**Figure 8-6. Power-Supply Sequencing Requirement Timing Diagram**

Make sure that the supply ramp rate is slower than  $0.1V/\mu s$  and that the wait time between a power-down and a power-up event is at least 100ms.

The TAC5142 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an internal analog regulator.

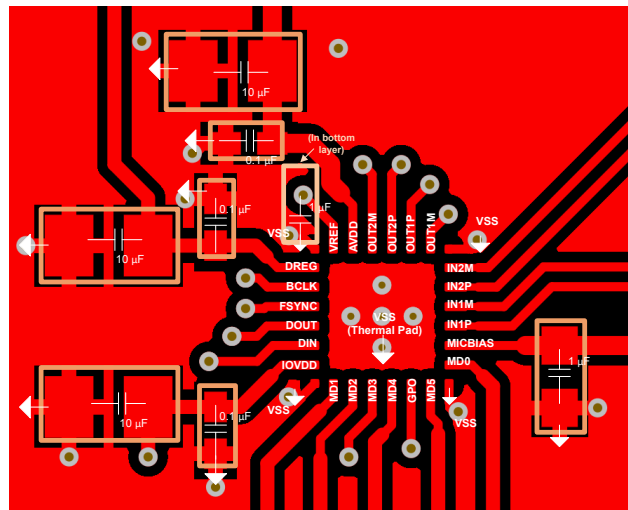
## 8.4 Layout

### 8.4.1 Layout Guidelines

Each system design and printed circuit board (PCB) layout is unique. The layout must be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize the device performance:

- Connect the thermal pad to ground. Use a via pattern to connect the device thermal pad, which is the area directly under the device, to the ground planes. This connection helps dissipate heat from the device.
- Use the same ground between VSS and VSSA to avoid any potential voltage difference between them.
- The decoupling capacitors for the power supplies must be placed close to the device pins.
- Route the analog differential audio signals differentially on the PCB for better noise immunity. Avoid crossing digital and analog signals to prevent undesirable crosstalk.
- Avoid running high-frequency clock and control signals near INxx and OUTxx pins where possible.
- The device internal voltage references must be filtered using external capacitors. Place the filter capacitors near the VREF pin for good performance.
- Directly tap the MICBIAS pin to avoid common impedance when routing the biasing or supply traces for multiple microphones to avoid coupling across microphones.
- Provide a direct connection from the VREF and MICBIAS external capacitor ground terminal to the VSS pin.
- Place the MICBIAS capacitor (with low equivalent series resistance) close to the device with minimal trace impedance.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. Treat the area directly under the device as a central ground area for the device, and all device grounds must be connected directly to that area.

### 8.4.2 Layout Example



**Figure 8-7. Example Layout**

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [TAx5x42EVM-K Hardware Control Evaluation Module User's Guide](#)

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision * (January 2024) to Revision A (November 2024) | Page |
|--|------|
| • Updated device status to production data. ....                     | 1    |

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TAC5142IRGER     | ACTIVE        | VQFN         | RGE             | 24   | 3000        | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | TAC5142                 | <a href="#">Samples</a> |
| XTAC5142IRGER    | ACTIVE        | VQFN         | RGE             | 24   | 3000        | TBD             | Call TI                              | Call TI              | -40 to 125   |                         | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAC5142IRGER | VQFN         | RGE             | 24   | 3000 | 330.0              | 12.4               | 4.25    | 4.25    | 1.15    | 8.0     | 12.0   | Q2            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAC5142IRGER | VQFN         | RGE             | 24   | 3000 | 367.0       | 367.0      | 35.0        |

**RGE 24**

**GENERIC PACKAGE VIEW**

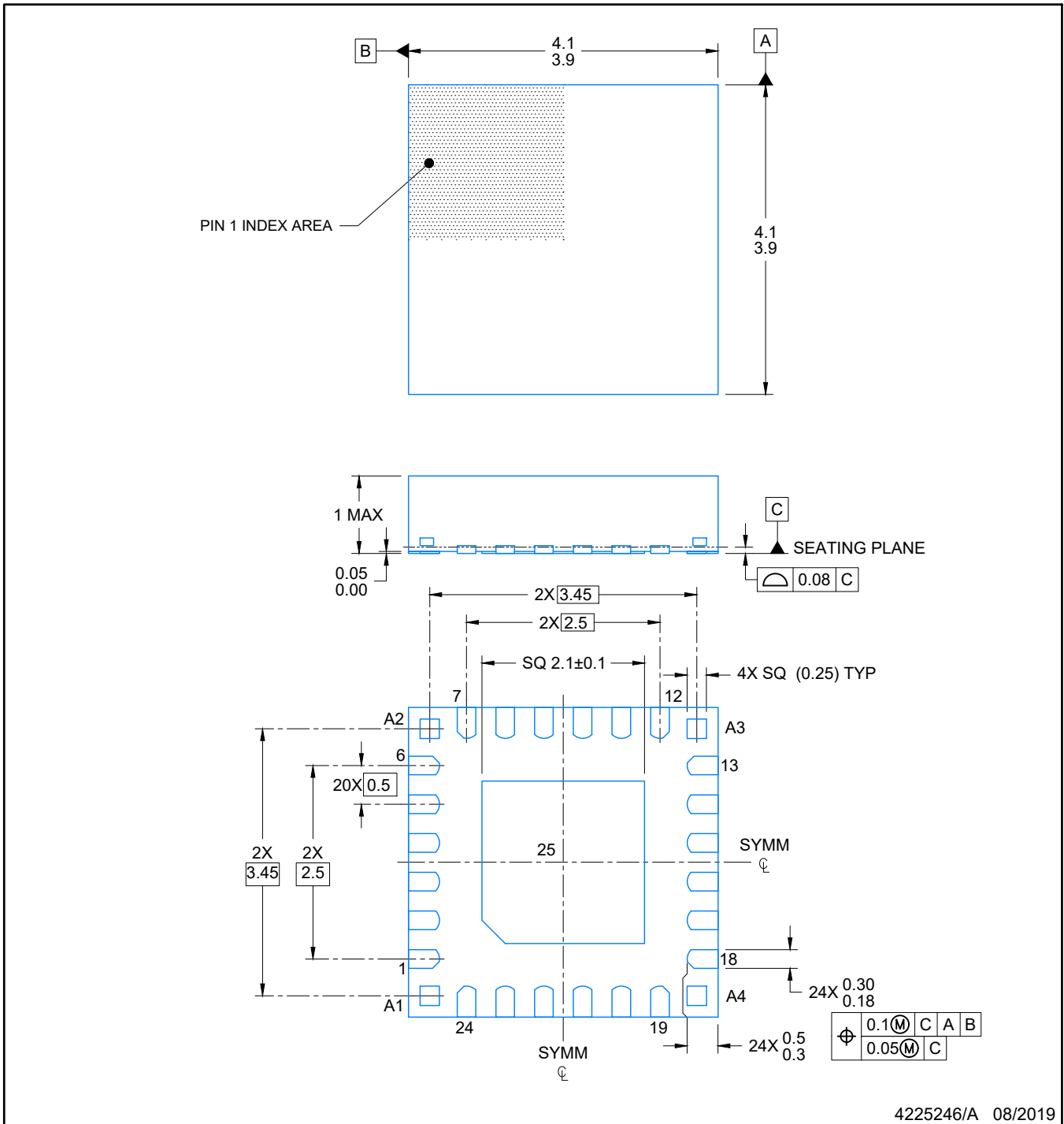
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H



4225246/A 08/2019

NOTES:

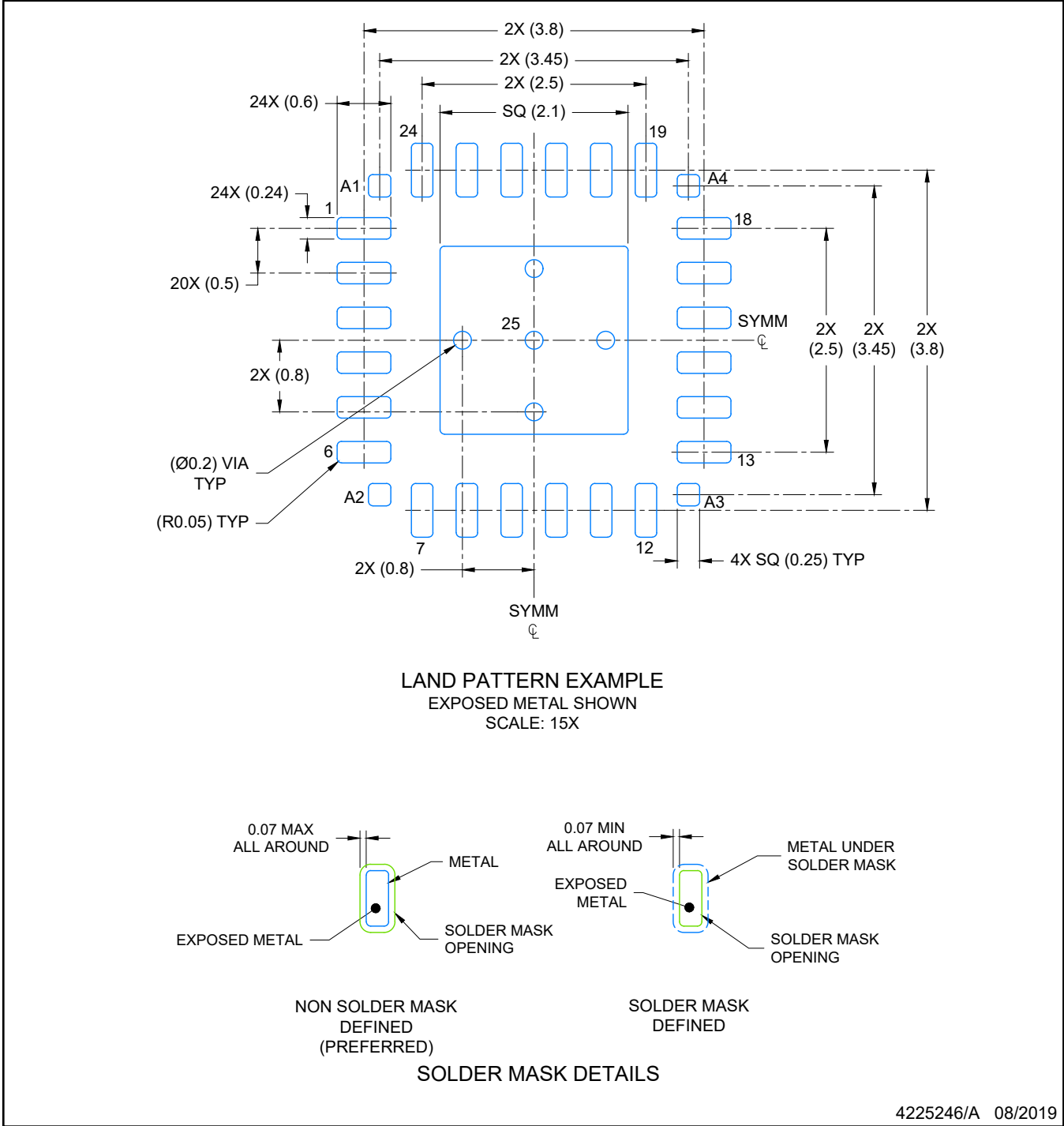
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RGE0024R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



4225246/A 08/2019

NOTES: (continued)

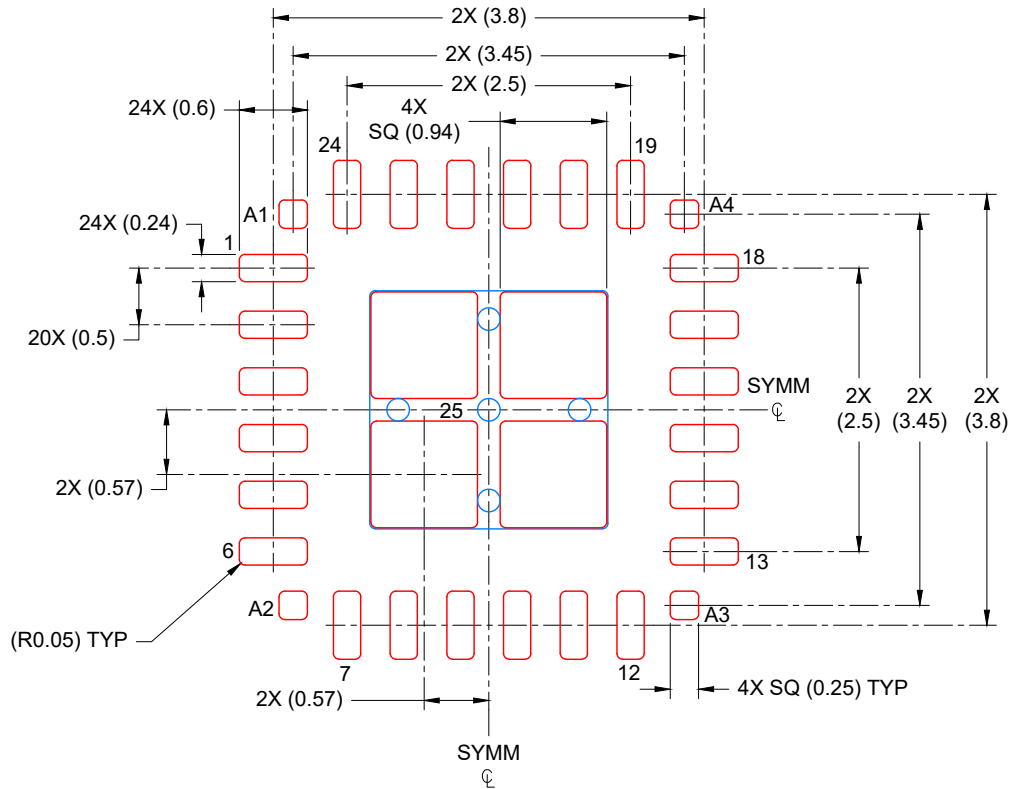
- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

VQFN - 1 mm max height

RGE0024R

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
80% PRINTED COVERAGE BY AREA  
SCALE: 15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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