TEXAS INSTRUMENTS

**TAD5212**
SLASFC1 – DECEMBER 2023

# TAD5212 High-performance stereo audio DAC with 119dB dynamic range

## 1 Features

- DAC performance:
  - DAC to Line Out Dynamic Range: 119 dB
  - DAC to HP Out Dynamic Range: 115 dB
  - THD+N: –95 dB
- Head Phone/Line Out output voltage:
  - Differential, 2-$V_{RMS}$ full-scale
  - Single-ended, 1-$V_{RMS}$ full-scale
- DAC sample Rates ($f_s$) = 8KHz to 768KHz
- Analog Input to Output By-pass
- Battery Protection
- Signal Distortion Limiter
- Thermal Foldback
- Low Latency Filter Selection
- Programmable HPF and Biquad Filters
- I$^2$C & SPI Control Interface
- Audio Serial Interface
  - Format: TDM, I$^2$S or Left Justified
  - Word Length: 16,20,24 or 32 Bits
- Programmable PLL for Flexible Clocking
- Low Power Modes
  - TBD mW for Playback
- Single Supply Operation: 1.8V or 3.3V
- I/O Supply Operation: 1.2V or 1.8V or 3.3V

## 2 Applications

- Telematics control unit
- Automotive head unit
- Digital cockpit processing unit
- Rear seat entertainment
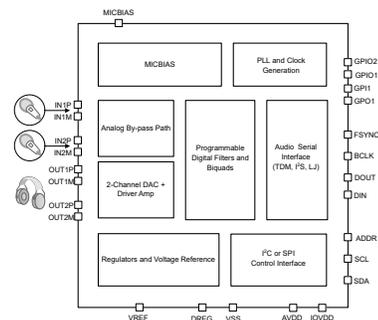- Reconfigurable instrument cluster

## 3 Description

The TAD5212 is a high performance Stereo 2V$_{RMS}$ DAC. The TAD5212 supports both differential and Single Ended input and output. DAC Output can be configured for either Line Out or Head Phone Load. TAD5212 can drive upto TBD mW into a Headphone Load. The TAD5212 integrates programable channel gain, digital volume control, a low-jitter phase-locked loop (PLL), a programmable high-pass filter (HPF), programmable EQ and biquad filters, low-latency filter modes, and allows for sample rates up to 768 kHz. The TAD5212 supports Analog Input to Output Bypass option. Data from Analog-In and Digital-In can be mixed inside the device as well. The TAD5212 supports time-division multiplexing (TDM), I$^2$S, or left-justified (LJ) audio formats, and can be controlled with I$^2$C or SPI. These integrated high-performance features, along with a single supply operation, make TAD5212 an excellent choice for space-constrained audio applications.

**Device Information**

| PART NUMBER | PACKAGE[1] | BODY SIZE (NOM) |
|---|---|---|
| TAD5212 | WQFN(28) | 4mm x 4mm with 0.5mm Pitch |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Block Diagram**

ADVANCE INFORMATION

**ADVANCE INFORMATION**

## Table of Contents

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|------|----------|-------|
| December 2023 | * | Initial Release |

## 5 Pin Configuration and Functions



Notes:-
Not to Scale
**Pinout is subject to changes**
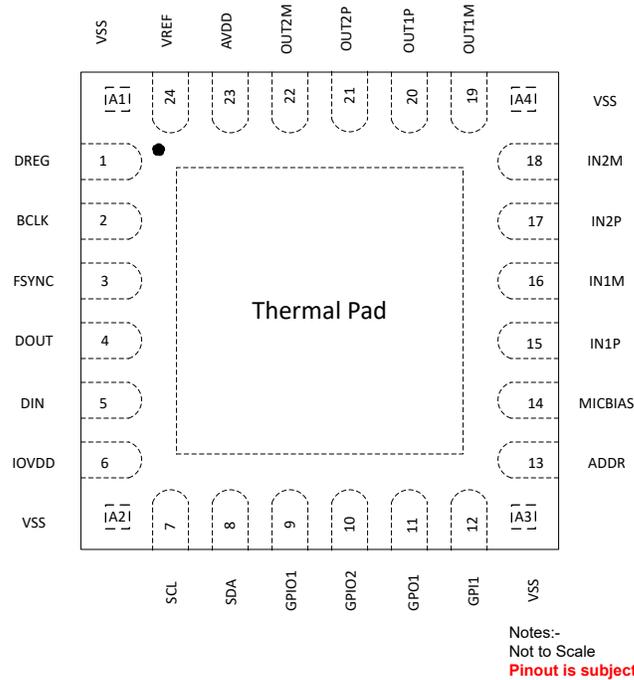
**Figure 5-1. 28-Pin QFN With Exposed Thermal Pad, Top View**

**Table 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| DREG | 1 | Digital Supply | Digital on-chip regulator output voltage for digital supply (1.5 V, nominal) |
| BCLK | 2 | Digital I/O | Audio serial data interface bus bit clock |
| FSYNC | 3 | Digital I/O | Audio serial data interface bus frame synchronization signal |
| DOUT | 4 | Digital I/O | Audio serial data interface bus output |
| DIN | 5 | Digital Input | Audio serial data interface bus input |
| IOVDD | 6 | Digital Supply | Digital I/O power supply (1.8 V or 3.3 V, nominal) |
| VSS | A2 | Ground | Ground Pin. Short directly to board Ground Plane. |
| SCL | 7 | Digital Input | Clock for I$^2$C Control Interface |
| SDA | 8 | Digital Input | Data for I$^2$C Control Interface |
| GPIO1 | 9 | Digital I/O | General-purpose digital input/output 0 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so forth) |
| GPIO2 | 10 | Digital I/O | General-purpose digital input/output 1 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so forth) |
| GPO1 | 11 | Digital Output | General-purpose digital output 1 (multipurpose functions such as audio data output, interrupt, and so forth) |
| GPI1 | 12 | Digital Input | General-purpose digital input 1 (multipurpose functions such as daisy-chain input, PLL input clock source, and so forth) |
| VSS | A3 | Ground | Ground Pin. Short directly to board Ground Plane. |

Product Folder Links: TAD5212

**ADVANCE INFORMATION**

**Table 5-1. Pin Functions (continued)**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| ADDR | 13 | Analog Input | I2C Address |
| MICBIAS | 14 | Analog | MICBIAS Output (Programmable output upto 3V) |
| IN1P | 15 | Analog Input | Analog Input 1P Pin |
| IN1M | 16 | Analog Input | Analog Input 1M Pin |
| IN2P | 17 | Analog Input | Analog Input 2P Pin |
| IN2M | 18 | Analog Input | Analog Input 2M Pin |
| VSS | A4 | Ground | Ground Pin. Short directly to board Ground Plane. |
| OUT1M | 19 | Analog Output | Analog Output 1M Pin |
| OUT1P | 20 | Analog Output | Analog Output 1P Pin |
| OUT2P | 21 | Analog Output | Analog Output 2P Pin |
| OUT2M | 22 | Analog Output | Analog Output 2M Pin |
| AVDD | 23 | Analog Supply | Analog power (3.3 V, nominal) |
| VREF | 24 | Analog | Analog reference voltage filter output |
| VSS | A1 | Ground | Ground Pin. Short directly to board Ground Plane. |

(1)    I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)[1]

|  |  | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | AVDD to AVSS | −0.3 | 3.9 | V |
| Supply voltage | IOVDD to VSS (thermal pad) | −0.3 | 3.9 | V |
| Ground voltage differences | AVSS to VSS (thermal pad) | −0.3 | 0.3 | V |
| Analog input voltage | Analog input pins voltage to AVSS | −0.3 | 5.656 | V |
| Digital input voltage | Digital input pins voltage to VSS (thermal pad) | −0.3 | IOVDD + 0.3 | V |
| Temperature | Functional ambient, $T_A$ | -55 | 125 | °C |
|  | Operating ambient, $T_A$ | −40 | 125 |  |
|  | Junction, $T_J$ | −40 | 150 |  |
|  | Storage, $T_{stg}$ | −65 | 150 |  |

(1)  Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

|  |  |  | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002[1] | ±2000 | V |
| $V_{(ESD)}$ | Electrostatic discharge | Charged-device model (CDM), per AEC Q100-011 | ±500 |  |

(1)  AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

|  |  |  | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **POWER** |  |  |  |  |  |  |
| AVDD[1] | Analog supply voltage to AVSS AVDD-3.3V Operation |  | 3.0 | 3.3 | 3.6 | V |
| AVDD[1] | Analog supply voltage to AVSS - AVDD 1.8V operation |  | 1.65 | 1.8 | 1.95 | V |
| IOVDD | IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation |  | 3.0 | 3.3 | 3.6 | V |
|  | IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation |  | 1.65 | 1.8 | 1.95 |  |
| IOVDD | IO supply voltage to VSS (thermal pad) - IOVDD 1.2-V operation |  | 1.08 | 1.2 | 1.32 | V |
| **INPUTS** |  |  |  |  |  |  |
| INxx | Analog input pins voltage to AVSS for line in bypass path | Analog input pins voltage to AVSS for line in bypass path | 0 |  | 5.6 | V |
| INxx | Analog input pins voltage to AVSS for microphone bypass path |  | 0.1 |  | MICBIAS – 0.1 | V |
|  | Digital input pins voltage to VSS (thermal pad) |  | 0 |  | IOVDD | V |
| ADDR | ADDR pin w.r.t AVSS |  | 0 |  | AVDD | V |
| **TEMPERATURE** |  |  |  |  |  |  |
| $T_A$ | Operating ambient temperature |  | −40 |  | 125 | °C |

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **OTHERS** | | | | | |
| | GPIOx or GPIx (used as CCLK input) clock frequency | | | 36.864[2] | MHz |
| $C_b$ | SCL and SDA bus capacitance for I2C interface supports standard-mode and fast-mode | | | 400 | pF |
| | SCL and SDA bus capacitance for I2C interface supports fast-mode plus | | | 550 | |
| $C_L$ | Digital output load capacitance | | 20 | 50 | pF |

(1)    AVSS and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2 V.
(2)    MCLK input rise time ($V_{IL}$ to $V_{IH}$) and fall time ($V_{IH}$ to $V_{IL}$) must be less than 5 ns. For better audio noise performance, MCLK input  must be used with low jitter.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | TAD5212-Q1 | UNIT |
|---|---|---|---|
| | | RGE (VQFN) | |
| | | 24 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 38.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 26.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 15.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 15.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 13.8 | °C/W |

(1)    For more information about traditional and new thermal metrics, see the spra953 application report.

## 6.5 Electrical Characteristics

at $T_A$ = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, $f_{IN}$ = 1-kHz sinusoidal signal, $f_S$ = 48 kHz, 32-bit audio data, BCLK = 256 × $f_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **DAC Performance for Line Output/Head Phone Playback** | | | | | |
| Full Scale Output Voltage | Differential output between OUTxP and OUTxM, AVDD=3.3V | | 2 | | $V_{RMS}$ |
| | Differential Output between OUTxP and OUTxM, AVDD=1.8V | | 1 | | |
| | Single-ended Output, AVDD=3.3V | | 1 | | |
| | Single-ended Output, AVDD=1.8V | | 0.5 | | |
| | Pseudo Differential Output between OUTxP and OUTxM, AVDD=3.3V | | 1 | | |
| | Pseudo Differential Output between OUTxP and OUTxM, AVDD=1.8V | | 0.5 | | |

Product Folder Links: *TAD5212*

at T$_A$ = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f$_{IN}$ = 1-kHz sinusoidal signal, f$_S$ = 48 kHz, 32-bit audio data, BCLK = 256 × f$_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| SNR | Signal-to-noise ratio, A-weighted[1] [2] | Differential Output, 0dBFS Signal, AVDD=3.3V | | 119 | | dB |
| | | Single Ended Output, 0dBFS Signal, AVDD=3.3V | | 111 | | |
| | | Pseudo Differential Output, 0dBFS Signal, AVDD=3.3V | | 110 | | |
| | | Differential Output, 0dBFS Signal, AVDD=1.8V | | 114 | | |
| | | Single Ended Output, 0dBFS Signal, AVDD=1.8V | | 105 | | |
| | | Pseudo Differential Output, 0dBFS Signal, AVDD=1.8V | | 104 | | |
| | | Differential Output, 0dBFS Signal, AVDD=3.3V, 0dBFS Signal, Power Tune Mode | | 112 | | |
| | | Single Ended Output, 0dBFS Signal, AVDD=3.3V, Power Tune Mode | | 102 | | |
| | | Pseudo Differential Output, 0dBFS Signal, AVDD=3.3V, Power Tune Mode | | 101 | | |
| | | Differential Output, 0dBFS Signal, AVDD=1.8V, Power Tune Mode | | 108 | | |
| | | Single Ended Output, 0dBFS Signal, AVDD=1.8V, Power Tune Mode | | 97 | | |
| | | Pseudo Differential Output, 0dBFS Signal, AVDD=1.8V, Power Tune Mode | | 96 | | |
| DR | Dynamic range, A-weighted[2] | Differential Output, -60dBFS Signal, AVDD=3.3V | | 119 | | dB |
| | | Single Ended Output, -60dBFS Signal, AVDD=3.3V | | 111 | | |
| | | Pseudo Differential Output, -60dBFS Signal, AVDD=3.3V | | 110 | | |
| | | Differential Output, -60dBFS Signal, AVDD=1.8V | | 114 | | |
| | | Single Ended Output, -60dBFS Signal, AVDD=1.8V | | 105 | | |
| | | Pseudo Differential Output, -60dBFS Signal, AVDD=1.8V | | 104 | | |
| | | Differential Output, -60dBFS Signal, AVDD=3.3V, 0dBFS Signal, Power Tune Mode | | 112 | | |
| | | Single Ended Output, -60dBFS Signal, AVDD=3.3V, Power Tune Mode | | 102 | | |
| | | Pseudo Differential Output, -60dBFS Signal, AVDD=3.3V, Power Tune Mode | | 101 | | |
| | | Differential Output, -60dBFS Signal, AVDD=1.8V, Power Tune Mode | | 108 | | |
| | | Single Ended Output, -60dBFS Signal, AVDD=1.8V, Power Tune Mode | | 97 | | |
| | | Pseudo Differential Output, -60dBFS Signal, AVDD=1.8V, Power Tune Mode | | 96 | | |
| THD+N | Total harmonic distortion[2] | | | -95 | | dB |
| | Head Phone Load Range | | | 16 | | Ω |
| | Line Out Load Range | | 600 | | | Ω |
| | Channel gain control range | Programmable 1-dB steps | –6 | | 12 | dB |
| **Analog Bypass to Line Out/Head Phone Amplifier** | | | | | | |

**ADVANCE INFORMATION**

*Submit Document Feedback*     7

at T$_A$ = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, f$_{IN}$ = 1-kHz sinusoidal signal, f$_S$ = 48 kHz, 32-bit audio data, BCLK = 256 × f$_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| | Input impedance | Differential input, between INxP and INxM | | | 8.8 | | kΩ |
| | | Single-ended input, between INxP and INxM | | | 4.4 | | |
| | | Differential input, between INxP and INxM, 40k Mode | | | 40k | | |
| | | Single-ended input, between INxP and INxM, 40k Mode | | | 20k | | |
| | Single Ended Full Scale Output | AVDD=3.3V | AVDD=3.3V | | 1 | | Vrms |
| | Differential Full Scale Output | AVDD=3.3V | | | 2 | | Vrms |
| | | AVDD=1.8V | | | 1 | | Vrms |
| | Gain Error | | | | 0.1 | | dB |
| | Noise, A-Weighted | Idle Channel, AC Coupled Input Shorted to Ground, Fully Differential output | | | 4.5 | | µV$_{RMS}$ |
| | Noise, A-Weighted | Idle Channel, AC Coupled Input Shorted to Ground, Single Ended output | | | 6.3 | | µV$_{RMS}$ |
| SNR | Signal-to-noise ratio, A-weighted[1] [2] | Idle Channel, AC Coupled Input Shorted to Ground, Fully Differential output, AVDD=3.3V | | | 113 | | dB |
| SNR | Signal-to-noise ratio, A-weighted[1] [2] | Idle Channel, AC Coupled Input Shorted to Ground, Single Ended output, AVDD=3.3V | | | 104 | | dB |
| THD+N | Total harmonic distortion[2] | IN1 differential AC-coupled input selected and -1-dB full-scale AC signal input, 0-dB channel gain | | | | | dB |
| **DAC Channel OTHER PARAMETERS** | | | | | | | |
| | Output Offset | 0 Input, Fully Differential Output | | | 0.2 | | mV |
| | Output Offset | 0 Input, Pseudo Differential Output | | | 0.4 | | mV |
| | Output Common Mode | Common Mode Level for OUTxP and OUTxM AVDD=1.8V (Register Configurable) | | | 0.9 | | V |
| | Output Common Mode | Common Mode Level for OUTxP and OUTxM AVDD=3.3V (Register Configurable) | | | 1.66 | | V |
| | Common Mode Error | DC Error in Common Mode Voltage | | | ±10 | | mV |
| | Digital volume control range | Programmable 0.5-dB steps | | −120 | | 42 | dB |
| | Output Signal Bandwidth | Upto 192KSPS FS Rate | | | 0.46 | | FS |
| | | >192KSPS | | | 100 | | kHz |
| | Input data sample rate | Programmable | | 3.675 | | 768 | kHz |
| | Input data sample word length | Programmable | | 16 | | 32 | Bits |
| | Digital high-pass filter cutoff frequency | First-order IIR filter with programmable coefficients, −3-dB point (default setting) | | | 2 | | Hz |
| | Interchannel isolation | | | | −134 | | dB |
| | Interchannel gain mismatch | | | | 0.1 | | dB |
| | Interchannel phase mismatch | 1-kHz sinusoidal signal | | | 0.01 | | Degrees |
| PSRR | Power-supply rejection ratio | 100-mV$_{PP}$, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain | | | 100 | | dB |
| | Mute Attenuation | | | | −130 | | dB |
| P$_{out}$ | Output Power Delivery | Single ended/Pseudo Differential R$_L$=16 Ohms, THD+N<1% | | | 62.5 | | mW |
| **MICROPHONE BIAS** | | | | | | | |

at $T_A$ = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, $f_{IN}$ = 1-kHz sinusoidal signal, $f_S$ = 48 kHz, 32-bit audio data, BCLK = 256 × $f_S$, TDM target mode and PLL on (unless otherwise noted)

| | PARAMETER | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | MICBIAS noise | BW = 20 Hz to 20 kHz, A-weighted, 1-µF capacitor between MICBIAS and AVSS | | 2 | | µV$_{RMS}$ |
| | MICBIAS voltage | Bypass to AVDD | | AVDD | | V |
| | MICBIAS voltage | AVDD=1.8V | | 1.375 | | V |
| | MICBIAS voltage | AVDD=3.3V | | 2.75 | | V |
| **DIGITAL I/O** | | | | | | |
| $V_{IL(SHDNZ)}$ | Low-level digital input logic voltage threshold | SHDNZ pin | −0.3 | | 0.25 × IOVDD | V |
| $V_{IH(SHDNZ)}$ | High-level digital input logic voltage threshold | SHDNZ pin | 0.75 × IOVDD | | IOVDD + 0.3 | V |
| $V_{IL}$ | Low-level digital input logic voltage threshold | All digital pins except SDA and SCL, IOVDD 1.8-V operation | −0.3 | | 0.35 × IOVDD | V |
| | | All digital pins except SDA and SCL, IOVDD 3.3-V operation | −0.3 | | 0.8 | |
| $V_{IH}$ | High-level digital input logic voltage threshold | All digital pins except SDA and SCL, IOVDD 1.8-V operation | 0.65 × IOVDD | | IOVDD + 0.3 | V |
| | | All digital pins except SDA and SCL, IOVDD 3.3-V operation | 2 | | IOVDD + 0.3 | |
| $V_{OL}$ | Low-level digital output voltage | All digital pins except SDA and SCL, $I_{OL}$ = −2 mA, IOVDD 1.8-V operation | | | 0.45 | V |
| | | All digital pins except SDA and SCL, $I_{OL}$ = −2 mA, IOVDD 3.3-V operation | | | 0.4 | |
| $V_{OH}$ | High-level digital output voltage | All digital pins except SDA and SCL, $I_{OH}$ = 2 mA, IOVDD 1.8-V operation | IOVDD − 0.45 | | | V |
| | | All digital pins except SDA and SCL, $I_{OH}$ = 2 mA, IOVDD 3.3-V operation | 2.4 | | | |
| $V_{IL(I2C)}$ | Low-level digital input logic voltage threshold | SDA and SCL | −0.5 | | 0.3 × IOVDD | V |
| $V_{IH(I2C)}$ | High-level digital input logic voltage threshold | SDA and SCL | 0.7 × IOVDD | | IOVDD + 0.5 | V |
| $V_{OL1(I2C)}$ | Low-level digital output voltage | SDA, $I_{OL(I2C)}$ = −3 mA, IOVDD > 2 V | | | 0.4 | V |
| $V_{OL2(I2C)}$ | Low-level digital output voltage | SDA, $I_{OL(I2C)}$ = −2 mA, IOVDD ≤ 2 V | | | 0.2 x IOVDD | V |
| $I_{OL(I2C)}$ | Low-level digital output current | SDA, $V_{OL(I2C)}$ = 0.4 V, standard-mode or fast-mode | 3 | | | mA |
| | | SDA, $V_{OL(I2C)}$ = 0.4 V, fast-mode plus | 20 | | | |
| $I_{IL}$ | Input logic-low leakage for digital inputs | All digital pins, input = 0 V | −5 | 0.1 | 5 | µA |
| $I_{IH}$ | Input logic-high leakage for digital inputs | All digital pins, input = IOVDD | −5 | 0.1 | 5 | µA |
| $C_{IN}$ | Input capacitance for digital inputs | All digital pins | | 5 | | pF |
| $R_{PD}$ | Pulldown resistance for digital I/O pins when asserted on | | | 20 | | kΩ |
| **TYPICAL SUPPLY CURRENT CONSUMPTION** | | | | | | |
| $I_{AVDD}$ | Current consumption in sleep mode (software shutdown mode) | All device external clocks stopped | | TBD | | µA |
| $I_{IOVDD}$ | | | | 1 | | |

**ADVANCE INFORMATION**

Product Folder Links: TAD5212

at $T_A$ = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, $f_{IN}$ = 1-kHz sinusoidal signal, $f_S$ = 48 kHz, 32-bit audio data, BCLK = 256 × $f_S$, TDM target mode and PLL on (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{AVDD}$ | Current consumption with DAC to HP 2-channel operation at $f_S$ 16-kHz, MICBIAS off, PLL on, BCLK = 512 × $f_S$ | | | TBD | | mA |
| $I_{IOVDD}$ | | | | 0.2 | | |
| $I_{AVDD}$ | Current consumption with DAC to HP 2-channel operation at $f_S$ 48-kHz, MICBIAS off, PLL off, BCLK = 512 × $f_S$ | | | TBD | | mA |
| $I_{IOVDD}$ | | | | TBD | | |

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.

(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter can result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

## 6.6 Timing Requirements: I²C Interface

at $T_A$ = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see TBD for timing diagram

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **STANDARD-MODE** | | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | | 100 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4 | | | µs |
| $t_{LOW}$ | Low period of the SCL clock | 4.7 | | | µs |
| $t_{HIGH}$ | High period of the SCL clock | 4 | | | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | 4.7 | | | µs |
| $t_{HD;DAT}$ | Data hold time | 0 | | 3.45 | µs |
| $t_{SU;DAT}$ | Data setup time | 250 | | | ns |
| $t_r$ | SDA and SCL rise time | | | 1000 | ns |
| $t_f$ | SDA and SCL fall time | | | 300 | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | 4 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 4.7 | | | µs |
| **FAST-MODE** | | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | | 400 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.6 | | | µs |
| $t_{LOW}$ | Low period of the SCL clock | 1.3 | | | µs |
| $t_{HIGH}$ | High period of the SCL clock | 0.6 | | | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | 0.6 | | | µs |
| $t_{HD;DAT}$ | Data hold time | 0 | | 0.9 | µs |
| $t_{SU;DAT}$ | Data setup time | 100 | | | ns |
| $t_r$ | SDA and SCL rise time | 20 | | 300 | ns |
| $t_f$ | SDA and SCL fall time | 20 × (IOVDD / 5.5 V) | | 300 | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | 0.6 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 1.3 | | | µs |
| **FAST-MODE PLUS** | | | | | |
| $f_{SCL}$ | SCL clock frequency | 0 | | 1000 | kHz |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.26 | | | µs |
| $t_{LOW}$ | Low period of the SCL clock | 0.5 | | | µs |
| $t_{HIGH}$ | High period of the SCL clock | 0.26 | | | µs |
| $t_{SU;STA}$ | Setup time for a repeated START condition | 0.26 | | | µs |
| $t_{HD;DAT}$ | Data hold time | 0 | | | µs |
| $t_{SU;DAT}$ | Data setup time | 50 | | | ns |
| $t_r$ | SDA and SCL Rise Time | | | 120 | ns |
| $t_f$ | SDA and SCL Fall Time | 20 × (IOVDD / 5.5 V) | | 120 | ns |
| $t_{SU;STO}$ | Setup time for STOP condition | 0.26 | | | µs |
| $t_{BUF}$ | Bus free time between a STOP and START condition | 0.5 | | | µs |

**ADVANCE INFORMATION**

## 6.7 Switching Characteristics: I²C Interface

at $T_A$ = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); seeTBD for timing diagram

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{d(SDA)}$ | SCL to SDA delay | Standard-mode | 200 | | 1250 | ns |
| | | Fast-mode | 200 | | 850 | ns |
| | | Fast-mode plus | | | 400 | ns |

## 6.8 Timing Requirements: SPI Interface

at $T_A$ = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(SCLK)}$ | SCLK period | | 40 | | | ns |
| $t_{H(SCLK)}$ | SCLK high pulse duration | | 18 | | | ns |
| $t_{L(SCLK)}$ | SCLK low pulse duration | | 18 | | | ns |
| $t_{LEAD}$ | Enable lead time | | 16 | | | ns |
| $t_{TRAIL}$ | Enable trail time | | 16 | | | ns |
| $t_{DSEQ}$ | Sequential transfer delay | | 20 | | | ns |
| $t_{SU(MOSI)}$ | MOSI data setup time | | 8 | | | ns |
| $t_{HLD(MOSI)}$ | MOSI data hold time | | 8 | | | ns |
| $t_{r(SCLK)}$ | SCLK rise time | 10% - 90% rise time | | | 6 | ns |
| $t_{f(SCLK)}$ | SCLK fall time | 90% - 10% fall time | | | 6 | ns |

## 6.9 Switching Characteristics: SPI Interface

at $T_A$ = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see for timing diagram

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{a(MISO)}$ | MISO access time | IOVDD = 1.8 V | | | 18 | ns |
| | | IOVDD = 3.3 V | | | 14 | |
| $t_{d(MISO)}$ | SCLK to MISO delay | 50% of SCLK to 50% of MISO, IOVDD = 1.8 V | | | 19 | ns |
| | | 50% of SCLK to 50% of MISO, IOVDD = 3.3 V | | | 15 | |
| $t_{dis(MISO)}$ | MISO disable time | IOVDD = 1.8 V | | | 18 | ns |
| | | IOVDD = 3.3 V | | | 14 | |

## 6.10 Timing Requirements: TDM, I²S or LJ Interface

at $T_A$ = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see for timing diagram

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{(BCLK)}$ | BCLK period | | 40 | | | ns |
| $t_{H(BCLK)}$ | BCLK high pulse duration [1] | | 18 | | | ns |
| $t_{L(BCLK)}$ | BCLK low pulse duration [1] | | 18 | | | ns |
| $t_{SU(FSYNC)}$ | FSYNC setup time | | 8 | | | ns |
| $t_{HLD(FSYNC)}$ | FSYNC hold time | | 8 | | | ns |
| $t_{r(BCLK)}$ | BCLK rise time | 10% - 90% rise time | | | 10 | ns |
| $t_{f(BCLK)}$ | BCLK fall time | 90% - 10% fall time | | | 10 | ns |

(1) The BCLK minimum high or low pulse duration must be higher than 25 ns (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

Product Folder Links: *TAD5212*

## 6.11 Switching Characteristics: TDM, I²S or LJ Interface

at T$_A$ = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| t$_{d(SDOUT-BCLK)}$ | BCLK to SDOUT delay | 50% of BCLK to 50% of SDOUT, IOVDD = 1.8 V | | | 18 | ns |
| | | 50% of BCLK to 50% of SDOUT, IOVDD = 3.3 V | | | 14 | |
| t$_{d(SDOUT-FSYNC)}$ | FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0) | 50% of FSYNC to 50% of SDOUT, IOVDD = 1.8 V | | | 18 | ns |
| | | 50% of FSYNC to 50% of SDOUT, IOVDD = 3.3 V | | | 14 | |
| f$_{(BCLK)}$ | BCLK output clock frequency; master mode [1] | | | | 24.576 | MHz |
| t$_{H(BCLK)}$ | BCLK high pulse duration; master mode | IOVDD = 1.8 V | 14 | | | ns |
| | | IOVDD = 3.3 V | 14 | | | |
| t$_{L(BCLK)}$ | BCLK low pulse duration; master mode | IOVDD = 1.8 V | 14 | | | ns |
| | | IOVDD = 3.3 V | 14 | | | |
| t$_{d(FSYNC)}$ | BCLK to FSYNC delay; master mode | 50% of BCLK to 50% of FSYNC, IOVDD = 1.8 V | | | 18 | ns |
| | | 50% of BCLK to 50% of FSYNC, IOVDD = 3.3 V | | | 14 | |
| t$_{r(BCLK)}$ | BCLK rise time; master mode | 10% - 90% rise time, IOVDD = 1.8 V | | | 10 | ns |
| | | 10% - 90% rise time, IOVDD = 3.3 V | | | 10 | |
| t$_{f(BCLK)}$ | BCLK fall time; master mode | 90% - 10% fall time, IOVDD = 1.8 V | | | 8 | ns |
| | | 90% - 10% fall time, IOVDD = 3.3 V | | | 8 | |

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

ADVANCE INFORMATION

# 7 Detailed Description

## 7.1 Overview

The TAD5212 is from a scalable family of devices. As with the extended family of devices, the TAD5212 consists of a high-performance, low-power, flexible audio digital-to-analog converter (DAC) with extensive feature integration. This device is intended for automotive applications such as telematics control unit, hands-free in-vehicle communication, emergency call, and multimedia applications. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained automotive sub-system designs. Package, performance, and device-compatible configuration registers make this device well suited for scalable system designs.

The TAD5212 consists of the following blocks:

- Low-noise programmable microphone bias output
- 2-channel, multibit, high-performance delta-sigma (ΔΣ) DACs
- Configurable single-ended, differential or pseudo-differential audio outputs
- Over Current Diagnostics and Protection for MICBIAS and analog outputs
- Automatic gain controller (AGC)
- Advanced Thermal foldback and protection
- Advanced Battery guard and distortion limiter
- Programmable interpolation filters with linear-phase or low-latency filter
- Programmable channel gain, volume control, and biquad filters for each channel
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable high-pass filter (HPF) and digital channel mixer
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

Communication to the TAD5212 for configuring the control registers is supported using an I²C and SPI interface. The device supports a highly flexible audio serial interface [time-division multiplexing (TDM), I²S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.
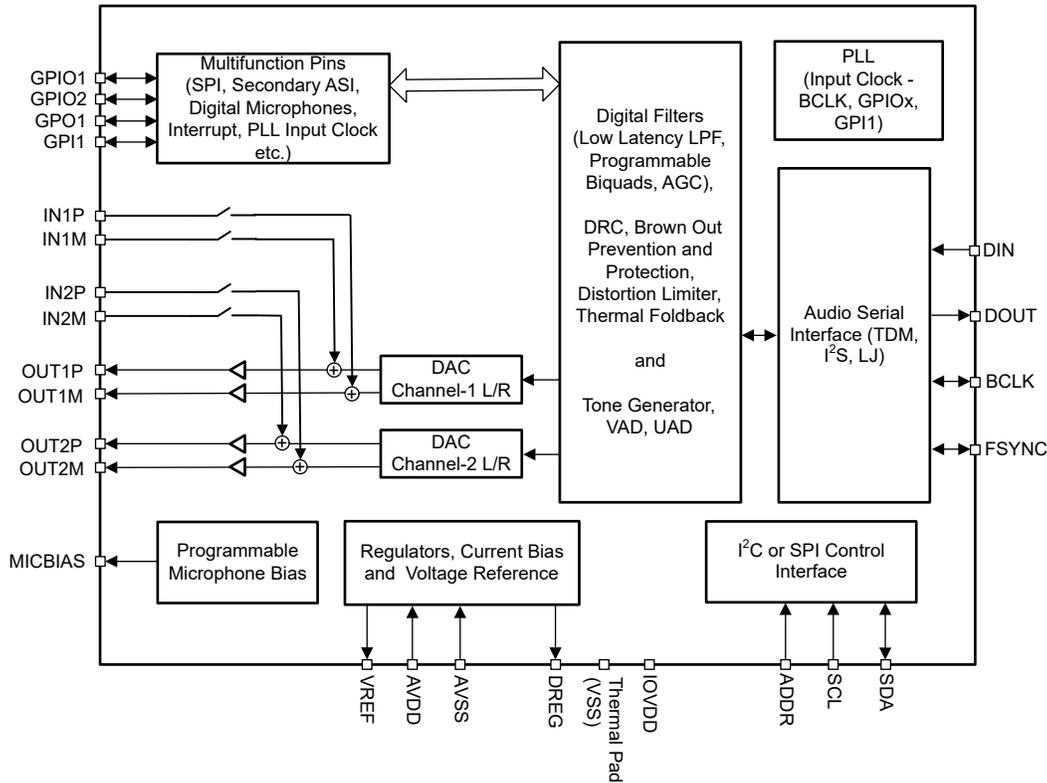
## 7.2 Functional Block Diagram

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

**Figure 7-1.**

## 7.3 Feature Description

### 7.3.1 Serial Interfaces

This device has two serial interfaces: control and audio data. The control serial interface is used for device configuration. The audio data serial interface is used for transmitting audio data to the host device.

#### 7.3.1.1 Control Serial Interfaces

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. All these registers can be accessed using either I²C or SPI communication to the device. For more information, see the *Section 7.5* section.

#### 7.3.1.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAD5212 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I²S or left-justified protocols format, programmable data length options, very flexible controller-target configurability for bus clock lines and the ability to communicate with multiple devices within a system directly.

The TAD5212 supports up to two ASI Interfaces. Secondary ASI Clock and Data Pins can be configured by setting GPIO's. Frame Sync of two ASI's must be synchronous. See the for more details on Secondary ASI.

**ADVANCE INFORMATION**

The bus protocol TDM, I$^2$S, or left-justified (LJ) format can be selected for primary ASI by using the PASI_FORMAT[1:0], P0_R26_D[7:6] register bits. As shown in Table 7-1 and .Table 7-2, these modes are all most significant byte (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length programmable as 16, 20, 24, or 32 bits by configuring the PASI_WLEN[1:0], P0_R26_D[5:4] register bits.

**Table 7-1. Primary Audio Serial Interface Format**

| P0_R26_D[7:6] : PASI_FORMAT[1:0] | PRIMARY AUDIO SERIAL INTERFACE FORMAT |
|---|---|
| 00 (default) | Time division multiplexing (TDM) mode |
| 01 | Inter IC sound (I$^2$S) mode |
| 10 | Left-justified (LJ) mode |
| 11 | Reserved (do not use this setting) |

**Table 7-2. Primary Audio Serial Interface Data Word-Length**

| P0_R7_D[5:4] : PASI_WLEN[1:0] | PRIMARY AUDIO OUTPUT CHANNEL DATA WORD-LENGTH |
|---|---|
| 00 | Data word-length set to 16 bits |
| 01 | Data word-length set to 20 bits |
| 10 | Data word-length set to 24 bits |
| 11 (default) | Data word-length set to 32 bits |

The frame sync pin, FSYNC, is used in this audio bus protocol to define the beginning of a frame and has the same frequency as the output data sample rates. The bit clock pin, BCLK, is used to clock out the digital audio data across the serial bus. The number of bit-clock cycles in a frame must accommodate multiple device active output channels with the programmed data word length.

A frame consists of multiple time-division channel slots (up to 32) to allow all input/output channel audio data transmissions to complete on the audio bus by a device or multiple devices sharing the same audio bus. The device supports up to eight input channels and eight output channels that can be configured on primary ASI bus to place their audio data on bus slot 0 to slot 31. Table 7-3 lists the output channel-1 slot configuration settings. In I$^2$S and LJ mode, the slots are divided into two sets, left-channel slots and right-channel slots, as described in the *Section 7.3.1.2.2* and *Section 7.3.1.2.3* sections.

**Table 7-3. Output Channel-1 Slot Assignment Settings**

| P0_R30_D[4:0] : PASI_TX_CH1_SLOT[4:0] | OUTPUT CHANNEL 1 SLOT ASSIGNMENT |
|---|---|
| 0 0000 = 0d (default) | Slot 0 for TDM or left slot 0 for I$^2$S, LJ. |
| 0 0001 = 1d | Slot 1 for TDM or left slot 1 for LJ. |
| … | … |
| 0 1111 = 15d | Slot 15 for TDM or left slot 15 for LJ. |
| 1 0000 = 32d | Slot 16 for TDM or right slot 0 for I$^2$S, LJ. |
| … | … |
| 1 1110 = 30d | Slot 30 for TDM or right slot 14 for LJ. |
| 1 1111 = 31d | Slot 31 for TDM or right slot 15 for LJ. |

Similarly, the slot assignment setting for output channel 2 to channel 8 can be done using the PASI_TX_CH2_SLOT (P0_R31) to PASI_TX_CH8_SLOT (P0_R37) registers and for input channel 1 to channel 8 by using the PASI_RX_CH1_SLOT(P0_R40) to PAS_RX_CH8_SLOT(P0_R47), respectively.

The slot word length is the same as the primary ASI channel word length set for the device. The output channel data word length must be set to the same value for all TAD5212 devices if all devices share the same ASI bus in a system. The maximum number of slots possible for the ASI bus in a system is limited by the available bus bandwidth, which depends upon the BCLK frequency, output data sample rate used, and the channel data word length configured.

Product Folder Links: TAD5212

The device also includes a feature that offsets the start of the slot data transfer with respect to the frame sync by up to 31 cycles of the bit clock. Offset can be configured independently for input and output data paths. Table 7-4 and Table 7-5 lists the programmable offset configuration settings for transmission and receive paths respectively.

**Table 7-4. Programmable Offset Settings for the ASI Slot Start for transmission**

| P0_R28_D[4:0] : PASI_TX_OFFSET[4:0] | PROGRAMMABLE OFFSET SETTING FOR SLOT DATA TRANSMISSION START |
|---|---|
| 0 0000 = 0d (default) | The device follows the standard protocol timing without any offset. |
| 0 0001 = 1d | Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I$^2$S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing. |
| ...... | ...... |
| 1 1110 = 30d | Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I$^2$S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. |
| 1 1111 = 31d | Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I$^2$S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. |

**Table 7-5. Programmable Offset Settings for the ASI Slot Start for Receive**

| P0_R38_D[4:0] : PASI_RX_OFFSET[4:0] | PROGRAMMABLE OFFSET SETTING FOR SLOT DATA RECEIVE START |
|---|---|
| 0 0000 = 0d (default) | The device follows the standard protocol timing without any offset. |
| 0 0001 = 1d | Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I$^2$S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing. |
| ...... | ...... |
| 1 1110 = 30d | Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I$^2$S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. |
| 1 1111 = 31d | Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I$^2$S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. |

The device also features the ability to invert the polarity of the frame sync pin, FSYNC, used to transfer the audio data as compared to the default FSYNC polarity used in standard protocol timing. This feature can be set using the PASI_FSYNC_POL, P0_R26_D3 register bit. Similarly, the device can invert the polarity of the bit clock pin, BCLK, which can be set using the PASI_BCLK_POL, P0_R26_D2 register bit.

In addition, the word clock and bit clock can be independently configured in either Controller or Target mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected DAC channels sampling frequencies.

**7.3.1.2.1 Time Division Multiplexed Audio (TDM) Interface**

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. Figure 7-2 to Figure 7-5 illustrate the protocol timing for TDM operation with various configurations.

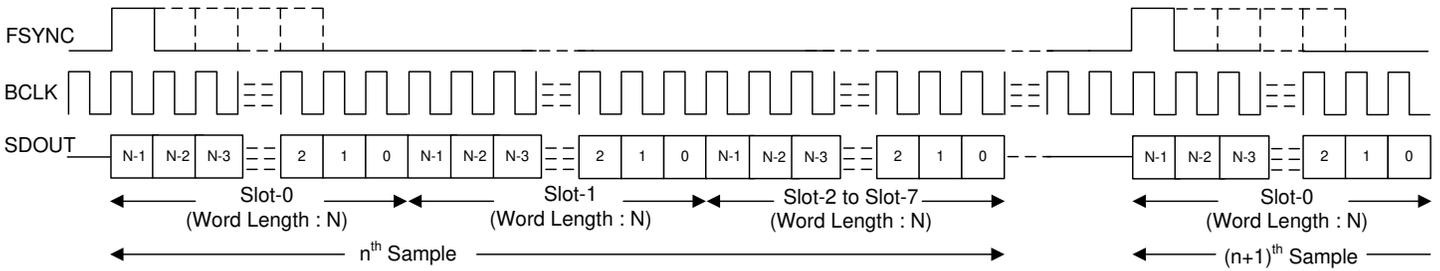**ADVANCE INFORMATION**

**Figure 7-2. TDM Mode Standard Protocol Timing (PASI_TX_OFFSET = 0)**



**Figure 7-3. TDM Mode Protocol Timing (PASI_TX_OFFSET = 2)**



**Figure 7-4. TDM Mode Protocol Timing (No Idle BCLK Cycles, PASI_TX_OFFSET = 2)**



**Figure 7-5. TDM Mode Protocol Timing (PASI_TX_OFFSET = 0 and PASI_BCLK_POL = 1)**

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well. For a higher BCLK frequency operation, using TDM mode with a PASI_TX_OFFSET value higher than 0 is recommended.

**7.3.1.2.2 Inter IC Sound (I²S) Interface**

The standard I²S protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In I²S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted on the falling edge of

BCLK in the second cycle after the *rising* edge of FSYNC. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC and each data bit is transmitted on the falling edge of BCLK. Figure 7-6 to Figure 7-9 illustrate the protocol timing for I²S operation with various configurations.



**Figure 7-6. I²S Mode Standard Protocol Timing (PASI_TX_OFFSET = 0)**
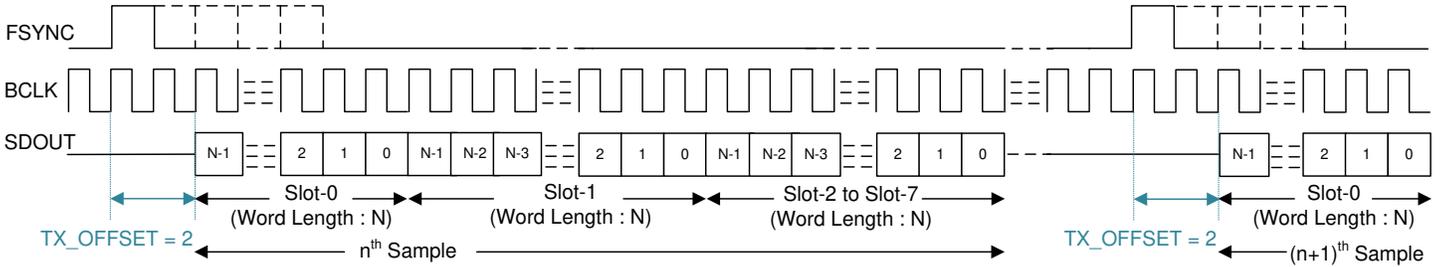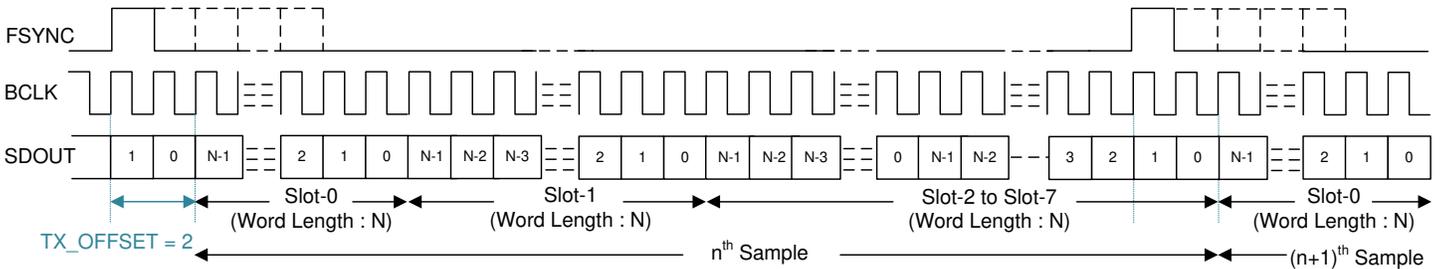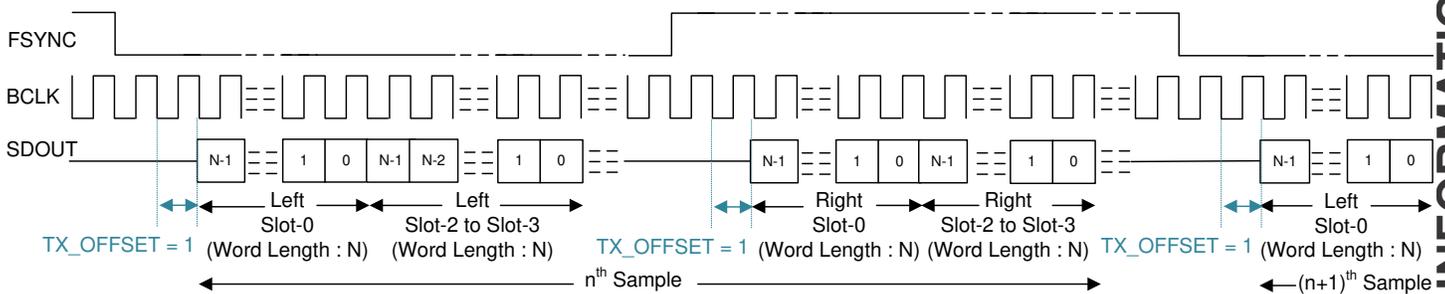


**Figure 7-7. I²S Protocol Timing (PASI_TX_OFFSET = 1)**



**Figure 7-8. I²S Protocol Timing (No Idle BCLK Cycles, PASI_TX_OFFSET = 0)**
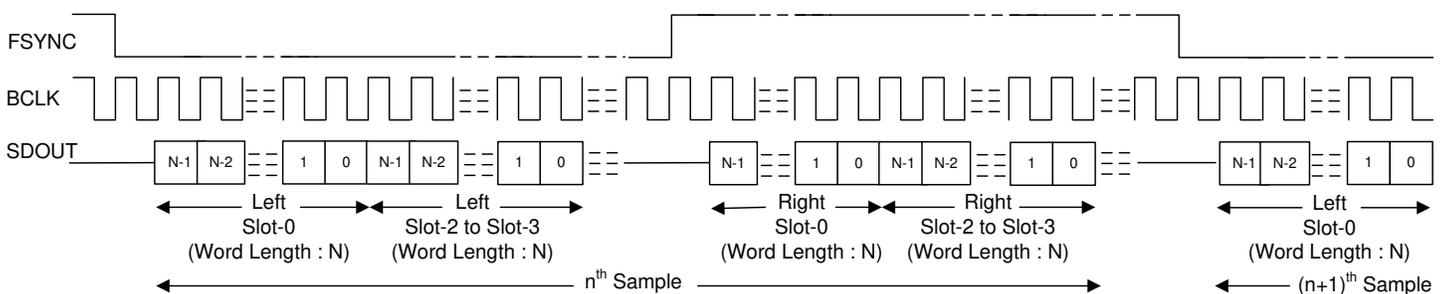


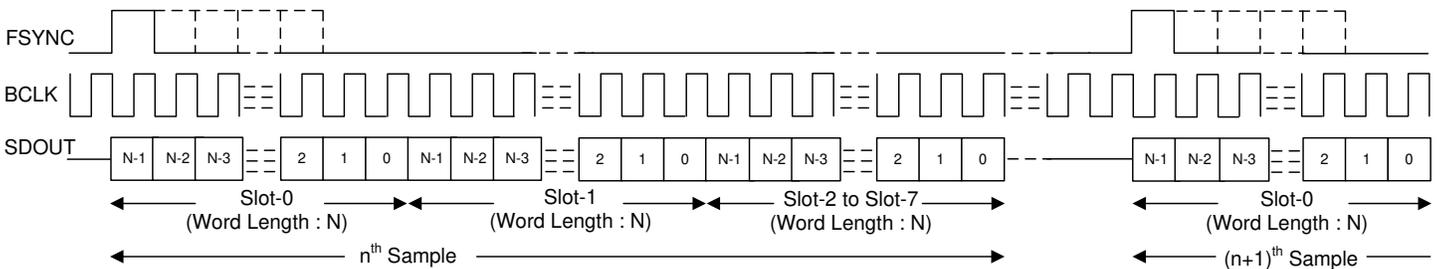**Figure 7-9. I²S Protocol Timing (PASI_TX_OFFSET = 0 and PASI_BCLK_POL = 1)**

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC high

Product Folder Links: TAD5212

pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured.

### 7.3.1.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC is transmitted on the falling edge of BCLK. Figure 7-10 to Figure 7-13 illustrate the protocol timing for LJ operation with various configurations.
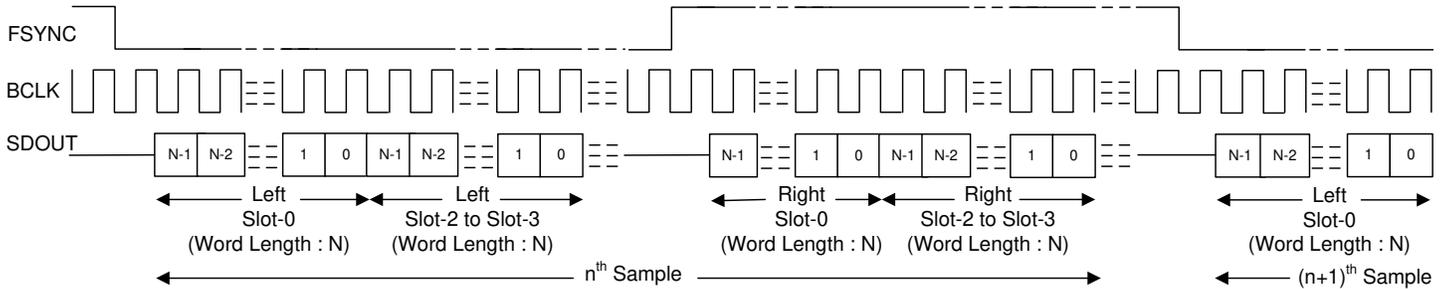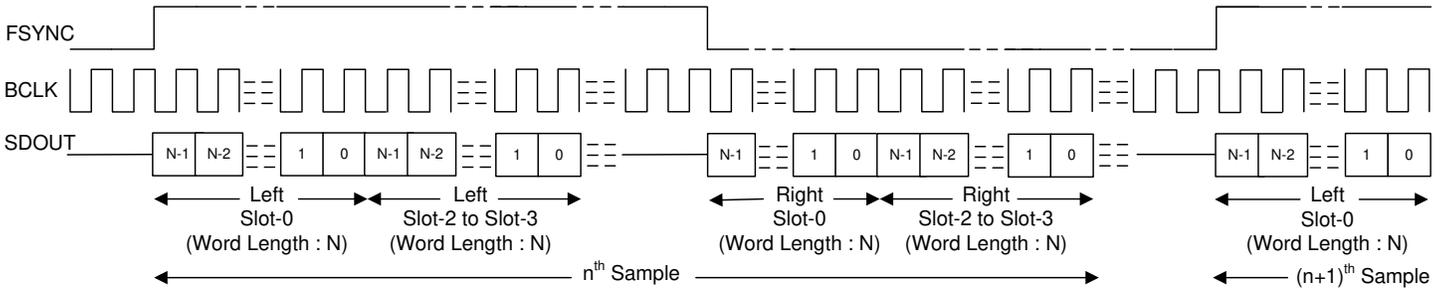


**Figure 7-10. LJ Mode Standard Protocol Timing (TX_OFFSET = 0)**
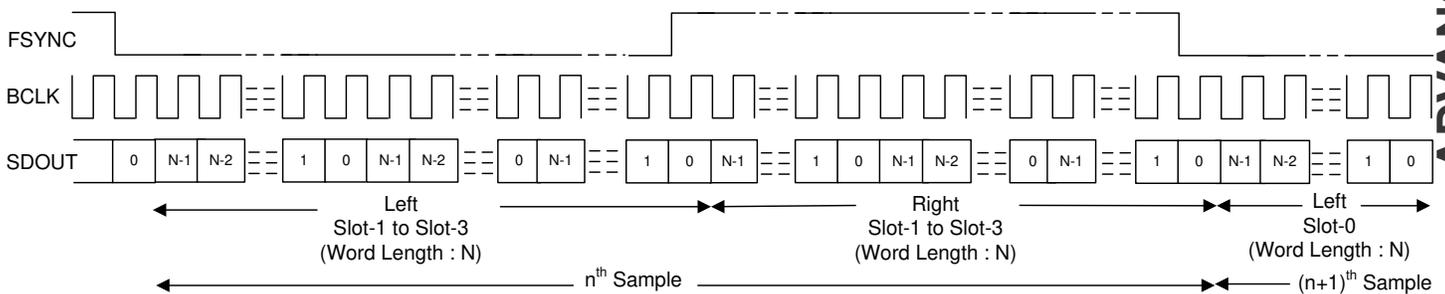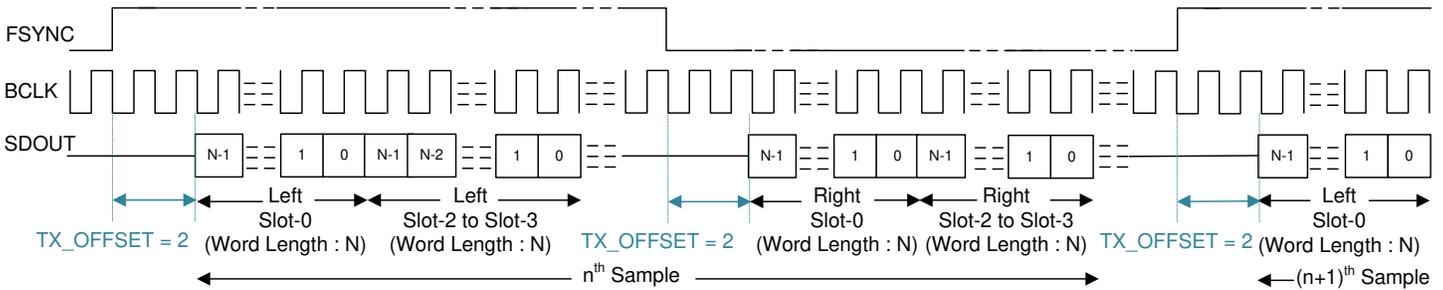


**Figure 7-11. LJ Protocol Timing (TX_OFFSET = 2)**
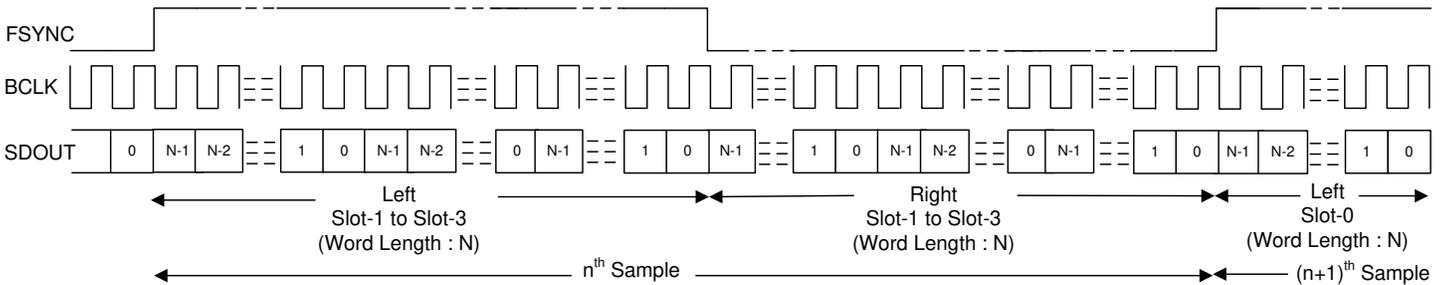


**Figure 7-12. LJ Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)**

ADVANCE INFORMATION
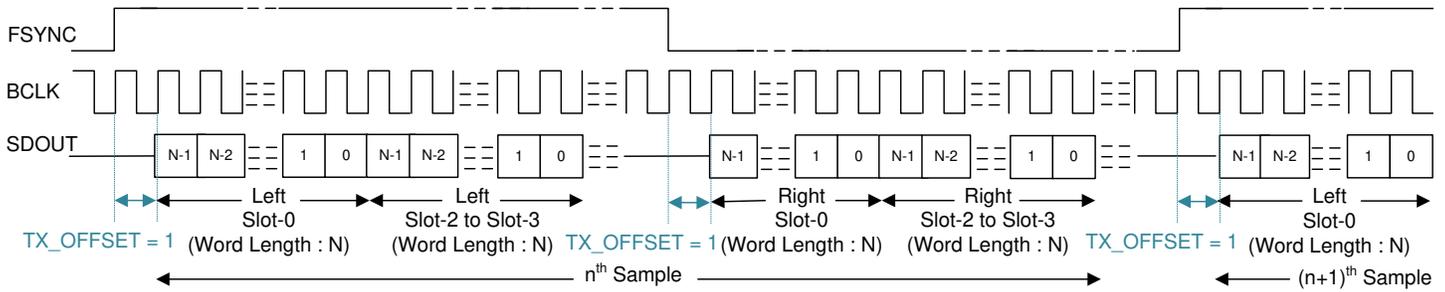
**Figure 7-13. LJ Protocol Timing (TX_OFFSET = 1 and BCLK_POL = 1)**

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC low pulse must be number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured. For a higher BCLK frequency operation, using LJ mode with a TX_OFFSET value higher than 0 is recommended.

### 7.3.1.3 Using Multiple Devices With Shared Buses

The device has many supported features and flexible options that can be used in the system to seamlessly connect multiple TAD5212 devices by sharing a single common I$^2$C or SPI control bus and an audio serial interface bus. This architecture enables multiple applications to be applied to a system that require a microphone or speaker array for beam-forming operation, audio conferencing, noise cancellation, and so forth. Figure 7-14 shows a diagram of multiple TAD5212 devices in a configuration where the control and audio data buses are shared.
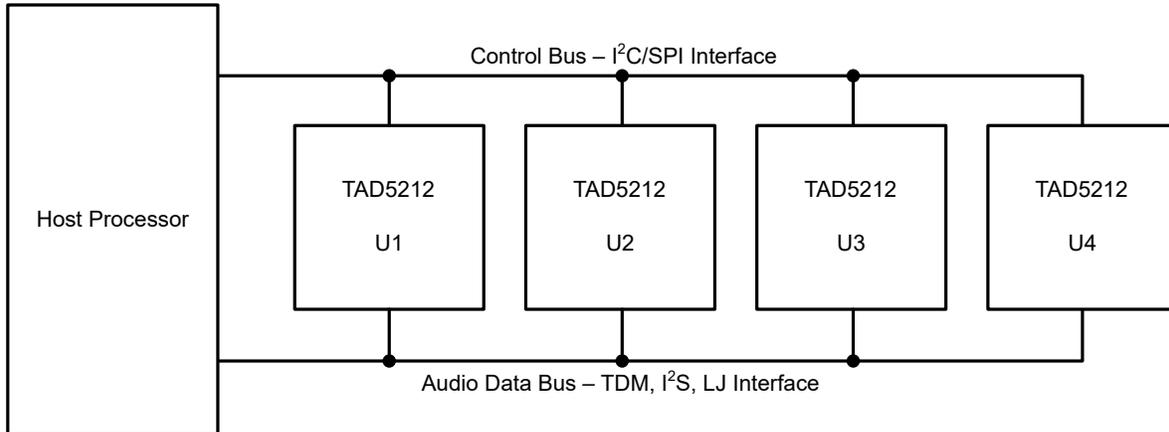


**Figure 7-14. Multiple TAD5212 Devices With Shared Control and Audio Data Buses**

The TAD5212 consists of the following features to enable seamless connection and interaction of multiple devices using a shared bus:
- Supports up to four pin-programmable I$^2$C target addresses
- I$^2$C broadcast simultaneously writes to (or triggers) all TAD5212 devices
- Supports up to 32 configuration input/output channel slots for the audio serial interface
- Tri-state feature (with enable and disable) for the unused audio data slots of the device
- Supports a bus-holder feature (with enable and disable) to keep the last driven value on the audio bus
- The GPIOx, GPI1 or GPO1 pin can be configured as a secondary input/output data lane or as a secondary audio serial interface
- The GPIOx, GPI1 or GPO1 pin can be used in a daisy-chain configuration of multiple TAD5212 devices

- Supports one BCLK cycle data latching timing to relax the timing requirement for the high-speed interface
- Programmable controller and target options for both primary and secondary audio serial interface
- Ability to synchronize the multiple devices for the simultaneous sampling requirement across devices
- Inter Channel Gain Alignment(ICGA) feature to align the DAC Channel gain across devices.

See the *Multiple TAC5x1x Devices With a Shared TDM and I²C/SPI Bus* application report for further details.

**ADVANCE INFORMATION**

Product Folder Links: *TAD5212*

### 7.3.1.4 Phase-Locked Loop (PLL) and Clock Generation

The device has a smart auto-configuration block to generate all necessary internal clocks required for the DAC modulators and the digital filter engine used for signal processing. This configuration is done by monitoring the frequency of the FSYNC and BCLK signal on the audio buses.

The device supports the various data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. Table 7-6 and Table 7-7 list the supported FSYNC and BCLK frequencies.

**Table 7-6. Supported FSYNC (Multiples or Submultiples of 48 kHz) and BCLK Frequencies**

| BCLK TO FSYNC RATIO | BCLK (MHz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | FSYNC (8 kHz) | FSYNC (16 kHz) | FSYNC (24 kHz) | FSYNC (32 kHz) | FSYNC (48 kHz) | FSYNC (96 kHz) | FSYNC (192 kHz) | FSYNC (384 kHz) | FSYNC (768 kHz) |
| 16 | **Reserved** | 0.256 | 0.384 | 0.512 | 0.768 | 1.536 | 3.072 | 6.144 | 12.288 |
| 24 | **Reserved** | 0.384 | 0.576 | 0.768 | 1.152 | 2.304 | 4.608 | 9.216 | 18.432 |
| 32 | 0.256 | 0.512 | 0.768 | 1.024 | 1.536 | 3.072 | 6.144 | 12.288 | 24.576 |
| 48 | 0.384 | 0.768 | 1.152 | 1.536 | 2.304 | 4.608 | 9.216 | 18.432 | **Reserved** |
| 64 | 0.512 | 1.024 | 1.536 | 2.048 | 3.072 | 6.144 | 12.288 | 24.576 | **Reserved** |
| 96 | 0.768 | 1.536 | 2.304 | 3.072 | 4.608 | 9.216 | 18.432 | **Reserved** | **Reserved** |
| 128 | 1.024 | 2.048 | 3.072 | 4.096 | 6.144 | 12.288 | 24.576 | **Reserved** | **Reserved** |
| 192 | 1.536 | 3.072 | 4.608 | 6.144 | 9.216 | 18.432 | **Reserved** | **Reserved** | **Reserved** |
| 256 | 2.048 | 4.096 | 6.144 | 8.192 | 12.288 | 24.576 | **Reserved** | **Reserved** | **Reserved** |
| 384 | 3.072 | 6.144 | 9.216 | 12.288 | 18.432 | **Reserved** | **Reserved** | **Reserved** | **Reserved** |
| 512 | 4.096 | 8.192 | 12.288 | 16.384 | 24.576 | **Reserved** | **Reserved** | **Reserved** | **Reserved** |
| 1024 | 8.192 | 16.384 | 24.576 | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** |
| 2048 | 16.384 | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** |

**Table 7-7. Supported FSYNC (Multiples or Submultiples of 44.1 kHz) and BCLK Frequencies**

| BCLK TO FSYNC RATIO | BCLK (MHz) | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | FSYNC (7.35 kHz) | FSYNC (14.7 kHz) | FSYNC (22.05 kHz) | FSYNC (29.4 kHz) | FSYNC (44.1 kHz) | FSYNC (88.2 kHz) | FSYNC (176.4 kHz) | FSYNC (352.8 kHz) | FSYNC (705.6 kHz) |
| 16 | **Reserved** | **Reserved** | 0.3528 | 0.4704 | 0.7056 | 1.4112 | 2.8224 | 5.6448 | 11.2896 |
| 24 | **Reserved** | 0.3528 | 0.5292 | 0.7056 | 1.0584 | 2.1168 | 4.2336 | 8.4672 | 16.9344 |
| 32 | **Reserved** | 0.4704 | 0.7056 | 0.9408 | 1.4112 | 2.8224 | 5.6448 | 11.2896 | 22.5792 |
| 48 | 0.3528 | 0.7056 | 1.0584 | 1.4112 | 2.1168 | 4.2336 | 8.4672 | 16.9344 | **Reserved** |
| 64 | 0.4704 | 0.9408 | 1.4112 | 1.8816 | 2.8224 | 5.6448 | 11.2896 | 22.5792 | **Reserved** |
| 96 | 0.7056 | 1.4112 | 2.1168 | 2.8224 | 4.2336 | 8.4672 | 16.9344 | **Reserved** | **Reserved** |
| 128 | 0.9408 | 1.8816 | 2.8224 | 3.7632 | 5.6448 | 11.2896 | 22.5792 | **Reserved** | **Reserved** |
| 192 | 1.4112 | 2.8224 | 4.2336 | 5.6448 | 8.4672 | 16.9344 | **Reserved** | **Reserved** | **Reserved** |
| 256 | 1.8816 | 3.7632 | 5.6448 | 7.5264 | 11.2896 | 22.5792 | **Reserved** | **Reserved** | **Reserved** |
| 384 | 2.8224 | 5.6448 | 8.4672 | 11.2896 | 16.9344 | **Reserved** | **Reserved** | **Reserved** | **Reserved** |
| 512 | 3.7632 | 7.5264 | 11.2896 | 15.0528 | 22.5792 | **Reserved** | **Reserved** | **Reserved** | **Reserved** |
| 1024 | 7.5264 | 15.0528 | 22.5792 | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** |
| 2048 | 15.0528 | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** | **Reserved** |

The TAD5212 also supports non-Audio sample rates beyond those listed in prior tables. Refer to Configuring Non-Audio Sample Rates for TAC5x1x devices for more details.

The TAD5212 sample rate can be configured using registers CLK_DET0 (P0_R62) and CLK_DET1 (P0_R63) for primary and secondary ASI respectively. These registers also capture the device auto detect result for the FSYNC frequency in auto detection mode. The registers CLK_DET2 (P0_R64) and CLK_DET3 (P0_R65)

**ADVANCE INFORMATION**

capture the BCLK to FSYNC ratio detected of the device . If the device finds any unsupported combinations of FSYNC frequency and BCLK to FSYNC ratios, the device generates an ASI clock-error interrupt and mutes all the channels accordingly.

The TAD5212 also supports enabling channels while DAC channels are already in operation. This requires a pre-configuration before power to describe maximum number of channels which can be enabled while in opeartion to ensure proper clock generation and use. This can be configured by using register DYN_PUPD_CFG (P0_R119). DAC_DYN_PUPD_EN bits can be used to independently enable DAC Channels dynamic power up. Number of channels can be configured using DAC_DYN_MAXCH_SEL bits.

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the modulators and digital filter engine, as well as other control blocks. The device also supports an option to use BCLK, GPIOx, or the GPI1 pin (as CCLK) as the audio clock source without using the PLL to reduce power consumption. However, the DAC performance may degrade based on jitter from the external clock source, and some processing features may not be supported if the external audio clock source frequency is not high enough. Therefore, TI recommends using the PLL for high-performance applications. More details and information on how to configure and use the device in low-power mode without using the PLL are discussed in the *TAC5x1x Power Consumption Matrix Across Various Usage Scenarios* application report.

The device also supports an audio bus controller mode operation using the GPIOx or GPI1 pin (as CCLK) as the reference input clock source and supports various flexible options and a wide variety of system clocks. More details and information on controller mode configuration and operation are discussed in the *Configuring and Operating TAC5x1x as an Audio Bus Controller* application report.

The audio bus clock error detection and auto-detect feature automatically generates all internal clocks, but can be disabled using the IGNORE_CLK_ERR (P0_R4_D6) and CUSTOM_CLK_CFG (P0_R50_D0) register bits, respectively. In the system, this disable feature can be used to support custom clock frequencies that are not covered by the auto detect scheme. For such application use cases, care must be taken to ensure that the multiple clock dividers are all configured appropriately. Therefore, TI recommends using the PPC3 GUI for device configuration settings; for more details see the *TAC5212EVM-PDK Evaluation module* user's guide and the PurePath™ console graphical development suite.

### 7.3.1.5 Output Channel Configurations

The device consists of two pairs of analog output pins (OUTxP and OUTxM) that can be configured as differential inputs or single-ended outputs for playback channel. The device supports simultaneous playback of up to four channels single-ended output or up to two channel differential output using the high-performance multichannel DAC. Table 7-8 shows the input source selection for the playback channels.

**Table 7-8. Input Source Selection for the Playback Channel**

| P0_R100_D[7:5] : OUT1x_SRC[2:0] | OUT1P/OUT1M Source Selection |
|---|---|
| 000 (default) | Output driver disabled |
| 001 | DAC signal chain |
| 010 | Analog bypass signal chain |
| 011 | Mixing of DAC and analog bypass signal chains |
| 100 | OUT1P for DAC and OUT1M for analog bypass signal chain |
| 101 | OUT1P for analog bypass and OUT1M for DAC signal chain. |
| 11x | Reserved. Do not use this setting. |

Similarly, the input source selection setting for output channel 2 can be configured using the OUT2x_SRC[2:0] (P0_R107_D[7:5]) register bits.

The TAD5212 supports up to 2 channel differential output, up to 2 channel pseudo-differential output and up to 4 channel single-ended output. Each of the output channels can be independently configured for differential or single-ended output.

Table 7-9 shows the configuration modes for the output pins

ADVANCE INFORMATION

**Table 7-9. Output Pin Configuration for the Playback Channel**

| P0_R100_D[4:2] : OUT1x_CFG[2:0] | OUT1P/OUT1M Pin Configuration |
|---|---|
| 000 (default) | OUT1P/OUT1M as a differential pair |
| 001 | OUT1P and OUT1M as independent single-ended outputs |
| 010 | Mono Single Ended output on OUT1P only |
| 011 | Mono Single Ended output on OUT1M only |
| 100 | Pseudo differential output with OUT1P as signal and OUT1M as VCOM |
| 101 | Pseudo differential output with OUT1P as signal, OUT1M as VCOM and OUT2M as VCOM sense. |
| 110 | Pseudo differential output with OUT1M as signal and OUT1P as VCOM |
| 111 | Reserved. Do not use this setting. |

Similarly, the output pin configuration for output channel 2 can be done using the OUT2x_CFG[2:0] (P0_R107_D[4:2]) register bits.

The TAD5212 can support a variety of load including headphone, lineout and receiver amplifiers. Load drive configurations are available for each pin independently. OUT1P_DRIVE[1:0] (OUT1x_CFG[7:6]) configures the load drive capability for OUT1P pin. OUT1M_DRIVE[1:0], OUT2P_DRIVE[1:0], OUT2M_DRIVE[1:0] are the output drive control for OUT1M, OUT2P and OUT2M respectively.

### 7.3.1.6 Reference Voltage

All audio data converters require a DC reference voltage. The TAD5212 achieves low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with high PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1-µF capacitor connected from the VREF pin to analog ground (VSS).

The value of this reference voltage can be configured using the P0_R77_D[1:0] register bits and must be set to an appropriate value based on the desired full-scale input for the device and the AVDD supply voltage available in the system. The default VREF value is set to 2.75 V, which in turn supports a 2-$V_{RMS}$ differential full-scale input to the device. The required minimum AVDD voltage for this mode is 3 V. Table 7-10 lists the various VREF settings supported along with required AVDD range and the supported full-scale input signal for that configuration.

**Table 7-10. VREF Programmable Settings**

| P0_R77_D[1:0] : VREF[1:0] | VREF OUTPUT VOLTAGE | DIFFERENTIAL FULL-SCALE INPUT SUPPORTED | SINGLE-ENDED FULL-SCALE INPUT SUPPORTED | AVDD RANGE REQUIREMENT |
|---|---|---|---|---|
| 00 (default) | 2.75 V | 2 $V_{RMS}$ (4 $V_{RMS}$ supported in high swing mode) | 1 $V_{RMS}$ | 3 V to 3.6 V |
| 01 | 2.5 V | 1.818 $V_{RMS}$ | 0.909 $V_{RMS}$ | 2.8 V to 3.6 V |
| 10 | 1.375 V | 1 $V_{RMS}$ | 0.5 $V_{RMS}$ | 1.7 V to 1.9 V |
| 11 | Reserved | Reserved | Reserved | Reserved |

To achieve low-power consumption, this audio reference block is powered down as described in the *Section 7.4* section. When exiting sleep mode, the audio reference block is powered up using the internal fast-charge scheme and the VREF pin settles to its steady-state voltage after the settling time (a function of the decoupling capacitor on the VREF pin). This time is approximately equal to 3.5 ms when using a 1-µF decoupling capacitor. If a higher-value decoupling capacitor is used on the VREF pin, the fast-charge setting must be reconfigured using the VREF_QCHG (P0_R2_D[4:3]) register bits, which support options of 3.5 ms (default), 10 ms, 50 ms, or 100 ms.

### 7.3.1.7 Programmable Microphone Bias

The device integrates a built-in, low-noise microphone bias pin that can be used in the system for biasing electret-condenser microphones or providing the supply to the MEMS analog or digital microphone. The

**ADVANCE INFORMATION**

**ADVANCE INFORMATION**

integrated bias amplifier supports up to 10 mA of load current that can be used for multiple microphones and is designed to provide a combination of high PSRR, low noise, and programmable bias voltages to allow the biasing to be fine tuned for specific microphone combinations.

When using this MICBIAS pin for biasing or supplying to multiple microphones, avoid any common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones. Table 7-11 shows the available microphone bias programmable options.

**Table 7-11. MICBIAS Programmable Settings**

| P0_R77_D[3:2] : MICBIAS_VAL[1:0] | P0_R77_D[1:0] : VREF_FSCALE[1:0] | MICBIAS OUTPUT VOLTAGE |
|---|---|---|
| 00 (default) | 00 (default) | 2.75 V (same as the VREF output) |
| | 01 | 2.5 V (same as the VREF output) |
| | 10 | 1.375 V (same as the VREF output) |
| | 11 | Reserved (do not use these settings) |
| 01 | 00 (default) | 1.375 V (0.5 times the VREF output) |
| | 01 | 1.250 V (0.5 times the VREF output) |
| | 10 or 11 | Reserved (do not use these settings) |
| 10 | XX | Reserved (do not use these settings) |
| 11 | XX | Same as AVDD |

The microphone bias output can be powered on or powered off (default) by configuring the MICBIAS_PDZ, P0_R120_D5 register bit. Additionally, the device provides an option to configure the GPIO1 or GPIx pin to directly control the microphone bias output powering on or off. This feature is useful to control the microphone directly without engaging the host for I$^2$C or SPI communication. The MICBIAS_PDZ, P0_R120_D5 register bit value is ignored if the GPIO1 or GPIx pin is configured to set the microphone bias on or off.

### 7.3.1.8 Signal-Chain Processing

The TAD5212 signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package makes the TAD5212 optimized for a variety of end-equipments and applications that require multichannel audio playback. Section 7.3.1.8.1 describe key components in DAC signal chain further.

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

**7.3.1.8.1 DAC Signal-Chain**

Figure 7-15 shows the key components of the playback signal chain.
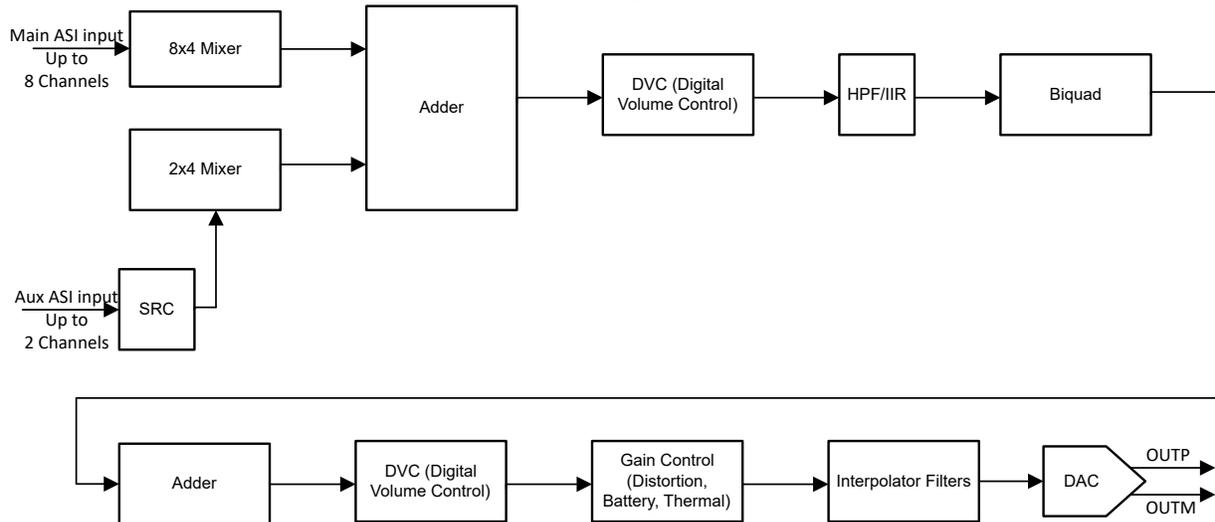


**Figure 7-15. DAC Signal-Chain Processing Flowchart**

The DAC signal chain offers a highly flexible low noise playback path for low noise and high-fidelity audio applications. This low-noise and low-distortion, multibit, delta-sigma DAC enables the TAD5212 to achieve 120dB dynamic range in a very low power. Moreover, the DAC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band. Further on in the signal chain, an integrated, high-performance multistage digital interpolation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The signal chain also consists of various highly programmable digital processing blocks such as biquad filters, phase calibration, gain calibration, high-pass filter, digital summer or mixer, synchronous sample rate converter, distortion limiter, thermal foldback, brownout prevention and volume control. The details on these processing blocks are discussed further in this section. The device also supports up to four channel single-ended output modes and an analog bypass option from analog input to DAC output.

The output channels for playback can be enabled or disabled by using the CH_EN (P0_R118) register, and the input channels for the audio serial interface can be enabled or disabled by using the PASI_RX_CHx_CFG or SASI_RX_CHx_CFG bits. The device supports simultaneous power-up and power-down of all active channels for simultaneous playback. However, based on the application needs, if some channels must be powered-up or powered-down dynamically when the other channel playback is on, then that use case is supported by setting the DYN_PUPD_CFG register.

The device supports multiple data mixing options where up to 8 Input Channels from Main ASI, 2 Input Channels from Aux ASI, and tone generator can be mixed with flexible gain options for each path before playback on DAC output. By default, these mixers are disabled and channels are configured for only one channel data. Mixers can be configured by setting ASI_DIN_Mixers in Page 17.

The device supports an output signal bandwidth up to 100 kHz, which allows the high-frequency non-audio signal to be played by using a 216-kHz (or higher) sample rate. Wide band mode can be enbaled or disabled by using DAC_CHx_BW_Mode bit.

For sample rates of 48 kHz or lower, the device supports all features and various programmable processing blocks. However, for sample rates higher than 48 kHz, there are limitations in the number of simultaneous channel recording and playback supported and the number of biquad filters and such. See the *TAC5212 Sampling Rates and Programmable Processing Blocks Supported* application report for further details.

*7.3.1.8.1.1 Programmable Channel Gain and Digital Volume Control*

The device has an independent programmable channel gain setting for each output channel that can be set to the appropriate value based on the maximum input signal expected in the system, This can be done by configuring OUT1x_LVL_CTRL and OUT2x_LVL_CTRL bits. Coarse gain configuration from -6dB to +24dB is available with these controls in steps of 6dB. .

The device has a programmable digital volume control with a range from –100 dB to 27 dB in steps of 0.5 dB with the option to mute the channel recording. The digital volume control value can be changed dynamically while the DAC channel is powered-up and playing. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the DAC_DSP_DISABLE_SOFT_STEP (P0_R115_D1) register bit.

The digital volume control setting is independently available for each of the 4 single ended output channels. In case of 2 Channel Differential DAC, Only settings for DAC_CH1A and DAC_CH2A are applicable. The device also supports an option to gang-up the volume control setting for all channels together using the channel 1A digital volume control setting, regardless if channel 1A is powered up or powered down. This gang-up can be enabled using the DAC_DSP_DVOL_GANG (P0_R115_D0) register bit.

Table 7-12 shows the programmable options available for the digital volume control.

**Table 7-12. Digital Volume Control (DVC) Programmable Settings**

| P0_R103_D[7:0] : DAC_CH1A_DVOL[7:0] | DVC SETTING FOR OUTPUT CHANNEL 1A |
|---|---|
| 0000 0000 = 0d | Output channel 1 DVC is set to mute |
| 0000 0001 = 1d | Output channel 1 DVC is set to –100 dB |
| 0000 0010 = 2d | Output channel 1 DVC is set to –99.5 dB |
| 0000 0011 = 3d | Output channel 1 DVC is set to –99 dB |
| … | … |
| 1100 1000 = 200d | Output channel 1 DVC is set to –0.5 dB |
| 1100 1001 = 201d (default) | Output channel 1 DVC is set to 0 dB |
| 1100 1010 = 202d | Output channel 1 DVC is set to 0.5 dB |
| … | … |
| 1111 1101 = 253d | Output channel 1 DVC is set to 26 dB |
| 1111 1110 = 254d | Output channel 1 DVC is set to 26.5 dB |
| 1111 1111 = 255d | Output channel 1 DVC is set to 27 dB |

Similarly, the digital volume control setting for output channel 1B,2A and 2B can be configured using the CH1B_DVOL (P0_R103) to CH2B_DVOL (P0_R112) register bits, respectively.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the playback channel which can cause audible artifacts. This feature can also be entirely disabled using the DAC_DSP_DISABLE_SOFT_STEP (P0_R115_D1) register bit.

*7.3.1.8.1.2 Programmable Channel Gain Calibration*

Along with the digital volume control, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1 dB for a range of –0.8-dB to 0.7-dB gain error. This adjustment is useful when trying to match the gain across channels resulting from trasnducer sensitivity and load impedance mismatch. This feature, in combination with the regular digital volume control, allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1 dB. Table 7-13 shows the programmable options available for the channel gain calibration.

**ADVANCE INFORMATION**

**Table 7-13. DAC Channel Gain Calibration Programmable Settings**

| P0_R104_D[7:4] : DAC_CH1A_FGAIN[3:0] | CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1A |
|---|---|
| 0000 = 0d | Input channel 1 gain calibration is set to –0.8 dB |
| 0001 = 1d | Input channel 1 gain calibration is set to –0.7 dB |
| … | … |
| 1000 = 8d (default) | Input channel 1 gain calibration is set to 0 dB |
| … | … |
| 1110 = 14d | Input channel 1 gain calibration is set to 0.6 dB |
| 1111 = 15d | Input channel 1 gain calibration is set to 0.7 dB |

Similarly, the channel gain calibration setting for input channel 1B,2A and 2B can be configured using the DAC_CH1B_CFG1 (P0_R106), DAC_CH2A_CFG1 (P0_R111), and DAC_CH2B_CFG1 (P0_R113) register bits, respectively.

#### 7.3.1.8.1.3 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all DAC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. Table 7-14 shows the predefined –3-dB cutoff frequencies available that can be set by using the DAC_DSP_HPF_SEL[1:0] register bits of P0_R115. Additionally, to achieve a custom –3-dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the DAC_DSP_HPF_SEL[1:0] register bits are set to 2'b00. Figure 7-16 illustrates a frequency response plot for the HPF filter.

**Table 7-14. HPF Programmable Settings**

| P0_R115_D[5:4] : DAC_DSP_HPF_SEL[1:0] | -3-dB CUTOFF FREQUENCY SETTING | -3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE | -3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE |
|---|---|---|---|
| 00 | Programmable 1st-order IIR filter | Programmable 1st-order IIR filter | Programmable 1st-order IIR filter |
| 01 (default) | $0.00002 \times f_S$ | 0.25 Hz | 1 Hz |
| 10 | $0.00025 \times f_S$ | 4 Hz | 12 Hz |
| 11 | $0.002 \times f_S$ | 32 Hz | 96 Hz |
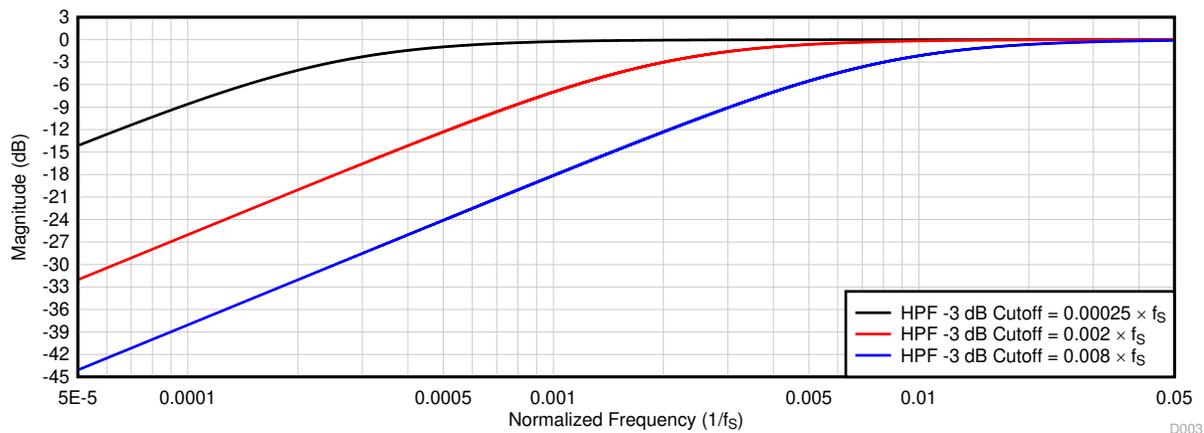


**Figure 7-16. HPF Filter Frequency Response Plot**

Equation 1 gives the transfer function for the first-order programable IIR filter:

Product Folder Links: *TAD5212*

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}}$$

(1)

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in Table 7-15 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If DAC_DSP_HPF_SEL[1:0] are set to 2'b00, the host device must write these coefficients values for the desired frequency response before powering-up any DAC channel for playback. Table 7-15 shows the filter coefficients for the first-order IIR filter.

**Table 7-15. 1st-Order IIR Filter Coefficients**

| FILTER | FILTER COEFFICIENT | DEFAULT COEFFICIENT VALUE | COEFFICIENT REGISTER MAPPING |
|---|---|---|---|
| Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter) | $N_0$ | 0x7FFFFFFF | P17_R120-R124 |
| | $N_1$ | 0x00000000 | P17_R125-R128 |
| | $D_1$ | 0x00000000 | P18_R8-R11 |

### 7.3.1.8.1.4 Programmable Digital Biquad Filters

The device supports up to 12 programmable digital biquad filters available for DAC signal chain limited to 3/channel. These highly efficient filters achieve the desired frequence response. The TAD5212 also supports on the fly programmable Biquad filters for two channel playback use case. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. Equation 2 gives the transfer function of each biquad filter:

$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{31} - 2D_1 z^{-1} - D_2 z^{-2}}$$

(2)

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for a low-pass, high-pass, or any other desired frequency shaping. As described in Table 7-16, these biquad filters can be allocated for each output channel based on the DAC_DSP_BQ_CFG[1:0] register setting of P0_R115. By setting DAC_DSP_BQ_CFG[1:0] to 2'b00, the biquad filtering for all playback channels are disabled and the host device can choose this setting if no additional filtering is required for the system application. See the *TAC5212 Programmable Biquad Filter Configuration and Applications* application report for further details.

**Table 7-16. Biquad Filter Allocation to the Output Channel**

| PROGRAMMABLE BIQUAD FILTER | RECORD OUTPUT CHANNEL ALLOCATION USING P0_R115_D[3:2] REGISTER SETTING | | |
|---|---|---|---|
| | DAC_DSP_BQ_CFG[1:0] = 2'b01 (1 Biquad per Channel) | DAC_DSP_BQ_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel) | DAC_DSP_BQ_CFG[1:0] = 2'b11 (3 Biquads per Channel) |
| Biquad filter 1 | Allocated to output channel 1 | Allocated to output channel 1 | Allocated to output channel 1 |
| Biquad filter 2 | Allocated to output channel 2 | Allocated to output channel 2 | Allocated to output channel 2 |
| Biquad filter 3 | Allocated to output channel 3 | Allocated to output channel 3 | Allocated to output channel 3 |
| Biquad filter 4 | Allocated to output channel 4 | Allocated to output channel 4 | Allocated to output channel 4 |
| Biquad filter 5 | Not used | Allocated to output channel 1 | Allocated to output channel 1 |
| Biquad filter 6 | Not used | Allocated to output channel 2 | Allocated to output channel 2 |
| Biquad filter 7 | Not used | Allocated to output channel 3 | Allocated to output channel 3 |
| Biquad filter 8 | Not used | Allocated to output channel 4 | Allocated to output channel 4 |
| Biquad filter 9 | Not used | Not used | Allocated to output channel 1 |
| Biquad filter 10 | Not used | Not used | Allocated to output channel 2 |

**Table 7-16. Biquad Filter Allocation to the Output Channel (continued)**

| PROGRAMMABLE BIQUAD FILTER | RECORD OUTPUT CHANNEL ALLOCATION USING P0_R115_D[3:2] REGISTER SETTING | | |
|---|---|---|---|
| | DAC_DSP_BQ_CFG[1:0] = 2'b01 (1 Biquad per Channel) | DAC_DSP_BQ_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel) | DAC_DSP_BQ_CFG[1:0] = 2'b11 (3 Biquads per Channel) |
| Biquad filter 11 | Not used | Not used | Allocated to output channel 3 |
| Biquad filter 12 | Not used | Not used | Allocated to output channel 4 |

Table 7-17 shows the biquad filter coefficients mapping to the register space.

**Table 7-17. Biquad Filter Coefficients Register Mapping**

| PROGRAMMABLE BIQUAD FILTER | BIQUAD FILTER COEFFICIENTS REGISTER MAPPING | PROGRAMMABLE BIQUAD FILTER | BIQUAD FILTER COEFFICIENTS REGISTER MAPPING |
|---|---|---|---|
| Biquad filter 1 | P16_R8-R27 | Biquad filter 7 | P17_R8-R27 |
| Biquad filter 2 | P16_R28-R47 | Biquad filter 8 | P17_R28-R47 |
| Biquad filter 3 | P16_R48-R67 | Biquad filter 9 | P17_R48-R67 |
| Biquad filter 4 | P16_R68-R87 | Biquad filter 10 | P17_R68-R87 |
| Biquad filter 5 | P16_R88-R107 | Biquad filter 11 | P17_R88-R107 |
| Biquad filter 6 | P16_R108-R127 | Biquad filter 12 | P17_R108-R127 |

### 7.3.1.8.1.5 Programmable Digital Mixer

The device supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels.

### 7.3.1.8.1.6 Configurable Digital Interpolation Filters

The device playback channel includes a high dynamic range, built-in digital interpolation filter to process the input data stream to generate digital data stream for multibit delta-sigma (ΔΣ) modulator. The interpolation filter can be chosen from four different types, depending on the required frequency response, group delay, power consumption, and phase linearity requirements for the target application. The selection of the interpolation filter option can be done by configuring the DAC_DSP_INTX_FILT, P0_R115_D[7:6] register bits. Low power filter can be configured by setting DAC_LOW_PWR_FILT, P0_R79_D2 bit. Table 7-18 shows the configuration register setting for the decimation filter mode selection for the record channel.

**Table 7-18. Interpolation Filter Mode Selection for the Playback Channel**

| P0_R79_D2 : DAC_LOW_PWR_FILT | P0_R115_D[7:6] : DAC_DSP_INTX_FILT[1:0] | INTERPOLATION FILTER MODE SELECTION |
|---|---|---|
| 0 | 00 (default) | Linear phase filters are used for the interpolation |
| 0 | 01 | Low latency filters are used for the interpolation |
| 0 | 10 | Ultra-low latency filters are used for the interpolation |
| 0 | 11 | Reserved (do not use this setting) |
| 1 | x | Low power filters are used for the interpolation |

### 7.3.1.8.1.6.1 Linear Phase Filters

The linear phase interpolation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

**ADVANCE INFORMATION**

#### 7.3.1.8.1.6.1.1 Sampling Rate: 16 kHz or 14.7 kHz

Figure 7-17 and Figure 7-18 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 16 kHz or 14.7 kHz. Table 7-19 lists the specifications for a interpolation filter with an 16-kHz or 14.7-kHz sampling rate.



**Figure 7-17. Linear Phase Interpolation Filter Magnitude Response**



**Figure 7-18. Linear Phase Interpolation Filter Pass-Band Ripple**

**Table 7-19. Linear Phase Interpolation Filter Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Pass-band ripple | Frequency range is 0 to 0.454 × $f_S$ | –0.17 | | 0.03 | dB |
| Stop-band attenuation | Frequency range is 0.6 × $f_S$ to 4 × $f_S$ | 80.4 | | | dB |
| | Frequency range is 4 × $f_S$ to 7.43 × $f_S$ | 86.9 | | | |
| Group delay or latency | Frequency range is 0 to 0.454 × $f_S$ | | 16.0 | | 1/$f_S$ |

#### 7.3.1.8.1.6.1.2 Sampling Rate: 24 kHz or 22.05 kHz

Figure 7-19 and Figure 7-20 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 24 kHz or 22.05 kHz. Table 7-20 lists the specifications for a interpolation filter with an 24-kHz or 22.05-kHz sampling rate.



**Figure 7-19. Linear Phase Interpolation Filter Magnitude Response**



**Figure 7-20. Linear Phase Interpolation Filter Pass-Band Ripple**

**Table 7-20. Linear Phase Interpolation Filter Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Pass-band ripple | Frequency range is 0 to 0.454 × $f_S$ | –0.05 | | 0.03 | dB |
| Stop-band attenuation | Frequency range is 0.58 × $f_S$ to 4 × $f_S$ | 81.9 | | | dB |
| | Frequency range is 4 × $f_S$ to 15.42 × $f_S$ | 87.6 | | | |

Product Folder Links: *TAD5212*

**Table 7-20. Linear Phase Interpolation Filter Specifications (continued)**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Group delay or latency | Frequency range is 0 to 0.454 × $f_S$ | | 17.6 | | 1/$f_S$ |

### 7.3.1.8.1.6.1.3 Sampling Rate: 32 kHz or 29.4 kHz

Figure 7-21 and Figure 7-22 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 32 kHz or 29.4 kHz. Table 7-21 lists the specifications for a interpolation filter with an 32-kHz or 29.4-kHz sampling rate.



**Figure 7-21. Linear Phase Interpolation Filter Magnitude Response**



**Figure 7-22. Linear Phase Interpolation Filter Pass-Band Ripple**
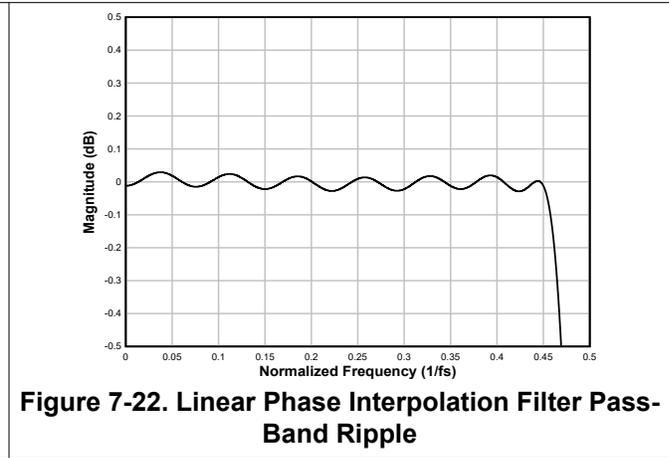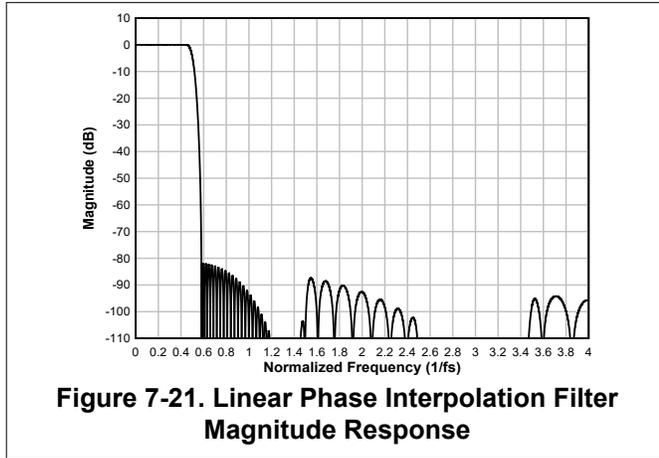
**Table 7-21. Linear Phase Interpolation Filter Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Pass-band ripple | Frequency range is 0 to 0.454 × $f_S$ | −0.05 | | 0.03 | dB |
| Stop-band attenuation | Frequency range is 0.586 × $f_S$ to 4 × $f_S$ | 81.9 | | | dB |
| | Frequency range is 4 × $f_S$ to 15.42 × $f_S$ | 87.6 | | | |
| Group delay or latency | Frequency range is 0 to 0.454 × $f_S$ | | 17.6 | | 1/$f_S$ |

### 7.3.1.8.1.6.1.4 Sampling Rate: 48 kHz or 44.1 kHz

Figure 7-23 and Figure 7-24 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 48 kHz or 44.1 kHz. Table 7-22 lists the specifications for a interpolation filter with an 48-kHz or 44.1-kHz sampling rate.



**Figure 7-23. Linear Phase Interpolation Filter Magnitude Response**



**Figure 7-24. Linear Phase Interpolation Filter Pass-Band Ripple**
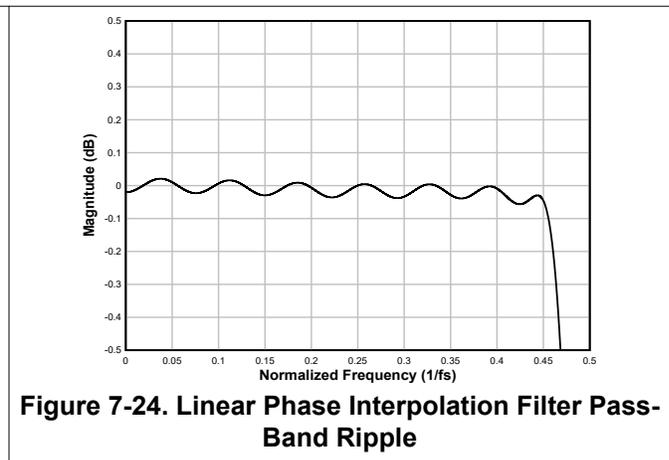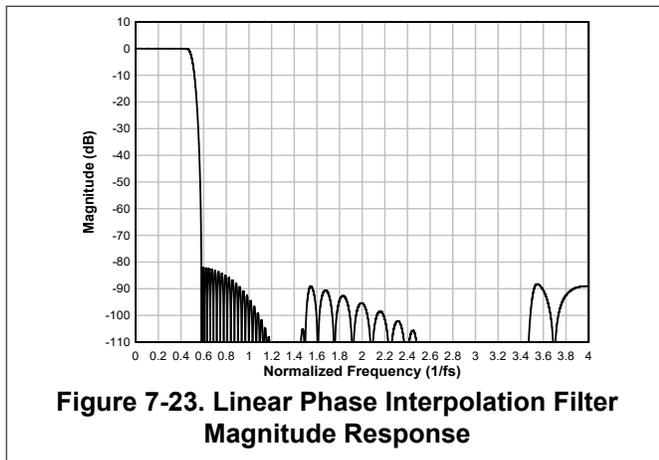
**Table 7-22. Linear Phase Interpolation Filter Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Pass-band ripple | Frequency range is 0 to 0.454 × f$_S$ | −0.08 | | 0.02 | dB |
| Stop-band attenuation | Frequency range is 0.585 × f$_S$ to 4 × f$_S$ | 82.0 | | | dB |
| | Frequency range is 4 × f$_S$ to 7.42 × f$_S$ onwards | 89.0 | | | |
| Group delay or latency | Frequency range is 0 to 0.454 × f$_S$ | | 17.3 | | 1/f$_S$ |

### 7.3.1.8.1.6.1.5 Sampling Rate: 96 kHz or 88.2 kHz

Figure 7-25 and Figure 7-26 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 96 kHz or 88.2 kHz. Table 7-23 lists the specifications for a interpolation filter with an 96-kHz or 88.2-kHz sampling rate.
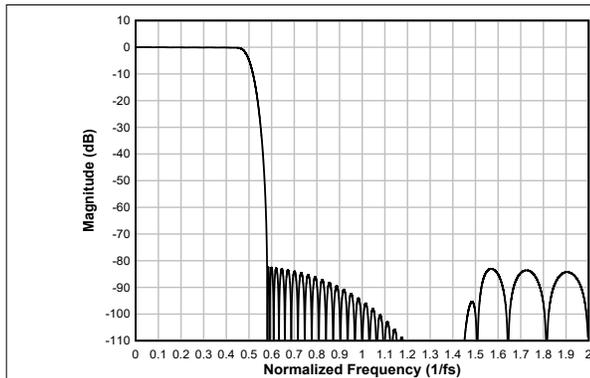


**Figure 7-25. Linear Phase Interpolation Filter Magnitude Response**
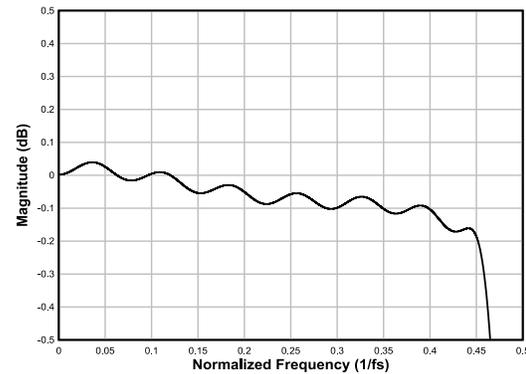


**Figure 7-26. Linear Phase Interpolation Filter Pass-Band Ripple**

**Table 7-23. Linear Phase Interpolation Filter Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Pass-band ripple | Frequency range is 0 to 0.452 × f$_S$ | −0.2 | | 0.04 | dB |
| Stop-band attenuation | Frequency range is 0.58 × f$_S$ to 3.42 × f$_S$ | 82.4 | | | dB |
| Group delay or latency | Frequency range is 0 to 0.454 × f$_S$ | | 16.7 | | 1/f$_S$ |

### 7.3.1.8.1.6.1.6 Sampling Rate: 384 kHz or 352.8 kHz

Figure 7-27 and Figure 7-28 respectively show the magnitude response and the pass-band ripple for a interpolation filter with a sampling rate of 384 kHz or 352.8 kHz. Table 7-24 lists the specifications for a interpolation filter with an 384-kHz or 352.8-kHz sampling rate.

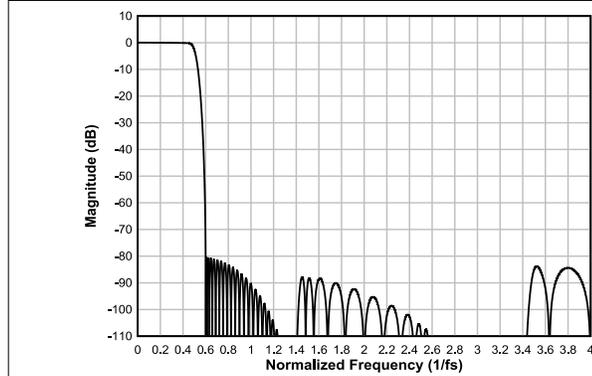Product Folder Links: *TAD5212*

ADVANCE INFORMATION
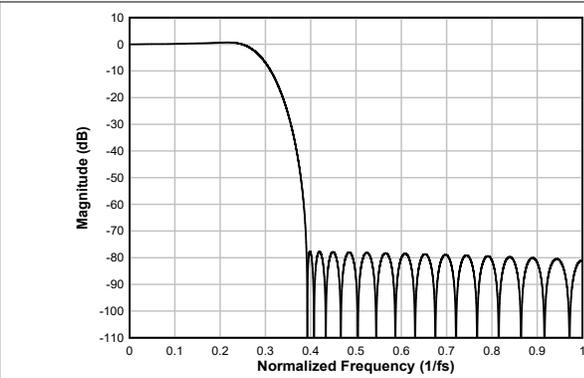
**Figure 7-27. Linear Phase Interpolation Filter Magnitude Response**
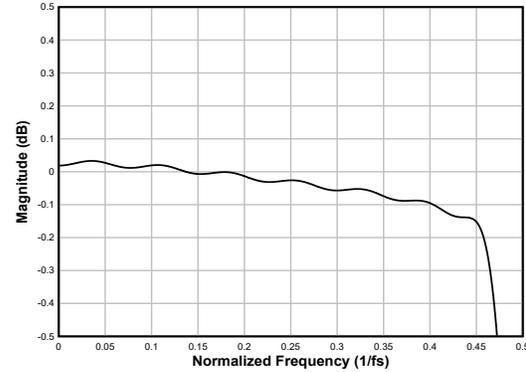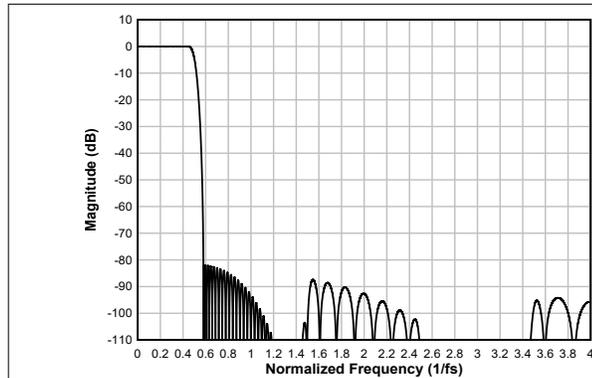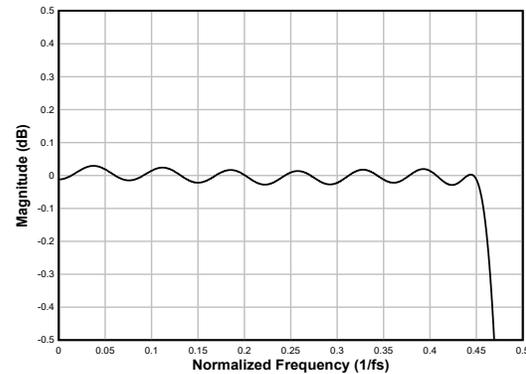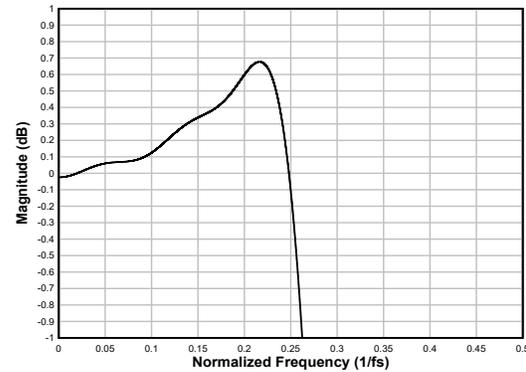


**Figure 7-28. Linear Phase Interpolation Filter Pass-Band Ripple**

**Table 7-24. Linear Phase Interpolation Filter Specifications**

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| Pass-band ripple | Frequency range is 0 to 0.245 × $f_S$ | −0.03 | | 0.67 | dB |
| Stop-band attenuation | Frequency range is 0.391 × $f_S$ to 1.61 × $f_S$ | 77.6 | | | dB |
| Group delay or latency | Frequency range is 0 to 0.212 × $f_S$ | | 10.7 | | 1/$f_S$ |

### 7.3.1.9 Interrupts, Status, and Digital I/O Pin Multiplexing

Certain events in the device may require host processor intervention and can be used to trigger interrupts to the host processor. One such event is an audio serial interface (ASI) bus error. The device powers down the record channels if any faults are detected with the ASI bus error clocks, such as:

• Invalid FSYNC frequency
• Invalid SBCLK to FSYNC ratio
• Long pauses of the SBCLK or FSYNC clocks

When an ASI bus clock error is detected, the device shuts down all the record and playback channels as quickly as possible. After all ASI bus clock errors are resolved, the device volume ramps back to its previous state to recover the audio. During an ASI bus clock error, the internal interrupt request (IRQ) interrupt signal asserts low if the clock error interrupt mask register bit INT_MASK0[7] (P1_R47_D7) is set low. The clock fault is also available for readback in the latched fault status register bit INT_LTCH0 (P1_R52), which is a read-only register. Reading the latched fault status register, INT_LTCH0, clears all latched fault status. The device can be additionally configured to route the internal IRQ interrupt signal on the GPIOx or GPO1 pins and also can be configured as open-drain outputs so that these pins can be wire-ANDed to the open-drain interrupt outputs of other devices.

The IRQ interrupt signal can either be configured as active low or active high polarity by setting the INT_POL (P0_R66_D7) register bit. This signal can also be configured as a single pulse or a series of pulses by programming the INT_EVENT[1:0] (P0_R66_D[6:5]) register bits. If the interrupts are configured as a series of pulses, the events trigger the start of pulses that stop when the latched fault status register is read to determine the cause of the interrupt.

The device also supports read-only live-status registers to determine if the channels are powered up or down and if the device is in sleep mode or not. These status registers are located in the DEV_STS0 (P0_R121) and DEV_STS1 (P0_R122) register bits.

The device has a multifunctional GPIO1 pin that can be configured for a desired specific function. Table 7-25 lists all possible allocations of these multifunctional pins for the various features.

Product Folder Links: TAD5212

**ADVANCE INFORMATION**

**Table 7-25. Multifunction Pin Assignments**

| ROW | PIN FUNCTION | GPIO1 | GPIO2 | GPO1 | GPI1 |
|---|---|---|---|---|---|
| — | — | GPIO1_CFG | GPO2_CFG | GPO1_CFG | GPI1_CFG |
| — | — | P0_R10[7:4] | P0_R11[7:4] | P0_R12[7:4] | P0_R13[1] |
| A | Pin disabled | S[1] | S (default) | S (default) | S (default) |
| B | General-purpose output (GPO) | S | S | S | NS |
| C | Interrupt output (IRQ) | S (default) | S | S | NS |
| D | PDM clock output (PDMCLK) | S | S | S | NS |
| E | MiCBIAS on/off input (BIASEN) | S | S | NS | S |
| F | General-purpose input (GPI) | S | S | NS | S |
| G | Controller clock input (CCLK) | S | S | S | S |
| H | ASI daisy-chain input | S | S | NS | S |
| I | ASI DOUT | S | S | S | NS |
| J | ASI BCLK | S | S | S | S |
| K | ASI FSYNC | S | S | S | S |
| L | General Purpose Clock Out | S | S | S | NS |
| M | ASI daisy-chain output | S | S | S | NS |

(1)    S means the feature mentioned in this row is *supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.

Each GPOx or GPIOx pin can be independently set for the desired drive configurations setting using the GPIOx_DRV[2:0] or GPO1_DRV[2:0] register bits. Table 7-26 lists the drive configuration settings.

**Table 7-26. GPIO or GPOx Pins Drive Configuration Settings**

| P0_R10_D[2:0] : GPIO1_DRV[2:0] | GPIO OUTPUT DRIVE CONFIGURATION SETTINGS FOR GPIO1 |
|---|---|
| 000 | The GPIO1 pin is set to high impedance (floated) |
| 001 | The GPIO1 pin is set to be driven active low or active high |
| 010 (default) | The GPIO1 pin is set to be driven active low or weak high (on-chip pullup) |
| 011 | The GPIO1 pin is set to be driven active low or Hi-Z (floated) |
| 100 | The GPIO1 pin is set to be driven weak low (on-chip pulldown) or active high |
| 101 | The GPIO1 pin is set to be driven Hi-Z (floated) or active high |
| 110 and 111 | Reserved (do not use these settings) |

Similarly, the GPO1 pin can be configured using the GPO1_DRV(P0_R12) register bits.

When configured as a general-purpose output (GPO), the GPIOx or GPO1 pin values can be driven by writing the GPO_GPI_VAL (P0_R14) registers. The GPIO_MON bits (P0_R14_D[3:1]) can be used to readback the status of the GPIOx or GPI1 pin when configured as a general-purpose input (GPI).

## 7.4 Device Functional Modes

## 7.5 Register Maps

This section describes the control registers for the device in detail. All these registers are eight bits in width and allocated to device configuration and programmable coefficients settings. These registers are mapped internally using a page scheme that can be controlled using either I²C or SPI communication to the device. Each page contains 128 bytes of registers. All device configuration registers are stored in page 0, page 1 and page 3. Page 0 is the default page setting at power up (and after a software reset). The device current page can be switch to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

Do not read from or write to reserved pages or reserved registers. Write only default values for the reserved bits in the valid registers.

The procedure for register access across pages is:
• Select page N (write data *N* to register 0 regardless of the current page number)
• Read or write data from or to valid registers in page N

ADVANCE INFORMATION

- Select the new page M (write data *M* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

**ADVANCE INFORMATION**

### 7.5.1 TAD5212_P0 Registers

Table 7-27 lists the memory-mapped registers for the TAD5212_P0 registers. All register offset addresses not listed in Table 7-27 should be considered as reserved locations and the register contents should not be modified.

#### Table 7-27. TAD5212_P0 Registers

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x0 | PAGE_CFG | Device page register | 0x00 | PAGE_CFG Register (Address = 0x0) [Reset = 0x00] |
| 0x1 | SW_RESET | Software reset register | 0x00 | SW_RESET Register (Address = 0x1) [Reset = 0x00] |
| 0x2 | VREF_CFG | | 0x00 | VREF_CFG Register (Address = 0x2) [Reset = 0x00] |
| 0x3 | AVDD_IOVDD_STS | | 0x00 | AVDD_IOVDD_STS Register (Address = 0x3) [Reset = 0x00] |
| 0x4 | MISC_CFG | | 0x00 | MISC_CFG Register (Address = 0x4) [Reset = 0x00] |
| 0x5 | MISC_CFG1 | | 0x15 | MISC_CFG1 Register (Address = 0x5) [Reset = 0x15] |
| 0x6 | DAC_CFG_A0 | DAC DEPOP configuration register | 0x55 | DAC_CFG_A0 Register (Address = 0x6) [Reset = 0x55] |
| 0x7 | MISC_CFG0 | Misc. configuration register | 0x00 | MISC_CFG0 Register (Address = 0x7) [Reset = 0x00] |
| 0xA | GPIO1_CFG0 | GPIO1 configuration register 0 | 0x32 | GPIO1_CFG0 Register (Address = 0xA) [Reset = 0x32] |
| 0xB | GPIO2_CFG0 | GPIO2 configuration register 0 | 0x00 | GPIO2_CFG0 Register (Address = 0xB) [Reset = 0x00] |
| 0xC | GPO1_CFG0 | GPO1 configuration register 0 | 0x00 | GPO1_CFG0 Register (Address = 0xC) [Reset = 0x00] |
| 0xD | GPI_CFG | GPI1 configuration register 0 | 0x00 | GPI_CFG Register (Address = 0xD) [Reset = 0x00] |
| 0xE | GPO_GPI_VAL | GPIO, GPO output value register | 0x00 | GPO_GPI_VAL Register (Address = 0xE) [Reset = 0x00] |
| 0xF | INTF_CFG0 | Interface configuration register 0 | 0x00 | INTF_CFG0 Register (Address = 0xF) [Reset = 0x00] |
| 0x10 | INTF_CFG1 | Interface configuration register 1 | 0x52 | INTF_CFG1 Register (Address = 0x10) [Reset = 0x52] |
| 0x11 | INTF_CFG2 | Interface configuration register 2 | 0x80 | INTF_CFG2 Register (Address = 0x11) [Reset = 0x80] |
| 0x12 | INTF_CFG3 | Interface configuration register 3 | 0x00 | INTF_CFG3 Register (Address = 0x12) [Reset = 0x00] |

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

### Table 7-27. TAD5212_P0 Registers (continued)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x14 | INTF_CFG5 | Interface configuration register 4 | 0x00 | INTF_CFG5 Register (Address = 0x14) [Reset = 0x00] |
| 0x18 | ASI_CFG0 | ASI configuration register 0 | 0x40 | ASI_CFG0 Register (Address = 0x18) [Reset = 0x40] |
| 0x19 | ASI_CFG1 | ASI configuration register 1 | 0x00 | ASI_CFG1 Register (Address = 0x19) [Reset = 0x00] |
| 0x1A | PASI_CFG0 | Primary ASI configuration register 0 | 0x30 | PASI_CFG0 Register (Address = 0x1A) [Reset = 0x30] |
| 0x1B | PASI_TX_CFG0 | PASI TX configuration register 0 | 0x00 | PASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00] |
| 0x1C | PASI_TX_CFG1 | PASI TX configuration register 1 | 0x00 | PASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00] |
| 0x1D | PASI_TX_CFG2 | PASI TX configuration register 2 | 0x00 | PASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00] |
| 0x20 | PASI_TX_CH3_CFG | PASI TX Channel 3 configuration register | 0x02 | PASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02] |
| 0x21 | PASI_TX_CH4_CFG | PASI TX Channel 4 configuration register | 0x03 | PASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03] |
| 0x22 | PASI_TX_CH5_CFG | PASI TX Channel 5 configuration register | 0x04 | PASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04] |
| 0x23 | PASI_TX_CH6_CFG | PASI TX Channel 6 configuration register | 0x05 | PASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05] |
| 0x24 | PASI_TX_CH7_CFG | PASI TX Channel 7 configuration register | 0x06 | PASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06] |
| 0x25 | PASI_TX_CH8_CFG | PASI TX Channel 8 configuration register | 0x07 | PASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07] |
| 0x26 | PASI_RX_CFG0 | PASI RX configuration register 0 | 0x00 | PASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00] |
| 0x27 | PASI_RX_CFG1 | PASI RX configuration register 1 | 0x00 | PASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00] |
| 0x28 | PASI_RX_CH1_CFG | PASI RX Channel 1 configuration register | 0x20 | PASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x20] |
| 0x29 | PASI_RX_CH2_CFG | PASI RX Channel 2 configuration register | 0x21 | PASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x21] |

**ADVANCE INFORMATION**

**Table 7-27. TAD5212_P0 Registers (continued)**

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x2A | PASI_RX_CH3_CFG | PASI RX Channel 3 configuration register | 0x02 | PASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02] |
| 0x2B | PASI_RX_CH4_CFG | PASI RX Channel 4 configuration register | 0x03 | PASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03] |
| 0x2C | PASI_RX_CH5_CFG | PASI RX Channel 5 configuration register | 0x04 | PASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04] |
| 0x2D | PASI_RX_CH6_CFG | PASI RX Channel 6 configuration register | 0x05 | PASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05] |
| 0x2E | PASI_RX_CH7_CFG | PASI RX Channel 7 configuration register | 0x06 | PASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06] |
| 0x2F | PASI_RX_CH8_CFG | PASI RX Channel 8 configuration register | 0x07 | PASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07] |
| 0x32 | CLK_CFG0 | Clock configuration register 0 | 0x00 | CLK_CFG0 Register (Address = 0x32) [Reset = 0x00] |
| 0x33 | CLK_CFG1 | Clock configuration register 1 | 0x00 | CLK_CFG1 Register (Address = 0x33) [Reset = 0x00] |
| 0x34 | CLK_CFG2 | Clock configuration register 2 | 0x40 | CLK_CFG2 Register (Address = 0x34) [Reset = 0x40] |
| 0x35 | CNT_CLK_CFG0 | controller mode clock configuration register 0 | 0x00 | CNT_CLK_CFG0 Register (Address = 0x35) [Reset = 0x00] |
| 0x36 | CNT_CLK_CFG1 | controller mode clock configuration register 1 | 0x00 | CNT_CLK_CFG1 Register (Address = 0x36) [Reset = 0x00] |
| 0x37 | CNT_CLK_CFG2 | controller mode clock configuration register 2 | 0x20 | CNT_CLK_CFG2 Register (Address = 0x37) [Reset = 0x20] |
| 0x38 | CNT_CLK_CFG3 | controller mode clock configuration register 3 | 0x00 | CNT_CLK_CFG3 Register (Address = 0x38) [Reset = 0x00] |
| 0x39 | CNT_CLK_CFG4 | controller mode clock configuration register 4 | 0x00 | CNT_CLK_CFG4 Register (Address = 0x39) [Reset = 0x00] |
| 0x3A | CNT_CLK_CFG5 | controller mode clock configuration register 5 | 0x00 | CNT_CLK_CFG5 Register (Address = 0x3A) [Reset = 0x00] |
| 0x3B | CNT_CLK_CFG6 | controller mode clock configuration register 6 | 0x00 | CNT_CLK_CFG6 Register (Address = 0x3B) [Reset = 0x00] |

**ADVANCE INFORMATION**

Product Folder Links: *TAD5212*

**Table 7-27. TAD5212_P0 Registers (continued)**

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x3C | CLK_ERR_STS0 | Clock error and status register 0 | 0x00 | CLK_ERR_STS0 Register (Address = 0x3C) [Reset = 0x00] |
| 0x3D | CLK_ERR_STS1 | Clock error and status register 1 | 0x00 | CLK_ERR_STS1 Register (Address = 0x3D) [Reset = 0x00] |
| 0x3E | CLK_DET_STS0 | Clock ratio detection register 0 | 0x00 | CLK_DET_STS0 Register (Address = 0x3E) [Reset = 0x00] |
| 0x3F | CLK_DET_STS1 | Clock ratio detection register 1 | 0x00 | CLK_DET_STS1 Register (Address = 0x3F) [Reset = 0x00] |
| 0x40 | CLK_DET_STS2 | Clock ratio detection register 2 | 0x00 | CLK_DET_STS2 Register (Address = 0x40) [Reset = 0x00] |
| 0x41 | CLK_DET_STS3 | Clock ratio detection register 3 | 0x00 | CLK_DET_STS3 Register (Address = 0x41) [Reset = 0x00] |
| 0x42 | INT_CFG | Interrupt configuration register | 0x00 | INT_CFG Register (Address = 0x42) [Reset = 0x00] |
| 0x43 | DAC_FLT_CFG | Interrupt configuration register | 0x50 | DAC_FLT_CFG Register (Address = 0x43) [Reset = 0x50] |
| 0x4F | PWR_TUNE_CFG1 | Power tune configuration register 1 | 0x00 | PWR_TUNE_CFG1 Register (Address = 0x4F) [Reset = 0x00] |
| 0x64 | OUT1x_CFG0 | Channel OUT1x configuration register 0 | 0x20 | OUT1x_CFG0 Register (Address = 0x64) [Reset = 0x20] |
| 0x65 | OUT1x_CFG1 | Channel OUT1x configuration register 1 | 0x20 | OUT1x_CFG1 Register (Address = 0x65) [Reset = 0x20] |
| 0x66 | OUT1x_CFG2 | Channel OUT2x configuration register 2 | 0x20 | OUT1x_CFG2 Register (Address = 0x66) [Reset = 0x20] |
| 0x67 | DAC_CH1A_CFG0 | DAC Channel 1A configuration register 0 | 0xC9 | DAC_CH1A_CFG0 Register (Address = 0x67) [Reset = 0xC9] |
| 0x68 | DAC_CH1A_CFG1 | DAC Channel 1A configuration register 1 | 0x80 | DAC_CH1A_CFG1 Register (Address = 0x68) [Reset = 0x80] |
| 0x69 | DAC_CH1B_CFG0 | DAC Channel 1B configuration register 0 | 0xC9 | DAC_CH1B_CFG0 Register (Address = 0x69) [Reset = 0xC9] |
| 0x6A | DAC_CH1B_CFG1 | DAC Channel 1B configuration register 1 | 0x80 | DAC_CH1B_CFG1 Register (Address = 0x6A) [Reset = 0x80] |
| 0x6B | OUT2x_CFG0 | Channel OUT2x configuration register 0 | 0x20 | OUT2x_CFG0 Register (Address = 0x6B) [Reset = 0x20] |

ADVANCE INFORMATION

**Table 7-27. TAD5212_P0 Registers (continued)**

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x6C | OUT2x_CFG1 | Channel OUT2x configuration register 1 | 0x20 | OUT2x_CFG1 Register (Address = 0x6C) [Reset = 0x20] |
| 0x6D | OUT2x_CFG2 | Channel OUT2x configuration register 2 | 0x20 | OUT2x_CFG2 Register (Address = 0x6D) [Reset = 0x20] |
| 0x6E | DAC_CH2A_CFG0 | DAC Channel 2A configuration register 0 | 0xC9 | DAC_CH2A_CFG0 Register (Address = 0x6E) [Reset = 0xC9] |
| 0x6F | DAC_CH2A_CFG1 | DAC Channel 2A configuration register 1 | 0x80 | DAC_CH2A_CFG1 Register (Address = 0x6F) [Reset = 0x80] |
| 0x70 | DAC_CH2B_CFG0 | DAC Channel 2B configuration register 0 | 0xC9 | DAC_CH2B_CFG0 Register (Address = 0x70) [Reset = 0xC9] |
| 0x71 | DAC_CH2B_CFG1 | DAC Channel 2B configuration register 1 | 0x80 | DAC_CH2B_CFG1 Register (Address = 0x71) [Reset = 0x80] |
| 0x73 | DSP_CFG1 | DSP configuration register 0 | 0x18 | DSP_CFG1 Register (Address = 0x73) [Reset = 0x18] |
| 0x76 | CH_EN | Channel enable configuration register | 0xCC | CH_EN Register (Address = 0x76) [Reset = 0xCC] |
| 0x77 | DYN_PUPD_CFG | Power up configuration register | 0x00 | DYN_PUPD_CFG Register (Address = 0x77) [Reset = 0x00] |
| 0x78 | PWR_CFG | Power up configuration register | 0x00 | PWR_CFG Register (Address = 0x78) [Reset = 0x00] |
| 0x79 | DEV_STS0 | Device status value register 0 | 0x00 | DEV_STS0 Register (Address = 0x79) [Reset = 0x00] |
| 0x7A | DEV_STS1 | Device status value register 1 | 0x80 | DEV_STS1 Register (Address = 0x7A) [Reset = 0x80] |
| 0x7E | I2C_CKSUM | I²C checksum register | 0x00 | I2C_CKSUM Register (Address = 0x7E) [Reset = 0x00] |

### 7.5.1.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in Table 7-28.

Return to the Summary Table.

The device memory map is divided into pages. This register sets the page.

<div style="writing-mode: vertical">ADVANCE INFORMATION</div>

**Table 7-28. PAGE_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PAGE[7:0] | R/W | 00000000b | These bits set the device page.<br>0d = Page 0<br>1d = Page 1<br>2d to 254d = Page 2 to page 254 respectively<br>255d = Page 255 |

### 7.5.1.2 SW_RESET Register (Address = 0x1) [Reset = 0x00]

SW_RESET is shown in Table 7-29.

Return to the Summary Table.

This register is the software reset register. Asserting a software reset places all register values in their default power-on-reset (POR) state.

**Table 7-29. SW_RESET Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | RESERVED | R | 0000000b | Reserved bits; Write only reset value |
| 0 | SW_RESET | R/W | 0b | Software reset. This bit is self clearing.<br>0d = Do not reset<br>1d = Reset all registers to their reset values |

### 7.5.1.3 VREF_CFG Register (Address = 0x2) [Reset = 0x00]

VREF_CFG is shown in Table 7-30.

Return to the Summary Table.

**Table 7-30. VREF_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 5-4 | VREF_QCHG[1:0] | R/W | 00b | The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω.<br>0d = VREF quick-charge duration of 3.5 ms (typical)<br>1d = VREF quick-charge duration of 10 ms (typical)<br>2d = VREF quick-charge duration of 50 ms (typical)<br>3d = VREF quick-charge duration of 100 ms (typical) |
| 3 | SLEEP_EXIT_VREF_EN | R/W | 0b | Sleep mode exit configuration<br>0d = Only DREG Enabled<br>1d = DREG and VREF enabled |
| 2 | AVDD_MODE | R/W | 0b | AVDD mode configuration.<br>0d = Internal AREG regulator is used (Should be used for AVDD > 2V)<br>1d = AVDD 1.8V used directly for AREG (Strictly use this setting for AVDD 1.7V-1.9V) |
| 1 | IOVDD_IO_MODE | R/W | 0b | IOVDD mode configuration.<br>0d = IOVDD at 3.3V / 1.8V / 1.2V (speed limitation applicable for 1.8V and 1.2V)<br>1d = IOVDD at 1.8V / 1.2V only (no speed limitation - Strictly don't use this setting for IOVDD > 2V). |
| 0 | SLEEP_ENZ | R/W | 0b | Sleep mode setting.<br>0d = Device is in sleep mode<br>1d = Device is not in sleep mode |

**ADVANCE INFORMATION**

### 7.5.1.4 AVDD_IOVDD_STS Register (Address = 0x3) [Reset = 0x00]

AVDD_IOVDD_STS is shown in Table 7-31.

Return to the Summary Table.

**Table 7-31. AVDD_IOVDD_STS Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | AVDD_MODE_STS | R | 0b | AVDD mode status flag register.<br>0d = AVDD_MODE as per configured<br>1d = AVDD > 2V (AVDD_MODE forced to 0d) |
| 6 | IOVDD_IO_MODE_STS | R | 0b | IOVDD mode status flag register.<br>0d = IOVDD_MODE as per configured<br>1d = IOVDD > 2V (IOVDD_IO_MODE forced to 0d) |
| 5-2 | RESERVED | R | 0000b | Reserved bits; Write only reset values |
| 1 | BRWNOUT_SHDN_STS | R | 0b | Brwnout shutdown status<br>0d = No brwnout shutdown<br>1d = Brwnout shutdown |
| 0 | BRWNOUT_SHDN_EXIT_SLEEP | R/W | 0b | Brwnout shutdown sleep exit config<br>0d = Stay in sleep mode<br>1d = Exit sleep mode |

### 7.5.1.5 MISC_CFG Register (Address = 0x4) [Reset = 0x00]

MISC_CFG is shown in Table 7-32.

Return to the Summary Table.

**Table 7-32. MISC_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | IGNORE_CLK_ERR | R/W | 0b | Clock error detection action<br>0b = Shutdown on Clock error<br>1b = Ignore Clock error |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | I2C_BRDCAST_EN | R/W | 0b | I$^2$C broadcast addressing setting.<br>0d = I$^2$C broadcast mode disabled<br>1d = I$^2$C broadcast mode enabled; the I$^2$C target address is fixed with pin-controlled LSB bits as '0' |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

### 7.5.1.6 MISC_CFG1 Register (Address = 0x5) [Reset = 0x15]

MISC_CFG1 is shown in Table 7-33.

Return to the Summary Table.

**Table 7-33. MISC_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | INCAP_QCHG[1:0] | R/W | 00b | The duration of the quick-charge for the external AC-coupling capacitor is set using an internal series impedance of 800 Ω.<br>0d = INxP, INxM quick-charge duration of 2.5 ms (typical)<br>1d = INxP, INxM quick-charge duration of 12.5 ms (typical)<br>2d = INxP, INxM quick-charge duration of 25 ms (typical)<br>3d = INxP, INxM quick-charge duration of 50 ms (typical) |

**Table 7-33. MISC_CFG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 5-4 | SHDN_CFG[1:0] | R/W | 01b | Shutdown configuration.<br>0d = DREG is powered down immediately after IOVDD is deasserted<br>1d = DREG remains active to enable a clean shut down until a time-out(DREG_KA_TIME) is reached; after the time-out period, DREG is forced to power off<br>2d = DREG remains active until the device cleanly shuts down<br>3d = Reserved; Don't use |
| 3-2 | DREG_KA_TIME[1:0] | R/W | 01b | These bits set how long DREG remains active after IOVDD is deasserted.<br>0d = DREG remains active for 30 ms (typical)<br>1d = DREG remains active for 25 ms (typical)<br>2d = DREG remains active for 10 ms (typical)<br>3d = DREG remains active for 5 ms (typical) |
| 1-0 | RESERVED | R/W | 01b | Reserved bits; Write only reset values |

### 7.5.1.7 DAC_CFG_A0 Register (Address = 0x6) [Reset = 0x55]

DAC_CFG_A0 is shown in Table 7-34.

Return to the Summary Table.

This register configures the device DAC DEPOP

**Table 7-34. DAC_CFG_A0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | RSERIES_DE_POP[3:0] | R/W | 0101b | HP Amp series resistor select config.<br>0d = Open<br>1d = 1K<br>2d = 2.5K<br>3d = 0.715k<br>4d = 10K<br>5d = 0.91k<br>6d = 2K<br>7d = 0.667k<br>8d = 20K<br>Dont use<br>Dont use<br>Dont use<br>Dont use<br>Dont use<br>Dont use<br>Dont use |
| 3-0 | PWR_UP_TIME_DE_POP[3:0] | R/W | 0101b | HP Amp external cap charging time config.<br>0d = 2ms<br>1d = 4ms<br>2d = 8ms<br>3d = 16ms<br>4d = 50ms<br>5d = 100ms<br>6d = 250ms<br>7d = 500ms<br>8d = 1s<br>9d = 5s<br>10d-15d = Reserved |

### 7.5.1.8 MISC_CFG0 Register (Address = 0x7) [Reset = 0x00]

MISC_CFG0 is shown in Table 7-35.

Return to the Summary Table.

**ADVANCE INFORMATION**

TEXAS INSTRUMENTS
www.ti.com

This register configures the device Misc.

**Table 7-35. MISC_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | DAC_ST_W_CAP_DIS | R/W | 0b | DAC start with dc blocking capacitor discharge sequence.<br>0d = disable<br>1d = enable |
| 6 | DAC_DLYD_PWRUP | R/W | 0b | DAC power up delayed config.<br>0d = disable<br>1d = enable (Delay power-up by based on DAC_DLYD_PWRUP_TIME config) |
| 5 | DAC_DLYD_PWRUP_TIME | R/W | 0b | DAC power up delayed time config.<br>0d = 128ms<br>1d = 512ms |
| 4 | HW_RESET_ON_CLK_STOP_EN | R/W | 0b | Assertion of Hard Reset when clock selected by CLK_SRC_SEL is not available for 2ms config<br>0d = disable<br>1d = enable |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset values |

**7.5.1.9 GPIO1_CFG0 Register (Address = 0xA) [Reset = 0x32]**

GPIO1_CFG0 is shown in Table 7-36.

Return to the Summary Table.

This register is the GPIO1 configuration register 0.

**Table 7-36. GPIO1_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | GPIO1_CFG[3:0] | R/W | 0011b | GPIO1 configuration.<br>0d = GPIO1 is disabled<br>1d = GPIO1 is configured as a general-purpose input (GPI) or any other input function<br>2d = GPIO1 is configured as a general-purpose output (GPO)<br>3d = GPIO1 is configured as a chip interrupt output (IRQ)<br>4d = GPIO1 is configured as a PDM clock output (PDMCLK)<br>5d = GPIO1 is configured as primary ASI DOUT<br>6d = GPIO1 is configured as primary ASI DOUT2<br>7d = GPIO1 is configured as secondary ASI DOUT<br>8d = GPIO1 is configured as secondary ASI DOUT2<br>9d = GPIO1 is configured as secondary ASI BCLK output<br>10d = GPIO1 is configured as secondary ASI FSYNC output<br>11d = GPIO1 is configured as general purpose CLKOUT<br>12d = GPIO1 is configured as PASI DOUT and SASI DOUT muxed<br>13d = GPIO1 is configured as DAISY_OUT for DIN Daisy<br>14d to 15d = Reserved |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2-0 | GPIO1_DRV[2:0] | R/W | 010b | GPIO1 output drive configuration. (Not valid if GPIO1_CFG configured as I$^2$S out)<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Drive active low and weak high<br>3d = Drive active low and Hi-Z<br>4d = Drive weak low and active high<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved; Don't use |

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

### 7.5.1.10 GPIO2_CFG0 Register (Address = 0xB) [Reset = 0x00]

GPIO2_CFG0 is shown in Table 7-37.

Return to the Summary Table.

This register is the GPIO2 configuration register 0.

**Table 7-37. GPIO2_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | GPIO2_CFG[3:0] | R/W | 0000b | GPIO2 configuration.<br>0d = GPIO2 is disabled<br>1d = GPIO2 is configured as a general-purpose input (GPI) or any other input function<br>2d = GPIO2 is configured as a general-purpose output (GPO)<br>3d = GPIO2 is configured as a chip interrupt output (IRQ)<br>4d = GPIO2 is configured as a PDM clock output (PDMCLK)<br>5d = GPIO2 is configured as primary ASI DOUT<br>6d = GPIO2 is configured as primary ASI DOUT2<br>7d = GPIO2 is configured as secondary ASI DOUT<br>8d = GPIO2 is configured as secondary ASI DOUT2<br>9d = GPIO2 is configured as secondary ASI BCLK output<br>10d = GPIO2 is configured as secondary ASI FSYNC output<br>11d = GPIO2 is configured as general purpose CLKOUT<br>12d = GPIO2 is configured as PASI DOUT and SASI DOUT muxed<br>13d = GPIO2 is configured as DAISY_OUT for DIN Daisy<br>14d to 15d = Reserved |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2-0 | GPIO2_DRV[2:0] | R/W | 000b | GPIO2 output drive configuration. (Not valid if GPIO2_CFG configured as I$^2$S out)<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Drive active low and weak high<br>3d = Drive active low and Hi-Z<br>4d = Drive weak low and active high<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved; Don't use |

### 7.5.1.11 GPO1_CFG0 Register (Address = 0xC) [Reset = 0x00]

GPO1_CFG0 is shown in Table 7-38.

Return to the Summary Table.

This register is the GPO1 configuration register 0.

**Table 7-38. GPO1_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | GPO1_CFG[3:0] | R/W | 0000b | GPO1 configuration.( For SPI mode, this pin act as DO and the below configuration settings are not applicable)<br>0d = GPO1 is disabled<br>1d = Reserved<br>2d = GPO1 is configured as a general-purpose output (GPO)<br>3d = GPO1 is configured as a chip interrupt output (IRQ)<br>4d = GPO1 is configured as a PDM clock output (PDMCLK)<br>5d = GPO1 is configured as primary ASI DOUT<br>6d = GPO1 is configured as primary ASI DOUT2<br>7d = GPO1 is configured as secondary ASI DOUT<br>8d = GPO1 is configured as secondary ASI DOUT2<br>9d = GPO1 is configured as secondary ASI BCLK output<br>10d = GPO1 is configured as secondary ASI FSYNC output<br>11d = GPO1 is configured as general purpose CLKOUT<br>12d = GPO1 is configured as PASI DOUT and SASI DOUT muxed<br>13d = GPO1 is configured as DAISY_OUT for DIN Daisy<br>14d to 15d = Reserved |

**ADVANCE INFORMATION**

**Table 7-38. GPO1_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2-0 | GPO1_DRV[2:0] | R/W | 000b | GPO1 output drive configuration. (Not valid if GPO1_CFG configured as I²S out)<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Drive active low and weak high<br>3d = Drive active low and Hi-Z<br>4d = Drive weak low and active high<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved; Don't use |

### 7.5.1.12 GPI_CFG Register (Address = 0xD) [Reset = 0x00]

GPI_CFG is shown in Table 7-39.

Return to the Summary Table.

This register is the GPI1 configuration register 0.

**Table 7-39. GPI_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-2 | RESERVED | R | 000000b | Reserved bits; Write only reset values |
| 1 | GPI1_CFG | R/W | 0b | GPI1 configuration.(For SPI mode, this pin act as CSZ and the below configuration settings are not applicable)<br>0d = GPI1 is disabled<br>1d = GPI1 is configured as a general-purpose input (GPI) or any other input function |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

### 7.5.1.13 GPO_GPI_VAL Register (Address = 0xE) [Reset = 0x00]

GPO_GPI_VAL is shown in Table 7-40.

Return to the Summary Table.

This register is the GPIO and GPO output value register.

**Table 7-40. GPO_GPI_VAL Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | GPIO1_VAL | R/W | 0b | GPIO1 output value when configured as a GPO.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1 |
| 6 | GPIO2_VAL | R/W | 0b | GPIO2 output value when configured as a GPO.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1 |
| 5 | GPO1_VAL | R/W | 0b | GPO1 output value when configured as a GPO.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1 |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | GPIO1_MON | R | 0b | GPIO1 monitor value when configured as a GPI.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 |
| 2 | GPIO2_MON | R | 0b | GPIO2 monitor value when configured as a GPI.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 |

ADVANCE INFORMATION

Product Folder Links: TAD5212

**Table 7-40. GPO_GPI_VAL Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 1 | GPI1_MON | R | 0b | GPI1 monitor value when configured as a GPI.<br>0d = Input monitor value 0<br>1d = Input monitor value 1 |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.1.14 INTF_CFG0 Register (Address = 0xF) [Reset = 0x00]

INTF_CFG0 is shown in Table 7-41.

Return to the Summary Table.

This register is the interface configuration register 0.

**Table 7-41. INTF_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | CCLK_SEL[1:0] | R/W | 00b | CCLK select configuration.<br>0d = CCLK is disabled<br>1d = GPIO1<br>2d = GPIO2<br>3d = GPI1 |
| 4-2 | PASI_DIN2_SEL[2:0] | R/W | 000b | Primary ASI DIN2 select configuration.<br>0d = Primary ASI DIN2 is disabled<br>1d = GPIO1<br>2d = GPIO2<br>3d = GPI1<br>4d = DOUT<br>5d = Primary ASI DIN<br>6d to 7d = Reserved |
| 1 | PASI_BCLK_SEL | R/W | 0b | Primary ASI BCLK select configuration.<br>0d = Primary ASI BCLK is BCLK<br>1d = Primary ASI BCLK is Secondary ASI BCLK |
| 0 | PASI_FSYNC_SEL | R/W | 0b | Primary ASI FSYNC select configuration.<br>0d = Primary ASI FSYNC is FSYNC<br>1d = Primary ASI FSYNC is Secondary ASI FSYNC |

### 7.5.1.15 INTF_CFG1 Register (Address = 0x10) [Reset = 0x52]

INTF_CFG1 is shown in Table 7-42.

Return to the Summary Table.

This register is the interface configuration register 1.

**ADVANCE INFORMATION**

**ADVANCE INFORMATION**

**Table 7-42. INTF_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | DOUT_SEL[3:0] | R/W | 0101b | DOUT select configuration.<br>0d = DOUT is disabled<br>1d = DOUT is configured as input<br>2d = DOUT is configured as a general-purpose output (GPO)<br>3d = DOUT is configured as a chip interrupt output (IRQ)<br>4d = DOUT is configured as a PDM clock output (PDMCLK)<br>5d = DOUT is configured as primary ASI DOUT<br>6d = DOUT is configured as primary ASI DOUT2<br>7d = DOUT is configured as secondary ASI DOUT<br>8d = DOUT is configured as secondary ASI DOUT2<br>9d = DOUT is configured as secondary ASI BCLK output<br>10d = DOUT is configured as secondary ASI FSYNC output<br>11d = DOUT is configured as general purpose CLKOUT<br>12d = DOUT is configured as PASI DOUT and SASI DOUT muxed<br>13d = DOUT is configured as DAISY_OUT for DIN Daisy<br>14d = DOUT is configured as DIN(LOOPBACK)<br>15d = Reserved |
| 3 | DOUT_VAL | R/W | 0b | DOUT output value when configured as a GPO.<br>0d = Drive the output with a value of 0<br>1d = Drive the output with a value of 1 |
| 2-0 | DOUT_DRV[2:0] | R/W | 010b | DOUT output drive configuration.<br>0d = Hi-Z output<br>1d = Drive active low and active high<br>2d = Drive active low and weak high<br>3d = Drive active low and Hi-Z<br>4d = Drive weak low and active high<br>5d = Drive Hi-Z and active high<br>6d to 7d = Reserved; Don't use |

### 7.5.1.16 INTF_CFG2 Register (Address = 0x11) [Reset = 0x80]

INTF_CFG2 is shown in Table 7-43.

Return to the Summary Table.

This register is the interface configuration register 2.

**Table 7-43. INTF_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PASI_DIN_EN | R/W | 1b | Primary ASI DIN enable configuration.<br>0d = Primary ASI DIN is disabled<br>1d = Primary ASI DIN is enabled |
| 6-4 | SASI_FSYNC_SEL[2:0] | R/W | 000b | Secondary ASI FSYNC select configuration.<br>0d = Secondary ASI disabled<br>1d = GPIO1<br>2d = GPIO2<br>3d = GPI1<br>4d = Reserved<br>5d = Primary ASI FSYNC<br>6d to 7d = Reserved |
| 3-1 | SASI_BCLK_SEL[2:0] | R/W | 000b | Secondary ASI BCLK select configuration.<br>0d = Secondary ASI disabled<br>1d = GPIO1<br>2d = GPIO2<br>3d = GPI1<br>4d = Reserved<br>5d = Primary ASI BCLK<br>6d to 7d = Reserved |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.1.17 INTF_CFG3 Register (Address = 0x12) [Reset = 0x00]

INTF_CFG3 is shown in Table 7-44.

Return to the Summary Table.

This register is the interface configuration register 3.

**Table 7-44. INTF_CFG3 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | SASI_DIN_SEL[2:0] | R/W | 000b | Secondary ASI DIN select configuration.<br>0d = Seondary ASI DIN is disabled<br>1d = GPIO1<br>2d = GPIO2<br>3d = GPI1<br>4d = DOUT<br>5d = Primary ASI DIN<br>6d to 7d = Reserved |
| 4-2 | SASI_DIN2_SEL[2:0] | R/W | 000b | Seondary ASI DIN2 select configuration.<br>0d = Seondary ASI DIN2 is disabled<br>1d = GPIO1<br>2d = GPIO2<br>3d = GPI1<br>4d = DOUT<br>5d = Primary ASI DIN<br>6d to 7d = Reserved |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset values |

### 7.5.1.18 INTF_CFG5 Register (Address = 0x14) [Reset = 0x00]

INTF_CFG5 is shown in Table 7-45.

Return to the Summary Table.

This register is the interface configuration register 4.

**Table 7-45. INTF_CFG5 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5-4 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 3-2 | PD_DAC_GPIO[1:0] | R/W | 00b | Power down DAC using GPIO select configuration.(DAC powered down if any one of the PD_DAC_GPIO/DAC_PDZ is configured power down)<br>0d = Power down DAC using GPIO is disabled<br>1d = Power down DAC using GPIO1<br>2d = Power down DAC using GPIO2<br>3d = Power down DAC using GPI1 |
| 1 | PLIM_GPIO | R/W | 0b | PLIM using GPIO1 configuration.<br>0d = PLIM using GPIO1 is disabled<br>1d = PLIM using GPIO1 |
| 0 | GPA_GPIO | R/W | 0b | GPA using GPIO1 configuration.<br>0d = GPA using GPIO1 is disabled<br>1d = GPA using GPIO1 |

### 7.5.1.19 ASI_CFG0 Register (Address = 0x18) [Reset = 0x40]

ASI_CFG0 is shown in Table 7-46.

Return to the Summary Table.

ADVANCE INFORMATION

This register is the ASI configuration register 0.

**ADVANCE INFORMATION**

### Table 7-46. ASI_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | PASI_DIS | R/W | 0b | Disable or enable primary ASI (PASI).<br>0d = Primary ASI enabled<br>1d = Primary ASI disabled |
| 6 | SASI_DIS | R/W | 1b | Disable or enable secondary ASI (SASI).<br>0d = Secondary ASI enabled<br>1d = Secondary ASI disabled |
| 5 | SASI_CFG_GANG | R/W | 0b | All configurations of secondary ASI ganged with primary ASI.<br>0d = Secondary ASI has independent configurations<br>1d = Secondary ASI configurations same as primary ASI |
| 4-3 | DAISY_EN[1:0] | R/W | 00b | Daisy chain feature enable (only 1 ASI with 1 DOUT AND DIN available)<br>0d = Daisy chain disabled<br>1d = PASI daisy chain enabled (Secondary ASI not available)<br>2d = SASI daisy chain enabled (Primary ASI not available)<br>3d = Reserved; Don't use |
| 2-0 | DAISY_IN_SEL[2:0] | R/W | 000b | Daisy input select configuration.<br>0d = Daisy input disabled<br>1d = GPIO1<br>2d = GPIO2<br>3d = GPI1<br>4d = Reserved<br>5d = DIN<br>6d to 7d = Reserved |

### 7.5.1.20 ASI_CFG1 Register (Address = 0x19) [Reset = 0x00]

ASI_CFG1 is shown in Table 7-47.

Return to the Summary Table.

This register is the ASI configuration register 1.

### Table 7-47. ASI_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | ASI_DOUT_CFG[1:0] | R/W | 00b | ASI data output configuration.<br>0d = 1 data output for Primary ASI and 1 data output for Secondary ASI<br>1d = 2 data outputs for Primary ASI<br>2d = 2 data outputs for Secondary ASI<br>3d = Reserved; Don't use |
| 5-4 | ASI_DIN_CFG[1:0] | R/W | 00b | ASI data input configuration.<br>0d = 1 data input for Primary ASI and 1 data input for Secondary ASI<br>1d = 2 data inputs for Primary ASI<br>2d = 2 data inputs for Secondary ASI<br>3d = Reserved; Don't use |
| 3 | DAISY_DIR | R/W | 0b | Daisy direction configuration.<br>0d = ASI DOUT daisy<br>1d = ASI DIN daisy |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

Product Folder Links: *TAD5212*

### 7.5.1.21 PASI_CFG0 Register (Address = 0x1A) [Reset = 0x30]

PASI_CFG0 is shown in Table 7-48.

Return to the Summary Table.

This register is the ASI configuration register 0.

**Table 7-48. PASI_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | PASI_FORMAT[1:0] | R/W | 00b | Primary ASI protocol format.<br>0d = TDM mode<br>1d = I²S mode<br>2d = LJ (left-justified) mode<br>3d = Reserved; Don't use |
| 5-4 | PASI_WLEN[1:0] | R/W | 11b | Primary ASI word or slot length.<br>0d = 16 bits (Recommended: This setting to be used with 10-kΩ input impedance configuration)<br>1d = 20 bits<br>2d = 24 bits<br>3d = 32 bits |
| 3 | PASI_FSYNC_POL | R/W | 0b | ASI FSYNC polarity (for PASI protocol only).<br>0d = Default polarity as per standard protocol<br>1d = Inverted polarity with respect to standard protocol |
| 2 | PASI_BCLK_POL | R/W | 0b | ASI BCLK polarity (for PASI protocol only).<br>0d = Default polarity as per standard protocol<br>1d = Inverted polarity with respect to standard protocol |
| 1 | PASI_BUS_ERR | R/W | 0b | ASI bus error detection.<br>0d = Enable bus error detection<br>1d = Disable bus error detection |
| 0 | PASI_BUS_ERR_RCOV | R/W | 0b | ASI bus error auto resume.<br>0d = Enable auto resume after bus error recovery<br>1d = Disable auto resume after bus error recovery and remain powered down until host configures the device |

### 7.5.1.22 PASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00]

PASI_TX_CFG0 is shown in Table 7-49.

Return to the Summary Table.

This register is the PASI TX configuration register 0.

**Table 7-49. PASI_TX_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | PASI_TX_EDGE | R/W | 0b | Primary ASI data output (on the primary and secondary data pin) transmit edge.<br>0d = Default edge as per the protocol configuration setting in PASI_BCLK_POL<br>1d = Inverted following edge (half cycle delay) with respect to the default edge setting |
| 6 | PASI_TX_FILL | R/W | 0b | Primary ASI data output (on the primary and secondary data pin) for any unused cycles<br>0d = Always transmit 0 for unused cycles<br>1d = Always use Hi-Z for unused cycles |
| 5 | PASI_TX_LSB | R/W | 0b | Primary ASI data output (on the primary and secondary data pin) for LSB transmissions.<br>0d = Transmit the LSB for a full cycle<br>1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle |

**ADVANCE INFORMATION**

**Table 7-49. PASI_TX_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 4-3 | PASI_TX_KEEPER[1:0] | R/W | 00b | Primary ASI data output (on the primary and secondary data pin) bus keeper.<br>0d = Bus keeper is always disabled<br>1d = Bus keeper is always enabled<br>2d = Bus keeper is enabled during LSB transmissions only for one cycle<br>3d = Bus keeper is enabled during LSB transmissions only for one and half cycles |
| 2 | PASI_TX_USE_INT_FSYNC | R/W | 0b | Primary ASI uses internal FSYNC for output data generation in Controller mode configuration as applicable.<br>0d = Use external FSYNC for ASI protocol data generation<br>1d = Use internal FSYNC for ASI protocol data generation |
| 1 | PASI_TX_USE_INT_BCLK | R/W | 0b | Primary ASI uses internal BCLK for output data generation in Controller mode configuration.<br>0d = Use external BCLK for ASI protocol data generation<br>1d = Use internal BCLK for ASI protocol data generation |
| 0 | PASI_TDM_PULSE_WIDTH | R/W | 0b | Primary ASI fsync pulse width in TDM format. (Valid for Controller mode)<br>0d = Fsync pulse is 1 bclk period wide<br>1d = Fsync pulse is 2 bclk period wide |

### 7.5.1.23 PASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00]

PASI_TX_CFG1 is shown in Table 7-50.

Return to the Summary Table.

This register is the PASI TX configuration register 1.

**Table 7-50. PASI_TX_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-5 | RESERVED | R | 000b | Reserved bits; Write only reset values |
| 4-0 | PASI_TX_OFFSET[4:0] | R/W | 00000b | Primary ASI output data MSB slot 0 offset (on the primary and secondary data pin).<br>0d = ASI data MSB location has no offset and is as per standard protocol<br>1d = ASI data MSB location (TDM mode is slot 0 or I$^2$S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol<br>2d = ASI data MSB location (TDM mode is slot 0 or I$^2$S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol<br>3d to 30d = ASI data MSB location (TDM mode is slot 0 or I$^2$S, LJ mode is the left and right slot 0) offset assigned as per configuration<br>31d = ASI data MSB location (TDM mode is slot 0 or I$^2$S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

### 7.5.1.24 PASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00]

PASI_TX_CFG2 is shown in Table 7-51.

Return to the Summary Table.

This register is the PASI TX configuration register 2.

Product Folder Links: *TAD5212*

ADVANCE INFORMATION

**Table 7-51. PASI_TX_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | PASI_TX_CH8_SEL | R/W | 0b | Primary ASI output channel 8 select.<br>0d = Primary ASI channel 8 output is on DOUT<br>1d = Primary ASI channel 8 output is on DOUT2 |
| 6 | PASI_TX_CH7_SEL | R/W | 0b | Primary ASI output channel 7 select.<br>0d = Primary ASI channel 7 output is on DOUT<br>1d = Primary ASI channel 7 output is on DOUT2 |
| 5 | PASI_TX_CH6_SEL | R/W | 0b | Primary ASI output channel 6 select.<br>0d = Primary ASI channel 6 output is on DOUT<br>1d = Primary ASI channel 6 output is on DOUT2 |
| 4 | PASI_TX_CH5_SEL | R/W | 0b | Primary ASI output channel 5 select.<br>0d = Primary ASI channel 5 output is on DOUT<br>1d = Primary ASI channel 5 output is on DOUT2 |
| 3 | PASI_TX_CH4_SEL | R/W | 0b | Primary ASI output channel 4 select.<br>0d = Primary ASI channel 4 output is on DOUT<br>1d = Primary ASI channel 4 output is on DOUT2 |
| 2 | PASI_TX_CH3_SEL | R/W | 0b | Primary ASI output channel 3 select.<br>0d = Primary ASI channel 3 output is on DOUT<br>1d = Primary ASI channel 3 output is on DOUT2 |
| 1 | PASI_TX_CH2_SEL | R/W | 0b | Primary ASI output channel 2 select.<br>0d = Primary ASI channel 2 output is on DOUT<br>1d = Primary ASI channel 2 output is on DOUT2 |
| 0 | PASI_TX_CH1_SEL | R/W | 0b | Primary ASI output channel 1 select.<br>0d = Primary ASI channel 1 output is on DOUT<br>1d = Primary ASI channel 1 output is on DOUT2 |

### 7.5.1.25 PASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02]

PASI_TX_CH3_CFG is shown in Table 7-52.

Return to the Summary Table.

This register is the PASI TX Channel 3 configuration register.

**Table 7-52. PASI_TX_CH3_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_TX_CH3_CFG[1:0] | R/W | 00b | Primary ASI output channel 3 configuration.<br>0d = Primary ASI channel 3 output is in a tri-state condition<br>Dont use<br>2d = Primary ASI channel 3 output corresponds to VBAT data<br>Dont use |
| 4-0 | PASI_TX_CH3_SLOT_NUM[4:0] | R/W | 00010b | Primary ASI output channel 3 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.26 PASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03]

PASI_TX_CH4_CFG is shown in Table 7-53.

Return to the Summary Table.

ADVANCE INFORMATION

This register is the PASI TX Channel 4 configuration register.

**Table 7-53. PASI_TX_CH4_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_TX_CH4_CFG[1:0] | R/W | 00b | Primary ASI output channel 4 configuration.<br>0d = Primary ASI channel 4 output is in a tri-state condition<br>Dont use<br>2d = Primary ASI channel 4 output corresponds to TEMP data<br>3d = Reserved |
| 4-0 | PASI_TX_CH4_SLOT_NUM[4:0] | R/W | 00011b | Primary ASI output channel 4 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

**7.5.1.27 PASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04]**

PASI_TX_CH5_CFG is shown in Table 7-54.

Return to the Summary Table.

This register is the PASI TX Channel 5 configuration register.

**Table 7-54. PASI_TX_CH5_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_TX_CH5_CFG[1:0] | R/W | 00b | Primary ASI output channel 5 configuration.<br>0d = Primary ASI channel 5 output is in a tri-state condition<br>1d = Primary ASI channel 5 output corresponds to ASI Input Channel 1 loopback data<br>2d = Primary ASI channel 5 output corresponds to echo reference Channel 1 data<br>3d = Reserved |
| 4-0 | PASI_TX_CH5_SLOT_NUM[4:0] | R/W | 00100b | Primary ASI output channel 5 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

**7.5.1.28 PASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05]**

PASI_TX_CH6_CFG is shown in Table 7-55.

Return to the Summary Table.

This register is the PASI TX Channel 6 configuration register.

**Table 7-55. PASI_TX_CH6_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |

Product Folder Links: *TAD5212*

ADVANCE INFORMATION

**Table 7-55. PASI_TX_CH6_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 6-5 | PASI_TX_CH6_CFG[1:0] | R/W | 00b | Primary ASI output channel 6 configuration.<br>0d = Primary ASI channel 6 output is in a tri-state condition<br>1d = Primary ASI channel 6 output corresponds to ASI Input Channel 2 loopback data<br>2d = Primary ASI channel 6 output corresponds to echo reference Channel 2 data<br>3d = Reserved |
| 4-0 | PASI_TX_CH6_SLOT_NUM[4:0] | R/W | 00101b | Primary ASI output channel 6 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.29 PASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06]

PASI_TX_CH7_CFG is shown in Table 7-56.

Return to the Summary Table.

This register is the PASI TX Channel 7 configuration register.

**Table 7-56. PASI_TX_CH7_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_TX_CH7_CFG[1:0] | R/W | 00b | Primary ASI output channel 7 configuration.<br>0d = Primary ASI channel 7 output is in a tri-state condition<br>1d = Primary ASI channel 7 output corresponds to {VBAT_WLby2, TEMP_WLby2}<br>2d = Primary ASI channel 7 output corresponds to {echo_ref_ch1, echo_ref_ch2}<br>3d = Reserved |
| 4-0 | PASI_TX_CH7_SLOT_NUM[4:0] | R/W | 00110b | Primary ASI output channel 7 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.30 PASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07]

PASI_TX_CH8_CFG is shown in Table 7-57.

Return to the Summary Table.

This register is the PASI TX Channel 8 configuration register.

**Table 7-57. PASI_TX_CH8_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_TX_CH8_CFG | R/W | 0b | Primary ASI output channel 8 configuration.<br>0d = Primary ASI channel 8 output is in a tri-state condition<br>1d = Primary ASI channel 8 output corresponds to ICLA data |

ADVANCE INFORMATION

**Table 7-57. PASI_TX_CH8_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4-0 | PASI_TX_CH8_SLOT_NUM[4:0] | R/W | 00111b | Primary ASI output channel 8 slot assignment. 0d = TDM is slot 0 or I$^2$S, LJ is left slot 0 1d = TDM is slot 1 or I$^2$S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I$^2$S, LJ is left slot 15 16d = TDM is slot 16 or I$^2$S, LJ is right slot 0 17d = TDM is slot 17 or I$^2$S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.31 PASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00]

PASI_RX_CFG0 is shown in Table 7-58.

Return to the Summary Table.

This register is the PASI RX configuration register 0.

**Table 7-58. PASI_RX_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | PASI_RX_EDGE | R/W | 0b | Primary ASI data input (on the primary and secondary data pin) receive edge. 0d = Default edge as per the protocol configuration setting in PASI_BCLK_POL 1d = Inverted following edge (half cycle delay) with respect to the default edge setting |
| 6 | PASI_RX_USE_INT_FSYNC | R/W | 0b | Primary ASI uses internal FSYNC for input data latching in Controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data latching 1d = Use internal FSYNC for ASI protocol data latching |
| 5 | PASI_RX_USE_INT_BCLK | R/W | 0b | Primary ASI uses internal BCLK for input data latching in Controller mode configuration. 0d = Use external BCLK for ASI protocol data latching 1d = Use internal BCLK for ASI protocol data latching |
| 4-0 | PASI_RX_OFFSET[4:0] | R/W | 00000b | Primary ASI data input MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I$^2$S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I$^2$S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I$^2$S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I$^2$S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

### 7.5.1.32 PASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00]

PASI_RX_CFG1 is shown in Table 7-59.

Return to the Summary Table.

This register is the PASI RX configuration register 1.

**Table 7-59. PASI_RX_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | PASI_RX_CH8_SEL | R/W | 0b | Primary ASI input channel 8 select.<br>0d = Primary ASI channel 8 input is on DIN<br>1d = Primary ASI channel 8 input is on DIN2 |
| 6 | PASI_RX_CH7_SEL | R/W | 0b | Primary ASI input channel 7 select.<br>0d = Primary ASI channel 7 input is on DIN<br>1d = Primary ASI channel 7 input is on DIN2 |
| 5 | PASI_RX_CH6_SEL | R/W | 0b | Primary ASI input channel 6 select.<br>0d = Primary ASI channel 6 input is on DIN<br>1d = Primary ASI channel 6 input is on DIN2 |
| 4 | PASI_RX_CH5_SEL | R/W | 0b | Primary ASI input channel 5 select.<br>0d = Primary ASI channel 5 input is on DIN<br>1d = Primary ASI channel 5 input is on DIN2 |
| 3 | PASI_RX_CH4_SEL | R/W | 0b | Primary ASI input channel 4 select.<br>0d = Primary ASI channel 4 input is on DIN<br>1d = Primary ASI channel 4 input is on DIN2 |
| 2 | PASI_RX_CH3_SEL | R/W | 0b | Primary ASI input channel 3 select.<br>0d = Primary ASI channel 3 input is on DIN<br>1d = Primary ASI channel 3 input is on DIN2 |
| 1 | PASI_RX_CH2_SEL | R/W | 0b | Primary ASI input channel 2 select.<br>0d = Primary ASI channel 2 input is on DIN<br>1d = Primary ASI channel 2 input is on DIN2 |
| 0 | PASI_RX_CH1_SEL | R/W | 0b | Primary ASI input channel 1 select.<br>0d = Primary ASI channel 1 input is on DIN<br>1d = Primary ASI channel 1 input is on DIN2 |

### 7.5.1.33 PASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x20]

PASI_RX_CH1_CFG is shown in Table 7-60.

Return to the Summary Table.

This register is the PASI RX Channel 1 configuration register.

**Table 7-60. PASI_RX_CH1_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_RX_CH1_CFG | R/W | 1b | Primary ASI input channel 1 configuration.<br>0d = Primary ASI channel 1 input is disabled<br>1d = Primary ASI channel 1 input corresponds to DAC Channel 1 data |
| 4-0 | PASI_RX_CH1_SLOT_NUM[4:0] | R/W | 00000b | Primary ASI input channel 1 slot assignment.<br>0d = TDM is slot 0 or $I^2S$, LJ is left slot 0<br>1d = TDM is slot 1 or $I^2S$, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or $I^2S$, LJ is left slot 15<br>16d = TDM is slot 16 or $I^2S$, LJ is right slot 0<br>17d = TDM is slot 17 or $I^2S$, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or $I^2S$, LJ is right slot 15 |

### 7.5.1.34 PASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x21]

PASI_RX_CH2_CFG is shown in Table 7-61.

Return to the Summary Table.

This register is the PASI RX Channel 2 configuration register.

ADVANCE INFORMATION

**Table 7-61. PASI_RX_CH2_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_RX_CH2_CFG | R/W | 1b | Primary ASI input channel 2 configuration.<br>0d = Primary ASI channel 2 input is disabled<br>1d = Primary ASI channel 2 input corresponds to DAC Channel 2 data |
| 4-0 | PASI_RX_CH2_SLOT_NUM[4:0] | R/W | 00001b | Primary ASI input channel 2 slot assignment.<br>0d = TDM is slot 0 or $I^2S$, LJ is left slot 0<br>1d = TDM is slot 1 or $I^2S$, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or $I^2S$, LJ is left slot 15<br>16d = TDM is slot 16 or $I^2S$, LJ is right slot 0<br>17d = TDM is slot 17 or $I^2S$, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or $I^2S$, LJ is right slot 15 |

**7.5.1.35 PASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02]**

PASI_RX_CH3_CFG is shown in Table 7-62.

Return to the Summary Table.

This register is the PASI RX Channel 3 configuration register.

**Table 7-62. PASI_RX_CH3_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_RX_CH3_CFG | R/W | 0b | Primary ASI input channel 3 configuration.<br>0d = Primary ASI channel 3 input is disabled<br>1d = Primary ASI channel 3 input corresponds to DAC Channel 3 data |
| 4-0 | PASI_RX_CH3_SLOT_NUM[4:0] | R/W | 00010b | Primary ASI input channel 3 slot assignment.<br>0d = TDM is slot 0 or $I^2S$, LJ is left slot 0<br>1d = TDM is slot 1 or $I^2S$, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or $I^2S$, LJ is left slot 15<br>16d = TDM is slot 16 or $I^2S$, LJ is right slot 0<br>17d = TDM is slot 17 or $I^2S$, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or $I^2S$, LJ is right slot 15 |

**7.5.1.36 PASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03]**

PASI_RX_CH4_CFG is shown in Table 7-63.

Return to the Summary Table.

This register is the PASI RX Channel 4 configuration register.

**Table 7-63. PASI_RX_CH4_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5 | PASI_RX_CH4_CFG | R/W | 0b | Primary ASI input channel 4 configuration.<br>0d = Primary ASI channel 4 input is disabled<br>1d = Primary ASI channel 4 input corresponds to DAC Channel 4 data |

ADVANCE INFORMATION

**Table 7-63. PASI_RX_CH4_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 4-0 | PASI_RX_CH4_SLOT_NUM[4:0] | R/W | 00011b | Primary ASI input channel 4 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.37 PASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04]

PASI_RX_CH5_CFG is shown in Table 7-64.

Return to the Summary Table.

This register is the PASI RX Channel 5 configuration register.

**Table 7-64. PASI_RX_CH5_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_RX_CH5_CFG[1:0] | R/W | 00b | Primary ASI input channel 5 configuration.<br>0d = Primary ASI channel 5 input is disabled<br>1d = Primary ASI channel 5 input corresponds to DAC Channel 5 data<br>2d = Primary ASI channel 5 input corresponds to ADC Channel 1 output loopback<br>3d = Reserved |
| 4-0 | PASI_RX_CH5_SLOT_NUM[4:0] | R/W | 00100b | Primary ASI input channel 5 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.38 PASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05]

PASI_RX_CH6_CFG is shown in Table 7-65.

Return to the Summary Table.

This register is the PASI RX Channel 6 configuration register.

**Table 7-65. PASI_RX_CH6_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_RX_CH6_CFG[1:0] | R/W | 00b | Primary ASI input channel 6 configuration.<br>0d = Primary ASI channel 6 input is disabled<br>1d = Primary ASI channel 6 input corresponds to DAC Channel 6 data<br>2d = Primary ASI channel 6 input corresponds to ADC Channel 2 output loopback<br>3d = Primary ASI channel 6 input corresponds to ICLA device 1 data |

**ADVANCE INFORMATION**

**ADVANCE INFORMATION**

**Table 7-65. PASI_RX_CH6_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4-0 | PASI_RX_CH6_SLOT_NUM[4:0] | R/W | 00101b | Primary ASI input channel 6 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.39 PASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06]

PASI_RX_CH7_CFG is shown in Table 7-66.

Return to the Summary Table.

This register is the PASI RX Channel 7 configuration register.

**Table 7-66. PASI_RX_CH7_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_RX_CH7_CFG[1:0] | R/W | 00b | Primary ASI input channel 7 configuration.<br>0d = Primary ASI channel 7 input is disabled<br>1d = Primary ASI channel 7 input corresponds to DAC Channel 7 data<br>2d = Primary ASI channel 7 input corresponds to ADC Channel 3 output loopback<br>3d = Primary ASI channel 7 input corresponds to ICLA device 2 data |
| 4-0 | PASI_RX_CH7_SLOT_NUM[4:0] | R/W | 00110b | Primary ASI input channel 7 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.40 PASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07]

PASI_RX_CH8_CFG is shown in Table 7-67.

Return to the Summary Table.

This register is the PASI RX Channel 8 configuration register.

**Table 7-67. PASI_RX_CH8_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | PASI_RX_CH8_CFG[1:0] | R/W | 00b | Primary ASI input channel 8 configuration.<br>0d = Primary ASI channel 8 input is disabled<br>1d = Primary ASI channel 8 input corresponds to DAC Channel 8 data<br>2d = Primary ASI channel 8 input corresponds to ADC Channel 4 output loopback<br>3d = Primary ASI channel 8 input corresponds to ICLA device 3 data |

Product Folder Links: *TAD5212*

**Table 7-67. PASI_RX_CH8_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 4-0 | PASI_RX_CH8_SLOT_NUM[4:0] | R/W | 00111b | Primary ASI input channel 8 slot assignment. <br> 0d = TDM is slot 0 or I$^2$S, LJ is left slot 0 <br> 1d = TDM is slot 1 or I$^2$S, LJ is left slot 1 <br> 2d to 14d = Slot assigned as per configuration <br> 15d = TDM is slot 15 or I$^2$S, LJ is left slot 15 <br> 16d = TDM is slot 16 or I$^2$S, LJ is right slot 0 <br> 17d = TDM is slot 17 or I$^2$S, LJ is right slot 1 <br> 18d to 30d = Slot assigned as per configuration <br> 31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.1.41 CLK_CFG0 Register (Address = 0x32) [Reset = 0x00]

CLK_CFG0 is shown in Table 7-68.

Return to the Summary Table.

This register is the clock configuration register 0.

**Table 7-68. CLK_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-2 | PASI_SAMP_RATE[5:0] | R/W | 000000b | Primary ASI sample rate configuration. -Typical (Allowed Range) <br> 0d = Primary ASI sampling rate auto detected in the device <br> 1d = 768000 (670320-791040) <br> 2d = 614400 (536256-632832) <br> 3d = 512000 (446880-527360) <br> 4d = 438857 (383040-452022) <br> 5d = 384000 (335160-395520) <br> 6d = 341333 (297920-351573) <br> 7d = 307200 (268128-316416) <br> 8d = 256000 (223440-263680) <br> 9d = 219429 (191520-226011) <br> 10d = 192000 (167580-197760) <br> 11d = 170667 (148960-175786) <br> 12d = 153600 (134064-158208) <br> 13d = 128000 (111720-131840) <br> 14d = 109714 (95760-113005) <br> 15d = 96000 (83790-98880) <br> 16d = 85333 (74480-87893) <br> 17d = 76800 (67032-79104) <br> 18d = 64000 (55860-65920) <br> 19d = 54857 (47880-56502) <br> 20d = 48000 (41895-49440) <br> 21d = 42667 (37240-43946) <br> 22d = 38400 (33516-39552) <br> 23d = 32000 (27930-32960) <br> 24d = 27429 (23940-28251) <br> 25d = 24000 (20947-24720) <br> 26d = 21333 (18620-21973) <br> 27d = 19200 (16758-19776) <br> 28d = 16000 (13965-16480) <br> 29d = 13714 (11970-14125) <br> 30d = 12000 (10473-12360) <br> 31d = 10667 (9310-10986) <br> 32d = 9600 (8379-9888) <br> 33d = 8000 (6982-8240) <br> 34d = 6857 (5985-7062) <br> 35d = 6000 (5236-6180) <br> 36d = 5333 (4655-5493) <br> 37d = 4800 (4189-4944) <br> 38d = 4000 (3491-4120) <br> 39d = 3429 (2992-3531) <br> 40d = 3000 (2618-3090) <br> 41d-63d = Reserved |

Product Folder Links: TAD5212

ADVANCE INFORMATION

**Table 7-68. CLK_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 1 | PASI_FS_RATE_NO_LIM | R/W | 0b | Limit sampling rate to standard audio sample rates only.<br>0d = Standard audio rates with 1% tolerance supported using auto mode<br>1d = Standard audio rates with 5% tolerance supported using auto mode |
| 0 | CUSTOM_CLK_CFG | R/W | 0b | Custom clock configuration enable, all dividers and mux selects need to be manually configured.<br>0d = Auto clock configuration<br>1d = Custom clock configuration |

### 7.5.1.42 CLK_CFG1 Register (Address = 0x33) [Reset = 0x00]

CLK_CFG1 is shown in Table 7-69.

Return to the Summary Table.

This register is the clock configuration register 1.

**Table 7-69. CLK_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-2 | SASI_SAMP_RATE[5:0] | R/W | 000000b | Secondary ASI sample rate configuration. -Typical (Range)<br>0d = Secondary ASI sampling rate auto detected in the device<br>1d = 768000 (670320-791040)<br>2d = 614400 (536256-632832)<br>3d = 512000 (446880-527360)<br>4d = 438857 (383040-452022)<br>5d = 384000 (335160-395520)<br>6d = 341333 (297920-351573)<br>7d = 307200 (268128-316416)<br>8d = 256000 (223440-263680)<br>9d = 219429 (191520-226011)<br>10d = 192000 (167580-197760)<br>11d = 170667 (148960-175786)<br>12d = 153600 (134064-158208)<br>13d = 128000 (111720-131840)<br>14d = 109714 (95760-113005)<br>15d = 96000 (83790-98880)<br>16d = 85333 (74480-87893)<br>17d = 76800 (67032-79104)<br>18d = 64000 (55860-65920)<br>19d = 54857 (47880-56502)<br>20d = 48000 (41895-49440)<br>21d = 42667 (37240-43946)<br>22d = 38400 (33516-39552)<br>23d = 32000 (27930-32960)<br>24d = 27429 (23940-28251)<br>25d = 24000 (20947-24720)<br>26d = 21333 (18620-21973)<br>27d = 19200 (16758-19776)<br>28d = 16000 (13965-16480)<br>29d = 13714 (11970-14125)<br>30d = 12000 (10473-12360)<br>31d = 10667 (9310-10986)<br>32d = 9600 (8379-9888)<br>33d = 8000 (6982-8240)<br>34d = 6857 (5985-7062)<br>35d = 6000 (5236-6180)<br>36d = 5333 (4655-5493)<br>37d = 4800 (4189-4944)<br>38d = 4000 (3491-4120)<br>39d = 3429 (2992-3531)<br>40d = 3000 (2618-3090)<br>41d-63d = Reserved |

Product Folder Links: *TAD5212*

ADVANCE INFORMATION

**Table 7-69. CLK_CFG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 1 | SASI_FS_RATE_NO_LIM | R/W | 0b | Limit sampling rate to standard audio sample rates only.<br>0d = Standard audio rates with 1% tolerance supported using auto mode<br>1d = Standard audio rates with 5% tolerance supported using auto mode |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.1.43 CLK_CFG2 Register (Address = 0x34) [Reset = 0x40]

CLK_CFG2 is shown in Table 7-70.

Return to the Summary Table.

This register is the clock configuration register 2.

**Table 7-70. CLK_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | PLL_DIS | R/W | 0b | Custom/Auto clock mode PLL setting.<br>0d = PLL is always enabled in custom clk mode/PLL is enabled based on DSP MIPS requirement in auto clock mode<br>1d = PLL is disabled |
| 6 | AUTO_PLL_FR_ALLOW | R/W | 1b | Allow the PLL to operate in fractional mode of operation.<br>0d = PLL fractional mode disabled<br>1d = PLL fractional mode allowed |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 3-1 | CLK_SRC_SEL[2:0] | R/W | 000b | Input clock source select.<br>0d = Primary ASI BCLK is the input clock source<br>1d = CCLK synchronized with Primary ASI FSYNC is the input clock source<br>2d = Secondary ASI BCLK is the input clock source<br>3d = CCLK synchronized with Secondary ASI FSYNC is the input clock source<br>4d = Fixed CCLK frequency (used only in controller mode configuration)<br>5d = Internal oscillator clock is the input clock source<br>6d to 7d = Reserved |
| 0 | RATIO_CLK_EDGE | R/W | 0b | Edge selection for clock source ratio detection.<br>0d = Use rising edge of clock source to check ratio with primary or secondary FSYNC<br>1d = Use falling edge of clock source to check ratio with primary or secondary FSYNC |

### 7.5.1.44 CNT_CLK_CFG0 Register (Address = 0x35) [Reset = 0x00]

CNT_CLK_CFG0 is shown in Table 7-71.

Return to the Summary Table.

This register is the controller mode clock configuration register 0.

**Table 7-71. CNT_CLK_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |

**Table 7-71. CNT_CLK_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 5-0 | CCLK_FS_RATIO_MSB[5:0] | R/W | 000000b | Most significant bits for selecting the ratio between CCLK and primary/secondary ASI FSYNC with which CCLK is synchonized.<br>0d = Auto detect the ratio (assumption is CCLK is synchronized with primary/secondary FSYNC)<br>1d to 16383d = Ratio as per configuration |

### 7.5.1.45 CNT_CLK_CFG1 Register (Address = 0x36) [Reset = 0x00]

CNT_CLK_CFG1 is shown in Table 7-72.

Return to the Summary Table.

This register is the controller mode clock configuration register 1.

**Table 7-72. CNT_CLK_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | CCLK_FS_RATIO_LSB[7:0] | R/W | 00000000b | LSB's for selecting the ratio between CCLK and primary/secondary ASI FSYNC with which CCLK is synchonized.<br>0d = Auto detect the ratio (assumption is CCLK is synchronized with primary/secondary FSYNC)<br>1d to 16383d = Ratio as per configuration |

### 7.5.1.46 CNT_CLK_CFG2 Register (Address = 0x37) [Reset = 0x20]

CNT_CLK_CFG2 is shown in Table 7-73.

Return to the Summary Table.

This register is the controller mode clock configuration register 2.

**Table 7-73. CNT_CLK_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | CCLK_FREQ_SEL[2:0] | R/W | 001b | These bits select the CCLK input frequency (used only in controller mode configuration).<br>0d = 12 MHz<br>1d = 12.288 MHz<br>2d = 13 MHz<br>3d = 16 MHz<br>4d = 19.2 MHz<br>5d = 19.68 MHz<br>6d = 24 MHz<br>7d = 24.576 MHz |
| 4 | PASI_CNT_CFG | R/W | 0b | Primary ASI controller or target configuration<br>0d = Primary ASI in target configuration<br>1d = Primary ASI in controller configuration |
| 3 | SASI_CNT_CFG | R/W | 0b | Secondary ASI controller or target configuration<br>0d = Secondary ASI in target configuration<br>1d = Secondary ASI in controller configuration |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | FS_MODE | R/W | 0b | Sample rate setting (valid when the device is in controller mode). This is applicable for both PASI and SASI.<br>0d = sampling rate is a multiple (or submultiple) of 48 kHz<br>1d = sampling rate is a multiple (or submultiple) of 44.1 kHz |

Product Folder Links: *TAD5212*

## 7.5.1.47 CNT_CLK_CFG3 Register (Address = 0x38) [Reset = 0x00]

CNT_CLK_CFG3 is shown in Table 7-74.

Return to the Summary Table.

This register is the controller mode clock configuration register 3.

**Table 7-74. CNT_CLK_CFG3 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | PASI_USE_INT_BCLK_FOR_FSYNC | R/W | 0b | Use internal BCLK for FSYNC generation in PASI during controller mode configuration.<br>0d = Use external BCLK for FSYNC generation<br>1d = Use internal BCLK for FSYNC generation |
| 6 | PASI_INV_BCLK_FOR_FSYNC | R/W | 0b | Invert PASI BCLK polarity only for PASI FSYNC generation in controller mode configuration.<br>0d = Do not invert PASI BCLK polarity for PASI FSYNC generation<br>1d = Invert PASI BCLK polarity for PASI FSYNC generation |
| 5-0 | PASI_BCLK_FS_RATIO_MSB[5:0] | R/W | 000000b | MSB bits for primary ASI BCLK to FSYNC ratio in controller mode. |

## 7.5.1.48 CNT_CLK_CFG4 Register (Address = 0x39) [Reset = 0x00]

CNT_CLK_CFG4 is shown in Table 7-75.

Return to the Summary Table.

This register is the controller mode clock configuration register 4.

**Table 7-75. CNT_CLK_CFG4 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | PASI_BCLK_FS_RATIO_LSB[7:0] | R/W | 00000000b | LSB byte for primary ASI BCLK to FSYNC ratio in controller mode. |

## 7.5.1.49 CNT_CLK_CFG5 Register (Address = 0x3A) [Reset = 0x00]

CNT_CLK_CFG5 is shown in Table 7-76.

Return to the Summary Table.

This register is the controller mode clock configuration register 5.

**Table 7-76. CNT_CLK_CFG5 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | SASI_USE_INT_BCLK_FOR_FSYNC | R/W | 0b | Use internal BCLK for FSYNC generation in SASI during controller mode configuration.<br>0d = Use external BCLK for FSYNC generation<br>1d = Use internal BCLK for FSYNC generation |
| 6 | SASI_INV_BCLK_FOR_FSYNC | R/W | 0b | Invert SASI BCLK polarity only for SASI FSYNC generation in controller mode configuration.<br>0d = Do not invert SASI BCLK polarity for SASI FSYNC generation<br>1d = Invert SASI BCLK polarity for SASI FSYNC generation |
| 5-0 | SASI_BCLK_FS_RATIO_MSB[5:0] | R/W | 000000b | MSB bits for secondary ASI BCLK to FSYNC ratio in controller mode. |

## 7.5.1.50 CNT_CLK_CFG6 Register (Address = 0x3B) [Reset = 0x00]

CNT_CLK_CFG6 is shown in Table 7-77.

Return to the Summary Table.

**ADVANCE INFORMATION**

This register is the controller mode clock configuration register 6.

**Table 7-77. CNT_CLK_CFG6 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | SASI_BCLK_FS_RATIO_LSB[7:0] | R/W | 00000000b | LSB byte for secondary ASI BCLK to FSYNC ratio in controller mode. |

### 7.5.1.51 CLK_ERR_STS0 Register (Address = 0x3C) [Reset = 0x00]

CLK_ERR_STS0 is shown in Table 7-78.

Return to the Summary Table.

This register is the clock error and status register 0.

**Table 7-78. CLK_ERR_STS0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | DSP_CLK_ERR | R | 0b | Flag indicating ratio error between FSYNC and selected clock source.<br>0d = No ratio error<br>1d = Ratio error between primary or secondary ASI FSYNC and selected clock source |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | SRC_RATIO_ERR | R | 0b | Flag indicating that SRC m:n ratio is unsupported. (not valid for custom m/n ratio config).<br>0d = m:n ratio supported<br>1d = Unsupported m:n ratio error |
| 3 | DEM_RATE_ERR | R | 0b | Flag indicating that clock configuration does not allow valid DEM rate.<br>0d = No DEM clock rate error<br>1d = DEM clock rate error in selected clock configuration |
| 2 | PDM_CLK_ERR | R | 0b | Flag indicating that clock configuration does not allow valid PDM clock generation.<br>0d = No PDM clock generation error<br>1d = PDM clock generation error in selected clock configuration |
| 1 | RESET_ON_CLK_STOP_DET_STS | R | 0b | Flag indicating that audio clock source stopped for atleast 1ms.<br>0d = No audio clock source error<br>1d = Audio clock source stopped for atleast 1ms |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.1.52 CLK_ERR_STS1 Register (Address = 0x3D) [Reset = 0x00]

CLK_ERR_STS1 is shown in Table 7-79.

Return to the Summary Table.

This register is the clock error and status register 1.

**Table 7-79. CLK_ERR_STS1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | PASI_BCLK_FS_RATIO_ERR | R | 0b | Flag indicating PASI bclk fsync ratio error.<br>0d = No PASI bclk fsync ratio error<br>1d = PASI bclk fsync ratio error in selected clock configuration |
| 6 | SASI_BCLK_FS_RATIO_ERR | R | 0b | Flag indicating SASI bclk fsync ratio error.<br>0d = No SASI bclk fsync ratio error<br>1d = SASI bclk fsync ratio error in selected clock configuration |

**ADVANCE INFORMATION**

**Table 7-79. CLK_ERR_STS1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 5 | CCLK_FS_RATIO_ERR | R | 0b | Flag indicating CCLK fsync ratio error.<br>0d = No CCLK fsync ratio error<br>1d = CCLK fsync ratio error |
| 4 | PASI_FS_ERR | R | 0b | Flag indicating PASI FS rate change or halt error.<br>0d = No PASI FS error<br>1d = PASI FS rate change or halt detected |
| 3 | SASI_FS_ERR | R | 0b | Flag indicating SASI FS rate change or halt error.<br>0d = No SASI FS error<br>1d = SASI FS rate change or halt detected |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset values |

**7.5.1.53 CLK_DET_STS0 Register (Address = 0x3E) [Reset = 0x00]**

CLK_DET_STS0 is shown in Table 7-80.

Return to the Summary Table.

This register is the clock ratio detection register 0.

**ADVANCE INFORMATION**

ADVANCE INFORMATION

**Table 7-80. CLK_DET_STS0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | PASI_SAMP_RATE_STS[5:0] | R | 000000b | Primary ASI Sample rate detected status.<br>0d = Reserved<br>1d = 768000 (670320-791040)<br>2d = 614400 (536256-632832)<br>3d = 512000 (446880-527360)<br>4d = 438857 (383040-452022)<br>5d = 384000 (335160-395520)<br>6d = 341333 (297920-351573)<br>7d = 307200 (268128-316416)<br>8d = 256000 (223440-263680)<br>9d = 219429 (191520-226011)<br>10d = 192000 (167580-197760)<br>11d = 170667 (148960-175786)<br>12d = 153600 (134064-158208)<br>13d = 128000 (111720-131840)<br>14d = 109714 (95760-113005)<br>15d = 96000 (83790-98880)<br>16d = 85333 (74480-87893)<br>17d = 76800 (67032-79104)<br>18d = 64000 (55860-65920)<br>19d = 54857 (47880-56502)<br>20d = 48000 (41895-49440)<br>21d = 42667 (37240-43946)<br>22d = 38400 (33516-39552)<br>23d = 32000 (27930-32960)<br>24d = 27429 (23940-28251)<br>25d = 24000 (20947-24720)<br>26d = 21333 (18620-21973)<br>27d = 19200 (16758-19776)<br>28d = 16000 (13965-16480)<br>29d = 13714 (11970-14125)<br>30d = 12000 (10473-12360)<br>31d = 10667 (9310-10986)<br>32d = 9600 (8379-9888)<br>33d = 8000 (6982-8240)<br>34d = 6857 (5985-7062)<br>35d = 6000 (5236-6180)<br>36d = 5333 (4655-5493)<br>37d = 4800 (4189-4944)<br>38d = 4000 (3491-4120)<br>39d = 3429 (2992-3531)<br>40d = 3000 (2618-3090)<br>41d-63d = Reserved |
| 1-0 | PLL_MODE_STS[1:0] | R | 00b | PLL usage status.<br>0d = PLL used in integer mode<br>1d = PLL used in fractional mode<br>2d = PLL not used<br>3d = Reserved |

### 7.5.1.54 CLK_DET_STS1 Register (Address = 0x3F) [Reset = 0x00]

CLK_DET_STS1 is shown in Table 7-81.

Return to the Summary Table.

This register is the clock ratio detection register 1.

**Table 7-81. CLK_DET_STS1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | SASI_SAMP_RATE_STS[5:0] | R | 000000b | Secondary ASI Sample rate detected status.<br>0d = Reserved<br>1d = 768000 (670320-791040)<br>2d = 614400 (536256-632832)<br>3d = 512000 (446880-527360)<br>4d = 438857 (383040-452022)<br>5d = 384000 (335160-395520)<br>6d = 341333 (297920-351573)<br>7d = 307200 (268128-316416)<br>8d = 256000 (223440-263680)<br>9d = 219429 (191520-226011)<br>10d = 192000 (167580-197760)<br>11d = 170667 (148960-175786)<br>12d = 153600 (134064-158208)<br>13d = 128000 (111720-131840)<br>14d = 109714 (95760-113005)<br>15d = 96000 (83790-98880)<br>16d = 85333 (74480-87893)<br>17d = 76800 (67032-79104)<br>18d = 64000 (55860-65920)<br>19d = 54857 (47880-56502)<br>20d = 48000 (41895-49440)<br>21d = 42667 (37240-43946)<br>22d = 38400 (33516-39552)<br>23d = 32000 (27930-32960)<br>24d = 27429 (23940-28251)<br>25d = 24000 (20947-24720)<br>26d = 21333 (18620-21973)<br>27d = 19200 (16758-19776)<br>28d = 16000 (13965-16480)<br>29d = 13714 (11970-14125)<br>30d = 12000 (10473-12360)<br>31d = 10667 (9310-10986)<br>32d = 9600 (8379-9888)<br>33d = 8000 (6982-8240)<br>34d = 6857 (5985-7062)<br>35d = 6000 (5236-6180)<br>36d = 5333 (4655-5493)<br>37d = 4800 (4189-4944)<br>38d = 4000 (3491-4120)<br>39d = 3429 (2992-3531)<br>40d = 3000 (2618-3090)<br>41d-63d = Reserved |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset values |

### 7.5.1.55 CLK_DET_STS2 Register (Address = 0x40) [Reset = 0x00]

CLK_DET_STS2 is shown in Table 7-82.

Return to the Summary Table.

This register is the clock ratio detection register 2.

**Table 7-82. CLK_DET_STS2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset values |
| 5-0 | FS_CLKSRC_RATIO_DET_MSB_STS[5:0] | R | 000000b | MSB bits for primary ASI or secondary ASI FSYNC to clock source ratio detected. |

ADVANCE INFORMATION

### 7.5.1.56 CLK_DET_STS3 Register (Address = 0x41) [Reset = 0x00]

CLK_DET_STS3 is shown in Table 7-83.

Return to the Summary Table.

This register is the clock ratio detection register 3.

**Table 7-83. CLK_DET_STS3 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | FS_CLKSRC_RATIO_DET_LSB_STS[7:0] | R | 00000000b | LSB byte for primary ASI or secondary ASI FSYNC to clock source ratio detected. |

### 7.5.1.57 INT_CFG Register (Address = 0x42) [Reset = 0x00]

INT_CFG is shown in Table 7-84.

Return to the Summary Table.

This regiser is the interrupt configuration register.

**Table 7-84. INT_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | INT_POL | R/W | 0b | Interrupt polarity.<br>0b = Active low (IRQZ)<br>1b = Active high (IRQ) |
| 6-5 | INT_EVENT[1:0] | R/W | 00b | Interrupt event configuration.<br>0d = INT asserts on any unmasked latched interrupts event<br>1d = INT asserts on any unmasked live interrupts event<br>2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event<br>3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event |
| 4-3 | PD_ON_FLT_CFG[1:0] | R/W | 00b | Powerdown configuration during fault for chx and micbias.<br>0d = Faults are not considered for power down<br>1d = Only unmasked faults are considered for power down<br>2d = All faults are considered for powerdown<br>3d = Reserved |
| 2 | LTCH_READ_CFG | R/W | 0b | Interrupt latch registers readback configuration.<br>0b = All interrupts can be read through the LTCH registers<br>1b = Only unmasked interrupts can be read through the LTCH registers |
| 1 | PD_ON_FLT_RCV_CFG | R/W | 0b | Configuration for Powerdown ADC channels on fault<br>0b = Auto recovery, ADC channels are re-powered up when fault goes away<br>1b = Manual recovery, ADC channels are not re-powered up when fault goes away |
| 0 | LTCH_CLR_ON_READ | R/W | 0b | Cfgn for clearing LTCH register bits<br>0 = LTCH reg bits are cleared on reg read only if live status is zero<br>1 = LTCH reg bits are cleared on reg read irrespective of live status |

### 7.5.1.58 DAC_FLT_CFG Register (Address = 0x43) [Reset = 0x50]

DAC_FLT_CFG is shown in Table 7-85.

Return to the Summary Table.

This regiser is the interrupt configuration register.

**Table 7-85. DAC_FLT_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | DAC_PD_ON_FLT_CFG[1:0] | R/W | 10b | Powerdown configuration during fault for DAC . <br>0d = Faults are not considered for power down<br>1d = Only unmasked faults are considered for power down<br>2d = All faults are considered for powerdown<br>3d = Reserved |
| 4 | DAC_PD_ON_FLT_RCV_CFG | R/W | 1b | Configuration for Powerdown DAC channels on fault<br>0b = Auto recovery, DAC channels are re-powered up when fault goes away<br>1b = Manual recovery, DAC channels are not re-powered up when fault goes away |
| 3 | OUT_CHx_PD_FLT_STS | R | 0b | Status for PD on OUTxx faults<br>0d = No DAC Channel is Powered Down due to fault/s<br>1d = Some DAC Channel is Powered Down due to fault/s |
| 2 | DAC_DIS_PD_W_PU | R/W | 0b | Disable power down on DRVR VG fault while powering up DAC<br>0b = Power down DAC on DRVR VG fault while power up<br>1b = Disable power down DAC on DRVR VG fault while power up |
| 1 | DAC_FLT_DET_DIS | R/W | 0b | DAC vg_fault/sc_fault detect config<br>0b = enable<br>1b = disable |
| 0 | AREG_SC_FLAG_DET_DIS | R/W | 0b | AREG short circuit detect config<br>0b = enable<br>1b = disable |

### 7.5.1.59 PWR_TUNE_CFG1 Register (Address = 0x4F) [Reset = 0x00]

PWR_TUNE_CFG1 is shown in Table 7-86.

Return to the Summary Table.

This register is configuration register for power tune configuration.

**Table 7-86. PWR_TUNE_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | DAC_CLK_BY2_MODE | R/W | 0b | DAC MOD CLK select configuration.<br>0d = MOD CLK 3MHz<br>1d = MOD CLK 1.5MHz |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | DAC_FIR_SEG_BYPASS | R/W | 0b | DAC FIR and segmenter bypass configuration.<br>0d = Bypass disable<br>1d = Bypass enable |
| 4-3 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 2 | DAC_LOW_PWR_FILT | R/W | 0b | Low Power Filter configuration for DAC<br>0d = Disable<br>1d = Enable |
| 1 | DAC_POWER_SCAL | R/W | 0b | DAC IREF select configuration.<br>0d = Vref/R<br>1d = Vref/2R |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.1.60 OUT1x_CFG0 Register (Address = 0x64) [Reset = 0x20]

OUT1x_CFG0 is shown in Table 7-87.

Return to the Summary Table.

ADVANCE INFORMATION

ADVANCE INFORMATION

This register is configuration register 0 for Channel OUT1x.

### Table 7-87. OUT1x_CFG0 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-5 | OUT1x_SRC[2:0] | R/W | 001b | OUT1x Source Configuration.<br>0d = Output driver disabled<br>1d = Input from DAC signal chain<br>2d = Input from Analog bypass path<br>3d = Input from both DAC signal chain and Analog bypass path<br>4d = Independent input from both DAC signal chain and Analog bypass path (DAC -> OUT1P , IN1P -> OUT1M)<br>5d = Independent input from both DAC signal chain and Analog bypass path (IN1M -> OUT1P, DAC -> OUT1M)<br>6d-7d = Reserved; Don't use |
| 4-2 | OUT1x_CFG[2:0] | R/W | 000b | OUT1x DAC / Analog Bypass Routing Configuration. (Don't use if OUT1x_SRC configured 4d or 5d)<br>0d = Differential (DAC1AP + DAC1BP / IN1M -> OUT1P ; DAC1AM + DAC1BM / IN1P -> OUT1M)<br>1d = Stereo single-ended (DAC1A / IN1M -> OUT1P ; DAC1B / IN1P -> OUT1M)<br>2d = Mono single-ended with output at OUT1P only (DAC1A + DAC1B / IN1M-> OUT1P)<br>3d = Mono single-ended with output at OUT1M only (DAC1A + DAC1B / IN1P -> OUT1M)<br>4d = Pseudo differential with OUT1M as VCOM (DAC1A, DAC1B / IN1M -> OUT1P, VCOM -> OUT1M)<br>5d = Pseudo differential with OUT1M as VCOM and OUT2M for external sensing (DAC1A, DAC1B / IN1M -> OUT1P, VCOM -> OUT1M)<br>6d = Pseudo differential with OUT1P as VCOM (IN1P -> OUT1M, VCOM -> OUT1P)<br>7d = Reserved; Don't use |
| 1 | OUT1x_VCOM | R/W | 0b | Channel OUT1x VCOM configuration.<br>0d = 0.6 * Vref (for 1.375V VREF mode alone as 0.654*Vref)<br>1d = AVDD by 2 |
| 0 | OUT1x_LP_MODE | R/W | 0b | Low power mode of OUT1x channel. (only valid for OUT1x_SRC configured as DAC signal chain) (not valid for OUT1x_CFG configured as Stereo SE)<br>0d = Low power mode is disabled (3 dB higher perf)<br>1d = Low power mode is enabled |

### 7.5.1.61 OUT1x_CFG1 Register (Address = 0x65) [Reset = 0x20]

OUT1x_CFG1 is shown in Table 7-88.

Return to the Summary Table.

This register is configuration register 1 for Channel OUT1x.

### Table 7-88. OUT1x_CFG1 Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | OUT1P_DRIVE[1:0] | R/W | 00b | Channel OUT1P drive configuration.<br>0d = Line out driver with minimum 300 Ω impedance<br>1d = Headphone driver with minimum 4 Ω impedance<br>2d = 4 Ω<br>3d = FD Receiver/Debug |

Product Folder Links: *TAD5212*

**Table 7-88. OUT1x_CFG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 5-3 | OUT1P_LVL_CTRL[2:0] | R/W | 100b | Channel OUT1P level control configuration.<br>0d = 24 dB (only for DAC sigchain SE)<br>1d = 18 dB (only for DAC sigchain)<br>2d = 12 dB (DAC sigchain -> RFB 80K if RIN=20k configured)<br>3d = 6 dB (DAC sigchain -> RFB 40K if RIN=20k configured)<br>4d = 0 dB (DAC sigchain -> RFB 20K if RIN=20k configured)<br>5d = -6 dB (DAC sigchain -> RFB 10K if RIN=20k configured)<br>6d = -12 dB (available for Rin 4.4-kΩ only)<br>7d = Reserved; Don't use |
| 2 | AIN1M_BYP_IMP | R/W | 0b | AIN1M Analog Bypass input impedance.<br>0d = 4.4-kΩ<br>1d = 20-kΩ |
| 1 | AIN1x_BYP_CFG | R/W | 0b | IN1x Analog Bypass input config.<br>0d = FD / Pseudo Diff<br>1d = SE |
| 0 | DAC_CH1_BW_MODE | R/W | 0b | DAC Channel 1 band-width selection.<br>0d = audio band-width (24 kHz mode)<br>1d = wide band-width (96 kHz mode) |

### 7.5.1.62 OUT1x_CFG2 Register (Address = 0x66) [Reset = 0x20]

OUT1x_CFG2 is shown in Table 7-89.

Return to the Summary Table.

This register is configuration register 2 for Channel OUT2x.

**Table 7-89. OUT1x_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | OUT1M_DRIVE[1:0] | R/W | 00b | Channel OUT1M drive configuration.<br>0d = Line out driver with minimum 300 Ω impedance<br>1d = Headphone driver with minimum 4 Ω impedance<br>2d = 4 Ω<br>3d = FD Receiver/Debug |
| 5-3 | OUT1M_LVL_CTRL[2:0] | R/W | 100b | Channel OUT1M level control configuration.<br>0d = 24 dB (only for DAC sigchain SE)<br>1d = 18 dB (only for DAC sigchain)<br>2d = 12 dB (DAC sigchain -> RFB 80K if RIN=20k configured)<br>3d = 6 dB (DAC sigchain -> RFB 40K if RIN=20k configured)<br>4d = 0 dB (DAC sigchain -> RFB 20K if RIN=20k configured)<br>5d = -6 dB (DAC sigchain -> RFB 10K if RIN=20k configured)<br>6d = -12 dB (available for Rin 4.4-kΩ only)<br>7d = Reserved; Don't use |
| 2 | AIN1P_BYP_IMP | R/W | 0b | AIN1P Analog Bypass input impedance.<br>0d = 4.4-kΩ<br>1d = 20-kΩ |
| 1 | DAC_CH1_FULLSCALE_VAL | R/W | 0b | DAC Channel 1 Fullscale value for VREF=2.75 V (applicable for the analog input).<br>0d = 2 Vrms differential ( 1 Vrms for single ended operation)<br>1d = 4 Vrms differential ( 2 Vrms for single ended operation) (For AC-coupled configuration external biasing is required for input common mode, this mode supported with common mode variance tolerance rail to rail) (only 2.75 VREF supported, only supported in audio band-width mode) |

**ADVANCE INFORMATION**

**Table 7-89. OUT1x_CFG2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 0 | DAC_CH1_CM_TOL | R/W | 0b | DAC Channel 1 input coupling (applicable for the analog input).<br>0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration<br>1d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) |

### 7.5.1.63 DAC_CH1A_CFG0 Register (Address = 0x67) [Reset = 0xC9]

DAC_CH1A_CFG0 is shown in Table 7-90.

Return to the Summary Table.

This register is configuration register 0 for DAC channel 1A.

**Table 7-90. DAC_CH1A_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | DAC_CH1A_DVOL[7:0] | R/W | 11001001b | Channel 1A digital volume control.<br>0d = Digtial Volume is muted<br>1d = Digital Volume Control set to -100 dB<br>2d = Digital Volume Control set to -99.5 dB<br>3d to 200d = Digital Volume Control set to as per configuration<br>201d = Digital Volume Control set to 0 dB<br>202d = Digital Volume Control set to +0.5 dB<br>203d to 253d = Digital Volume Control set to as per configuration<br>254d = Digital Volume Control set to +26.5 dB<br>255d = Digital Volume Control set to +27 dB |

### 7.5.1.64 DAC_CH1A_CFG1 Register (Address = 0x68) [Reset = 0x80]

DAC_CH1A_CFG1 is shown in Table 7-91.

Return to the Summary Table.

This register is configuration register 1 for DAC channel 1A.

**Table 7-91. DAC_CH1A_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | DAC_CH1A_FGAIN[3:0] | R/W | 1000b | DAC channel 1A fine gain calibration.<br>0d = Fine gain is set to -0.8 dB<br>1d = Fine gain is set to -0.7 dB<br>2d = Fine gain is set to -0.6 dB<br>3d to 7d = Fine gain is set as per configuration<br>8d = Fine gain is set to 0 dB<br>9d = Fine gain is set to 0.1 dB<br>10d to 13d = Fine gain is set as per configuration<br>14d = Fine gain is set to 0.6 dB<br>15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

### 7.5.1.65 DAC_CH1B_CFG0 Register (Address = 0x69) [Reset = 0xC9]

DAC_CH1B_CFG0 is shown in Table 7-92.

Return to the Summary Table.

This register is configuration register 0 for DAC channel 1B.

Product Folder Links: *TAD5212*

**ADVANCE INFORMATION**

**Table 7-92. DAC_CH1B_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | DAC_CH1B_DVOL[7:0] | R/W | 11001001b | Channel 1B digital volume control.<br>0d = Digtial Volume is muted<br>1d = Digital Volume Control set to -100 dB<br>2d = Digital Volume Control set to -99.5 dB<br>3d to 200d = Digital Volume Control set to as per configuration<br>201d = Digital Volume Control set to 0 dB<br>202d = Digital Volume Control set to +0.5 dB<br>203d to 253d = Digital Volume Control set to as per configuration<br>254d = Digital Volume Control set to +26.5 dB<br>255d = Digital Volume Control set to +27 dB |

### 7.5.1.66 DAC_CH1B_CFG1 Register (Address = 0x6A) [Reset = 0x80]

DAC_CH1B_CFG1 is shown in Table 7-93.

Return to the Summary Table.

This register is configuration register 1 for DAC channel 1B.

**Table 7-93. DAC_CH1B_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | DAC_CH1B_FGAIN[3:0] | R/W | 1000b | DAC channel 1B fine gain calibration.<br>0d = Fine gain is set to -0.8 dB<br>1d = Fine gain is set to -0.7 dB<br>2d = Fine gain is set to -0.6 dB<br>3d to 7d = Fine gain is set as per configuration<br>8d = Fine gain is set to 0 dB<br>9d = Fine gain is set to 0.1 dB<br>10d to 13d = Fine gain is set as per configuration<br>14d = Fine gain is set to 0.6 dB<br>15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

### 7.5.1.67 OUT2x_CFG0 Register (Address = 0x6B) [Reset = 0x20]

OUT2x_CFG0 is shown in Table 7-94.

Return to the Summary Table.

This register is configuration register 0 for Channel OUT2x.

**Table 7-94. OUT2x_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-5 | OUT2x_SRC[2:0] | R/W | 001b | OUT2x Source Configuration.<br>0d = Output driver disabled<br>1d = Input from DAC signal chain<br>2d = Input from Analog bypass path<br>3d = Input from both DAC signal chain and Analog bypass path<br>4d = Independent input from both DAC signal chain and Analog bypass path (DAC -> OUT2P , IN2P -> OUT2M)<br>5d = Independent input from both DAC signal chain and Analog bypass path (IN2M -> OUT2P, DAC -> OUT2M)<br>6d-7d = Reserved; Don't use |

ADVANCE INFORMATION

**Table 7-94. OUT2x_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4-2 | OUT2x_CFG[2:0] | R/W | 000b | OUT2x DAC / Analog Bypass Routing Configuration. (Don't use if OUT1x_SRC configured 4d or 5d)<br>0d = Differential (DAC2AP + DAC2BP / IN2M -> OUT2P ; DAC2AM + DAC2BM / IN2P -> OUT2M)<br>1d = Stereo single-ended (DAC2A / IN2M -> OUT2P ; DAC2B / IN2P -> OUT2M)<br>2d = Mono single-ended with output at OUT2P only (DAC2A + DAC2B / IN2M-> OUT2P)<br>3d = Mono single-ended with output at OUT2M only (DAC2A + DAC2B / IN2P -> OUT2M)<br>4d = Pseudo differential with OUT2M as VCOM (DAC2A, DAC2B / IN2M -> OUT2P, VCOM -> OUT2M)<br>5d =Reserved; Don't use<br>6d = Pseudo differential with OUT2P as VCOM (IN2P -> OUT2M, VCOM -> OUT2P)<br>7d = Reserved; Don't use |
| 1 | OUT2x_VCOM | R/W | 0b | Channel OUT2x VCOM configuration.<br>0d = 0.6 * Vref (for 1.375V VREF mode alone as 0.654*Vref)<br>2d = AVDD by 2 |
| 0 | OUT2x_LP_MODE | R/W | 0b | Low power mode of OUT2x channel. (only valid for OUT2x_SRC configured as DAC signal chain) (not valid for OUT2x_CFG configured as Stereo SE)<br>0d = Low power mode is disabled (3 dB higher perf)<br>1d = Low power mode is enabled |

### 7.5.1.68 OUT2x_CFG1 Register (Address = 0x6C) [Reset = 0x20]

OUT2x_CFG1 is shown in Table 7-95.

Return to the Summary Table.

This register is configuration register 1 for Channel OUT2x.

**Table 7-95. OUT2x_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | OUT2P_DRIVE[1:0] | R/W | 00b | Channel OUT2P drive configuration.<br>0d = Line out driver with minimum 300 Ω impedance<br>1d = Headphone driver with minimum 4 Ω impedance<br>2d = 4 Ω<br>3d = FD Receiver/Debug |
| 5-3 | OUT2P_LVL_CTRL[2:0] | R/W | 100b | Channel OUT2P level control configuration<br>0d = 24 dB (only for DAC sigchain SE)<br>1d = 18 dB (only for DAC sigchain)<br>2d = 12 dB (DAC sigchain -> RFB 80K if RIN=20k configured)<br>3d = 6 dB (DAC sigchain -> RFB 40K if RIN=20k configured)<br>4d = 0 dB (DAC sigchain -> RFB 20K if RIN=20k configured)<br>5d = -6 dB (DAC sigchain -> RFB 10K if RIN=20k configured)<br>6d = -12 dB (available for Rin 4.4-kΩ only)<br>7d = Reserved; Don't use |
| 2 | AIN2M_BYP_IMP | R/W | 0b | AIN2M Analog Bypass input impedance.<br>0d = 4.4-kΩ<br>1d = 20-kΩ |
| 1 | AIN2x_BYP_CFG | R/W | 0b | IN2x Analog Bypass input config.<br>0d = FD / Pseudo Diff<br>1d = SE |
| 0 | DAC_CH2_BW_MODE | R/W | 0b | DAC Channel 2 band-width selection.<br>0d = audio band-width (24 kHz mode)<br>1d = wide band-width (96 kHz mode) |

### 7.5.1.69 OUT2x_CFG2 Register (Address = 0x6D) [Reset = 0x20]

OUT2x_CFG2 is shown in Table 7-96.

Return to the Summary Table.

This register is configuration register 2 for Channel OUT2x.

**Table 7-96. OUT2x_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | OUT2M_DRIVE[1:0] | R/W | 00b | Channel OUT2M drive configuration.<br>0d = Line out driver with minimum 300 Ω impedance<br>1d = Headphone driver with minimum 4 Ω impedance<br>2d = 4 Ω<br>3d = FD Receiver/Debug |
| 5-3 | OUT2M_LVL_CTRL[2:0] | R/W | 100b | Channel OUT2M level control configuration.<br>0d = 24 dB (only for DAC sigchain SE)<br>1d = 18 dB (only for DAC sigchain)<br>2d = 12 dB (DAC sigchain -> RFB 80K if RIN=20k configured)<br>3d = 6 dB (DAC sigchain -> RFB 40K if RIN=20k configured)<br>4d = 0 dB (DAC sigchain -> RFB 20K if RIN=20k configured)<br>5d = -6 dB (DAC sigchain -> RFB 10K if RIN=20k configured)<br>6d = -12 dB (available for Rin 4.4-kΩ only)<br>7d = Reserved; Don't use |
| 2 | AIN2P_BYP_IMP | R/W | 0b | AIN2P Analog Bypass input impedance.<br>0d = 4.4-kΩ<br>1d = 20-kΩ |
| 1 | DAC_CH2_FULLSCALE_VAL | R/W | 0b | DAC Channel 2 Fullscale value for VREF=2.75 V (applicable for the analog input).<br>0d = 2 Vrms differential ( 1 Vrms for single ended operation)<br>1d = 4 Vrms differential ( 2 Vrms for single ended operation) (For AC-coupled configuration external biasing is required for input common mode, this mode supported with common mode variance tolerance rail to rail) (only 2.75 VREF supported, only supported in audio band-width mode) |
| 0 | DAC_CH2_CM_TOL | R/W | 0b | DAC Channel 2 input coupling (applicable for the analog input).<br>0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration<br>1d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) |

### 7.5.1.70 DAC_CH2A_CFG0 Register (Address = 0x6E) [Reset = 0xC9]

DAC_CH2A_CFG0 is shown in Table 7-97.

Return to the Summary Table.

This register is configuration register 0 for DAC channel 2A.

**Table 7-97. DAC_CH2A_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DAC_CH2A_DVOL[7:0] | R/W | 11001001b | Channel 2A digital volume control.<br>0d = Digtial Volume is muted<br>1d = Digital Volume Control set to -100 dB<br>2d = Digital Volume Control set to -99.5 dB<br>3d to 200d = Digital Volume Control set to as per configuration<br>201d = Digital Volume Control set to 0 dB<br>202d = Digital Volume Control set to +0.5 dB<br>203d to 253d = Digital Volume Control set to as per configuration<br>254d = Digital Volume Control set to +26.5 dB<br>255d = Digital Volume Control set to +27 dB |

**ADVANCE INFORMATION**

**ADVANCE INFORMATION**

### 7.5.1.71 DAC_CH2A_CFG1 Register (Address = 0x6F) [Reset = 0x80]

DAC_CH2A_CFG1 is shown in Table 7-98.

Return to the Summary Table.

This register is configuration register 1 for DAC channel 2A.

**Table 7-98. DAC_CH2A_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | DAC_CH2A_FGAIN[3:0] | R/W | 1000b | DAC channel 2A fine gain calibration.<br>0d = Fine gain is set to -0.8 dB<br>1d = Fine gain is set to -0.7 dB<br>2d = Fine gain is set to -0.6 dB<br>3d to 7d = Fine gain is set as per configuration<br>8d = Fine gain is set to 0 dB<br>9d = Fine gain is set to 0.1 dB<br>10d to 13d = Fine gain is set as per configuration<br>14d = Fine gain is set to 0.6 dB<br>15d = Fine gain is set to 0.7 dB |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

### 7.5.1.72 DAC_CH2B_CFG0 Register (Address = 0x70) [Reset = 0xC9]

DAC_CH2B_CFG0 is shown in Table 7-99.

Return to the Summary Table.

This register is configuration register 0 for DAC channel 2B.

**Table 7-99. DAC_CH2B_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | DAC_CH2B_DVOL[7:0] | R/W | 11001001b | Channel 2B digital volume control.<br>0d = Digtial Volume is muted<br>1d = Digital Volume Control set to -100 dB<br>2d = Digital Volume Control set to -99.5 dB<br>3d to 200d = Digital Volume Control set to as per configuration<br>201d = Digital Volume Control set 0 dB<br>202d = Digital Volume Control set to +0.5 dB<br>203d to 253d = Digital Volume Control set to as per configuration<br>254d = Digital Volume Control set to +26.5 dB<br>255d = Digital Volume Control set to +27 dB |

### 7.5.1.73 DAC_CH2B_CFG1 Register (Address = 0x71) [Reset = 0x80]

DAC_CH2B_CFG1 is shown in Table 7-100.

Return to the Summary Table.

This register is configuration register 1 for DAC channel 2B.

**Table 7-100. DAC_CH2B_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | DAC_CH2B_FGAIN[3:0] | R/W | 1000b | DAC channel 2B fine gain calibration.<br>0d = Fine gain is set to -0.8 dB<br>1d = Fine gain is set to -0.7 dB<br>2d = Fine gain is set to -0.6 dB<br>3d to 7d = Fine gain is set as per configuration<br>8d = Fine gain is set to 0 dB<br>9d = Fine gain is set to 0.1 dB<br>10d to 13d = Fine gain is set as per configuration<br>14d = Fine gain is set to 0.6 dB<br>15d = Fine gain is set to 0.7 dB |

Product Folder Links: *TAD5212*

**Table 7-100. DAC_CH2B_CFG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

### 7.5.1.74 DSP_CFG1 Register (Address = 0x73) [Reset = 0x18]

DSP_CFG1 is shown in Table 7-101.

Return to the Summary Table.

This register is the digital signal processor (DSP) configuration register 0.

**Table 7-101. DSP_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | DAC_DSP_INTX_FILT[1:0] | R/W | 00b | DAC channel decimation filter response.<br>0d = Linear phase<br>1d = Low latency<br>2d = Ultra-low latency<br>3d = Reserved; Don't use |
| 5-4 | DAC_DSP_HPF_SEL[1:0] | R/W | 01b | DAC channel high-pass filter (HPF) selection.<br>0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P17_R120-127 and P18_R8-11 set as the all-pass filter<br>1d = HPF with a cutoff of 0.00002 x $f_S$ (1 Hz at $f_S$ = 48 kHz) is selected<br>2d = HPF with a cutoff of 0.00025 x $f_S$ (12 Hz at $f_S$ = 48 kHz) is selected<br>3d = HPF with a cutoff of 0.002 x $f_S$ (96 Hz at $f_S$ = 48 kHz) is selected |
| 3-2 | DAC_DSP_BQ_CFG[1:0] | R/W | 10b | Number of biquads per DAC channel configuration.<br>0d = No biquads per channel; biquads are all disabled<br>1d = 1 biquad per channel<br>2d = 2 biquads per channel<br>3d = 3 biquads per channel |
| 1 | DAC_DSP_DISABLE_SOFT_STEP | R/W | 0b | DAC Soft-stepping disable during DVOL change, mute, and unmute.<br>0d = Soft-stepping enabled<br>1d = Soft-stepping disabled |
| 0 | DAC_DSP_DVOL_GANG | R/W | 0b | DVOL control ganged across DAC channels.<br>0d = Each DAC channel has its own DVOL CTRL settings as programmed in the DAC_CHx_DVOL bits<br>1d = All active channels must use the channel 1 DVOL setting (DAC_CH1_DVOL) irrespective of whether channel 1 is turned on or not |

### 7.5.1.75 CH_EN Register (Address = 0x76) [Reset = 0xCC]

CH_EN is shown in Table 7-102.

Return to the Summary Table.

This register is the channel enable configuration register.

**Table 7-102. CH_EN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

ADVANCE INFORMATION

**Table 7-102. CH_EN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 3 | OUT_CH1_EN | R/W | 1b | Output channel 1 enable setting.<br>0d = Output channel 1 is disabled<br>1d = Output channel 1 is enabled |
| 2 | OUT_CH2_EN | R/W | 1b | Output channel 2 enable setting.<br>0d = Output channel 2 is disabled<br>1d = Output channel 2 is enabled |
| 1 | OUT_CH3_EN | R/W | 0b | Output channel 3 enable setting.<br>0d = Output channel 3 is disabled<br>1d = Output channel 3 is enabled |
| 0 | OUT_CH4_EN | R/W | 0b | Output channel 4 enable setting.<br>0d = Output channel 4 is disabled<br>1d = Output channel 4 is enabled |

### 7.5.1.76 DYN_PUPD_CFG Register (Address = 0x77) [Reset = 0x00]

DYN_PUPD_CFG is shown in Table 7-103.

Return to the Summary Table.

This register is the power-up configuration register.

**Table 7-103. DYN_PUPD_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | DAC_DYN_PUPD_EN | R/W | 0b | Dynamic channel power-up, power-down enable for playback path.<br>0d = Channel power-up, power-down is not supported if any channel playback is on<br>1d = Channel can be powered up or down individually, even if channel playback is on |
| 4 | DAC_DYN_MAXCH_SEL | R/W | 0b | Dynamic mode maximum channel select configuration for playback path.<br>0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled<br>1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset value |

### 7.5.1.77 PWR_CFG Register (Address = 0x78) [Reset = 0x00]

PWR_CFG is shown in Table 7-104.

Return to the Summary Table.

This register is the power-up configuration register.

**Table 7-104. PWR_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | DAC_PDZ | R/W | 0b | Power control for DAC channels.<br>0d = Power down all DAC channels<br>1d = Power up all enabled DAC channels |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

Product Folder Links: *TAD5212*

ADVANCE INFORMATION

**Table 7-104. PWR_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | UAG_EN | R/W | 0b | Enable ultrasound activity detection (UAG) algorithm.<br>0d = UAG is disabled<br>1d = UAG is enabled |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.1.78 DEV_STS0 Register (Address = 0x79) [Reset = 0x00]

DEV_STS0 is shown in Table 7-105.

Return to the Summary Table.

This register is the device status value register 0.

**Table 7-105. DEV_STS0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | OUT_CH1_STATUS | R | 0b | DAC channel 1 power status.<br>0d = DAC channel is powered down<br>1d = DAC channel is powered up |
| 2 | OUT_CH2_STATUS | R | 0b | DAC channel 2 power status.<br>0d = DAC channel is powered down<br>1d = DAC channel is powered up |
| 1 | OUT_CH3_STATUS | R | 0b | DAC channel 3 power status.<br>0d = DAC channel is powered down<br>1d = DAC channel is powered up |
| 0 | OUT_CH4_STATUS | R | 0b | DAC channel 4 power status.<br>0d = DAC channel is powered down<br>1d = DAC channel is powered up |

### 7.5.1.79 DEV_STS1 Register (Address = 0x7A) [Reset = 0x80]

DEV_STS1 is shown in Table 7-106.

Return to the Summary Table.

This register is the device status value register 1.

**Table 7-106. DEV_STS1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | MODE_STS[2:0] | R | 100b | Device mode status.<br>0-3d = Reserved<br>4d = Device is in sleep mode or software shutdown mode<br>5d = Reserved<br>6d = Device is in active mode with all record and playback channels turned off<br>7d = Device is in active mode with at least one record or playback channel turned on |
| 4 | PLL_STS | R | 0b | PLL status.<br>0d = PLL is not enabled<br>1d = PLL is enabled |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |

ADVANCE INFORMATION

**Table 7-106. DEV_STS1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.1.80 I2C_CKSUM Register (Address = 0x7E) [Reset = 0x00]

I2C_CKSUM is shown in Table 7-107.

Return to the Summary Table.

This register returns the I$^2$C transactions checksum value.

**Table 7-107. I2C_CKSUM Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | I2C_CKSUM[7:0] | R/W | 00000000b | These bits return the I$^2$C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages. |

Product Folder Links: *TAD5212*

## 7.5.2 TAD5212_P1 Registers

Table 7-108 lists the memory-mapped registers for the TAD5212_P1 registers. All register offset addresses not listed in Table 7-108 should be considered as reserved locations and the register contents should not be modified.

**Table 7-108. TAD5212_P1 Registers**

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x0 | PAGE_CFG | Device page register | 0x00 | PAGE_CFG Register (Address = 0x0) [Reset = 0x00] |
| 0x3 | DSP_CFG0 | | 0x00 | DSP_CFG0 Register (Address = 0x3) [Reset = 0x00] |
| 0xD | CLK_CFG0 | | 0x00 | CLK_CFG0 Register (Address = 0xD) [Reset = 0x00] |
| 0xF | CHANNEL_CFG2 | | 0x00 | CHANNEL_CFG2 Register (Address = 0xF) [Reset = 0x00] |
| 0x17 | SRC_CFG0 | SRC configuration register 1 | 0x00 | SRC_CFG0 Register (Address = 0x17) [Reset = 0x00] |
| 0x18 | SRC_CFG1 | SRC configuration register 2 | 0x00 | SRC_CFG1 Register (Address = 0x18) [Reset = 0x00] |
| 0x19 | JACK_DET_CFG0 | JACK DET configuration register 0 | 0x00 | JACK_DET_CFG0 Register (Address = 0x19) [Reset = 0x00] |
| 0x1A | JACK_DET_CFG1 | JACK DET configuration register 1 | 0x00 | JACK_DET_CFG1 Register (Address = 0x1A) [Reset = 0x00] |
| 0x1B | JACK_DET_CFG2 | JACK DET configuration register 2 | 0x00 | JACK_DET_CFG2 Register (Address = 0x1B) [Reset = 0x00] |
| 0x1C | JACK_DET_CFG3 | JACK DET configuration register 3 | 0x00 | JACK_DET_CFG3 Register (Address = 0x1C) [Reset = 0x00] |
| 0x1F | LPSG_CFG1 | LPSG | 0x80 | LPSG_CFG1 Register (Address = 0x1F) [Reset = 0x80] |
| 0x20 | LPSG_CFG1 | LPSG configuration register 1 | 0x00 | LPSG_CFG1 Register (Address = 0x1F) [Reset = 0x80] |
| 0x23 | LIMITER_CFG | Limiter configuration register 2 | 0x00 | LIMITER_CFG Register (Address = 0x23) [Reset = 0x00] |
| 0x2B | PLIM_CFG0 | PLIM configuration register 0 | 0x00 | PLIM_CFG0 Register (Address = 0x2B) [Reset = 0x00] |
| 0x2C | MIXER_CFG0 | MISC configuration register 0 | 0x00 | MIXER_CFG0 Register (Address = 0x2C) [Reset = 0x00] |

**ADVANCE INFORMATION**

Product Folder Links: TAD5212

**Table 7-108. TAD5212_P1 Registers (continued)**

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x2D | MISC_CFG0 | MISC configuration register 0 | 0x00 | MISC_CFG0 Register (Address = 0x2D) [Reset = 0x00] |
| 0x2E | BRWNOUT | | 0xBF | BRWNOUT Register (Address = 0x2E) [Reset = 0xBF] |
| 0x2F | INT_MASK0 | Interrupt Mask Register-0 | 0xFF | INT_MASK0 Register (Address = 0x2F) [Reset = 0xFF] |
| 0x32 | INT_MASK4 | Interrupt Mask Register-3 | 0x00 | INT_MASK4 Register (Address = 0x32) [Reset = 0x00] |
| 0x33 | INT_MASK5 | Interrupt Mask Register-3 | 0x30 | INT_MASK5 Register (Address = 0x33) [Reset = 0x30] |
| 0x34 | INT_LTCH0 | Latched Interrupt Readback Register-0 | 0x00 | INT_LTCH0 Register (Address = 0x34) [Reset = 0x00] |
| 0x35 | CHx_LTCH | Summary of Diagnostics | 0x00 | CHx_LTCH Register (Address = 0x35) [Reset = 0x00] |
| 0x38 | OUT_CH1_LTCH | | 0x00 | OUT_CH1_LTCH Register (Address = 0x38) [Reset = 0x00] |
| 0x39 | OUT_CH2_LTCH | | 0x00 | OUT_CH2_LTCH Register (Address = 0x39) [Reset = 0x00] |
| 0x3A | INT_LTCH1 | Latched Interrupt Readback Register-0 | 0x00 | INT_LTCH1 Register (Address = 0x3A) [Reset = 0x00] |
| 0x3B | INT_LTCH2 | Latched Interrupt Readback Register-3 | 0x00 | INT_LTCH2 Register (Address = 0x3B) [Reset = 0x00] |
| 0x3C | INT_LIVE0 | Live Interrupt Readback Register-0 | 0x00 | INT_LIVE0 Register (Address = 0x3C) [Reset = 0x00] |
| 0x3D | CHx_LIVE | Summary of Diagnostics | 0x00 | CHx_LIVE Register (Address = 0x3D) [Reset = 0x00] |
| 0x40 | OUT_CH1_LIVE | | 0x00 | OUT_CH1_LIVE Register (Address = 0x40) [Reset = 0x00] |
| 0x41 | OUT_CH2_LIVE | | 0x00 | OUT_CH2_LIVE Register (Address = 0x41) [Reset = 0x00] |
| 0x42 | INT_LIVE1 | Latched Interrupt Readback Register-0 | 0x00 | INT_LIVE1 Register (Address = 0x42) [Reset = 0x00] |
| 0x43 | INT_LIVE2 | Latched Interrupt Readback Register-3 | 0x00 | INT_LIVE2 Register (Address = 0x43) [Reset = 0x00] |
| 0x4E | DIAG_CFG8 | | 0xBA | DIAG_CFG8 Register (Address = 0x4E) [Reset = 0xBA] |

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

## Table 7-108. TAD5212_P1 Registers (continued)

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x4F | DIAG_CFG9 | | 0x4B | DIAG_CFG9 Register (Address = 0x4F) [Reset = 0x4B] |
| 0x54 | DIAG_CFG14 | | 0x48 | DIAG_CFG14 Register (Address = 0x54) [Reset = 0x48] |
| 0x55 | DIAGDATA_CFG | | 0x00 | DIAGDATA_CFG Register (Address = 0x55) [Reset = 0x00] |
| 0x62 | DIAG_MON_MSB_OUT1P | | 0x00 | DIAG_MON_MSB_OUT1P Register (Address = 0x62) [Reset = 0x00] |
| 0x63 | DIAG_MON_LSB_OUT1P | | 0x06 | DIAG_MON_LSB_OUT1P Register (Address = 0x63) [Reset = 0x06] |
| 0x64 | DIAG_MON_MSB_OUT1M | | 0x00 | DIAG_MON_MSB_OUT1M Register (Address = 0x64) [Reset = 0x00] |
| 0x65 | DIAG_MON_LSB_OUT1M | | 0x07 | DIAG_MON_LSB_OUT1M Register (Address = 0x65) [Reset = 0x07] |
| 0x66 | DIAG_MON_MSB_OUT2P | | 0x00 | DIAG_MON_MSB_OUT2P Register (Address = 0x66) [Reset = 0x00] |
| 0x67 | DIAG_MON_LSB_OUT2P | | 0x08 | DIAG_MON_LSB_OUT2P Register (Address = 0x67) [Reset = 0x08] |
| 0x68 | DIAG_MON_MSB_OUT2M | | 0x00 | DIAG_MON_MSB_OUT2M Register (Address = 0x68) [Reset = 0x00] |
| 0x69 | DIAG_MON_LSB_OUT2M | | 0x09 | DIAG_MON_LSB_OUT2M Register (Address = 0x69) [Reset = 0x09] |
| 0x6A | DIAG_MON_MSB_TEMP | | 0x00 | DIAG_MON_MSB_TEMP Register (Address = 0x6A) [Reset = 0x00] |
| 0x6B | DIAG_MON_LSB_TEMP | | 0x0A | DIAG_MON_LSB_TEMP Register (Address = 0x6B) [Reset = 0x0A] |
| 0x6E | DIAG_MON_MSB_AVDD | | 0x00 | DIAG_MON_MSB_AVDD Register (Address = 0x6E) [Reset = 0x00] |
| 0x6F | DIAG_MON_LSB_AVDD | | 0x0C | DIAG_MON_LSB_AVDD Register (Address = 0x6F) [Reset = 0x0C] |

**ADVANCE INFORMATION**

**ADVANCE INFORMATION**

**Table 7-108. TAD5212_P1 Registers (continued)**

| Address | Acronym | Register Name | Reset Value | Section |
|---|---|---|---|---|
| 0x70 | DIAG_MON_MSB_GPA | | 0x00 | DIAG_MON_MSB_GPA Register (Address = 0x70) [Reset = 0x00] |
| 0x71 | DIAG_MON_LSB_GPA | | 0x0D | DIAG_MON_LSB_GPA Register (Address = 0x71) [Reset = 0x0D] |

### 7.5.2.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in Table 7-109.

Return to the Summary Table.

The device memory map is divided into pages. This register sets the page.

**Table 7-109. PAGE_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PAGE[7:0] | R/W | 00000000b | These bits set the device page.<br>0d = Page 0<br>1d = Page 1<br>2d to 254d = Page 2 to page 254 respectively<br>255d = Page 255 |

### 7.5.2.2 DSP_CFG0 Register (Address = 0x3) [Reset = 0x00]

DSP_CFG0 is shown in Table 7-110.

Return to the Summary Table.

**Table 7-110. DSP_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | DIS_DVOL_OTF_CHG | R/W | 0b | Disable run-time changes to DVOL settings.<br>0d = Digital volume control changes supported while ADC is powered-on<br>1d = Digital volume control changes not supported while ADC is powered-on. |
| 0 | EN_BQ_OTF_CHG | R/W | 0b | Enable run-time changes to Biquad settings.<br>0d = Disable on the fly biquad changes<br>1d = Enable on the fly biquad changes |

### 7.5.2.3 CLK_CFG0 Register (Address = 0xD) [Reset = 0x00]

CLK_CFG0 is shown in Table 7-111.

Return to the Summary Table.

Product Folder Links: TAD5212

**Table 7-111. CLK_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CNT_TGT_CFG_OVR_PASI | R/W | 0b | ASI controller target Config Override Register<br>0d = controller-target Config as per PASI_CNT_CFG bit.<br>1d = Override the standard behavior of the PASI_CNT_CFG. In this case the clock auto detect feature is not available.<br>PASI_CNT_CFG = 0 : BCLK is input but FSYNC is output.<br>PASI_CNT_CFG = 1 : BCLK is output but FSYNC in input. |
| 6 | CNT_TGT_CFG_OVR_SASI | R/W | 0b | ASI controller target Config Override Register<br>0d = controller-target Config as per SASI_CNT_CFG bit.<br>1d = Override the standard behavior of the SASI_CNT_CFG. In this case the clock auto detect feature is not available.<br>SASI_CNT_CFG = 0 : BCLK is input but FSYNC is output.<br>SASI_CNT_CFG = 1 : BCLK is output but FSYNC in input. |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4-3 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 2 | PASI_USE_INT_FSYNC | R/W | 0b | For Primary use internal FSYNC in controller mode configuration.<br>0d = Use external FSYNC<br>1d = Use internal FSYNC |
| 1 | SASI_USE_INT_FSYNC | R/W | 0b | For Secondary use internal FSYNC in controller mode configuration.<br>0d = Use external FSYNC<br>1d = Use internal FSYNC |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

### 7.5.2.4 CHANNEL_CFG2 Register (Address = 0xF) [Reset = 0x00]

CHANNEL_CFG2 is shown in Table 7-112.

Return to the Summary Table.

**Table 7-112. CHANNEL_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | DAC_FORCE_DYN_MODE_CUST_MAX_CH | R/W | 0b | DAC Force dynamic mode custom max channel<br>0d = In Dynamic, Max channel is based on DAC_DYN_MAXCH_SEL<br>1d = In Dynamic mode, max channel is custom as per DAC_DYN_MODE_CUST_MAX_CH |
| 6-3 | DAC_DYN_MODE_CUST_MAX_CH[3:0] | R/W | 0000b | DAC Dynamic mode custom max channel configuration ([3]->CH4_EN, [2]->CH3_EN, [1]->CH2_EN, [0]->CH1_EN)<br>[3]->CH4_EN<br>[2]->CH3_EN<br>[1]->CH2_EN<br>[0]->CH1_EN |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset values |

### 7.5.2.5 SRC_CFG0 Register (Address = 0x17) [Reset = 0x00]

SRC_CFG0 is shown in Table 7-113.

Return to the Summary Table.

This register is configuration register 1 for SRC.

**Table 7-113. SRC_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SRC_EN | R/W | 0b | SRC enable config<br>0b = SRC disable<br>1b = SRC enable |

**ADVANCE INFORMATION**

**Table 7-113. SRC_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 6 | DIS_AUTO_SRC_DET | R/W | 0b | SRC auto detect config<br>0b = SRC auto detect enabled<br>1b = SRC auto detect disabled |
| 5-0 | RESERVED | R | 000000b | Reserved bits; Write only reset value |

### 7.5.2.6 SRC_CFG1 Register (Address = 0x18) [Reset = 0x00]

SRC_CFG1 is shown in Table 7-114.

Return to the Summary Table.

This register is configuration register 2 for SRC.

**Table 7-114. SRC_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | MAIN_FS_CUSTOM_CFG | R/W | 0b | Main Fs custom config<br>0b = Main Fs is auto inferred<br>1b = Main Fs need to be selected from MAIN_FS_SELECT_CFG |
| 6 | MAIN_FS_SELECT_CFG | R/W | 0b | Main Fs select config<br>0b = PASI Fs shall be used as Main Fs<br>1b = SASI Fs shall be used as Main Fs |
| 5-3 | MAIN_AUX_RATIO_M_CUSTOM_CFG[2:0] | R/W | 000b | Main and Aux Fs Ratio m:n config<br>0d = m is auto inferred<br>1d = 1<br>2d = 2<br>3d = 3<br>4d = 4<br>5d = Reserved<br>6d = 6<br>7d = Reserved |
| 2-0 | MAIN_AUX_RATIO_N_CUSTOM_CFG[2:0] | R/W | 000b | Main and Aux Fs Ratio m:n config<br>0d = n is auto inferred<br>1d = 1<br>2d = 2<br>3d = 3<br>4d = 4<br>5d = Reserved<br>6d = 6<br>7d = Reserved |

### 7.5.2.7 JACK_DET_CFG0 Register (Address = 0x19) [Reset = 0x00]

JACK_DET_CFG0 is shown in Table 7-115.

Return to the Summary Table.

This register is the JACK DET configuration register 0.

**Table 7-115. JACK_DET_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | JACK_DET_MONITOR_FREQ[1:0] | R/W | 00b | Headset Detection Pulse Frequency<br>0d = 0.5 Hz<br>1d = 1 Hz<br>2d = 7.5 Hz<br>3d = 15 Hz |
| 5 | JACK_DET_PULSE_WIDTH | R/W | 0b | Detector Pulse High Width<br>0d = 4ms (MICBIAS PIN Cap = 1 uF)<br>1d = 32ms (MICBIAS PIN Cap = 10 uF) |

Product Folder Links: *TAD5212*

**ADVANCE INFORMATION**

**Table 7-115. JACK_DET_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2-1 | HPDET_CLOCK_SEL[1:0] | R/W | 00b | Headphone Detection Clock Timeperiod Select<br>0d = 1ms<br>1d = 2ms<br>2d = 4ms<br>3d = Reserved |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

### 7.5.2.8 JACK_DET_CFG1 Register (Address = 0x1A) [Reset = 0x00]

JACK_DET_CFG1 is shown in .

Return to the .

This register is the JACK DET configuration register 1.

**Table 7-116. JACK_DET_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | JACK_DET_COMP_CTRL 2 | R/W | 0b | Hook Press Threshold Control in Fixed External Resistance case, controls the choice of Lowest Microphone impedance to be supported or Highest Hook button Impedance to be supported<br>0d = Minimum Microphone resistance supported, R_Mic = 800 Ωs and Max Hook button impedance supported, R_Hook = 320 Ωs for AC coupled Headphones R26<3> = 0 (else, when R26<3> = 1, R_hook = 150 Ωs)<br>1d = Max Hook button impedance supported, R_hook = 680 Ωs and Minimum Microphone resistance supported, R_Mic = 1350 Ωs for AC coupled Headphones R26<3> = 0 (else, when R26<3> = 1, R_Mic = 1750 Ωs) |
| 5-4 | JACK_DET_COMP_CTRL 3[1:0] | R/W | 00b | Hook Pressed Jack Insertion support, valid only for External Resistor Type P0_R25_D4 = 0 else Don't care.<br>0d = supports minimum Hook button impedance of 150 Ωs for Hook Pressed Jack Insertion detection<br>1d = supports minimum Hook button impedance of 100 Ωs for Hook Pressed Jack Insertion detection<br>2d = supports minimum Hook button impedance of 50 Ωs for Hook Pressed Jack Insertion detection<br>3d = Reserved |
| 3 | HPDET_COUPLING | R/W | 0b | Headphone detect coupling<br>0d = AC coupled<br>1d = DC coupled |
| 2 | HPDET_USE_2x_CURR | R/W | 0b | Headset detect current sel config<br>0d = 2x current for headphone detection disabled<br>1d = 2x current for headphone detection enabled |
| 1 | JACK_DET_EN | R/W | 0b | Headset Detection Enable<br>0d = Headset Detection Disabled<br>1d = Headset Detection Enabled |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.2.9 JACK_DET_CFG2 Register (Address = 0x1B) [Reset = 0x00]

JACK_DET_CFG2 is shown in .

Return to the .

**ADVANCE INFORMATION**

This register is the JACK DET configuration register 2.

**Table 7-117. JACK_DET_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | HPDET_DEB | R/W | 0b | Headphone Detection Debounce Programmability<br>0d = No Debounce<br>1d = Debounce of 3 detections |
| 5-3 | JACK_DET_DEB_INSERT[2:0] | R/W | 000b | Headset Insert Detection Debounce Programmability<br>0d = Debounce Time = 16ms<br>1d = Debounce Time = 32ms<br>2d = Debounce Time = 64ms<br>3d = Debounce Time = 128ms<br>4d = Debounce Time = 256ms<br>5d = Debounce Time = 512ms<br>6d = Reserved. Don not use<br>7d = No Debounce |
| 2 | JACK_DET_DEB_REMOVAL | R/W | 0b | Headset Removal Detection Debounce Programmability<br>0d = Debounce of 5 detections<br>1d = Debounce of 3 detections |
| 1-0 | JACK_DET_DEB_HOOK_PRESS[1:0] | R/W | 00b | Hook Press Debounce config<br>0d = No Debounce<br>1d = No Debounce<br>2d = Debounce of 2 detections<br>3d = Debounce of 3 detections |

### 7.5.2.10 JACK_DET_CFG3 Register (Address = 0x1C) [Reset = 0x00]

JACK_DET_CFG3 is shown in Table 7-118.

Return to the Summary Table.

This register is the JACK DET configuration register 3.

**Table 7-118. JACK_DET_CFG3 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | JACK_TYPE_FLAG[1:0] | R | 00b | Headset Jack type flag<br>0d = Jack is not inserted<br>1d = Jack is inserted without Microphone<br>2d = Reserved. Do not use<br>3d = Jack is inserted with Microphone |
| 5-4 | HEADSET_TYPE_DET[1:0] | R | 00b | Headset type<br>0d = Headset is not inserted<br>1d = Jack is inserted with mono-HS (RIGHT)<br>2d = Jack is inserted with mono-HS (LEFT)<br>3d = Jack is inserted with stereo-HS |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

### 7.5.2.11 LPSG_CFG1 Register (Address = 0x1F) [Reset = 0x80]

LPSG_CFG1 is shown in Table 7-119.

Return to the Summary Table.

Low Power Signal Generation configuration register 1

**ADVANCE INFORMATION**

**Table 7-119. LPSG_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | LPSG_CH_SEL[1:0] | R/W | 10b | LPSG channel select.- UAG<br>0d = UAG activity is generated on channel 1<br>1d = UAG activity is generated on channel 2<br>2d = UAG activity is generated on channel 3<br>3d = UAG activity is generated on channel 4 |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4-0 | RESERVED | R | 00000b | Reserved bits; Write only reset values |

### 7.5.2.12 LIMITER_CFG Register (Address = 0x23) [Reset = 0x00]

LIMITER_CFG is shown in Table 7-120.

Return to the Summary Table.

This register is configuration register 2 for Limiter.

**Table 7-120. LIMITER_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | LIMITER_INP_SEL[1:0] | R/W | 00b | Limiter input select config<br>0d = max(dacin_ch0, dacin_ch1)<br>1d = dacin_ch1<br>2d = dacin_ch0<br>3d = avg(dacin_ch0, dacin_ch1) |
| 5-4 | LIMITER_OUT_SEL[1:0] | R/W | 00b | Limiter output select config<br>0d = applied on both<br>1d = dacin_ch1<br>2d = dacin_ch0<br>3d = applied none |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset values |

### 7.5.2.13 PLIM_CFG0 Register (Address = 0x2B) [Reset = 0x00]

PLIM_CFG0 is shown in Table 7-121.

Return to the Summary Table.

This register is configuration register 0 for PLIM.

**Table 7-121. PLIM_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | EN_PLIM | R/W | 0b | Enable PLIM<br>0d = Disable<br>1d = Enable |
| 6-4 | PLIM_ATTN_VAL[2:0] | R/W | 000b | PLIM attenuation factor<br>0d = 0dB<br>1d = -6dB<br>2d = -12dB<br>3d = -18dB<br>4d = -24dB<br>5d = -30dB<br>6d = -36dB<br>7d = -42dB |
| 3 | PLIM_BY_SAR_GPA | R/W | 0b | PLIM attenuation value source<br>0d = Plimit attentation based on GPIO and reg_plimi_attn_val<br>1d = Plimit attenuation based on GPA Analog voltage. LUT will map SAR ADC data to Attenuation factor |

ADVANCE INFORMATION

**ADVANCE INFORMATION**

**Table 7-121. PLIM_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 2 | PLIM_RECOVERY | R/W | 0b | PLIM attenuation recovery<br>0d = Plimit func doesn't recover. It stays at same attenuation level or can apply more attenuation if required<br>1d = Plimit func recovers (reduces the attenuation) if "gpio_val=0" or "sar_adc_gpa" data suggest that Battery Voltage has recovered then we can reduce the attenuation being applied |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

### 7.5.2.14 MIXER_CFG0 Register (Address = 0x2C) [Reset = 0x00]

MIXER_CFG0 is shown in Table 7-122.

Return to the Summary Table.

This register is the MISC configuration register 0.

**Table 7-122. MIXER_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | EN_DAC_ASI_MIXER | R/W | 0b | Enable DAC ASI Mixer<br>0b = Disabled<br>1b = Enabled |
| 6 | EN_SIDE_CHAIN_MIXER | R/W | 0b | Enable Side Chain Mixer<br>0b = Disabled<br>1b = Enabled |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | EN_LOOPBACK_MIXER | R/W | 0b | Enable Loopback Mixer<br>0b = Disabled<br>1b = Enabled |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

### 7.5.2.15 MISC_CFG0 Register (Address = 0x2D) [Reset = 0x00]

MISC_CFG0 is shown in Table 7-123.

Return to the Summary Table.

This register is the MISC configuration register 0.

**Table 7-123. MISC_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | EN_DISTORTION | R/W | 0b | Distortion Limiter enable config<br>0b = Distortion Limiter disable<br>1b = Distortion Limiter enable |
| 6 | EN_BOP | R/W | 0b | BOP enable config<br>0b = BOP disable<br>1b = BOP enable |
| 5 | EN_THERMAL_FOLDBACK | R/W | 0b | Thermal Foldback enable config<br>0b = Thermal Foldback disable<br>1b = Thermal Foldback enable |
| 4 | EN_DRC | R/W | 0b | DRC enable config<br>0b = DRC disable<br>1b = DRC enable |
| 3 | DAC_SIGNAL_GENERATOR_1_ENABLE | R/W | 0b | DAC signal generator 1 enable config<br>0b = Signal generator disabled<br>1b = Signal generator enabled |

**Table 7-123. MISC_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 2 | DAC_SIGNAL_GENERATOR_2_ENABLE | R/W | 0b | DAC signal generator 2 enable config<br>0b = Signal generator disabled<br>1b = Signal generator enabled |
| 1 | DSP_VBAT_AVDD_SEL | R/W | 0b | SAR data source select for DSP Limiter, BOP, DRC<br>0b = SAR VBAT data to DSP<br>1b = SAR AVDD data to DSP |
| 0 | BRWNOUT_EN | R/W | 0b | Brownout enable config<br>0b = Brownout disable<br>1b = Brownout enable |

### 7.5.2.16 BRWNOUT Register (Address = 0x2E) [Reset = 0xBF]

BRWNOUT is shown in Table 7-124.

Return to the Summary Table.

**Table 7-124. BRWNOUT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | BRWNOUT_THRS[7:0] | R/W | 10111111b | Threshold for brownout shutdown (IF P1_R45_D1->DSP_VBAT_AVDD_SEL=1)<br>Default = 7.8V (~2.7V)<br>Nd = $((0.9 \times (N \times 16)/4095) - 0.211764) \times 17)$ (V) $(((0.9 \times (N \times 16)/4095) - 0.225) \times 6$ (V)) |

### 7.5.2.17 INT_MASK0 Register (Address = 0x2F) [Reset = 0xFF]

INT_MASK0 is shown in Table 7-125.

Return to the Summary Table.

Interrupt masks.

**Table 7-125. INT_MASK0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | INT_MASK0 | R/W | 1b | Clock error interrupt mask.<br>0b = Don't Mask<br>1b = Mask |
| 6 | INT_MASK0 | R/W | 1b | PLL Lock interrupt mask.<br>0b = Don't Mask<br>1b = Mask |
| 5 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 4 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 1 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 0 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |

### 7.5.2.18 INT_MASK4 Register (Address = 0x32) [Reset = 0x00]

INT_MASK4 is shown in Table 7-126.

Return to the Summary Table.

Interrupt masks.

**ADVANCE INFORMATION**

**Table 7-126. INT_MASK4 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | INT_MASK4 | R/W | 0b | OUT Short Circuit Fault Interrupt Mask.<br>0b = Don't Mask<br>1b = Mask |
| 4 | INT_MASK4 | R/W | 0b | DRVR Virtual Ground Fault Interrupt Mask.<br>0b = Don't Mask<br>1b = Mask |
| 3 | INT_MASK4 | R/W | 0b | Headset insert detection interrupt mask.<br>0b = Don't Mask<br>1b = Mask |
| 2 | INT_MASK4 | R/W | 0b | Headset remove detection interrupt mask.<br>0b = Don't Mask<br>1b = Mask |
| 1 | INT_MASK4 | R/W | 0b | Headset detection hook(button) interrupt mask.<br>0b = Don't Mask<br>1b = Mask |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

### 7.5.2.19 INT_MASK5 Register (Address = 0x33) [Reset = 0x30]

INT_MASK5 is shown in Table 7-127.

Return to the Summary Table.

Interrupt masks.

**Table 7-127. INT_MASK5 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | INT_MASK5 | R/W | 0b | GPA up threshold fault mask.<br>0b = Don't Mask<br>1b = Mask |
| 6 | INT_MASK5 | R/W | 0b | GPA low threshold fault mask.<br>0b = Don't Mask<br>1b = Mask |
| 5 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 4 | RESERVED | R/W | 1b | Reserved bit; Write only reset value |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

### 7.5.2.20 INT_LTCH0 Register (Address = 0x34) [Reset = 0x00]

INT_LTCH0 is shown in Table 7-128.

Return to the Summary Table.

Latched interrupt readback.

**Table 7-128. INT_LTCH0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | INT_LTCH0 | R | 0b | Interrupt due to clock error (self clearing bit).<br>0b = No interrupt<br>1b = Interrupt |

**Table 7-128. INT_LTCH0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 6 | INT_LTCH0 | R | 0b | Interrupt due to PLL Lock (self clearing bit)<br>0b = No interrupt<br>1b = Interrupt |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.2.21 CHx_LTCH Register (Address = 0x35) [Reset = 0x00]

CHx_LTCH is shown in Table 7-129.

Return to the Summary Table.

Channel level Diagnostics Latched Status

**Table 7-129. CHx_LTCH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | STS_CHx_LTCH | R | 0b | Status of Output CH1_LTCH.<br>0b = No faults occurred in output channel 1<br>1b = Fault or Faults have occurred in output channel 1 |
| 4 | STS_CHx_LTCH | R | 0b | Status of Output CH2_LTCH.<br>0b = No faults occurred in output channel 2<br>1b = Fault or Faults have occurred in output channel 2 |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.2.22 OUT_CH1_LTCH Register (Address = 0x38) [Reset = 0x00]

OUT_CH1_LTCH is shown in Table 7-130.

Return to the Summary Table.

**Table 7-130. OUT_CH1_LTCH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | OUT_CH1_LTCH | R | 0b | OUT1P Short Circuit Fault (self clearing bit).<br>0b = No short ciruit fault<br>1b = Short circuit fault |
| 6 | OUT_CH1_LTCH | R | 0b | OUT1M Short Circuit Fault (self clearing bit).<br>0b = No short ciruit fault<br>1b = Short circuit fault |
| 5 | OUT_CH1_LTCH | R | 0b | Channel 1 DRVRP Virtual Ground Fault (self clearing bit).<br>0b = No virtual ground fault<br>1b = Virtual ground fault |
| 4 | OUT_CH1_LTCH | R | 0b | Channel 1 DRVRM Virtual Ground Fault (self clearing bit).<br>0b = No virtual ground fault<br>1b = Virtual ground fault |

**ADVANCE INFORMATION**

Product Folder Links: TAD5212

**Table 7-130. OUT_CH1_LTCH Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1-0 | RESERVED | R | 00b | Reserved bits; Write only reset value |

### 7.5.2.23 OUT_CH2_LTCH Register (Address = 0x39) [Reset = 0x00]

OUT_CH2_LTCH is shown in Table 7-131.

Return to the Summary Table.

**Table 7-131. OUT_CH2_LTCH Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | OUT_CH2_LTCH | R | 0b | OUT2P Short Circuit Fault (self clearing bit).<br>0b = No short ciruit fault<br>1b = Short circuit fault |
| 6 | OUT_CH2_LTCH | R | 0b | OUT2M Short Circuit Fault (self clearing bit).<br>0b = No short ciruit fault<br>1b = Short circuit fault |
| 5 | OUT_CH2_LTCH | R | 0b | Channel 2 DRVRP Virtual Ground Fault (self clearing bit).<br>0b = No virtual ground fault<br>1b = Virtual ground fault |
| 4 | OUT_CH2_LTCH | R | 0b | Channel 2 DRVRM Virtual Ground Fault (self clearing bit).<br>0b = No virtual ground fault<br>1b = Virtual ground fault |
| 3-2 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 1 | MASK_AREG_SC_FLAG | R/W | 0b | AREG SC fault mask.<br>0b = Don't Mask<br>1b = Mask |
| 0 | AREG_SC_FLAG_LTCH | R | 0b | AREG SC fault (self clearing bit).<br>0b = No AREG short circuit fault<br>1b = AREG short ciruit fault |

### 7.5.2.24 INT_LTCH1 Register (Address = 0x3A) [Reset = 0x00]

INT_LTCH1 is shown in Table 7-132.

Return to the Summary Table.

Latched interrupt readback.

**Table 7-132. INT_LTCH1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | INT_LTCH1 | R | 0b | Interrupt due to Headset Insert Detection (self clearing bit).<br>0b = No interrupt<br>1b = Interrupt |
| 2 | INT_LTCH1 | R | 0b | Interrupt due to Headset Remove Detection (self clearing bit).<br>0b = No interrupt<br>1b = Interrupt |
| 1 | INT_LTCH1 | R | 0b | Interrupt due to Headset hook(button) (self clearing bit).<br>0b = No interrupt<br>1b = Interrupt |

Product Folder Links: *TAD5212*

**Table 7-132. INT_LTCH1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.2.25 INT_LTCH2 Register (Address = 0x3B) [Reset = 0x00]

INT_LTCH2 is shown in Table 7-133.

Return to the Summary Table.

Latched interrupt readback.

**Table 7-133. INT_LTCH2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | INT_LTCH2 | R | 0b | Interrupt due to GPA up threshold fault (self clearing bit).<br>0b = No interrupt<br>1b = Interrupt |
| 6 | INT_LTCH2 | R | 0b | Interrupt due to GPA low threshold fault (self clearing bit)<br>0b = No interrupt<br>1b = Interrupt |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.2.26 INT_LIVE0 Register (Address = 0x3C) [Reset = 0x00]

INT_LIVE0 is shown in Table 7-134.

Return to the Summary Table.

Latched interrupt readback.

**Table 7-134. INT_LIVE0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | INT_LIVE0 | R | 0b | Interrupt due to clock error .<br>0b = No interrupt<br>1b = Interrupt |
| 6 | INT_LIVE0 | R | 0b | Interrupt due to PLL Lock<br>0b = No interrupt<br>1b = Interrupt |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.2.27 CHx_LIVE Register (Address = 0x3D) [Reset = 0x00]

CHx_LIVE is shown in Table 7-135.

Return to the Summary Table.

ADVANCE INFORMATION

Channel level Diagnostics Live Status

**Table 7-135. CHx_LIVE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | STS_CHx_LIVE | R | 0b | Status of Output CH1_LIVE.<br>0b = No faults occurred in output channel 1<br>1b = Fault or Faults have occurred in output channel 1 |
| 4 | STS_CHx_LIVE | R | 0b | Status of Output CH2_LIVE.<br>0b = No faults occurred in output channel 2<br>1b = Fault or Faults have occurred in output channel 2 |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.2.28 OUT_CH1_LIVE Register (Address = 0x40) [Reset = 0x00]

OUT_CH1_LIVE is shown in Table 7-136.

Return to the Summary Table.

**Table 7-136. OUT_CH1_LIVE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | OUT_CH1_LIVE | R | 0b | OUT1P Short Circuit Fault .<br>0b = No short ciruit fault<br>1b = Short circuit fault |
| 6 | OUT_CH1_LIVE | R | 0b | OUT1M Short Circuit Fault .<br>0b = No short ciruit fault<br>1b = Short circuit fault |
| 5 | OUT_CH1_LIVE | R | 0b | Channel 1 DRVRP Virtual Ground Fault .<br>0b = No virtual ground fault<br>1b = Virtual ground fault |
| 4 | OUT_CH1_LIVE | R | 0b | Channel 1 DRVRM Virtual Ground Fault .<br>0b = No virtual ground fault<br>1b = Virtual ground fault |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

### 7.5.2.29 OUT_CH2_LIVE Register (Address = 0x41) [Reset = 0x00]

OUT_CH2_LIVE is shown in Table 7-137.

Return to the Summary Table.

**Table 7-137. OUT_CH2_LIVE Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | OUT_CH2_LIVE | R | 0b | OUT2P Short Circuit Fault .<br>0b = No short ciruit fault<br>1b = Short circuit fault |
| 6 | OUT_CH2_LIVE | R | 0b | OUT2M Short Circuit Fault .<br>0b = No short ciruit fault<br>1b = Short circuit fault |
| 5 | OUT_CH2_LIVE | R | 0b | Channel 2 DRVRP Virtual Ground Fault .<br>0b = No virtual ground fault<br>1b = Virtual ground fault |

Product Folder Links: *TAD5212*

**Table 7-137. OUT_CH2_LIVE Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 4 | OUT_CH2_LIVE | R | 0b | Channel 2 DRVRM Virtual Ground Fault .<br>0b = No virtual ground fault<br>1b = Virtual ground fault |
| 3-1 | RESERVED | R | 000b | Reserved bits; Write only reset value |
| 0 | AREG_SC_FLAG_LIVE | R | 0b | AREG SC fault .<br>0b = No AREG short circuit fault<br>1b = AREG short ciruit fault |

### 7.5.2.30 INT_LIVE1 Register (Address = 0x42) [Reset = 0x00]

INT_LIVE1 is shown in Table 7-138.

Return to the Summary Table.

Live interrupt readback.

**Table 7-138. INT_LIVE1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | INT_LIVE1 | R | 0b | Interrupt due to Headset Insert Detection .<br>0b = No interrupt<br>1b = Interrupt |
| 2 | INT_LIVE1 | R | 0b | Interrupt due to Headset Remove Detection .<br>0b = No interrupt<br>1b = Interrupt |
| 2 | INT_LIVE1 | R | 0b | Interrupt due to Headset hook(button) .<br>0b = No interrupt<br>1b = Interrupt |
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | |

### 7.5.2.31 INT_LIVE2 Register (Address = 0x43) [Reset = 0x00]

INT_LIVE2 is shown in Table 7-139.

Return to the Summary Table.

Live interrupt readback.

**Table 7-139. INT_LIVE2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | INT_LIVE2 | R | 0b | Interrupt due to GPA up threshold fault .<br>0b = No interrupt<br>1b = Interrupt |
| 6 | INT_LIVE2 | R | 0b | Interrupt due to GPA low threshold fault<br>0b = No interrupt<br>1b = Interrupt |
| 5 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 4 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 3 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R | 0b | Reserved bit; Write only reset value |

ADVANCE INFORMATION

**Table 7-139. INT_LIVE2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 1 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.2.32 DIAG_CFG8 Register (Address = 0x4E) [Reset = 0xBA]

DIAG_CFG8 is shown in Table 7-140.

Return to the Summary Table.

**Table 7-140. DIAG_CFG8 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | GPA_UP_THRS_FLT_TH RES[7:0] | R/W | 10111010b | General Purpose Analog High Threshold<br>Default = ~ 2.6V<br>nd = ((0.9×(N*16)/4095)-0·225)x6 (V) |

### 7.5.2.33 DIAG_CFG9 Register (Address = 0x4F) [Reset = 0x4B]

DIAG_CFG9 is shown in Table 7-141.

Return to the Summary Table.

**Table 7-141. DIAG_CFG9 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | GPA_LOW_THRS_FLT_T HRES[7:0] | R/W | 01001011b | General Purpose Analog Low Threshold<br>Default = ~ 0.2V<br>nd = ((0.9×(N*16)/4095)-0·225)x6 (V) |

### 7.5.2.34 DIAG_CFG14 Register (Address = 0x54) [Reset = 0x48]

DIAG_CFG14 is shown in Table 7-142.

Return to the Summary Table.

**Table 7-142. DIAG_CFG14 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | AVDD_FILT_SEL[1:0] | R/W | 10b | AVDD filter select<br>0d = 3.5MHz<br>1d = 200kHz<br>2d = 100kHz<br>3d = No filter |
| 4 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 3-2 | VBAT_FILT_SEL[1:0] | R/W | 10b | VBAT filter select<br>0d = 3.5MHz<br>1d = 200kHz<br>2d = 100kHz<br>3d = No filter |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

### 7.5.2.35 DIAGDATA_CFG Register (Address = 0x55) [Reset = 0x00]

DIAGDATA_CFG is shown in Table 7-143.

Return to the Summary Table.

### Table 7-143. DIAGDATA_CFG Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | RESERVED | R/W | 0000b | Reserved bits; Write only reset values |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 1 | OVRD_VBAT_TEMP_DATA | R/W | 0b | Override VBAT and TEMP data<br>0b= Override Disabled<br>1b= Override Enabled |
| 0 | HOLD_SAR_DATA | R/W | 0b | Hold SAR data update during register readback<br>0b= Data update is not held, Data register is continuously updated<br>1b= Data update is held, Data register readback can be done |

### 7.5.2.36 DIAG_MON_MSB_OUT1P Register (Address = 0x62) [Reset = 0x00]

DIAG_MON_MSB_OUT1P is shown in Table 7-144.

Return to the Summary Table.

### Table 7-144. DIAG_MON_MSB_OUT1P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DIAG_MON_MSB_OUT_CH1P[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

### 7.5.2.37 DIAG_MON_LSB_OUT1P Register (Address = 0x63) [Reset = 0x06]

DIAG_MON_LSB_OUT1P is shown in Table 7-145.

Return to the Summary Table.

### Table 7-145. DIAG_MON_LSB_OUT1P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | DIAG_MON_LSB_OUT_CH1P[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 0110b | Channel ID |

### 7.5.2.38 DIAG_MON_MSB_OUT1M Register (Address = 0x64) [Reset = 0x00]

DIAG_MON_MSB_OUT1M is shown in Table 7-146.

Return to the Summary Table.

### Table 7-146. DIAG_MON_MSB_OUT1M Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DIAG_MON_MSB_OUT_CH1N[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

### 7.5.2.39 DIAG_MON_LSB_OUT1M Register (Address = 0x65) [Reset = 0x07]

DIAG_MON_LSB_OUT1M is shown in Table 7-147.

Return to the Summary Table.

### Table 7-147. DIAG_MON_LSB_OUT1M Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | DIAG_MON_LSB_OUT_CH1N[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 0111b | Channel ID |

#### 7.5.2.40 DIAG_MON_MSB_OUT2P Register (Address = 0x66) [Reset = 0x00]

DIAG_MON_MSB_OUT2P is shown in Table 7-148.

Return to the Summary Table.

### Table 7-148. DIAG_MON_MSB_OUT2P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DIAG_MON_MSB_OUT_CH2P[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

#### 7.5.2.41 DIAG_MON_LSB_OUT2P Register (Address = 0x67) [Reset = 0x08]

DIAG_MON_LSB_OUT2P is shown in Table 7-149.

Return to the Summary Table.

### Table 7-149. DIAG_MON_LSB_OUT2P Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | DIAG_MON_LSB_OUT_CH2P[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1000b | Channel ID |

#### 7.5.2.42 DIAG_MON_MSB_OUT2M Register (Address = 0x68) [Reset = 0x00]

DIAG_MON_MSB_OUT2M is shown in Table 7-150.

Return to the Summary Table.

### Table 7-150. DIAG_MON_MSB_OUT2M Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DIAG_MON_MSB_OUT_CH2N[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

#### 7.5.2.43 DIAG_MON_LSB_OUT2M Register (Address = 0x69) [Reset = 0x09]

DIAG_MON_LSB_OUT2M is shown in Table 7-151.

Return to the Summary Table.

### Table 7-151. DIAG_MON_LSB_OUT2M Register Field Descriptions

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | DIAG_MON_LSB_OUT_CH2N[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1001b | Channel ID |

#### 7.5.2.44 DIAG_MON_MSB_TEMP Register (Address = 0x6A) [Reset = 0x00]

DIAG_MON_MSB_TEMP is shown in Table 7-152.

Return to the Summary Table.

**Table 7-152. DIAG_MON_MSB_TEMP Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | DIAG_MON_MSB_TEMP[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

### 7.5.2.45 DIAG_MON_LSB_TEMP Register (Address = 0x6B) [Reset = 0x0A]

DIAG_MON_LSB_TEMP is shown in Table 7-153.

Return to the Summary Table.

**Table 7-153. DIAG_MON_LSB_TEMP Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | DIAG_MON_LSB_TEMP[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1010b | Channel ID |

### 7.5.2.46 DIAG_MON_MSB_AVDD Register (Address = 0x6E) [Reset = 0x00]

DIAG_MON_MSB_AVDD is shown in Table 7-154.

Return to the Summary Table.

**Table 7-154. DIAG_MON_MSB_AVDD Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | DIAG_MON_MSB_AVDD[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

### 7.5.2.47 DIAG_MON_LSB_AVDD Register (Address = 0x6F) [Reset = 0x0C]

DIAG_MON_LSB_AVDD is shown in Table 7-155.

Return to the Summary Table.

**Table 7-155. DIAG_MON_LSB_AVDD Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | DIAG_MON_LSB_AVDD[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1100b | Channel ID |

### 7.5.2.48 DIAG_MON_MSB_GPA Register (Address = 0x70) [Reset = 0x00]

DIAG_MON_MSB_GPA is shown in Table 7-156.

Return to the Summary Table.

**Table 7-156. DIAG_MON_MSB_GPA Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | DIAG_MON_MSB_GPA[7:0] | R | 00000000b | Diagnostic SAR Monitor Data MSB Byte |

**ADVANCE INFORMATION**

**7.5.2.49 DIAG_MON_LSB_GPA Register (Address = 0x71) [Reset = 0x0D]**

DIAG_MON_LSB_GPA is shown in Table 7-157.

Return to the Summary Table.

**Table 7-157. DIAG_MON_LSB_GPA Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | DIAG_MON_LSB_GPA[3:0] | R | 0000b | Diagnostic SAR Monitor Data LSB Nibble |
| 3-0 | Channel[3:0] | R | 1101b | Channel ID |

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

### 7.5.3 TAD5212_P3 Registers

Table 7-158 lists the memory-mapped registers for the TAD5212_P3 registers. All register offset addresses not listed in Table 7-158 should be considered as reserved locations and the register contents should not be modified.

**Table 7-158. TAD5212_P3 Registers**

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x0 | PAGE_CFG | Device page register | 0x00 | PAGE_CFG Register (Address = 0x0) [Reset = 0x00] |
| 0x1A | SASI_CFG0 | Secondary ASI configuration register 0 | 0x30 | SASI_CFG0 Register (Address = 0x1A) [Reset = 0x30] |
| 0x1B | SASI_TX_CFG0 | SASI TX configuration register 0 | 0x00 | SASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00] |
| 0x1C | SASI_TX_CFG1 | SASI TX configuration register 1 | 0x00 | SASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00] |
| 0x1D | SASI_TX_CFG2 | SASI TX configuration register 2 | 0x00 | SASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00] |
| 0x20 | SASI_TX_CH3_CFG | SASI TX Channel 3 configuration register | 0x02 | SASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02] |
| 0x21 | SASI_TX_CH4_CFG | SASI TX Channel 4 configuration register | 0x03 | SASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03] |
| 0x22 | SASI_TX_CH5_CFG | SASI TX Channel 5 configuration register | 0x04 | SASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04] |
| 0x23 | SASI_TX_CH6_CFG | SASI TX Channel 6 configuration register | 0x05 | SASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05] |
| 0x24 | SASI_TX_CH7_CFG | SASI TX Channel 7 configuration register | 0x06 | SASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06] |
| 0x25 | SASI_TX_CH8_CFG | SASI TX Channel 8 configuration register | 0x07 | SASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07] |
| 0x26 | SASI_RX_CFG0 | SASI RX configuration register 0 | 0x00 | SASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00] |
| 0x27 | SASI_RX_CFG1 | SASI RX configuration register 1 | 0x00 | SASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00] |
| 0x28 | SASI_RX_CH1_CFG | SASI RX Channel 1 configuration register | 0x00 | SASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x00] |

ADVANCE INFORMATION

**Table 7-158. TAD5212_P3 Registers (continued)**

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x29 | SASI_RX_CH2_CFG | SASI RX Channel 2 configuration register | 0x01 | SASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x01] |
| 0x2A | SASI_RX_CH3_CFG | SASI RX Channel 3 configuration register | 0x02 | SASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02] |
| 0x2B | SASI_RX_CH4_CFG | SASI RX Channel 4 configuration register | 0x03 | SASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03] |
| 0x2C | SASI_RX_CH5_CFG | SASI RX Channel 5 configuration register | 0x04 | SASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04] |
| 0x2D | SASI_RX_CH6_CFG | SASI RX Channel 6 configuration register | 0x05 | SASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05] |
| 0x2E | SASI_RX_CH7_CFG | SASI RX Channel 7 configuration register | 0x06 | SASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06] |
| 0x2F | SASI_RX_CH8_CFG | SASI RX Channel 8 configuration register | 0x07 | SASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07] |
| 0x32 | CLK_CFG12 | Clock configuration register 12 | 0x00 | CLK_CFG12 Register (Address = 0x32) [Reset = 0x00] |
| 0x33 | CLK_CFG13 | | 0x00 | CLK_CFG13 Register (Address = 0x33) [Reset = 0x00] |
| 0x34 | CLK_CFG14 | Clock configuration register 14 | 0x10 | CLK_CFG14 Register (Address = 0x34) [Reset = 0x10] |
| 0x35 | CLK_CFG15 | Clock configuration register 15 | 0x01 | CLK_CFG15 Register (Address = 0x35) [Reset = 0x01] |
| 0x36 | CLK_CFG16 | Clock configuration register 16 | 0x00 | CLK_CFG16 Register (Address = 0x36) [Reset = 0x00] |
| 0x37 | CLK_CFG17 | Clock configuration register 17 | 0x00 | CLK_CFG17 Register (Address = 0x37) [Reset = 0x00] |
| 0x38 | CLK_CFG18 | Clock configuration register 18 | 0x08 | CLK_CFG18 Register (Address = 0x38) [Reset = 0x08] |
| 0x39 | CLK_CFG19 | Clock configuration register 19 | 0x20 | CLK_CFG19 Register (Address = 0x39) [Reset = 0x20] |
| 0x3A | CLK_CFG20 | Clock configuration register 20 | 0x04 | CLK_CFG20 Register (Address = 0x3A) [Reset = 0x04] |

ADVANCE INFORMATION

**Table 7-158. TAD5212_P3 Registers (continued)**

| Address | Acronym | Register Name | Reset Value | Section |
|---------|---------|---------------|-------------|---------|
| 0x3B | CLK_CFG21 | Clock configuration register 21 | 0x00 | CLK_CFG21 Register (Address = 0x3B) [Reset = 0x00] |
| 0x3C | CLK_CFG22 | Clock configuration register 18 | 0x01 | CLK_CFG22 Register (Address = 0x3C) [Reset = 0x01] |
| 0x3D | CLK_CFG23 | Clock configuration register 18 | 0x01 | CLK_CFG23 Register (Address = 0x3D) [Reset = 0x01] |
| 0x3E | CLK_CFG24 | Clock configuration register 21 | 0x01 | CLK_CFG24 Register (Address = 0x3E) [Reset = 0x01] |
| 0x44 | CLK_CFG30 | | 0x00 | CLK_CFG30 Register (Address = 0x44) [Reset = 0x00] |
| 0x45 | CLK_CFG31 | | 0x00 | CLK_CFG31 Register (Address = 0x45) [Reset = 0x00] |
| 0x46 | CLKOUT_CFG1 | CLKOUT configuration register 1 | 0x00 | CLKOUT_CFG1 Register (Address = 0x46) [Reset = 0x00] |
| 0x47 | CLKOUT_CFG2 | CLKOUT configuration register 2 | 0x01 | CLKOUT_CFG2 Register (Address = 0x47) [Reset = 0x01] |
| 0x49 | SARCLK_CFG1 | SAR clock configuration register 1 | 0x00 | SARCLK_CFG1 Register (Address = 0x49) [Reset = 0x00] |

**ADVANCE INFORMATION**

### 7.5.3.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in Table 7-159.

Return to the Summary Table.

The device memory map is divided into pages. This register sets the page.

**Table 7-159. PAGE_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | PAGE[7:0] | R/W | 00000000b | These bits set the device page.<br>0d = Page 0<br>1d = Page 1<br>2d to 254d = Page 2 to page 254 respectively<br>255d = Page 255 |

### 7.5.3.2 SASI_CFG0 Register (Address = 0x1A) [Reset = 0x30]

SASI_CFG0 is shown in Table 7-160.

Return to the Summary Table.

This register is the ASI configuration register 0.

**Table 7-160. SASI_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | SASI_FORMAT[1:0] | R/W | 00b | Secondary ASI protocol format.<br>0d = TDM mode<br>1d = I²S mode<br>2d = LJ (left-justified) mode<br>3d = Reserved; Don't use |
| 5-4 | SASI_WLEN[1:0] | R/W | 11b | Secondary ASI word or slot length.<br>0d = 16 bits (Recommended this setting to be used with 10-kΩ input impedance configuration)<br>1d = 20 bits<br>2d = 24 bits<br>3d = 32 bits |
| 3 | SASI_FSYNC_POL | R/W | 0b | ASI FSYNC polarity (for SASI protocol only).<br>0d = Default polarity as per standard protocol<br>1d = Inverted polarity with respect to standard protocol |
| 2 | SASI_BCLK_POL | R/W | 0b | ASI BCLK polarity (for SASI protocol only).<br>0d = Default polarity as per standard protocol<br>1d = Inverted polarity with respect to standard protocol |
| 1 | SASI_BUS_ERR | R/W | 0b | ASI bus error detection.<br>0d = Enable bus error detection<br>1d = Disable bus error detection |
| 0 | SASI_BUS_ERR_RCOV | R/W | 0b | ASI bus error auto resume.<br>0d = Enable auto resume after bus error recovery<br>1d = Disable auto resume after bus error recovery and remain powered down until host configures the device |

### 7.5.3.3 SASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00]

SASI_TX_CFG0 is shown in Table 7-161.

Return to the Summary Table.

This register is the SASI TX configuration register 0.

**Table 7-161. SASI_TX_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | SASI_TX_EDGE | R/W | 0b | Secondary ASI data output (on the primary and secondary data pin) transmit edge.<br>0d = Default edge as per the protocol configuration setting in SASI_BCLK_POL<br>1d = Inverted following edge (half cycle delay) with respect to the default edge setting |
| 6 | SASI_TX_FILL | R/W | 0b | Secondary ASI data output (on the primary and secondary data pin) for any unused cycles<br>0d = Always transmit 0 for unused cycles<br>1d = Always use Hi-Z for unused cycles |
| 5 | SASI_TX_LSB | R/W | 0b | Secondary ASI data output (on the primary and secondary data pin) for LSB transmissions.<br>0d = Transmit the LSB for a full cycle<br>1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle |
| 4-3 | SASI_TX_KEEPER[1:0] | R/W | 00b | Secondary ASI data output (on the primary and secondary data pin) bus keeper.<br>0d = Bus keeper is always disabled<br>1d = Bus keeper is always enabled<br>2d = Bus keeper is enabled during LSB transmissions only for one cycle<br>3d = Bus keeper is enabled during LSB transmissions only for one and half cycles |

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

**Table 7-161. SASI_TX_CFG0 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 2 | SASI_TX_USE_INT_FSYNC | R/W | 0b | Secondary ASI uses internal FSYNC for output data generation in controller mode configuration as applicable.<br>0d = Use external FSYNC for ASI protocol data generation<br>1d = Use internal FSYNC for ASI protocol data generation |
| 1 | SASI_TX_USE_INT_BCLK | R/W | 0b | Secondary ASI uses internal BCLK for output data generation in controller mode configuration.<br>0d = Use external BCLK for ASI protocol data generation<br>1d = Use internal BCLK for ASI protocol data generation |
| 0 | SASI_TDM_PULSE_WIDTH | R/W | 0b | Secondary ASI fsync pulse width in TDM format.<br>0d = Fsync pulse is 1 bclk period wide<br>1d = Fsync pulse is 2 bclk period wide |

### 7.5.3.4 SASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00]

SASI_TX_CFG1 is shown in Table 7-162.

Return to the Summary Table.

This register is the SASI TX configuration register 1.

**Table 7-162. SASI_TX_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-5 | RESERVED | R | 000b | Reserved bits; Write only reset value |
| 4-0 | SASI_TX_OFFSET[4:0] | R/W | 00000b | Secondary ASI output data MSB slot 0 offset (on the primary and secondary data pin).<br>0d = ASI data MSB location has no offset and is as per standard protocol<br>1d = ASI data MSB location (TDM mode is slot 0 or $I^2S$, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol<br>2d = ASI data MSB location (TDM mode is slot 0 or $I^2S$, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol<br>3d to 30d = ASI data MSB location (TDM mode is slot 0 or $I^2S$, LJ mode is the left and right slot 0) offset assigned as per configuration<br>31d = ASI data MSB location (TDM mode is slot 0 or $I^2S$, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

### 7.5.3.5 SASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00]

SASI_TX_CFG2 is shown in Table 7-163.

Return to the Summary Table.

This register is the SASI TX configuration register 2.

**Table 7-163. SASI_TX_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | SASI_TX_CH8_SEL | R/W | 0b | Secondary ASI output channel 8 select.<br>0d = Secondary ASI channel 8 output is on DOUT<br>1d = Secondary ASI channel 8 output is on DOUT2 |
| 6 | SASI_TX_CH7_SEL | R/W | 0b | Secondary ASI output channel 7 select.<br>0d = Secondary ASI channel 7 output is on DOUT<br>1d = Secondary ASI channel 7 output is on DOUT2 |
| 5 | SASI_TX_CH6_SEL | R/W | 0b | Secondary ASI output channel 6 select.<br>0d = Secondary ASI channel 6 output is on DOUT<br>1d = Secondary ASI channel 6 output is on DOUT2 |

**Table 7-163. SASI_TX_CFG2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 4 | SASI_TX_CH5_SEL | R/W | 0b | Secondary ASI output channel 5 select.<br>0d = Secondary ASI channel 5 output is on DOUT<br>1d = Secondary ASI channel 5 output is on DOUT2 |
| 3 | SASI_TX_CH4_SEL | R/W | 0b | Secondary ASI output channel 4 select.<br>0d = Secondary ASI channel 4 output is on DOUT<br>1d = Secondary ASI channel 4 output is on DOUT2 |
| 2 | SASI_TX_CH3_SEL | R/W | 0b | Secondary ASI output channel 3 select.<br>0d = Secondary ASI channel 3 output is on DOUT<br>1d = Secondary ASI channel 3 output is on DOUT2 |
| 1 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 0 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |

### 7.5.3.6 SASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02]

SASI_TX_CH3_CFG is shown in Table 7-164.

Return to the Summary Table.

This register is the SASI TX Channel 3 configuration register.

**Table 7-164. SASI_TX_CH3_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH3_CFG[1:0] | R/W | 00b | Secondary ASI output channel 3 configuration.<br>0d = Secondary ASI channel 3 output is in a tri-state condition<br>Dont use<br>2d = Secondary ASI channel 3 output corresponds to VBAT data<br>3d = Reserved |
| 4-0 | SASI_TX_CH3_SLOT_NUM[4:0] | R/W | 00010b | Secondary ASI output channel 3 slot assignment.<br>0d = TDM is slot 0 or $I^2S$, LJ is left slot 0<br>1d = TDM is slot 1 or $I^2S$, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or $I^2S$, LJ is left slot 15<br>16d = TDM is slot 16 or $I^2S$, LJ is right slot 0<br>17d = TDM is slot 17 or $I^2S$, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or $I^2S$, LJ is right slot 15 |

### 7.5.3.7 SASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03]

SASI_TX_CH4_CFG is shown in Table 7-165.

Return to the Summary Table.

This register is the SASI TX Channel 4 configuration register.

**Table 7-165. SASI_TX_CH4_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH4_CFG[1:0] | R/W | 00b | Secondary ASI output channel 4 configuration.<br>0d = Secondary ASI channel 4 output is in a tri-state condition<br>Dont use<br>2d = Secondary ASI channel 4 output corresponds to TEMP data<br>3d = Reserved |

Product Folder Links: TAD5212

**Table 7-165. SASI_TX_CH4_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4-0 | SASI_TX_CH4_SLOT_NUM[4:0] | R/W | 00011b | Secondary ASI output channel 4 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.3.8 SASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04]

SASI_TX_CH5_CFG is shown in Table 7-166.

Return to the Summary Table.

This register is the SASI TX Channel 5 configuration register.

**Table 7-166. SASI_TX_CH5_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH5_CFG[1:0] | R/W | 00b | Secondary ASI output channel 5 configuration.<br>0d = Secondary ASI channel 5 output is in a tri-state condition<br>1d = Secondary ASI channel 5 output corresponds to ASI Input Channel 1 loopback data<br>2d = Secondary ASI channel 5 output corresponds to echo reference channel 1 data<br>3d = Reserved |
| 4-0 | SASI_TX_CH5_SLOT_NUM[4:0] | R/W | 00100b | Secondary ASI output channel 5 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.3.9 SASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05]

SASI_TX_CH6_CFG is shown in Table 7-167.

Return to the Summary Table.

This register is the SASI TX Channel 6 configuration register.

**Table 7-167. SASI_TX_CH6_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH6_CFG[1:0] | R/W | 00b | Secondary ASI output channel 6 configuration.<br>0d = Secondary ASI channel 6 output is in a tri-state condition<br>1d = Secondary ASI channel 6 output corresponds to ASI Input Channel 2 loopback data<br>2d = Secondary ASI channel 6 output corresponds to echo reference channel 2 data<br>3d = Reserved |

ADVANCE INFORMATION

**Table 7-167. SASI_TX_CH6_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4-0 | SASI_TX_CH6_SLOT_NUM[4:0] | R/W | 00101b | Secondary ASI output channel 6 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.3.10 SASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06]

SASI_TX_CH7_CFG is shown in Table 7-168.

Return to the Summary Table.

This register is the SASI TX Channel 7 configuration register.

**Table 7-168. SASI_TX_CH7_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_TX_CH7_CFG[1:0] | R/W | 00b | Secondary ASI output channel 7 configuration.<br>0d = Secondary ASI channel 7 output is in a tri-state condition<br>1d = Secondary ASI channel 7 output corresponds to {VBAT_WLby2, TEMP_WLby2}<br>2d = Secondary ASI channel 7 output corresponds to {echo_ref_ch1_wlby2, echo_ref_ch2_wlby2}<br>3d = Reserved |
| 4-0 | SASI_TX_CH7_SLOT_NUM[4:0] | R/W | 00110b | Secondary ASI output channel 7 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.3.11 SASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07]

SASI_TX_CH8_CFG is shown in Table 7-169.

Return to the Summary Table.

This register is the SASI TX Channel 8 configuration register.

**Table 7-169. SASI_TX_CH8_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_TX_CH8_CFG | R/W | 0b | Secondary ASI output channel 8 configuration.<br>0d = Secondary ASI channel 8 output is in a tri-state condition<br>1d = Secondary ASI channel 8 output corresponds to ICLA data |

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

**Table 7-169. SASI_TX_CH8_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4-0 | SASI_TX_CH8_SLOT_NUM[4:0] | R/W | 00111b | Secondary ASI output channel 8 slot assignment.<br>0d = TDM is slot 0 or I²S, LJ is left slot 0<br>1d = TDM is slot 1 or I²S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I²S, LJ is left slot 15<br>16d = TDM is slot 16 or I²S, LJ is right slot 0<br>17d = TDM is slot 17 or I²S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I²S, LJ is right slot 15 |

### 7.5.3.12 SASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00]

SASI_RX_CFG0 is shown in Table 7-170.

Return to the Summary Table.

This register is the SASI RX configuration register 0.

**Table 7-170. SASI_RX_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SASI_RX_EDGE | R/W | 0b | Secondary ASI data input (on the primary and secondary data pin) receive edge.<br>0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL)<br>1d = Inverted following edge (half cycle delay) with respect to the default edge setting |
| 6 | SASI_RX_USE_INT_FSYNC | R/W | 0b | Secondary ASI uses internal FSYNC for input data latching in controller mode configuration as applicable.<br>0d = Use external FSYNC for ASI protocol data latching<br>1d = Use internal FSYNC for ASI protocol data latching |
| 5 | SASI_RX_USE_INT_BCLK | R/W | 0b | Secondary ASI uses internal BCLK for input data latching in controller mode configuration.<br>0d = Use external BCLK for ASI protocol data latching<br>1d = Use internal BCLK for ASI protocol data latching |
| 4-0 | SASI_RX_OFFSET[4:0] | R/W | 00000b | Secondary ASI data input MSB slot 0 offset (on the primary and secondary data pin).<br>0d = ASI data MSB location has no offset and is as per standard protocol<br>1d = ASI data MSB location (TDM mode is slot 0 or I²S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol<br>2d = ASI data MSB location (TDM mode is slot 0 or I²S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol<br>3d to 30d = ASI data MSB location (TDM mode is slot 0 or I²S, LJ mode is the left and right slot 0) offset assigned as per configuration<br>31d = ASI data MSB location (TDM mode is slot 0 or I²S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol |

### 7.5.3.13 SASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00]

SASI_RX_CFG1 is shown in Table 7-171.

Return to the Summary Table.

This register is the SASI RX configuration register 1.

Product Folder Links: TAD5212

ADVANCE INFORMATION

**ADVANCE INFORMATION**

**Table 7-171. SASI_RX_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SASI_RX_CH8_SEL | R/W | 0b | Secondary ASI input channel 8 select.<br>0d = Secondary ASI channel 8 input is on DIN<br>1d = Secondary ASI channel 8 input is on DIN2 |
| 6 | SASI_RX_CH7_SEL | R/W | 0b | Secondary ASI input channel 7 select.<br>0d = Secondary ASI channel 7 input is on DIN<br>1d = Secondary ASI channel 7 input is on DIN2 |
| 5 | SASI_RX_CH6_SEL | R/W | 0b | Secondary ASI input channel 6 select.<br>0d = Secondary ASI channel 6 input is on DIN<br>1d = Secondary ASI channel 6 input is on DIN2 |
| 4 | SASI_RX_CH5_SEL | R/W | 0b | Secondary ASI input channel 5 select.<br>0d = Secondary ASI channel 5 input is on DIN<br>1d = Secondary ASI channel 5 input is on DIN2 |
| 3 | SASI_RX_CH4_SEL | R/W | 0b | Secondary ASI input channel 4 select.<br>0d = Secondary ASI channel 4 input is on DIN<br>1d = Secondary ASI channel 4 input is on DIN2 |
| 2 | SASI_RX_CH3_SEL | R/W | 0b | Secondary ASI input channel 3 select.<br>0d = Secondary ASI channel 3 input is on DIN<br>1d = Secondary ASI channel 3 input is on DIN2 |
| 1 | SASI_RX_CH2_SEL | R/W | 0b | Secondary ASI input channel 2 select.<br>0d = Secondary ASI channel 2 input is on DIN<br>1d = Secondary ASI channel 2 input is on DIN2 |
| 0 | SASI_RX_CH1_SEL | R/W | 0b | Secondary ASI input channel 1 select.<br>0d = Secondary ASI channel 1 input is on DIN<br>1d = Secondary ASI channel 1 input is on DIN2 |

### 7.5.3.14 SASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x00]

SASI_RX_CH1_CFG is shown in Table 7-172.

Return to the Summary Table.

This register is the SASI RX Channel 1 configuration register.

**Table 7-172. SASI_RX_CH1_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_RX_CH1_CFG | R/W | 0b | Secondary ASI input channel 1 configuration.<br>0d = Secondary ASI channel 1 input is disabled<br>1d = Secondary ASI channel 1 input corresponds to DAC Channel 1 data |
| 4-0 | SASI_RX_CH1_SLOT_NUM[4:0] | R/W | 00000b | Secondary ASI input channel 1 slot assignment.<br>0d = TDM is slot 0 or $I^2S$, LJ is left slot 0<br>1d = TDM is slot 1 or $I^2S$, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or $I^2S$, LJ is left slot 15<br>16d = TDM is slot 16 or $I^2S$, LJ is right slot 0<br>17d = TDM is slot 17 or $I^2S$, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or $I^2S$, LJ is right slot 15 |

### 7.5.3.15 SASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x01]

SASI_RX_CH2_CFG is shown in Table 7-173.

Return to the Summary Table.

This register is the SASI RX Channel 2 configuration register.

Product Folder Links: *TAD5212*

**Table 7-173. SASI_RX_CH2_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_RX_CH2_CFG | R/W | 0b | Secondary ASI input channel 2 configuration.<br>0d = Secondary ASI channel 2 input is disabled<br>1d = Secondary ASI channel 2 input corresponds to DAC Channel 2 data |
| 4-0 | SASI_RX_CH2_SLOT_NUM[4:0] | R/W | 00001b | Secondary ASI input channel 2 slot assignment.<br>0d = TDM is slot 0 or $I^2S$, LJ is left slot 0<br>1d = TDM is slot 1 or $I^2S$, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or $I^2S$, LJ is left slot 15<br>16d = TDM is slot 16 or $I^2S$, LJ is right slot 0<br>17d = TDM is slot 17 or $I^2S$, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or $I^2S$, LJ is right slot 15 |

### 7.5.3.16 SASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02]

SASI_RX_CH3_CFG is shown in Table 7-174.

Return to the Summary Table.

This register is the SASI RX Channel 3 configuration register.

**Table 7-174. SASI_RX_CH3_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_RX_CH3_CFG | R/W | 0b | Secondary ASI input channel 3 configuration.<br>0d = Secondary ASI channel 3 input is disabled<br>1d = Secondary ASI channel 3 input corresponds to DAC Channel 3 data |
| 4-0 | SASI_RX_CH3_SLOT_NUM[4:0] | R/W | 00010b | Secondary ASI input channel 3 slot assignment.<br>0d = TDM is slot 0 or $I^2S$, LJ is left slot 0<br>1d = TDM is slot 1 or $I^2S$, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or $I^2S$, LJ is left slot 15<br>16d = TDM is slot 16 or $I^2S$, LJ is right slot 0<br>17d = TDM is slot 17 or $I^2S$, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or $I^2S$, LJ is right slot 15 |

### 7.5.3.17 SASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03]

SASI_RX_CH4_CFG is shown in Table 7-175.

Return to the Summary Table.

This register is the SASI RX Channel 4 configuration register.

**Table 7-175. SASI_RX_CH4_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5 | SASI_RX_CH4_CFG | R/W | 0b | Secondary ASI input channel 4 configuration.<br>0d = Secondary ASI channel 4 input is disabled<br>1d = Secondary ASI channel 4 input corresponds to DAC Channel 4 data |

ADVANCE INFORMATION

**Table 7-175. SASI_RX_CH4_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 4-0 | SASI_RX_CH4_SLOT_NUM[4:0] | R/W | 00011b | Secondary ASI input channel 4 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.3.18 SASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04]

SASI_RX_CH5_CFG is shown in Table 7-176.

Return to the Summary Table.

This register is the SASI RX Channel 5 configuration register.

**Table 7-176. SASI_RX_CH5_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_RX_CH5_CFG[1:0] | R/W | 00b | Secondary ASI input channel 5 configuration.<br>0d = Secondary ASI channel 5 input is disabled<br>1d = Secondary ASI channel 5 input corresponds to DAC Channel 5 data<br>2d = Secondary ASI channel 5 input corresponds to ADC Channel 1 output loopback<br>3d = Reserved |
| 4-0 | SASI_RX_CH5_SLOT_NUM[4:0] | R/W | 00100b | Secondary ASI input channel 5 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.3.19 SASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05]

SASI_RX_CH6_CFG is shown in Table 7-177.

Return to the Summary Table.

This register is the SASI RX Channel 6 configuration register.

**Table 7-177. SASI_RX_CH6_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_RX_CH6_CFG[1:0] | R/W | 00b | Secondary ASI input channel 6 configuration.<br>0d = Secondary ASI channel 6 input is disabled<br>1d = Secondary ASI channel 6 input corresponds to DAC Channel 6 data<br>2d = Secondary ASI channel 6 input corresponds to ADC Channel 2 output loopback<br>3d = Secondary ASI channel 6 input corresponds to ICLA device 1 data |

Product Folder Links: *TAD5212*

ADVANCE INFORMATION

**Table 7-177. SASI_RX_CH6_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4-0 | SASI_RX_CH6_SLOT_NUM[4:0] | R/W | 00101b | Secondary ASI input channel 6 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.3.20 SASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06]

SASI_RX_CH7_CFG is shown in Table 7-178.

Return to the Summary Table.

This register is the SASI RX Channel 7 configuration register.

**Table 7-178. SASI_RX_CH7_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_RX_CH7_CFG[1:0] | R/W | 00b | Secondary ASI input channel 7 configuration.<br>0d = Secondary ASI channel 7 input is disabled<br>1d = Secondary ASI channel 7 input corresponds to DAC Channel 7 data<br>2d = Secondary ASI channel 7 input corresponds to ADC Channel 3 output loopback<br>3d = Secondary ASI channel 7 input corresponds to ICLA device 2 data |
| 4-0 | SASI_RX_CH7_SLOT_NUM[4:0] | R/W | 00110b | Secondary ASI input channel 7 slot assignment.<br>0d = TDM is slot 0 or I$^2$S, LJ is left slot 0<br>1d = TDM is slot 1 or I$^2$S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I$^2$S, LJ is left slot 15<br>16d = TDM is slot 16 or I$^2$S, LJ is right slot 0<br>17d = TDM is slot 17 or I$^2$S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I$^2$S, LJ is right slot 15 |

### 7.5.3.21 SASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07]

SASI_RX_CH8_CFG is shown in Table 7-179.

Return to the Summary Table.

This register is the SASI RX Channel 8 configuration register.

**Table 7-179. SASI_RX_CH8_CFG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-5 | SASI_RX_CH8_CFG[1:0] | R/W | 00b | Secondary ASI input channel 8 configuration.<br>0d = Secondary ASI channel 8 input is disabled<br>1d = Secondary ASI channel 8 input corresponds to DAC Channel 8 data<br>2d = Secondary ASI channel 8 input corresponds to ADC Channel 4 output loopback<br>3d = Secondary ASI channel 8 input corresponds to ICLA device 3 data |

ADVANCE INFORMATION

**Table 7-179. SASI_RX_CH8_CFG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 4-0 | SASI_RX_CH8_SLOT_NUM[4:0] | R/W | 00111b | Secondary ASI input channel 8 slot assignment.<br>0d = TDM is slot 0 or I²S, LJ is left slot 0<br>1d = TDM is slot 1 or I²S, LJ is left slot 1<br>2d to 14d = Slot assigned as per configuration<br>15d = TDM is slot 15 or I²S, LJ is left slot 15<br>16d = TDM is slot 16 or I²S, LJ is right slot 0<br>17d = TDM is slot 17 or I²S, LJ is right slot 1<br>18d to 30d = Slot assigned as per configuration<br>31d = TDM is slot 31 or I²S, LJ is right slot 15 |

### 7.5.3.22 CLK_CFG12 Register (Address = 0x32) [Reset = 0x00]

CLK_CFG12 is shown in Table 7-180.

Return to the Summary Table.

This register is the clock configuration register 12.

**Table 7-180. CLK_CFG12 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | PDIV_CLKSRC_SEL[1:0] | R/W | 00b | Source clock selection for PLL PDIV Divider.<br>0d = PLL_PDIV_IN_CLK is Primary ASI BCLK<br>1d = PLL_PDIV_IN_CLK is Secondary ASI BCLK<br>2d = PLL_PDIV_IN_CLK is CCLK<br>3d = PLL_PDIV_IN_CLK is internal Oscillator Clock |
| 5-3 | PASI_BCLK_DIV_CLK_SEL[2:0] | R/W | 000b | Primary ASI BCLK divider clock source selection.<br>0d = Primary ASI BCLK divider clock source is PLL output<br>1d = Reserved<br>2d = Primary ASI BCLK divider clock source is secondary ASI BCLK<br>3d = Primary ASI BCLK divider clock source is CCLK<br>4d = Primary ASI BCLK divider clock source is internal oscillator clock<br>5d = Primary ASI BCLK divider clock source is DSP clock<br>6d to 7d = Reserved |
| 2-0 | RESERVED | R | 000b | Reserved bits; Write only reset value |

### 7.5.3.23 CLK_CFG13 Register (Address = 0x33) [Reset = 0x00]

CLK_CFG13 is shown in Table 7-181.

Return to the Summary Table.

**Table 7-181. CLK_CFG13 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R | 0b | Reserved bit; Write only reset value |
| 6-4 | SASI_BCLK_DIV_CLK_SEL[2:0] | R/W | 000b | Secondaary ASI BCLK divider clock source selection.<br>0d = Secondaary ASI BCLK divider clock source is PLL output<br>1d = Secondaary ASI BCLK divider clock source is primary ASI BCLK<br>2d = Reserved<br>3d = Secondaary ASI BCLK divider clock source is CCLK<br>4d = Secondaary ASI BCLK divider clock source is internal oscillator clock<br>5d = Secondaary ASI BCLK divider clock source is DSP clock<br>6d to 7d = Reserved |
| 3-0 | RESERVED | R | 0000b | Reserved bits; Write only reset value |

Product Folder Links: TAD5212

### 7.5.3.24 CLK_CFG14 Register (Address = 0x34) [Reset = 0x10]

CLK_CFG14 is shown in Table 7-182.

Return to the Summary Table.

This register is the clock configuration register 14.

**Table 7-182. CLK_CFG14 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | DIG_NM_DIV_CLK_SRC_SEL[1:0] | R/W | 00b | Source clock selection for DIG NMDIV CLK clock.<br>0d = DIG NM divider input clock is Primary ASI BCLK<br>1d = DIG NM divider input clock is Secondary ASI BCLK<br>2d = DIG NM divider input clock is CCLK<br>3d = DIG NM divider input clock is internal oscillator clock |
| 5-4 | ANA_NM_DIV_CLK_SRC_SEL[1:0] | R/W | 01b | Source clock selection for NMDIV CLK clock.<br>0d = NM divider input clock is PLL Output<br>1d = NM divider input clock is PLL Output<br>2d = NM divider input clock is DIG NM Divider Clock Source<br>3d = NM divider input clock is Primary ASI BCLK (Low Jitter Path) |
| 3-2 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 1-0 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |

### 7.5.3.25 CLK_CFG15 Register (Address = 0x35) [Reset = 0x01]

CLK_CFG15 is shown in Table 7-183.

Return to the Summary Table.

This register is the clock configuration register 15.

**Table 7-183. CLK_CFG15 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | PLL_PDIV[7:0] | R/W | 00000001b | PLL pre-scaler P-divider value (Don't care when auto detection is enabled)<br>0d = PLL PDIV value is 256<br>1d = PLL PDIV value is 1<br>2d = PLL PDIV value is 2<br>3d to 254d = PLL PDIV value is as per configuration<br>255d = PLL PDIV value is 255 |

### 7.5.3.26 CLK_CFG16 Register (Address = 0x36) [Reset = 0x00]

CLK_CFG16 is shown in Table 7-184.

Return to the Summary Table.

This register is the clock configuration register 16.

**Table 7-184. CLK_CFG16 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | PLL_JMUL_MSB | R/W | 0b | PLL integer portion J-multiplier value MSB bit. (Don't care when auto detection is enabled) |
| 6 | PLL_DIV_CLK_DIG_BY_2 | R/W | 0b | PLL DIV clock divide by 2 configuration<br>0d = No divide/2 inside PLL<br>1d = PLL does a divide/2 |
| 5-0 | PLL_DMUL_MSB[5:0] | R/W | 000000b | PLL fractional portion D-multiplier value MSB bits. (Don't care when auto detection is enabled) |

**ADVANCE INFORMATION**

Product Folder Links: TAD5212

**7.5.3.27 CLK_CFG17 Register (Address = 0x37) [Reset = 0x00]**

CLK_CFG17 is shown in Table 7-185.

Return to the Summary Table.

This register is the clock configuration register 17.

**Table 7-185. CLK_CFG17 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | PLL_DMUL_LSB[7:0] | R/W | 00000000b | PLL fractional portion D-multiplier value LSB byte. Above D-multiplier value MSB bits (PLL_DMUL_MSB) along with this LSB byte (PLL_DMUL_LSB) is concatenated to determine final D-multiplier value. (Don't care when auto detection is enabled)<br>0d = PLL DMUL value is 0<br>1d = PLL DMUL value is 1<br>2d = PLL DMUL value is 2<br>3d to 9998d = PLL JMUL value is as per configuration<br>9999d = PLL JMUL value is 9999<br>10000d to 16383d = Reserved; Don't use |

**7.5.3.28 CLK_CFG18 Register (Address = 0x38) [Reset = 0x08]**

CLK_CFG18 is shown in Table 7-186.

Return to the Summary Table.

This register is the clock configuration register 18.

**Table 7-186. CLK_CFG18 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | PLL_JMUL_LSB[7:0] | R/W | 00001000b | PLL integer portion J-multiplier value LSB byte. Above J-multiplier value MSB bit (PLL_JMUL_MSB) along with this LSB byte (PLL_JMUL_LSB) is concatenated to determine fianl J-multiplier value. (Don't care when auto detection is enabled)<br>0d = Reserved; Don't use<br>1d = PLL JMUL value is 1<br>2d = PLL JMUL value is 2<br>3d to 510d = PLL JMUL value is as per configuration<br>511d = PLL JMUL value is 511 |

**7.5.3.29 CLK_CFG19 Register (Address = 0x39) [Reset = 0x20]**

CLK_CFG19 is shown in Table 7-187.

Return to the Summary Table.

This register is the clock configuration register 19.

**Table 7-187. CLK_CFG19 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-5 | NDIV[2:0] | R/W | 001b | NDIV divider value. (Don't care when auto detection is enabled)<br>0d = NDIV value is 8<br>1d = NDIV value is 1<br>2d = NDIV value is 2<br>3d to 6d = NDIV value is as per configuration<br>7d = NDIV value is 7 |

Product Folder Links: *TAD5212*

**Table 7-187. CLK_CFG19 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 4-2 | PDM_DIV[2:0] | R/W | 000b | PDM divider value. (Don't care when auto detection is enabled)<br>0d = PDM_DIV value is 1<br>1d = PDM_DIV value is 2<br>2d = PDM_DIV value is 4<br>3d = PDM_DIV value is 8<br>4d = PDM_DIV value is 16<br>5d-7d Reserved |
| 1-0 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |

### 7.5.3.30 CLK_CFG20 Register (Address = 0x3A) [Reset = 0x04]

CLK_CFG20 is shown in Table 7-188.

Return to the Summary Table.

This register is the clock configuration register 20.

**Table 7-188. CLK_CFG20 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-2 | MDIV[5:0] | R/W | 000001b | MDIV divider value. (Don't care when auto detection is enabled)<br>0d = MDIV value is 64<br>1d = MDIV value is 1<br>2d = MDIV value is 2<br>3d to 62d = MDIV value is as per configuration<br>63d = MDIV value is 63 |
| 1-0 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |

### 7.5.3.31 CLK_CFG21 Register (Address = 0x3B) [Reset = 0x00]

CLK_CFG21 is shown in Table 7-189.

Return to the Summary Table.

This register is the clock configuration register 21.

**Table 7-189. CLK_CFG21 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | RESERVED | R/W | 00b | Reserved bits; Write only reset values |
| 5-4 | DIG_DAC_MODCLK_DIV[1:0] | R/W | 00b | DAC modulator clock divider value. (Don't care when auto detection is enabled)<br>0d = DIG_DAC_MODCLK_DIV value is 1<br>1d = DIG_DAC_MODCLK_DIV value is 2<br>2d = DIG_DAC_MODCLK_DIV value is 4<br>3d = Reserved |
| 3 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 2 | PASI_BDIV_MSB | R/W | 0b | Primary ASI BCLK divider value MSB bit. (Don't care when auto detection is enabled) |
| 1 | SASI_BDIV_MSB | R/W | 0b | Secondary ASI BCLK divider value MSB bit. (Don't care when auto detection is enabled) |
| 0 | RESERVED | R | 0b | Reserved bit; Write only reset value |

### 7.5.3.32 CLK_CFG22 Register (Address = 0x3C) [Reset = 0x01]

CLK_CFG22 is shown in Table 7-190.

Return to the Summary Table.

Product Folder Links: TAD5212

ADVANCE INFORMATION

This register is the clock configuration register 18.

**Table 7-190. CLK_CFG22 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PASI_BDIV_LSB[7:0] | R/W | 00000001b | Secondary ASI BCLK divider value. (Don't care when auto detection is enabled)<br>0d = SASI BCLK divider value is 512<br>1d = SASI BCLK divider value is 1<br>2d = SASI BCLK divider value is 2<br>3d to 62d = SASI BCLK divider value is as per configuration<br>63d = SASI BCLK divider value is 511 |

### 7.5.3.33 CLK_CFG23 Register (Address = 0x3D) [Reset = 0x01]

CLK_CFG23 is shown in Table 7-191.

Return to the Summary Table.

This register is the clock configuration register 18.

**Table 7-191. CLK_CFG23 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | SASI_BDIV_LSB[7:0] | R/W | 00000001b | Secondary ASI BCLK divider value. (Don't care when auto detection is enabled)<br>0d = SASI BCLK divider value is 512<br>1d = SASI BCLK divider value is 1<br>2d = SASI BCLK divider value is 2<br>3d to 62d = SASI BCLK divider value is as per configuration<br>63d = SASI BCLK divider value is 511 |

### 7.5.3.34 CLK_CFG24 Register (Address = 0x3E) [Reset = 0x01]

CLK_CFG24 is shown in Table 7-192.

Return to the Summary Table.

This register is the clock configuration register 21.

**Table 7-192. CLK_CFG24 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | RESERVED | R | 00b | Reserved bits; Write only reset value |
| 5-0 | ANA_NM_DIV[5:0] | R/W | 000001b | Analog N-M DIV divider value. (Don't care when auto detection is enabled)<br>0d = ANA_NM_DIV value is 64<br>1d = ANA_NM_DIV value is 1<br>2d = ANA_NM_DIV value is 2<br>3d to 62d = ANA_NM_DIV value is as per configuration<br>63d = NDIV value is 63 |

### 7.5.3.35 CLK_CFG30 Register (Address = 0x44) [Reset = 0x00]

CLK_CFG30 is shown in Table 7-193.

Return to the Summary Table.

**Table 7-193. CLK_CFG30 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | RESERVED | R | 00000b | Reserved bits; Write only reset value |

Product Folder Links: *TAD5212*

**Table 7-193. CLK_CFG30 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 2 | NDIV_EN | R/W | 0b | NDIV divider enable<br>0d = divider disabled<br>1d = divider enabled |
| 1 | MDIV_EN | R/W | 0b | MDIV divider enable<br>0d = divider disabled<br>1d = divider enabled |
| 0 | PDM_DIV_EN | R/W | 0b | PDM divider enable<br>0d = divider disabled<br>1d = divider enabled |

### 7.5.3.36 CLK_CFG31 Register (Address = 0x45) [Reset = 0x00]

CLK_CFG31 is shown in Table 7-194.

Return to the Summary Table.

**Table 7-194. CLK_CFG31 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 6 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 5 | RESERVED | R/W | 0b | Reserved bit; Write only reset value |
| 4 | DIG_DAC_MODCLK_DIV_EN | R/W | 0b | DAC MODCLK divider enable<br>0d = divider disabled<br>1d = divider enabled |
| 3 | PASI_BDIV_EN | R/W | 0b | PASI BDIV divider enable<br>0d = divider disabled<br>1d = divider enabled |
| 2 | SASI_BDIV_EN | R/W | 0b | SASI BDIV divider enable<br>0d = divider disabled<br>1d = divider enabled |
| 1 | PASI_FSYNC_DIV_EN | R/W | 0b | PASI FSYNC DIV divider enable<br>0d = divider disabled<br>1d = divider enabled |
| 0 | SASI_FSYNC_DIV_EN | R/W | 0b | SASI FSYNC DIV divider enable<br>0d = divider disabled<br>1d = divider enabled |

### 7.5.3.37 CLKOUT_CFG1 Register (Address = 0x46) [Reset = 0x00]

CLKOUT_CFG1 is shown in Table 7-195.

Return to the Summary Table.

This register is the CLKOUT configuration register 1.

**Table 7-195. CLKOUT_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-3 | RESERVED | R | 00000b | Reserved bits; Write only reset value |

ADVANCE INFORMATION

**ADVANCE INFORMATION**

**Table 7-195. CLKOUT_CFG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 2-0 | CLKOUT_CLK_SEL[2:0] | R/W | 000b | General Purpose CLKOUT divider clock source selection.<br>0d = Source clock is PLL output<br>1d = Source clock is primary ASI BCLK<br>2d = Source clock is secondary ASI BCLK<br>3d = Source clock is CCLK<br>4d = Source clock is internal oscillator clock<br>5d = Source clock is DSP clock<br>6d to 7d = Reserved |

### 7.5.3.38 CLKOUT_CFG2 Register (Address = 0x47) [Reset = 0x01]

CLKOUT_CFG2 is shown in Table 7-196.

Return to the Summary Table.

This register is the CLKOUT configuration register 2.

**Table 7-196. CLKOUT_CFG2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | CLKOUT_DIV_EN | R/W | 0b | CLKOUT divider enable.<br>0d = CLKOUT divider disabled<br>1d = CLKOUT divider enabled |
| 6-0 | CLKOUT_DIV[6:0] | R/W | 0000001b | CLKOUT DIV divider value.<br>0d = CLKOUT_DIV value is 128<br>1d = CLKOUT_DIV value is 1<br>2d = CLKOUT_DIV value is 2<br>3d to 126d = CLKOUT_DIV value is as per configuration<br>127d = CLKOUT_DIV value is 127 |

### 7.5.3.39 SARCLK_CFG1 Register (Address = 0x49) [Reset = 0x00]

SARCLK_CFG1 is shown in Table 7-197.

Return to the Summary Table.

This register is the SAR clock configuration register 1

**Table 7-197. SARCLK_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | SAR_CLK_FREQ_SEL[1:0] | R/W | 00b | SAR clock frequency mode<br>0d = SAR clock frequency is ~6MHz<br>1d = SAR clock frequency is ~3MHz<br>2d = SAR clock frequency is ~1.5MHz<br>3d = SAR clock frequency is ~12MHz (valid only when SAR clock is generated directly using internal oscilator clock |
| 5 | SAR_CLK_SRC_AUTO_DIS | R/W | 0b | SAR divider source clock auto selection disable<br>0d = SAR divider source clock auto-selection based on clock detection scheme<br>1d = SAR divider source clock auto-selection disabled and selected based on BST_CLK_SRC_SEL |
| 4 | SAR_CLK_SRC_MANUAL_SEL | R/W | 0b | SAR clock source manual selection (don't care in auto mode)<br>0d = SAR clock generated based on Audio clock available for ADC/DAC<br>1d = SAR clock generated based on internal oscillator clock |
| 3 | SAR_CLK_EN_AUTO_DIS | R/W | 0b | SAR divider source clock auto selection disable<br>0d = SAR divider auto-enabled<br>1d = SAR divider enabled/disabled based on manual control using BST_CLK_EN |

Product Folder Links: *TAD5212*

**Table 7-197. SARCLK_CFG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 2 | SAR_CLK_MANUAL_EN | R/W | 0b | SAR divider manual enable (don't care in auto mode)<br>0d = SAR divider disabled<br>1d = SAR divider enabled |
| 1-0 | SAR_CLK_MANUAL_DIV[1:0] | R/W | 00b | SAR divider value (don't care in auto mode)<br>0d = SAR divider value is 1<br>1d = SAR divider value is 2<br>2d = SAR divider value is 4<br>3d = SAR divider value is 8 |

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

# 8 Application and Implementation

## 8.1 Application Information

The TAD5212 is a stereo, high-performance audio DAC that supports sample rates of up to 768 kHz. The device supports up to 4 channel simultaneous playback which can be configured as a 2 channel differential or psuedo differential output or up to 4 channel single-ended output with options for headphone and lineout drive capabilities.

Communication to the TAD5212 for configuration of the control registers is supported using an I$^2$C or SPI interface. The device supports a highly flexible, audio serial interface (TDM, I$^2$S, and LJ) to transmit audio data seamlessly in the system across devices.

## 8.2 Typical Application

### 8.2.1 Application

Figure 8-1 shows a typical configuration of the TAD5212 for an application using two channel lineout operation with an I$^2$C control interface and a time-division multiplexing (TDM) audio data target interface.
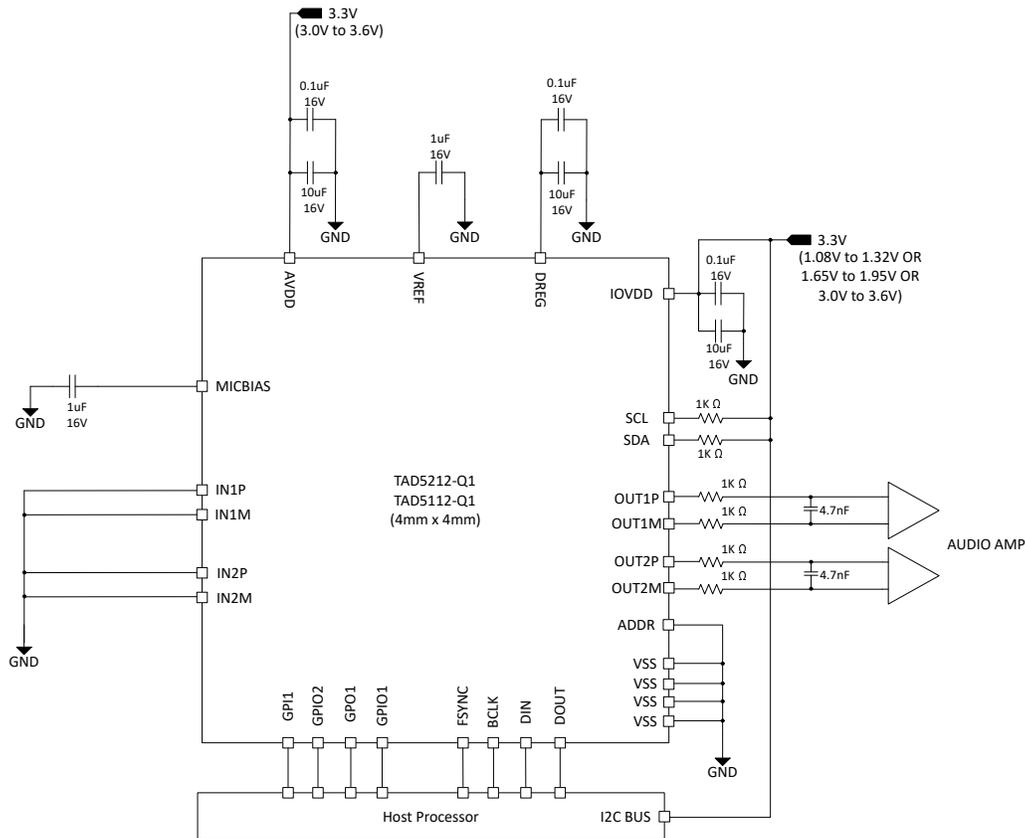


**Figure 8-1. Stereo Lineout Block Diagram**

### 8.2.2 Design Requirements

Table 8-1 lists the design parameters for this application.

**Table 8-1. Design Parameters**

| PARAMETER | VALUE |
|---|---|
| AVDD | 3.3V |
| IOVDD | 1.2V or 1.8V or 3.3V |
| AVDD supply current consumption | TBD |
| IOVDD supply current consumption | TBD |
| Maximum MICBIAS current | 5mA |
| Load on OUT1M, OUT1P, OUT2M, OUT2P | >600 ohms |

### 8.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAD5212 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
   a. Power up the IOVDD and AVDD power supplies
   b. Wait for at least 1ms to allow the device to initialize the internal registers.
   c. The device now goes into sleep mode (low-power mode < 10 μA)
2. Transition from sleep mode to active mode whenever required for the operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Override the default configuration registers or programmable coefficients value as required (this step is optional)
   d. Enable all desired audio serial interface input/output channels by writing to P0_R40 to P0_R47 for DAC
   e. Power-up the DAC by writing to P0_R120
   f. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

      This specific step can be done at any point in the sequence after step a.

      See the *Section 7.3.1.4* section for supported sample rates and the BCLK to FSYNC ratio.
   g. The device recording data is now sent to the host processor using the TDM audio serial data bus and playback data from TDM is now played on the lineout
3. Transition from active mode to sleep mode (again) as required in the system for low-power operation:
   a. Enter sleep mode by writing to P0_R2 to enable sleep mode
   b. Wait at least 6 ms (when FSYNC = 48 kHz) for the volume to ramp down and for all blocks to power down
   c. Read P0_R122 to check the device shutdown and sleep mode status
   d. If the device P0_R122_D[7:5] status bit is 3'b100 then stop FSYNC and BCLK in the system
   e. The device now goes into sleep mode (low-power mode < 10 μA) and retains all register values
4. Transition from sleep mode to active mode (again) as required for the recording operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio
   d. The device recording data is now sent to the host processor using the TDM audio serial data bus and playback data from TDM is now played on the lineout
5. Repeat step 4 and step 5 as required for mode transitions

Submit Document Feedback   131

Product Folder Links: *TAD5212*

ADVANCE INFORMATION

## 9 Power Supply Recommendations

The power-supply sequence between the IOVDD and AVDD rails can be applied in any order. However, after all supplies are stable, then only initiate the I$^2$C or SPI transactions to initialize the device.

For the supply power-up requirement, $t_1$, $t_2$ must be at least 2 ms to allow the device to initialize the internal registers. See the *Section 7.4* section for details on how the device operates in various modes after the device power supplies are settled to the recommended operating voltage levels. For the supply power-down requirement, $t_3$, $t_4$ must be at least 10 ms. This timing (as shown in Figure 9-1) allows the device to ramp down the volume on the playback data, power down the analog and digital blocks, and put the device into shutdown mode. The device can also be immediately put into shutdown mode by ramping down power supplies, but doing so causes an abrupt shutdown.
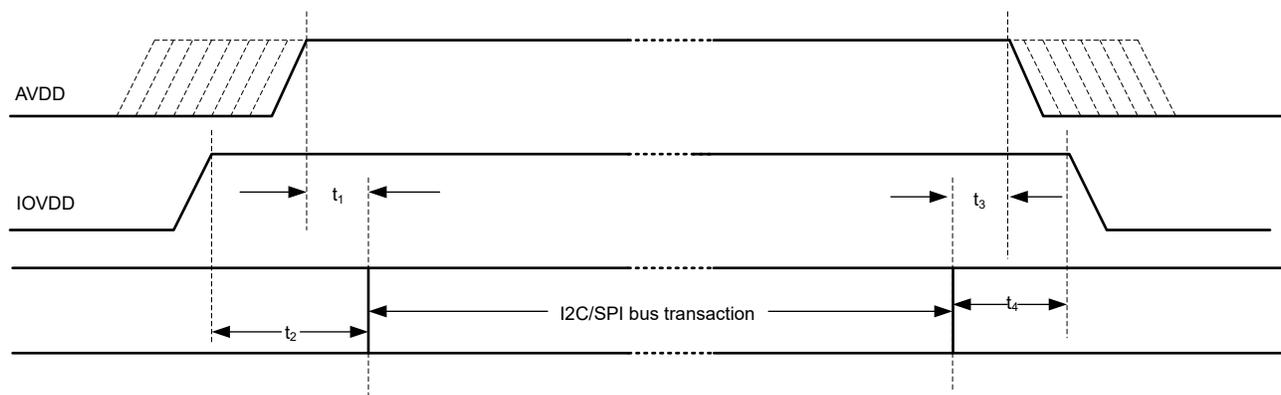


**Figure 9-1. Power-Supply Sequencing Requirement Timing Diagram**

Make sure that the supply ramp rate is slower than 0.1V/µs and that the wait time between a power-down and a power-up event is at least 100 ms. For supply ramp rate slower than 0.1 V/ms, host device must apply a software reset as first transaction before doing any device configuration. Make sure all digital input pins are at valid input levels and not toggling during supply sequencing.

The TAD5212 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Documentation Support

#### 10.1.1 Related Documentation

### 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

### 10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

### 10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
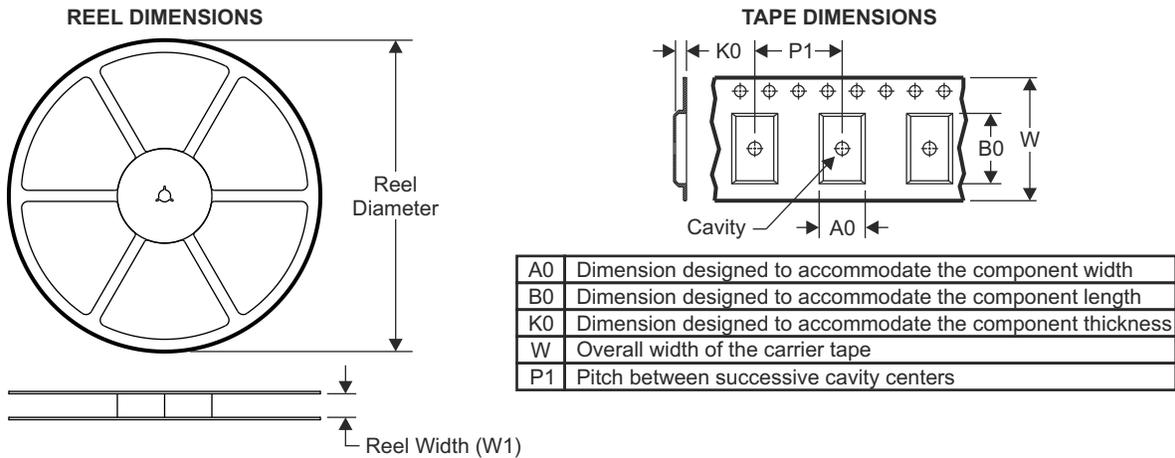
### 10.6 Glossary

TI Glossary          This glossary lists and explains terms, acronyms, and definitions.
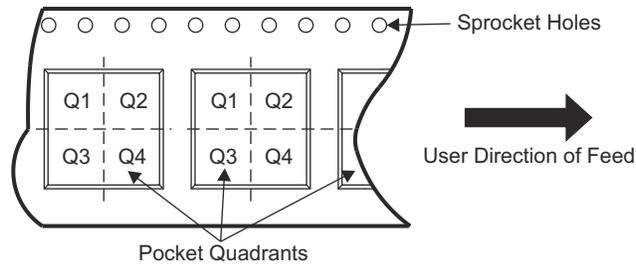
## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**ADVANCE INFORMATION**

## 11.1 Tape and Reel Information

**REEL DIMENSIONS**



**TAPE DIMENSIONS**



| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| XTAD5212IRGER | VQFN | RGE | 24 | 3000 | 330.0 | 12.4 | 4.25 | 4.25 | 1.15 | 8.0 | 12.0 | Q1 |

ADVANCE INFORMATION

Product Folder Links: *TAD5212*

**TAPE AND REEL BOX DIMENSIONS**
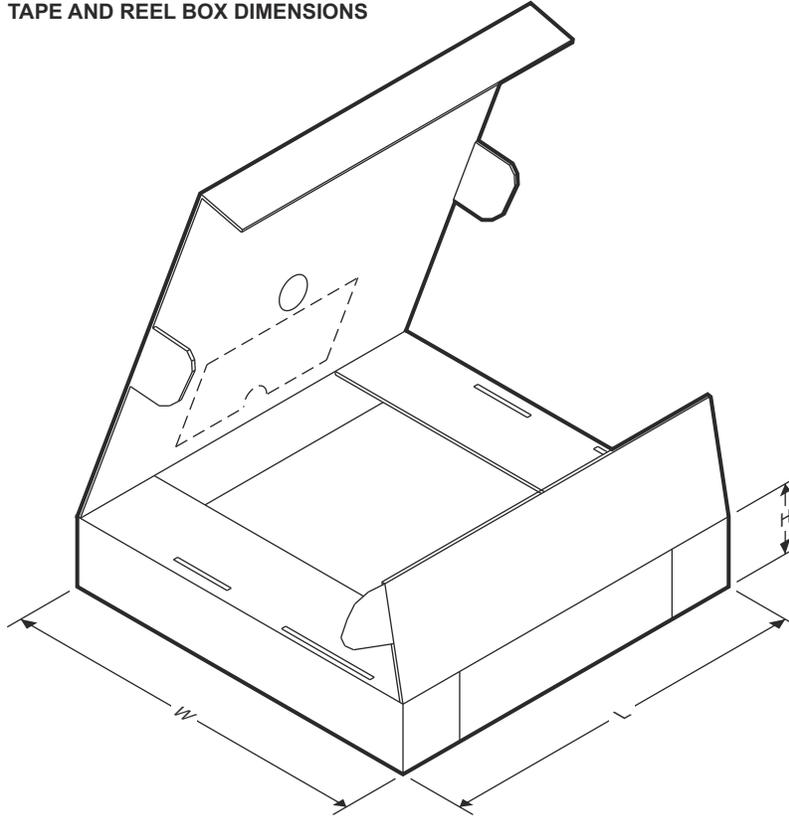


| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| XTAD5212IRGER | VQFN | RGE | 24 | 3000 | 367.0 | 367.0 | 35.0 |

**ADVANCE INFORMATION**

Texas
INSTRUMENTS
www.ti.com

ADVANCE INFORMATION

## PACKAGE OUTLINE

RGE0024R

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD



4225246/A   08/2019
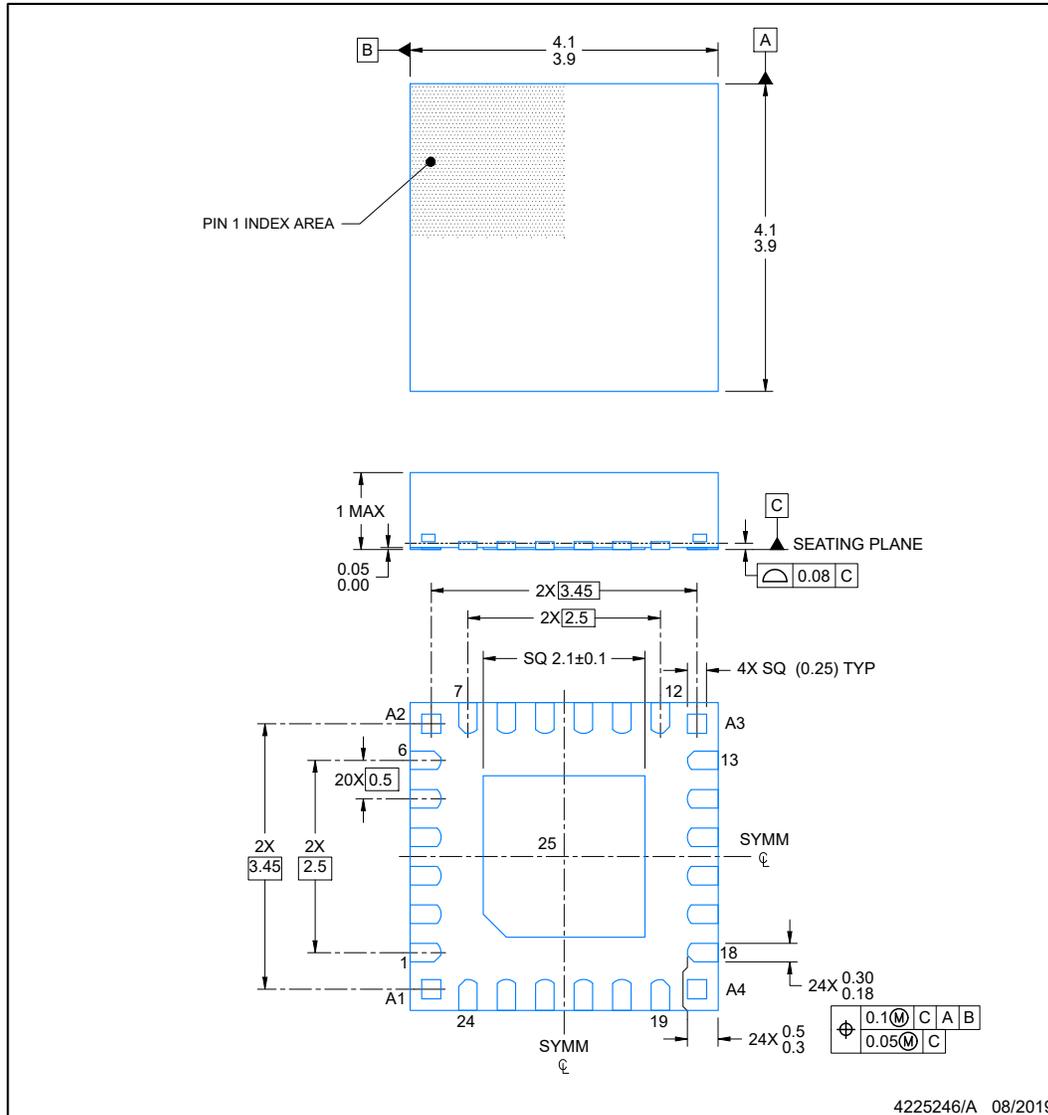
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

Texas
INSTRUMENTS
www.ti.com

# EXAMPLE BOARD LAYOUT

## RGE0024R

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

ADVANCE INFORMATION



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

SOLDER MASK DETAILS

NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED
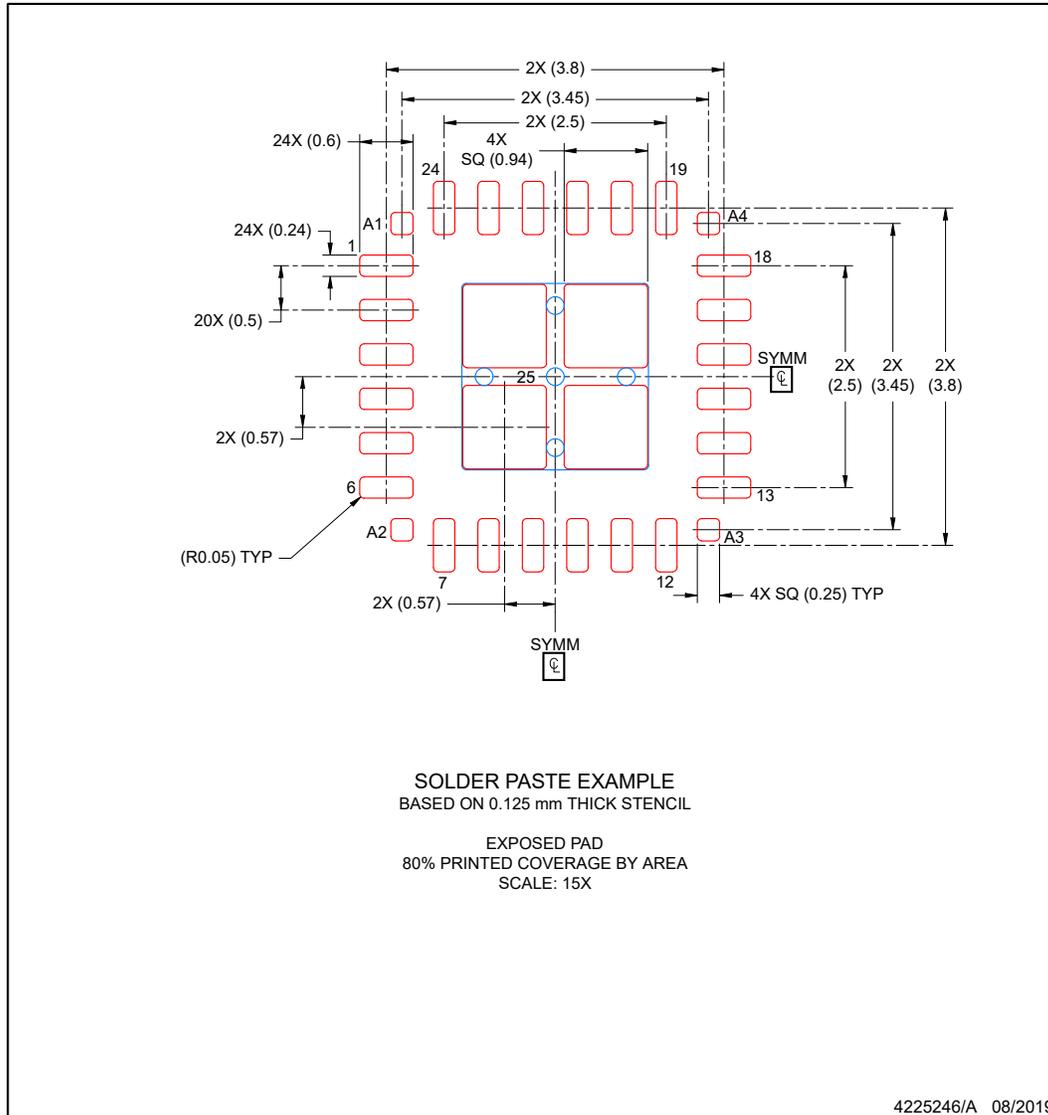
4225246/A   08/2019
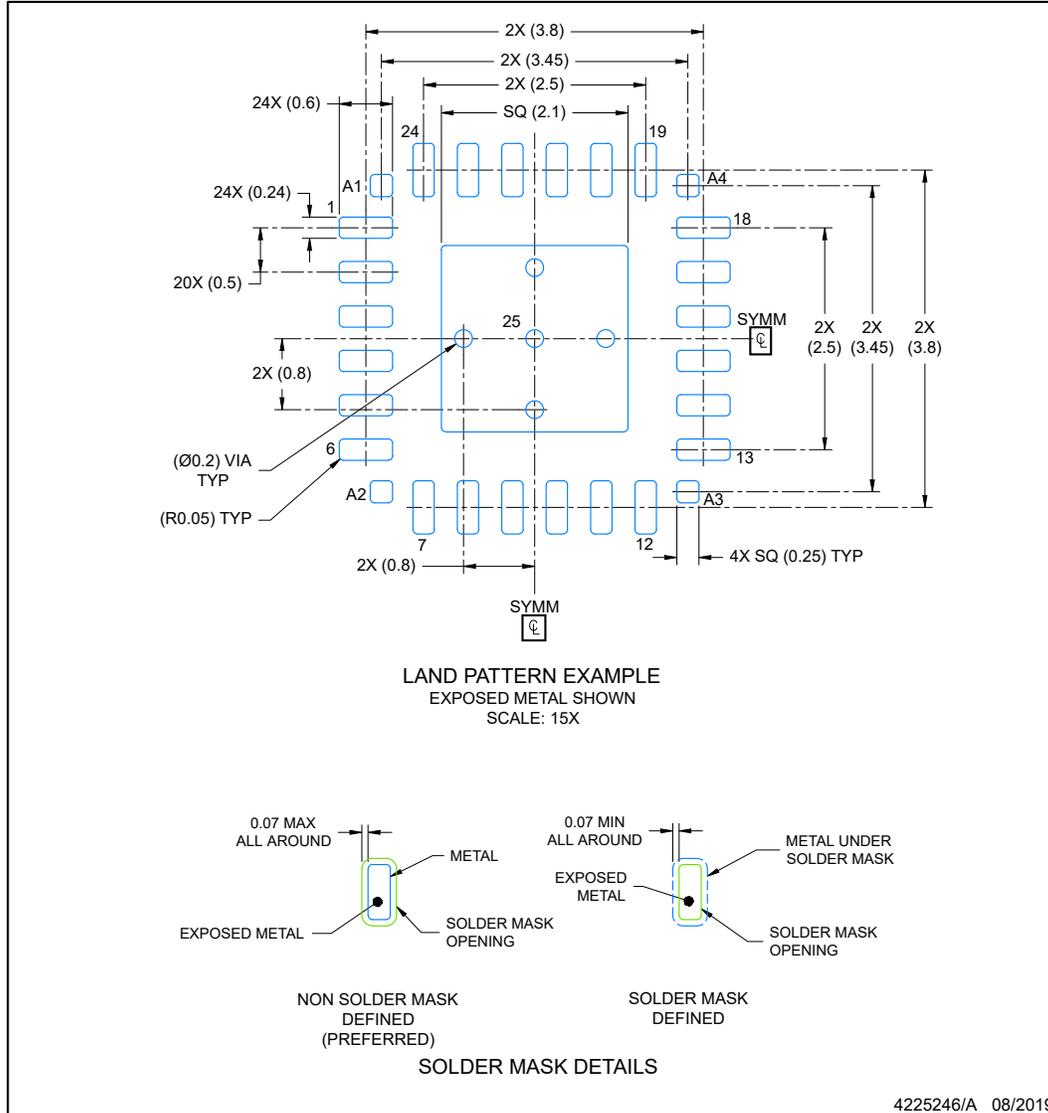
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

Product Folder Links: TAD5212

**EXAMPLE STENCIL DESIGN**

RGE0024R

**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK-NO LEAD

ADVANCE INFORMATION



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4225246/A   08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

Product Folder Links: *TAD5212*

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| XTAD5212IRGER | ACTIVE | VQFN | RGE | 24 | 3000 | TBD | Call TI | Call TI | -40 to 125 | | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.
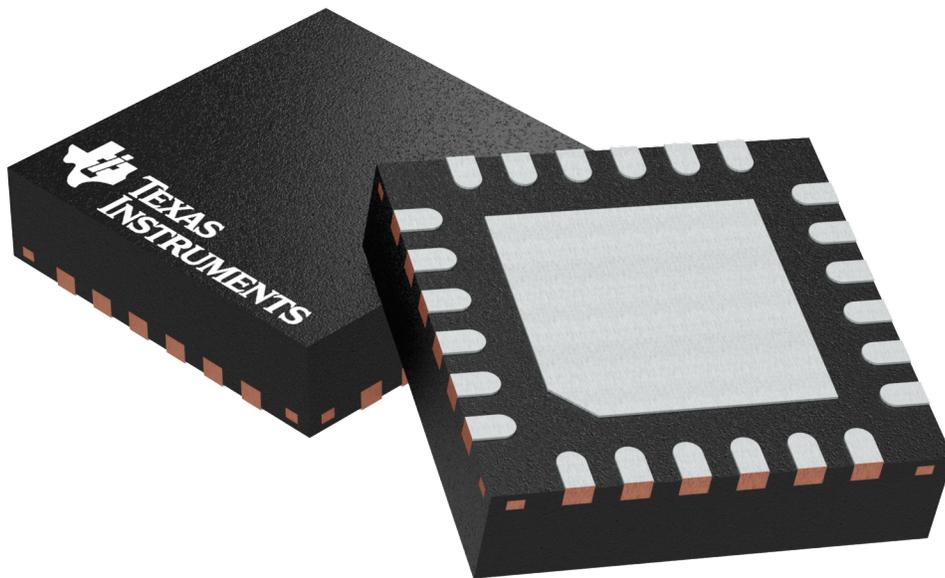
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated