Multipoint-Low Voltage Differential Signaling (M-LVDS) Evaluation Module

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1 Related Documentation From Texas Instruments and Others

- *Introduction to M-LVDS* (SLLA108)
- *LVDS Designer's Notes* (SLLA014).
- *Reducing EMI With Low Voltage Differential Signaling* (SLLA030).
- *Interface Circuits for TIA/EIA-644 (LVDS)* (SLLA038).
- *Transmission at 200 Mbps in VME Card Cage Using LVDM* (SLLA088).
- *LVDS Multidrop Connections* (SLLA054).
- SN65MLVD20x data sheets, *Multipoint-LVDS Line Drivers and Receivers*, (SLLS573 and SLLS558)
- *Electromagnetic Compatibility Printed Circuit Board and Electronic Module Design*, VEC workshop, Violette Engineering Corporation.

2 M-LVDS Evaluation Module

This document describes the multipoint low-voltage differential-signaling (M-LVDS) evaluation module (EVM) used to aid designers in development and analysis of this new signaling technology. The Texas Instruments SN65MLVD2DRB and SN65MLVD3DRB series are low-voltage differential line receivers complying with the M-LVDS standard (TIA/EIA-899). The EVM kit contains the assembled printed-circuit board and all of the released devices referred to in Table 1. Using the EVM to evaluate these devices should provide insight into the design of low-voltage differential circuits. The EVM board allows the designer to connect an input to the driver and configure a point-to-point or multidrop data bus.

The EVM can be used to evaluate device parameters while acting as a guide for high-frequency board layout. The board allows for the connection of a 100-Ω controlled impedance cable of varying lengths. This provides the designer with a tool for evaluation and successful design of an end product.

2.1 Overview

The EVM comes with all the production devices in Table 1. The SN65MLVD3 and SN65MLVD201 are installed on the circuit board, and can easily be replaced with the other devices supplied, namely, SN65MLVD2DRB and SN65MLVD204AD. These are all TIA/EIA-899 M-LVDS standard compliant devices. While initially intended for half-duplex or multipoint applications, M-LVDS devices are not precluded from being used in a point-to-point or multidrop configuration. In these configurations there can be a distinct advantage to the additional current drive provided by an M-LVDS driver.

The M-LVDS devices shown in Table 1 all include output slew-rate limited drivers, thus the need for different nominal signaling rates. The M-LVDS standard recommends the transition time not exceed 0.5 of the unit interval (UI). The definition of transition time (t_r and t_f) in M-LVDS is the 10% to 90% levels shown in Figure 1. Using the maximum transition time for each of the drivers and the 0.5(t_{UI}) *rule* results in the signaling rates shown in Table 1. This slew-rate control differentiates M-LVDS devices from LVDS (TIA/EIA-644A) compliant devices. The slower transition times available with M-LVDS help to reduce higher frequency components in the transmitted signal. This reduces EMI and allows longer stubs on the main transmission line. For this reason it is generally better to select a driver with a specified signaling rate no greater than is required in the system.

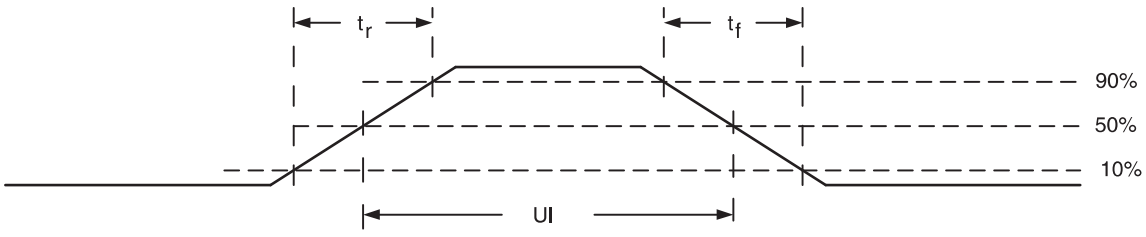


Figure 1. M-LVDS Unit Interval Definition

Table 1. M-LVDS Devices Supported by the EVM

Nominal Signaling Rate (Mbps)	Footprints	Receiver Type	Part Number	Status
250	SON	Type-1	SN65MLVD2DRB	Production
250	SON	Type-2	SN65MLVD3DRB	Production
200	SN75176	Type-1	SN65MLVD201D	Production
100	SN75176	Type-2	SN65MLVD204AD	Production

The EVM has been designed with the receiver section (DRB footprint, U1) on one half of the board and the transceiver section (SN75176 footprint, U2) on the other half (see Figure 21). The EVM as delivered incorporates footprints for two 100-Ω termination resistors at each driver output and receiver input. These allow the user to evaluate a single driver, receiver, or transceiver, while not having to deal with a transmission line or additional I/Os.

Jumpers are included to allow the two sections of the EVM to either share the same power and ground or be run off of independent supplies. Ground shifts or common-mode offsets can be introduced by the removal of these jumpers and using separate power supplies.

2.2 M-LVDS Standard TIA/EIA-899

The M-LVDS standard was created in response to a demand from the data communications community for a general-purpose high-speed balanced interface standard for multipoint applications. The TIA/EIA-644 standard defines the LVDS electrical-layer characteristics used for transmitting information in point-to-point and multidrop architectures. TIA/EIA-644 does not address data transmission for multipoint architectures, therefore the need for development of a new standard.

The standard, Electrical Characteristics of Multipoint-Low-Voltage Differential Signaling (M-LVDS) TIA/EIA-899, specifies low-voltage differential signaling drivers and receivers for data interchange across half-duplex or multipoint data bus structures. M-LVDS is capable of operating at signaling rates up to 500 Mbps. In other words, when the devices are used at the nominal signaling rate, the rise and fall times are within the specified values in the standard. The M-LVDS standard defines the transition time (t_r and t_f) to be 1 ns or slower into a test load. Using this information combined with the requirement that the transition time not exceed 0.5 of the unit interval (UI), gives a minimum unit interval of 2 ns, leading to the 500 Mpbs maximum signaling rate.

The standard defines Type-1 and Type-2 receivers. Type-1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type-2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. Type-1 receivers maximize the differential noise margin and are intended for the maximum signaling rate. Type-2 receivers are intended for control signals, slower signaling rates, or where failsafe provisions are needed. The bus voltage logic state definition can be seen in Table 2 and Figure 2.

Table 2. Receiver Input Voltage Threshold Requirements

Receiver Type	Low	High
Type-1	$-2.4\ V \le V_{ID} \le -0.05\ V$	$0.05\ V \le V_{ID} \le 2.4\ V$
Type-2	$-2.4\ V \le V_{ID} \le 0.05\ V$	$0.15\ V \le V_{ID} \le 2.4\ V$

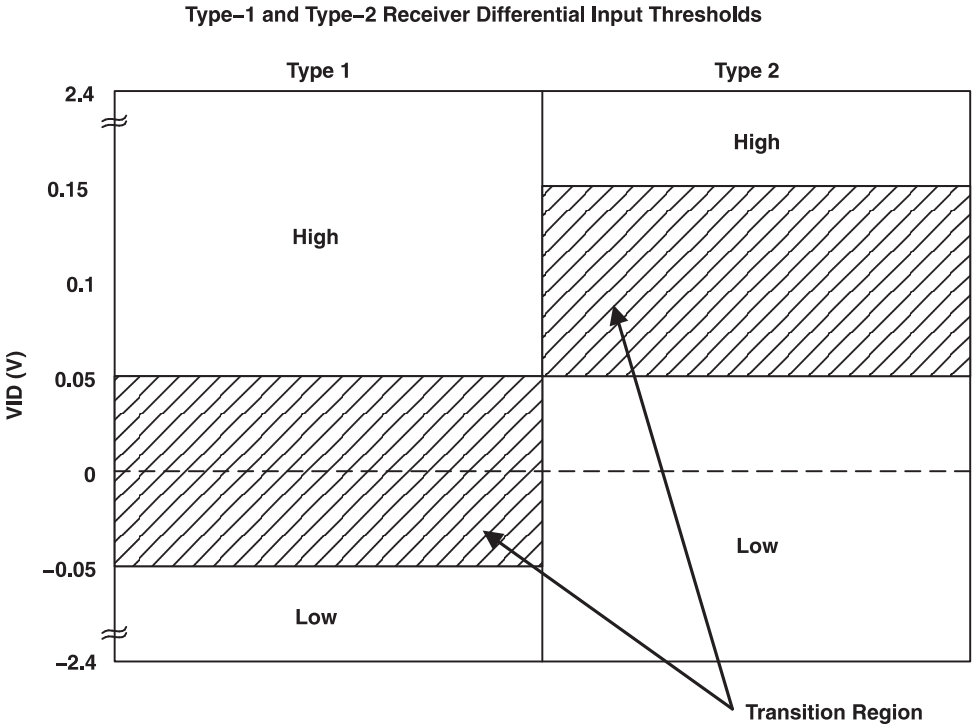


Figure 2. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region

2.3 M-LVDS EVM Kit Contents

The M-LVDS EVM kit contains the following:

- M-LVDS EVM PCB with SN65MLVD201D and SN65MLVD3DRB installed (6424409B)
- Additional devices SN65MLVD2DRB and SN65MLVD204AD
- M-LVDS EVM kit documentation (user's guide)
- *SN65MLVD200A, SN65MLVD202A, SN65MLVD204A, and SN65MLVD205A, Multipoint-LVDS Line Driver and Receiver* data sheet (SLLS573 and)
- *SN65MLVD201, SN65MLVD203, SN65MLVD206, and SN65MLVD207, Multipoint-LVDS Line Driver and Receiver* data sheet (SLLS558)
- *SN65MLVD2, SN65MLVD3, Single M-LVDS Receivers* data sheet (SLLS767)

2.4 Configurations

The M-LVDS EVM board allows the user to construct various bus configurations. The two devices on the EVM allow for point-to-point simplex, parallel-terminated point-to-point simplex, and two-node multidrop operation. All of these modes of operation can be configured through onboard jumpers, external cabling, and different resistor combinations. The devices which are delivered with the EVM change output operation but, configuration of jumpers to setup the transmission type is independent of the devices installed

2.4.1 Point-to-Point

The point-to-point simplex configuration is shown in Figure 3. The setup schematic for this option is shown in Figure 9. Although this is not the intended mode of operation for M-LVDS, it works well for high noise or long higher-loss transmission lines. Due to the increased drive current, a single 100-Ω termination resistor on the EVM results in a differential bus voltage (V_{OD}) twice as large as a doubly terminated line. This practice is acceptable as long as the combination of input voltage and common-mode voltage does not exceed absolute maximum ratings of the line circuits.

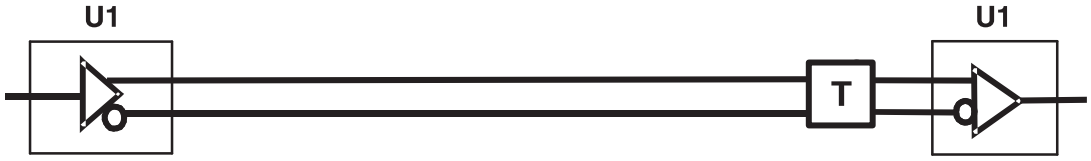


Figure 3. Point-to-Point Simplex Circuit

This configuration also can have a termination at the source and load (parallel terminated), thereby, keeping normal M-LVDS signal levels as shown in Figure 4.

The schematic for this option is shown in Figure 10. Due to the increased drive current, double termination can be used to improve transmission line characteristics.

Figure 4. Parallel Termination Simplex Circuit

2.4.2 Multidrop

A multidrop configuration (see Figure 5) with two receiver nodes can be simulated with the EVM. To get additional receiver nodes on the same bus requires additional EVMs. M-LVDS controlled driver transition times and higher signal levels help to accommodate the multiple stubs and additional loads on the bus. This does not exempt good design practices, which would keep stubs short to help prevent excessive signal reflections.

A bus line termination could be placed at both ends of the transmission line, improving the signal quality by reducing return reflections to the driver. This would allow the use of standard compliant TIA/EIA 644A receivers on the bus in addition to M-LVDS receivers.

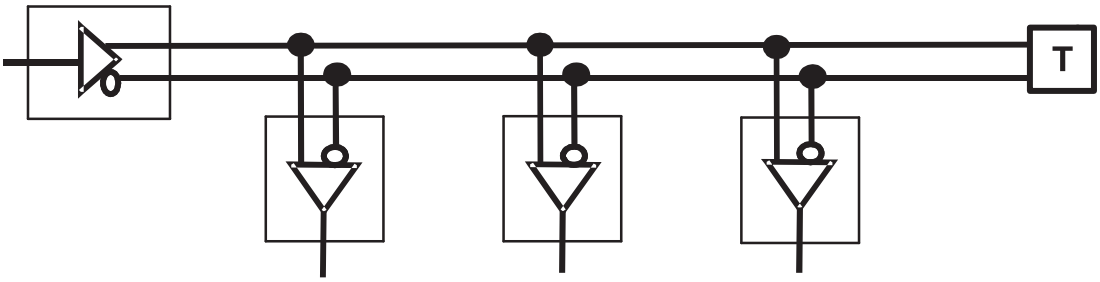


Figure 5. Multidrop or Distributed Simplex Circuit

2.4.3 Multipoint

The multipoint configuration is the primary application of the M-LVDS devices and the associated standard. The M-LVDS standard allows for any combination of drivers, receivers, or transceivers up to a total of 32 on the line. Figure 6 shows a representation of a five-node multipoint configuration using transceivers. Increased drive current, in addition to the wider common-mode input, allows M-LVDS parts to drive multiple receivers over longer line lengths with up to 2 V of ground noise.

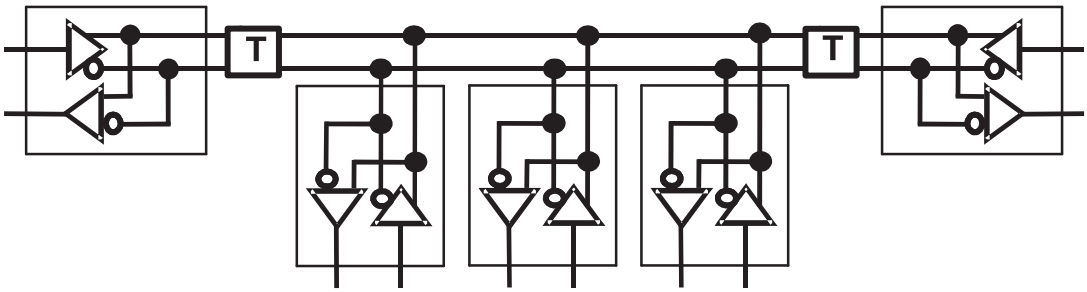


Figure 6. Five-Node Multipoint Circuit

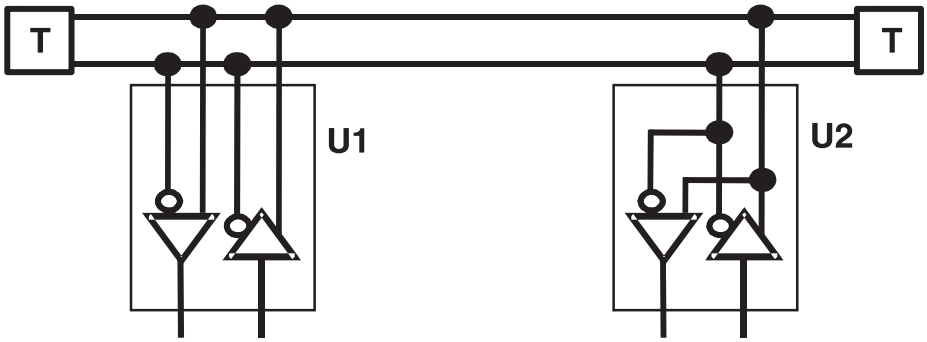


Figure 7. Two-Node Multipoint Circuit

2.4.4 EVM Operation With Separate Power Supplies

The EVM has been designed with independent power planes for the two devices. The two devices can be powered with independent supplies or with a single supply. Sending and receiving data between backplanes, racks, or cabinets where separate power sources may exist can have offset ground potentials between nodes. Jumpers JP9, 10, 11, and 12 tie the two separate power and ground planes together. If two separate supplies are used and jumpers JP9, 10, 11, and 12 are removed, care should be taken to ensure the absolute maximum device ratings are not exceeded. Keep in mind that if jumpers JP9, 10, 11, and 12 are not removed when using separate power supplies, a difference in potential between the supplies causes a current to flow between supplies and through the jumpers.

The EVM can be configured with three power supplies with isolated outputs in such a way as to input a fixed offset between the grounds (see Figure 8). This induces a ground potential difference voltage between U1 and U2. To demonstrate this capability, the following steps should be followed.

1. Adjust PS1 and PS3 to the supply voltage (3.3V) and current limit to 60mA.
2. Set PS2 to 0V
3. Induce a ground offset by varying the output of PS2.

WARNING

PS2 Output

The PS2 output should not exceed ± 2 V to remain within the device ratings.

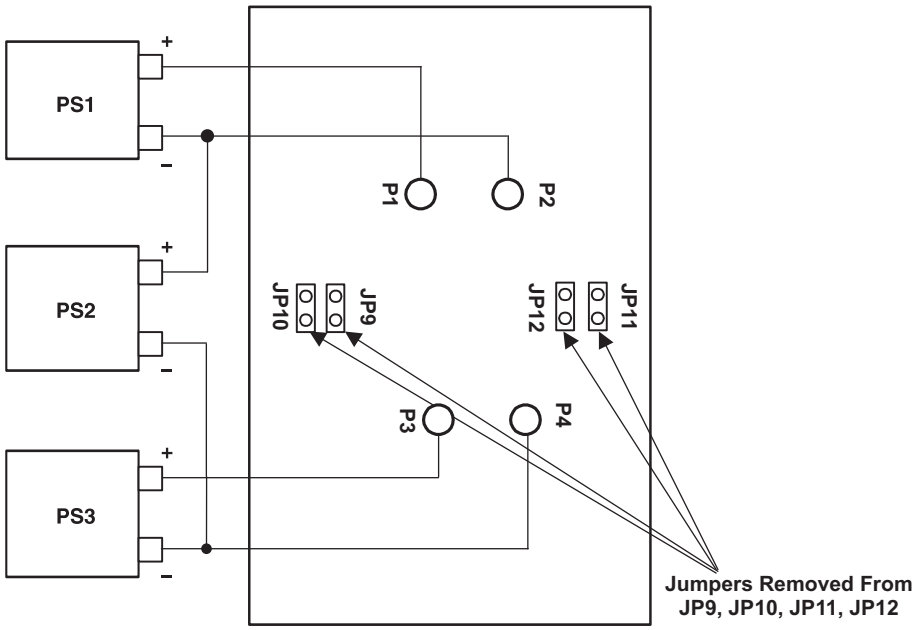


Figure 8. EVM Configuration for Including a Ground Potential Difference Voltage Between Nodes

2.5 Recommended Equipment

- 3.3 Vdc at 0.6-A power supply or multiple power supplies (with both devices powered and enabled, the board draws about 25 mA with no input signal applied).
- A 100-Ω transmission medium from the driver to the receiver, (twisted-pair cable recommended, CAT5 cable for example).
- A function or pattern generator capable of supplying 3.3-V signals at the desired signaling rate.
- A multiple-channel high-bandwidth oscilloscope, preferably above the 1-GHz range
- Differential or single-ended oscilloscope probes.

3 Test Setup

This section describes how to setup and use the M-LVDS EVM.

3.1 Typical Cable Test Configurations

Each of the following test configurations is a transmission line consisting of a twisted-pair cable connected on the 2-pin connectors (JP1and JP5). Table 3 shows the possible configurations.

In addition to the different transmission topologies, the EVM also can be configured to run off two or three separate power supplies, as described in the previous section. This allows the user to induce a ground shift or offset between the two different drivers and receivers. This setup can be used with any transmission line test.

Table 3. EVM Configuration Options

Configuration	Jumpers In	Resistors In	Resistors Out	Diagram
Point-to-point simplex transmission	JP3	R3	R2, 10, 11	Figure 9
Point-to-point parallel terminated simplex transmission	JP3	R3, 10	R2, 11	Figure 10
Two-node multipoint transmission	JP3, JP6	R3	R2, 10, 11	Figure 11

3.1.1 Point-to-Point Simplex Transmission

1. Connect a twisted-pair cable from JP1 to JP5.
2. Verify that resistor R3 is installed.
3. Remove resistors R2, R10, and R11. This properly terminates the transmission line at one end.
4. Enable the receiver of the device U1 by installing the jumper JP3.
5. Verify that the U2 receiver is disabled by ensuring that no jumper is installed on JP6.
6. Verify that the driver of device U2 is enabled by ensuring that jumper JP7 is uninstalled.

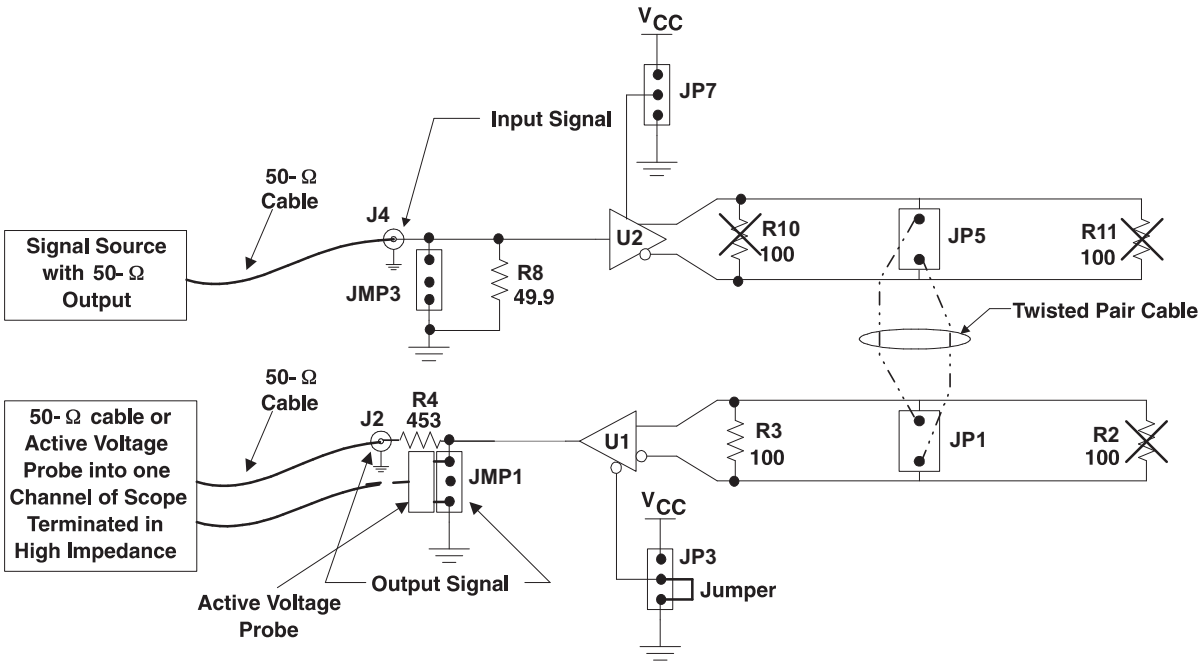


Figure 9. Point-to-Point Simplex Transmission

3.1.2 Point-to-Point Parallel Terminated Simplex Transmission

1. Connect a twisted-pair cable from JP1 to JP5.
2. Verify resistor R3 and R10 are installed.
3. Remove resistors R2 and R11, if already installed. This properly terminates the transmission line at both ends.
4. Enable the receiver of the device U1 by installing the jumper JP3.
5. Verify that the U2 receiver is disabled by ensuring that no jumper is installed on JP6.
6. Verify that the driver of device U2 is enabled by ensuring that jumper JP7 is uninstalled.

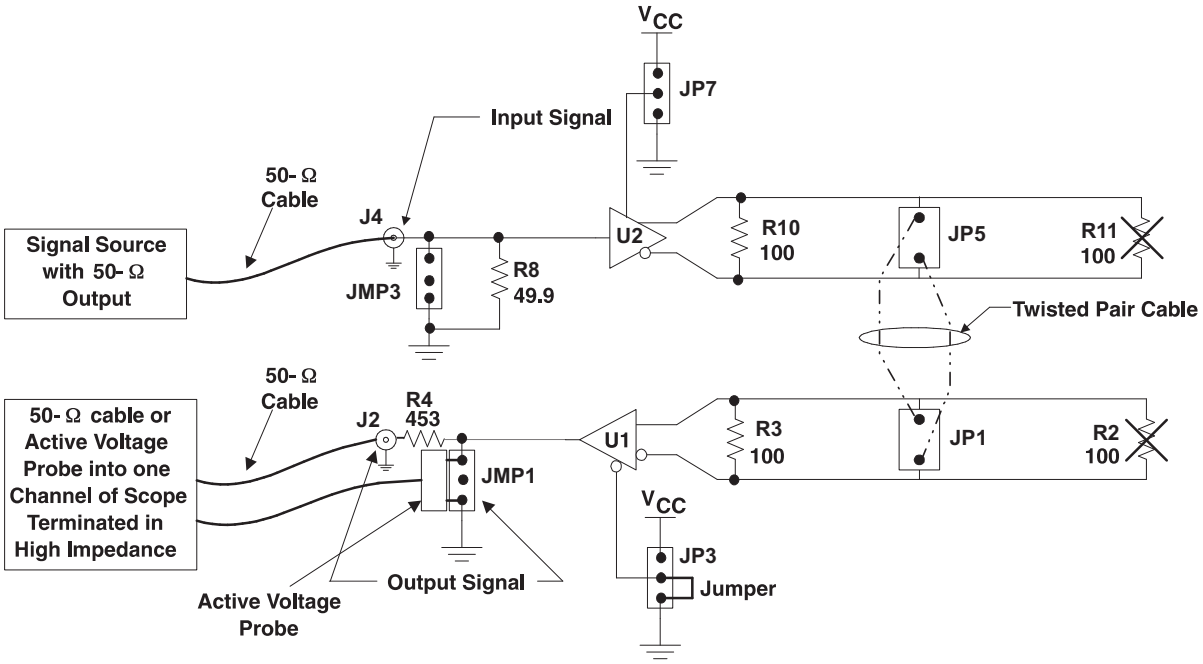


Figure 10. Point-to-Point Parallel Terminated Simplex Transmission

3.1.3 Two-Node Multidrop Transmission

1. Connect a twisted-pair cable from JP1 to JP5.
2. Verify that resistor R3 is installed.
3. Remove resistors R2, R10, and R11, if already installed. This properly terminates the transmission line at one end.
4. Enable the receiver of device U1 by installing the jumper JP3.
5. Enable the receiver of device U2 by installing the jumper JP6.
6. Verify that the driver of device U2 is enabled by ensuring that jumper JP7 is not installed.

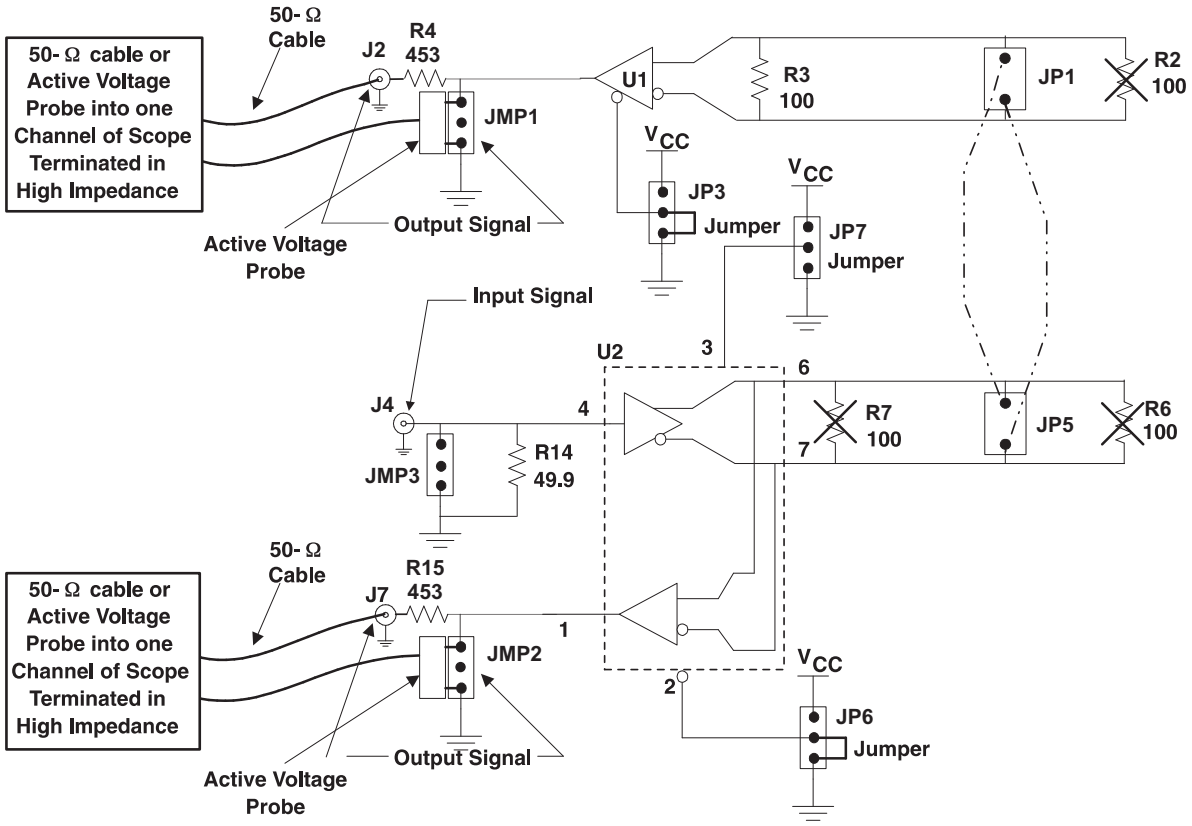


Figure 11. Two-Node Multidrop Transmission

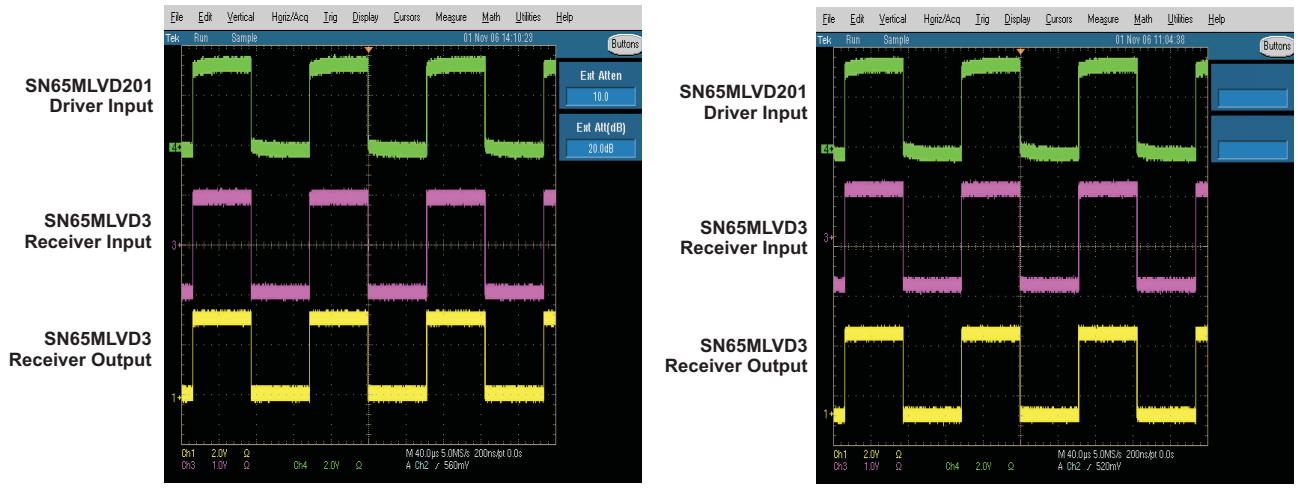
3.2 Test Results

The test configurations described in Section 2.1 were used to simulate point-to-point simplex, parallel-terminated point-to-point simplex, and two-node multidrop. The test results are shown in the following figures. An Agilent PARBERT was used to generate input signals, and a Tektronix TDS784D was used to collect the output data.

The EVM was populated with a SN65MLVD3 and SN65MLVD201 for U1 and U2, respectively. The eye patterns were measured with the source generating a clock pattern.

Figure 12, Figure 13, and Figure 14 show the point-to-point simplex transmission eye patterns. The top green Trace 4 is the driver input signal applied to the DIN signal at J4 and monitored at JMP3 using the high impedance single-ended probe. The middle pink Trace 3 is the signal at the receiver input JP1 using the high impedance differential probe. The bottom yellow Trace 1 is the receiver output of SN65MLVD3 at JMP1 using a high impedance single ended probe.

Measuring the output signal Rout on J2 or J7 with a 50-Ω cable terminated into 50-Ω at the scope requires installing a 453-Ω resistor in R4 and R15 which will attenuate the signal due to the 453-Ω resistor in series with the receiver output. The resistor is installed as a current limit for termination into a 50-Ω load. As can be seen in Figure 12, the magnitude of Trace 3 on the left is one-tenth of Trace 2 on the right because the scope has compensated for an External Attenuation factor of 10 dB or 20 dB.



50-Ω Output Termination **High-Impedance Output Termination**

Figure 12. Point-to-Point Simplex Typical Eye Patterns at 8 kHz

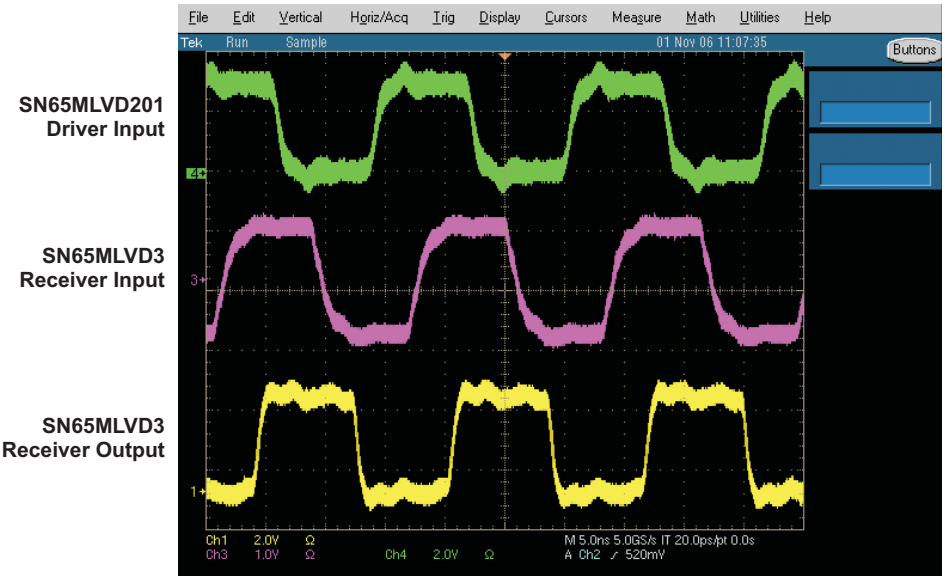


Figure 13. Point-to-Point Simplex Typical Eye Patterns at 61.44 MHz With High-Impedance Output Termination

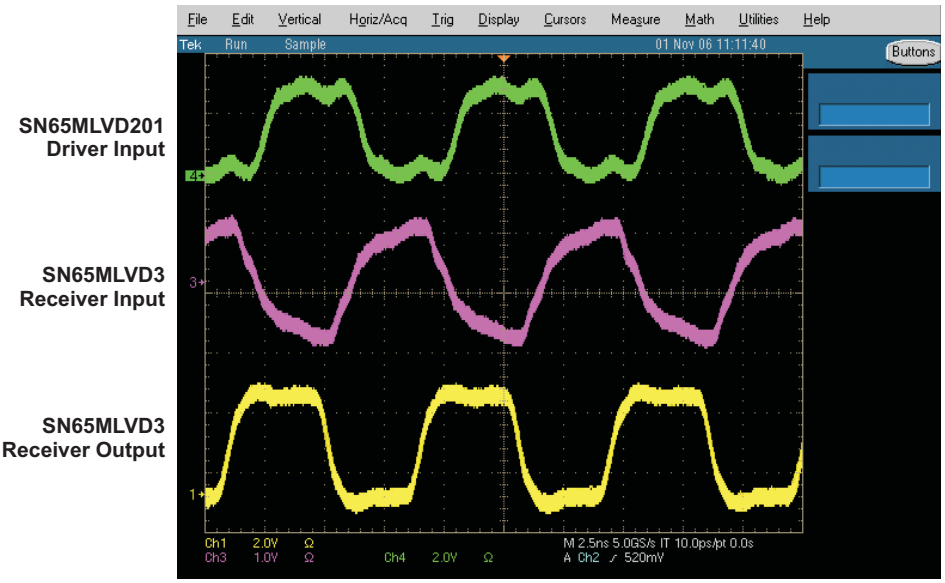


Figure 14. Point-to-Point Simplex Typical Eye Patterns at 125 MHz With High-Impedance Output Termination

The eye patterns in Figure 15, Figure 16, and Figure 17 are parallel-terminated point-to-point simplex data where the top green Trace 4 is the driver input signal applied to the DIN signal at J4 and monitored at JMP3 using the high-impedance, single-ended probe. The middle pink Trace 3 is the signal at the receiver input JP1 using the high-impedance differential probe. The bottom yellow Trace 1 is the receiver output of SN65MLVD3 at JMP1 using a high-impedance, single-ended probe.

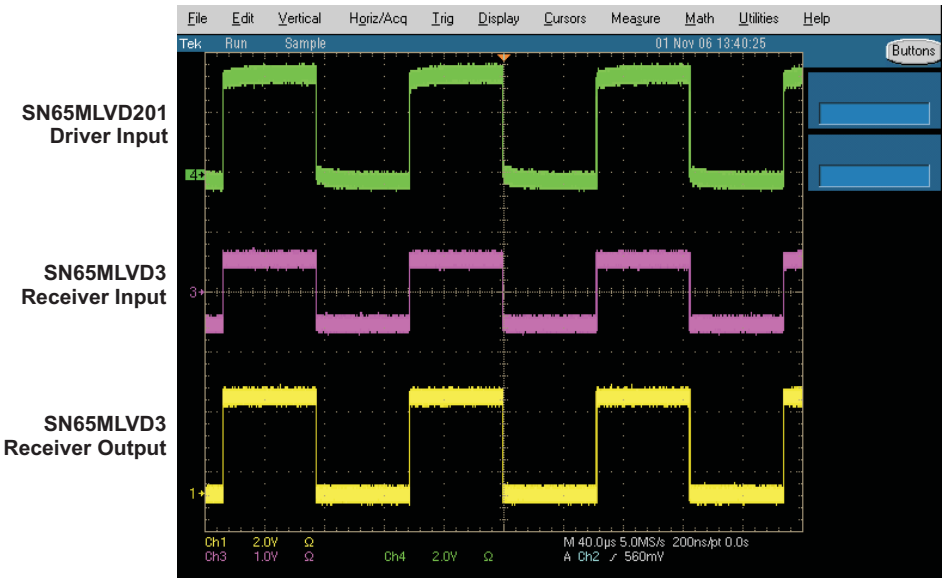


Figure 15. Parallel Terminated Point-to-Point Parallel Simplex Typical Eye Pattern at 8 kHz with High-Impedance Output Termination

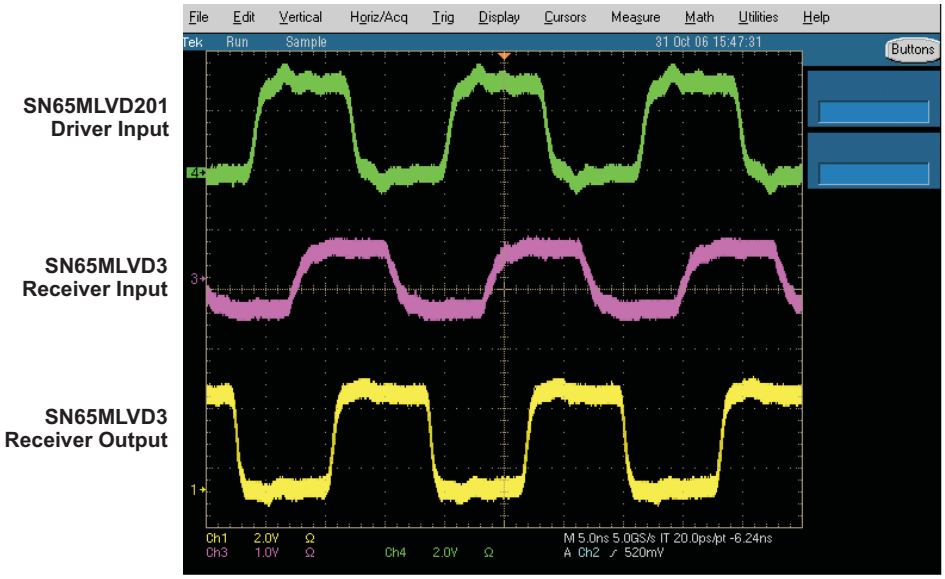


Figure 16. Parallel Terminated Point-to-Point Parallel Simplex Typical Eye Pattern at 61.44 MHz with High-Impedance Output Termination

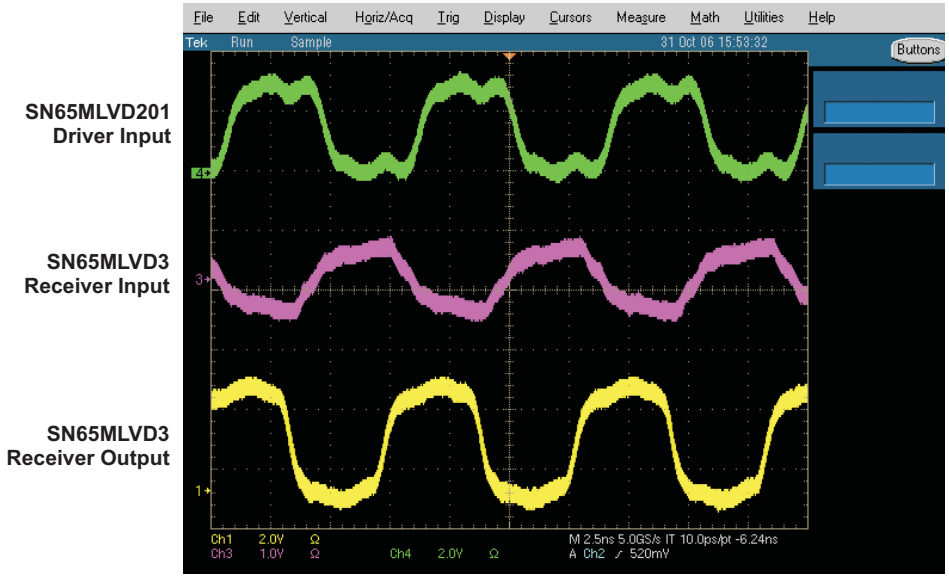


Figure 17. Parallel Terminated Point-to-Point Parallel Simplex Typical Eye Pattern at 125 MHz with High-Impedance Output Termination

Figure 18, Figure 19, and Figure 20 represent the two-node multidrop transmission eye patterns where the top green Trace 4 is the driver input signal applied to the DIN signal at J4 and monitored at JMP3 using the high-impedance, single-ended probe. The middle pink Trace 3 is the signal at the receiver input JP1 using the high-impedance differential probe. The bottom yellow Trace 1 is the receiver output of SN65MLVD3 at JMP1 using a high-impedance, single-ended probe. The offset zero-crossing shows the difference between Type-2 (Receiver #1 Output) and Type-1 (Receiver #2 Output).

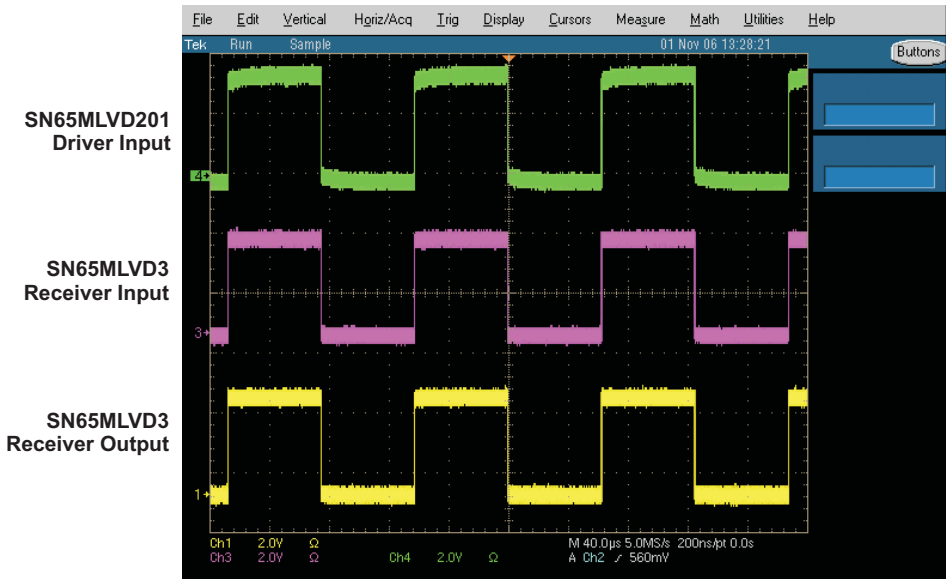


Figure 18. Two-Node Multidrop Typical Eye Pattern at 8 kHz With High-Impedance Output Termination

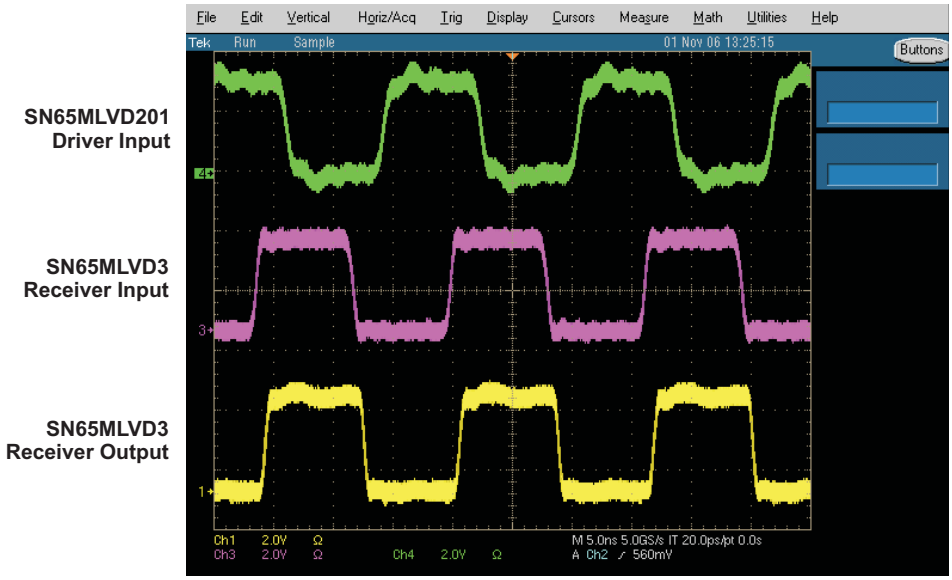


Figure 19. Two-Node Multidrop Typical Eye Pattern at 61.44 MHz With High-Impedance Output Termination

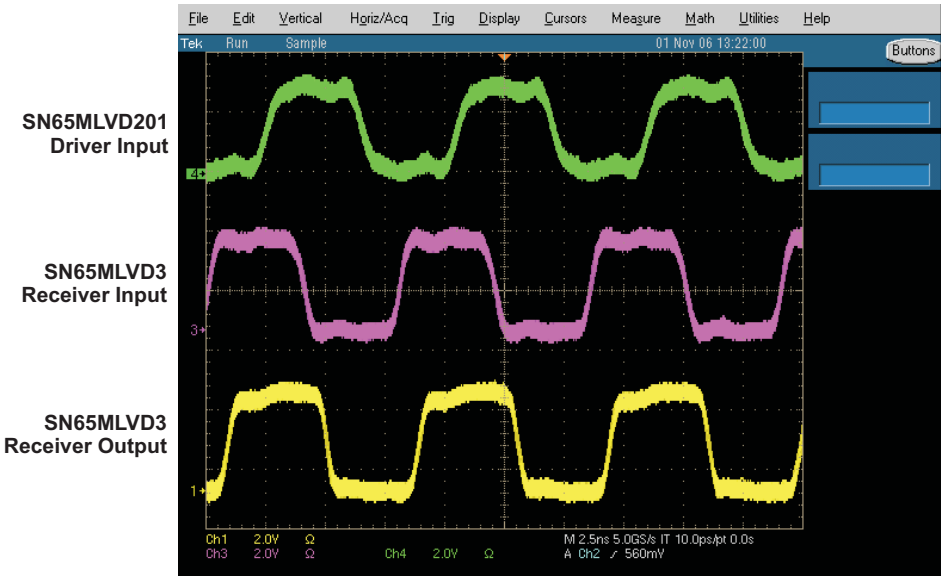


Figure 20. Two-Node Multidrop Typical Eye Pattern at 125 MHz With High-Impedance Output Termination

4 Bill of Materials, Board Layout, and PCB Construction

This section contains the bill of materials, board layout of the M-LVDS, and describes the printed-circuit board.

4.1 Bill of Materials

Table 4. M-LVDS EVM Bill of Materials

Item No.	Qty	Reference Designator	Part No.	Value	PCB Footprint	Manufacturer
1	1	C1	ECJ-2VC-1H1-50J	15pF uninstall	cc0805	Panasonic
2	1	C2	ECJ-2VB-1H1-03K	0.01µF uninstalled	cc0805	Panasonic
3	2	C3	ECJ-2VB-1H1-102K	0.001 µF uninstalled	cc0805	
4	2	C4,C8	GRM319R71H104KA01D	0.1uF	cc1206	Murata Electronics North America
5	2	C5,C9	ECJ-3YB-1E1-06M	10µF uninstalled	cc1206	Panasonic
6	1	C6	ECJ-1VB-1H1-03K	0.01 uninstalled	cc0603	Panasonic
7	1	C7	ECJ-1VB-1H1-102K	0.001 uninstalled	cc0603	Panasonic
8	2	C10,C13	293D106X0035D2W	10µF	cc7343	Sprague
9	2	C11,C14	TAJE686K025R	68µF	cc7343	AVX
10	2	C12,C15	12063G105ZAT2A	1.0µF	cc1206	AVX
11	1	C16		15pF uninstalled	cc0805	
12	3	JMP1–JMP3	4-103239-0x3	3 pin berg	jmp3	AMP
13	9	JP1,JP3,JP5–JP7,JP9–JP12	HTSW-150-07-G-S	HEADER 2_0	jmp2	Samtec
14	4	J1,J3,J5,J6	142-0701-801	sma_edge_uninstalled	sma_edge	EF Johnson
15	3	J2,J4,J7	142-0701-801	sma_edge	sma_edge	EF Johnson
16	4	P1–P4	108-0740-001	Banana-Jack	4mm	Emerson Network Power Connectivity Solutions
17	3	R1,R5,R9	311-0.0ARTR-ND	0 uninstalled	r0805	Panasonic
18	2	R2,R11	ERJ-6ENF1000V	100 uninstalled	r0805	Panasonic
19	2	R3,R10	CR0805-10W-1000FT	100 Ω	r0805	Venkel
20	2	R4,R15	ERJ-6ENF4530V	453 Ω uninstalled	r0805	Panasonic
21	3	R7,R13,R14	ERJ-6ENF4751V	4.7 kΩ	r0805	Panasonic - Ecg
22	1	R8	ERJ-6ENF49R9V	50 uninstalled	r0805	Panasonic
23	1	R12	311-0.0ARTR-ND	0 unistalled	r0805	Panasonic
24	1	U1	SN65MLVD3DRB	SN65MLVD3DRB	SON	TI
25	1	U2	SN65MLVD201D	SN65MLVD201D	SN75176	TI
26	2	Shunts	Place shunt in JP3, JP6, JP9, JP10, JP11, JP12 only	HTSW-150-07-G-S	0.1x0.1"	Samtek

4.2 Board Layout

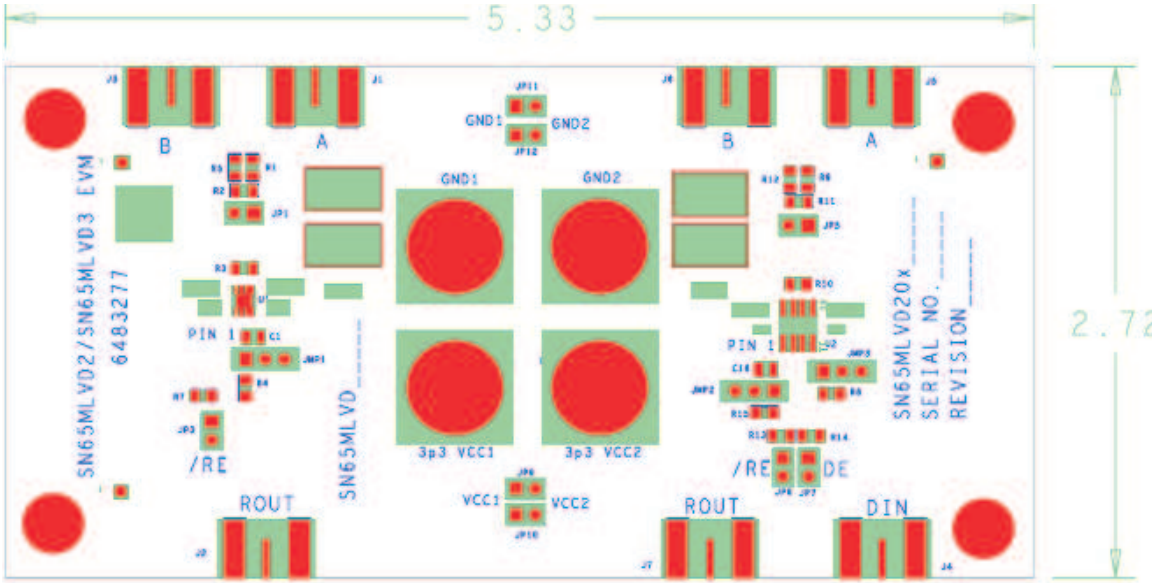


Figure 21. Assembly Drawing

The top layer of the EVM contains the controlled impedance and matched length traces.

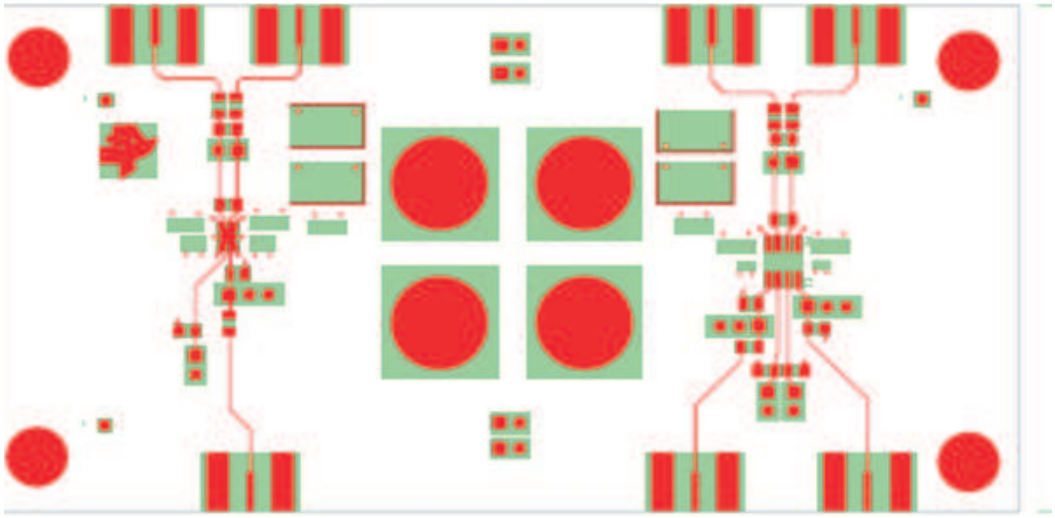


Figure 22. Top Layer

The second layer of the EVM has the separate ground planes. These are the reference planes for the controlled impedance traces on the top layer.

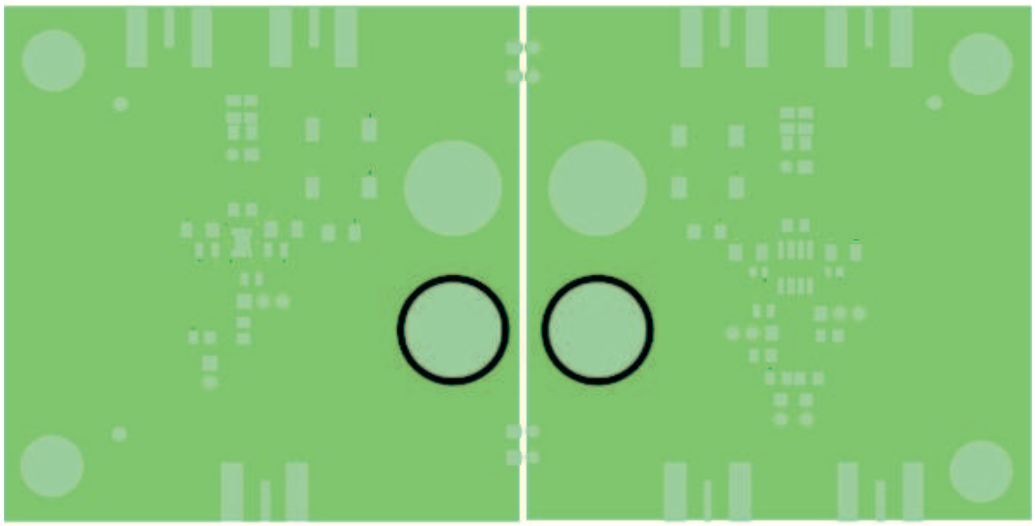


Figure 23. Second Layer

The third layer of the EVM has the power planes. These are matched to the ground planes to reduce radiated emission and crosstalk, while increasing distributed capacitance.

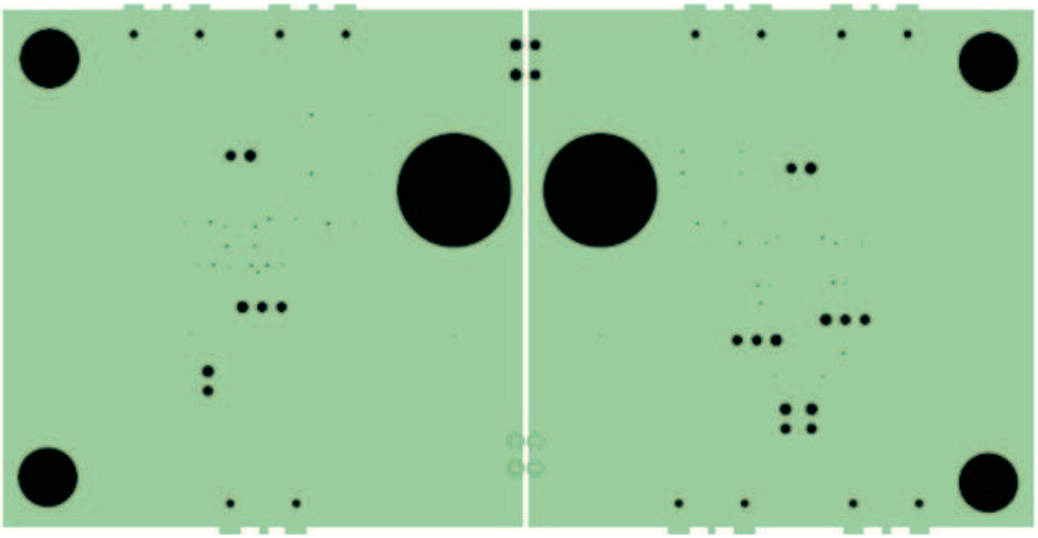


Figure 24. Third Layer

The bottom layer of the EVM contains bulk and decoupling capacitors to be placed close to the power and ground pins on the device. Not all decoupling capacitors have been installed on the EVM. However, the footprints have been provided in the layout so that additional capacitors can be installed for extra noise filtering for the application, if necessary.

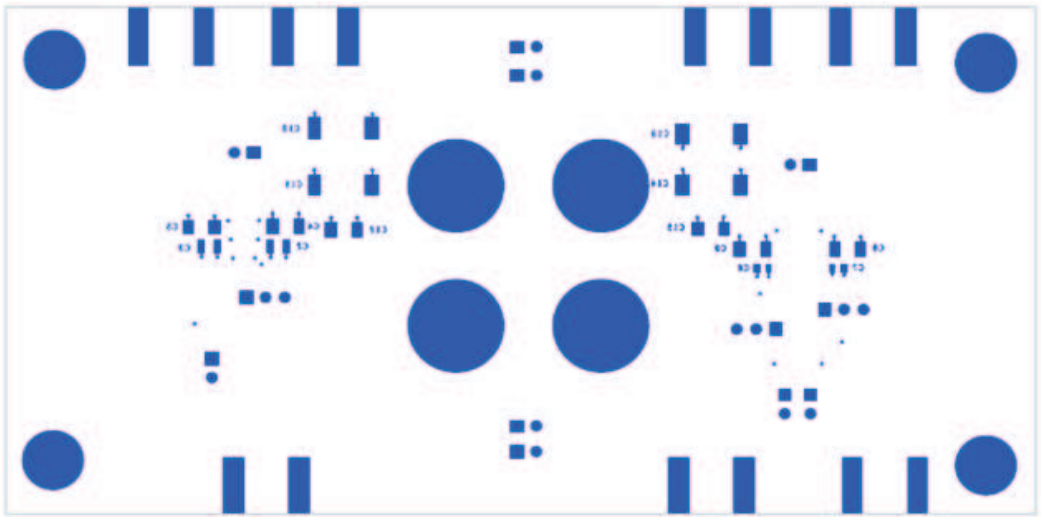


Figure 25. Bottom Layer

4.3 PCB Construction

Information in this section was obtained from the following source:

- *Electromagnetic Compatibility Printed Circuit Board and Electronic Module Design*, VEC workshop, Violette Engineering Corporation.

Characteristic impedance is the ratio of voltage to current in a transmission line wave traveling in one direction. This characteristic impedance is the value that is matched with our termination resistors so as to reduce reflections. This reduction in reflections improves signal to noise ratio on the line and reduces EMI caused by common mode voltages and spikes.

Two typical approaches are used for controlled impedance in printed-circuit board construction, microstrip and stripline. Microstrip construction is shown in Figure 26. The characteristic impedance of a microstrip trace on a printed-circuit board is approximated by:

$$Z_O = \frac{60}{\sqrt{0.475\epsilon r + 0.67}} \times \ln\frac{4h}{0.67(0.8\ W + t)} \quad (1)$$

where εr is the permeability of the board material, h is the distance between the ground plane and the signal trace, W is the trace width, and t is the thickness of the trace. The differential impedance for a two microstrip traces can be approximated as follows with S being the distance between two microstrip traces:

$$Z_{DIFF} = 2 \times Z_O \times \left(1 - 0.48e^{-0.96s/h}\right) \quad (2)$$

Stripline construction is also shown in Figure 3-6, the signal lines should be centered between the ground planes. The characteristic impedance of a stripline trace in a printed-circuit board is approximated by:

$$Z_O = \frac{60}{\sqrt{\epsilon r}} \times \ln\frac{4h}{0.67\pi(0.8\ W + t)} \quad (3)$$

where εr is the permeability of the board material, h is the distance between the ground plane and the signal trace, W is the trace width, and t is the thickness of the trace. The differential impedance for a two stripline traces can be approximated as follows with S being the distance between two stripline traces:

$$Z_{DIFF} = 2 \times Z_O \times \left(1 - 0.374e^{-2.9s/h}\right) \quad (4)$$

NOTE: For edge-coupled striplines, the term 0.374 may be replaced with 0.748 for lines which are closely coupled (S < 12 mils, or 0,3 mm).

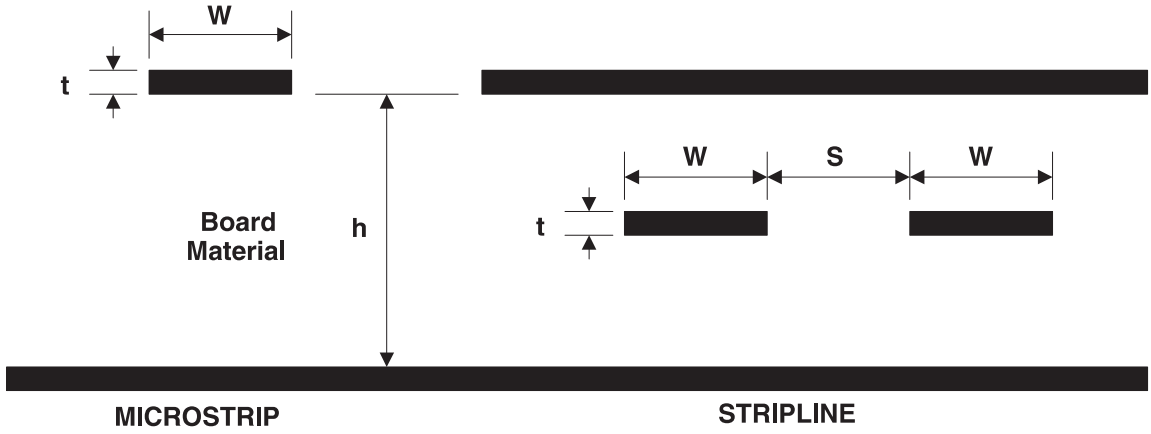


Figure 26. Trace Configurations in Printed-Circuit Boards

Stripline construction is the preferred configuration for differential signaling. This configuration reduces radiated emissions from circuit board traces due to better control of the lines of flux. The additional ground plane also allows for better control of impedance on the traces.

It can be seen from the functions and physical construction parameters that careful consideration must be given to these parameters for a robust board design. For instance it is not uncommon for εr to vary 10% across one board, affecting skew. This is a good reason to keep differential lines close. Other factors to keep in mind when doing a printed-circuit layout for transmission lines are as follows:

1. Differences in electrical length translate into skew.
2. Careful attention to dimensions, length and spacing help to insure isolation between differential pairs.
3. Where possible use *ideal interconnects*, point-to-point with no loads or branches. This keeps the impedance more uniform from end to end and reduce reflections on the line.
4. Discontinuities on the line, vias, pads, test points:
   - Reduce characteristic impedance
   - Increase the prop delay, and rise-time degradation
   - Increase signal transition time
5. Prioritize signals and avoid turns in critical signals. Turns can cause impedance discontinuities.
6. Within a pair of traces, the distance between the traces should be minimized to maintain common-mode rejection of the receivers. Differential transmission works best when both lines of the pair are kept as identical as possible.

Table 5 shows the layer stackup of the EVM with the defined trace widths for the controlled impedance etch runs using microstrip construction.

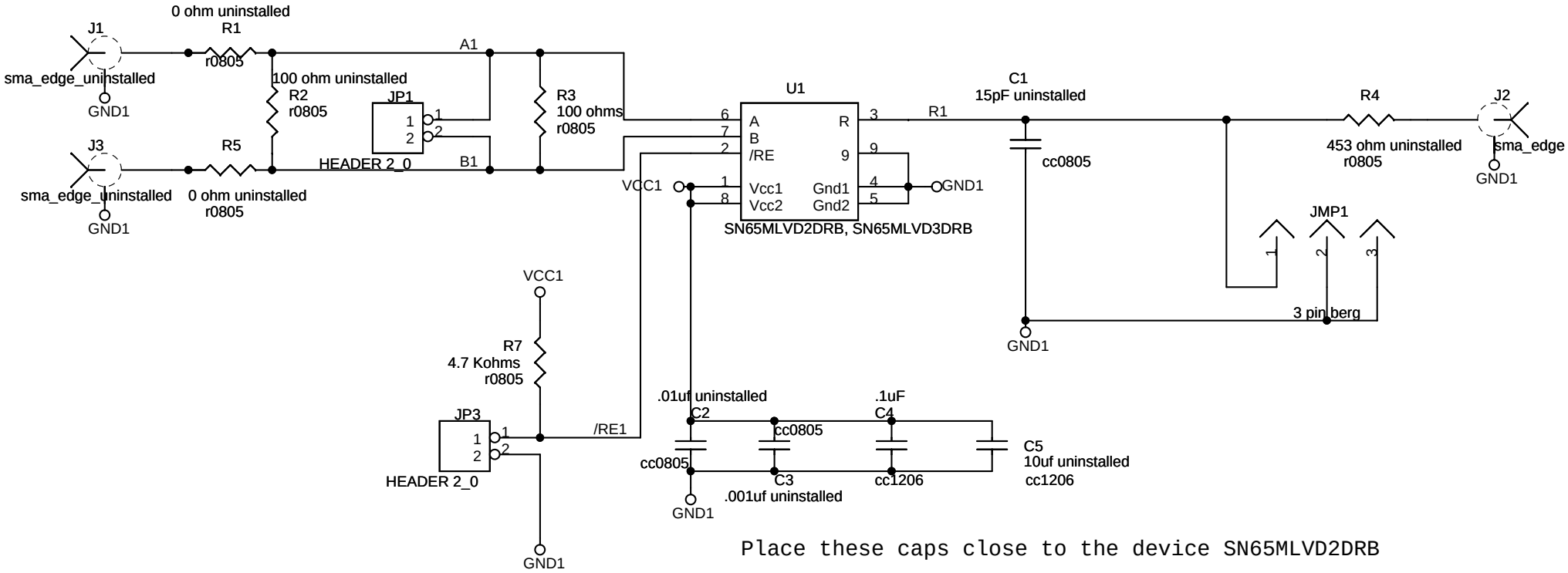
Table 5. EVM Layer Stackup

Layer No.	Material Type	Layer Type	Thickness (mils)	Copper Weight (oz)	Single-Ended Model	
					Line Width (mils)	Impedance (Ω)
1	COPPER	Signal	2.4	0.5 (start)	8	49.3
	FR4	Dielectric	4.5			
2	COPPER	Plane	1.2	1		
	FR4	Dielectric	4.5			
3	COPPER	Plane	1.2	1		
	FR4	Dielectric	4.5			
4	COPPER	Signal	2.4	0.5 (start)	8	49.3

Appendix A

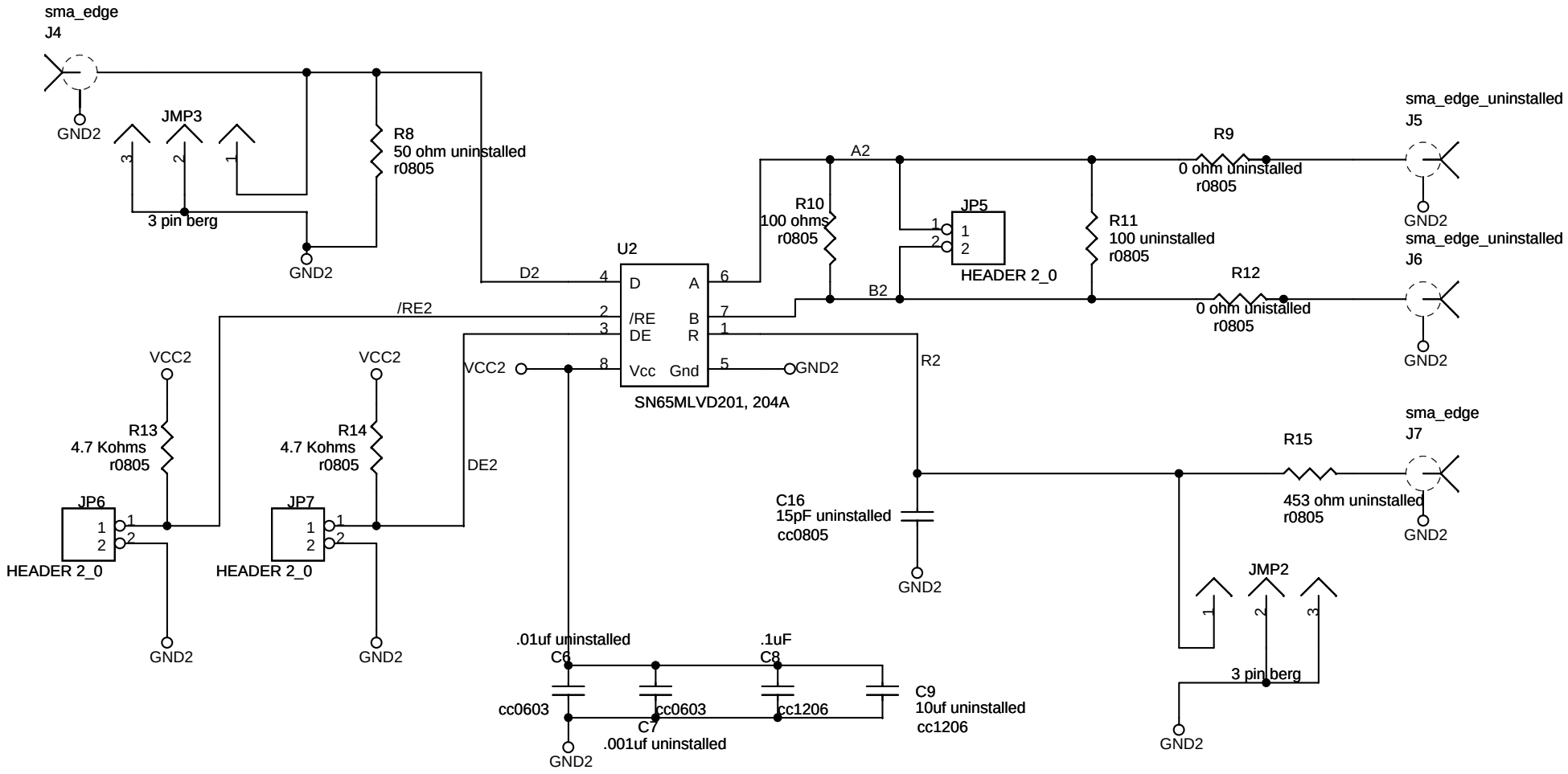
A.1 Schematic

This Appendix contains the EVM schematic.



Place these caps close to the device SN65MLVD2DRB

Title: SN65MLVD2 / SN65MLVD3 EVM Board		
Size: A	Document Number: 6483277	Rev: 12
Date: Friday, November 03, 2006	Sheet 1 of 3	



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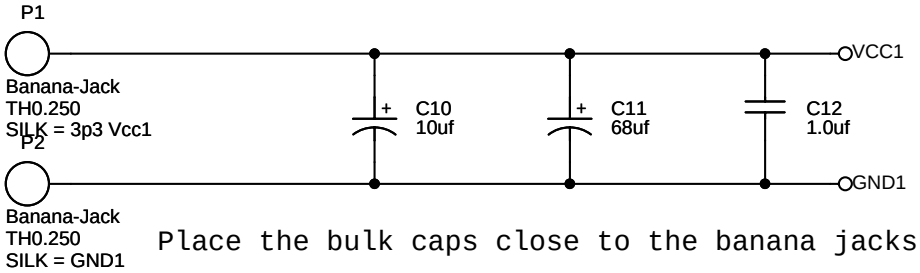
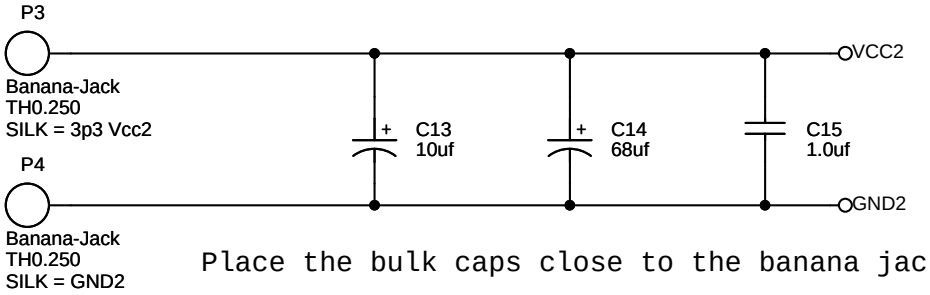
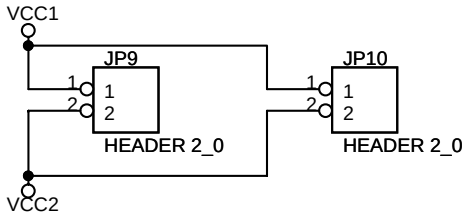
Date: Friday, November 03, 2006	Sheet 2 of 3	

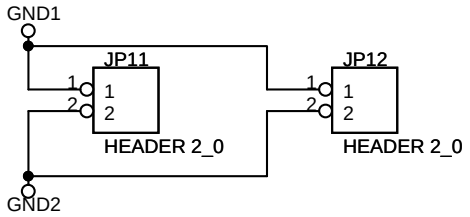


Place the bulk caps close to the banana jacks



Place the bulk caps close to the banana jacks





SN65MLVD2 / SN65MLVD3 EVM BOARD REVISION HISTORY

R10	Released initial design for review by team	KM	6/22/06
R11	Released initial design for review by team	KM	7/21/06
R12	Updated schematic with feedback from board design review which is documented on eDocs	KM	7/24/06

NOTES

1: Nets A & B should be matched and have an impedance of 50 ohms to gnd
2: Place net names on all jumpers and headers unless SILK specifies otherwise
3: Place TI logo on top side metal
4: Place board name, revision, and Edge number on top side silkscreen
5: All parts on 0 or 90 degree orientation
6: Use FR4 material
7: All receptacles must be placed as noted within the schematic
8: Mark pin 1 on SILK for orientation of device U1 & U2

Title: SN65MLVD2 / SN65MLVD3 EVM BOARD - Power		
Size: A	Document Number: 6483277	Rev: 12
Date: Tuesday, July 25, 2006	Sheet 3 of 3	

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 3.6 V and the output voltage range of 0 V to 3.6 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 37°C. The EVM is designed to operate properly with certain components above 37°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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