Functional Safety Information

TLC2272-Q1
Functional Safety FIT Rate, FMD and Pin FMA

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1 Overview

This document contains information for TLC2272-Q1 (SOIC (D) 8 and TSSOP (PW) 8 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

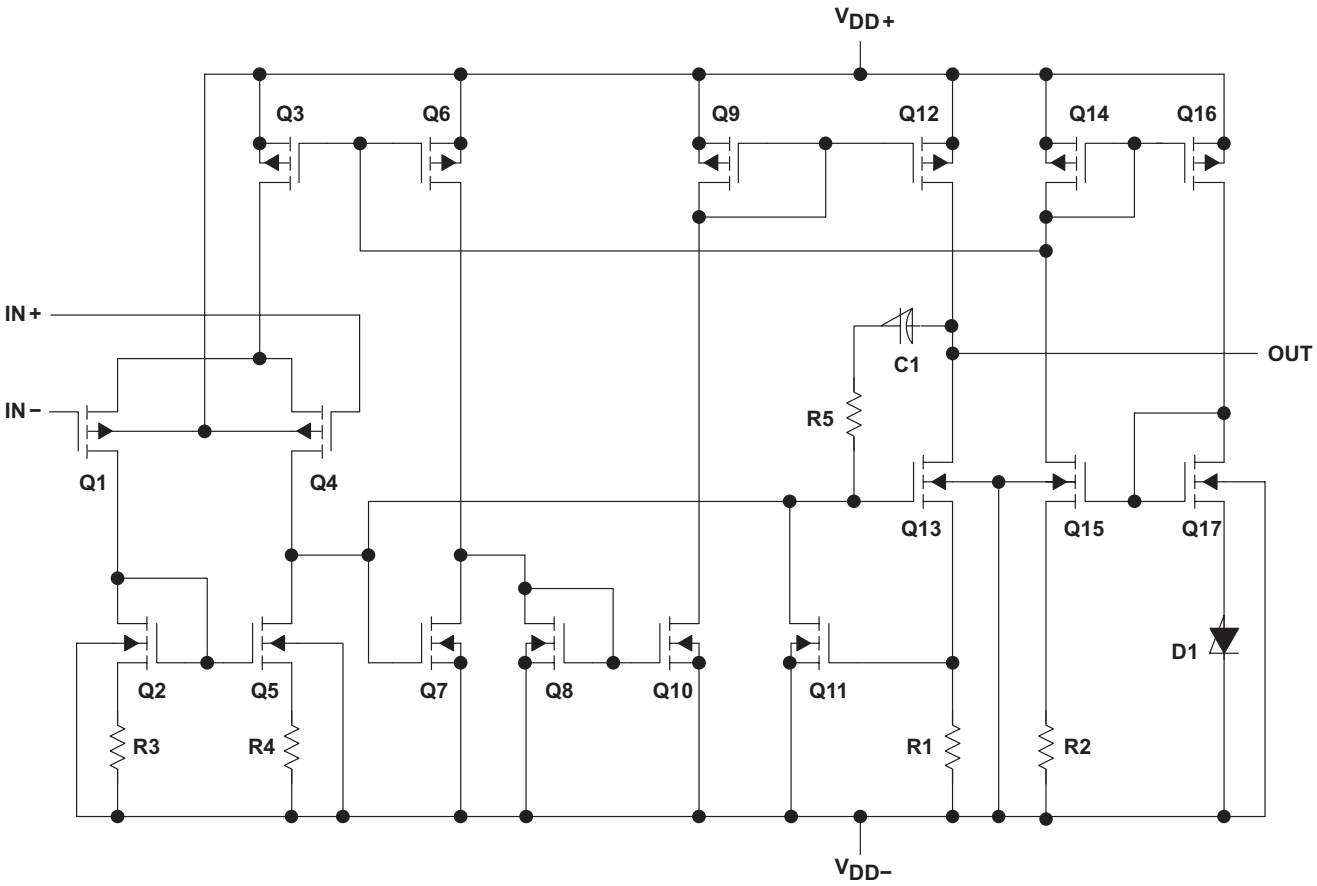

Figure 1-1. Functional Block Diagram

TLC2272-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

2.1 SOIC (D) 8 Package

This section provides Functional Safety Failure In Time (FIT) rates for SOIC (D) 8 package of TLC2272-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	47
Die FIT Rate	39
Package FIT Rate	8

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 848 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	4 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

2.2 TSSOP (PW) 8 Package

This section provides Functional Safety Failure In Time (FIT) rates for the TSSOP (PW) 8 package of TLC2272-Q1 based on two different industry-wide used reliability standards:

- Table 2-3 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-4 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-3. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	125
Die FIT Rate	116
Package FIT Rate	9

The failure rate and mission profile information in Table 2-3 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 848 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-4. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
5	CMOS, BICMOS Digital, analog / mixed	4 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-4 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for TLC2272-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
Output open (Hi-Z)	20%
Output saturated high	25%
Output saturated low	25%
Output functional, out of specification voltage or timing	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the TLC2272-Q1 (SOIC (D) 8 and TSSOP (PW) 8 package). The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6.)
- Pin open-circuited (seeTable 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to supply (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- *Short circuit to Supply or Power* means short to VDD+
- *Short to GND* means short to VDD–

4.1 SOIC (D) 8 Package

Figure 4-1 shows the TLC2272-Q1 pin diagram for the SOIC (D) 8 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLC2272-Q1 data sheet.

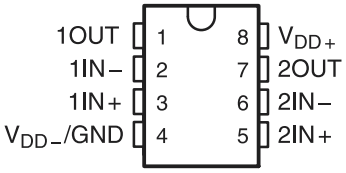

Figure 4-1. Pin Diagram (SOIC (D) 8) Package

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1OUT	1	Depending on circuit configuration, the device will likely be forced into a short-circuit condition with the 1OUT voltage ultimately forced to the VDD– voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
1IN–	2	Negative feedback not present to the device. Depending on the circuit configuration, the output will most likely move to the negative supply.	B
1IN+	3	Device common-mode; tied to negative rail. Depending on the circuit configuration, the output will likely not respond because of the device being put into an invalid common-mode condition.	C
2IN+	5	Device common-mode; tied to negative rail. Depending on the circuit configuration, the output will likely not respond because of the device being put in an invalid common-mode condition.	C
2IN–	6	Negative feedback not present to the device. Depending on the circuit configuration, the output will most likely move to the negative supply.	B
2OUT	7	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the 2OUT voltage ultimately forced to the VDD– voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
VDD+	8	Op-amp supplies will be shorted together, leaving the VDD+ pin at some voltage between the VDD+ and VDD– sources (depending on source impedance).	A

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1OUT	1	No negative feedback or ability for 1OUT to drive the application.	B
1IN–	2	Inverting pin of the op amp; left floating. Negative feedback will not be provided to the device, likely resulting in the device output moving between the positive and negative rails. The 1IN– pin voltage will likely end up at the positive or negative rail because of leakage on the ESD diodes.	B
1IN+	3	Input common-mode; left floating. The op amp will not be provided with common-mode bias, and the device output will likely end up at the positive or negative rail. The 1IN+ pin voltage will likely end up at the positive or negative rail because of leakage on the ESD diodes.	B
VDD–	4	Negative supply; left floating. The op amp ceases to function because no current can source or sink to the device.	B
2IN+	5	Input common-mode; left floating. The op amp will not be provided with common-mode bias, and the device output will likely end up at the positive or negative rail. The 2IN+ pin voltage will likely end up at the positive or negative rail because of leakage on the ESD diodes.	B
2IN–	6	Inverting pin of the op amp; left floating. Negative feedback will not be provided to the device, likely resulting in the device output moving between the positive and negative rails. The 2IN– pin voltage will likely end up at the positive or negative rail because of leakage on the ESD diodes.	B
2OUT	7	No negative feedback or ability for 2OUT to drive the application.	B
VDD+	8	Positive supply; left floating. The op amp ceases to function because no current can source or sink to the device.	A

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
1OUT	1	2	Depending on the circuit configuration, the circuit gain will be reduced to unity gain, and the application may not function as intended.	B
1IN–	2	3	Both inputs will be tied together. Depending on the offset of the device, this will likely move the output voltage to near mid-supply.	D
1IN+	3	4	Device common-mode; tied to negative rail. Depending on the circuit configuration, the output will likely not respond because of the device being put into an invalid common-mode condition.	C
VDD–	4	5	Device common-mode; tied to negative rail. Depending on the circuit configuration, the output will likely not respond because of the device being put into an invalid common-mode condition.	C
2IN+	5	6	Both inputs will be tied together. Depending on the offset of the device, this configuration will likely move the output voltage to near mid-supply.	D
2IN–	6	7	Depending on the circuit configuration, the circuit gain will be reduced to unity gain and the application may not function as intended.	B
2OUT	7	8	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the 2OUT voltage ultimately forced to the VDD+ voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
VDD+	8	1	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the VDD+ voltage ultimately forced to the 1OUT voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A

Table 4-5. Pin FMA for Device Pins Short-Circuited to Supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1OUT	1	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the 1OUT voltage ultimately forced to the VDD+ voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
1IN–	2	Negative feedback not present to the device. Depending on the noninverting input voltage and circuit configuration, the output will most likely move to the negative supply.	B
1IN+	3	Depending on the circuit configuration, the application will likely not function because of the device common-mode being connected to 1IN+.	B
VDD–	4	Op-amp supplies will be shorted together, leaving the VDD– pin at some voltage between the VDD– and VDD+ sources (depending on source impedance).	A
2IN+	5	Depending on the circuit configuration, the application will likely not function because of the device common-mode being connected to 2IN+.	B
2IN–	6	Negative feedback not present to the device. Depending on the noninverting input voltage and circuit configuration, the output will most likely move to the negative supply.	B
2OUT	7	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the 2OUT voltage ultimately forced to the VDD+ voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A

4.2 TSSOP (PW) 8 Package

Figure 4-2 shows the TLC2272-Q1 pin diagram for the TSSOP (PW) 8 package. For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the TLC2272-Q1 data sheet.

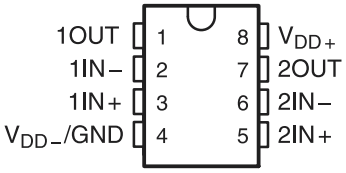

Figure 4-2. Pin Diagram (TSSOP (PW) 8 Package)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1OUT	1	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the 1OUT voltage ultimately forced to the VDD– voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
1IN–	2	Negative feedback not present to the device. Depending on the circuit configuration, the output will most likely move to the negative supply.	B
1IN+	3	Device common-mode; tied to the negative rail. Depending on the circuit configuration, the output will likely not respond because of the device being put into an invalid common-mode condition.	C
2IN+	5	Device common-mode; tied to the negative rail. Depending on the circuit configuration, the output will likely not respond because of the device being put into an invalid common-mode condition.	C
2IN–	6	Negative feedback not present to the device. Depending on the circuit configuration, the output will most likely move to the negative supply.	B
2OUT	7	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the 2OUT voltage ultimately forced to the VDD– voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
VDD+	8	Op-amp supplies will be shorted together, leaving the VDD+ pin at some voltage between the VDD+ and VDD– sources (depending on source impedance).	A

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1OUT	1	No negative feedback or ability for 1OUT to drive application.	B
1IN–	2	Inverting pin o the op amp; left floating. Negative feedback will not be provided to the device, likely resulting in the device output moving between the positive and negative rails. The 1IN– pin voltage will likely end up at the positive or negative rail because of leakage on the ESD diodes.	B
1IN+	3	Input common-mode; left floating. The op amp will not be provided with common–mode bias, and the device output will likely end up at the positive or negative rail. The 1IN+ pin voltage will likely end up at the positive or negative rail because of leakage on the ESD diodes.	B
VDD–	4	Negative supply; left floating. The op amp ceases to function because no current can source or sink to the device.	B
2IN+	5	Input common-mode; left floating. The op amp will not be provided with common–mode bias, and the device output will likely end up at the positive or negative rail. the 2IN+ pin voltage will likely end up at the positive or negative rail because of leakage on the ESD diodes.	B
2IN–	6	Inverting pin of the op amp; left floating. Negative feedback will not be provided to the device, likely resulting in the device output moving between the positive and negative rails. The 2IN– pin voltage will likely end up at the positive or negative rail because of leakage on the ESD diodes.	B
2OUT	7	No negative feedback or ability for 2OUT to drive the application.	B
VDD+	8	Positive supply; left floating. The op amp ceases to function because no current can source or sink to the device.	A

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
1OUT	1	2	Depending on the circuit configuration, the circuit gain will be reduced to unity gain, and the application may not function as intended.	B
1IN–	2	3	Both inputs will be tied together. Depending on the offset of the device, this configuration will likely move the output voltage to near mid-supply.	D
1IN+	3	4	Device common-mode; tied to the negative rail. Depending on the circuit configuration, the output will likely not respond because of the device being put into an invalid common-mode condition.	C
VDD–	4	5	Device common-mode; tied to the negative rail. Depending on the circuit configuration, the output will likely not respond because of the device being put into an invalid common-mode condition.	C
2IN+	5	6	Both inputs will be tied together. Depending on the offset of the device, this configuration will likely move the output voltage to near mid-supply.	D
2IN–	6	7	Depending on the circuit configuration, the circuit gain will be reduced to unity gain, and the application may not function as intended.	B
2OUT	7	8	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the 2OUT voltage ultimately forced to the VDD+ voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
VDD+	8	1	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the VDD+ voltage ultimately forced to the 1OUT voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A

Table 4-9. Pin FMA for Device Pins Short-Circuited to supply

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
1OUT	1	Depending on the circuit configuration, the device will likely be forced into a short-circuit condition, with the 1OUT voltage ultimately forced to the VDD+ voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A
1IN-	2	Negative feedback not present to device. Depending on the noninverting input voltage and circuit configuration, the output will most likely move to the negative supply.	B
1IN+	3	Depending on the circuit configuration, the application will likely not function because of the device common-mode being connected to 1IN+.	B
VDD-	4	Op-amp supplies will be shorted together, leaving the VDD– pin at some voltage between the VDD– and VDD+ sources (depending on source impedance).	A
2IN+	5	Depending on the circuit configuration, the application will likely not function because of the device common-mode being connected to 2IN+.	B
2IN-	6	Negative feedback not present to device. Depending on the noninverting input voltage and circuit configuration, the output will most likely move to the negative supply.	B
2OUT	7	Depending on thecircuit configuration, the device will likely be forced into a short-circuit condition, with the 2OUT voltage ultimately forced to the VDD+ voltage. Prolonged exposure to short-circuit conditions could result in long-term reliability issues.	A

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2021) to Revision A (April 2022)	Page
• Changed Table 3-1 to show correct information	5

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265