Application Report

TPS62933 Thermal Performance with SOT583 Package

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ABSTRACT

Thermal design is very important for small outline transistor (SOT) packages. This application report compares the thermal performance of TPS62933 where the package is flip-chip on lead (FCOL) SOT583 with TPS54335A where the package is conventional wire-bond SO Power PAD (8) and TPS56339 and has FCOL SOT23(-6) package. The results show that TPS62933 has the best thermal performance using the small R_{DSon}.

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Trademarks

1 Introduction

Small outline transistor (SOT) packages are widely used due to their low cost and low profile, the SOT23 is one of the most widely used SOT packages. But today more DC/DCs are using the SOT5x3 packages, whose size is even smaller than that of the SOT23 package. Due to the limit size, bonding wire technology is not recommended to use in SOT5x3 package and thus it does not have a thermal PAD. As a result, improving the thermal performance for chips with SOT5x3 package both in the IC design phase and the PCB layout design phase is necessary.

Bonding wire and FCOL have different ways to connect the die with the package. This paper shows the differences between two bump methods, and introduces a general rule for SOT5x3 package layout and gives an example of TI suggested layout. Finally, based on the layout analysis, this paper compares the thermal performance of FCOL SOT5x3 package with FCOL SOT23 package and bonding wore SO Power PAD package.

2 Bonding Wire Package Introduction

There are 500 to 1,200 chips, which are also called dies, being attached to each sheet of wafers that have completed the front-end process. A dicing process will divide the chips into individual and use wires to connect the chip with the outside so that each chip can be used for the required field. Bonding wire is a method of bonding thin metal wires to a pad, as a technology that connects the internal die and the outside.

As shown in Figure 2-1, the chip fastens on the middle of the lead frame with glue. Wires act as a bridge between the bonding pad of the chip (first bond) and the pad of the carrier (second bond). The material of the wire is copper or gold, the length is from several hundred μm to several mm and the diameter is typically 15 to 35 μm. The total R_{DSon} is the R_{DSon} of the die plus the bonding wire's resistor. For a high-current converter, the resistor of the bonding wire significantly increases the total R_{DSon} of the device, meaning to keep the total R_{DSon} smaller, you must increase the die size to decrease the die R_{DSon}. The bonding wire will also increase the parasitic inductance between Vin, SW pin to Vin, and the SW pad on the die. It will decrease the SW ringing slew rate because of higher parasitic inductance, which is bad for efficiency.

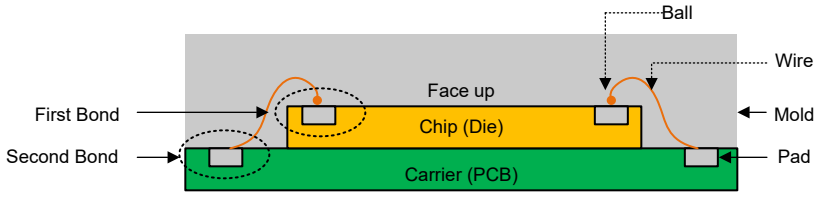

Figure 2-1. Simplified Structure of Bonding Wire Package.

To improve the thermal performance, the Power PAD can be added so that the leadframe die pad (or thermal pad) is exposed on the bottom of the IC. This provides an extremely low thermal resistance path between the die and the exterior of the package. The thermal pad on the bottom of the IC can then be soldered directly to the printed circuit board (PCB), using the PCB as a heatsink. In addition, through the use of thermal vias, the thermal pad can be directly connected to a ground plane or special heat sink structure designed into the PCB.

3 Flip Ship on Lead Package Introduction

Flip chip assembly is the direct electrical connection of face-down (hence, *flipped*) electronic components onto substrates, circuit boards, or other components, by means of conductive bumps on the chip bond pads. While in contrast, bonding wire uses face-up chips with an individual wire connected to each bond pad. Figure 3-1 is a conceptual view of a flip chip and substrate.

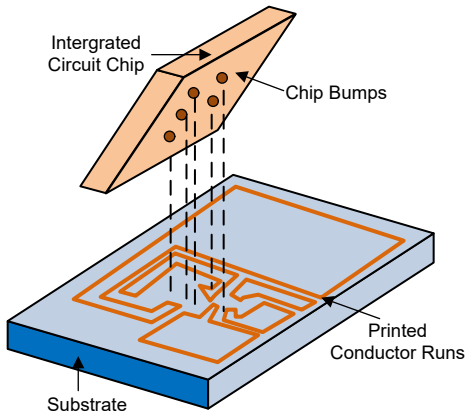

Figure 3-1. Simplified Structure of Flip Chip on Lead Package

The continuing boom in flip chip packaging results from flip chip's advantages in size, performance, flexibility, reliability, and cost over other microelectronic assembly methods:

1. Smallest Size – Eliminating bond wires and cumbersome individual packages reduces the required board area per chip by up to 95% and the height by more than 50%. Weight can be less than 5% of the packaged device weight. Flip chip is the simplest minimal package, smallest because it is very close to chip size.
2. Highest Performance – Because of its small size, flip chip offers the highest speed electrical performance of any assembly method. Eliminating bond wires reduces the delaying inductance and capacitance of the connection by a factor of 10, and shortens the signal path by a factor of 25 to 100. The result is high speed off-chip interconnection.
3. Greatest Connection Flexibility – Flip chip gives the greatest input/output connection flexibility. Wire bond connections are limited to the perimeter of the die, driving die sizes up as the number of connections increases. Flip chip connections can use the whole area of the die, accommodating many more connections on a smaller die, and placing them most efficiently. Area connections also allow 3-D stacking of die and other components.
4. Most Rugged – Flip chip is mechanically the most rugged interconnection method. Flip chips, when completed with an adhesive *underfill*, are solid little blocks of cured epoxy. They have survived laboratory tests simulating the forces of rocket liftoff and of artillery firing, as well as millions of cumulative total hours of actual use in computers and under automobile hoods.
5. Lowest Cost – Flip chip can be the lowest cost interconnection for high volume automated production, with costs of a fraction of a cent per connection. This explains flip chip's longevity in the cost-conscious automotive world, and growing popularity in smart cards, RFID cards, cellular telephones, and other cost-dominated applications.

4 SOT 583 Package Layout Guideline

TPS62933 uses FCOL SOT583 package whose size is 1.6mm×2.1mm. It is rather small and doesn't have a thermal pad. In order to improve the thermal performance, on time resistor of the FET is designed to have a small value, so that the power loss of the chip can be reduced. Also, PCB design should be optimized to achieve good thermal dissipation.

A 4-layer PCB is helpful for thermal dispassion, TI's SOT583 solution can support a 2-layer application, TI's EVMs use a 2-layer PCB. The typical application circuit of the TPS62933 device is shown in Figure 4-1 and a layout image is provided in Figure 4-2 and Figure 4-3.

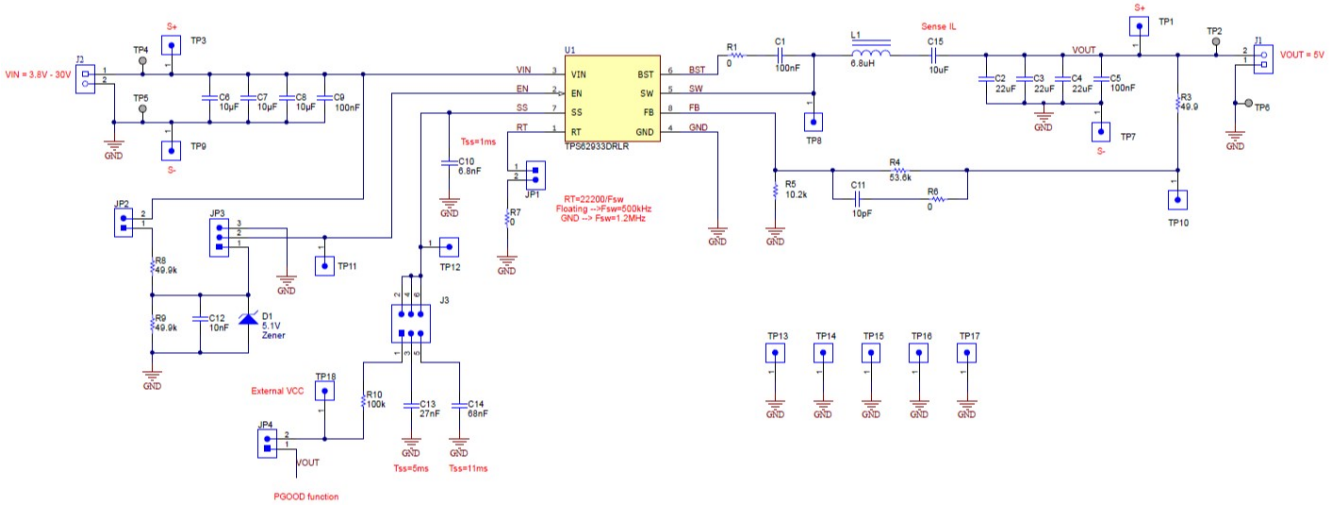

Figure 4-1. Typical Application Circuit of TPS62933 Device

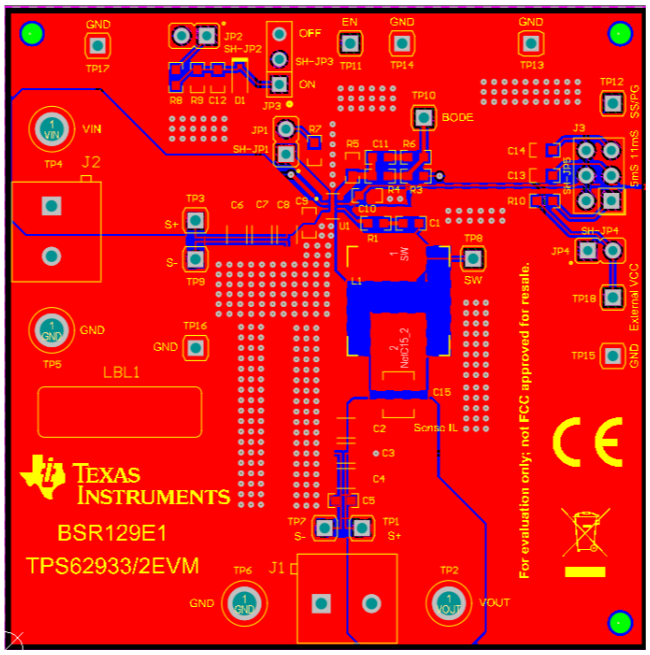

Figure 4-2. Top Layer of TPS62933 EVM

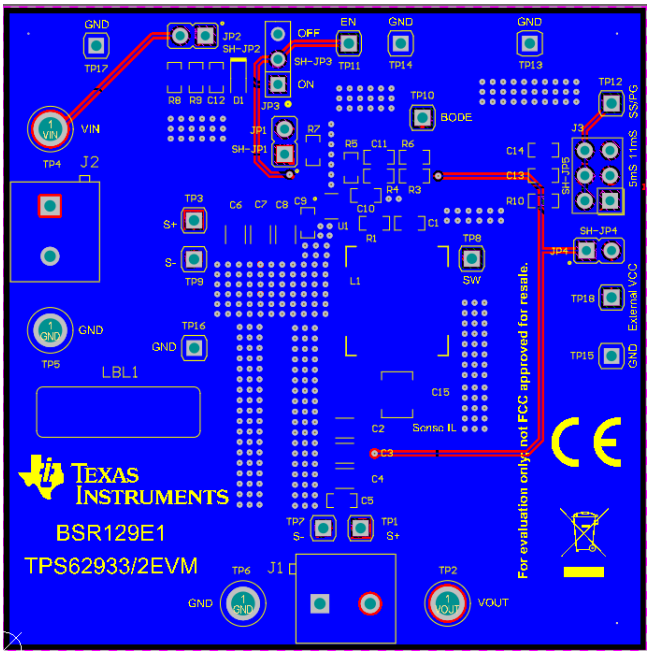

Figure 4-3. Bottom Layer of TPS62933 EVM

The layout in Figure 4-2 and Figure 4-3 is for reference. In some PCB designs, the top and bottom layer may not have so much space. In those cases, IC pins can be connected with vias to copper planes in the inner layers. It is important to realize that in FCOL packages, all IC pins are potential heat conductors and good a thermal connection to PCB copper planes can enhance the thermal cooling effect.

The following list, provides the layout priority:

- VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas provide better heat dissipation.
- The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
- Provide sufficient vias for the input capacitor and output capacitor.
- Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
- Do not allow switching current to flow under the device.
- A separate VOUT path should be connected to the upper feedback resistor.
- Make a Kelvin connection to the GND pin for the feedback path.
- The voltage feedback loop should be placed away from the high-voltage switching trace, and would preferably have a ground shield.
- The trace of the VFB node should be as small as possible to avoid noise coupling.
- The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

For a 4-layer PCB, put your signal wire at layer 2 or layer 3, make sure the bottom layer GND does not separate by the line, this will increase thermal dissipation. Also, add more GND via to make all GND in each layer connect together. TI suggests pouring GND polygon for the top layer and the bottom layer.

5 Thermal Performance

TPS54335A, TPS56339 and TPS62933 can all be applied in 19V/5V case. TPS54335A uses wire bonding SO Power PAD 8 package, its synchronous MOSFETs' R_{DSon}s are 128mΩ and 84mΩ which are not that small and will do harm to the thermal performance. The thermal PAD can help a lot with the cooling. But TPS54335A is vulnerable to its big size which is 4.89mm×3.9mm.

TPS56339 uses FCOL SOT236 package whose size is 1.6mm×2.9mm which is much smaller than SOP 8 package. Although it does not have a thermal PAD due to the limited size and flip chip package, it's R_{DSon} of the high side FET and low side FET is 70mΩ and 35mΩ respectively which is much smaller than that of TPS54335A.

TPS62933, as is mentioned before, whose size is the smallest. Its synchronous MOSFETs' R_{DSon} is 80mΩ and 32mΩ respectively. The R_{DSon} of the low side FET is smaller than that of TPS56339, which will do good to the thermal performance since the low side MOSFET turns on much longer than the high side MOSFET in low duty cycle cases.

To figure out the thermal performance of the three parts mentioned above, thermal scans are shown in Figure 5-1, Figure 5-2 and Figure 5-3 respectively in the test condition listed in Table 5-1.

Table 5-1. Test Conditions

	TPS62933	TPS56339	TPS54335A
	FCOL SOT583	FCOL SOT263	Bonding wire SOP8
V_{in}	19V	19V	19V
V_{out}	5V	5V	5V
I_{out}	3A	3A	3A
Frequency	500kHz	500kHz	500kHz
Inductor	6.8μH	6.8μH	6.8μH
Size of PCB	65mm×65mm	65mm×65mm	63mm×63mm
Total numbers of layers	2	2	2
Width of copper	2oz	2oz	2oz

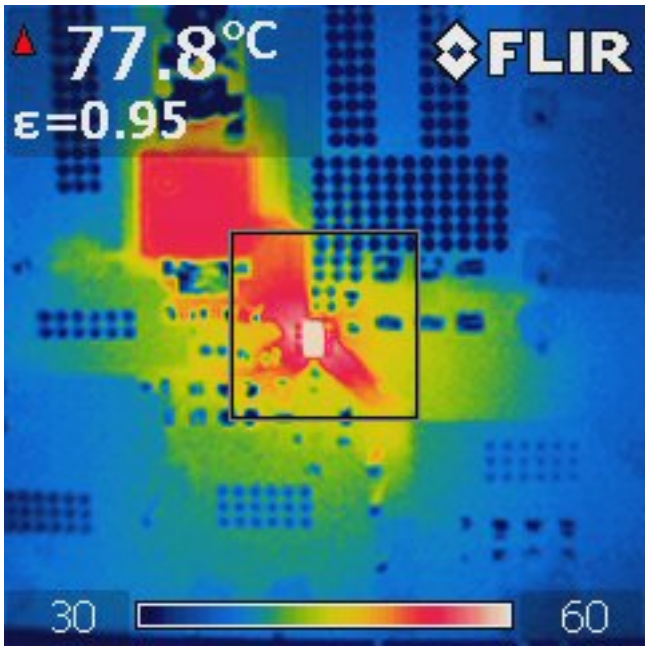

Figure 5-1. Thermal Scan of TPS62933 EVM

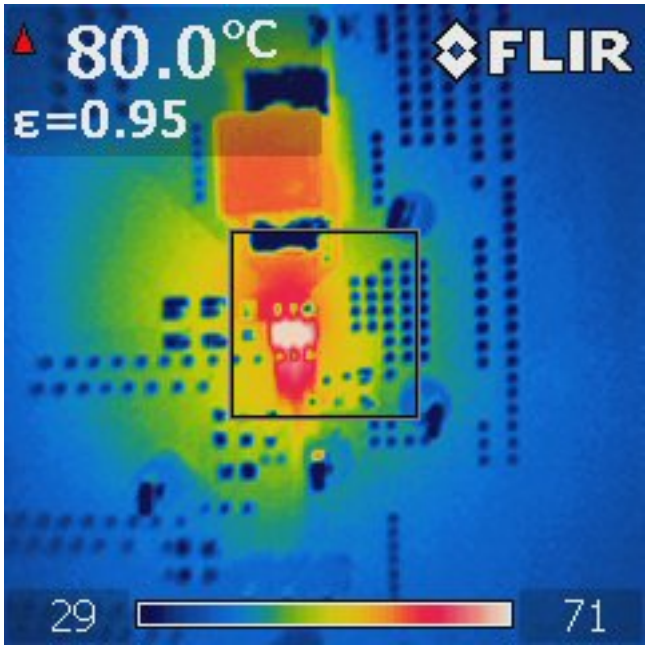

Figure 5-2. Thermal Scan of TPS56339 EVM

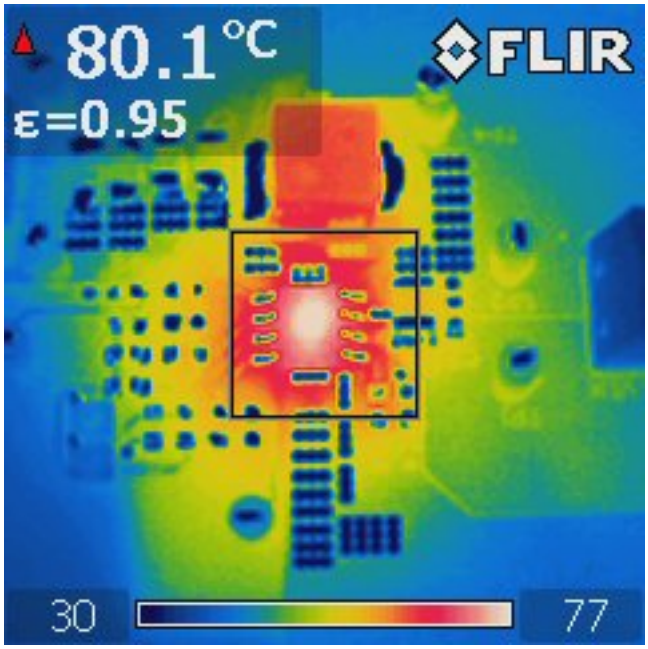

Figure 5-3. Thermal scan of TPS54335A EVM.

All ICs were mounted on the similar size evaluation board whose information is listed in table2. The layout was optimized for good thermal performance based on guidelines mentioned in Section 4. The bonding wire SOP8 shows the highest temperature and FCOL SOT23 shares a similar performance. The FCOL SOT583 package hotspot is 3°C cooler than the bonding wire SOP8 and FCOL SOT236. This is benefit from the low R_{DSon} of the low side MOSFET.

$R_{\theta JA}$ is the thermal resistance of the junction to the environment in still air conditions and is the most common thermal parameter for the semiconductor package. In most cases, the total heat of the device is eventually distributed into the air, so the air temperature is easy to measure or pre-determined and the junction temperature can be easily estimated with $R_{\theta JA}$ as long as the power consumption is known. The equation usually assumed to be valid for calculating junction temperature from $R_{\theta JA}$ is Equation 1 .

$$R_{\theta JA} = \frac{T_J - T_A}{P_T} \quad (1)$$

Where, P_T is the total chip dissipated power, T_J is the temperature of the junction and T_A is the ambient temperature.

Table 5-2 gives the thermal resistance based on EVM layout. From the test result the TPS62933 has the lowest thermal performance at full loading conditions.

Table 5-2. Thermal Results of Different Parts

	TPS62933	TPS56339	TPS54335A
	FCOL SOT583	FCOL SOT263	Bonding wire SOP8
T_A	27.7°C	27.7°C	27.7°C
T_J	79.1°C	88°C	93.4°C
P_J	0.816W	0.85W	1.66W
$R_{\theta JA}$	62.99°C/W	70.89°C/W	39.51°C/W

6 Summary

FCOL packages have some electrical and thermal advantages. In FCOL packages, each pin has a good thermal connection to the silicon die. The PCB layout can be optimized to let each pin conduct more heat from die to PCB, which can lower the overall thermal resistance from junction to ambient.

Even TPS62933 with FCOL SOT5x3 package has a smaller size than that with FCOL SOT23 package, the R_{DSon} can be designed smaller especially the low side FET R_{DSon} can help get better thermal performance. TI's EVMs provides a good example for the customer to do layout for an SOT5x3 package.

7 References

- Texas Instruments, *TPS5433xA 4.5-V to 28-V Input, 3-A Output, Synchronous Step-Down DC-DC Converter* data sheet.
- Texas Instruments, *TPS56339 4.5-V to 24-V Input, 3-A Output Synchronous Buck Converter* data sheet.

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