Closing the Feedback Loop

by Lloyd H. Dixon, Jr

Topic 2

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Switching power supplies almost always use closed-loop negative feedback systems in order to achieve design objectives for line and load regulation and dynamic response. As shown in Figure 1, the closed loop can be described in terms of these major elements:

	Reference and comparator
G1(s):	Error amplifier and compensation networks
G2(s):	Pulse width modulator and power switching circuit
$H_e(s)$:	Output power filter

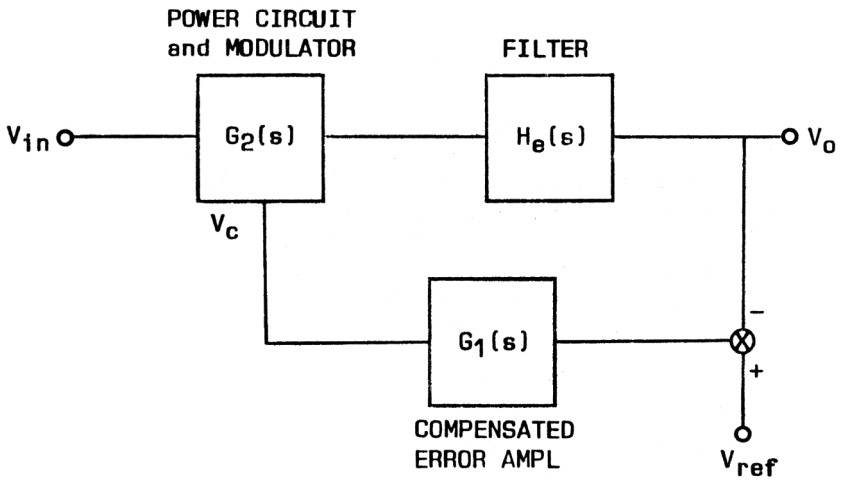

Figure 1. Control loop block diagram

Fortunately, these closed-loop control systems can be stabilized using simple analytical techniques. Unity gain crossover occurs only once in the gain vs. frequency characteristic, permitting the use of a simplified version of the Nyquist stability criterion. Bode plots provide a simple and powerful method of displaying and calculating the loop gain parameters (see Appendix B).

The switching frequency, f_c, the gain-frequency characteristics of the pulse width modulator and power switching circuit, G2(s), and the filter, $H_e(s)$, are predetermined by the application and the choice of circuit topology. The task in closing the feedback loop is to define the characteristic of the error amplifier and related compensation networks, G1(s), that will result in the optimum closed loop gain-bandwidth for good dynamic response, line and load regulation and stability.

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CLOSED LOOP DESIGN PROCEDURE

(1) Define the Goal: Make a Bode plot of the desired closed-loop characteristic that will achieve the best possible gain-bandwidth for good dynamic response, line and load regulation and stability.

(2) Define the Control to Output Gain: Decide upon the control method. Make a Bode plot of G2(s), the gain characteristic of the pulse width modulator and power switch, and $H_e(s)$, the filter.

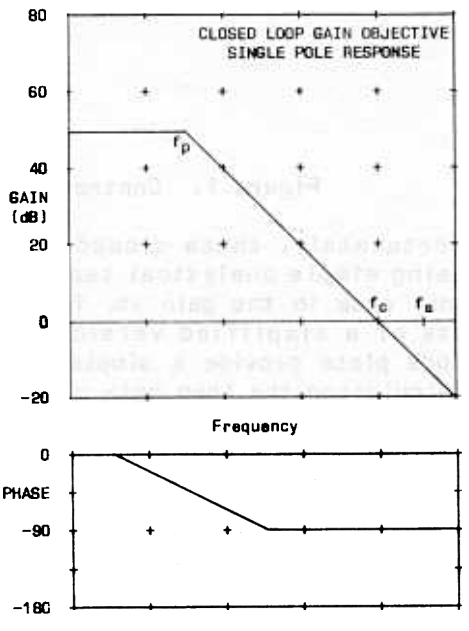
(3) Design the Compensation Network: Subtract the gain(dB) and phase plotted in (2) above from (1). The result is the G1(s) characteristic necessary to attain the closed loop objective.

DEFINE THE GOAL

Stability Criterion: Referring to Figure 2, if the gain magnitude crosses unity (0 dB) only once, the system is stable if the phase lag at the crossover frequency, f_c, is less than 180 degrees (in addition to the normal 180 degree phase shift of the negative feedback system). At other frequencies, the phase lag may exceed 180 degrees and the system will still be stable.

The 'phase margin' is the amount by which the phase lag at the crossover frequency, f_c, is less than 180 degrees. The 'gain margin' is the factor by which the gain is less than unity (0 dB) at the frequency where the phase lag is 180 degrees. If the phase lag at f_c is only slightly less than 180 degrees (small phase margin), the system will be stable, but will exhibit condsiderable overshoot and ringing. A phase margin of 45 degrees provides for good response with very little overshoot.

Nyquist's stability criterion permits the phase lag to exceed 180 degrees at frequencies below f_c where the gain is greater than 0 dB, but this is not a good practice. The system will be conditionally stable, but if the loop gain decreases it becomes unstable. That is exactly what happens when the system runs into large signal bounds, as with large step changes in load. The system will then oscillate or have severe underdamped ringing.



Figure

Short Cut Stabilization Method: It is easy to achieve good loop stability by using a dominant low frequency pole to roll the loop gain off at a very low frequency. Unity gain cross over must occur substantially below the output filter pole frequency to avoid

the additonal phase lag it introduces. The result of this short cut stabilization method is poor dynamic response.

Closed Loop Objective: The goal in designing the stabilization network is to optimize line and load regulation and dynamic response by providing high loop gain out to high frequencies. Phase lag must not approach within 45 degrees of 180 at f_C and all lower frequencies to avoid oscillations, ringing and instability. Stability analysis must be made at circuit operating extremes.

A practical goal for the closed loop characteristic is that of a net single pole as shown in Figure 2. The resulting high gain at low frequency provides good DC regulation. Gain falls off linearly at -20 dB/decade with 90 degree phase lag until well above f_C. High f_C provides good small signal dynamic response.

Maximum Crossover Frequency: (1) Sampling theory shows it is not possible to transmit information at any frequency greater than 1/2 the sampling frequency (which is the switching frequency, $f_S/2$). (2) The system becomes unstable when f_C exceeds $f_S/(2\pi D)$ with duty cycle, D, greater than 0.5.[1] At $f_C = f_S/(2\pi D)$, system response is maximally fast. (3) At $f_C = f_S/(2\pi D)$ the error amplifier gain may be high enough to cause the amplified output ripple voltage to drive the error amplifier into saturation, necessitating a further reduction in f_C.

In the examples given in Appendix C, a crossover frequency $f_C = f_S/4$ is attempted, but not always attained because of right-half-plane zeros or insufficient error amplifier gain-bandwidth.

DEFINE THE CONTROL TO OUTPUT GAIN

The control to output gain, or transfer characteristic, is the combined gain and phase vs. frequency characteristics of the PWM and switching circuit, G2(s), plus the output filter, He(s). The PWM, switching circuit and filter are fundamental to the design of the switching power supply. These elements are usually designed well before the process of closing the loop is started.

Because the control to output gain is part of the total loop, it is necessary to make a Bode plot of the control to output gain in order to know how to design the remainder of the loop -- the error amplifier and compensation network. This task is facilitated by the equations given in Appendix C for each PWM-switching topology combination. These equations translate the previously defined physical parameters of the PWM and switching circuit into gain and phase vs. frequency for the Bode plots.

Control method: The mode of operation of the pulse width modulator has a great effect upon the performance of the closed loop system and the design of the compensation networks. This discussion considers only PWM methods that run at fixed frequency, which all function on the basis of a comparator

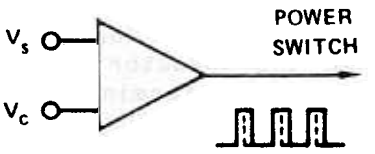


Figure 3.

as shown in Figure 3. A control voltage, V_C, is compared to a fixed frequency linear sawtooth ramp voltage, V_S. The comparator output provides rectangular fixed frequency pulses which drive the power switching transistors. The duty cycle of the power switch conduction is thereby controlled according to the relationship between V_C and V_S.

Direct Duty Cycle Control: The oldest, most commonly used method, implemented in most control IC's. The sawtooth ramp is constant amplitude, (see Figure 4), and the circuit operates exactly as above. Disadvantages are: (1) Provides no voltage feedforward to anticipate the affects of input voltage changes. Slow response to sudden input changes. Poor audio susceptibility. Poor open loop line regulation, requiring higher loop gain to achieve specifications. (2) In continuous mode regulators, provides no help in dealing with the resonant two pole filter characteristic with its sudden 180 degree phase shift. Control changes must propagate through these two filter poles to make a desired output correction, resulting in poor dynamic response.

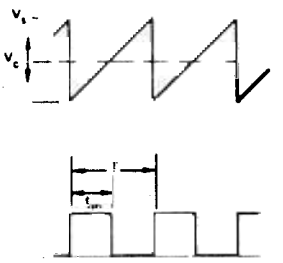


Figure 4.

Voltage Feedforward Control: Functions exactly like direct duty cycle control above with one key exception -- the sawtooth ramp is not constant amplitude, but varies in direct proportion to the input voltage (see Figure 5). The effect of this simple modification is dramatic. Because V_S varies directly with input voltage, if V_C is constant the duty cycle varies inversely with input voltage. Thus the volt-second product, $V_{in}D$, remains constant without any control change. Open loop line regulation is very good, and the problems of direct duty cycle control in (1) above are corrected. Much less closed loop gain is required, mostly to achieve good dynamic response. The UC1840 is a third generation control IC with voltage feedforward capability.

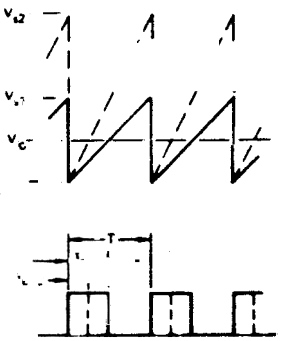


Figure 5.

Current Mode Control: This newest control method, embodied in the UC1846 IC, also controls the duty cycle by comparing the control voltage to a fixed frequency sawtooth ramp. In this case, the ramp voltage is not derived artificially from a ramp generator, but is provided directly from the power switching circuit inductor current waveform through a current sampling resistor (Figure 6). Thus the inductor current ramp is fed back to the control comparator, forming a second, inner control loop. The control voltage out of the error amplifier is derived from the output voltage compared to a voltage reference, as before, but now the control voltage programs the inductor current via the inner loop and no longer controls the duty cycle directly.

The results of this method are profound. All of the problems of the direct duty cycle control method (1) and (2) above are corrected with current mode control. In addition to having the voltage feedforward characteristic with instantaneous open loop response to input changes, current mode control eliminates the inductor filter pole, because this pole is inside the inner loop. This reduces two pole second order filter which is not easy to compensate to a single pole (the filter capacitor) first order filter, which permits simpler compensation networks.

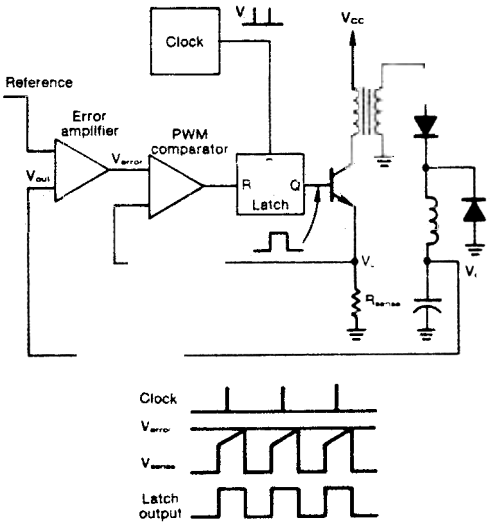


Figure 6.

Current mode control circuits used with continuous mode power switching circuits benefit from slope compensation, and it is required for stability at duty cycles greater than 50%. Ref. Appendix A. Power transformer magnetizing current superimposed upon the reflected load current acts to provide some slope compensation, but the amount is rather variable and indeterminate.

DESIGN THE COMPENSATION NETWORK

The control to output gain characteristic subtracted from the overall closed loop objective roughly defines the characteristic sought in the error amplifier with its compensation network. In general, the procedure involves:
(1) Put zeros in the compensation network near the frequencies where excess poles occur in the control to output gain so that phase shift has an adequate margin (45 degrees) up to the crossover frequency.
(2) Put poles in the compensation network near the frequencies where ESR zeros and right-half-plane zeros occur in the control to output gain. Otherwise these zeros will flatten the gain characteristic and prevent it from falling off as desired.
(3) If low frequency gain is too low to obtain desired DC regulation because of zeros added in step (1), add a pole-zero pair at low frequency to boost gain.
(4) In complex situations, a certain amount of juggling with trial solutions is inevitable.

Compensation Circuits: Two circuits that will handle most compensation requirements are given in Appendix A. These circuits are applied to the example problems in Appendix C. Try to use the power switching topology/control method combination that allows the use of the essentially flat characteristic of circuit A-1 which has no input capacitor, to avoid the poor large signal behavior that invariably results with circuits like A-2 because of abnormal voltage levels that appear on the input capacitor, C_i.

Determine Closed Loop Regulation: It is possible to calculate the DC regulation of the system using classical closed loop analysis, but this is often awkward and of questionable value, because the gain of the system often changes as a function of input and load variables.

It is simpler and more direct to calculate the DC regulation as the large signal problem that it really is: (1) Use the DC equation of the topology/control method combination (Eq. 1a in the examples) to calculate the DC control voltage, V_C, required to maintain the output voltage at the desired level under extremes of line and load conditons. The extreme V_C swing must of course be less than the sawtooth ramp amplitude or the system will not even have control over the desired range of conditions. (2) Divide the extreme V_C swing by the low frequency gain of the E/A compensation circuit. (3) The result is the output error voltage required to provide the desired V_C control swing, which can be expressed as a percentage of the nominal output voltage.

Insufficient Gain-bandwidth: If the amplifier gain-bandwidth is not enough for the desired compensation scheme, there are some alternatives other than: (1) use an IC with a better amplifier, or (2) back down on the crossover frequency.

One alternative is to use a control method that requires less loop gain because line regulation problems are eliminated with input feedforward, and the two pole filter characteristic is gone with current mode control.

Also, when the ramp slope at the comparator input can be set independently, such as in the UC1840 or UC1846, greater control to output gain-bandwidth is achieved by reducing the ramp slope and correspondingly reducing the duty cycle clamp voltage. The full output range is now controlled with a smaller control voltage range, and error amplifier gain-bandwidth requirement is reduced.

Control to output gain-bandwidth is also increased by sensing the highest available output voltage. This reduces the gain-bandwidth requirement of the error amplifier.

EXAMPLES OF CLOSING THE LOOP

Examples are worked out in Appendix C for most basic topologies operated in discontinuous as well as continuous inductor current modes, and using three control methods: direct duty cycle control, voltage feedforward and current mode control.

In the examples given, an input voltage range of 2:1 and load current range of 10:1 is assumed for consistency and to permit direct comparison. All elements of the power circuit are assumed to be transformed to the level of a 12 volt output, and actual primary side voltages, currents and transformer turns ratio, if used, are not visible. The 12 volt output is used as the basis for feedback voltage sensing.

MISCELLANEOUS POINTS

EMI Filter Resonance: When an input EMI filter is used, make sure its resonance is well damped and its resonant frequency is not near the resonant frequency of the output filter, or severe interaction will result.

Modulator Phase Lag: The vast majority of PWM control chips use a simple comparator method of determining pulse width, wherein the output pulse is terminated according to the instantaneous value of the feedback control voltage at the moment of pulse termination. This "naturally sampled" method of pulse width modulation ideally results in zero phase lag in the modulator and in the converter power switching stage.[2] In practice, however, comparator delays and storage time delays in the power switch will cause a phase lag directly proportional to the delay time, t_d, and signal frequency, f, according to the relationship:

$$\Phi_m = 360\ t_d/T = 360\ t_d\ f$$

This additional phase lag reduces the phase margin at the unity gain crossover frequency and may therefore contribute to control loop instability. For example, at a crossover frequency of 25 kHz, consistent with a switching frequency greater than 50kHz, a storage time of 1 microsecond in the power switch will cause an additional phase lag of 9 degrees, reducing phase margin by that amount.

REFERENCES

(1) J. R. Wood, "Taking Account of Output Resistance and Crossover Frequency in Closed Loop Design," POWERCON 10, pp. D4.1-D4.16, March 1983.

(2) R. D. Middlebrook, "Predicting Modulator Phase Lag in PWM Converter Feedback Loops," POWERCON 8, pp. H4.1-H4.6, April 1981.

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