

Power Supply Design Seminar

# Comparison of AC/DC Power-Conversion Topologies for Three-Phase Industrial Systems

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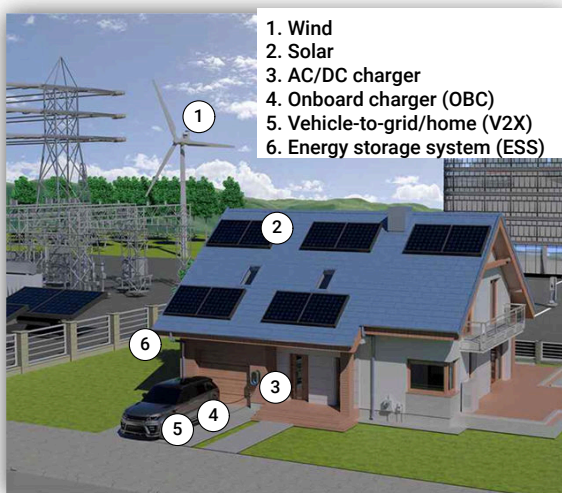
*This paper compares two- and three-level AC/DC converters for three-phase industrial applications, focusing our analysis on two-level, T-type, active neutral point clamped (ANPC), neutral point clamped (NPC) and flying capacitor (FC) topologies. Our evaluation includes system trade-offs such as efficiency, electromagnetic interference (EMI), operating principles, power switching selection and DC link capacitor stress, with a discussion of the impact on the bill of materials (BOM) for the various topologies.*

## Power Conversion System Overview

### Overview: End Equipment with an AC/DC Converter

In recent years, there has been an accelerated adoption of renewable energy (solar and wind), energy storage systems, and electric vehicles (EV) as the world pushes toward a more sustainable future. This fast adoption has significant implications across the entire energy ecosystem, from energy generation, storage and transmission to distribution networks.

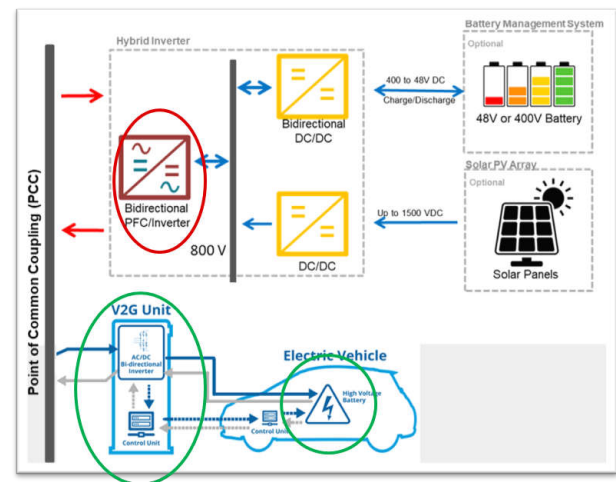
**Figure 1** shows a sustainable ecosystem model. The end equipment in this example includes wind turbines, solar panels, energy storage systems, an offboard EV charger, and an onboard charger with vehicle-to-grid functionality. The overarching challenges associated with these types of end equipment include grid stability, power quality, time for energy delivery and efficiency.



**Figure 1.** Sustainable ecosystem model.

As highlighted in **Figure 2**, a common subsystem in these equipment types (hybrid inverters, vehicle to grid

and EV onboard chargers) is the AC/DC converter. The performance of the AC/DC converter significantly contributes to the overall system stability (or reliability), power quality, rate of energy delivery (such as the charging time of an EV) and efficiency. Let's take a closer look at the AC/DC converter.



**Figure 2.** Schematic representation of AC/DC tied to the grid.

### Overview: Existing AC/DC Topologies

In this section, we're only going to discuss the boost topology, since that is the most common topology used for three-phase industrial applications. But before we dive deeper, let's look at a generic example of a three-phase boost AC/DC stage, shown in **Figure 3**. The elements highlighted in the block diagram are the point of common coupling on the grid side, the EMI filter stage, the boost AC/DC stage, and the DC load at VDC+ and VDC-.

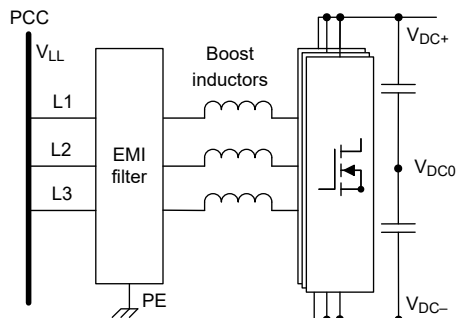
There are a number of benefits when employing a boost AC/DC topology:

- Higher efficiency (a boost topology means lower application currents, and thus fewer  $I^2R$  losses).

- Less EMI noise injected in the grid because of inductive coupling.
- The ability to handle better surges from the grid given the capacitive behavior of the DC link.

The basic requirements for boost AC/DC converters are:

- Boost power factor correction (PFC) ( $V_{DC} \gg \sqrt{2} V_{LL}$ ), where  $V_{DC}$  is the DC voltage of the DC link and  $V_{LL}$  is the line-to-line voltage of the grid.
- Inductive behavior on the grid side.
- Capacitive behavior on the DC side.



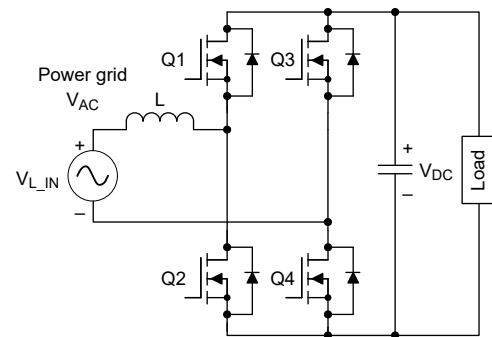
**Figure 3.** Boost AC/DC block diagram.

## Overview: Single Phase vs. Three Phase

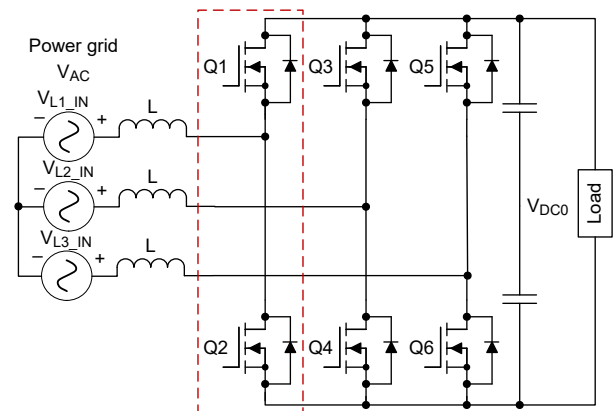
For a given power requirement, a three-phase converter requires less current, is a smaller size, and produces less power ripple than a single-phase converter. For example, an 11-kW single-phase PFC requires 48 A, while an 11-kW three-phase PFC requires only 16 A per phase. Less current means fewer losses and thus improves the power densities of such systems.

A single phase has power ripple in the DC link, while a balanced three-phase converter does not. **Figure 4** and **Figure 5** illustrate examples of single- and three-phase PFCs, respectively. In **Figure 5**, the blue rectangle highlights the switching cell, which we will discuss in **Three-Phase Boost Converter Topologies: Overview and Operating Principles** for a few common AC/DC topologies. Notice that in **Figure 5**, the neutral of the grid

connects virtually to the middle point of the DC link (at high frequencies), as denoted by VDC0.



**Figure 4.** Single-phase, two-level PFC.



**Figure 5.** Three-phase PFC with the switching cell highlighted for a two-level topology.

## Three-Phase Boost Converter Topologies: Overview and Operating Principles

### Multilevel Topologies Overview on AC/DC Power Stages

Let's introduce some of most common AC/DC topologies employed in industrial applications. For simplicity, the following schematics highlight only the switch cell of these topologies (thus, only one of three legs is shown). The two- and three-level FC topologies both require two connections to the DC link (VDC+ and VDC-). The T-type, Vienna, ANPC and NPC topologies require three connections to the DC link (VDC+, VDC0 and VDC-).

2L, two-level converter	FC 3L, flying capacitor

Table 1. Topologies requiring two connections to the DC link.

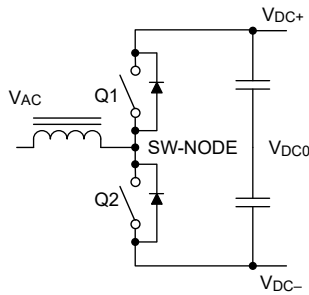
T-type 3L, three-level T-type converter	3L, Vienna rectifier

ANPC 3L, active neutral point converter	NPC 3L, neutral point converter

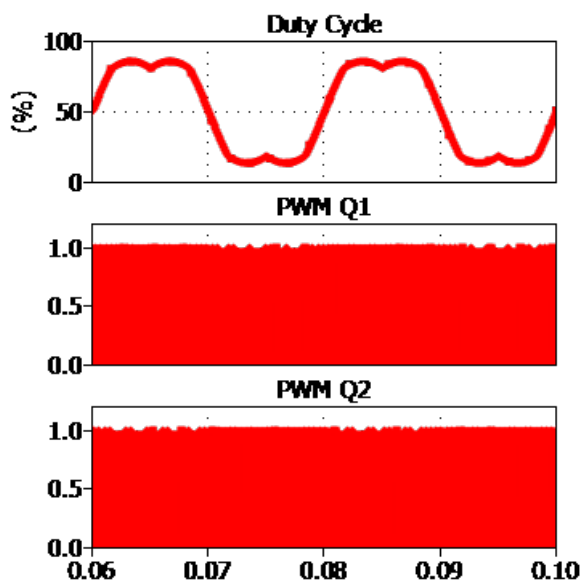
Table 2. Topologies requiring three connections to the DC link.

## Two-Level Inverter Basic Operational Principles

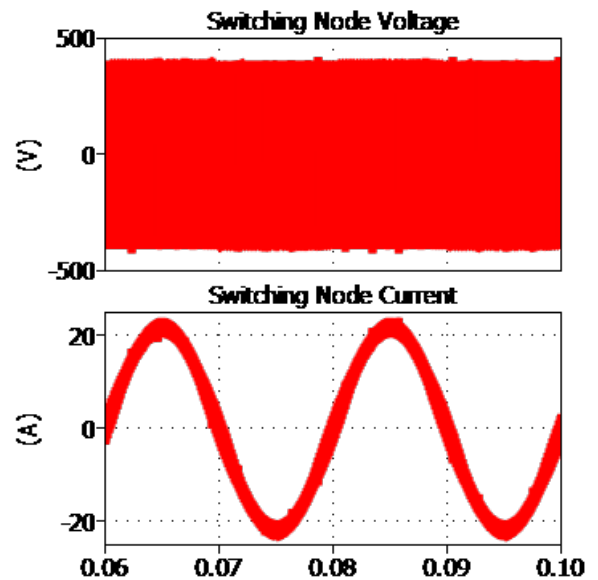
**Figure 6** shows the basic operation of a two-level inverter, where  $V_{AC}$  is referenced to  $V_{DC0}$ . This is a bidirectional topology capable of both inverter and PFC modes. **Figure 7** and **Figure 8** show the corresponding switching characteristics of the inverter mode over two cycles. In **Figure 8**, the positive switching node current denotes the inductor current flowing into the grid  $V_{AC}$ .



**Figure 6.** Schematic representation of a two-level inverter single switching cell.



**Figure 7.** Switching duty cycle and gate-driver pulse-width modulation (PWM) signals.



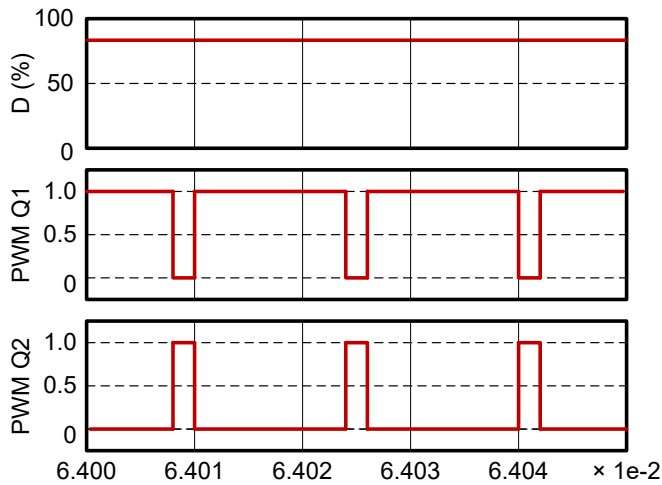
**Figure 8.** Switching voltage and current.

For a positive sine wave ( $V_{DC0} \leq V_{AC} \leq V_{DC+}$ ) and a duty cycle greater than 50%, Q1 and Q2 are switching at  $f_{PWM}$ . The output voltage is defined by the duty cycle of the PWM (where Q1 is on more often than Q2).

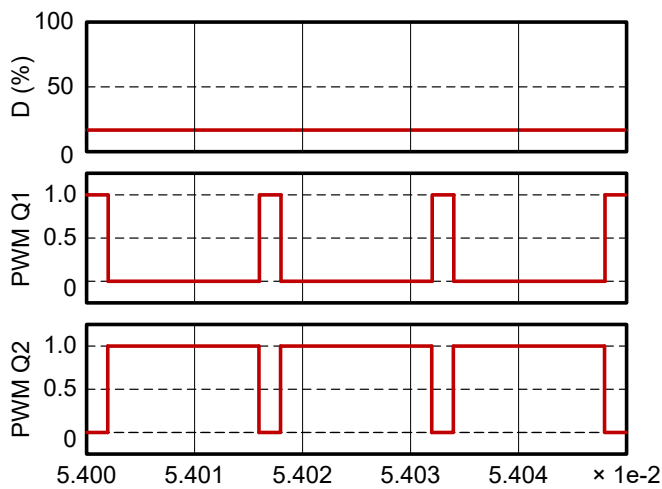
**Figure 9** highlights an example PWM profile for a positive sine wave. There is dead time between Q1 and Q2 to prevent shoot-through during the switching transition. For a negative sine wave ( $V_{DC-} \leq V_{AC} \leq V_{DC0}$ ) and a duty cycle less than 50%, Q1 and Q2 are switching at  $f_{PWM}$ . Again, the output voltage is defined by the duty cycle of the PWM (Q1 is off more often than Q2).

**Figure 10** highlights an example PWM profile for a negative sine wave.

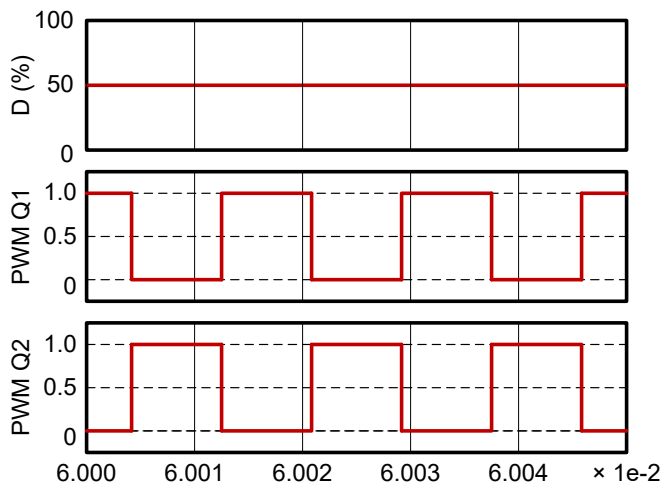
As shown in **Figure 11**, at the zero crossing of the sine wave the duty cycle is close to 50%. For this two-level topology, the output ripple frequency ( $f_{RIPPLE}$ ) is equal to  $f_{PWM}$ . The  $f_{RIPPLE}$  defines filtering component sizes such as magnetics and capacitors. Furthermore, Q1 and Q2 need be  $V_{DC}$ -rated; for example, for a  $V_{DC}$  of 800 V, the switches need to be 1,200-V rated.



**Figure 9.** PWM profile when the grid phase voltage is positive.



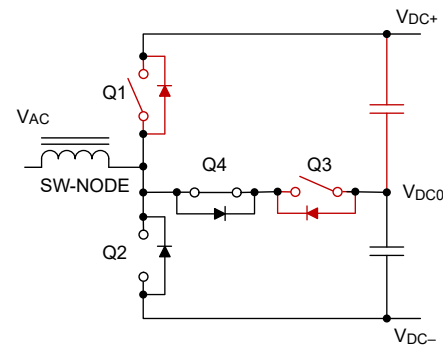
**Figure 10.** PWM profile when the grid phase voltage is negative.



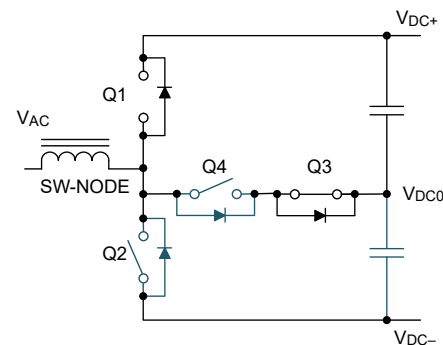
**Figure 11.** PWM profile at zero crossing.

## Three-Level T-Type Inverter Basic Operational Principles

**Figure 12** shows the basic operation of a three-level T-type inverter, a bidirectional topology capable of both inverter and PFC modes. For a positive sine wave ( $V_{DC0} \leq V_{AC} \leq V_{DC+}$ ), Q4 is permanently in the on-state and Q2 is permanently off. Q1 and Q3 in red are switching  $f_{PWM}$  (see **Figure 12**). As expected, the dead time between Q1 and Q3 needs to be accounted for. For a negative sine wave ( $V_{DC-} \leq V_{AC} \leq V_{DC0}$ ), Q3 is permanently in the on-state and Q1 is permanently off. Q2 and Q4 in blue are switching  $f_{PWM}$ , as shown in **Figure 13**. Again, the dead time between Q2 and Q3 needs to be accounted for. For this topology, the output  $f_{RIPPLE}$  is equal to  $f_{PWM}$ . Q1 and Q2 need be  $V_{DC}$ -rated (for a  $V_{DC}$  of 800 V, the switches need to be 1,200 V-rated) and Q3 and Q4 can be one-half  $V_{DC}$ -rated (for a  $V_{DC}$  of 800 V, the switches need to be 600 V-rated).

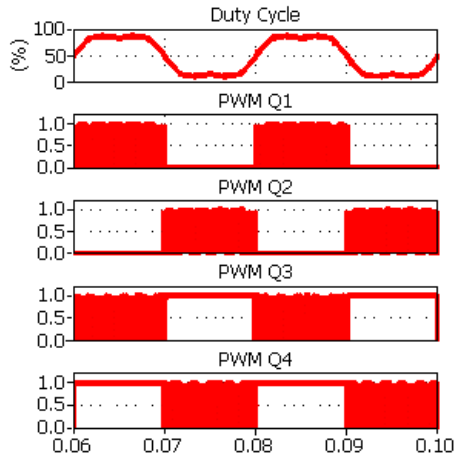


**Figure 12.** Schematic representation of a T-type inverter single switching cell when the grid voltage is positive, with devices in commutation highlighted in red.

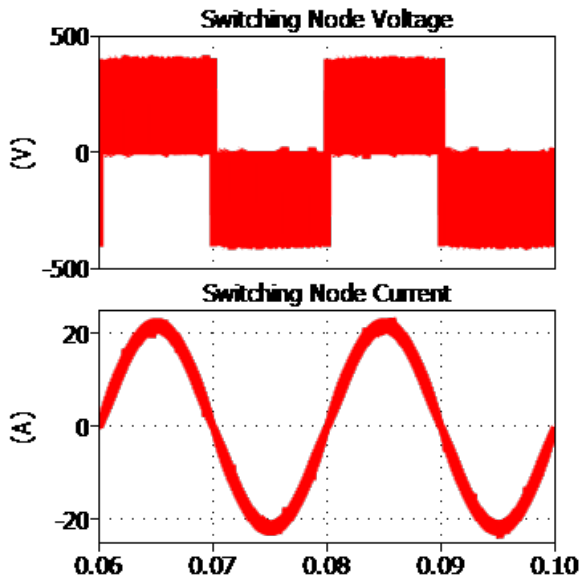


**Figure 13.** Schematic representation of a T-type inverter single switching cell when the grid voltage is negative, with devices in commutation highlighted in blue.

**Figure 14** and **Figure 15** show the corresponding switching characteristics of the inverter mode over two cycles. As expected, the output voltage has three levels ( $V_{DC+}$ ,  $V_{DC-}$  and  $V_{DC0}$ ). In addition, the three-level inverter current ripple is less than the two-level inverter.



**Figure 14.** Switching duty cycle and gate-driver PWM signals.

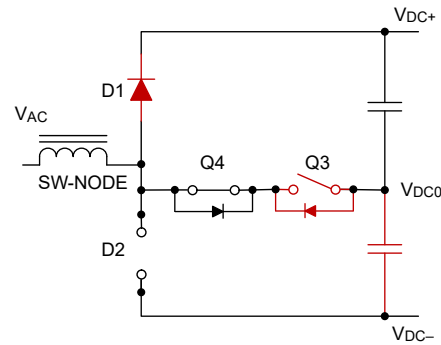


**Figure 15.** Switching voltage and current.

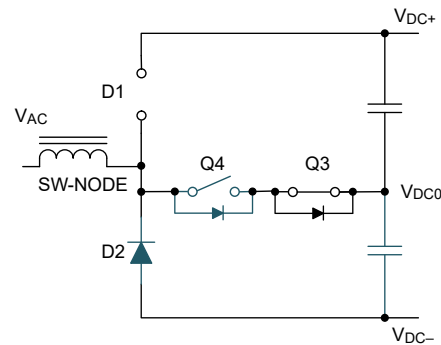
### Three-Level Vienna Basic Operational Principles in PFC Mode

**Figure 16** shows the basic operation of a three-level Vienna rectifier. This is a unidirectional topology capable of only PFC mode. **Figure 18** and **Figure 19** show the corresponding switching characteristics of the PFC mode over two cycles. In **Figure 19**, the current is

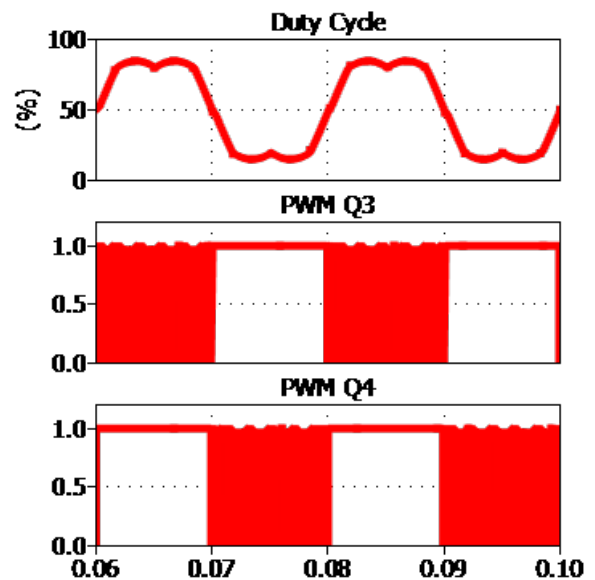
negative because of the PFC mode (with positive current defined as current flowing into the grid  $V_{AC}$ ).



**Figure 16.** Schematic representation of a Vienna rectifier single switching cell during a positive grid cycle, with devices in commutation highlighted in red.



**Figure 17.** Schematic representation of a Vienna rectifier single switching cell during a negative grid cycle, with devices in commutation highlighted in blue.



**Figure 18.** Switching duty cycle and gate-driver PWM signals.



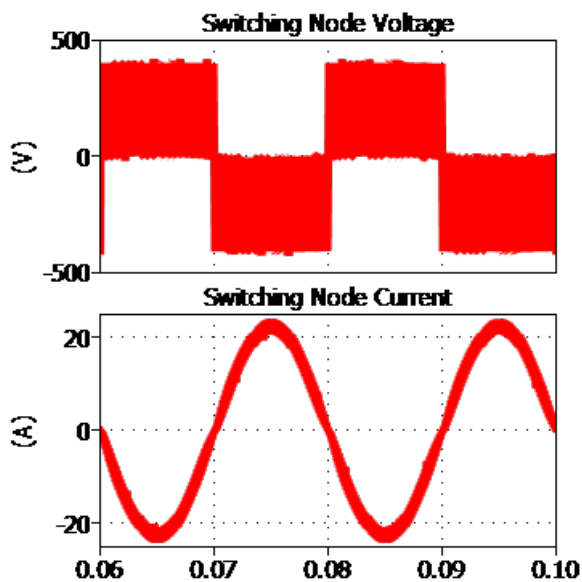


Figure 19. Switching voltage and current.

For a positive sine wave ( $V_{DC0} \leq V_{AC} \leq V_{DC+}$ ), Q4 is permanently in the on-state and Q3 in red is switching at  $f_{PWM}$  (see Figure 16). For a negative sine wave ( $V_{DC-} \leq V_{AC} \leq V_{DC0}$ ), Q3 is permanently in the on-state and Q4 is in blue switching at  $f_{PWM}$  (see Figure 17). Similar to the T-type, the Vienna  $f_{RIPPLE}$  is equal to  $f_{PWM}$ . D1 and D2 need be  $V_{DC}$ -rated (for example, for a  $V_{DC}$  bus of 800 V, you would need 1,200-V-rated devices) and Q3 and Q4 can be one-half  $V_{DC}$  rated (for example, an 800- $V_{DC}$  bus requires 600-V-rated devices). As you can see, the Vienna operation is very similar to the T-type.

### Three-Level ANPC Inverter Basic Operational Principles

Figure 20 shows the basic operation of a three-level ANPC inverter, a bidirectional topology capable of inverter and PFC modes.

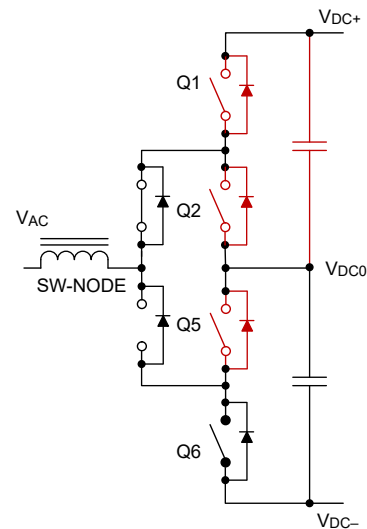
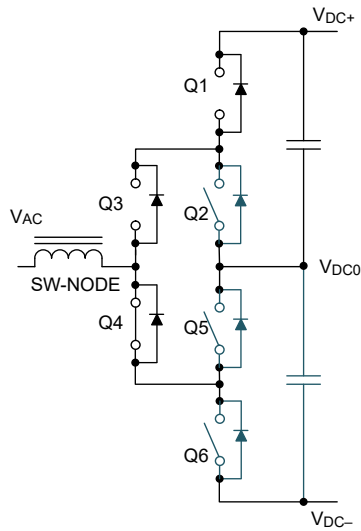


Figure 20. Schematic representation of an ANPC inverter single switching cell when the grid voltage is positive, with devices in conduction highlighted in red.

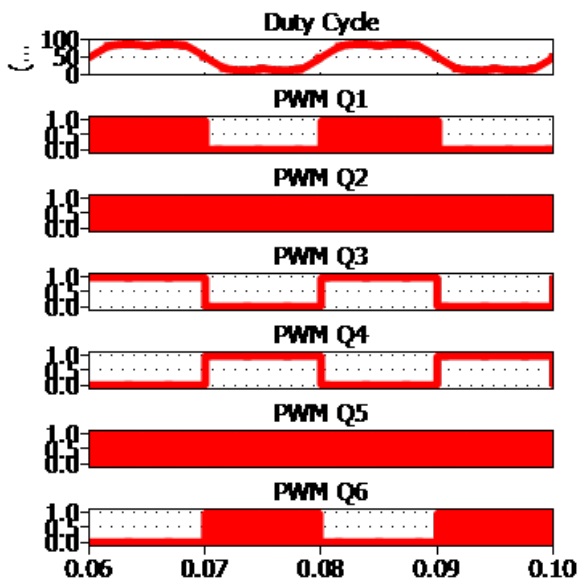
For a positive sine wave ( $V_{DC0} \leq V_{AC} \leq V_{DC+}$ ), Q3 is permanently in the on-state and Q4 is off (see Figure 20). Q1 and Q2 in red are switching at  $f_{PWM}$ . Additionally, Q5 is switching with Q1 to keep one-half  $V_{DC}$  across Q4 and Q6. For a negative sine wave ( $V_{DC-} \leq V_{AC} \leq V_{DC0}$ ), Q4 is permanently in the on-state and Q3 is off (see Figure 21). Q5 and Q6 in blue are switching at  $f_{PWM}$ . Additionally, Q2 is switching with Q6 to keep one-half  $V_{DC}$  across Q1 and Q3. Here,  $f_{RIPPLE}$  is equal to  $f_{PWM}$ , but Q3 and Q4 are switching at  $f_{AC}$  (50 or 60 Hz). All switches can be one-half  $V_{DC}$ -rated (800 V to 600 V). In contrast to T-type, one special requirement of an ANPC inverter is that it requires shutdown sequencing to balance voltages to one-half  $V_{DC}$ .



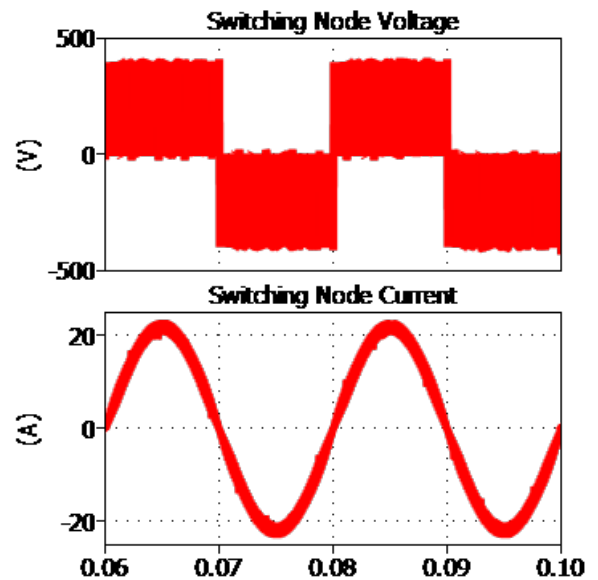
**Figure 22** and **Figure 23** show the corresponding switching characteristics of the ANPC inverter mode over two cycles.



**Figure 21.** Schematic representation of an ANPC inverter single switching cell when the grid voltage is negative, with devices in commutation highlighted in blue.



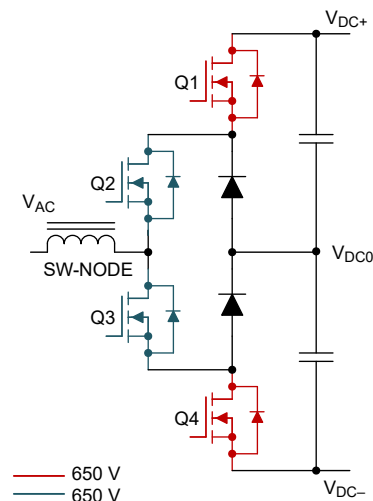
**Figure 22.** Switching duty cycle and gate-drive PWM signals.



**Figure 23.** Switching voltage and current.

### Three-Level NPC Inverter Basic Operational Principles

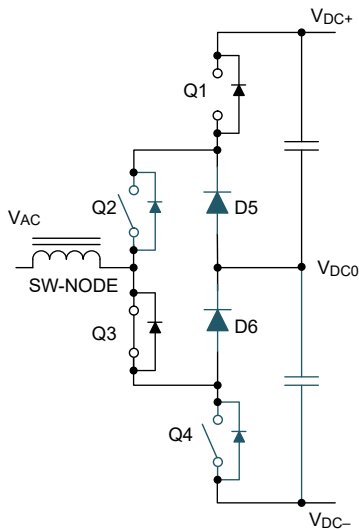
**Figure 24** shows the basic operation of a three-level NPC inverter, a bidirectional topology capable of inverter and PFC modes.



**Figure 24.** Schematic representation of an NPC inverter single switching cell when the grid voltage is positive, with devices in commutation highlighted in red.

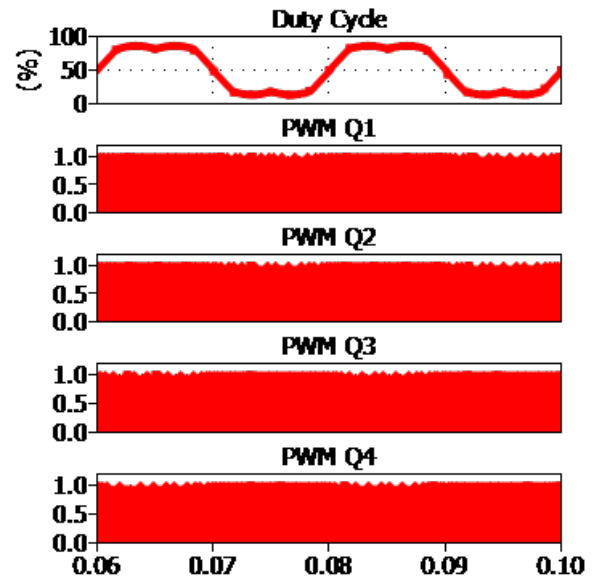
For a positive sine wave ( $V_{DC0} \leq V_{AC} \leq V_{DC+}$ ), Q2 is permanently in the on-state and Q4 is off (see **Figure 24**). Q1 and Q3 in red are switching at  $f_{PWM}$ . Depending on the inductor current direction, either D5 or D6 can be active (freewheeling) when Q1 is off and Q3 is

on. For example, if the inductor current flows from the switch node to  $V_{AC}$ , then D5 is forward-biased and D6 is reverse-biased. In contrast, if the inductor current flows from  $V_{AC}$  to the switch node, then D6 is forward-biased and D5 is reverse-biased. For a negative sine wave ( $V_{DC-} \leq V_{AC} \leq V_{DC0}$ ), Q3 is permanently in the on-state and Q1 is off (see [Figure 25](#)). Q4 and Q2 in blue are switching at  $f_{PWM}$ . The output  $f_{RIPPLE}$  is equal to  $f_{PWM}$ . As we mentioned, either D5 or D6 can be active (freewheeling) depending on the inductor current direction. Like an ANPC inverter, all switches can be one-half  $V_{DC}$ -rated (for example, an 800-V- $V_{DC}$  bus requires 600-V-rated devices). This topology also requires shutdown sequencing to balance voltages to one-half  $V_{DC}$ .

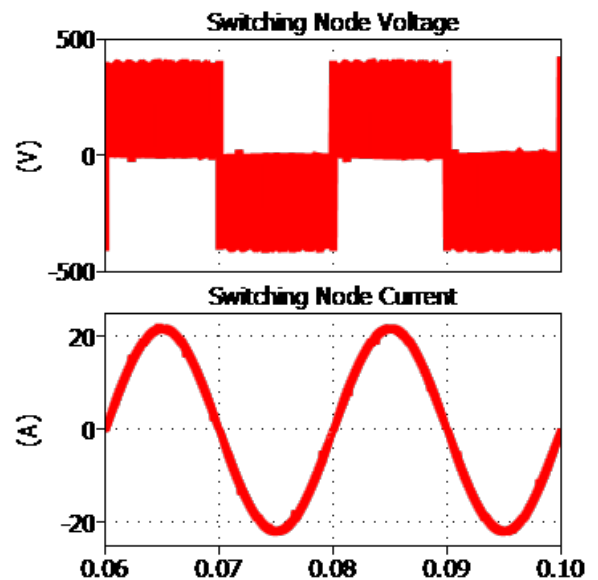


**Figure 25.** Schematic representation of an NPC inverter single switching cell when the grid voltage is negative, with devices in commutation highlighted in blue.

[Figure 26](#) and [Figure 27](#) show the corresponding switching characteristics of the inverter mode over two cycles.



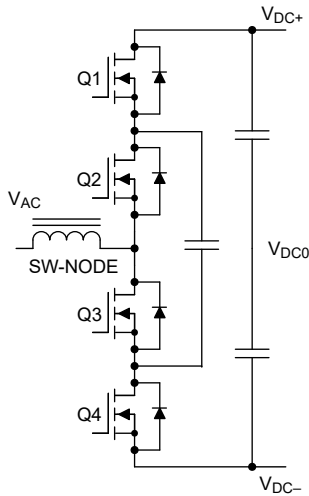
**Figure 26.** Switching duty cycle and gate-driver PWM signals.



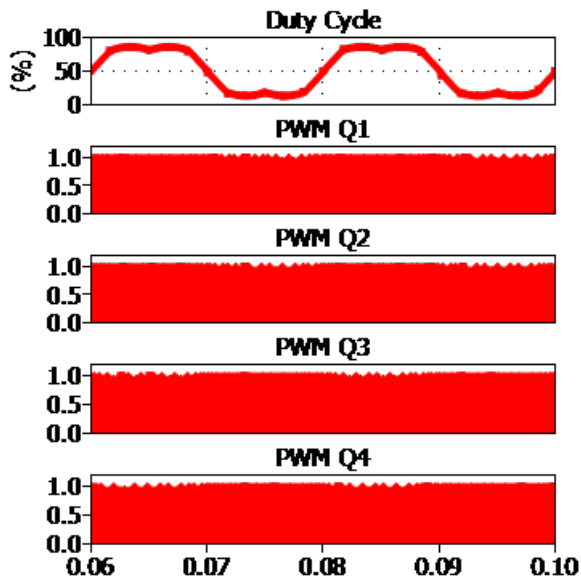
**Figure 27.** Switching voltage and current.

### Three-Level FC Inverter Basic Operational Principles

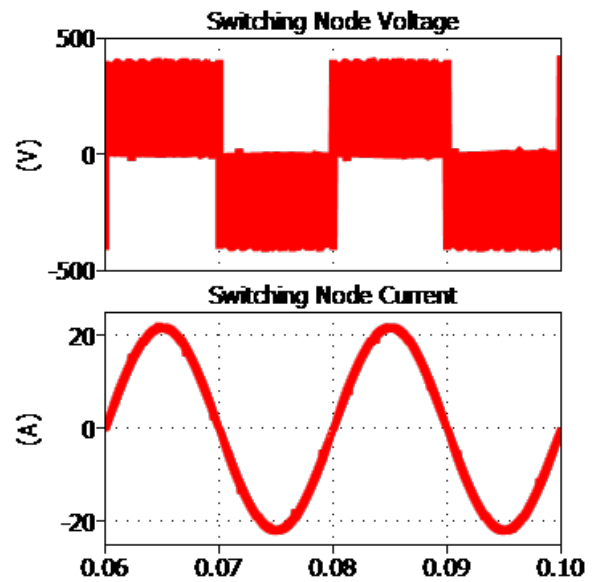
**Figure 28** shows the basic operation of a three-level FC inverter, a bidirectional topology capable of inverter and PFC modes. **Figure 29** and **Figure 30** show the corresponding switching characteristics of the inverter mode over two cycles.



**Figure 28.** Schematic representation of a three-level FC inverter single switching cell.



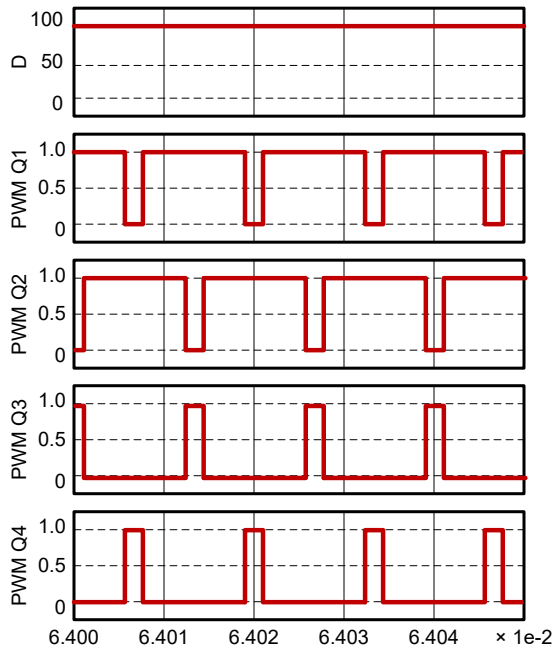
**Figure 29.** Switching duty cycle and gate-driver PWM signals.



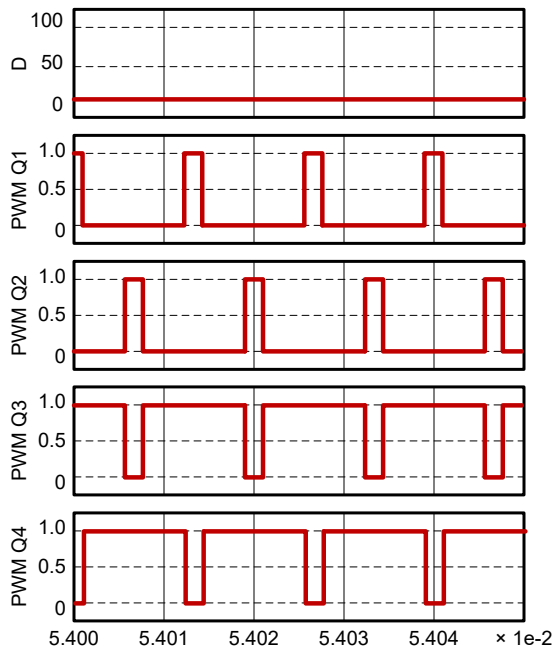
**Figure 30.** Switching voltage and current.

In this topology, all field-effect transistors (FETs) are switching  $f_{PWM}$ . Switch pairs Q1 and Q4 and Q2 and Q3 are complementary to each other, thus requiring two pairs of dead times. For a positive sine wave ( $V_{DC0} \leq V_{AC} \leq V_{DC+}$ ), at the positive peak Q1 and Q4 and Q2 and Q3 are 180 degrees phase-shifted to each other. Q1 and Q2 are more in the on-state than Q3 and Q4 (see **Figure 31**). For a negative sine wave ( $V_{DC-} \leq V_{AC} \leq V_{DC0}$ ), at the negative peak Q1 and Q4 and Q2 and Q3 are 180 degrees phase-shifted to each other. Q1 and Q2 are more in the off-state than Q3 and Q4 (see **Figure 32**). At the zero crossing, the duty cycle of Q1 and Q4 and Q2 and Q3 are each 50% (see **Figure 33**).

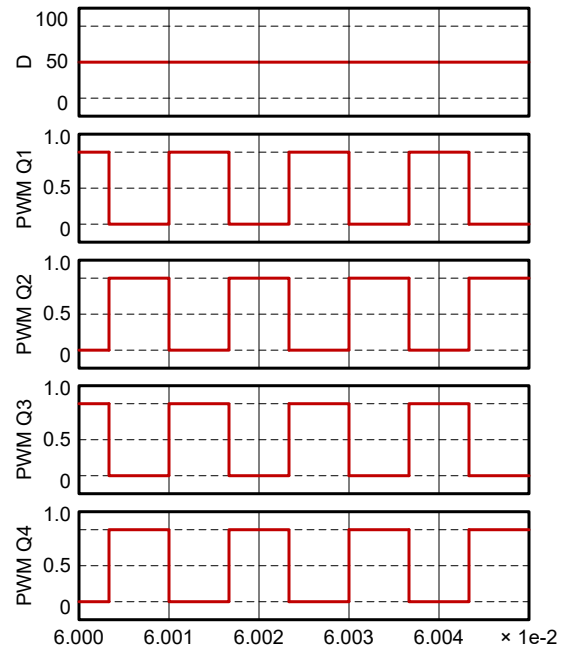
In contrast to the previous topologies,  $f_{RIPPLE}$  is equal to two times the  $f_{PWM}$ . This means smaller filter component sizes for magnetics and capacitors. For a three-level FC, all switches can be one-half  $V_{DC}$ -rated (for example, an 800- $V_{DC}$  bus requires 600-V-rated devices). The initial charging of the FC to one-half  $V_{DC}$  is vital. Furthermore, active control of the voltage for each FC is required in order to keep it charged at half of the DC bus voltage, thus increasing the control scheme complexity. Like the ANPC and NPC inverters, a three-level FC inverter requires shutdown sequencing to balance voltages to one-half  $V_{DC}$ .



**Figure 31.** PWM profile when the grid phase voltage is positive.



**Figure 32.** PWM profile when the grid phase voltage is negative.



**Figure 33.** PWM profile for a zero crossing.

## Power Topology Comparisons

When designing three-phase converters, you need to consider:

- Input filtering.
- Output filtering.
- Active component selection.
- Control.
- Drivers.
- Measurements.

Converter size, efficiency and cost are at first approximations, driven by:

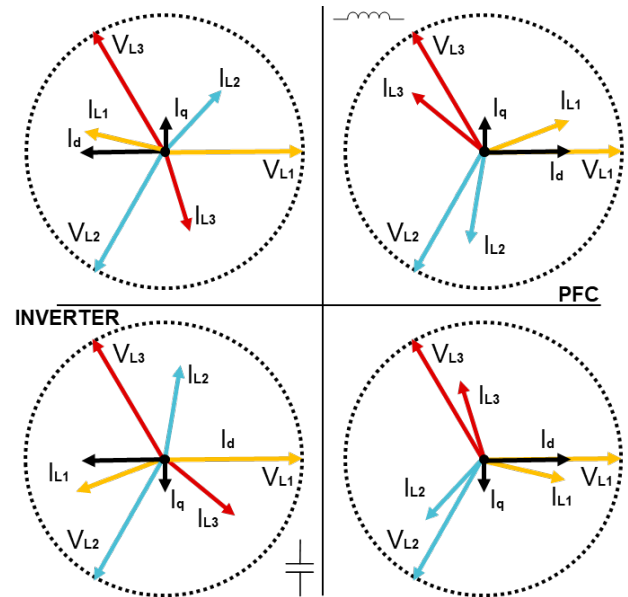
- Active components and cooling.
- Output filtering (capacitors).
- Input filtering (EMI filtering).

## Applied Methodology

Let's compare the power losses; root-mean-square (RMS) current in the DC link; and common-mode noise for the Vienna, T-type, ANPC, NPC and FC converters. In order to keep the investigation consistent, we specified a constant power of 11 kVA at 800 V<sub>DC</sub> and 400 V<sub>AC</sub>. The converters will switch at different switching frequencies,

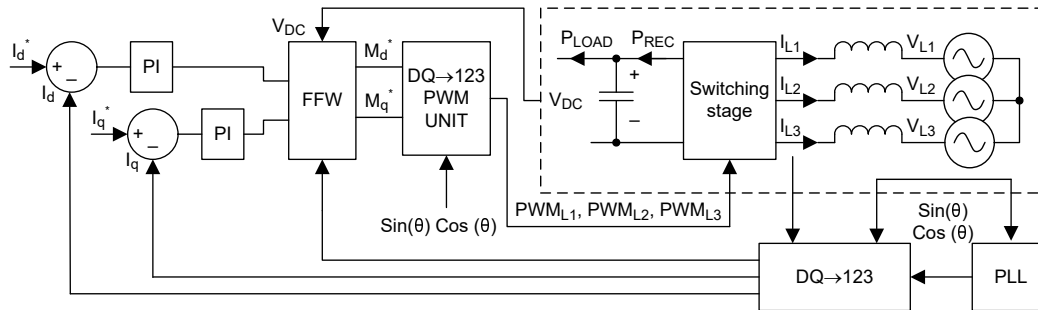
but always with the aim to keep 130 W dissipated by the active components.

The AC/DC converters run at fixed apparent power but the power factor will change, thus leading to PFC, inverter, capacitive and inductive behavior. **Figure 34** depicts the four quadrants' operating points of a three-phase inverter for a symmetrical system. Three-phase currents, voltages and their corresponding phase shifts are shown when having the AC/DC converter working respectively as a PFC, inductive load, inverter and capacitive load. The currents and voltages have a constant amplitude, thus implying constant apparent power.



**Figure 34.** Operating region of a three-phase converter.

Applying the synchronous reference frame control scheme to control the currents with respect to the voltages by keeping a fixed amplitude enabled us to control the active and reactive powers with precision (see **Figure 35**).



**Figure 35.** Synchronous reference frame control block diagram when having current control loops.

In **Figure 35**:

- The phase-locked loop (PLL) is responsible for the synchronization of the grid with the converter. The PLL provides a reference angle with respect to the grid by computing the grid voltage measurements.
- Clarke and Park transformations transform three-phase variables into direct and quadrature variables by using the angle obtained from the PLL (123 -> DQ). Direct and quadrature currents control the active and reactive power directly, and thus the apparent power ( $I_d$  and  $I_q$ ).
- Feed forward (FFW) makes the current control loops faster and keeps the bandwidth of the system fixed, with the DC link voltage normalization and grid voltages applied internally.
- Two proportional-integral (PI) control loops control the  $I_d$  and  $I_q$  currents.

**Figure 35** also shows how to control the currents in the three-phase converter by changing  $I_d^*$  and  $I_q^*$ . **Equation 1** and **Equation 2** express the values of  $I_d$  and  $I_q$ :

$$I_d^* = I_{ref} \times \cos(\theta) \quad (1)$$

$$I_q^* = I_{ref} \times \sin(\theta) \quad (2)$$

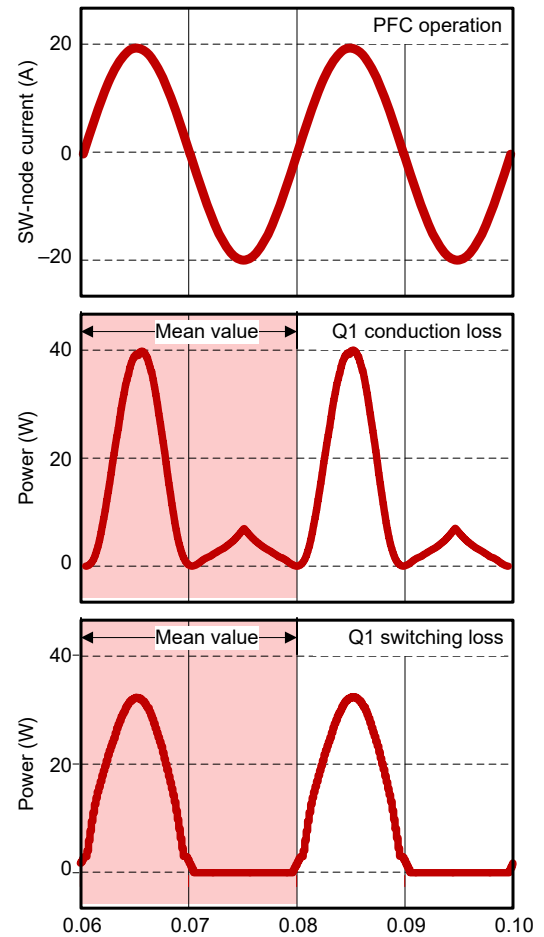
where  $I_{ref}$  is the grid current (in this case equal to 16  $A_{RMS}$ ), and  $\theta$  is the desired displacement between the currents and voltages.

In a practical scenario,  $\theta$  can vary between  $-180$  degrees and  $180$  degrees in order to achieve PFC, inverter, and inductive and capacitive behavior.

## Active Components Power-Loss Comparisons

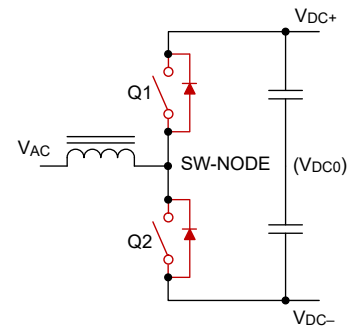
### Component Loss Measurements

When running a time-domain simulation, the conduction and switching losses of each active component used for each topology vary with respect to time, as shown in **Figure 36**.



**Figure 36.** Conduction and switching losses of an active component.

In **Figure 36**,  $I_{SW}$  represents the switching-node current of a three-phase two-level converter, together with the conduction and switching losses of Q1 (see **Figure 37**).



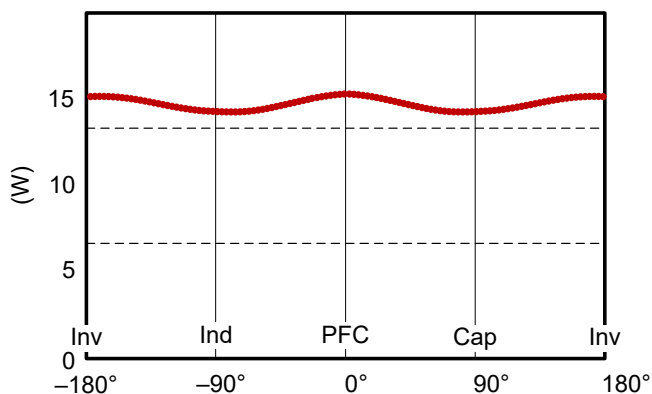
**Figure 37.** Two-level converter single-leg schematic representation.

You can see from **Figure 36** that conduction and switching losses change in time with respect to the electrical period (20 ms) because the current is changing as well. On the first half period (between 0.06 s and 0.07 s), the switching and conduction losses present the same trend as the current. On the second half period (between 0.07 s and 0.08 s), switching losses are null because Q1 is always soft switching.

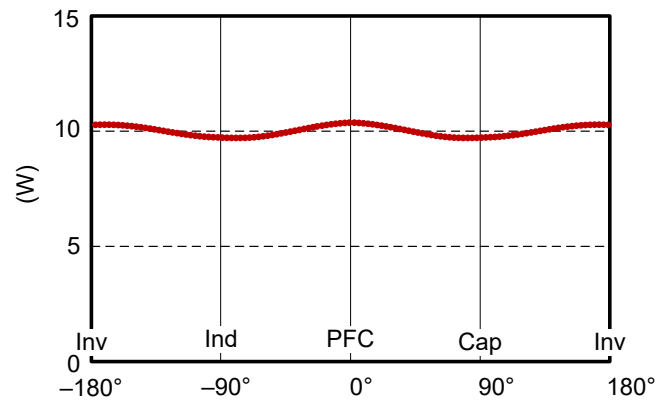
On the other hand, conduction losses are not properly sinusoidal because of space vector modulation (see **Figure 37**). Calculating the average values of the instantaneous powers thus obtains the mean values for conduction and switching losses. The red rectangle in **Figure 36** represents the region where the mean value of the losses is calculated.

### Two-Level Converter Active Component Loss Analysis

A two-level, three-phase converter comprises three fundamental switching cells, as represented in **Figure 37**. We selected a converter with power rating of 11 kVA, silicon carbide (SiC) devices with a drain-to-source on-resistance  $R_{DS(on)}$  of 75 m $\Omega$  and a blocking voltage of 1.2 kV for both Q1 and Q2. With a switching frequency of 60 kHz, the six switches dissipate a total loss of 130 W in the active components. **Figure 38** and **Figure 39** highlight the conduction and switching losses of Q1 and Q2 (see **Figure 37**), respectively, as a function of the power factor. The switching losses are the turnon and turnoff losses of the device.



**Figure 38.** Q1 and Q2 conduction losses of a two-level converter as a function of the power factor when operating at 11 kW.



**Figure 39.** Q1 and Q2 switching losses of a two-level converter as a function of the power factor (operating angle).

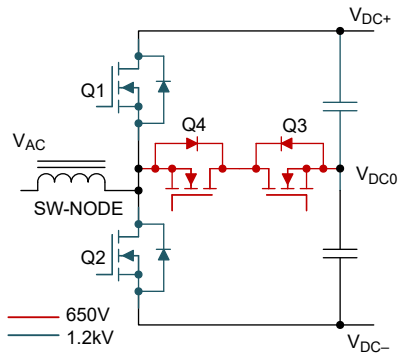
The conduction and switching losses within the top and bottom switches are the same because of the sinusoidal behavior presented by the converter itself. The losses will be equal because half of the period current passes through Q1 and the other half passes through Q2. When changing the power factor of the converter, there are no significant differences in both the conduction and switching losses. From these results, it is possible to conclude that two-level three-phase converters behave mostly the same in terms of efficiency and power dissipation when changing the power factor. In other words, working as a PFC or inverter does not significantly change device selection. This topology is optimized even when selecting the same power switches.

### Three-Level T-Type and Vienna Rectifier

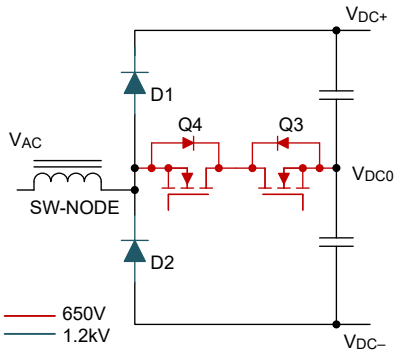
For a three-level T-type inverter with a power rating of 11 kVA, we selected SiC devices with an  $R_{DS(on)}$  of 75 m $\Omega$  and a blocking voltage of 1.2 kV for Q1 and Q2, and 60 m $\Omega$  and 650 V for Q3 and Q4 (see **Figure 40**). With a switching frequency of 100 kHz, we measured an average total loss of 130 W in the active components from the 12 switches.

In the Vienna rectifier, we selected SiC diodes with a blocking voltage of 1.2 kV and 30 A, rated for D1 and D2, and 60-m $\Omega$  and 650-V SiC metal-oxide semiconductor field-effect transistors (MOSFETs) for Q3 and Q4 (see **Figure 40**). Switching at 95 kHz achieved the target loss.



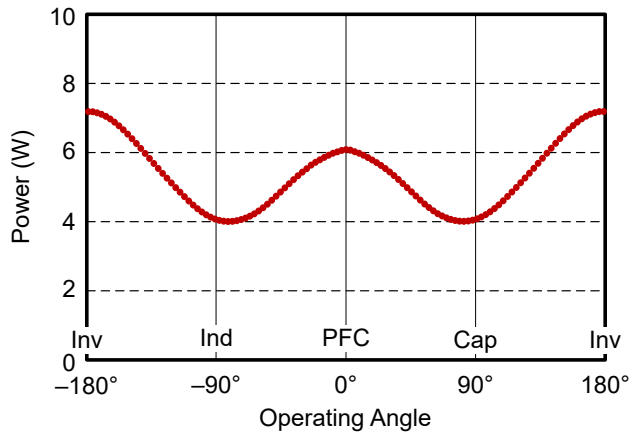


**Figure 40.** Three-level T-type single-leg schematic representation, with 1.2-kV components highlighted in blue and 650 V highlighted in red.

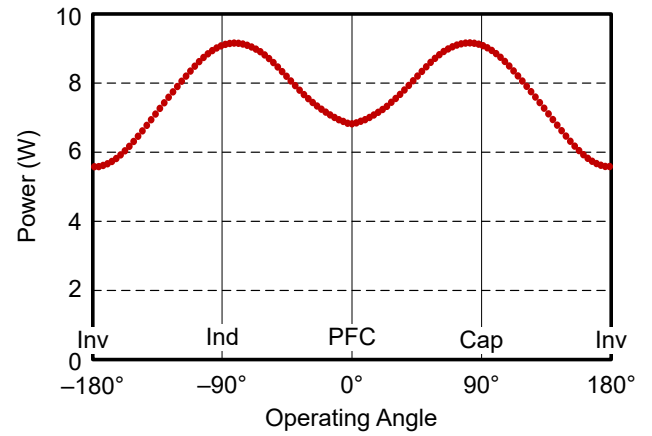


**Figure 41.** Three-level Vienna single-leg schematic representation, with 1.2-kV components highlighted in blue and 650 V highlighted in red.

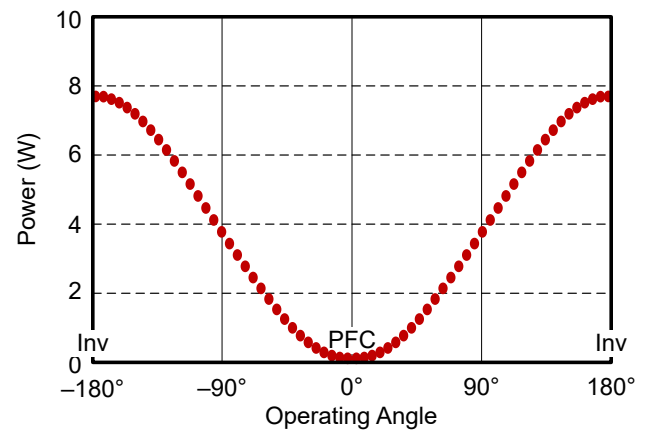
Figure 42 through Figure 45 show the conduction and switching losses of Q1, Q2, Q3 and Q4 as a function of the power factor.



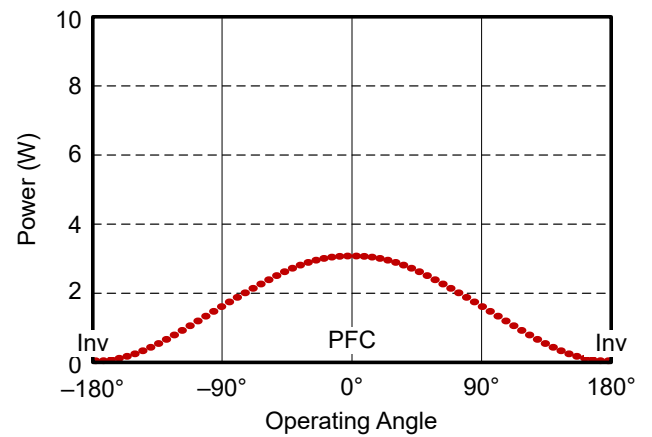
**Figure 42.** Q1 and Q2 conduction losses of a T-type converter as a function of the power factor.



**Figure 43.** Q3 and Q4 conduction losses of a T-type converter as a function of the power factor.



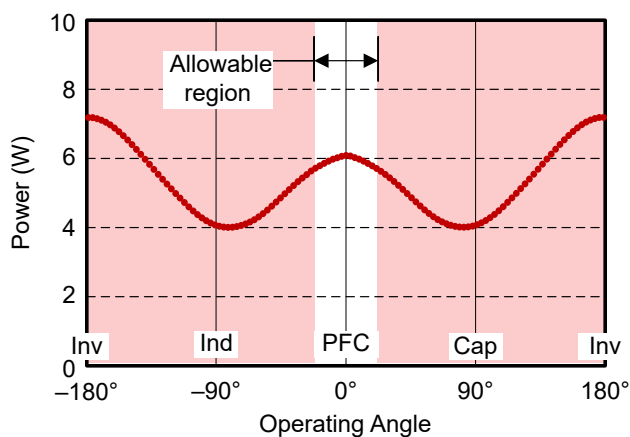
**Figure 44.** Q1 and Q2 switching losses of a T-type converter as a function of the power factor.



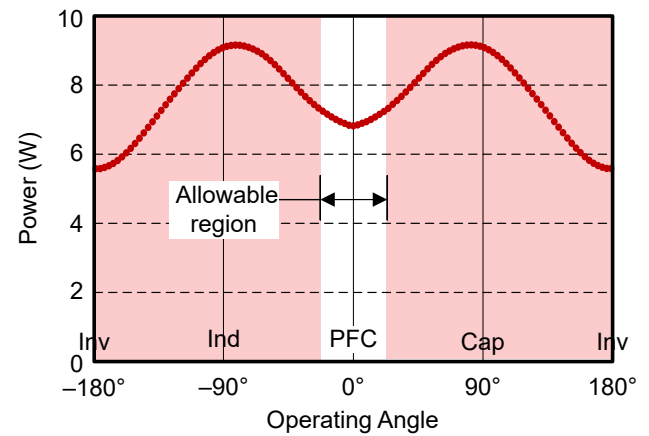
**Figure 45.** Q3 and Q4 switching losses of a T-type converter as a function of the power factor.

From [Figure 42](#) and [Figure 43](#), you can see that the conduction losses of Q1, Q2, Q3 and Q4 are never null. Q1 and Q2 present lower losses when working as a PFC and Q3 and Q4 dissipate higher losses when pushing reactive power toward the grid (capacitive and inductive). From [Figure 44](#) and [Figure 45](#), you can see that when operating a T-type converter as an inverter, no switching losses are present in Q3 and Q4, but the maximum losses are measured in Q1 and Q2. Furthermore, the switching losses in Q1 and Q2 are much lower with respect to a two-level converter, even if switching at a higher switching frequency (from 60 kHz to 100 kHz). The reason is that Q1 and Q2 are switching at 400 V instead of 800 V. When a converter is working as inverter, as in photovoltaic (PV) applications, it is not necessary to have Q3 and Q4 based on wide band-gap devices, but you could also use lower-cost devices such as insulated gate-bipolar transistors with antiparallel diodes or silicon superjunction MOSFETs.

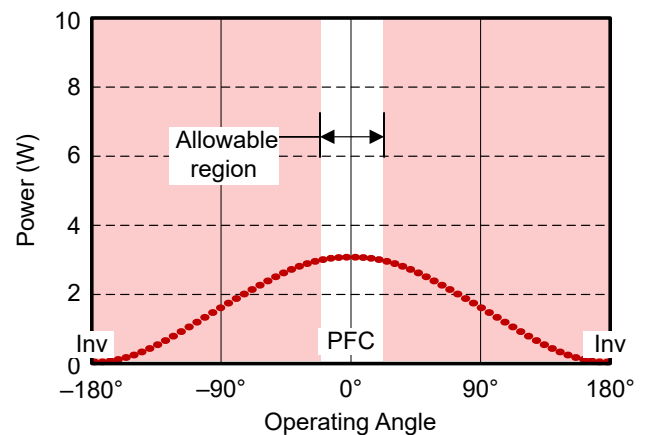
When the converter is operating in PFC mode, there are no switching losses in Q1 and Q2. In this case, you can evaluate less-expensive options for Q1 and Q2, making this converter type attractive for applications such as unidirectional DC charger stations. Substituting Q1 and Q2 with diodes as in a Vienna rectifier achieves lower BOM costs, but at the expense of optimal reactive power compensation. [Figure 46](#) through [Figure 48](#) show the losses of a Vienna rectifier.



**Figure 46.** D1 and D2 conduction losses in a Vienna rectifier.



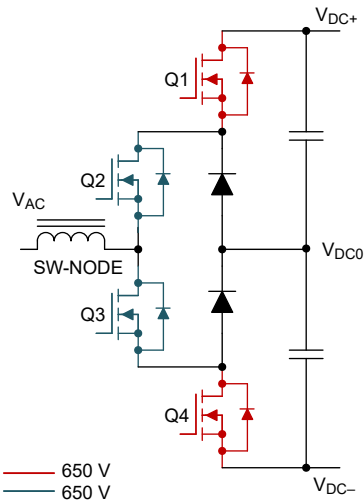
**Figure 47.** Q3 and Q4 conduction losses in a Vienna rectifier.



**Figure 48.** Q3 and Q4 switching losses in a Vienna rectifier.

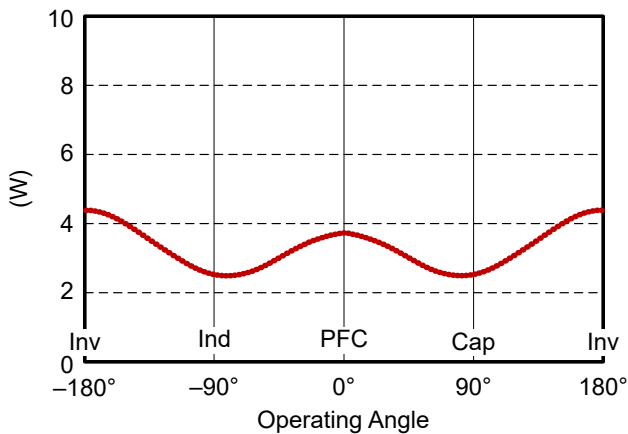
### Three-Level NPC Converters

In a three-level NPC converter with a power rating of 11 kVA, SiC devices were selected with an  $R_{DS(on)}$  of 3 m $\Omega$  and a blocking voltage of 600 V for Q1 and Q2, and for the diodes, SiC Schottky barrier diodes (SBDs) with 30-A and 650-V ratings (see [Figure 49](#)). The converter operates at 98 kHz, thus presenting 130 W of power losses.

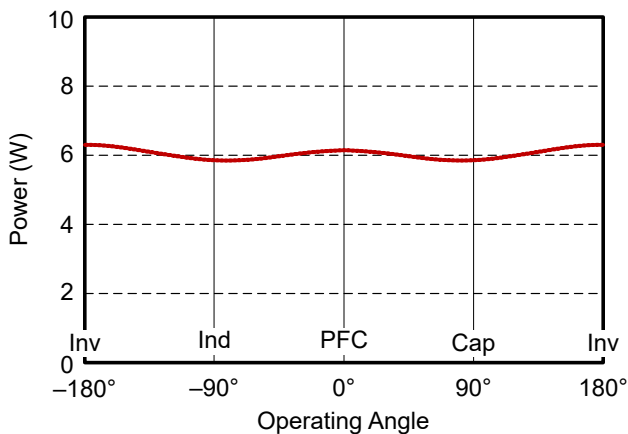


**Figure 49.** Three-level NPC single-leg schematic representation.

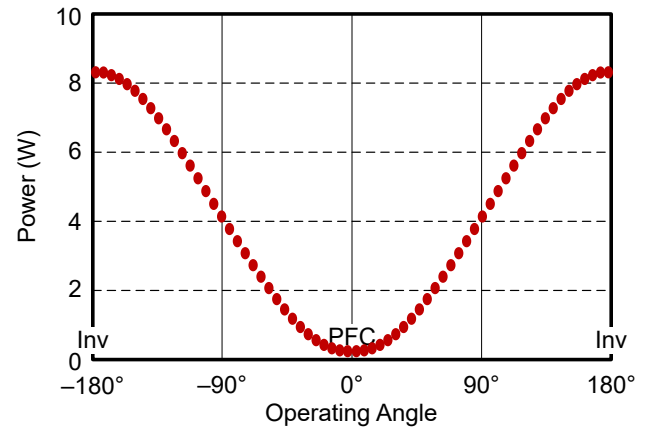
We derived the conduction and switching losses for all of the active components shown in **Figure 49**. **Figure 50** through **Figure 53** show the results.



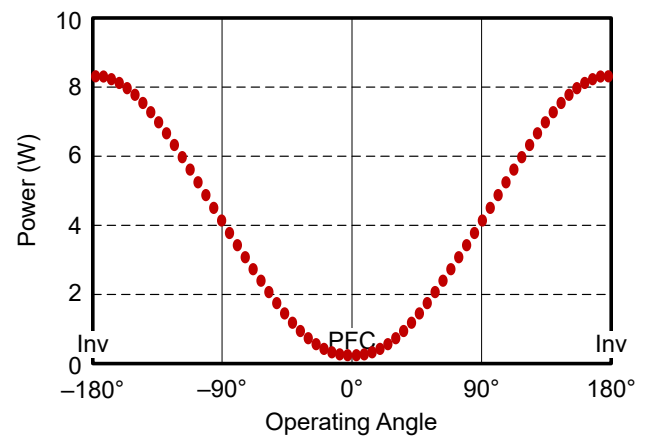
**Figure 50.** Q1 and Q4 conduction losses of an NPC converter as a function of the power factor.



**Figure 51.** Q2 and Q3 conduction losses of an NPC converter as a function of the power factor.



**Figure 52.** Q1 and Q4 switching losses of an NPC converter as a function of the power factor.



**Figure 53.** Q2 and Q3 conduction losses of an NPC converter as a function of the power factor.

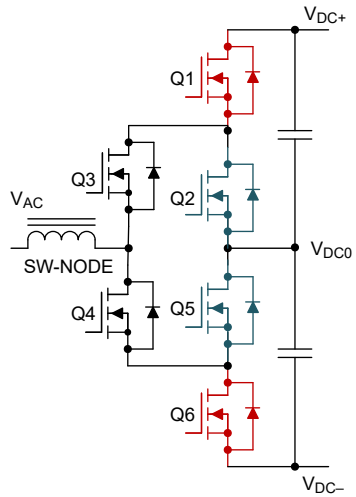
Q1, Q2, Q3 and Q4 are always presenting conduction losses. There is an important difference in the conduction losses of Q1, Q4, Q2 and Q3, caused by the voltage ratio between the grid and DC link. If the voltage on the DC link is higher, Q2 and Q3 will dissipate more power, thus leading to possible overheating of the single device if not properly designed. Based on the AC-to-DC voltage ratio, you can select the right switching devices, as lower  $R_{DS(on)}$  for Q2 and Q3, when having a high AC-to-DC voltage ratio.

The switching loss graphs show that the active devices present equal switching losses at their peak. When the three-level NPC converter operates as a PFC, Q1 and Q4 present no switching losses, allowing you to select low-cost devices beyond SiC. Similarly, when the three-level

NPC converter works only as an inverter, you could use silicon devices for Q2 and Q3.

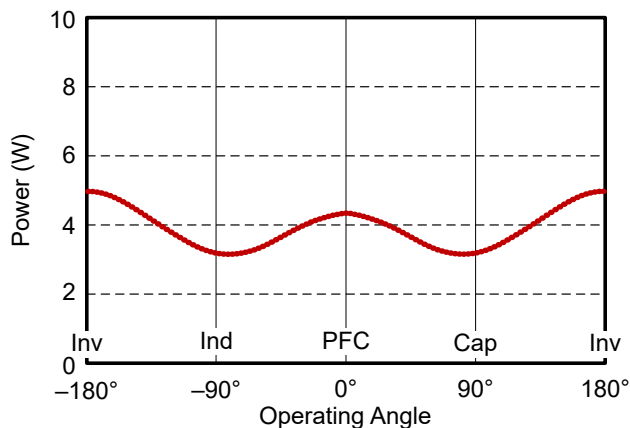
### Three-Level ANPC Converter

For a three-level ANPC converter with a power rating of 11 kVA, we selected SiC devices with an  $R_{DS(on)}$  of 35 m $\Omega$ ; a blocking voltage of 650 V for Q1, Q2, Q5 and Q6 for high-frequency operation; and for low-frequency operation (Q3, Q4), 35-m $\Omega$  and 650-V ratings. See **Figure 54**.

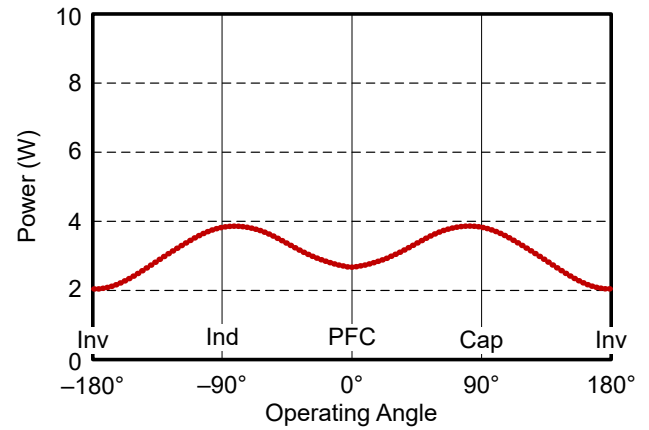


**Figure 54.** Three-level ANPC single-leg schematic representation. All of the components are 600-V-rated and Q1, Q2, Q5 and Q6 are high-frequency switches.

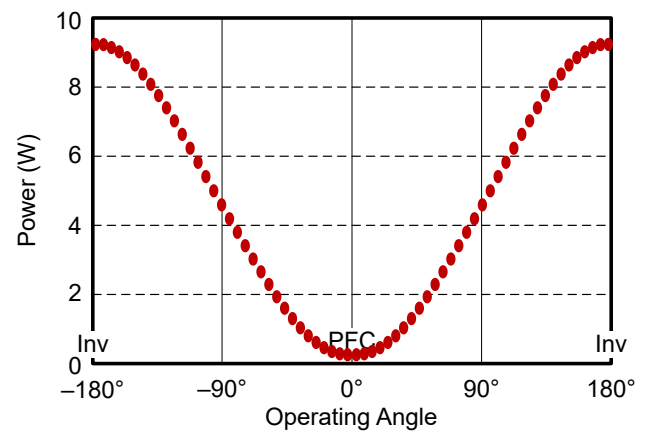
The converter operates at 108 kHz, thus presenting 130 W of power losses. **Figure 55** through **Figure 58** show switching and conduction losses as a function of the power factor.



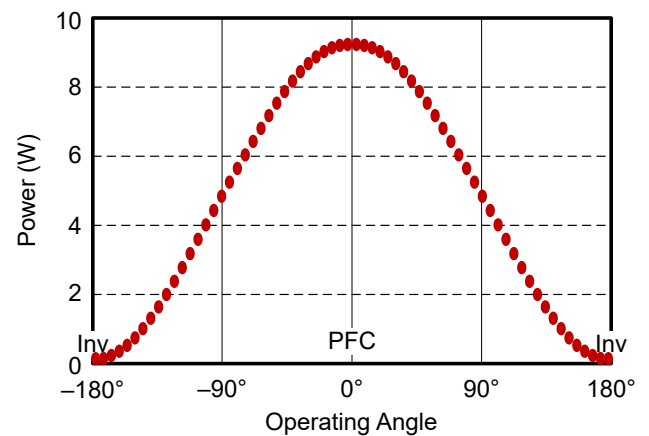
**Figure 55.** Q1 and Q6 conduction losses of an ANPC converter as a function of the power factor.



**Figure 56.** Q2 and Q5 conduction losses of an ANPC converter as a function of the power factor.



**Figure 57.** Q1 and Q6 switching losses of an ANPC converter as a function of the power factor.



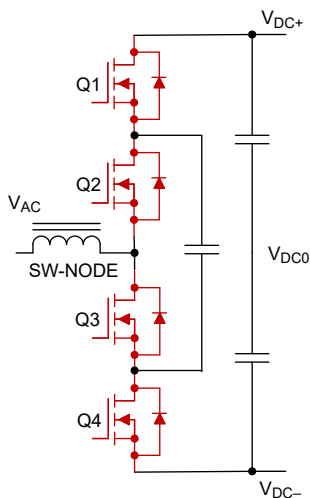
**Figure 58.** Q2 and Q5 switching losses of an ANPC converter as a function of the power factor.

Q1, Q2, Q5 and Q6 are always presenting conduction losses. There is not an important difference in the conduction losses of Q1, Q4 and Q2 and Q3 with respect

to an NPC converter. The switching loss graphs that the active devices present equal switching losses at their peak. When the converter operates as a PFC, Q1 and Q6 present no switching losses, you can select non-SiC devices. Similarly, when the converter works only as an inverter, you can select non-SiC devices for Q2 and Q5.

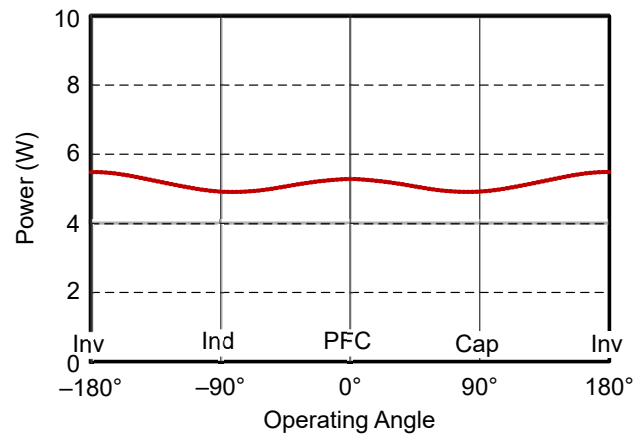
### Three-Level FC Converter

In this topology, we selected 35-m $\Omega$  600-V rated devices for all of the switches. See **Figure 59**. The switching frequency selected for this topology is 69 kHz, which leads to 130 W of power dissipation. The conduction losses for the switches have been extrapolated as shown in **Figure 60**.

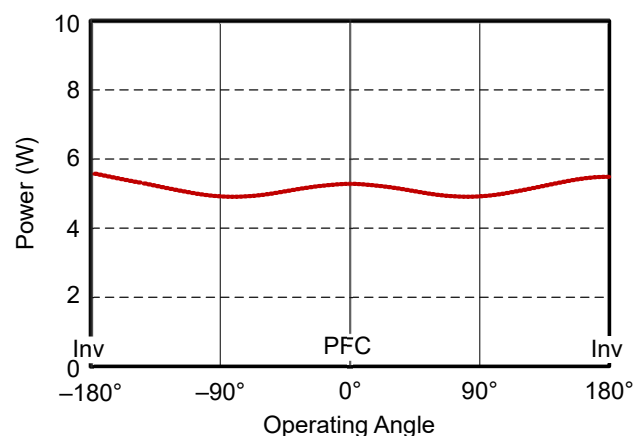


**Figure 59.** Three-level FC single-leg schematic representation. All of the switches are 600-V-rated (Q1, Q2, Q3 and Q4).

From **Figure 60**, you can see that the conduction losses are approximately constant in all four devices and operating modes, thus leading to the conclusion that the losses are optimized across the devices. Derived switching losses (see **Figure 61**) show that there is not a significant difference between PFC and inverter operation.



**Figure 60.** Q1, Q2, Q3 and Q4 conduction losses of an FC converter as a function of the power factor.



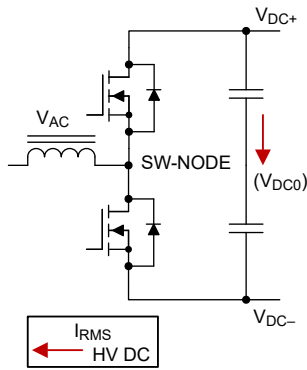
**Figure 61.** Q1, Q2, Q3 and Q4 switching losses of an FC converter as a function of the power factor.

### Ripple Current in the Capacitors

Applying the same methodology proposed in **Applied Methodology**, we ran all of the converters at full power and analyzed the ripple current flowing in the DC link capacitors based on the power factor in order to gather information about film, electrolytic and ceramic capacitors for each converter topology.

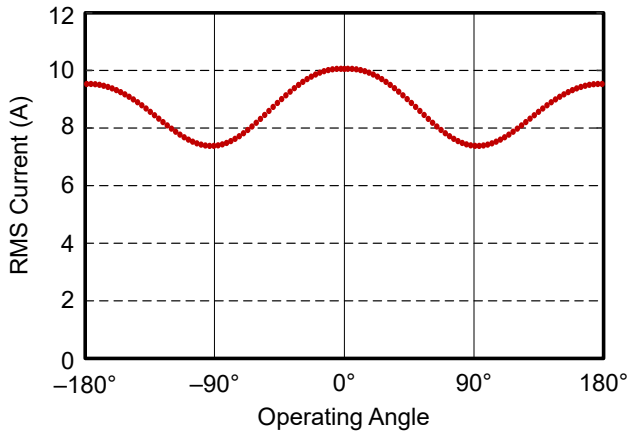
### Two-Level Topology

We ran the two-level converter by changing the power factor, keeping the same RMS current in the grid, and measuring the RMS current flowing in the DC link capacitors; see **Figure 62**. For the two-level converter, we did not notice significant changes in the RMS current flowing in the capacitor.



**Figure 62.** Two-level schematic representation of the current.

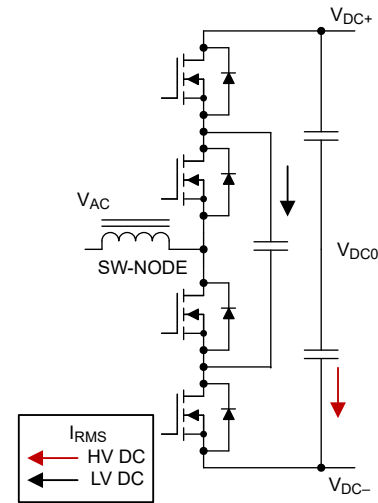
From **Figure 63**, we noticed that the RMS current comprises mostly high frequencies (the low-frequency components are negligible). Thus, film and ceramic capacitors together would be a good combination for designing the DC link capacitors.



**Figure 63.** High-frequency RMS ripple current flowing in the DC link capacitors.

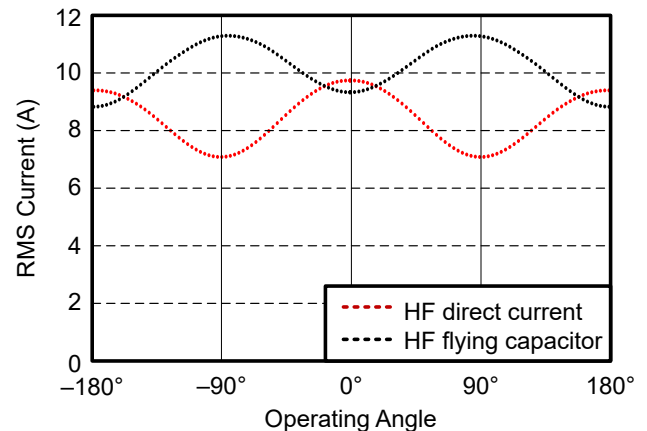
### Three-Level Topology Without the Presence of a DC Middle Point

We ran the three-level FC converter by changing the power factor, keeping the same RMS current in the grid, and measuring the RMS current flowing in the DC link capacitors; see **Figure 64**.



**Figure 64.** Three-level FC schematic representation with current flowing in the DC link and the flying capacitor.

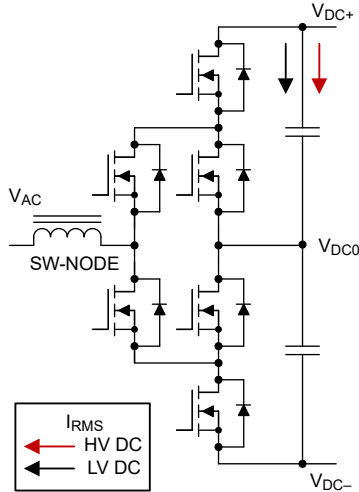
From **Figure 65**, we noticed that the RMS current comprises mostly high frequencies (the low-frequency components are negligible) for both the DC link and FCs. Thus, film and ceramic capacitors together would be a good combination for designing the DC link capacitors. For the FC, selecting ceramic capacitors decreases the parasitic inductances in the power loop.



**Figure 65.** High-frequency ripple current flowing in the DC link capacitors and FC as a function of the power factor.

### Three-Level Topology DC Middle Point

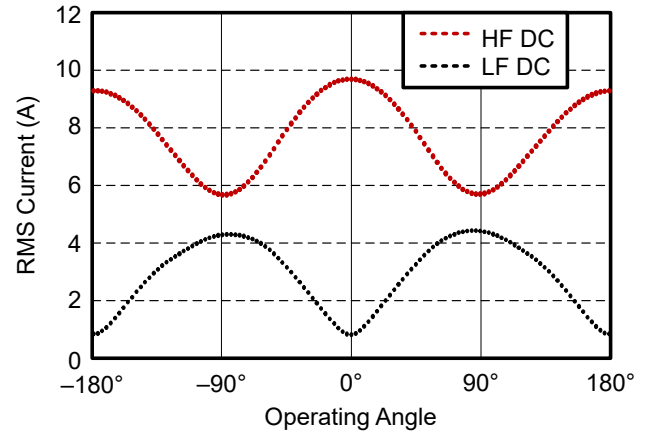
Referencing **Figure 66**, we ran the three-level converters by changing the power factor, keeping the same RMS current in the grid, and measuring the RMS current flowing in the DC link capacitors.



**Figure 66.** Three-level ANPC schematic representation of the current flowing in the DC link.

We achieved the same results for all of the three-level converters with a middle point (VDC0). From **Figure 67**, we observed both high- and low-frequency components in the DC link, indicating the necessity to have ceramic, film and electrolytic capacitors in this

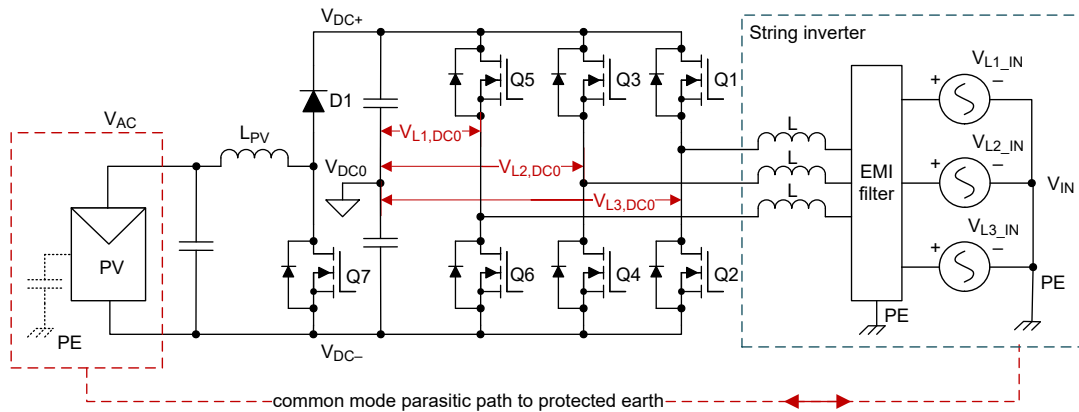
topology. Design optimization is possible whether the converter operates as a PFC or inverter because the low-frequency components are the lowest, thus not requiring many capacitors.



**Figure 67.** Three-level ANPC schematic representation of the current flowing in the DC link with split high- and low-frequency components.

### Common-Mode Noise Comparison

In order to find the common-mode noise voltage, we measured the switching-node voltages with respect to the middle-point reference VDC0. **Figure 68** and **Equation 3** show how we measured and calculated the common-mode noise.



**Figure 68.** Schematic representation of the noise injected by a three-phase inverter into the grid.

$$V_{CM} = \frac{(V_{L1,DC0} + V_{L2,DC0} + V_{L3,DC0})}{3} \quad (3)$$

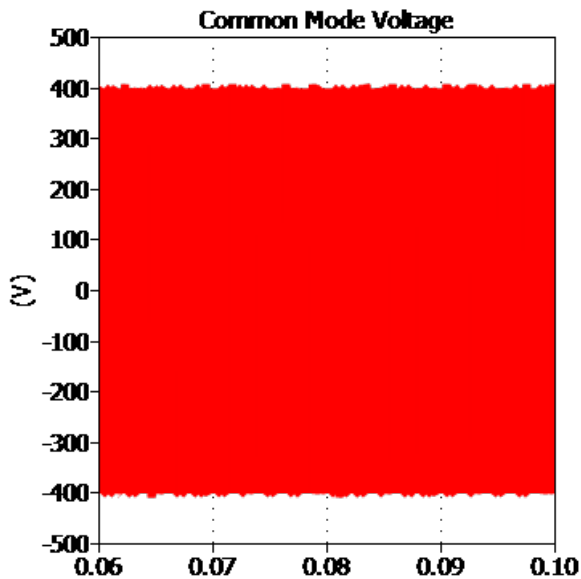


When the three-phase converter switches, it generates a common-mode voltage that creates parasitic currents. Common-mode noise can be significant, especially in photovoltaic applications where surface capacitive coupling to ground is significantly high. The parasitic capacitors of solar panels are typically 200 nF/kWp (kilowatts peak power installed). Large parasitic capacitance can result in issues related to safety and the possible unwanted trigger of the residual current device.

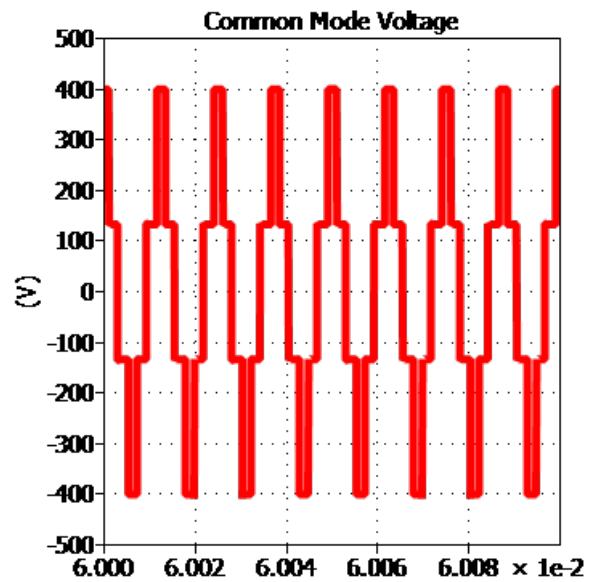
## Two-Level Converters

We conducted various tests at different power factors and loads to determine the impact of the common-mode voltage caused by the DC link voltage and topology type.

**Figure 69** shows the common-mode voltage generated by a two-level converter. **Figure 70** zooms in on a portion of **Figure 69**.



**Figure 69.** Common-mode noise measured when operating a two-level converter.



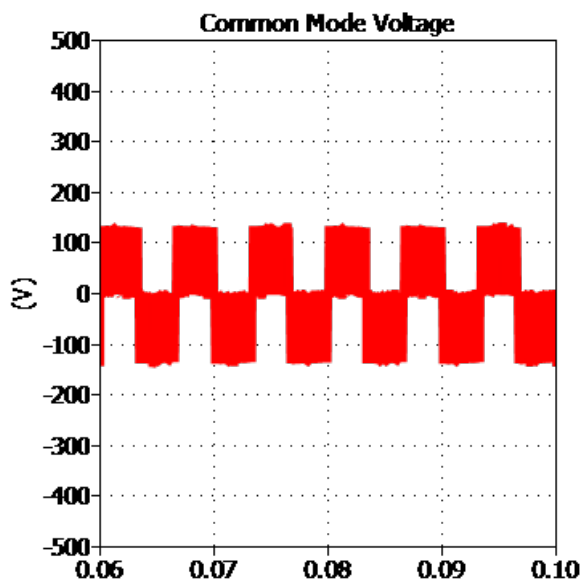
**Figure 70.** Zoomed-in area of **Figure 69**.

We measured a high peak common-mode voltage of 400 V and an RMS voltage of 310 V<sub>RMS</sub> when having a 800-V<sub>DC</sub> link, which could require an oversized common-mode filter to mitigate the high common-mode noise.

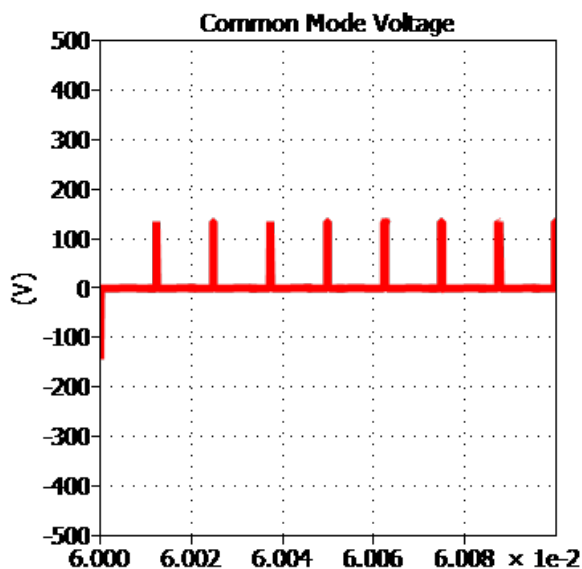
## Three-Level Converters

We conducted various tests at different power factors and loads. In all of the tests, the common-mode voltage was mostly affected by the DC link voltage value and not by the load. We detected no significant differences in the noise between the three-level converters as discussed in this paper.

**Figure 71** shows the common-mode voltage generated by a three-level converter. **Figure 72** zooms in on a portion of **Figure 71**.



**Figure 71.** Common-mode noise measured when operating a three-level converter.



**Figure 72.** Zoomed-in area of Figure 71.

Looking at **Figure 71** and **Figure 72**, there is a high peak voltage of 133 V and an RMS voltage of 74 V<sub>RMS</sub> when having a 800-V<sub>DC</sub> link, which shows a significant improvement in the common-mode noise with respect to a two-level converter. This could help lead to a cost and size reduction of the input and output EMI filter.

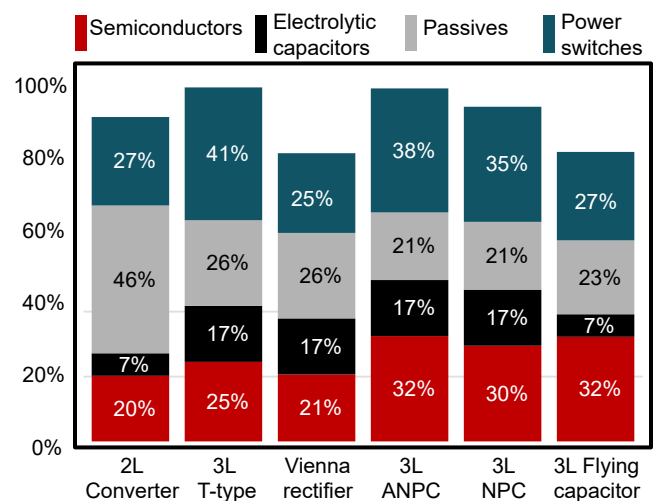
## BOM Comparison

Let's now compare the different boost converter BOM costs, assuming that all topologies deliver about the

same performance with respect to total harmonic distortion, EMI and efficiency.

In **Figure 73**, we grouped the BOM into four categories:

- Power switches: power devices such as high-voltage silicon MOSFETs or SiC MOSFETs.
- Passives: common-mode chokes, film capacitors and PFC inductors.
- Electrolytic capacitors: high-voltage electrolytic capacitors used for DC ripple rejection.
- Semiconductors: gate drivers, isolated power supplies, current-measurement devices, voltage-measurement devices and microcontrollers.



**Figure 73.** BOM comparison.

The reference cost model was the two-level converter, accounting for cost at 100%. The passive components including electrolytic capacitors account for 53% of the relative total cost. The power switches account for only 27%. The Vienna rectifier has lowest relative cost because its passive components, capacitors and switches cost the least. NPC, T-type and ANPC converters have similar costs. The power density of these converters is also comparable. The FC3L offers remarkable cost savings because of its lower passives cost, which makes this topology very attractive for achieving high power density economically.

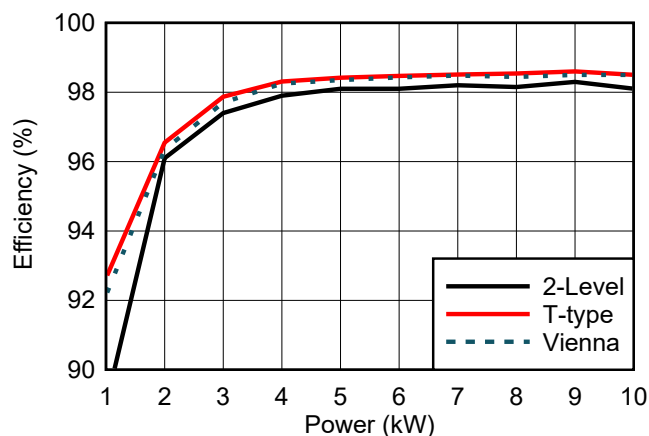
## Experimental Results Comparison

### T-Type and Two-Level Converters and the Vienna Rectifier

We operated the **10-kW, Bidirectional Three-Phase Three-Level (T-Type) Inverter and PFC Reference Design** as a two- and three-level converter and a Vienna rectifier. This is a converter rated for 11 kW. We ran the converter at 800 V and 50 kHz in PFC mode.

The specifications when operating as a T-type converter were 650 V, 60 mΩ (SiC) and 1,200 V, 75 mΩ (SiC). The specifications when operating as a two-level converter were 1,200 V, 75 mΩ (SiC). The specifications when operating as a Vienna rectifier were 1,200 V, 40 A (SBD SiC) and 650 V, 60 mΩ (SiC).

**Figure 74** shows the efficiency curves obtained during the experiments.



**Figure 74.** Efficiency results when having the 10-kW, Bidirectional Three-Phase Three-Level (T-Type) Inverter and PFC Reference Design operating as a T-type, 2-level and Vienna rectifier.

For all power ratings, we achieved an efficiency higher than 98%. The T-type converter and Vienna rectifier have higher efficiencies compared to two-level converters because the switches are presenting lower switching losses thanks to the half switching voltage. At higher loads, the T-type converter shows superior performance thanks to the synchronous rectification feature.

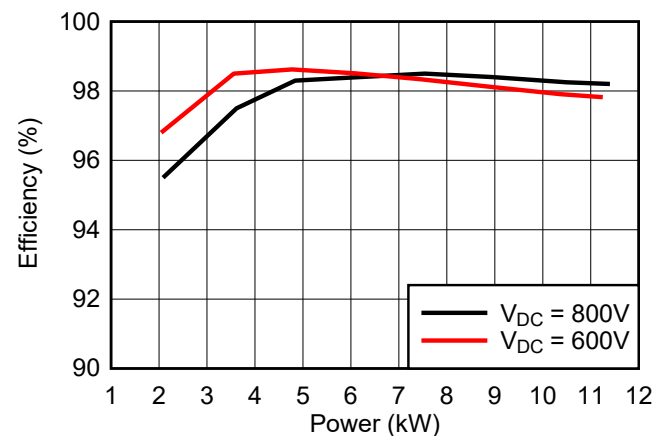
### ANPC Operating with the PWM 1 Technique

We operated the **11-kW, Bidirectional, Three-Phase ANPC Based on GaN Reference Design** as a three-level converter. This is also a converter rated for 11 kW. We ran the converter at 800 V and 100 kHz in PFC mode.

The specifications during operation were:

- Silicon superjunction MOSFETs for the low-frequency switches (40-mΩ, 600-V ratings).
- GaN for the high-frequency switches (30-mΩ, 600-V GaN).

**Figure 75** shows the efficiency curves obtained during the experiments.



**Figure 75.** Efficiency results when having the 11-kW, Bidirectional, Three-Phase ANPC Based on GaN Reference Design operating as a ANPC converter operating PWM technique 1.

At a higher DC link voltage and low loads, the efficiency is lower. On the other hand, at higher DC link voltages and high loads, the efficiency improves significantly.

## Conclusions

Multilevel topologies have smaller passives that offer as much as a 50% reduction in size for a three-level inverter vs. a two-level inverter. They enable FETs with significantly lower switching and conduction losses, which improves efficiency by using FETs with half the blocking voltage for the same DC bus voltage. All three-level topologies keep the switching voltage to half of a two-level inverter, which reduces overall EMI.

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