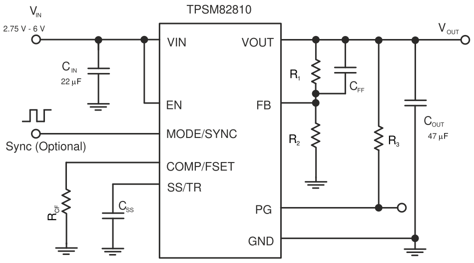
TPSM8281x 2.75V to 6V Input, 4A and 3A Step-Down Power Module With Integrated Inductor and Frequency Synchronization in QFN and MagPack™ Package

1 Features

- Adjustable and synchronizable switching frequency of 1.8MHz to 4MHz
- Two package types
  - µSIL 14-pin with 2.4mm maximum height
  - EMI reduced MagPack 13-pin with 2.0mm maximum height
- Spread spectrum clocking - optional
- Selectable forced PWM or PFM/PWM operation
- Output voltage accuracy ±1% (PWM operation)
- 2.75V to 6V input voltage range
- 0.6V to 5.5V output voltage range
- Adjustable soft start or tracking
- Power-good output with window comparator
- Precise ENABLE input allows
  - User-defined undervoltage lockout
  - Exact sequencing
- Optimized for low EMI
  - MagPack shielded package available
  - Eliminated bond wires
  - Optimized pinout for simple PCB layout
- 100% duty cycle
- Output discharge
- 15µA typical quiescent current
- Excellent thermal performance
- –40°C to 125°C operating temperature range
- Create a custom design using the TPSM828303 with the WEBENCH® Power Designer

2 Applications

- Optical modules, data center interconnect
- Signal measurement, source generation, instrumentation
- Patient monitoring and diagnostics
- Wireless infrastructure
- Ruggedized Communication: sensors, imaging, and radar



Schematic

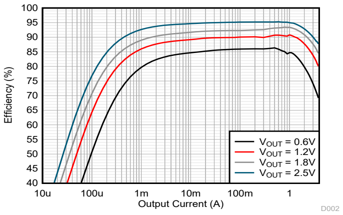
3 Description

TPSM8281x is a family of pin-to-pin, 3A and 4A compatible, high-efficiency, and easy to use synchronous step-down DC/DC power modules with integrated inductors. The devices are based on a fixed-frequency peak current-mode control topology and they support high power density requirements for telecommunication, test and measurement, and medical applications. Low resistance switches allow up to 4A continuous output current at high ambient temperatures. The switching frequency is externally adjustable from 1.8MHz to 4MHz and can also be synchronized to an external clock in the same frequency range. In PFM/PWM mode, the TPSM8281x maintains high efficiency across the whole load range. The TPSM8281x provide 1% output voltage accuracy in PWM mode, which enables designing power supplies with high output voltage accuracy. The SS/TR pin helps limiting inrush current through a precise start-up ramp. It also supports sequencing by tracking the output voltage to an external source. The family is available in a 14-pin µSIL package with nominal 3.0mm × 4.0mm footprint and in a 13-pin MagPack package with nominal 2.5mm × 3.0mm footprint.

Device Information

PART NUMBER[3]	OUTPUT CURRENT	PACKAGE[1]	PACKAGE SIZE[2]
TPSM82810	4A	SIL (µSiL, 14)	3.0mm × 4.0mm
TPSM82813	3A	SIL (µSiL, 14)	3.0mm × 4.0mm
		VCA (QFN, 13)[4]	2.5mm × 3.0mm
TPSM82812[5]	2A	VCA (QFN, 13)	2.5mm × 3.0mm
TPSM82811[5]	1A		

(1) For more information, see Section 12.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) See the *Device Comparison Table*.
(4) Advance information (not production data).
(5) Preview information (not production data).



Efficiency vs Output Current; V_{IN} = 3.3V; PFM; VCA Package; T_A = 25°C

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4 Device Comparison Table

DEVICE NUMBER	OUTPUT CURRENT	SPREAD SPECTRUM CLOCKING
TPSM8281**0**SILR	4A	OFF
TPSM8281**0S**SILR	4A	ON
TPSM8281**3**SILR	3A	OFF
TPSM8281**3S**SILR	3A	ON
TPSM8281**3P**VCAR(1)	3A	OFF
TPSM8281**2P**VCAR(2)	2A	OFF
TPSM8281**1P**VCAR(2)	1A	OFF

(1) Advance information (not production data).
(2) Preview information (not production data).

5 Pin Configuration and Functions

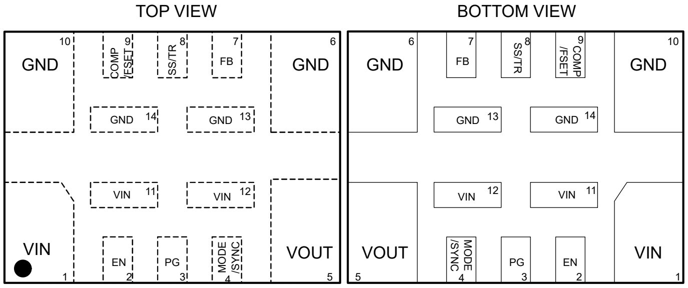


Figure 5-1. SIL Package, 14-Pin µSiL

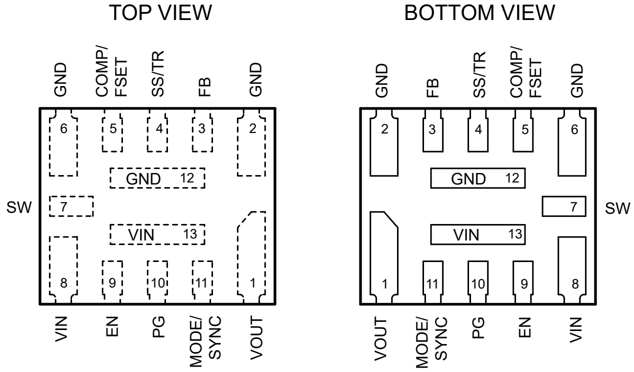


Figure 5-2. VCA Package, 13-Pin QFN

Table 5-1. Pin Functions

PIN			TYPE[1]	DESCRIPTION
NAME	SIL	VCA		
EN	2	9	I	This pin is the enable pin of the device. Connect to logic low to disable the device. Pull high to enable the device. Do not leave this pin unconnected.
FB	7	3	I	Voltage feedback input. Connect the output voltage resistor divider to this pin.
GND	6, 10, 13, 14	2, 6, 12		Ground pin
MODE/ SYNC	4	11	I	The device runs in PFM/PWM mode when this pin is pulled low. When the pin is pulled high, the device runs in forced PWM mode. Do not leave this pin unconnected. The MODE/SYNC pin can also be used to synchronize the device to an external frequency. See *Section 9.3.2*.
COMP/ FSET	9	5	I	Device compensation and frequency set input. A resistor from this pin to GND defines the compensation of the control loop as well as the switching frequency if not externally synchronized. The switching frequency is set to 2.25 MHz if the pin is tied to GND or VIN. See Table 8-1. Do not leave this pin unconnected.
PG	3	10	O	Open-drain power-good output with window comparator. This pin is pulled to GND while VOUT is outside the power-good threshold. This pin can be left open or tied to GND if not used. A pullup resistor can be connected to any voltage not larger than VIN.
SS/TR	8	4	I	Soft-start, tracking pin. A capacitor connected from this pin to GND defines the output voltage rise time. The pin can also be used as an input for tracking and sequencing - see *Voltage Tracking*.
VOUT	5	1		Output voltage pin. This pin is internally connected to the integrated inductor.
VIN	1, 11, 12	8, 13		Power supply input. Connect the input capacitor as close as possible between the VIN and GND pins.
SW	—	7	O	Switch pin of the power stage. This pin can be left floating.

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

Over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Pin voltage	VIN, VOUT, EN, MODE/SYNC	-0.3	6.5	V
Pin voltage	FB	-0.3	4	V
Pin voltage	PG, SS/TR, COMP/FSET	-0.3	V_{IN}+0.3	V
I_{SINK_PG}	Sink current at PG pin		10	mA
T_J	Operating junction temperature	-40	125	°C
T_{stg}	Storage temperature	-40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage range	2.75		6	V
V_{OUT}	Output voltage range	0.6		5.5	V
C_{OUT}	Effective output capacitance(1)	27	47	470	µF
C_{IN}	Effective input capacitance(1)	5	10		µF
R_{CF}		4.5		100	kΩ
T_J	Operating junction temperature	-40		125	°C

(1) The values given for all the capacitors in the table are effective capacitance, which includes the DC bias effect. Due to the DC bias effect of ceramic capacitors, the effective capacitance is lower than the nominal value when a voltage is applied. Please check the manufacturer´s DC bias curves for the effective capacitance vs DC voltage applied. Please see Section 9.3.3 about the output capacitance vs compensation setting and output voltage.

6.4 Thermal Information

THERMAL METRIC(1)		TPSM8281x µSIL (JEDEC 51-5) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	12.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report and Section 12.3 - Thermal Consideration.

6.5 Thermal Information

THERMAL METRIC[1]		TPSM8281x	UNIT
		VCA (JEDEC 51-5)	
		13 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.0	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	(-1.4)[2]	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report and Section 12.3 - Thermal Consideration.

(2) Case top temperature can be higher than temperature of active circuit because of inductor power dissipation. This results in a negative Junction-to-top characterization parameter.

6.6 Electrical Characteristics

Over operating junction temperature (T_J = -40 °C to +125 °C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Operating Quiescent Current	EN = high, I_{OUT}= 0 mA, Device not switching		15	21	µA
I_{SD}	Shutdown Current	EN = 0 V		0.11	18	µA
V_{UVLO}	Undervoltage Lockout Threshold	Rising Input Voltage	2.5	2.6	2.75	V
		Falling Input Voltage	2.25	2.5	2.6	V
T_{SD}	Thermal Shutdown Temperature	Rising Junction Temperature		170		°C
	Thermal Shutdown Hysteresis			15		
CONTROL (EN, SS/TR, PG, MODE/SYNC)						
V_{IH}	High Level Input Voltage for MODE/ SYNC Pin		1.1			V
V_{IL}	Low Level Input Voltage for MODE/ SYNC Pin				0.3	V
f_{SYNC}	Frequency Range on MODE/SYNC Pin for Synchronization		1.8		4	MHz
	Duty Cycle of Synchronization Signal at MODE/SYNC Pin		40%	50%	60%	
V_{IH}	Input Threshold Voltage for EN pin	Rising EN	1.06	1.1	1.15	V
V_{IL}	Input Threshold Voltage for EN pin	Falling EN	0.96	1.0	1.05	V
I_{LKG}	Input Leakage Current for EN, MODE/ SYNC Pins	EN, MODE/SYNC = V_{IN} or GND			150	nA
V_{TH_PG}	UVP Power Good Threshold	Rising (%V_{FB})	92%	95%	98%	
	UVP Power Good Threshold	Falling (%V_{FB})	87%	90%	93%	
	OVP Power Good Threshold	Rising (%V_{FB})	107%	110%	113%	
	OVP Power Good Threshold	Falling (%V_{FB})	104%	107%	111%	
	Power Good De-glitch Time	for a high level to low level transition on power good		40		µs
V_{OL_PG}	Power Good Output Low Voltage	I_{PG} = 2 mA		0.07	0.3	V
I_{LKG_PG}	Input Leakage Current for PG Pin	V_{PG} = 5 V			100	nA
$I_{SS/TR}$	SS/TR Pin Source Current		2.1	2.5	2.8	µA
	Tracking Gain	V_{FB} / $V_{SS/TR}$		1		
	Tracking Offset	FB pin with $V_{SS/TR}$ = 0 V		17		mV
POWER SWITCH						
$R_{DS(ON)}$	High-Side MOSFET ON-Resistance	$V_{IN} \geq 5$ V		37	60	mΩ

6.6 Electrical Characteristics (continued)

Over operating junction temperature (T_J = -40 °C to +125 °C) and V_{IN} = 2.75 V to 6 V. Typical values at V_{IN} = 5 V and T_J = 25 °C. (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DS(ON)}$	Low-Side MOSFET ON-Resistance	$V_{IN} \geq 5$ V		15	35	mΩ
R_{DP}	Dropout resistance	100% mode. Maximum value at V_{IN} = 3.3V, T_J = 85°C		50	90	mΩ
I_{LIMH}	High-Side MOSFET Current Limit (1)	TPSM82810; V_{IN} = 3 V to 6 V	4.8	5.6	6.55	A
I_{LIMH}	High-Side MOSFET Current Limit(1)	TPSM82813; V_{IN} = 3V to 6 V	3.9	4.5	5.25	A
I_{LIMNEG}	Negative Current Limit (1)	MODE/SYNC = HIGH		-1.8		A
f_S	PWM Switching Frequency Range		1.8	2.25	4	MHz
f_S	PWM Switching Frequency	with COMP/FSET tied to VIN or GND	2.025	2.25	2.475	MHz
	PWM Switching Frequency Tolerance	using a resistor from COMP/FSET to GND	-19%		18%	
$t_{on,min}$	Minimum on-time	V_{IN} = 3.3 V		50	75	ns
$t_{off,min}$	Minimum off-time	V_{IN} = 3.3 V		30		ns
OUTPUT						
V_{FB}	Feedback Voltage Accuracy	$V_{IN} \geq V_{OUT}$ + 1 V; PWM mode	594	600	606	mV
		$V_{IN} \geq V_{OUT}$ + 1 V; PFM mode $V_{OUT} \geq$ 1.5 V; $C_{OUT,eff} \geq$ 27µF	594	600	612	mV
		1 V ≤ V_{OUT} < 1.5 V; PFM mode $C_{OUT,eff} \geq$ 47µF	594	600	615	mV
I_{LKG_FB}	Input Leakage Current (FB pin)	V_{FB} = 0.6 V		1	70	nA
V_{FB}	Feedback Voltage Accuracy with Voltage Tracking	$V_{IN} \geq V_{OUT}$ + 1 V; PWM mode $V_{SS/TR}$ = 0.3 V	297	300	321	mV
R_{dis}	Output Discharge Resistance			30	50	Ω
t_{delay}	Start-up Delay Time	I_{OUT} = 0 mA, Time from EN=high to start switching; V_{IN} applied already	135	200	450	µs
t_{ramp}	Ramp time; SS/TR Pin Open	I_{OUT} = 0 mA, Time from first switching pulse until 95% of nominal output voltage	100	150	200	µs

(1) This is the static current limit. It can be temporarily higher in applications due to internal propagation delay (see Current Limit And Short Circuit Protection section).

6.7 Typical Characteristics

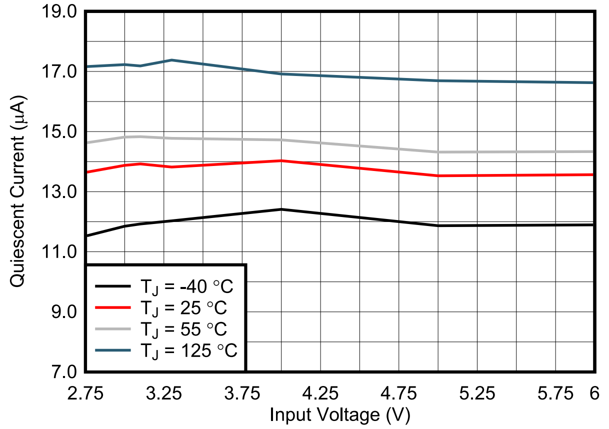


Figure 6-1. Quiescent Current

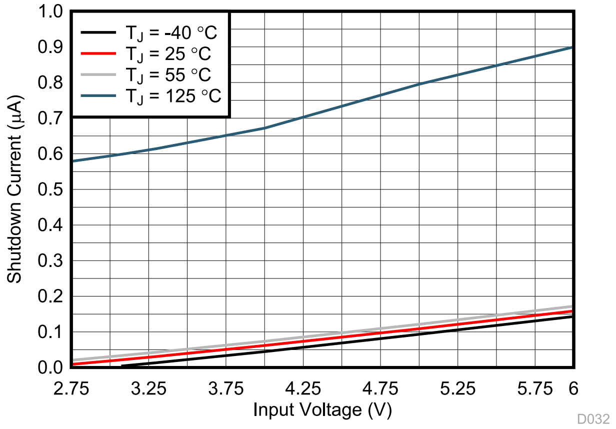


Figure 6-2. Shutdown Current

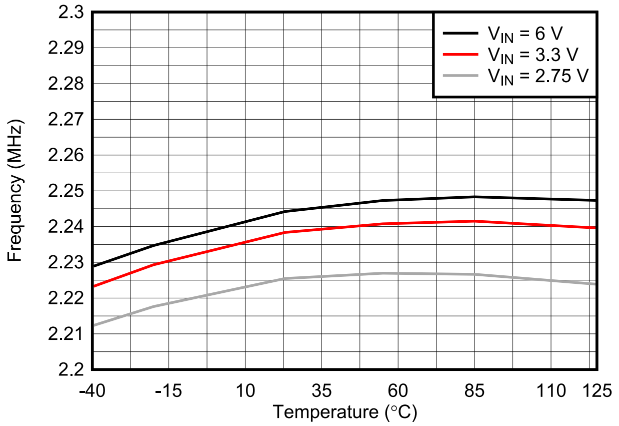


Figure 6-3. Oscillator Frequency vs Temperature (COMP/FSET tied to VIN or GND)

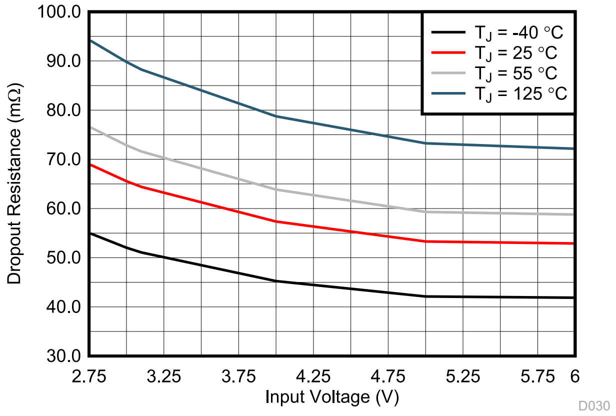


Figure 6-4. Dropout Resistance

7 Parameter Measurement Information

7.1 Schematic

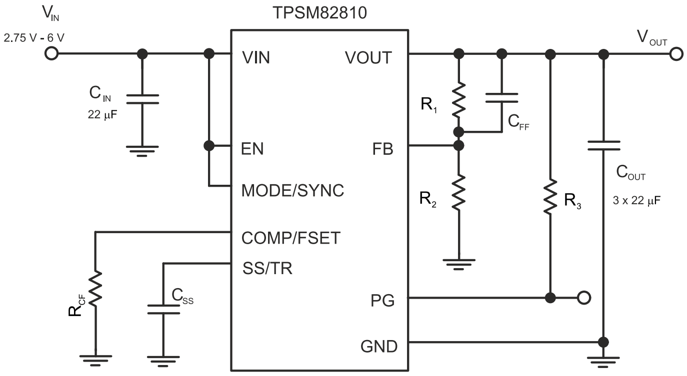


Figure 7-1. Measurement Setup for TPSM8281x

Table 7-1. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER (1)
IC	TPSM82810 or TPSM82813	Texas Instruments
C_{IN}	22µF / X7T / 10V; GRM21BD71A226ME44	Murata
C_{OUT}	3 x 22µF / X7T / 10V; GRM21BD71A226ME44	Murata
C_{SS}	4.7nF	Any
R_{CF}	10kΩ	Any
C_{FF}	10pF	Any
R_1	Depending on VOUT	Any
R_2	Depending on VOUT	Any
R_3	100kΩ	Any

(1) See the *Third-party Products Disclaimer*.

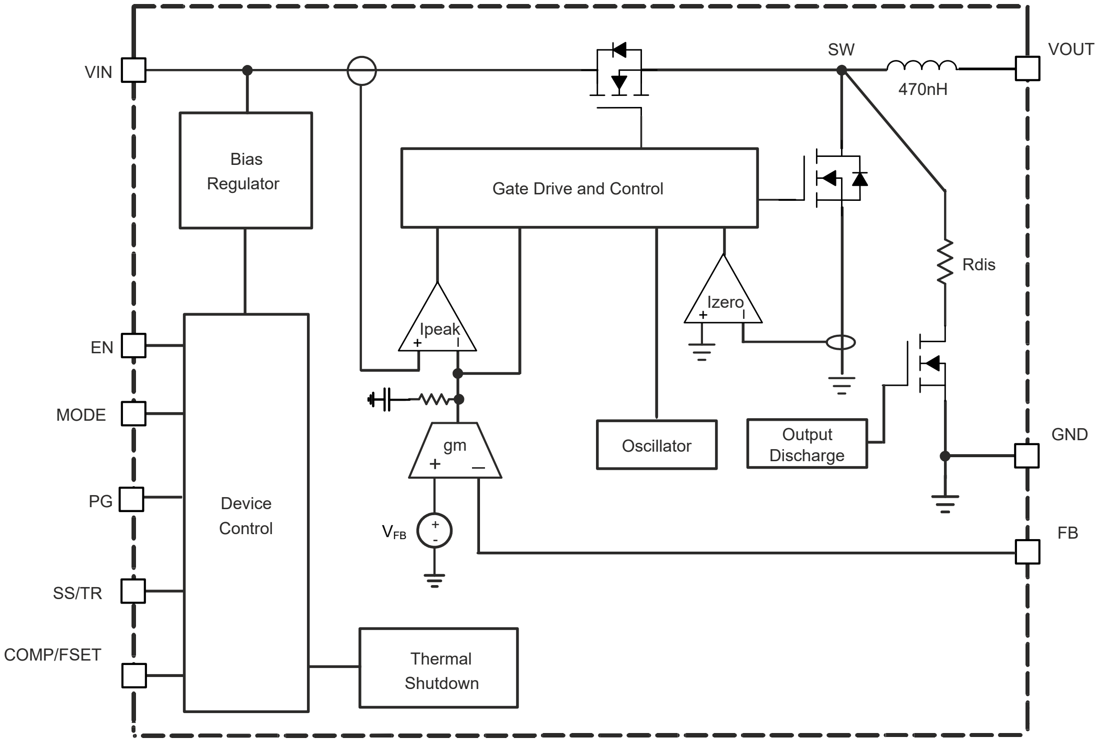
8 Detailed Description

8.1 Overview

The TPSM8281x synchronous switch mode DC/DC converter power modules are based on a fixed-frequency peak current-mode control topology. The control loop is internally compensated. To optimize the bandwidth of the control loop to the wide range of output capacitance that can be used with the TPSM8281x, one of three internal compensation settings can be selected. See *Section 8.3.3*. The compensation setting is selected either by a resistor from COMP/FSET to GND, or by the logic state of this pin. The regulation network achieves fast and stable operation with small external components and low-ESR ceramic output capacitors.

The devices support fixed-frequency forced PWM operation with the MODE/SYNC pin tied to a logic high level. When the MODE/SYNC pin is set to a logic low level, the device operates in power save mode (PFM) at low-output currents and automatically transitions to fixed-frequency PWM mode at higher output currents. In PFM mode, the switching frequency decreases linearly based on the load to sustain high efficiency down to very low output currents. The device can be synchronized to an external clock signal in a range from 1.8MHz to 4MHz applied to the MODE/SYNC pin.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Precise Enable (EN)

The TPSM8281x starts operation when the rising EN threshold is exceeded. For proper operation, the EN pin must be terminated and must not be left floating. Pulling the EN pin low forces the device into shutdown. In this mode, the internal high-side and low-side MOSFETs are turned off and the entire internal control circuitry is switched off. The voltage applied at the EN pin of the TPSM8281x is compared to a fixed threshold of 1.1V for a rising voltage.

The enable input threshold for a falling edge is typically 100mV lower than the rising edge threshold. The Precise Enable input provides a user-programmable undervoltage lockout by adding a resistor divider to the input of the EN pin. The Precise Enable input also allows you to drive the pin by a slowly changing voltage and enables the use of an external RC network to achieve a precise power-up delay. See the *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold* analog design journal for more details.

8.3.2 Output Discharge

The purpose of the discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and keep the output voltage close to 0V when the device is off. The output discharge feature is only active once the TPSM8281x has been enabled at least once since the supply voltage was applied. The discharge function is enabled as soon as the device is disabled, in thermal shutdown, or in undervoltage lockout. The minimum supply voltage required for the discharge function to remain active is typically 1V.

8.3.3 COMP/FSET

This pin sets two different parameters independently:

- Internal compensation settings for the control loop (three settings available)
- The switching frequency in PWM mode from 1.8MHz to 4MHz

A resistor from COMP/FSET to GND changes the compensation as well as the switching frequency. The change in compensation adapts the device to different values of output capacitance. The resistor must be placed close to the pin to keep the parasitic capacitance on the pin to a minimum. The compensation setting is set after enabling the converter, so a change in the resistor during operation only has an effect on the switching frequency but not on the compensation.

To save external components, the pin can also be directly tied to VIN or GND to set a pre-defined switching frequency and compensation. Do not leave the pin floating.

The switching frequency must be selected based on the maximum input voltage and the output voltage to meet the specifications for the minimum on-time. Using V_{IN} = 5.5V and V_{OUT} = 1.1V as an example, the minimum duty cycle given with Equation 1 is 0.2, which results in a maximum switching frequency of 2.67MHz according to Equation 2.

$$D_{min} = \frac{V_{OUT}}{V_{IN,\,max}} \tag{1}$$

$$f_{s,\,max} = \frac{1}{t_{on,\,min} \times D_{min}} \tag{2}$$

The compensation range has to be chosen based on the minimum effective capacitance used. The capacitance can be increased from the minimum value as given in Table 8-1 up to the maximum of 470µF in all of the three compensation ranges. If the capacitance of an output changes during operation, for example, when load switches are used to connect or disconnect parts of the circuitry, the compensation has to be chosen for the minimum capacitance on the output. With large output capacitance, the compensation must be done based on that large capacitance to get the best load transient response. Compensating for large output capacitance but placing less capacitance on the output can lead to instability.

The switching frequency for the different compensation setting is determined by the following equations.

For compensation (comp) setting 1:

$$R_{CF}(k\Omega) = \frac{18 MHz \cdot k\Omega}{f_S(MHz)} \tag{3}$$

For compensation (comp) setting 2:

$$R_{CF}(k\Omega) = \frac{60MHz \cdot k\Omega}{f_S(MHz)} \quad (4)$$

For compensation (comp) setting 3:

$$R_{CF}(k\Omega) = \frac{180MHz \cdot k\Omega}{f_S(MHz)} \quad (5)$$

Table 8-1. Switching Frequency and Compensation

COMPENSATION	R_{CF}	SWITCHING FREQUENCY	MINIMUM OUTPUT CAPACITANCE FOR VOUT < 1V	MINIMUM OUTPUT CAPACITANCE FOR 1V ≤ VOUT < 3.3V	MINIMUM OUTPUT CAPACITANCE FOR VOUT ≥ 3.3V
for smallest output capacitance (comp setting 1)	10kΩ ... 4.5kΩ	1.8MHz (10kΩ) ... 4MHz (4.5kΩ) according to Equation 3	53µF	32µF	27µF
for medium output capacitance (comp setting 2)	33kΩ ... 15kΩ	1.8MHz (33kΩ) ... 4MHz (15kΩ) according to Equation 4	100µF	60µF	50µF
for large output capacitance (comp setting 3)	100kΩ ... 45kΩ	1.8MHz (100kΩ) ... 4MHz (45kΩ) according to Equation 5	200µF	120µF	100µF
for smallest output capacitance (comp setting 1)	tied to GND	internally fixed 2.25MHz	53µF	32µF	27µF
for large output capacitance (comp setting 3)	tied to V_{IN}	internally fixed 2.25MHz	200µF	120µF	100µF

Refer to *Section 9.2.2.5* for further details on the output capacitance required depending on the output voltage. All values are the effective value of capacitance.

A too high resistor value for R_{CF} is read as "tied to V_{IN}", and a value below the lowest range as "tied to GND". The minimum output capacitance in Table 8-1 is for capacitors close to the output of the device. If the capacitance is distributed, a lower compensation setting can be required.

8.3.4 MODE/SYNC

When MODE/SYNC is set low, the device operates in PWM or PFM mode, depending on the output current. The MODE/SYNC pin forces PWM mode when set high. The pin also allows you to apply an external clock in a frequency range from 1.8MHz to 4MHz for external synchronization. When an external clock is applied, the device operates in PWM mode. As with the switching frequency selection, the specification for the minimum on-time has to be observed when applying the external clock signal. When using external synchronization, it is recommended to set the internal switching frequency as set by R_{CF} to a similar value as the externally applied clock. This ensures that, if the external clock fails, the switching frequency stays in the same range and the settling time to the internal clock is reduced. When there is no resistor from COMP/FSET to GND, but the pin is pulled high or low, external synchronization is not possible. An internal PLL allows you to change from an internal clock to external clock during operation. The synchronization to the external clock is done on the falling edge of the applied clock to the rising edge of the internal SW pin. The MODE/SYNC pin can be changed during operation.

8.3.5 Spread Spectrum Clocking (SSC) - TPSM8281xS

These devices offer spread spectrum clocking, where the switching frequency is randomly changed in PWM mode when the internal clock is used. The frequency variation is typically between the nominal switching frequency and up to 288kHz above the nominal switching frequency. When the device is externally synchronized, the TPSM8281xS follows the external clock and the internal spread spectrum block is turned off. SSC is also disabled during soft start.

8.3.6 Undervoltage Lockout (UVLO)

If the input voltage drops, the undervoltage lockout prevents mis-operation of the device by switching off both the MOSFETs. The device is fully operational for voltages above the rising UVLO threshold and turns off if the input voltage goes below the falling threshold.

8.3.7 Power-Good Output (PG)

The device has a power good output with window comparator. The PG pin goes high impedance after the FB pin voltage is above 95% and less than 107% of the nominal voltage, and is driven low after the voltage falls below typically 90% or higher than 110% of the nominal voltage. Table 8-2 shows the typical PG pin logic. The PG pin is an open-drain output and is specified to sink up to 2mA. The power good output requires a pullup resistor connected to any voltage rail less than VIN. The PG signal can be used for sequencing of multiple rails by connecting to the EN pin of other converters. If not used, the PG pin can be left floating or connected to GND.

Table 8-2. Power Good Pin Logic

DEVICE STATE		PG LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enabled (EN = High)	$0.57V \le V_{FB} \le 0.642V$	√	
	$V_{FB} < 0.54V$ or $V_{FB} > 0.66V$		√
Shutdown (EN = Low)			√
UVLO	$2V \le V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{JSD}$		√
Power Supply Removal	$V_{IN} < 2V$	√	

The PG pin has a 40µs deglitch time on the falling edge.

8.3.8 Thermal Shutdown

The junction temperature (T_J) of the device is monitored by an internal temperature sensor. If T_J exceeds 170°C (typ), the device goes into thermal shutdown. Both the high-side and low-side power FETs are turned off and PG goes low. When T_J decreases below the hysteresis amount of typically 15°C, the converter resumes normal operation, beginning with soft start. During PFM, the thermal shutdown is not active.

8.4 Device Functional Modes

8.4.1 Pulse Width Modulation (PWM) Operation

The TPSM8281x has two operating modes: Forced PWM mode and PFM/PWM mode.

With the MODE/SYNC pin set to high, the TPSM8281x operates with pulse width modulation in continuous conduction mode (CCM). The switching frequency is either defined by a resistor from the COMP/FSET pin to GND or by an external clock signal applied to the MODE/SYNC pin.

8.4.2 Power Save Mode Operation (PFM/PWM)

When the MODE/SYNC pin is low, power save mode is allowed. The device operates in PWM mode as long as the peak inductor current is above the PFM threshold of about 1.2A. When the peak inductor current drops below the PFM threshold, the device starts to skip switching pulses.

In power save mode, the switching frequency decreases linearly with the load current to maintain high efficiency. The linear behavior of the switching frequency in power save mode is shown in Figure 8-1.

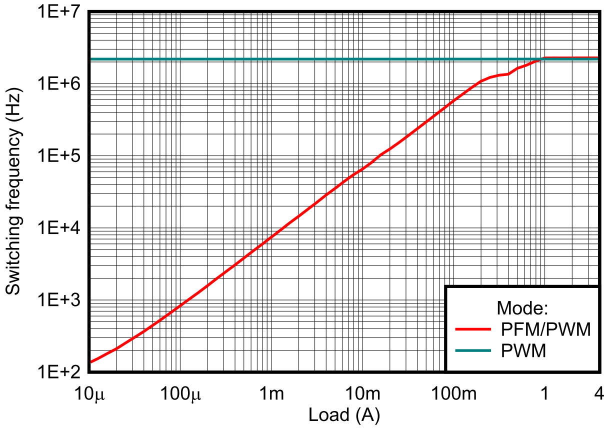


Figure 8-1. Switching Frequency versus Output Current (V_{IN} = 5V, V_{OUT} = 1.8V)

8.4.3 100% Duty-Cycle Operation

The device offers a low input-to-output voltage differential by entering 100% duty cycle mode. When the minimum off-time of typically 30 ns is reached, the TPSM8281x skips switching cycles while it approaches 100% mode. In 100% mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN\ (min)} = V_{OUT\ (min)} + I_{OUT} \times R_{DP} \tag{6}$$

where

- R_{DP} is the resistance from V_{IN} to V_{OUT}, which includes the high-side MOSFET on-resistance and DC resistance of the inductor
- $V_{OUT\ (min)}$ is the minimum output voltage the load can accept

8.4.4 Current Limit and Short Circuit Protection

The TPSM8281x is protected against overload and short circuit events. If the inductor current exceeds the current limit I_{LIMH}, the high-side MOSFET is turned off and the low-side MOSFET is turned on to ramp down the inductor current. The high-side MOSFET turns on again only if the current in the low-side MOSFET has decreased below the low-side current limit. Due to internal propagation delays, the actual current can exceed the static current limit. The dynamic current limit is given as:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_L}{L} \cdot t_{PD} \tag{7}$$

where

- I_{LIMH} is the static current limit, as specified in the electrical characteristics
- L is the effective inductance (typically 470nH)
- V_L is the voltage across the inductor (V_{IN} - V_{OUT})
- t_{PD} is the internal propagation delay of typically 50ns

The dynamic peak current is calculated as follows:

$$I_{peak(typ)} = I_{LIMH} + \frac{V_{IN} - V_{OUT}}{L} \cdot 50ns \tag{8}$$

The low-side MOSFET also contains a negative current limit to prevent excessive current from flowing back through the inductor to the input. If the low-side sinking current limit is exceeded, the low-side MOSFET is turned off. In this scenario, both MOSFETs are off until the start of the next cycle. The negative current limit is only active in Forced PWM mode.

8.4.5 Soft Start / Tracking (SS/TR)

The internal soft-start circuitry controls the output voltage slope during start-up. This control avoids excessive inrush current and makes sure of a controlled output voltage rise time. This control also prevents unwanted voltage drops from high impedance power sources or batteries. When EN is set high, the device starts switching after a delay of about 200µs. Then V_{OUT} rises with a slope controlled by an external capacitor connected to the SS/TR pin.

A capacitor connected from SS/TR to GND is charged with 2.5µA by an internal current source during soft start until the capacitor reaches the reference voltage of 0.6V. After reaching 0.6V, the SS/TR pin voltage is clamped internally while the SS/TR pin voltage keeps rising to a maximum of about 3.3V. The capacitance required to set a certain ramp-time (t_{ramp}) is:

$$C_{SS}\left[nF\right] = \frac{2.5\mu A \cdot t_{ramp}\left[ms\right]}{0.6V} \tag{9}$$

Leaving the SS/TR pin un-connected provides the fastest start-up ramp of 150µs typically. If the device is set to shutdown (EN = GND), undervoltage lockout, or thermal shutdown, an internal resistor pulls the SS/TR pin to GND tomake sure of a proper low level. Returning from those states causes a new start-up sequence.

A voltage applied at the SS/TR pin can also be used to track a controller voltage. The output voltage follows this voltage in both directions up and down in forced PWM mode. In PFM mode, the output voltage decreases based on the load current. An external voltage applied on SS/TR is internally clamped to the feedback voltage (0.6V). TI recommends to set the final value of the external voltage on SS/TR to be slightly above 0.6V to make sure the device operates with the internal reference voltage when the power-up sequencing is finished. See *Section 9.3.1*.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPSM8281x are synchronous step-down converter power modules. The required power inductor is integrated inside the TPSM8281x. The inductor is shielded and has an inductance of 470 nH with approximately a ±20% tolerance. The TPSM82810 and TPSM82813 are pin-to-pin and BOM-to-BOM compatible, differing only in the rated output current.

9.2 Typical Application

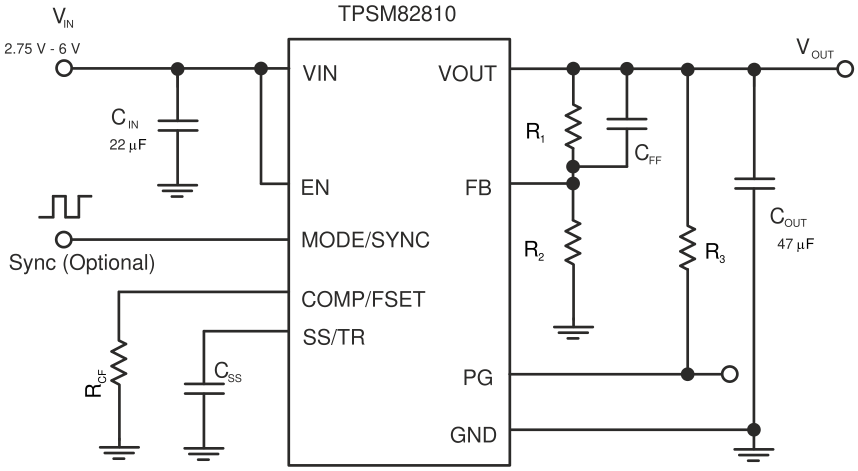


Figure 9-1. Typical Application Schematic

9.2.1 Design Requirements

The design guidelines provide a component selection to operate the device within the recommended operating conditions.

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM8281x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Programming the Output Voltage

The output voltage of the TPSM8281x is adjustable. Choose resistors R1 and R2 to set the output voltage within a range of 0.6V to 5.5V according to Equation 10. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100kΩ to have at least 6μA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in the *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1\right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1\right) \tag{10}$$

9.2.2.3 Feedforward capacitor

A feedforward capacitor (C_{FF}) is recommended in parallel with R_1 in order to improve the transient response. Regardless of the FB resistor values, the C_{FF} value must always be 10pF.

9.2.2.4 Input Capacitor

For most applications, a 22μF nominal ceramic capacitor is recommended. The input capacitor buffers the input voltage for transient events and also decouples the converter from the supply. A X7R or X7T multilayer ceramic capacitor (MLCC) is recommended for best filtering and must be placed between VIN and GND as close as possible to those pins. For applications with ambient temperatures below 85°C, a capacitor with X5R dielectric can be used. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating. The minimum required input capacitance is 5μF.

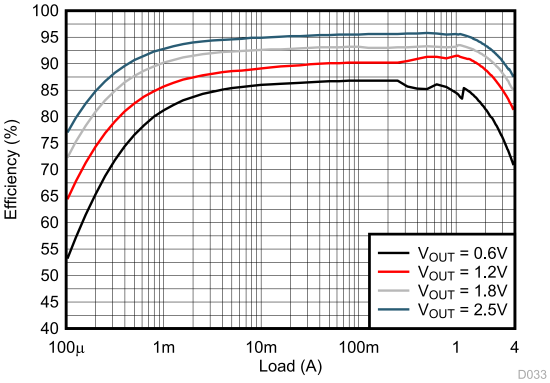
9.2.2.5 Output Capacitor

The architecture of the TPSM8281x allows the use of ceramic output capacitors which have low equivalent series resistance (ESR). These capacitors provide low output voltage ripple and are recommended. To keep the low resistance up to high frequencies and to get a narrow capacitance variation with temperature, it is recommended to use an X7R or X7T dielectric. At temperatures below 85°C, an X5R dielectric can be used.

Using a higher capacitance value has advantages like smaller voltage ripple and a tighter DC output accuracy in power save mode. By changing the device compensation with a resistor from COMP/FSET to GND, the device can be compensated in three steps based on the minimum capacitance used on the output. The maximum capacitance is 470μF in any of the compensation settings. The minimum capacitance required on the output depends on the compensation setting and output voltage as shown in Table 8-1. For output voltages below 1V, the minimum required capacitance increases linearly from 32μF at 1V to 53μF at 0.6V with the compensation setting for smallest output capacitance. Other compensation settings scale the same. Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering the package size and voltage rating.

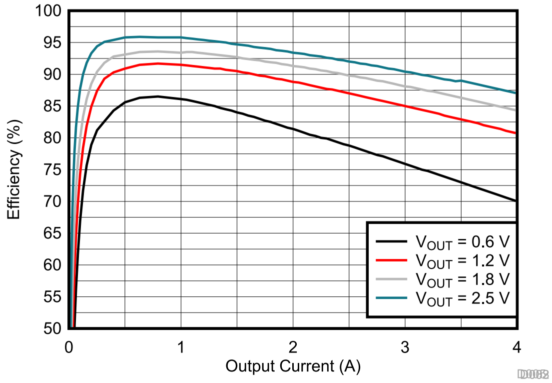
9.2.3 Application Curves

T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, 1.8MHz, PWM mode, BOM = Table 7-1 unless otherwise noted.



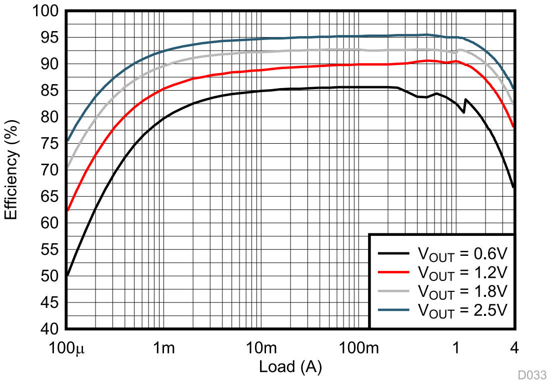
V_{IN} = 3.3V PFM, SIL Package T_A = 25°C

Figure 9-2. Efficiency versus Output Current



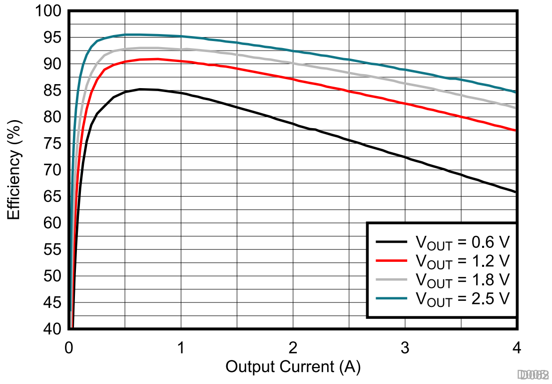
V_{IN} = 3.3V PWM, SIL Package T_A = 25°C

Figure 9-3. Efficiency versus Output Current



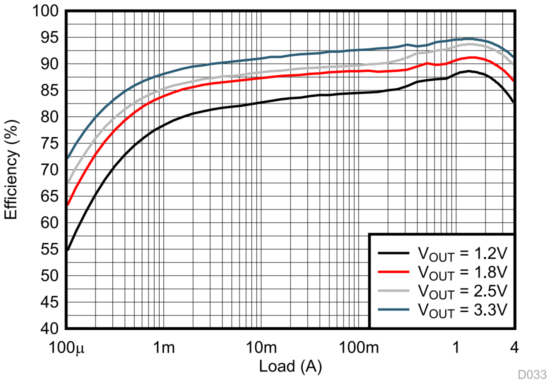
V_{IN} = 3.3V PFM, SIL Package T_A = 85°C

Figure 9-4. Efficiency versus Output Current



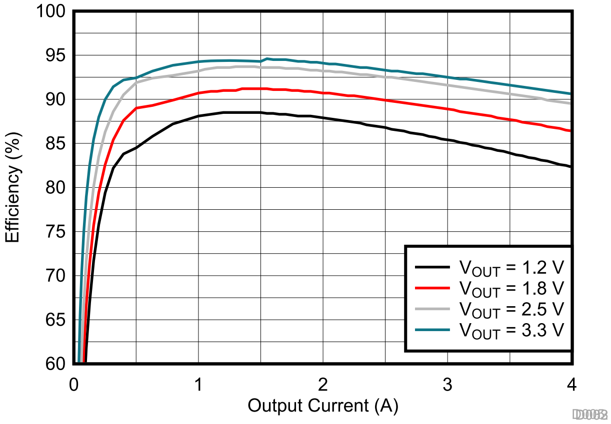
V_{IN} = 3.3V PWM, SIL Package T_A = 85°C

Figure 9-5. Efficiency versus Output Current



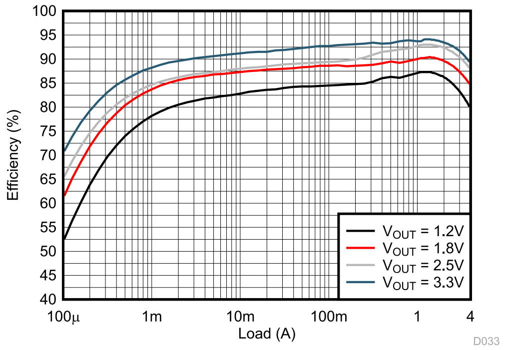
V_{IN} = 5V PFM, SIL Package T_A = 25°C

Figure 9-6. Efficiency versus Output Current



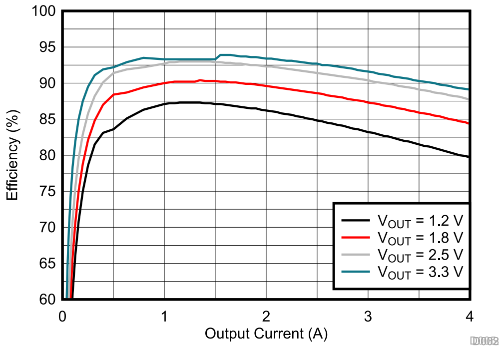
V_{IN} = 5V PWM, SIL Package T_A = 25°C

Figure 9-7. Efficiency versus Output Current



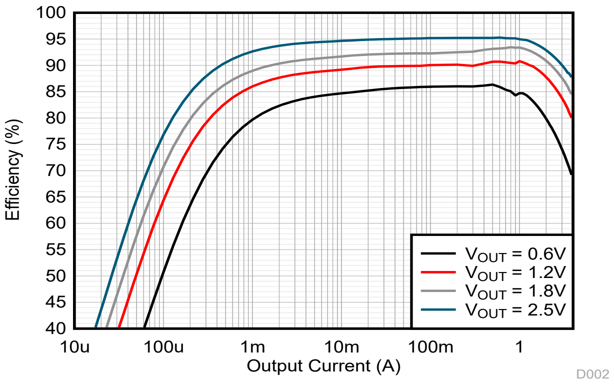
V_{IN} = 5V PFM, SIL Package T_A = 85°C

Figure 9-8. Efficiency versus Output Current



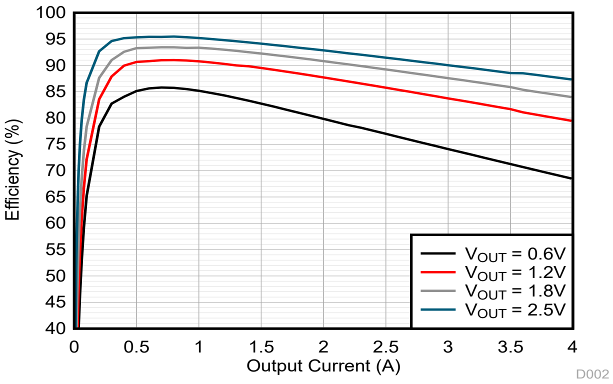
V_{IN} = 5V PWM, SIL Package T_A = 85°C

Figure 9-9. Efficiency versus Output Current



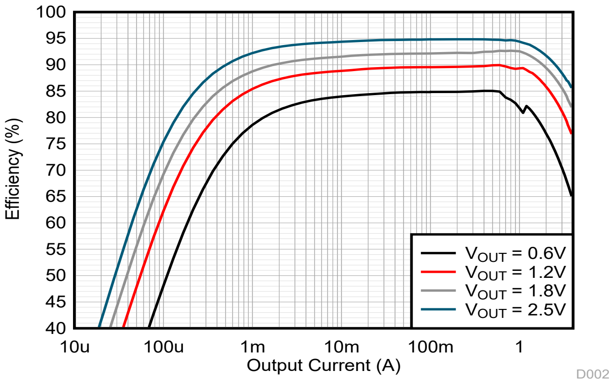
V_{IN} = 3.3V PFM, VCA Package T_A = 25°C

Figure 9-10. Efficiency versus Output Current



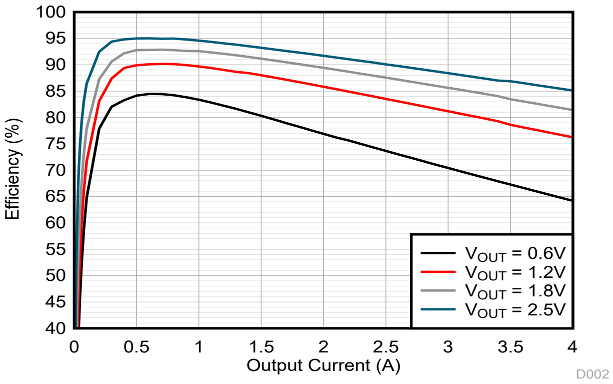
V_{IN} = 3.3V PWM, VCA Package T_A = 25°C

Figure 9-11. Efficiency versus Output Current



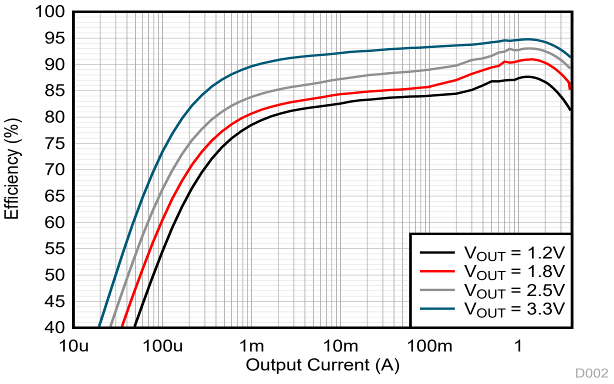
V_{IN} = 3.3V PFM, VCA Package T_A = 85°C

Figure 9-12. Efficiency versus Output Current



V_{IN} = 3.3V PWM, VCA Package T_A = 85°C

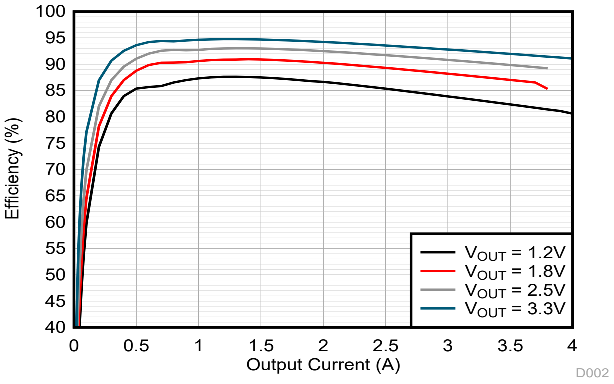
Figure 9-13. Efficiency versus Output Current



V_{IN} = 5V PFM, VCA T_A = 25°C

Package

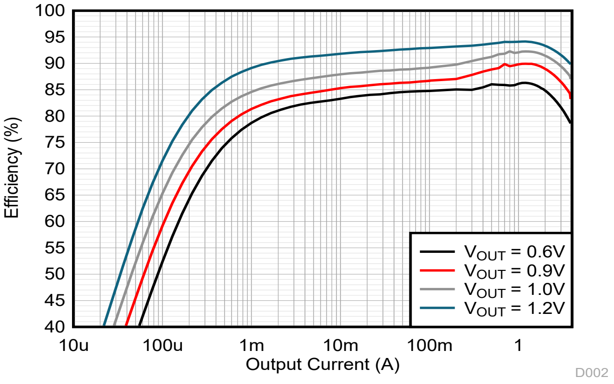
Figure 9-14. Efficiency versus Output Current



V_{IN} = 5V PWM, VCA T_A = 25°C

Package

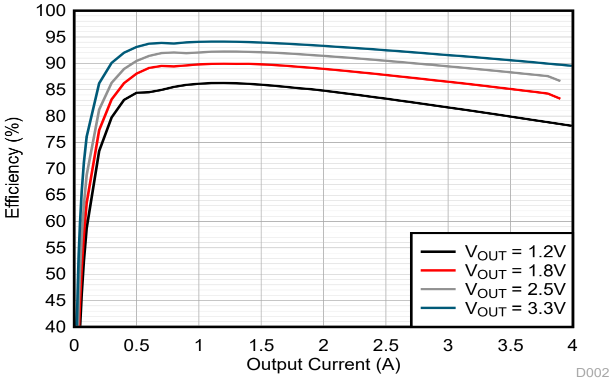
Figure 9-15. Efficiency versus Output Current



V_{IN} = 5V PFM, VCA T_A = 85°C

Package

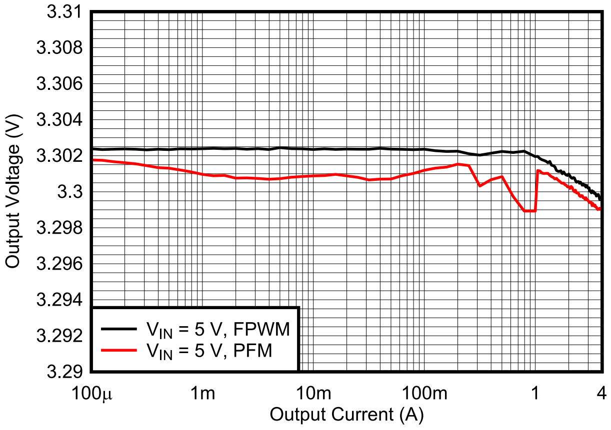
Figure 9-16. Efficiency versus Output Current



V_{IN} = 5V PWM, VCA T_A = 85°C

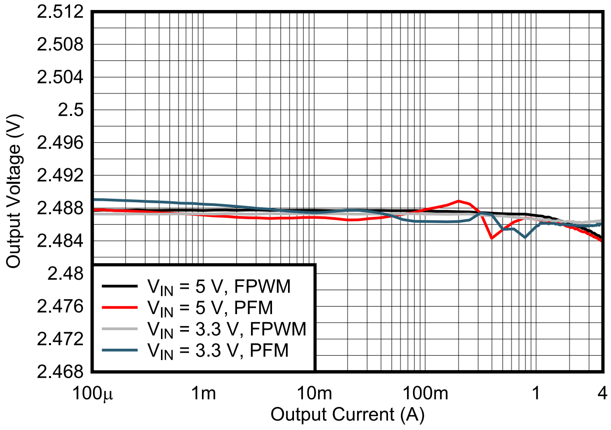
Package

Figure 9-17. Efficiency versus Output Current



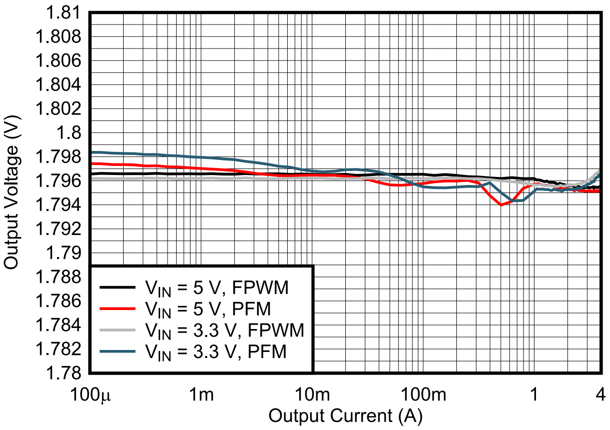
V_{OUT} = 3.3V T_A = 25°C

Figure 9-18. Output Voltage versus Output Current



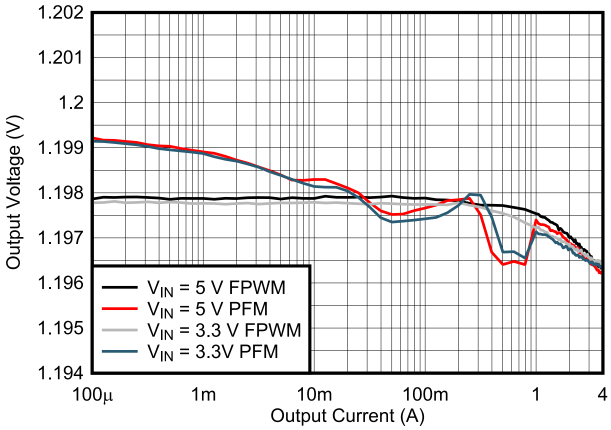
V_{OUT} = 2.5V T_A = 25°C

Figure 9-19. Output Voltage versus Output Current



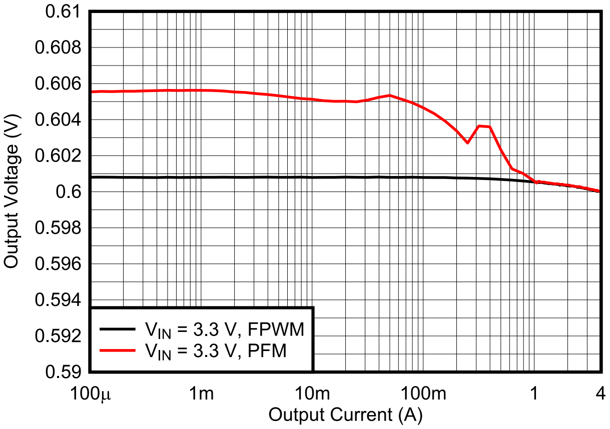
V_{OUT} = 1.8V T_A = 25°C

Figure 9-20. Output Voltage versus Output Current



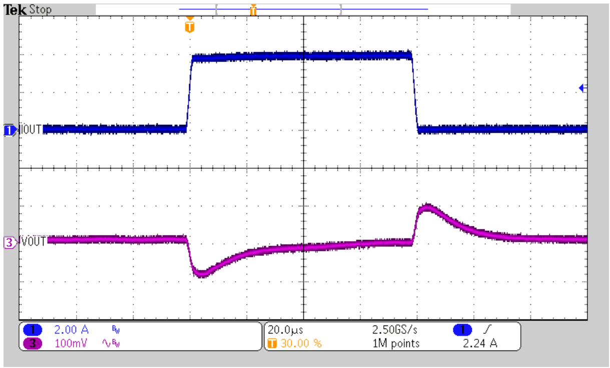
V_{OUT} = 1.2V T_A = 25°C

Figure 9-21. Output Voltage versus Output Current



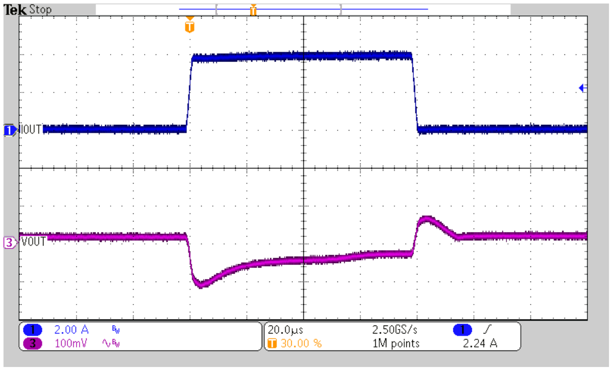
V_{OUT} = 0.6V T_A = 25°C

Figure 9-22. Output Voltage versus Output Current



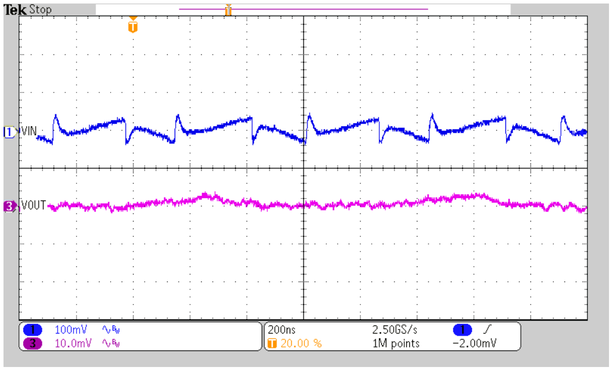
V_{OUT} = 1.8V PWM T_A = 25°C
V_{IN} = 5.0V I_{OUT} = 0A to 4A to 0A

Figure 9-23. Load Transient Response



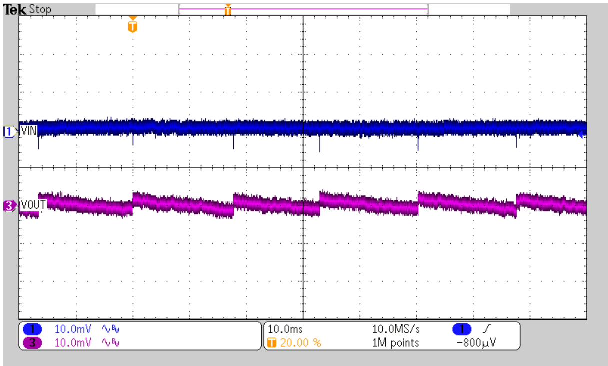
V_{OUT} = 1.8V PFM T_A = 25°C
V_{IN} = 5.0V I_{OUT} = 0A to 4A to 0A

Figure 9-24. Load Transient Response



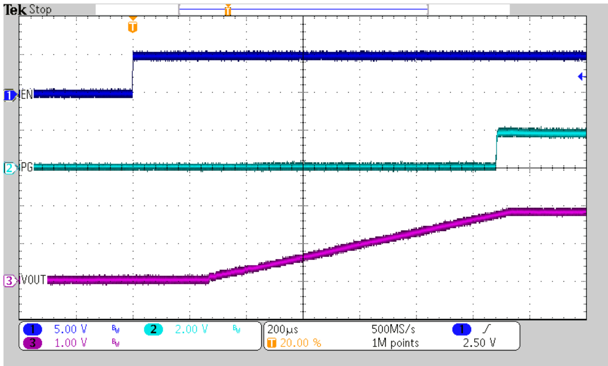
V_{OUT} = 1.8V PWM T_A = 25 °C
I_{OUT} = 4A V_{IN} = 5.0V BW = 20MHz

Figure 9-25. Output and Input Voltage Ripple



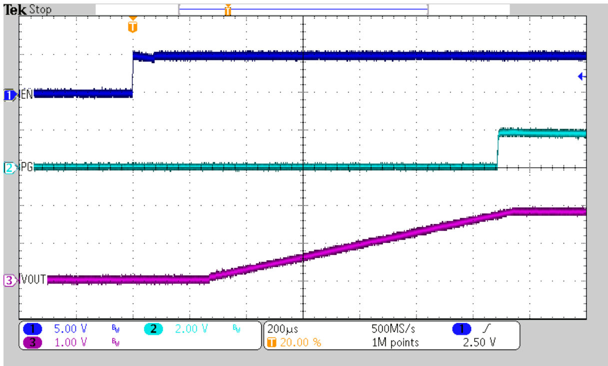
V_{OUT} = 1.8V PFM T_A = 25°C
I_{OUT} = 0A V_{IN} = 5.0V BW = 20MHz

Figure 9-26. Output and Input Voltage Ripple



V_{OUT} = 1.8V PWM T_A = 25°C
I_{OUT} = 4A V_{IN} = 5V C_{SS} = 4.7nF

Figure 9-27. Start-Up Timing



V_{OUT} = 1.8V PFM T_A = 25°C
I_{OUT} = 0A V_{IN} = 5V C_{SS} = 4.7nF

Figure 9-28. Start-Up Timing

9.3 System Examples

9.3.1 Voltage Tracking

The SS/TR pin is externally driven by another voltage source to achieve output voltage tracking. The application circuit is shown in Figure 10-21. From 0V to 0.6V, the internal reference voltage to the internal error amplifier follows the SS/TR pin voltage. When the SS/TR pin voltage is above 0.6V, the voltage tracking is disabled and the FB pin voltage is regulated at 0.6V. The device achieves ratiometric or coincidental (simultaneous) output tracking, as shown in Figure 10-22.

The R2 value must be set properly to achieve accurate voltage tracking by taking the 2.5µA charging current into account. 1kΩ or smaller is a sufficient value for R2. For decreasing SS/TR pin voltage, the device does not sink current from the output when the device is in PFM mode. The resulting decrease of the output voltage can be slower than the SS/TR pin voltage if the load is light. When driving the SS/TR pin with an external voltage, do not exceed the voltage rating of the SS/TR pin which is VIN+0.3V.

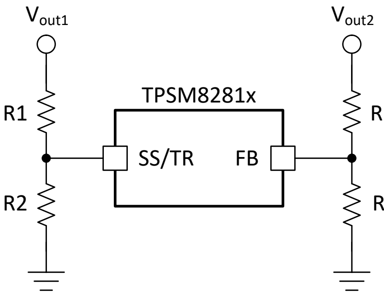
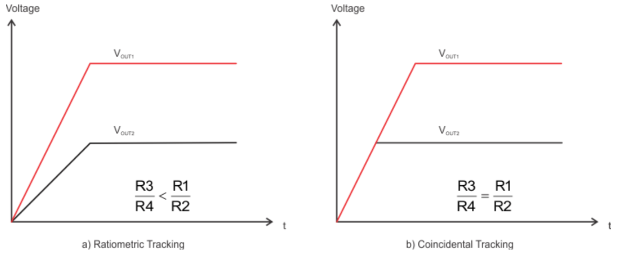


Figure 9-29. Schematic for Output Voltage Tracking



a) Ratiometric Tracking

b) Coincidental Tracking

Figure 9-30. Output Voltage Tracking

9.3.2 Synchronizing to an External Clock

The TPSM8281x can be synchronized by applying a clock on the MODE/SYNC pin. There is no need for any additional circuitry. See Figure 10-23. The clock can be applied, changed, and removed during operation. The value of the R_{CF} resistor is recommended to be chosen such that the internally defined frequency and the externally-applied frequency are close to each other to have a fast settling time to the external clock. Synchronizing to a clock is not possible, if the COMP/FSET pin is connected to Vin or GND. Figure 10-24 and Figure 10-25 show the external clock being applied and removed. When an external clock is applied, the device operates in PWM mode.

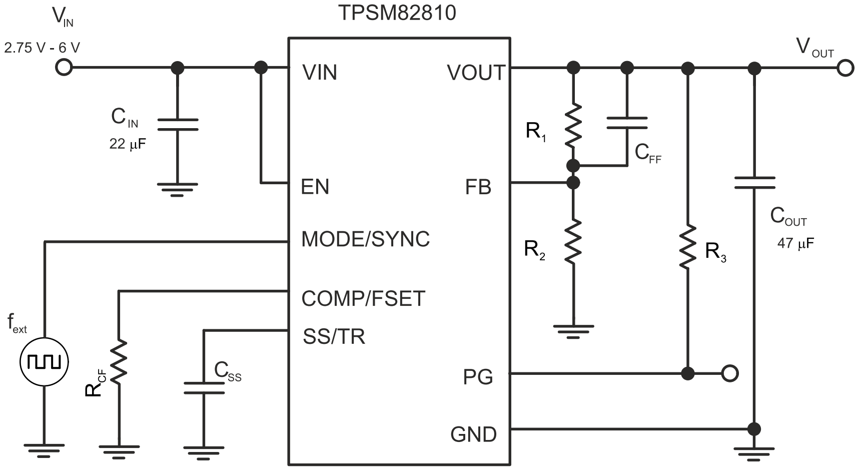
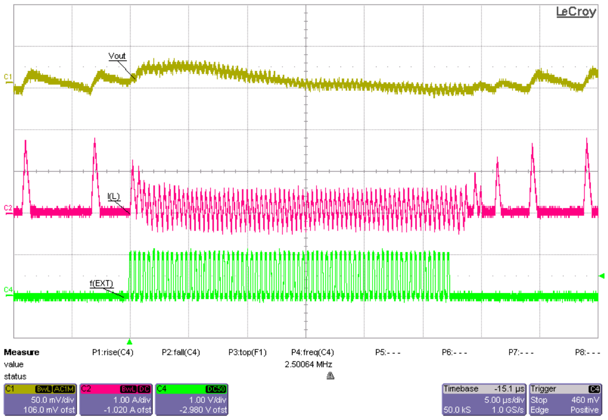


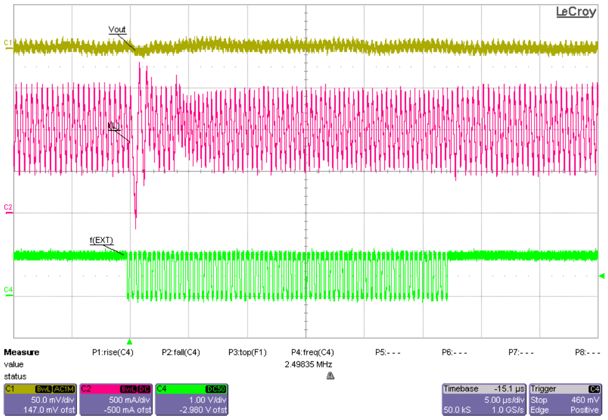
Figure 9-31. Frequency Synchronization



V_{IN} = 5V R_{CF} = 8.06kΩ I_{OUT} = 0.1A

V_{OUT} = 1.8V f_{EXT} = 2.5MHz

Figure 9-32. Applying and Removing the Synchronization Signal (PFM)



V_{IN} = 5V R_{CF} = 8.06kΩ I_{OUT} = 1A

V_{OUT} = 1.8V f_{EXT} = 2.5MHz

Figure 9-33. Applying and Removing the Synchronization Signal (FPWM)

9.4 Power Supply Recommendations

The TPSM8281x device family has no special requirements for the input power supply. The output current of the input power supply needs to be rated according to the supply voltage, output voltage, and output current of the TPSM8281x.

9.5 Layout

9.5.1 Layout Guidelines

A proper layout is critical for the operation of any switched mode power supply, especially at high switching frequencies. Therefore, the PCB layout of the TPSM8281x demands careful attention to ensure best performance. A poor layout can lead to issues like bad line and load regulation, instability, increased EMI radiation, and noise sensitivity. Refer to the *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal for a detailed discussion of general best practices. Specific recommendations for the device are listed below.

- The input capacitor must be placed as close as possible to the VIN and GND pins of the device. This is the most critical component placement. Route the input capacitor directly to the VIN and GND pins avoiding vias.
- Place the output capacitor ground close to the VOUT and GND pins and route it directly avoiding vias.
- Place the FB resistors, R1 and R2, and the feedforward capacitor C_{FF} close to the FB pin and place C_{SS} close to the SS/TR pin to minimize noise pickup.
- Place the R_{CF} resistor close to the COMP/FSET pin to minimize the parasitic capacitance.
- The recommended layout is implemented on the EVM and shown in the *TPSM82810EVM-089 Evaluation Module User's Guide* and in *Section 12.2*.
- The recommended land pattern for the TPSM8281x is shown at the end of this data sheet. For best manufacturing results, it is important to create the pads as solder mask defined (SMD), when some pins (such as VIN, VOUT, and GND) are connected to large copper planes. Using SMD pads keeps each pad the same size and avoids solder pulling the device during reflow.

9.5.2 Layout Example

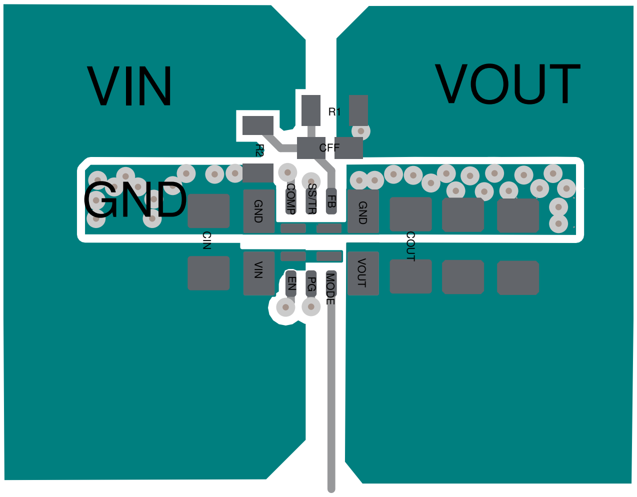


Figure 9-34. Example Layout SIL Package

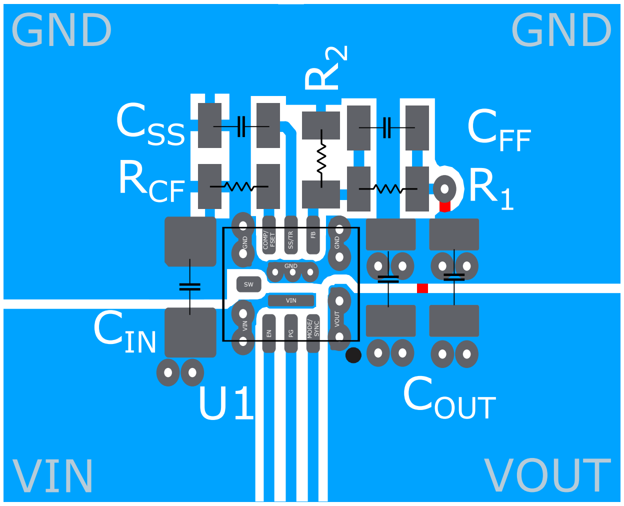


Figure 9-35. Example Layout VCA Package

9.5.2.1 Thermal Consideration

The TPSM8281x module temperature must be kept less than the maximum rating of 125°C. The following are three basic approaches for enhancing thermal performance:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM8281x, apply the typical efficiency stated in this data sheet to the desired application condition to compute the power dissipation of the module. Then, calculate the module temperature rise by multiplying the power dissipation by the thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* and *Semiconductor and IC Package Thermal Metrics*.

The thermal values in *Section 6.4* used the recommended land pattern, shown at the end of this data sheet, including the 18 vias as they are shown. The TPSM8281x was simulated on a PCB defined by JEDEC 51-7. The 9 vias on the GND pins were connected to copper on other PCB layers, while the remaining 9 vias were not connected to other layers.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Third-Party Products Disclaimer

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10.1.2 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPSM8281x device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPSM82810EVM-089 Evaluation Module* user's guide
- Texas Instruments, *Thermal Characteristics of Linear and Logic Packages Using JEDEC PCB Designs* application note
- Texas Instruments, *Five Steps to a Great PCB Layout for a Step-Down Converter* analog design journal
- Texas Instruments, *Design Considerations for a Resistive Feedback Divider in a DC/DC Converter* analog design journal
- Texas Instruments, *Achieving a Clean Start-up by Using a DC/DC Converter with a Precise Enable-pin Threshold* analog design journal

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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10.5 Trademarks

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10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (December 2020) to Revision B (July 2024) **Page**

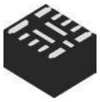
- Added TPSM82811 and TPSM82812 to the data sheet.................... 1
- Added the VCA package option to the data sheet.................... 1
- Updated the *ESD Ratings* table to show CDM testing was per JS-002.................... 4

Changes from Revision * (September 2019) to Revision A (December 2020) **Page**

- Changed device status from Advance Information to Production Data.................... 1
- Updated the numbering format for tables, figures and cross-references throughout the document. 1

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

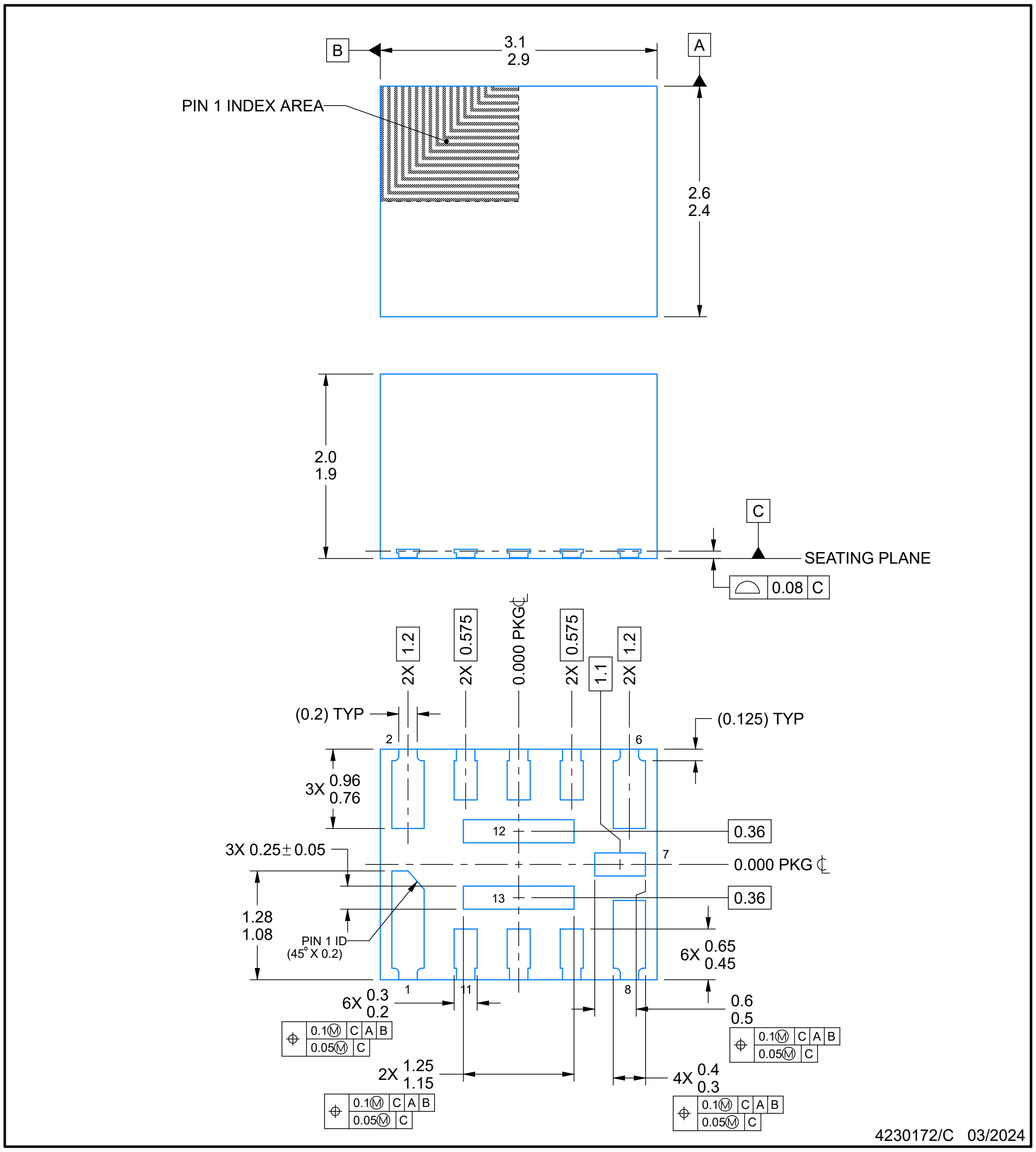


PACKAGE OUTLINE

VCA0013A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

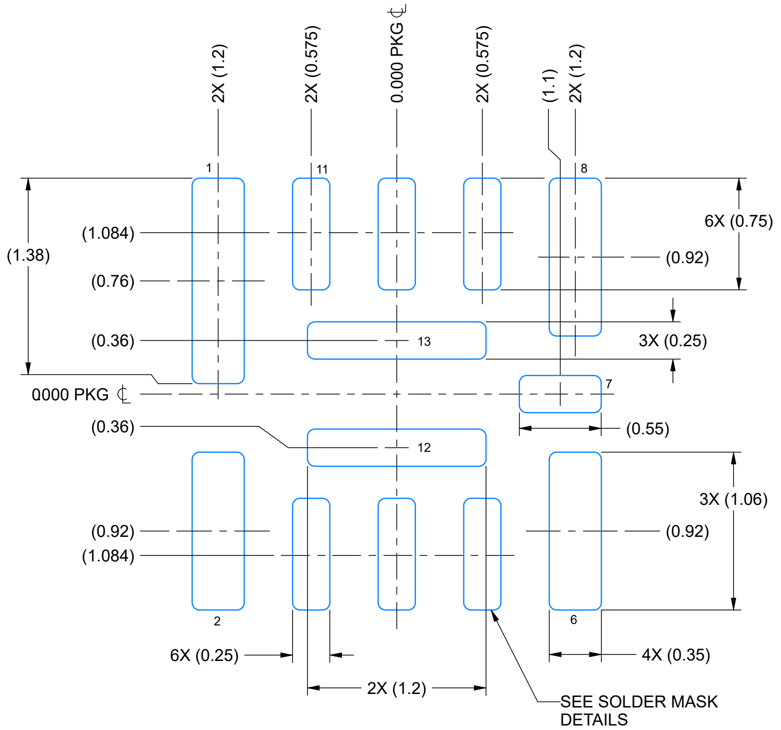
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

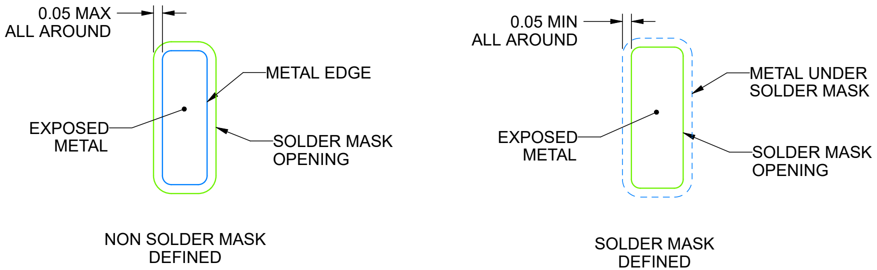
VCA0013A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED
PINS 1, 2, 6, 8, 12 & 13

SOLDER MASK DETAILS

4230172/C 03/2024

NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271)

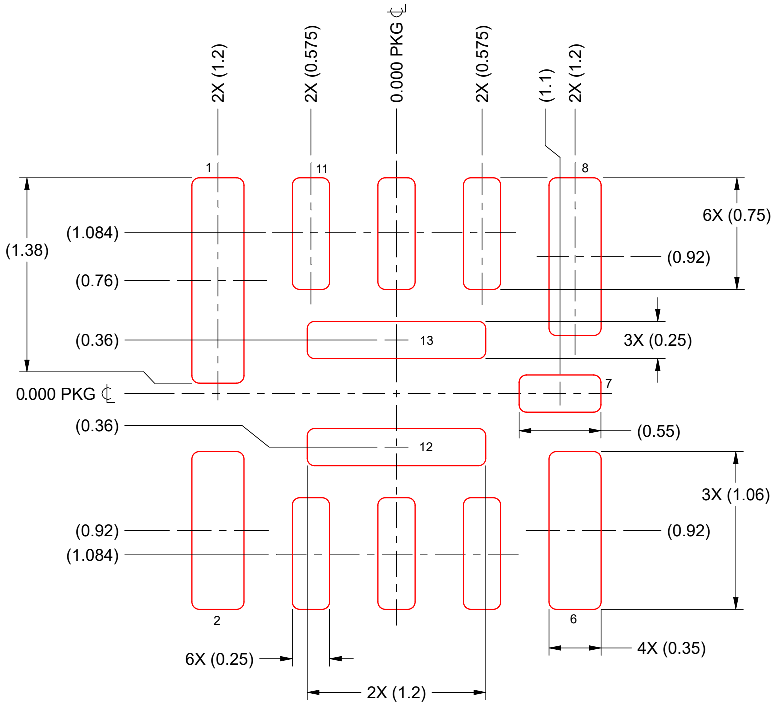
www.ti.com

EXAMPLE STENCIL DESIGN

VCA0013A

QFN-FCMOD - 2 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 25X

4230172/C 03/2024

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM82810SILR	ACTIVE	uSiP	SIL	14	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	FG	Samples
TPSM82810SSILR	ACTIVE	uSiP	SIL	14	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	GC	Samples
TPSM82813SILR	ACTIVE	uSiP	SIL	14	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	GD	Samples
TPSM82813SSILR	ACTIVE	uSiP	SIL	14	3000	RoHS & Green	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	HF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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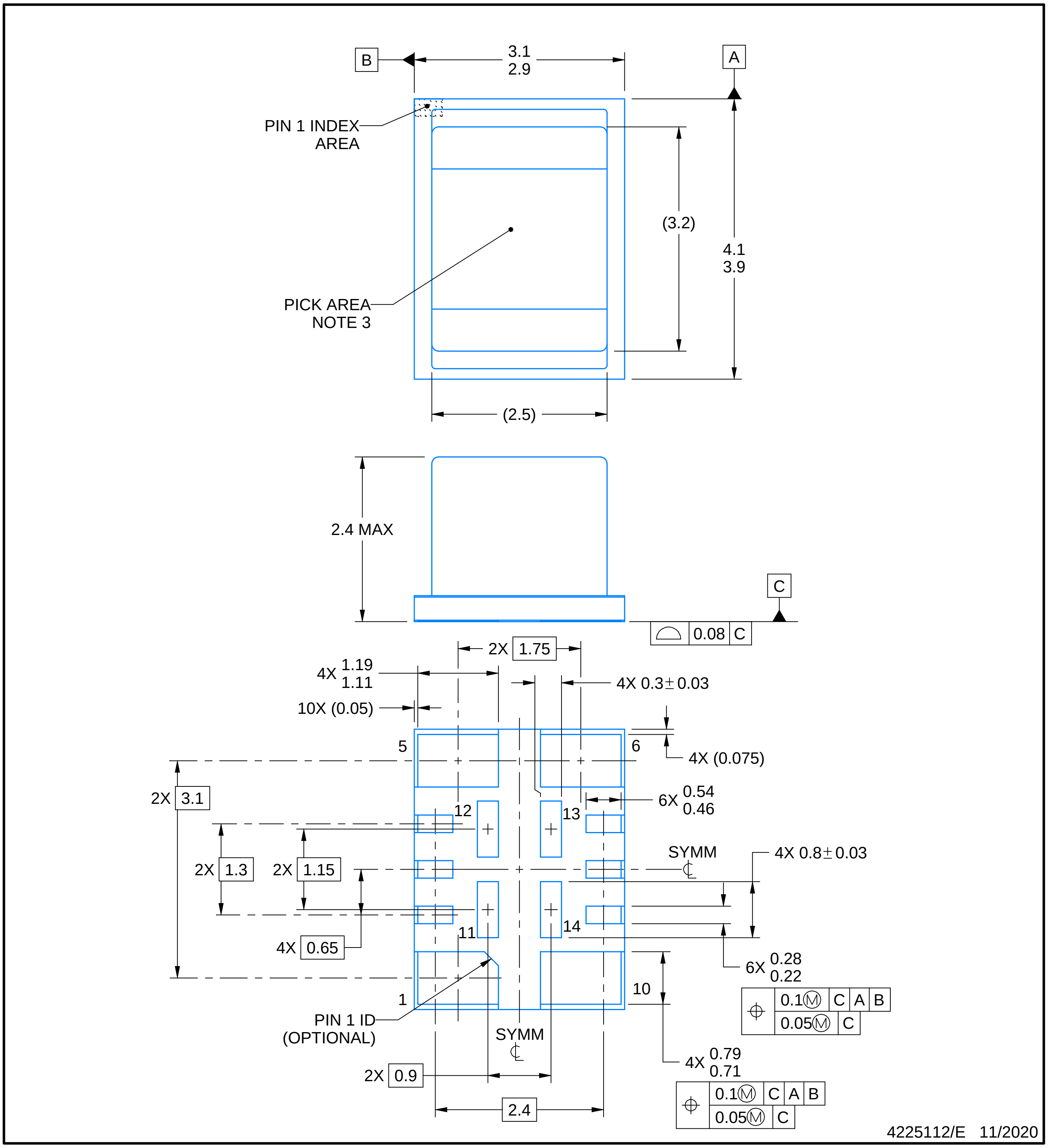
PACKAGE OUTLINE

uSIP™ - 2.4 mm max height

MICRO SYSTEM IN PACKAGE

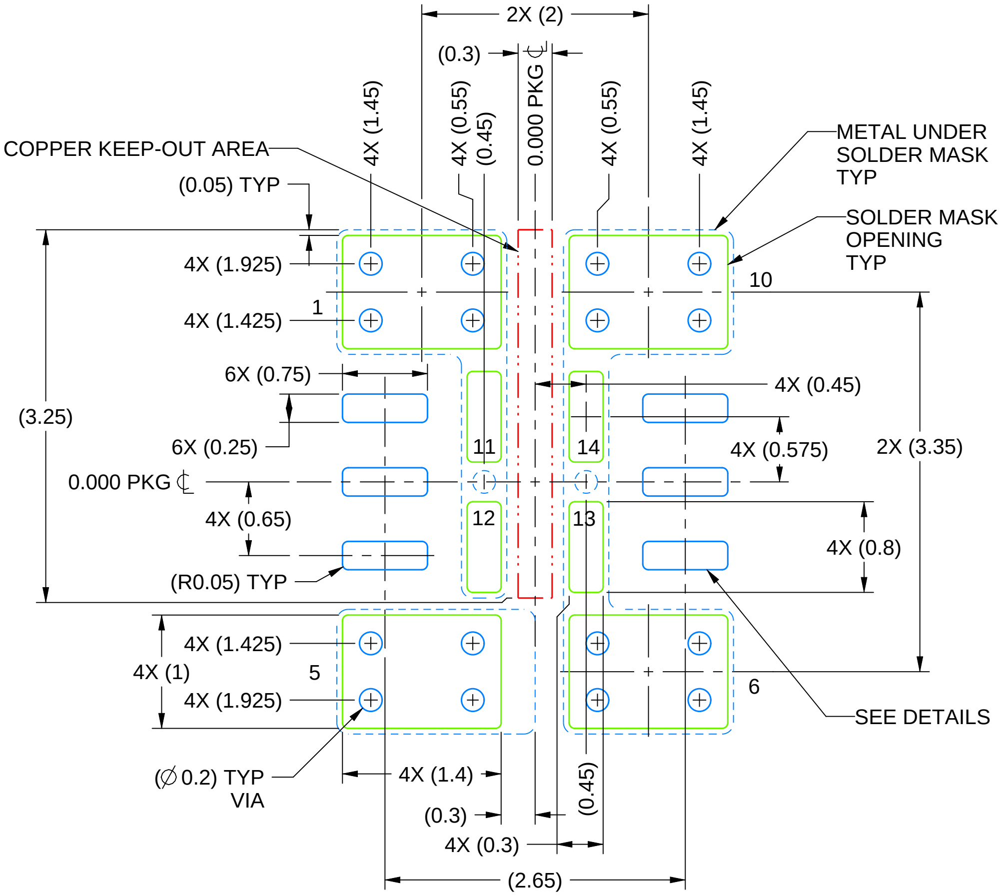


MicroSiP is a trademark of Texas Instruments

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅1.3 mm or smaller recommended.
4. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
SCALE:15X

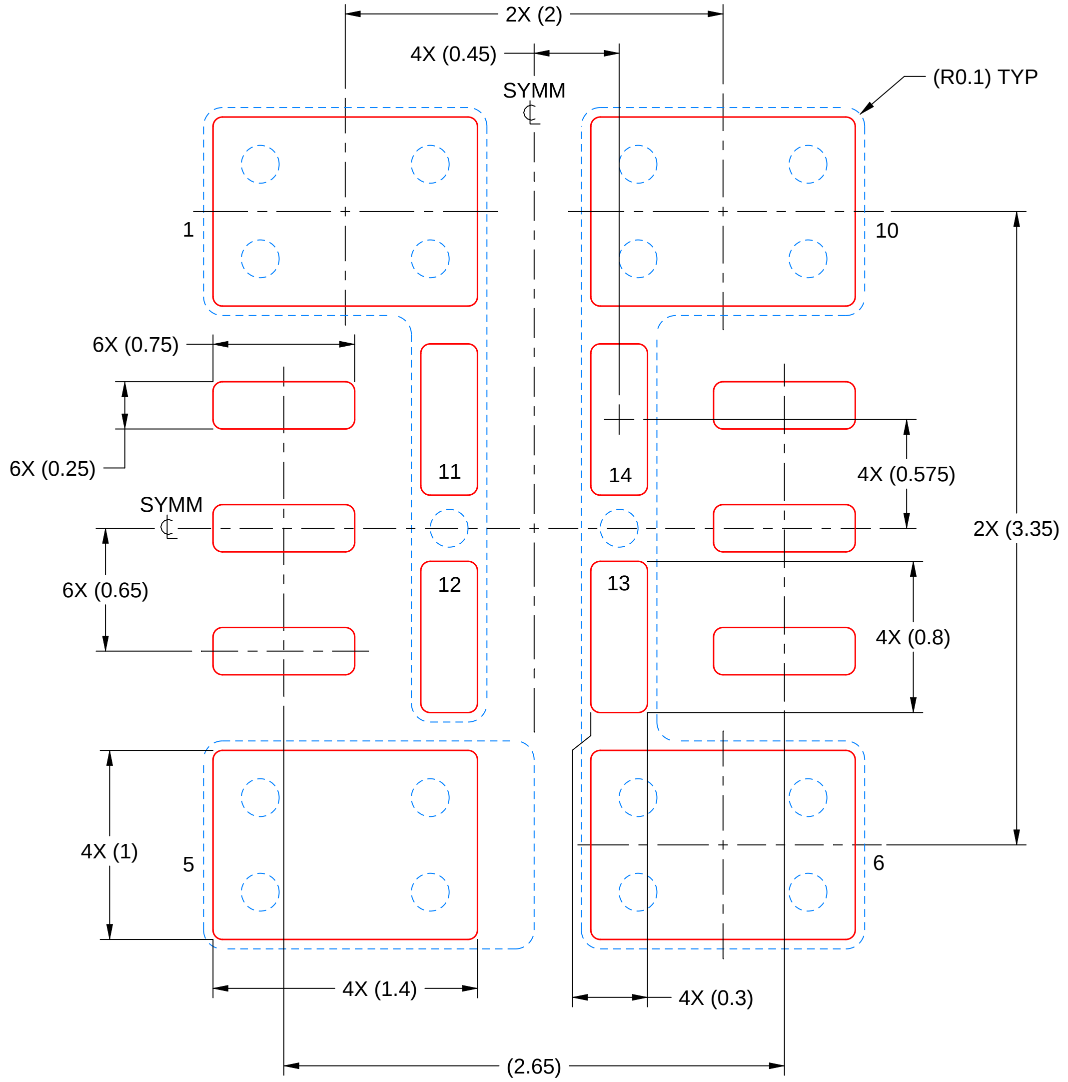
NON SOLDER MASK DEFINED

SOLDER MASK DEFINED
PADS 1, 5, 6, 10 AND 11 - 14

SOLDER MASK DETAILS
NOT TO SCALE

NOTES: (continued)

5. This package is designed to be soldered to thermal pads on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4225112/E 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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