BQ25303J Standalone 1-Cell, 17-V, 3.0-A Battery Charger with JEITA Battery Temperature Monitoring

1 Features

- Standalone charger and easy to configure
- High-efficiency, 1.2-MHz, synchronous switch-mode buck charger
  - 92.5% charge efficiency at 2A from 5-V input for 1-cell battery
  - 91.8% charge efficiency at 2A from 9-V input for 1-cell battery
- Single input to support USB input and high voltage adaptors
  - Support 4.1-V - 17-V input voltage range with 28-V absolute maximum input voltage rating
  - Input Voltage Dynamic Power Management (VINDPM) tracking battery voltage
- High integration
  - Integrated reverse blocking and synchronous switching MOSFET
  - Internal input and charge current sense
  - Internal loop compensation
  - Integrated bootstrap diode
- 4.1-V / 4.2-V / 4.35-V / 4.4-V charge voltage
- 3.0-A maximum fast charge current
- 200-nA low battery leakage current at 4.5-V V_{BAT}
- 4.25-µA VBUS supply current in IC disable mode
- Charge current thermal regulation at 120°C
- Precharge current: 10% of fast charge current
- Termination current: 10% of fast charge current
- Charge accuracy
  - ±0.5% charge voltage regulation
  - ±10% charge current regulation
- Safety
  - Thermal regulation and thermal shutdown
  - Input Under-Voltage Lockout (UVLO) and Over-Voltage Protection (OVP)
  - Battery overcharge protection
  - Safety timer for precharge and fast charge
  - Charge disabled if current setting pin ICHG is open or short
  - JEITA Battery temperature protection
  - Fault report on STAT pin
- Available in WQFN 3x3-16 package

2 Applications

- Wireless speaker
- Gaming
- Cradle charger
- Medical

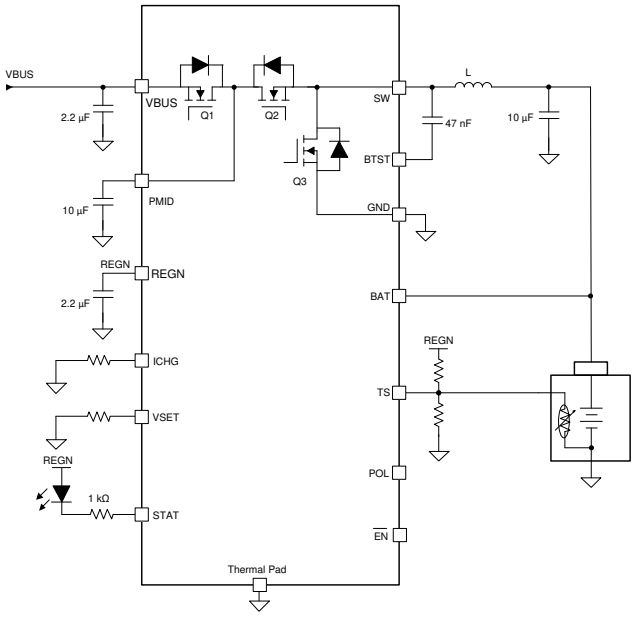
3 Description

The BQ25303J is a highly-integrated standalone switch-mode battery charger for 1-cell Li-ion and Li-polymer batteries. The BQ25303J supports 4.1-V to 17-V input voltage and 3-A fast charge current. The integrated current sensing topology of the device enables high charge efficiency and low BOM cost. The best-in-class 200-nA low quiescent current of the device conserves battery energy and maximizes the shelf time for portable devices. The BQ25303J is available in a 3x3 WQFN package for easy 2-layer layout and space limited applications.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
BQ25303J	RTE	3.00mm x 3.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

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4 Revision History

DATE	REVISION	NOTES
February 2021	*	Initial release.

5 Description (continued)

The BQ25303J supports 4.1-V to 17-V input to charge single cell batteries. The BQ25303J provides up to 3-A continuous charge current to a single cell 1S battery The device features fast charging for portable devices. Its input voltage regulation delivers maximum charging power to the battery from input source. The solution is highly integrated with an input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), and low-side switching FET (LSFET, Q3).

The BQ25303J features lossless integrated current sensing to reduce power loss and BOM cost with minimized component count. It also integrates a bootstrap diode for the high-side gate drive and battery temperature monitor to simplify system design. The device initiates and completes a charging cycle without host control. The BQ25303J charge voltage and charge current are set by external resistors. The BQ25303J detects the charge voltage setting at startup and charges the battery in four phases: battery short, pre-conditioning, constant current, and constant voltage. At the end of the charging cycle, the charger automatically terminates if the charge current is below the termination current threshold and the battery voltage is above the recharge threshold. When the battery voltage falls below the recharge threshold, the charger will automatically start another charging cycle. The charger provides various safety features for battery charging and system operations, including battery temperature monitoring based on negative temperature coefficient (NTC) thermistor, charge safety timer, input over-voltage and over-current protections, as well as battery over-voltage protection. Pin open and short protection is also built in to protect against the charge current setting pin ICHG accidently open or short to GND. The thermal regulation regulates charge current to limit die temperature during high power operation or high ambient temperature conditions.

The STAT pin output reports charging status and fault conditions. When the input voltage is removed, the device automatically enters HiZ mode with very low leakage current from battery to the charger device. The BQ25303J is available in a 3 mm x 3 mm thin WQFN package.

6 Device Comparison Table

	BQ25300	BQ25302	BQ25303J	BQ25306
Battery Cells in Series	1	1	1	1, 2
Input Operation Voltage	4.1V to 17V	4.1V to 6.2V	4.1V to 17V	4.1V to 17V
Charge Voltage	3.6V, 4.15V, 4.2V, 4.05V	4.1V, 4.35V, 4.4V, 4.2V	4.1V, 4.35V, 4.4V, 4.2V	programmable from 3.4V to 9.0V
Maximum Fast Charge Current ICHG	3.0A	2.0A	3.0A	3.0A
Battery Temperature Protection (JEITA or Cold/Hot)	Cold/Hot	Cold/Hot	JEITA	Cold/Hot

7 Pin Configuration and Functions

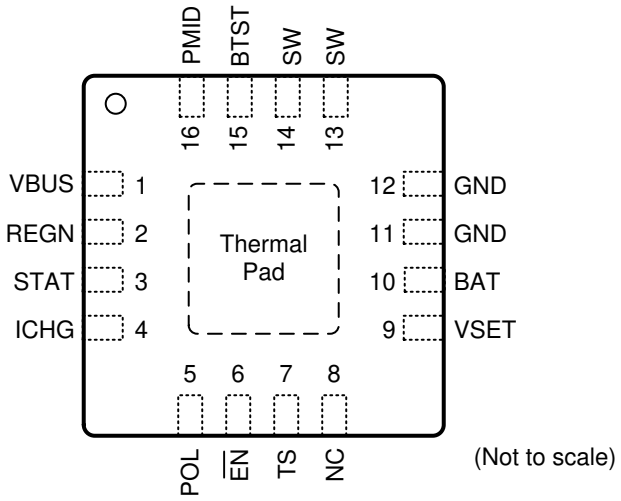


Figure 7-1. RTE Package 16-Pin WQFN Top View

Table 7-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
VBUS	1	P	Charger input voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 2.2uF ceramic capacitor from VBUS to GND and place it as close as possible to IC.
PMID	16	P	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of high-side MOSFET (HSFET). Place ceramic 10µF on PMID to GND and place it as close as possible to IC.
SW	13,14	P	Switching node. Connected to output inductor. Internally SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047µF bootstrap capacitor from SW to BTST.
BTST	15	P	High-side FET driver supply. Internally, the BTST is connected to the cathode of the internal boost-strap diode. Connect the 0.047µF bootstrap capacitor from SW to BTST.
GND	11,12	P	Ground. Connected directly to thermal pad on the top layer. A single point connection is recommended between power ground and analog ground near the IC GND pins.
REGN	2	P	Low-side FET driver positive supply output. Connect a 2.2µF ceramic capacitor from REGN to GND. The capacitor should be placed close to the IC.
BAT	10	AI	Battery voltage sensing input. Connect this pin to the positive terminal of the battery pack and the node of inductor output terminal. 10-µF capacitor is recommended to connect to this pin.
TS	7	AI	Battery temperature voltage input. Connect a negative temperature coefficient thermistor (NTC). Program temperature window with a resistor divider from REGN to TS and TS to GND. Charge suspends when TS pin voltage is out of range. When TS pin is not used, connect a 10-kΩ resistor from REGN to TS and a 10-kΩ resistor from TS to GND. It is recommended to use a 103AT-2 thermistor.
ICHG	4	AI	Charge current program input. Connect a 1% resistor RICHG from this pin to ground to program the charge current as ICHG = K_{ICHG} / R_{ICHG} (K_{ICHG} = 40,000). No capacitor is allowed to connect at this pin. When ICHG pin is pulled to ground or left open, the charger stop switching and STAT pin starts blinking.
STAT	3	AO	Charge status indication output. This pin is open drain output. Connect this pin to REGN via a current limiting resistor and LED. The STAT pin indicates charger status as: • Charge in progress: STAT pin is pulled LOW • Charge completed, charge disabled by $\overline{EN}$: STAT pin is OPEN • Fault conditions: STAT pin blinks.
VSET	9	AI	Charge Voltage Setting Input. VSET pin sets battery charge voltage. Program battery regulation voltage with a resistor pull-down from VSET to GND: • Floating (R > 200kΩ±10%): 4.1V • Shorted to GND (R < 510Ω): 4.2V • R = 51kΩ ± 10%: 4.35V • R = 10kΩ ± 10%: 4.4V The maximum allowed capacitance on this pin is 50pF.
POL	5	AI	$\overline{EN}$ pin polarity selection.

Table 7-1. Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
$\overline{EN}$	6	AI	Device disable input. With POL pin floating, the device is enabled with $\overline{EN}$ pin floating or pulled low, and the device is disabled if $\overline{EN}$ pin is pulled high. With POL pin grounded, the device is enabled with $\overline{EN}$ pin pulled high, and the device is disabled with $\overline{EN}$ pin pulled low or floating.
NC	8	-	No connection. Keep this pin floating or grounded.
Thermal Pad	17	-	Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane. Ground layer(s) are connected to thermal pad through vias under thermal pad.

(1) AI = Analog input, AO = Analog Output, AIO = Analog input Output, DI = Digital input, DO = Digital Output, DIO = Digital input Output, P = Power

8 Specifications

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Voltage Range (with respect to GND)	VBUS (converter not switching)	–2	28	V
	PMID (converter not switching)	–0.3	28	V
	SW	–2(–3 for 10ns)	20	V
	BTST	-0.3	25.5	V
	BAT	–0.3	11	V
	REGN	–0.3	5.5	V
	VSET	–0.3	11	V
	ICHG, REGN, TS, STAT, POL, $\overline{EN}$	–0.3	5.5	V
Voltage Range	BTST to SW	–0.3	5.5	V
Output Sink Current	STAT		6	mA
Output Sink Current	REGN		16	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{BAT}	Battery voltage			4.4	V
I_{VBUS}	Input current			3	A
I_{SW}	Output current (SW)			3	A
T_A	Ambient temperature	–40		85	°C
L	Recommended inductance at V_{VBUS_MAX} < 6.2V		1.0		µH
L	Recommended inductance at V_{VBUS_MAX} > 6.2V		2.2		µH
C_{VBUS}	Recommended capacitance at VBUS		2.2		µF
C_{PMID}	Recommended capacitance at PMID		10		µF
C_{BAT}	Recommended capacitance at BAT		10		µF

8.4 Thermal Information

THERMAL METRIC[1]		BQ2530x RTE 16-PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC[1])	45.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.9	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OVP}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, L=2.2µH, TJ = -40°C to +125°C, and TJ = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
I_{VBUS_REVS}	V_{BUS} reverse current from BAT/SW to VBUS TJ = -40°C - 85°C	$V_{BAT} = V_{SW}$ = 4.5V, V_{BUS} is shorted to GND, measure V_{BUS} reverse current		0.07	3	µA
$I_{Q\_VBUS\_DIS}$	V_{BUS} leakage current in disable mode TJ = -40°C - 85°C	V_{BUS} = 5V, V_{BAT} = 4V, charger is disabled, /EN is pulled high		3.5	4.25	µA
$I_{Q\_BAT\_HIZ}$	BAT and SW pin leakage current in HiZ mode TJ = -40°C - 65°C	$V_{BAT} = V_{SW}$ = 4.5V, V_{BUS}floating		0.17	1	µA
VBUS POWER UP						
V_{VBUS_OP}	V_{BUS} operating range		4.1		17.0	V
V_{VBUS_UVLOZ}	V_{BUS} power on reset	V_{BUS} rising	3.0		3.80	V
$V_{VBUS\_UVLOZ\_HYS}$	V_{BUS} power on reset hysteresis	V_{BUS} falling		250		mV
V_{VBUS_LOWV}	A condition to turnon REGN	V_{BUS} rising, REGN turns on, V_{BAT} = 3.2V	3.8	3.90	4.00	V
$V_{VBUS\_LOWV\_HYS}$	A condition to turnon REGN, hysteresis	V_{BUS} falling, REGN turns off, V_{BAT} = 3.2V		300		mV
V_{SLEEP}	Enter sleep mode threshold	V_{BUS} falling, V_{BUS} - V_{BAT}, $V_{VBUS\_LOWV} < V_{BAT} < V_{BATREG}$	30	60	100	mV
V_{SLEEPZ}	Exit sleep mode threshold	V_{BUS} rising, V_{BUS} - V_{BAT}, $V_{VBUS\_LOWV} < V_{BAT} < V_{BATREG}$	110	157	295	mV
$V_{VBUS\_OVP\_RISE}$	V_{BUS} overvoltage rising threshold	V_{BUS} rising, converter stops switching	17.00	17.40	17.80	V
$V_{VBUS\_OVP\_HYS}$	V_{BUS} overvoltage falling hysteresis	V_{BUS} falling, converter stops switching		750		mV
MOSFETS						
R_{DSON_Q1}	Top reverse blocking MOSFET on-resistance between VBUS and PMID (Q1)	V_{REGN} = 5V		40	65	mΩ
R_{DSON_Q2}	High-side switching MOSFET on-resistance between PMID and SW (Q2)	V_{REGN} = 5V		50	82	mΩ
R_{DSON_Q3}	Low-side switching MOSFET on-resistance between SW and GND (Q3)	V_{REGN} = 5V		45	72	mΩ
BATTERY CHARGER						

8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, L=2.2µH, TJ = -40°C to +125°C, and TJ = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BATREG}	Charge voltage regulation	VSET pin floating, TJ = -40°C to +85°C	4.08	4.100	4.120	V
		Connect VSET pin to 51kΩ resistor, TJ = -40°C to +85°C	4.328	4.350	4.371	V
		Connect VSET pin to 10kΩ resistor, TJ = -40°C to +85°C	4.378	4.400	4.422	V
		VSET pin is grounded, TJ = -40°C to +85°C	4.179	4.200	4.221	V
I_{CHG}	Charge current regulation	ICHG set at 1.72A with R_{ICHG} = 23.2kΩ	1.55	1.72	1.89	A
		ICHG set at 1.0A with R_{ICHG} = 40.2kΩ	0.90	1.00	1.10	A
		ICHG set at 0.5A with R_{ICHG} = 78.7kΩ	0.40	0.50	0.60	A
I_{TERM}	Termination current regulation	ICHG = 1.72A, 10% of ICHG, R_{ICHG} = 23.2kΩ	138	172	206	mA
		ICHG = 1.0A, 10% of ICHG, R_{ICHG} = 40.2kΩ	70	100	130	mA
		ICHG = 0.5A, ITERM = 63mA, R_{ICHG} = 78.7kΩ	33	63	93	mA
I_{PRECHG}	Precharge current	ICHG = 1.72A, 10% of ICHG, R_{ICHG} = 23.2kΩ	115	172	225	mA
		ICHG = 1.0A, 10% of ICHG, R_{ICHG} = 40.2kΩ	50	100	150	mA
		ICHG = 0.5A, R_{ICHG} = 78.7kΩ	28	63	98	mA
$V_{BAT\_SHORT\_RISE}$	V_{BAT} short rising threshold	Short to precharge	2.05	2.20	2.35	V
$V_{BAT\_SHORT\_FALL}$	V_{BAT} short falling threshold	Precharge to short	1.85	2.00	2.15	V
I_{BAT_SHORT}	Battery short current	V_{BAT} < $V_{BAT\_SHORT\_FALL}$,	25	35	46	mA
$V_{BAT\_LOWV\_RISE}$	Rising threshold	Precharge to fast charge	2.90	3.00	3.10	V
$V_{BAT\_LOWV\_FALL}$	Falling threshold	Fast charge to precharge	2.60	2.70	2.80	V
V_{RECHG_HYS}	Recharge hysteresis below V_{BATREG}	V_{BAT} falling	110	160	216	mV
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_MIN}	Minimum input voltage regulation	V_{BAT} = 3.5V, measured at PMID pin	4	4.07	4.2	V
V_{INDPM}	Input voltage regulation	V_{BAT} = 4V, measured at PMID pin, V_{INDPM} = 1.044*VBAT+ 0.125V	4.15	4.28	4.41	V
I_{INDPM_3A}	Input current regulation	V_{BUS} = 5V	3.00	3.35	3.70	A
BATTERY OVER-VOLTAGE PROTECTION						
$V_{BAT\_OVP\_RISE}$	Battery overvoltage rising threshold	V_{BAT} rising, as percentage of V_{BATREG}	101.9	103.5	105.0	%
$V_{BAT\_OVP\_FALL}$	Battery overvoltage falling threshold	V_{BAT} falling, as percentage of V_{BATREG}	100.0	101.6	103.1	%
CONVERTER PROTECTION						
$V_{BTST\_REFRESH}$	Bootstrap refresh comparator threshold	(V_{BTST} - V_{SW}) when LSFET refresh pulse is requested, V_{BUS} = 5V	2.7	3	3.3	V
I_{HSFET_OCP}	HSFET cycle by cycle over current limit threshold		5.2	6.2	6.7	A
STAT INDICATION						
I_{STAT_SINK}	STAT pin sink current		6			mA
F_{BLINK2}	STAT pin blink frequency			1		Hz
F_{BLINK_DUTY}	STAT pin blink duty cycle			50		%
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy		111	120	133	°C
T_{SHUT}	Thermal Shutdown Rising threshold	Temperature increasing		150		°C

8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, L=2.2µH, TJ = -40°C to +125°C, and TJ = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Thermal Shutdown Falling threshold	Temperature decreasing		125		°C
BUCK MODE OPERATION						
F_{SW}	PWM switching frequency	SW node frequency	1.02	1.20	1.38	MHz
D_{MAX}	Maximum PWM Duty Cycle			97.0		%
REGN LDO						
V_{REGN_UVLO}	REGN UVLO	V_{VBUS} rising			3.85	V
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5V, I_{REGN} = 0 to 16mA	4.20		5.0	V
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 12V, I_{REGN} = 16mA	4.50		5.40	V
ICHG SETTING						
V_{ICHG}	ICHG pin regulated voltage		993	998	1003	mV
$R_{ICHG\_SHORT\_FALL}$	Resistance to disable charge		1.00			kΩ
$R_{ICHG\_OPEN\_RISE}$	Resistance to disable charge				565	kΩ
R_{ICHG}	Programmable resistance at ICHG	V_{BUS} = 5V, resistance decrease	11.70		250	kΩ
R_{ICHG_HIGH}	ICHG setting resistor threshold to clamp precharge and termination current to 63mA	R_{ICHG} > R_{ICHG_HIGH}	60.0	65.0	70.0	kΩ
JEITA THERMISTOR COMPARATORS						
V_{T1}%	T1 (0°C) threshold, charge suspended if thermistor temperature is below T1	V_{TS} rising, charger suspends charge. As Percentage to V_{REGN}	72.68	73.5	74.35	%
V_{T1}%	V_{TS} falling	As Percentage to V_{REGN}	70.68	71.5	72.33	%
V_{T2}%	T2 (10°C) threshold, charge current is reduced to 20% of ICHG	V_{TS} rising. As Percentage to V_{REGN}	67.7	68.5	69.5	%
V_{T2}%	V_{TS} falling	As Percentage to V_{REGN}	66.5	67.3	68.2	%
V_{T3}%	T3 (45°C) threshold, charge at 50% of ICHG and VREG = 4.1V above this temperature	V_{TS} falling. As Percentage to V_{REGN}	46.35	47.25	48.15	%
V_{T3}%	V_{TS} Rising	As Percentage to V_{REGN}	47.35	48.25	49.15	%
V_{T5}%	T5 (60°C) threshold, charge suspended above this temperature.	V_{TS} falling. As Percentage to V_{REGN}	36.95	37.75	38.55	%
V_{T5}%	V_{TS} Rising	As Percentage to V_{REGN}	37.95	38.75	39.55	%
COLD/HOT THERMISTOR COMPARATOR						
LOGIC I/O PIN CHARACTERESTICS (POL, EN)						
V_{ILO}	Input low threshold	Falling			0.40	V
V_{IH}	Input high threshold	Rising	1.3			V
I_{BIAS}	High-level leakage current at $\overline{EN}$ pin	$\overline{EN}$ pin is pulled up to 1.8 V		1.0		µA

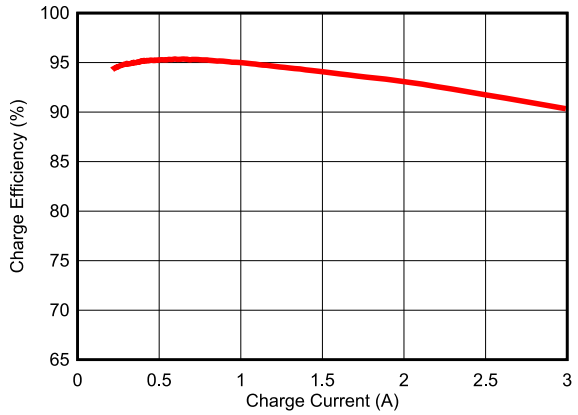
8.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
$t_{CHG\_ON\_EN}$	Delay from enable at /EN pin to charger power on	/EN pin voltage rising		245		ms
$t_{CHG\_ON\_VBUS}$	Delay from VBUS to charge start	/EN pin is grounded, batttery present		275		ms
BATTERY CHARGER						
t_{SAFETY_FAST}	Charge safety timer	Fast charge safety timer 20 hours	15.0	20.0	24.0	hr

8.6 Timing Requirements (continued)

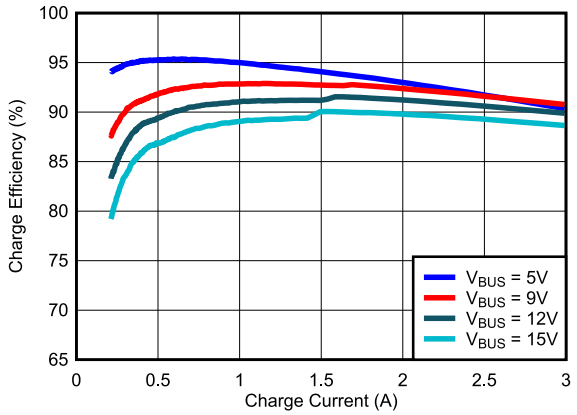
PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t_{SAFETY_PRE}	Charge safety timer	Precharge safety timer	1.5	2.0	2.5	hr

8.7 Typical Characteristics



f_{SW} = 1.2 MHz
V_{VBUS} = 5.0 V, V_{BAT} = 3.8 V
Inductance = 1.0 uH
Inductor DCR = 10 mΩ

Figure 8-1. 1-Cell Battery Charge Efficiency vs. Charge Current



f_{SW} = 1.2 MHz
V_{BAT} = 3.8 V
Inductance = 2.2 uH
Inductor DCR = 20 mΩ

Figure 8-2. 1-Cell Battery Charge Efficiency vs. Charge Current

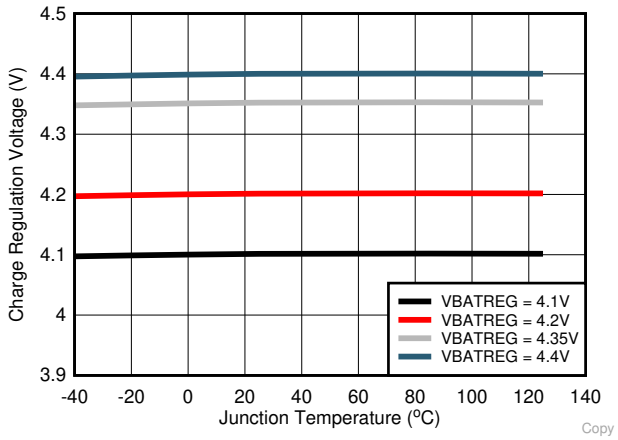


Figure 8-3. Battery Charge Regulation Voltage vs. Junction Temperature

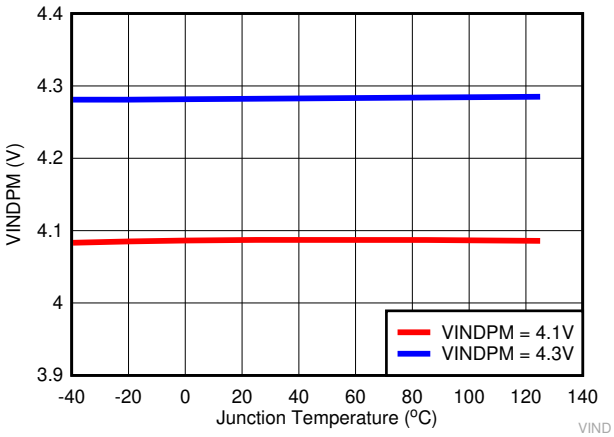


Figure 8-4. VINDPM vs. Junction Temperature

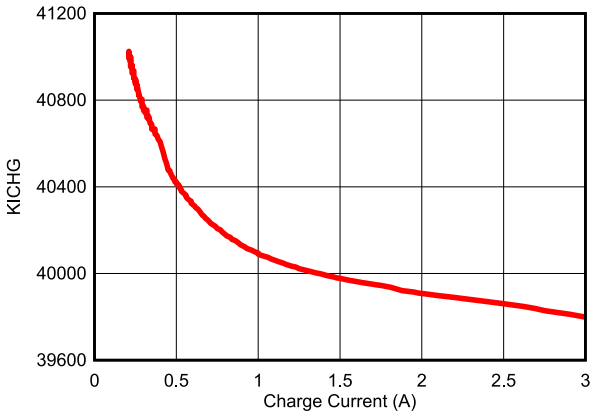


Figure 8-5. KICHG vs. Charge Current

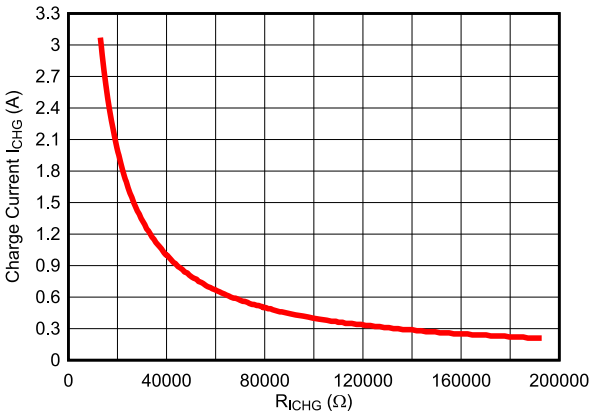


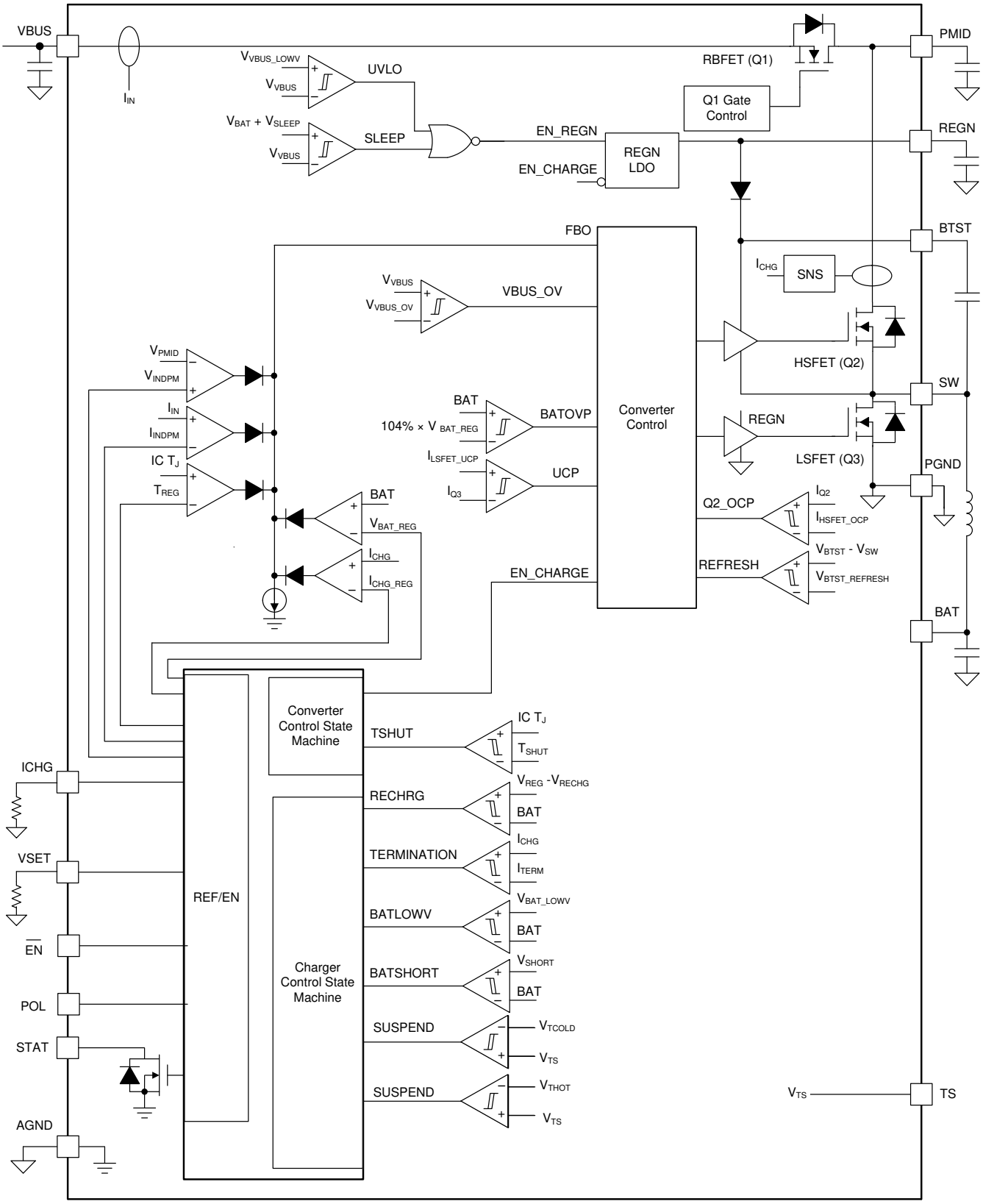
Figure 8-6. Charge Current vs. Charge Current Setting Resistance RICHG

9 Detailed Description

9.1 Overview

The BQ25303J is a highly integrated standalone switch-mode battery charger for single cell Li-Ion and Li-polymer batteries with charge voltage and charge current programmable by an external resistor. It includes an input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and bootstrap diode for the high-side gate drive as well as current sensing circuitry.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Device Power Up

The $\overline{EN}$ pin enable or disable the device. When the device is disabled, the device draws minimum current from VBUS pin. The device can be powered up from either VBUS or by enabling the device from $\overline{EN}$ pin.

9.3.1.1 Power-On-Reset (POR)

The $\overline{EN}$ pin can enable or disable the device. When the device is disabled, the device is in disable mode and it draws minimum current at VBUS. When the device is enabled, if VBUS rises above V_{VBUS_UVLOZ}, the device powers part of internal bias and comparators and starts Power on Reset (POR).

9.3.1.2 REGN Regulator Power Up

The internal bias circuits are powered from the input source. The REGN supplies internal bias circuits as well as the HSFET and LSFET gate drive. The REGN also provides voltage rail to STAT LED indication. The REGN is enabled when all the below conditions are valid:

- Chip is enabled by $\overline{EN}$ pin
- V_{VBUS} above V_{VBUS_UVLOZ}
- V_{VBUS} above V_{BAT} + V_{SLEEPZ}
- After sleep comparator deglitch time, VSET detection time, and REGN delay time

REGN remains on at fault conditions. REGN is powered by VBUS only and REGN is off when VBUS power is removed.

9.3.1.3 Charger Power Up

Following REGN power-up, if there is no fault conditions, the charger powers up with soft start. If there is any fault, the charger will remain off until fault is clear. Any of the fault conditions below gates charger power-up:

- V_{VBUS} > V_{VBUS_OVP}
- Thermistor cold/hot fault on TS pin
- V_{BAT} > V_{BAT_OVP}
- Safety timer fault
- ICHG pin is open or short to GND
- Die temperature is above TSHUT

9.3.1.4 Charger Enable and Disable by $\overline{EN}$ Pin

With POL pin floating, the charger can be enabled with $\overline{EN}$ pin pulled low (or floating) or disabled by $\overline{EN}$ pin pulled high. The charger is in disable mode when disabled.

9.3.1.5 Device Unplugged from Input Source

When V_{BUS} is removed from an adaptor, the device stays in HiZ mode and the leakage current from the battery to BAT pin and SW pin is less than $I_{Q\_BAT\_HIZ}$.

9.3.2 Battery Charging Management

The BQ25303J charges 1-cell Li-Ion battery with up to 3.0-A charge current from 4.1-V to 17-V input with JEITA battery temperature monitoring.A new charge cycle starts when the charger power-up conditions are met. The charge voltage is set by external resistor connected at VSET pin and charge current are set by external resistors at ICHG pin. The charger terminates the charging cycle when the charging current is below termination threshold I_{TERM} and charge voltage is above recharge threshold(V_{BATREG} - V_{RECHG_HYS}), and device is not in IINDPM or thermal regulation. When a fully charged battery's voltage is discharged below recharge threshold, the device automatically starts a new charging cycle with safety timer reset. To initiate a recharge cycle, the conditions of charger power-up must be met. The STAT pin output indicates the charging status of charging (LOW), charging complete or charge disabled (HIGH) or charging faults (BLINKING).

9.3.2.1 Battery Charging Profile

The device charges the battery in four phases: battery short, preconditioning, constant current, constant voltage. The device charges battery based on charge voltage set by VSET pin and charge current set by ICHG pin as well as actual battery voltage. The battery charging profile is shown in Figure 9-1. The battery short current is provided by internal linear regulator.

Table 9-1. Charging Current Setting

MODE	BATTERY VOLTAGE V_{BAT}	CHARGE CURRENT	TYPICAL VALUE
Battery Short	$V_{BAT} < V_{BAT\_SHORT}$	I_{BAT_SHORT}	35 mA
Precharge	$V_{BAT\_SHORT} < V_{BAT} < V_{BAT\_LOWV}$	I_{PRECHG}	10% of I_{CHG} (I_{PRE} > 63mA)
Fast Charge	$V_{BAT\_LOWV} < V_{BAT}$	I_{CHG}	Set by ICHG resistor

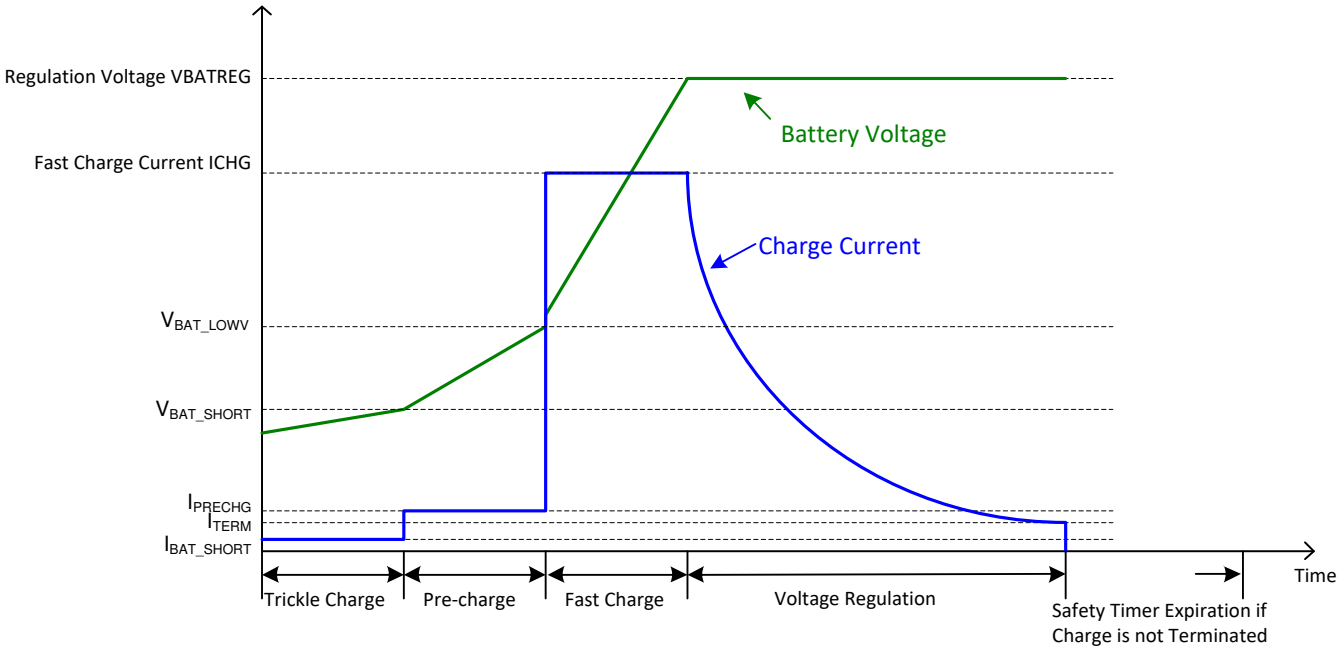


Figure 9-1. Battery Charging Profile

9.3.2.2 Precharge

The device charges the battery at 10% of set fast charge current in precharge mode. When $R_{ICHG} > R_{ICHG\_HIGH}$, the precharge current is clamped at 63mA.

9.3.2.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold and the charge current is below termination current. After a charging cycle is completed, the converter stops swicthing, charge is terminated and the system load is powered from battery. Termination is temporarily disabled when the charger device is in input current regulation or thermal regulation mode and the charging safety timer is counted at half the clock rate. The charge termination current is 10% of set fast charge current if $R_{ICHG} < R_{ICHG\_HIGH}$. The termination current is clamped at 63mA if $R_{ICHG} > R_{ICHG\_HIGH}$.

9.3.2.4 Battery Recharge

A charge cycle is completed when battery is fully charged with charge terminated. If the battery voltage decreases below the recharge threshold (V_{BATREG} - V_{RECHG_HYS}), the charger is enabled with safety timer reset and enabled.

9.3.2.5 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 20 hours when the battery voltage is above V_{BAT_LOWV} threshold and 2 hours below V_{BAT_LOWV} threshold. When the safety timer expires, charge is suspended until the safety timer is reset. Safety timer is reset and charge starts under one of the following conditions:

- Battery voltage falls below recharge threshold
- VBUS voltage is recycled
- $\overline{EN}$ pin is toggled
- Battery voltage transits across V_{BAT_SHORT} threshold
- Battery voltage transits across V_{BAT_LOWV} threshold

If the safety timer expires and the battery voltage is above recharge threshold, the charger is suspended and the STAT pin is open. If the safety timer expires and the battery voltage is below the recharge threshold, the charger is suspended and the STAT pin blinks to indicate a fault. The safety timer fault is cleared with safety timer reset.

During input current regulation, thermal regulation, JEITA COOL and JEITA WARM, the safety timer counts at half the original clock frequency and the safety timer is doubled. During TS fault, V_{BUS_OVP}, V_{BAT_OVP}, ICHG pin open and short, and IC thermal shutdown faults, the safety timer is suspended. Once the fault(s) is clear, the safety timer resumes to count.

9.3.2.6 Thermistor Temperature Monitoring

The charger device provides a single thermistor input TS pin for battery temperature monitor. To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges. To initiate a charge cycle, the voltage on TS pin must be within the V_{T1}% to V_{T5}% thresholds. If TS voltage is out of T1-T5 temperature range, the charger stops charging and waits until the battery temperature is within the T1 to T5 range. .

At cool temperature (T1-T2), the charge current is reduced to 20% of the set fast charge if $R_{ICHG} < R_{ICHG\_HIGH}$. If $R_{ICHG} > R_{ICHG\_HIGH}$, the charge current is reduced to 50% of fast charge current in cool charge. At normal temperature (T2 - T3), the charger charges battery as fast charge and the fast charge current is set by a resister at ICHG pin. At warm temperature (T3 -T5), the charge voltage is reduced to 4.1 V and 50% of fast charge current. If the charge voltage is set below 4.1V, the charge voltage will remain unchanged during warm charge.

RT1 and RT2 programs temperatures from T1 to T5. In the equations, $R_{NTC,T1}$ is NTC thermistor resistance value at temperature T1 and $R_{NTC,T5}$ is NTC thermistor resistance values at temperature T5. Select 0°C to 60°C for battery charge temperature range, then NTC thermistor 103AT-2 thermistor resistance is $R_{NTC,T1}$ = 27.28 kΩ (at 0°C) and $R_{NTC,T5}$ = 3.02 kΩ (at 60°C), from the Equation 1 and Equation 2, RT1 and RT2 are derived as:

• RT1 = 4.32 kΩ

• RT1 = 21 kΩ

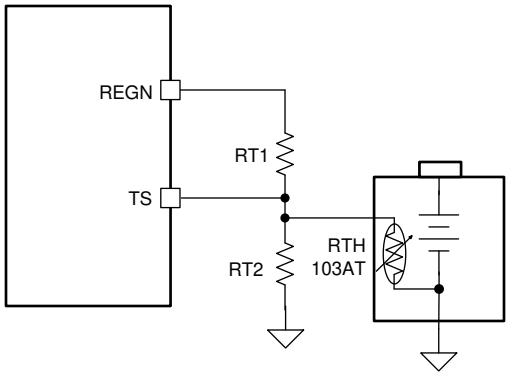


Figure 9-2. Battery Temperature Sensing Circuit

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}\%} - \frac{1}{V_{T1}\%}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}\%} - 1\right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}\%} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{T1}\%} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \quad (2)$$

(3)

(4)

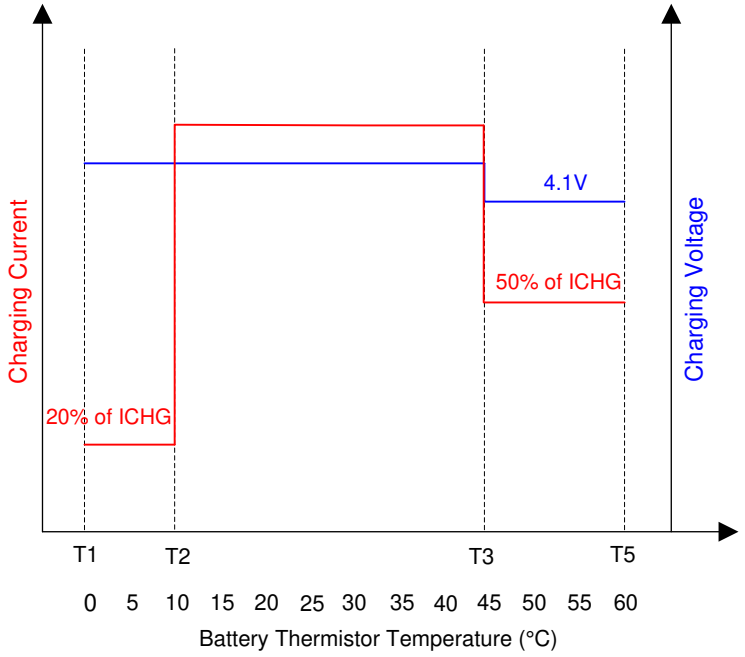


Figure 9-3. JEITA Profile

9.3.3 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive a LED that is pulled up to REGN rail through a current limit resistor.

Table 9-2. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging complete	HIGH
HiZ mode, sleep mode, charge disable	HIGH
Safety timer expiration with battery voltage above recharge threshold	HIGH
Charge faults: 1. VBUS input over voltage 2. TS cold/hot faults 3. Battery over voltage 4. IC thermal shutdown 5. Safety timer expiration with battery voltage below recharge threshold 6. ICHG pin open or short	BLINKING at 1 Hz with 50% duty cycle

9.3.4 Protections

9.3.4.1 Voltage and Current Monitoring

The device closely monitors the input voltage and input current for safe operation.

9.3.4.1.1 Input Over-Voltage Protection

This device integrates the functionality of an input over-voltage protection (OVP). The input OVP threshold is $V_{VBUS\_OVP\_RISE}$. During an input over-voltage event, the converter stops switching and safety timer stops counting as well. The converter resumes switching and the safety timer resumes counting once the VBUS voltage drops back below ($V_{VBUS\_OVP\_RISE}$ - $V_{VBUS\_OVP\_HYS}$). The REGN LDO remains on during an input over-voltage event. The STAT pin blinks during an input OVP event.

9.3.4.1.2 Input Voltage Dynamic Power Management (VINDPM)

When the input current of the device exceeds the current capability of the power supply, the charger device regulates PMID voltage by reducing charge current to avoid crashing the input power supply. VINDPM dynamically tracks the battery voltage. The actual VINDPM is the higher of V_{INDPM_MIN} and (1.044*VBAT + 125mV).

9.3.4.1.3 Input Current Limit

The device has built-in input current limit. When the input current is over the threshold I_{INDPM}, the converter duty cycle is reduced to reduce input current.

9.3.4.1.4 Cycle-by-Cycle Current Limit

High-side (HS) FET current is cycle-by-cycle limited. Once the HSFET peak current hits the limit I_{HSFET_OCP}, the HSFET shuts down until the current is reduced below a threshold.

9.3.4.2 Thermal Regulation and Thermal Shutdown

The device monitors the junction temperature T_J to avoid overheating the chip and limit the device surface temperature. When the internal junction temperature exceeds thermal regulation limit T_{REG}, the device lowers down the charge current. During thermal regulation, the average charging current is usually below the programmed battery charging current. Therefore, termination is disabled and the safety timer runs at half the clock rate.

Additionally, the device has thermal shutdown built in to turn off the charger when device junction temperature exceeds T_{SHUT} rising threshold. The charger is reenabled when the junction temperature is below T_{SHUT} falling threshold. During thermal shutdown, the safety timer stops counting and it resumes when the temperature drops below the threshold.

9.3.4.3 Battery Protection

9.3.4.3.1 Battery Over-Voltage Protection (V_{BAT_OVP})

The battery voltage is clamped at above the battery regulation voltage. When the battery voltage is over $V_{BAT\_OVP\_RISE}$, the converter stops switching until the battery voltage is below the falling threshold. During a battery over-voltage event, the safety timer stops counting and STAT pin reports the fault and it resumes once the battery voltage falls below the falling threshold. A 7-mA pull-down current is on the BAT pin once BAT_OVP is triggered. BAT_OVP may be triggered in charging mode, termination mode, and fault mode.

9.3.4.3.2 Battery Short Circuit Protection

When the battery voltage falls below the V_{BAT_SHORT} threshold, the charge current is reduced to I_{BAT_SHORT}.

9.3.4.4 ICHG Pin Open and Short Protection

To protect against ICHG pin is short or open, the charger immediately shuts off once ICHG pin is open or short to GND and STAT pin blinks to report the fault. At powerup, if ICHG pin is detected open or short to GND, the charge will not power up until the fault is clear.

9.4 Device Functional Modes

9.4.1 Disable Mode, HiZ Mode, Sleep Mode, Charge Mode, Termination Mode, and Fault Mode

The device operates in different modes depending on VBUS voltage, battery voltage, and $\overline{EN}$ pin, POL pin, and ICHG pin connection. The functional modes are listed in the following table.

Table 9-3. Device Functional Modes

MODE	CONDITIONS	REGN LDO	CHARGE ENABLED	STAT PIN
Disable Mode	Device is disabled, POL floating or pulled high, and $\overline{EN}$ pulled high	OFF	NO	OPEN
	Device is disabled, POL pulled low, $\overline{EN}$ pulled low or floating	OFF	NO	OPEN
HiZ Mode	Device is enabled and $V_{VBUS} < V_{VBUS\_UVLOZ}$	OFF	NO	OPEN
Sleep Mode	Device is enabled and $V_{VBUS} > V_{VBUS\_UVLOZ}$ and $V_{VBUS} < V_{BAT} + V_{SLEEPZ}$	OFF	NO	OPEN
Charge Mode	Device is enabled, $V_{VBUS} > V_{VBUS\_LOWV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$, no faults, charge is not terminated	ON	YES	SHORT to GND
Charge Termination Mode	$V_{VBUS} > V_{VBUS\_LOWV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$ and device is enabled, no faults, charge is terminated	ON	NO	OPEN
Fault Mode	V_{BUS_OVP}, TS cold/hot, V_{BAT_OVP}, IC thermal shutdown, safety timer fault, ICHG pin open or short	ON	NO	BLINKING

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

A typical application consists of a single cell battery charger for Li-Ion, Li-polymer batteries used in a wide range of portable devices and accessories. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), and low-side switching FET (LSFET, Q3). The Buck converter output is connected to the battery directly to charge the battery and power system loads. The device also integrates a bootstrap diode for high-side gate drive.

10.2 Typical Applications

The typical applications in this section include a standalone charger without power path, and a standalone charger with external power path.

10.2.1 Typical Application

The typical application in this section includes a standalone charger without power path.

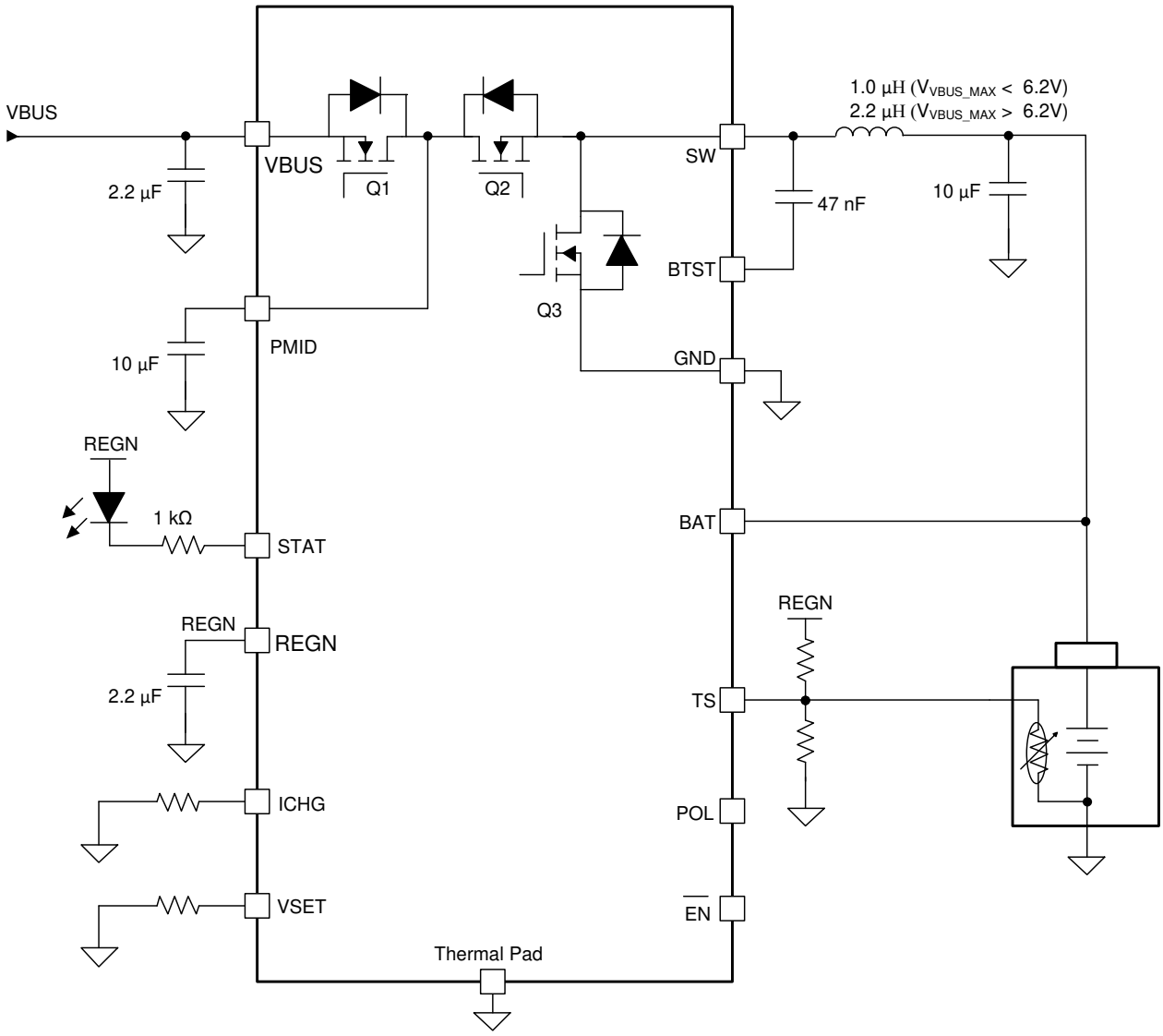


Figure 10-1. Typical Application Diagram

10.2.1.1 Design Requirements

Table 10-1. Design Requirements

PARAMETER	VALUE
Input Voltage	4.1V to 17V
Input Current	3.0A
Fast Charge Current	3.0A
Battery Regulation Voltage	4.1V/4.2V/4.35V/4.4V

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Charge Voltage Settings

Battery charge voltage is set by a resistor connected at the VSET pin. When the REGN LDO startup conditions are met, and before the REGN LDO powers up, the internal VSET detection circuit is enabled to detect VSET pin

resistance and set battery charge voltage accordingly. The VSET detection circuit is disabled after detection is complete and changing resistance values on the fly does not change the battery charge voltage. VSET detection is reenabled once the REGN LDO is recycled.

10.2.1.2.2 Charge Current Setting

The charger current is set by the resistor value at the ICHG pin according to the equation below:

I_{CHG} (A) = K_{ICHG} (A·Ω) / R_{ICHG}(Ω)

K_{ICHG} is a coefficient that is listed in Electrical Characteristics table and R_{ICHG} is the resistor value from ICHG pin to GND. K_{ICHG} is typically 40,000 (A·Ω) and it is slightly shifted up at lower charge current setting. The K_{ICHG} vs. ICHG typical characteresitc curve is shown in Figure 8-5.

10.2.1.2.3 Inductor Selection

The 1.2-MHz switching frequency allows the use of small inductor and capacitor values. Inductance value is selected based on maximum input voltage V_{VBUS_MAX} in applications. 1-µH inductor is recommended if V_{VBUS_MAX} < 6.2V and 2.2-µH inductor is recommended if V_{VBUS_MAX} > 6.2V. An inductor saturation current I_{SAT}should be higher than the charging curren I_{CHG} plus half the ripple current I_{RIPPLE}:

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{5}$$

The inductor ripple current I_{RIPPLE} depends on the input voltage (V_{VBUS}), the duty cycle (D = V_{BAT}/V_{VBUS}), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \tag{6}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5.

10.2.1.2.4 Input Capacitor

Design input capacitance to provide enough ripple current rating to absorb the input switching ripple current. Worst case RMS ripple current is half of the charging current when the duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{Cin} occurs where the duty cycle is closest to 50% and can be estimated using Equation 7.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{7}$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for the input decoupling capacitor and should be placed as close as possible to the drain of the high-side MOSFET and source of the low-side MOSFET. The voltage rating of the capacitor must be higher than the normal input voltage level. A rating of 25-V or higher capacitor is preferred for 15-V input voltage.

10.2.1.2.5 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. The equation below shows the output capacitor RMS current I_{COUT} calculation.

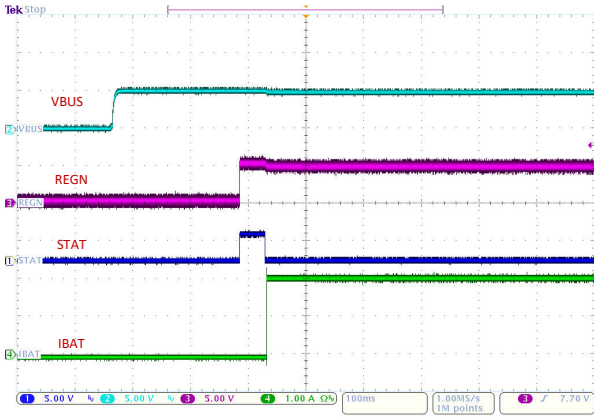
$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{8}$$

The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{9}$$

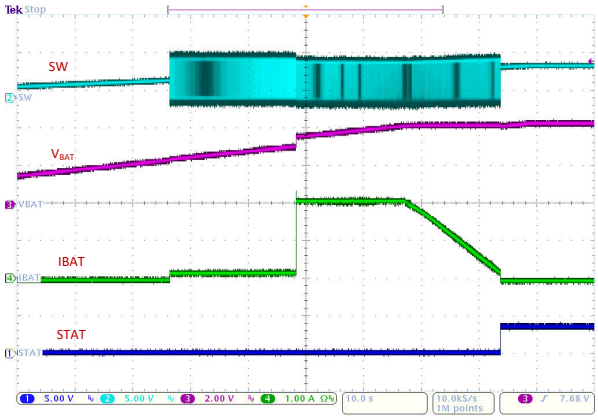
At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

10.2.1.3 Application Curves



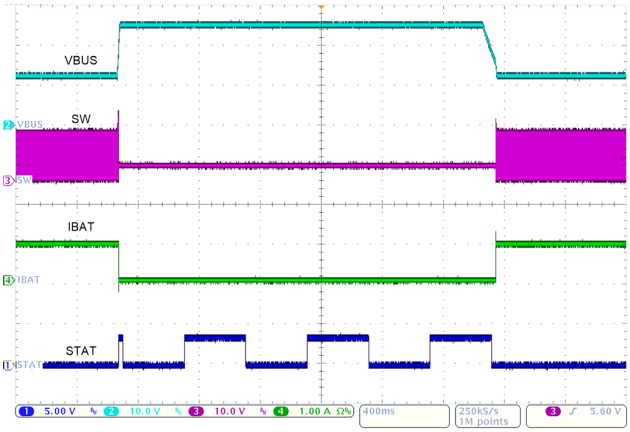
VBUS = 5 V
ICHG = 2A
Device Enabled

Figure 10-2. Power Up from VBUS



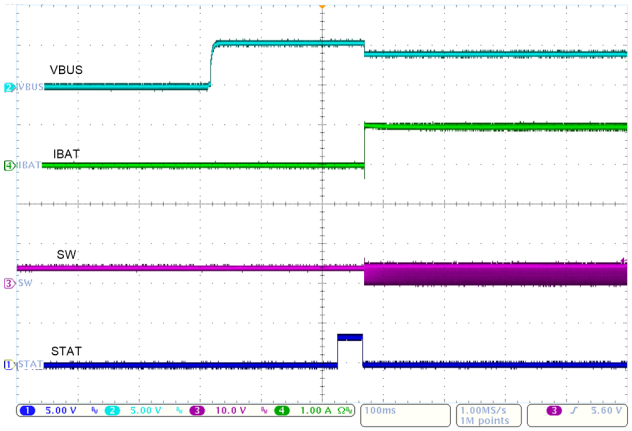
VBUS = 5 V
ICHG = 2 A
VBAT = 1.5V - 4.2V
VBATREG = 4.2V

Figure 10-3. Charge Cycle



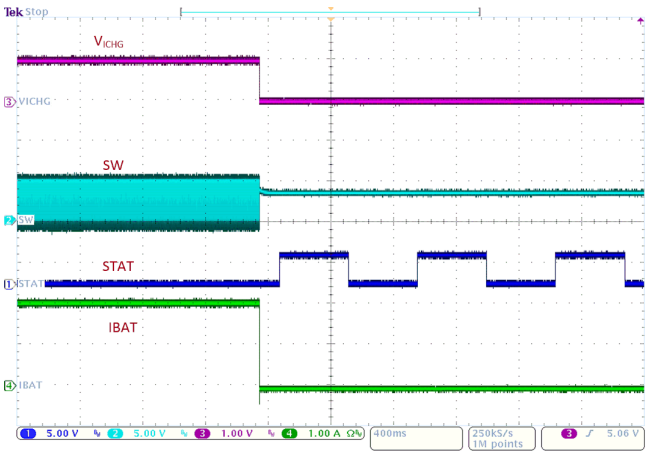
VBUS = 12V -25V -12V
ICHG = 1A
VBAT = 3.8V

Figure 10-4. VBUS Over Voltage Protection



VBUS = 5 V
ICHG = 2A
Adaptor Currrent Limit: 1A
VBAT = 3.5V

Figure 10-5. VBUS startup into VINDPM



VBUS = 5 V

From ICHG = 2A to ICHG pin short

Figure 10-6. ICHG Pin Short Circuit Protection

10.2.2 Typical Application with External Power Path

In the case where a system needs to be immediately powered up from VBUS when the battery is overdischarged or dead, the application circuit shown in Figure 10-7 can be used to provide a power path from VBUS/PMID to VSYS. PFET Q4 is an external PFET that turns on to supply VSYS from the battery when VBUS is removed; PFET Q4 turns off when VBUS is plugged in and VSYS is supplied from VBUS/PMID.

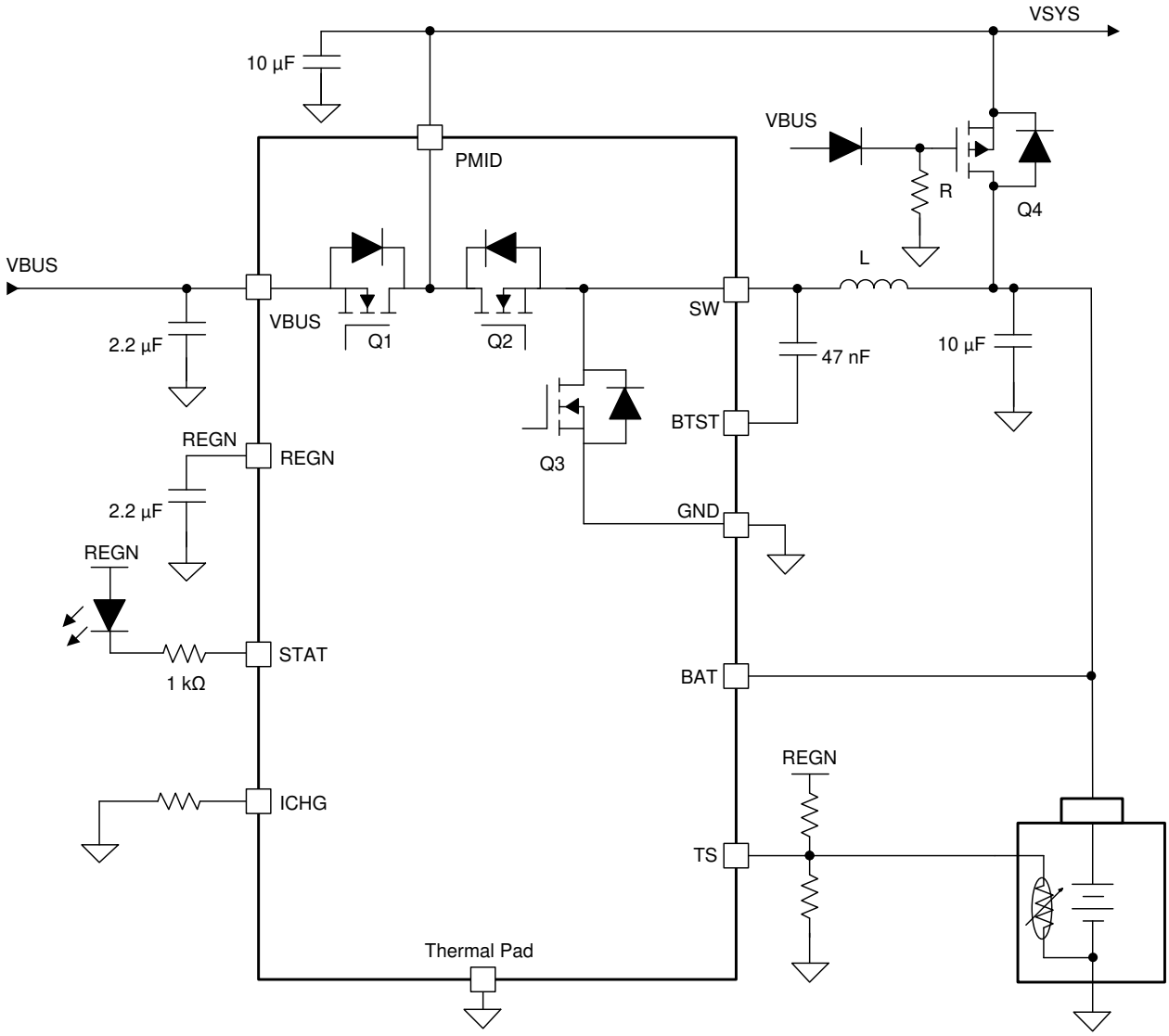


Figure 10-7. Typical Application Diagram with Power Path

10.2.2.1 Design Requirements

For design requirements, see Section 10.2.1.1.

10.2.2.2 Detailed Design Procedure

For detailed design procedure, see Section 10.2.1.2.

10.2.2.3 Application Curves

For application curves, see Section 10.2.1.3.

11 Power Supply Recommendations

In order to provide an output voltage on the BAT pin, the device requires a power supply between 4.1 V and 17 V Li-Ion battery with positive terminal connected to BAT. The source current rating needs to be at least 3 A in order for the buck converter to provide maximum output power to BAT or the system connected to BAT pin.

12 Layout

12.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 12-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor as close as possible to PMID pin and use shortest thick copper trace to connect input capacitor to PMID pin and GND plane.
- It is critical that the exposed thermal pad on the backside of the device be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers. Connect the GND pins to thermal pad on the top layer.
- Put output capacitor near to the inductor output terminal and the charger device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
- Route analog ground separately from power ground if possible. Connect analog ground and power ground together using thermal pad as the single ground connection point under the charger device. It is acceptable to connect all grounds to a single ground plane if multiple ground planes are not available.
- Decoupling capacitors should be placed next to the device pins and make trace connection as short as possible.
- For high input voltage and high charge current applications, sufficient copper area on GND should be budgeted to dissipate heat from power losses.
- Ensure that the number and sizes of vias allow enough copper for a given current path

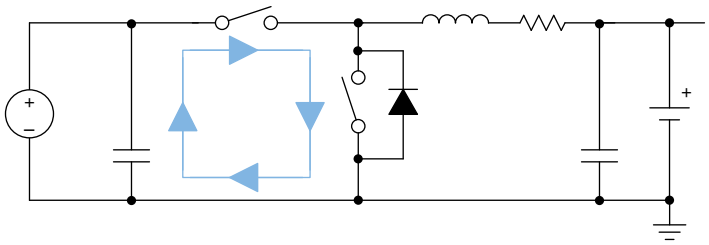


Figure 12-1. High Frequency Current Path

12.2 Layout Example

The device pinout and component count are optimized for a 2 layer PCB design. The 2-layer PCB layout example is shown in Figure 12-2.

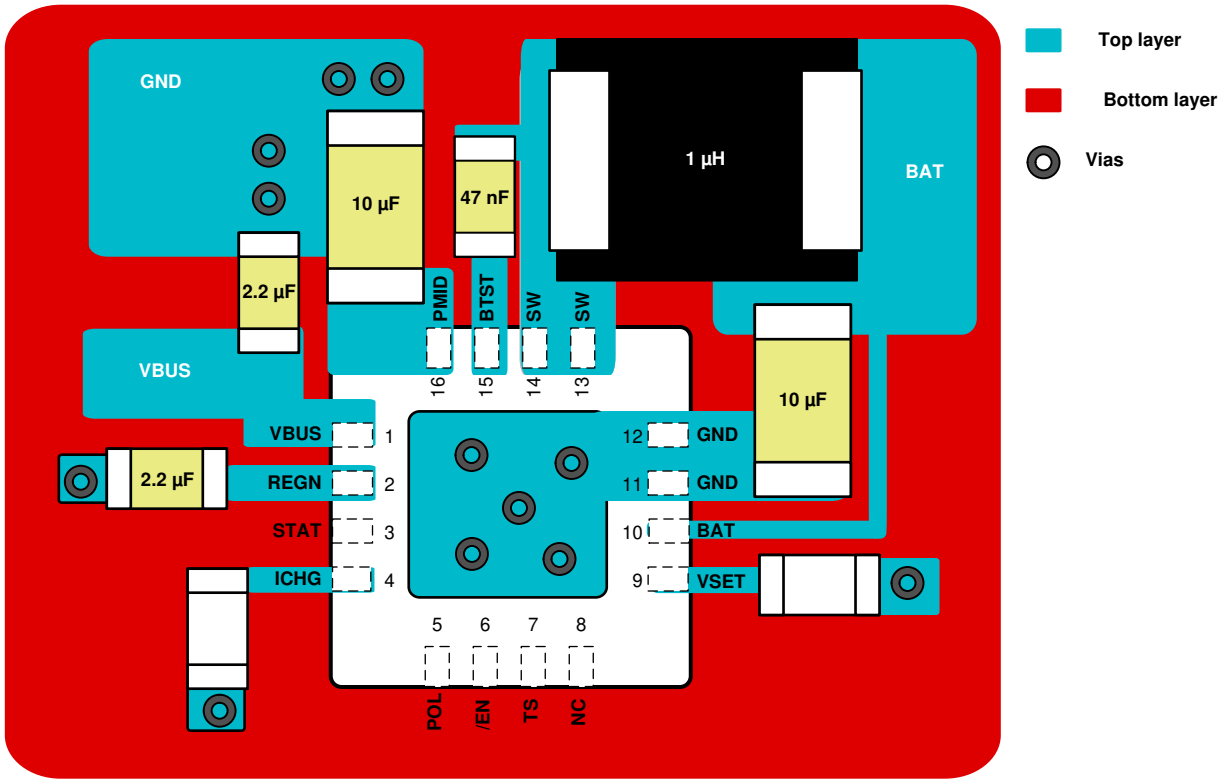


Figure 12-2. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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13.4 Trademarks

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13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25303JRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ303J	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

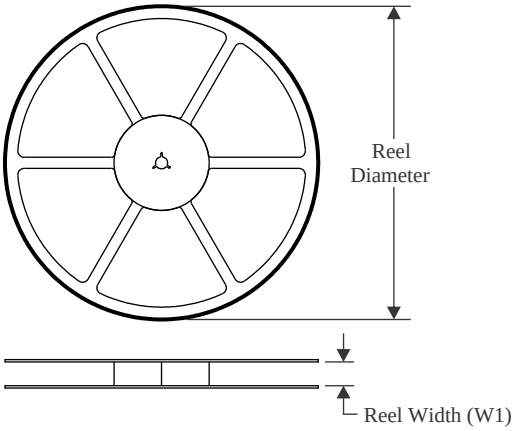
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

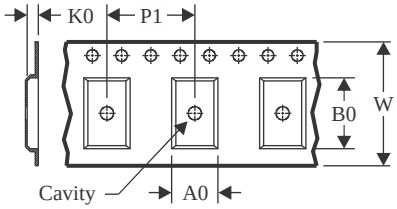
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

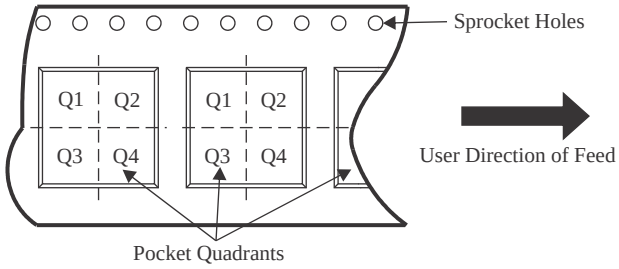


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

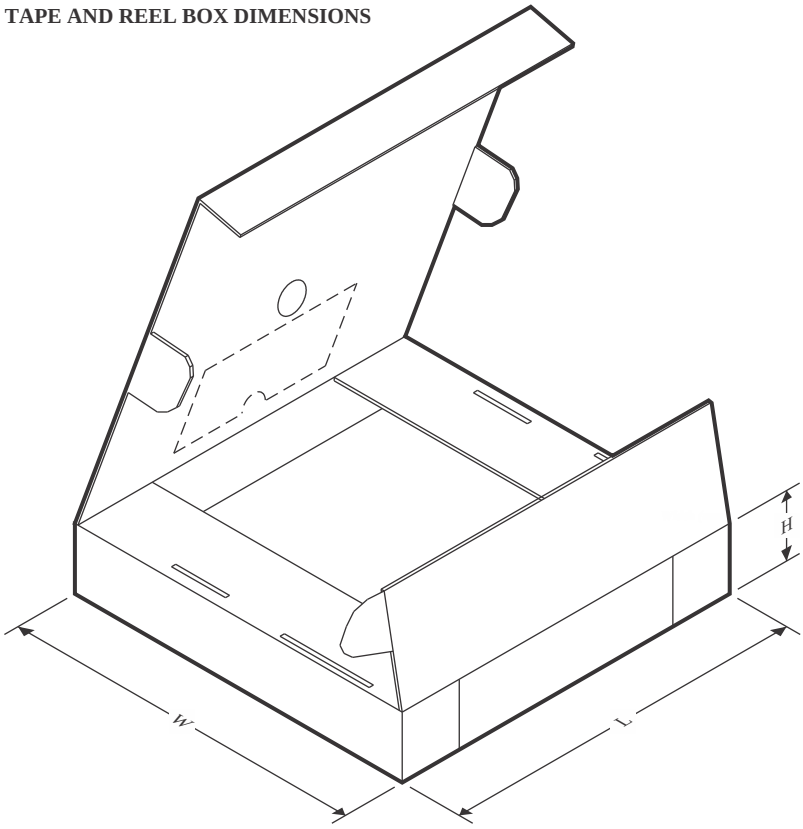
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25303JRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
BQ25303JRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25303JRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
BQ25303JRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

GENERIC PACKAGE VIEW

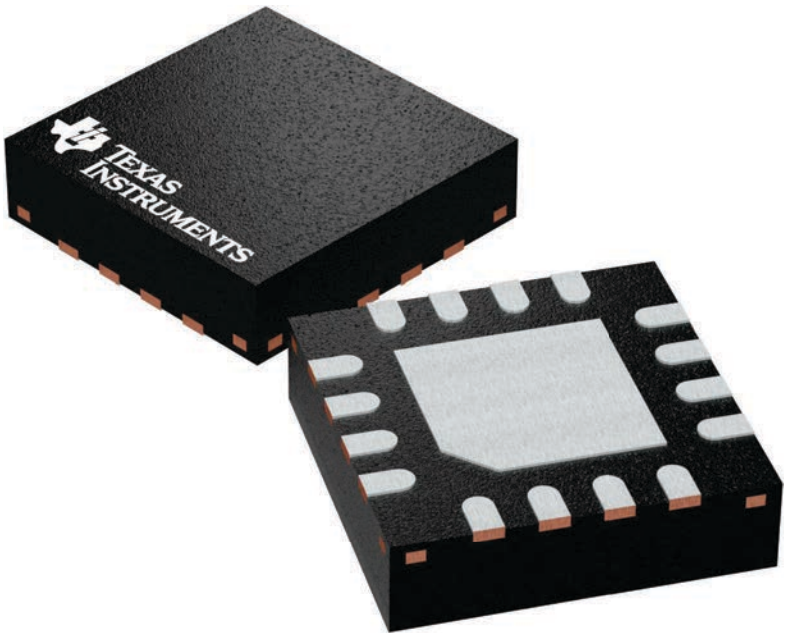
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

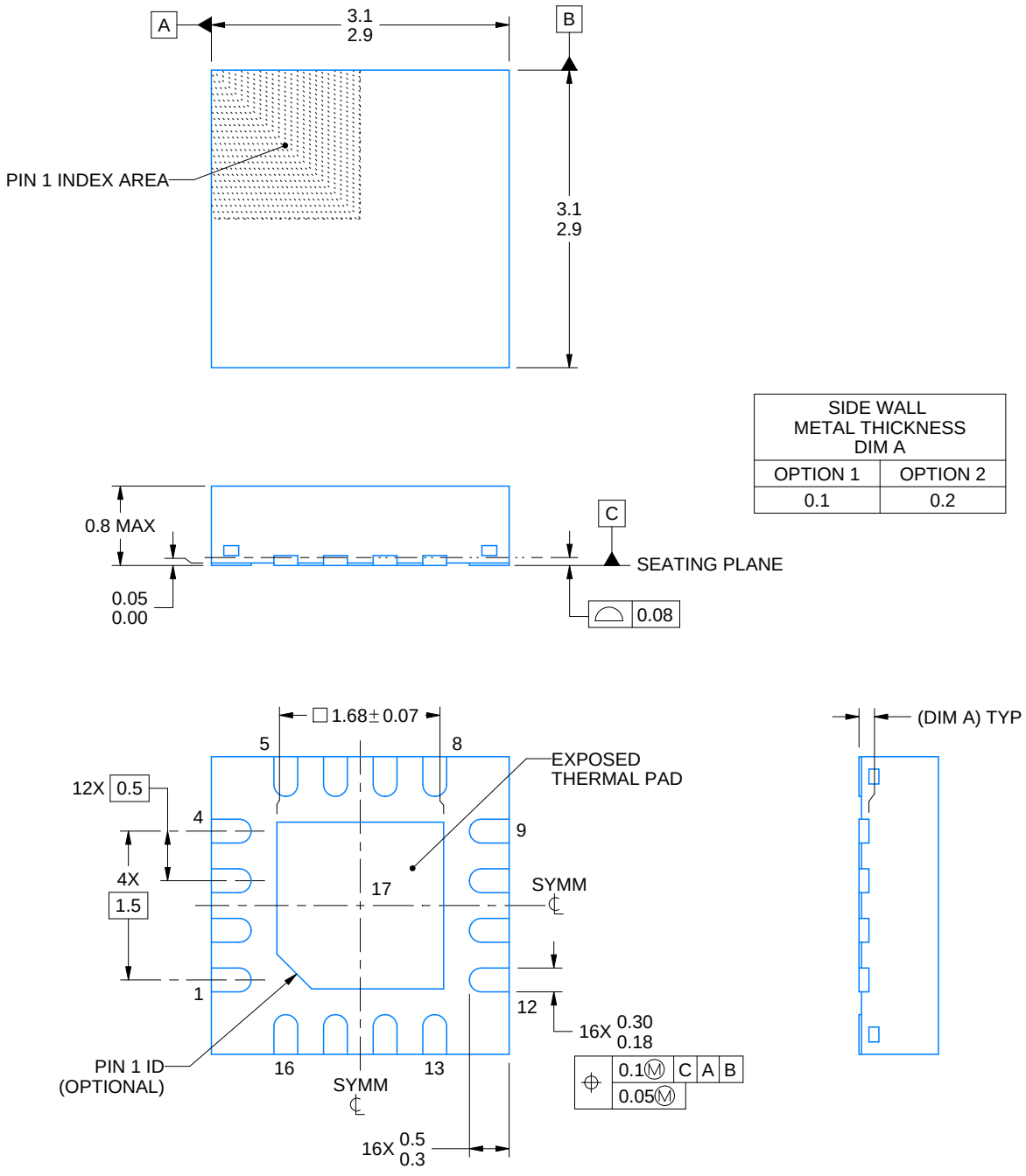


RTE0016C

PACKAGE OUTLINE

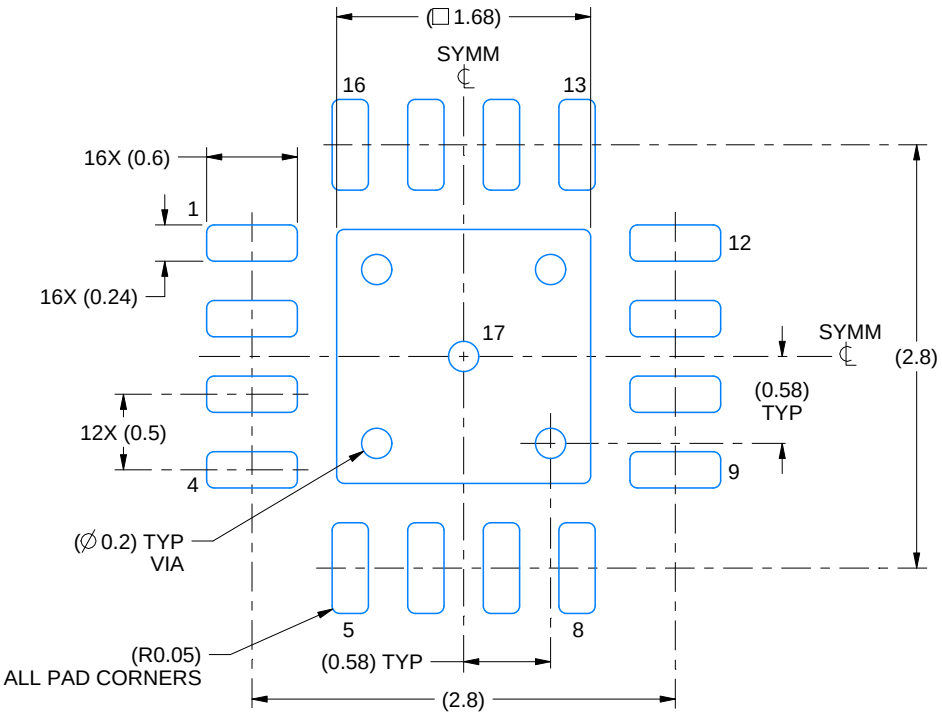
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

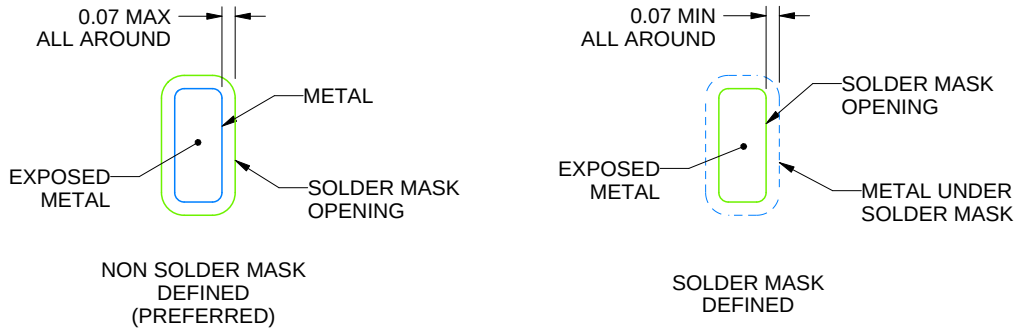


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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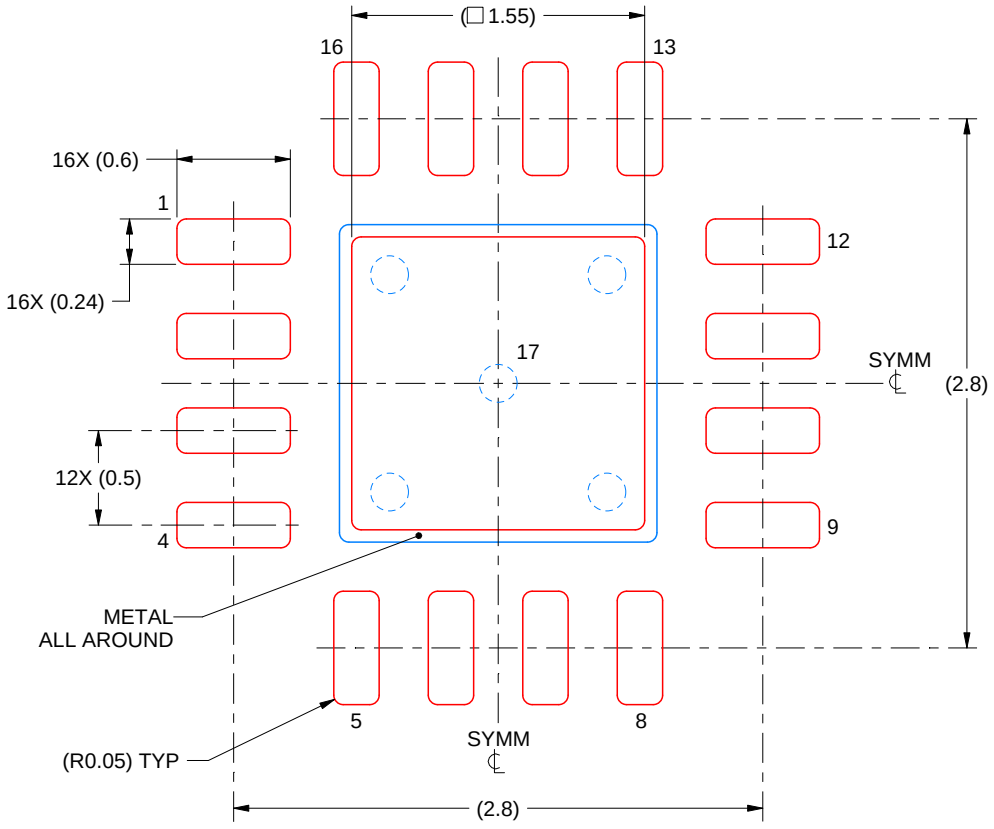
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265