BQ769142 Technical Reference Manual

Technical Reference Manual

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About This Manual

This technical reference manual (TRM) discusses the modules and peripherals of the BQ769142 device, and how each is used to build a complete battery pack monitor and protection solution. For details on the hardware device features and electrical specifications, see *BQ769142 3-Series to 14-Series High Accuracy Battery Monitor and Protector for Li-Ion, Li-Polymer, and LiFePO$_4$ Battery Packs* (SLUSE91).

Battery Monitor Notational Conventions

The following notation is used if commands, subcommands, and data memory values are mentioned within a text block:

- Commands and subcommands: *italics* with parentheses and no breaking spaces, for example, *Battery Status()*
- Data memory: *italics*, **bold**, and breaking spaces; for example, ***Power Config***
- Register bits and flags: *italics* and brackets; for example, *[TDA]*
- Data memory bits: *italics* and **bold**; for example, ***[LED1]***
- Modes and states: ALL CAPITALS; for example, DEEPSLEEP

Trademarks

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Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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Chapter 1

Introduction

The Texas Instruments BQ769142 is a highly integrated, high accuracy battery monitor and protector for 3-series to 14-series Li-ion, Li-polymer, and $LiFePO_4$ battery packs. The device includes a high accuracy monitoring system, a highly configurable protection subsystem, and support for autonomous or host-controlled cell balancing. Integration includes high-side charge-pump NFET drivers, dual programmable LDOs for external system use, and a host communication peripheral supporting 400-kHz I^2C, SPI, and HDQ one-wire standards. Device features include:

- Battery monitoring capability for 3-series to 14-series cells
- Integrated charge pump for high-side NFET protection with optional autonomous recovery
- Extensive protection suite including voltage, temperature, current, and internal diagnostics
- Two independent ADCs
  - Support for simultaneous current and voltage sampling
  - High-accuracy coulomb counter with input offset error < 1 µV (typical)
  - High accuracy cell voltage measurement < 10 mV (typical)
- Wide-range current applications (±200-mV measurement range across sense resistor)
- Integrated secondary chemical fuse drive protection
- Autonomous or host-controlled cell balancing
- Multiple power modes (typical battery pack operating range conditions)
  - NORMAL mode: 286 µA
  - Multiple SLEEP mode options: 24 µA to 41 µA
  - Multiple DEEPSLEEP mode options: 9.2 µA to 10.7 µA
  - SHUTDOWN Mode: 1 µA
- High voltage tolerance of 85 V on cell connect and select additional pins
- Support for temperature sensing using internal sensor and up to 9 external thermistors
- Integrated one-time-programmable (OTP) memory programmable by customers on production line
- Communication options include 400-kHz I^2C, SPI, and HDQ one-wire interface
- Dual programmable LDOs for external system usage

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2.1 Overview

The BQ769142 product is a highly integrated, accurate battery monitor and protector for 3-series to 14-series Li-ion, Li-polymer, and $LiFePO_4$ battery packs. A high accuracy voltage, current, and temperature measurement accuracy provides data for host-based algorithms and control. A feature-rich and highly configurable protection subsystem provides a wide set of protections which can be triggered and recovered completely autonomously by the device or under full control of a host processor. The integrated charge pump with high-side protection NFET drivers allows host communication with the device even when FETs are off by preserving the ground connection to the pack. Dual programmable LDOs are included for external system use, with each independently programmable to voltages of 1.8 V, 2.5 V, 3.0 V, 3.3 V, and 5.0 V, capable of providing up to 45 mA each.

The BQ769142 device includes one-time-programmable (OTP) memory for customers to setup device operation on their own production line. Multiple communications interfaces are supported, including 400-kHz I^2C, SPI, and HDQ one-wire standards. Multiple digital control and status data are available through several multifunction pins on the device, including an interrupt to the host processor, and independent controls for host override of each high-side protection NFET. Three dedicated pins are provided for temperature measurement using external thermistors, and multifunction pins can be programmed to use for additional thermistors, supporting a total of up to 9 thermistors, in addition to an internal die temperature measurement. Figure 2-1 shows the BQ769142 block diagram.

2.2 Functional Block Diagram

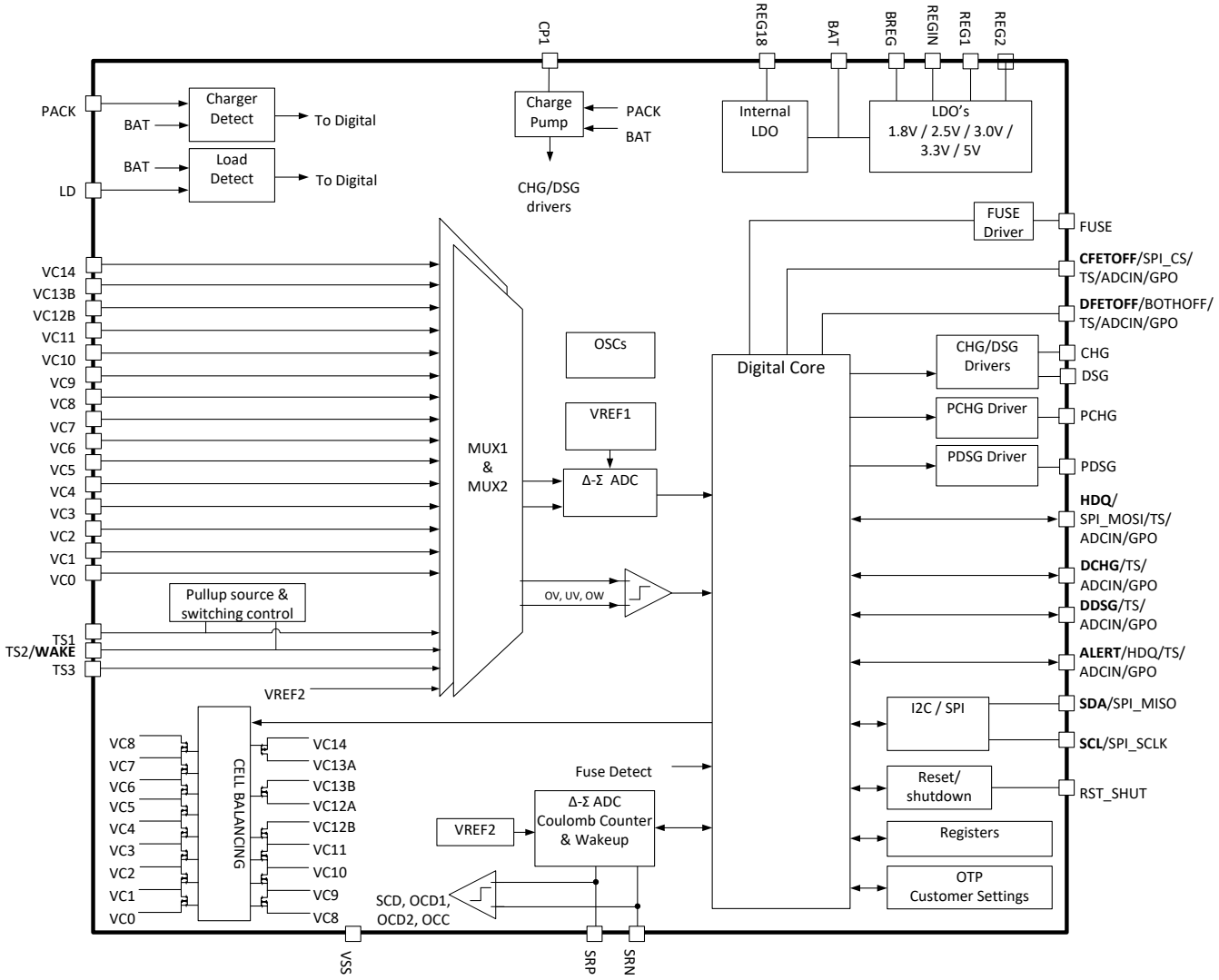


Figure 2-1. BQ769142 Block Diagram

3.1 Direct Commands and Subcommands

The BQ769142 device includes support for direct commands and subcommands. The direct commands are accessed using a 7-bit command address that is sent from a host through the device serial communications interface and either triggers an action, or provides a data value to be written to the device, or instructs the device to report data back to the host. Subcommands are additional commands that are accessed indirectly using the 7-bit command address space and provide the capability for block data transfers. When a subcommand is initiated, a 16-bit subcommand address is first written to the 7-bit command addresses 0x3E (lower byte) and 0x3F (upper byte). The device initially assumes a read-back of data may be needed, and auto-populates existing data into the 32-byte transfer buffer (which uses 7-bit command addresses 0x40–0x5F), and writes the checksum for this data into address 0x60. If the host instead intends to write data into the device, the host will overwrite the new data into the transfer buffer, a checksum for the data into address 0x60, and the data length into address 0x61. As soon as address 0x61 is written, the device checks the checksum written into 0x60 with the data written into 0x40-0x5F, and if this is correct, it proceeds to transfer the data from the transfer buffer into the device's memory. The checksum is the 8-bit sum of the subcommand bytes (0x3E and 0x3F) plus the number of bytes used in the transfer buffer, then the result is bitwise inverted. The verification cannot take place until the data length is written, so the device realizes how many bytes in the transfer buffer are included. The checksum and data length must be written together as a word in order to be valid. The data length includes the two bytes in 0x3E and 0x3F, the two bytes in 0x60 and 0x61, and the length of the transfer buffer. Therefore, if the entire 32-byte transfer buffer is used, the data length will be 0x24.

Some subcommands are only used to initiate an action and do not involve sending or receiving data. In these cases, the host can simply write the subcommand into 0x3E and 0x3F, it is not necessary to write the length and checksum or any further data.

The commands supported in the device are described in *Commands and Subcommands*. Single-byte commands are direct commands, while two-byte commands are subcommands. Data formats are described in *Data Formats*.

The most efficient approach to read the data from a subcommand (to minimize bus traffic) is shown below:

1. Write lower byte of subcommand to 0x3E.
2. Write upper byte of subcommand to 0x3F.
3. Read 0x3E and 0x3F. If this returns 0xFF, this indicates the subcommand has not completed operation yet. When the subcommand has completed, the readback will return what was originally written. Continue reading 0x3E and 0x3F until it returns what was written originally. Note: this response only applies to subcommands that return data to be read back.
4. Read the length of response from 0x61.
5. Read buffer starting at 0x40 for the expected length.
6. Read the checksum at 0x60 and verify it matches the data read.

An easier approach that is less efficient on bus traffic is:

1. Write the lower byte of the subcommand to 0x3E.
2. Write the upper byte of the subcommand to 0x3F.
3. Read 0x3E and 0x3F. If this returns 0xFF, this indicates that the subcommand has not completed the operation yet. When the subcommand has completed, the readback will return what was originally written.

Continue reading 0x3E and 0x3F until it returns what was written originally. Note: this response only applies to subcommands that return data to be read back.

4. Read 0x40 to 0x61 in a block. Ensure that the checksum at 0x60 is correct over the length designated by 0x61. This means sometimes more bytes are read than necessary, but it also makes it possible to use a standard function that can be called for all subcommands.

Note: 0x61 provides the length of the buffer data plus 4 (that is, length of the buffer data plus the length of 0x3E and 0x3F plus the length of 0x60 and 0x61).

The checksum is calculated over 0x3E, 0x3F, and the buffer data, it does not include the checksum or length in 0x60 and 0x61.

If the checksum and length are read together, this can trigger an auto-increment in some cases, in which case the buffer will be populated with another block's data. So, generally the checksum and length should not be read together unless the buffer has already been read, or if auto-incrementing is intended.

Command or subcommand bits denoted RSVD_0 should only be written as a "0", while bits denoted RSVD_1 should only be written as a "1".

3.2 Configuration Using OTP or Registers

The BQ769142 device includes registers, which are stored in the RAM, and are integrated in one-time programmable (OTP) memory. At initial powerup, the device loads OTP settings into registers, which are used by the device firmware during operation. The device can also perform a reset on demand if the *0x0012 RESET()* subcommand is sent. The recommended procedure is for the customer to write settings into OTP on the manufacturing line, in which case the device will use these settings whenever it is powered up. Alternatively, the host processor can initialize registers after powerup, without using the OTP memory, but the registers will need to be reinitialized after each power cycle of the device. Register values are preserved while the device is in NORMAL, SLEEP, or DEEPSLEEP modes. If the device enters SHUTDOWN mode, all register memory is cleared, and the device will return to the default parameters when powered again.

The OTP memory in the BQ769142 device is initially all-zeros. Each bit can be left as a "0" or written to a "1," but it cannot be written from a "1" back to a "0." The OTP memory includes two full images of the Data Memory configuration settings. At powerup, the device will XOR each setting in the first OTP image with the corresponding setting in the second OTP image and with the default value for the corresponding setting, with the resulting value stored into the RAM register for use during operation. This allows any setting to be changed from the default value using the first image, then changed back to the default once using the second image. The OTP memory also includes a 16-bit signature, which is calculated over most of the settings and stored in OTP. When the device is powered up, it will read the OTP settings and check that the signature matches that stored, to provide robustness against bit errors in reading or corruption of the memory. If a signature error is detected, the device will boot into the default configuration (as if the OTP is cleared).

The device supports up to eight different signature values, so up to eight partial changes in OTP can be made, with the signature updated accordingly. The OTP signature does not include the Manufacturing Data (available using the *0x0070 MANU_DATA()* subcommand) nor any PF status data that was written to OTP (which is read using the *0x0053 SAVED_PF_STATUS()* subcommand).

Note

The ***Settings:Configuration:Vcell Mode*** was written in OTP by TI with the value = 0xAFFF, which modified this parameter from its original hardware default value of 0x0000. This programming step used one of the eight available OTP signature settings, leaving seven remaining signature settings for customer use. The bits in this parameter programmed by TI to a "1" can be programmed back to a "0" by the customer using the second OTP XOR image, but after that they cannot be changed back to a "1" again.

The OTP memory settings are typically written after the device is assembled onto the PCB, but before cells are attached to the board. Programming the OTP memory settings requires the voltage applied on the BAT pin and the temperature to be within allowed limits, per specifications. All configuration settings are first loaded into registers using the serial communication interface (see Chapter 9). The *0x00A0 OTP_WR_CHECK()* subcommand can be sent to initiate a self-check whether OTP writing can be accomplished. The device must be in FULLACCESS and CONFIG_UPDATE modes when this subcommand is sent. Table 3-1 shows the *0x00A0 OTP_WR_CHECK()* information the device returns.

Table 3-1. *0x00A0 OTP_WR_CHECK()* Bit Definitions

Byte-0		
Bit	**Name**	**Description**
7	Programming OK	If this bit is set, conditions are met for programming, and none of the remaining bits in this byte will be set.
6	Reserved	
5	Locked	The device is not in FULLACCESS and CONFIG_UPDATE mode or the OTP Lock bit was set to prevent further modification.
4	No_SIG	Signature cannot be written (indicating the signature has already been written too many times).
3	No_DATA	Could not program data (indicating data has been programmed too many times; no XOR bits left)
2	HighTemp	The measured internal temperature is above the allowed OTP programming temperature range.
1	LowVoltage	The measured stack voltage is below the allowed OTP programming voltage.
0	HighVoltage	The measured stack voltage is above the allowed OTP programming voltage.
Bytes-1,2		
If byte 0, bit 3 is set, then byte 1 and byte 2 will contain the LSB and MSB of the address of the first data value that could not be programmed.		

If the self-check is successful, then the actual OTP write can be initiated by sending the *0x00A1 OTP_WRITE()* subcommand. This subcommand provides the same feedback as the *0x00A0 OTP_WR_CHECK()* subcommand above, with byte-0, bit-7 being set if programming completed successfully. The time for OTP programming depends on the number of bytes that must be programmed, with the device taking approximately 200 µs per byte programmed.

Special exceptions are provided that allow programming the Manufacturing Data and PF status data to OTP during normal operation if ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is set.

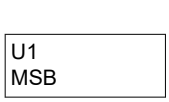
Note

The Manufacturing Data can be written with device settings while in CONFIG_UPDATE mode, as described above, but it can also be written using the *MANU_DATA()* subcommand in FULLACCESS mode. When Manufacturing Data is written using this subcommand, or the PF status data is written (which requires both ***Settings:Protection:Protection Configuration[PF_OTP]*** = 1 and ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** = 1), the minimum voltage required on BAT is still checked and required for programming, but the maximum voltage is not restricted to the specified level, since this may not be practical in normal system operation. This OTP programming is performed at a slow rate of approximately 125 ms per byte while in normal system operation.

3.3 Data Formats

3.3.1 Unsigned Integer

Unsigned integers are stored without changes as 1-byte, 2-byte, or 4-byte values in little endian byte order.



0	1
U2 LSB	U2 MSB

0	1	2	3
U4 L LSB	U4 L MSB	U4 H LSB	U4 H MSB

3.3.2 Integer

Integer values are stored in 2's-complement format in 1-byte, 2-byte, or 4-byte values in little endian byte order.

0
I1 MSB

0	1
I2 LSB	I2 MSB

0	1	2	3
I4 L LSB	I4 L MSB	I4 H LSB	I4 H MSB

3.3.3 Floating Point

Floating point values are stored using the IEEE754 Single Precision 4-byte format in little endian byte order.

0	1	2	3
Fract [0–7]	Fract [8–15]	Exp[0] + Fract[16–22]	Sign + Exp[1–7]

Where:

Exp: 8-bit exponent stored with an offset bias of 127. The values 00 and FF have unique meanings.

Fract: 23-bit fraction. If the exponent is > 0, then the mantissa is 1.fract. If the exponent is zero, then the mantissa is 0.fract.

The floating point value depends on the unique cases of the exponent:

- If the exponent is FF and the fraction is zero, this represents ± infinity.
- If the exponent is FF and the fraction is non-zero this represents "not a number" (NaN).
- If the exponent is 00 then the value is a subnormal number represented by $(-1)^{sign} \times 2^{-126} \times 0.fraction$.
- Otherwise, the value is a normalized number represented by $(-1)^{sign} \times 2^{(exponent - 127)} \times 1.fraction$.

3.3.4 Hex

Bit register definitions are stored in unsigned integer format.

4.1 Voltage Measurement

The BQ769142 device integrates a voltage ADC that is multiplexed between measurements of cell voltages, an internal temperature sensor, and up to nine external thermistors, and performs measurements of the voltage at the VC14 pin, the PACK pin, the LD pin, the internal Vref used by the coulomb counter, and the VSS rail (for diagnostic purposes). The BQ769142 device supports measurement of individual differential cell voltages in a series configuration, ranging from 3-series cells to 14-series cells. Each cell voltage measurement is a differential measurement of the voltage between two adjacent cell input pins, such as VC1–VC0, VC2–VC1, and so on. The cell voltage measurements are processed based on trim and calibration corrections, and then reported in 16-bit resolution using units of 1 mV. The raw 24-bit digital output of the ADC is also available for readout using 32-bit subcommands (the 24-bit data is contained in the lower 3 bytes of the 32-bit data, and is sign-extended to create the upper byte). The cell voltage measurements can support a recommended voltage range from –0.2 V to 5.5 V. If a cell voltage is applied that exceeds a level of 5 × VREF1 (approximately 6.06 V), the device may report a value of -6.06 V (and the cell voltage raw counts similarly would report a value of -8388608). For best performance it is recommended to stay at a maximum input of 5.5 V. The 16-bit cell and VC14 (Stack), PACK, and LD pin voltage measurements are available by using the commands listed below.

Table 4-1. Commands to Read 16-Bit Voltage Measurements

Command	Name	Unit
0x14 and 0x15	Cell 1 Voltage	mV
0x16 and 0x17	Cell 2 Voltage	mV
0x18 and 0x19	Cell 3 Voltage	mV
0x1A and 0x1B	Cell 4 Voltage	mV
0x1C and 0x1D	Cell 5 Voltage	mV
0x1E and 0x1F	Cell 6 Voltage	mV
0x20 and 0x21	Cell 7 Voltage	mV
0x22 and 0x23	Cell 8 Voltage	mV
0x24 and 0x25	Cell 9 Voltage	mV
0x26 and 0x27	Cell 10 Voltage	mV
0x28 and 0x29	Cell 11 Voltage	mV
0x2A and 0x2B	Cell 12 Voltage	mV
0x2E and 0x2F	Cell 13 Voltage	mV
0x32 and 0x33	Cell 14 Voltage	mV
0x34 and 0x35	Stack (VC14 pin) voltage	userV
0x36 and 0x37	PACK pin voltage	userV
0x38 and 0x39	LD pin voltage	userV

4.1.1 Voltage Measurement Schedule

The BQ769142 voltage measurements are taken in a measurement loop that consists of multiple measurement slots. All 14 cell voltages are measured on each loop, then one slot is used for one of the VC14 or PACK or LD pin voltages, one slot is used for internal temperature or Vref or VSS measurement, two slots are unused, then up to three slots are used to measure thermistors or multifunction pin voltages (ADCIN functionality). Over

the course of three loops, a full set of measurements is completed. One measurement loop consists of either 18 (if no thermistors or ADCIN are enabled), 19 (if one thermistor or ADCIN is enabled), 20 (if two thermistors or ADCIN are enabled), or 21 (if three or more thermistors or ADCIN are enabled) measurement slots.

The speed of a measurement loop can be controlled by settings. Each voltage measurement (slot) takes 3 ms (or 1.5 ms if ***Settings:Configuration:Power Config:FASTADC*** is set), so a typical measurement loop with 21 slots per loop takes 63 ms (or 31.5 ms if ***Settings:Configuration:Power Config:FASTADC*** is set). If measurement data is not required as quickly, the timing for the measurement loop can be programmed to slower speeds, which injects idle slots in each loop after the measurement slots. Using slower loop cycle time reduces the power dissipation of the device when in NORMAL mode. This is set using the ***Settings:Configuration:Power Config:LOOP_SLOW_0*** and ***LOOP_SLOW_1*** configuration bits, as shown below. For example, assuming a typical measurement loop with 21 slots (63 ms) per loop, and these settings configured for half speed (126 ms), the device injects 21 current-only slots after each measurement loop of 21 slots.

Table 4-2. Voltage Measurement Schedule

LOOP_SLOW_1	LOOP_SLOW_0	Measurement Loop Cycle Time
0	0	63 ms
0	1	126 ms
1	0	252 ms
1	1	504 ms

4.1.2 Usage of VC Pins for Cells Versus Interconnect

If the BQ769142 device is used in a system with fewer than 14 series cells, the additional cell inputs can be utilized to improve measurement performance. For example, a long connection may exist between two cells in a pack, such that there may be significant interconnect resistance between the cells, such as shown in Figure 4-1 between CELL-A and CELL-B. By connecting VC10 close to the positive terminal of CELL-B, and connecting VC11 close to the negative terminal of CELL-A, more accurate cell voltage measurements are obtained for CELL-A and CELL-B, since the I·R voltage across the interconnect resistance between the cells is not included in either cell voltage measurement. Since the device reports the voltage across the interconnect resistance and the synchronized current in *DASTATUS1–4()*, the resistance of the interconnect between CELL-A and CELL-B can also be calculated and monitored during operation. It is recommended to include the series resistance and bypass capacitor on cell inputs connected in this manner, as shown below.

Note

It is important that the differential input for each cell input not fall below –0.3 V (the Absolute Maximum datasheet limit), with the recommended minimum voltage of –0.2 V. Therefore, it is important that the I·R voltage drop across the interconnect resistance does not cause a violation of this requirement.

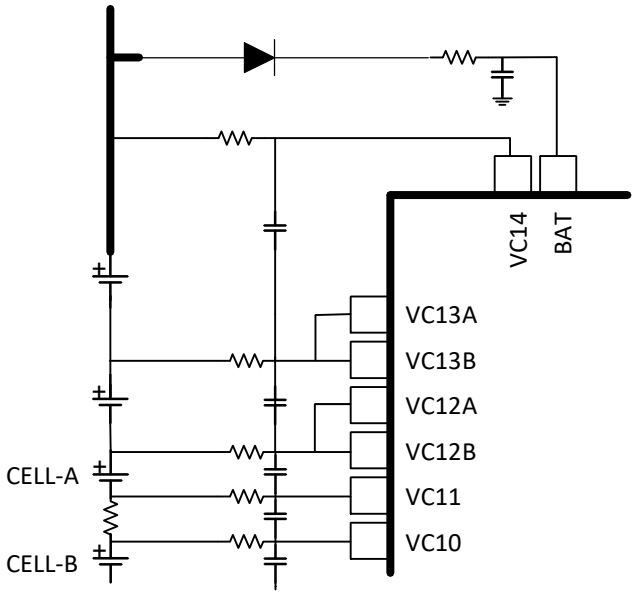


Figure 4-1. Using Cell Input Pins for Interconnect Measurement

If this connection across an interconnect is not needed (or it is preferred to avoid the extra resistor and capacitor), then the unused cell input pins should be shorted to adjacent cell input pins, as shown in Figure 4-2 for VC11.

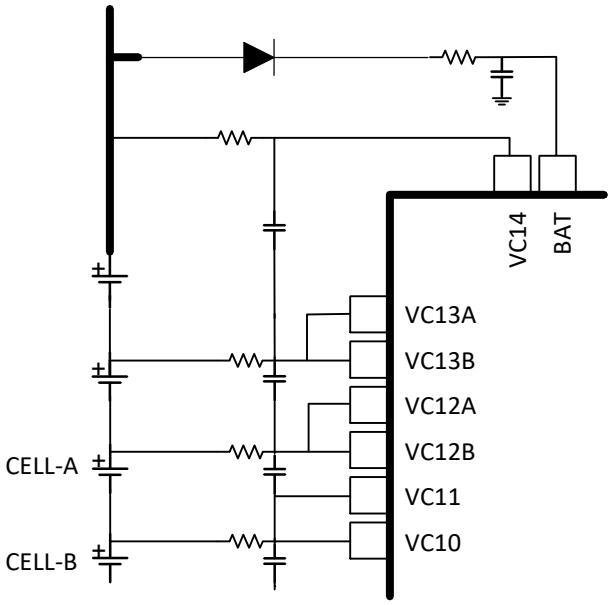


Figure 4-2. Terminating an Unused Cell Input Pin

The ***Settings:Configuration:Vcell Mode*** configuration register is used to specify which cell inputs are used for actual cells. The device uses this information to disable cell voltage protections associated with inputs which are used to measure interconnect or are not used at all. Voltage measurements for all inputs are reported in 16-bit format (in units of mV) as well as 32-bit format (in units of raw ADC counts), irrespective of whether they are used for cells or not.

4.1.3 Cell Interconnect Resistance

If measurement of an interconnect between cells is not practical or desired, the BQ769142 device also includes fixed settings for cell interconnect resistance in ***Settings:Interconnect Resistances:Cell 1 Interconnect –***

Cell 14 Interconnect in units of mΩ. The device will subtract the measured current times these interconnect resistance values from each differential cell voltage measurement before reporting the final cell voltage value.

4.2 General Purpose ADCIN Functionality

Several multifunction pins on the BQ769142 device can be used for general purpose ADC input (ADCIN) measurement, if not being used for other purposes. This includes the TS1, TS2, TS3, CFETOFF, DFETOFF, HDQ, DCHG, DDSG, and ALERT pins. When used for ADCIN functionality, the internal bandgap reference is used by the ADC, and the input range of the ADC is limited to the REG18 pin voltage. The digital fullscale range of the ADC is effectively 1.6667 × VREF1, which is approximately 2.02 V during normal operation. To configure the multifunction pins for this functionality, see Section 6.4.

When a pin is configured for ADCIN functionality, the voltage is reported in mV using the command that normally reports thermistor temperature on that pin. For example, if TS1 is configured for ADCIN functionality, the *0x70 TS1 Temperature()* command will return a 16-bit signed value corresponding to the pin voltage in mV.

The BQ769142 device also reports the raw ADC counts in *0x0076 DASTATUS6()* when a measurement is taken using the TS1 pin. This data can be used during manufacturing to better calibrate the ADCIN functionality.

4.3 Coulomb Counter and Digital Filters

The BQ769142 device monitors pack current using a low-side sense resistor, which connects to the SRP and SRN pins through an external RC filter, which should be connected such that a charging current will create a positive voltage on SRP relative to SRN. The device supports sense resistors of 1 mΩ or below. The differential voltage between SRP and SRN is digitized by an integrated coulomb counter ADC, which can digitize voltages over a ±200-mV range and uses multiple digital filters to provide optimized measurement of the instantaneous, averaged, and integrated current. The pins can also support higher positive voltages relative to VSS, such as which may occur during overcurrent or short circuit in discharge conditions, without damage to the device, although the current is not accurately digitized in this case. Multiple digitized current values are available, including two using separate hardware digital filters, CC1 and CC2, as well as a firmware filter CC3.

The units for the current reporting are in userA (userAmps), which can be programmed to be 0.1 mA, 1 mA, 10 mA, or 100 mA using the ***Settings:Configuration:DA Configuration:[USER_AMPS_1:0]*** configuration setting. Given the 16-bit values can range from –32768 to +32767, this allows representation of currents ranging from –3276 A to +3276 A.

Table 4-3. Current Measurement Units

USER_AMPS_1	USER_AMPS_0	Units for Reporting
0	0	0.1 mA
0	1	1 mA
1	0	10 mA
1	1	100 mA

The CC1 filter generates a 16-bit current measurement that is used for charge integration and other decision purposes, with one output generated every 250 ms when the device is operating in NORMAL mode. The CC1 data is available from the *0x0075 DAStatus5()* subcommand.

The CC2 filter generates a 24-bit current measurement that is used for current reporting, with one output every 3 ms when the device is operating in NORMAL mode (which can be reduced to one output every 1.5 ms when the ***Settings:Configuration:Power Config[FASTADC]*** bit is set, with reduced measurement resolution). It is reported in 16-bit format using the *0x3A CC2 Current()* command. The 32-bit CC2 data is available as raw coulomb counter ADC counts from the *0x0075 DASTATUS5()* subcommand (the 24-bit data is contained in the lower three bytes of the 32-bit data, and is sign-extended to create the upper byte).

The CC3 filter output is an average of a programmable number of CC2 current samples (up to 255), which are set using the ***Settings:Configuration:CC3 Samples*** configuration setting. The CC3 output is reported in 16-bit format using the *0x0075 DASTATUS5()* subcommand. The 32-bit CC3 data is also available in units of ADC

counts from the *0x0075 DASTATUS5()* subcommand (the averaged data is contained in the lower bytes of the 32-bit data, and is sign-extended into the upper byte).

The integrated passed charge is available as a 64-bit value from the *0x0076 DASTATUS6()* subcommand, which includes the upper 32-bits of accumulated charge in units of userAh, the lower 32-bits of accumulated charge as the fractional portion, and a 32-bit accumulated time over which the charge has been integrated in units of seconds. The accumulated charge integration and timer can be reset using the *0x0082 RESET_PASSQ()* subcommand. If the device undergoes a partial reset or is reset using the RST_SHUT pin, the *0x0082 RESET_PASSQ()* should be sent to ensure the charge accumulation is properly initialized.

4.4 Synchronized Voltage and Current Measurement

While the cell voltages are digitized sequentially using a single muxed ADC during normal operation, the current is digitized continuously by the dedicated coulomb counter ADC. The current is measured synchronously with each cell voltage measurement, and can be used for individual cell impedance analysis. The ongoing periodic current measurements can be read out through the digital communication interface, while the measurements taken that were synchronized with particular cell voltage measurements are stored paired with the associated cell voltage measurement for separate readout. The synchronous voltage and current data are available in units of raw ADC counts through the 0x0071-0x0074 subcommands. The Cell-1 voltage is measured and stored as *Cell 1 Voltage Cnts()*, the current is simultaneously measured and stored as *Cell 1 Current Cnts()*, and similarly for all other cells. Reading this data from the block subcommands ensures the synchronously aligned voltage and current data are read out together.

4.5 Subcommands *0x0071–0x0074 DASTATUS1-4()*, Cell Voltage and Synchronized Current Counts

The *0x0071 DASTATUS1()*, *0x0072 DASTATUS2()*, *0x0073 DASTATUS3()*, and *0x0074 DASTATUS4()* subcommands provide raw ADC counts in 32-bit format of the cell voltage measurements, as well as the synchronized current measurements taken simultaneously with each cell voltage measurement.

Note

Only the 24-bit raw data is generated by the data converters, but the data is provided in a 32-bit numerical format (the 24-bit data is contained in the lower three bytes of the 32-bit data, and is sign-extended to create the upper byte). The raw ADC data provided for cell-voltage measurements uses a digital fullscale range of ± (5 × VREF1), although cell voltage measurements more negative than –0.2 V cannot practically be measured. The raw coulomb counter ADC data provided for current measurements uses a digital fullscale range of ± (VREF2 / 5).

The 32-bit cell voltage counts data has an LSB value of approximately $5 \times V_{REF1} / 2^{23} \cong 5 \times 1.212\ V / 2^{23} \cong 0.722\ \mu V$.

Note

This data was not processed using the internal factory gain and offset trim corrections, which are used for calculation of the 16-bit data provided by the *Cell # Voltage()* commands.

The 32-bit current counts data has an LSB value of approximately $V_{REF2} / (5 \times 2^{23}) \cong 1.24\ V / (5 \times 2^{23}) \cong 29.56$ nV.

Note

This data was not processed for gain or offset, which are used for calculating the 16-bit current data provided by the *CC2 Current()* and *CC3 Current()* commands.

Table 4-4 provides further details.

Table 4-4. Cell Voltage and Synchronized Current Counts

Subcommand Address	Bytes within Block	Name	Unit
0x0071	0–3	Cell 1 Voltage Counts	ADC counts
	4–7	Cell 1 Current Counts	ADC counts
	8–11	Cell 2 Voltage Counts	ADC counts
	12–15	Cell 2 Current Counts	ADC counts
	16–19	Cell 3 Voltage Counts	ADC counts
	20–23	Cell 3 Current Counts	ADC counts
	24–27	Cell 4 Voltage Counts	ADC counts
	28–31	Cell 4 Current Counts	ADC counts
0x0072	0–3	Cell 5 Voltage Counts	ADC counts
	4–7	Cell 5 Current Counts	ADC counts
	8–11	Cell 6 Voltage Counts	ADC counts
	12–15	Cell 6 Current Counts	ADC counts
	16–19	Cell 7 Voltage Counts	ADC counts
	20–23	Cell 7 Current Counts	ADC counts
	24–27	Cell 8 Voltage Counts	ADC counts
	28–31	Cell 8 Current Counts	ADC counts
0x0073	0–3	Cell 9 Voltage Counts	ADC counts
	4–7	Cell 9 Current Counts	ADC counts
	8–11	Cell 10 Voltage Counts	ADC counts
	12–15	Cell10 Current Counts	ADC counts
	16–19	Cell 11 Voltage Counts	ADC counts
	20–23	Cell 11 Current Counts	ADC counts
	24–27	Cell 12 Voltage Counts	ADC counts
	28–31	Cell 12 Current Counts	ADC counts
0x0074	0–3	Reserved	—
	4–7	Reserved	—
	8–11	Cell 13 Voltage Counts	ADC counts
	12–15	Cell 13 Current Counts	ADC counts
	16–19	Reserved	—
	20–23	Reserved	—
	24–27	Cell 14 Voltage Counts	ADC counts
	28–31	Cell 14 Current Counts	ADC counts

4.6 Subcommands *0x0075–0x0077 DASTATUS5–7()*, Additional Measurements

The *0x0075 DASTATUS5()* subcommand provides voltage measurements of the REG18 LDO voltage, the VSS pin, as well as calculated values for the minimum, maximum, and sum of cell voltage measurements. It also provides the readings used for cell and FET temperature, minimum, maximum, and average cell temperature, and both CC1 and CC3 current values.

Since the VREF2 measurement is measured by the voltage ADC using VREF1, the REG18 voltage measurement provides information on the ratio of one reference versus the other and should stay approximately constant. This measurement can be used as a diagnostic check to determine if one reference changes value versus the other.

The VSS measurement is included as an additional diagnostic measurement to ensure that the ADC input mux is working properly. This measurement should normally result in a value near 0. If an internal fault were to occur that caused the ADC input mux to be stuck at a particular setting, such as a cell input, then the

VSS measurement would be significantly higher. If the mux were stuck at a setting such as an interconnect measurement or VSS, the cell voltage measurements would be reported as very low voltage.

The Battery Voltage Sum is the sum of all enabled cell voltage measurements, reported in units of cV (10 mV). This value can be compared with the *0x34 Stack Voltage()* and used as a diagnostic check.

Note

Because the measurements are taken by the same ADC at different times, transient changes in the cell voltages can cause differences in the sum versus the stack measurement, and will need to be considered.

The 32-bit raw CC2 counts and raw CC3 counts data have an LSB value of approximately V_{REF2} / (5 × 2^{23}) ≅ 1.24 V / (5 × 2^{23}) ≅ 29.56 nV.

Note

This data was not processed for gain or offset, which are used for calculation of the 16-bit current data provided by the *CC2 Current()* and *CC3 Current()* commands.

Table 4-5 provides further details.

Table 4-5. *0x0075 DASTATUS5()* Subcommand Detail

Subcommand Address	Bytes Within Block	Name	Unit
0x0075	0–1	V_{REG18}	16-bit ADC counts
	2–3	VSS	16-bit ADC counts
	4–5	Max Cell Voltage	mV
	6–7	Min Cell Voltage	mV
	8–9	Battery Voltage Sum	cV
	10–11	Avg Cell Temperature	0.1 K
	12–13	FET Temperature	0.1 K
	14–15	Max Cell Temperature	0.1 K
	16–17	Min Cell Temperature	0.1 K
	18–19	Avg Cell Temperature	0.1 K
	20–21	CC3 Current	userA
	22–23	CC1 Current	userA
	24–27	CC2 Counts	32-bit ADC counts
	28–31	CC3 Counts	32-bit ADC counts

The *0x0076 DASTATUS6()* subcommand provides the accumulated charge value and associated timer. It also includes the 32-bit raw ADC count for the CFETOFF, DFETOFF, ALERT, TS1, and TS2 pin measurements, which can be used for customer calibration of the general-purpose ADC input measurement capability of the device.

The 32-bit raw ADC counts data for the CFETOFF, DFETOFF, ALERT, TS1, TS2, TS3, HDQ, DCHG, and DDSG pins has a different LSB value, depending on whether the pin is configured for thermistor measurement mode or general purpose ADC (ADCIN) input mode. When configured for thermistor measurement, the raw ADC counts have an LSB of approximately 5 / 3 × 1.8 V / 2^{23} ≅ 0.358 µV. When configured for ADCIN measurement, the raw ADC counts have an LSB of approximately 5 / 3 × V_{REF1} / 2^{23} ≅ 5 / 3 × 1.212 V / 2^{23} ≅ 0.241 µV.

Note

This data has not been processed using gain and offset trim corrections, which are used for calculation of the 16-bit data provided in ADCIN mode by the temperature commands, such as *TS1 Temperature()*.

The details of this subcommand are shown below.

Table 4-6. *0x0076 DASTATUS6()* Subcommand Detail

Subcommand Address	Bytes Within Block	Name	Unit
0x0076	0–3	Accumulated charge (integer portion)	32-bit signed integer portion in userAh
	4–7	Accumulated charge (fractional portion), initialized to 0.5 userAh when reset	32-bit fractional portion in userAh
	8–11	Accumulated Time	32-bit unsigned integer in seconds
	12–15	CFETOFF Counts	32-bit ADC counts
	16–19	DFETOFF Counts	32-bit ADC counts
	20–23	ALERT Counts	32-bit ADC counts
	24–27	TS1 Counts	32-bit ADC counts
	28–31	TS2 Counts	32-bit ADC counts

The *0x0077 DASTATUS7()* subcommand provides the 32-bit raw ADC count for the TS3, HDQ, DCHG, and DDSG pin measurement, which can be used for customer calibration of the general-purpose ADC input measurement capability of the device. The details of this subcommand are shown below.

Table 4-7. *0x0077 DASTATUS7()* Subcommand Detail

Subcommand Address	Bytes within Block	Name	Unit
0x0077	0–3	TS3 Counts	32-bit ADC counts
	4–7	HDQ Counts	32-bit ADC counts
	8–11	DCHG Counts	32-bit ADC counts
	12–15	DDSG Counts	32-bit ADC counts
	16–31	Reserved	-

4.7 Internal Temperature Measurement

The BQ769142 device integrates the capability to measure its internal die temperature by digitizing an internal transistor base-emitter voltage. This voltage is measured periodically as part of the measurement loop and is processed to provide a temperature value using the *0x68 Int Temperature()* command.

This internal temperature measurement can be used for cell temperature protections and logic that uses minimum, maximum, or average cell temperature by setting the ***Settings:Configuration:DA Configuration[TINT_EN]*** configuration bit and keeping the ***Settings:Configuration:DA Configuration[TINT_FETT]*** bit cleared. The internal temperature measurement can instead be used for FET temperature by setting both ***Settings:Configuration:DA Configuration[TINT_EN]*** and ***Settings:Configuration:DA Configuration[TINT_FETT]***, although in this case it will not be used for cell temperature.

The calculation of temperature is performed as follows:

Internal Temperature (in units of 0.1 K) = (ADC value) × ***Calibration:Internal Temp Model:Int Gain*** / 65536 + ***Calibration:Internal Temp Model:Int base offset*** + ***Calibration:Temperature:Internal Temp Offset***

except if (ADC value) > ***Calibration:Internal Temp Model:Int Maximum AD***, then the reported internal temperature is calculated using the ***Calibration:Internal Temp Model:Int Maximum AD*** as the ADC value. If internal temperature is calculated > ***Calibration:Internal Temp Model:Int Maximum Temp***, the reported internal temperature is set to ***Calibration:Internal Temp Model:Int Maximum Temp***.

4.8 Thermistor Temperature Measurement

The BQ769142 device includes an on-chip temperature measurement and can also support up to nine external thermistors on multifunction pins (TS1, TS2, TS3, CFETOFF, DFETOFF, ALERT, HDQ, DCHG, and DDSG). The device includes an internal pullup resistor to bias a thermistor during measurement.

The internal pull-up resistor has two options which can set the pull-up resistor to either 18-kΩ or 180-kΩ (or none at all). The 18-kΩ option is intended for use with thermistors such as the Semitec 103-AT, which has 10-kΩ resistance at room temperature. The 180-kΩ is intended for use with higher resistance thermistors such as the Semitec 204AP-2, which has 200-kΩ resistance at room temperature. The resistor values are measured during factory production and stored within the device for use during temperature calculation. The individual pin configuration registers determine which pin is used for a thermistor measurement, what value of pull-up resistor is used, as well as whether the thermistor measurement is used for a cell or FET temperature reading. For more detail on these pin configuration registers, see Section 6.4.

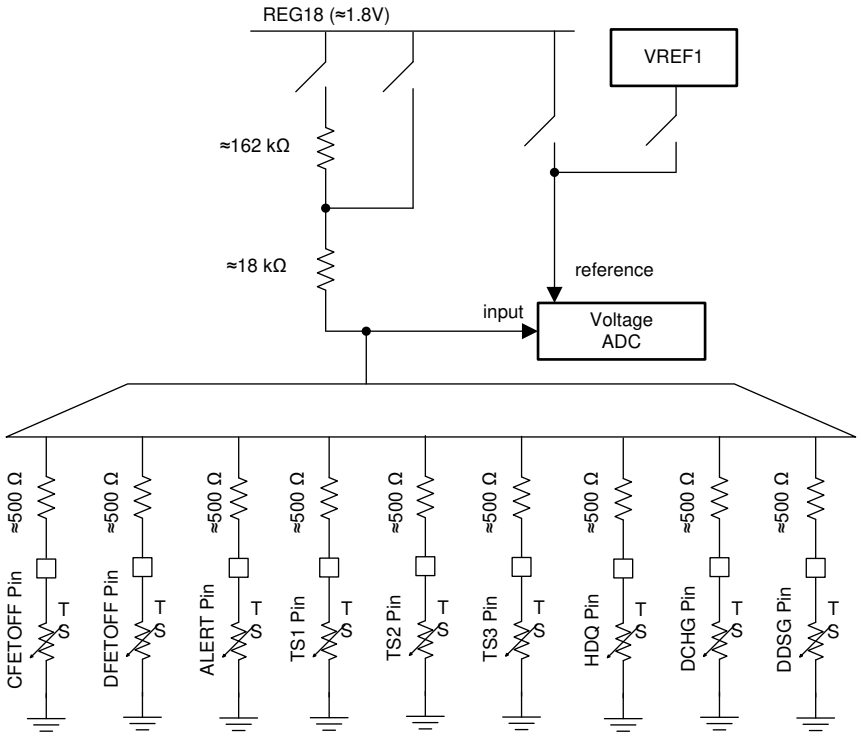


Figure 4-3. External Thermistor Biasing

Table 4-8. Temperature Measurement Commands

Command Address	Name	Comment
0x68	Int Temperature	Internal die temperature
0x6A	CFETOFF Temperature	CFETOFF pin thermistor
0x6C	DFETOFF Temperature	DFETOFF pin thermistor
0x6E	ALERT Temperature	ALERT pin thermistor
0x70	TS1 Temperature	TS1 pin thermistor
0x72	TS2 Temperature	TS2 pin thermistor
0x74	TS3 Temperature	TS3 pin thermistor
0x76	HDQ Temperature	HDQ pin thermistor
0x78	DCHG Temperature	DCHG pin thermistor
0x7A	DDSG Temperature	DDSG pin thermistor

The calculation of temperature from the measured ADC value is performed using a temperature model, which includes gain, offset, and a polynomial computation. The device includes configuration registers for one temperature model based on the 18-kΩ pull-up resistor in ***Calibration:18K Temperature Model***, and a second temperature model based on the 180-kΩ pull-up resistor in ***Calibration:180K Temperature Model***. This allows one type of thermistor to be used for measuring cell temperature, versus another type may be used for

measuring FET temperature. The default parameters for the models match the Semitec 103-AT and 204AP-2 thermistors.

In order to provide a high precision temperature result, the device uses the same 1.8 V LDO voltage for the ADC reference as is used for biasing the thermistor pullup resistor, thereby implementing a ratiometric measurement that removes the error contribution from the LDO voltage level. The device processes the digitized thermistor voltage to calculate the temperature based on multiorder polynomials, which can be programmed by the user based on the specific thermistor selected.

4.9 Factory Trim of Voltage ADC

The BQ769142 device includes factory trim for the cell voltage ADC measurements in order to optimize the voltage measurement performance even if no further calibration is performed by the customer. Calibration can be performed by the customer on the production line to further optimize the performance in the system. The trim information is used to correct the raw ADC readings before they are reported as 16-bit voltage values. The 32-bit ADC voltage data, which is generated in units of ADC counts, is modified before reporting by subtracting a stored offset trim value. The resulting reported data does not include any further correction (such as for gain), therefore the customer will need to process them before use.

The device also includes a factory gain trim for the voltage measurements performed using the general purpose ADC input capability on the multifunction pins as well as the TS1, TS2, and TS3 pins. The raw ADC reading is provided for each pin in 32-bit ADC counts using the *0x0076 - 0x0077 DASTATUS6-7()* subcommands.

4.10 Voltage Calibration (ADC Measurements)

The BQ769142 device includes optional capability for the customer to calibrate each cell voltage gain and the gain for the stack voltage, the PACK pin voltage, and the LD pin voltage individually, and multifunction pin general ADC measurements. An offset calibration value ***Calibration:Vcell Offset:Vcell Offset*** is included for use with the cell voltage measurements, and ***Calibration:Vdiv Offset:Vdiv Offset*** is used with the TOS (stack), PACK, and LD voltage measurements. The cell voltage gains determined during calibration are written in ***Calibration:Voltage:Cell 1 Gain – Cell 14 Gain***, where ***Cell 1 Gain*** is used for the measurement of VC1-VC0, ***Cell 2 Gain*** is used for the measurement of VC2-VC1, and so forth. Similarly, the calibration voltage gain for the TOS voltage should be written in ***Calibration:Voltage:TOS Gain***, the PACK pin voltage gain in ***Calibration:Voltage:Pack Gain***, the LD pin voltage gain in ***Calibration:Voltage:LD Gain***, and multifunction pin general purpose ADCIN measurement gain in ***Calibration:Voltage:ADC Gain***.

If values for the calibration gain configuration are not written, the BQ769142 device will use factory trim or default values for the respective gain values. When a calibration gain configuration value is written, the device will use that in place of any factory trim or default gain. The raw ADC measurement data (in units of counts) is corrected by first subtracting a stored offset trim value, then the gain is applied, then the ***Calibration:Vcell Offset:Vcell Offset*** (for cell voltage measurements) or the ***Calibration:Vdiv Offset:Vdiv Offset*** (for TOS, PACK, or LD voltage measurements) is subtracted, before the final voltage value is reported.

The factory trim values for the Cell Gain parameters can be read from the Cell Gain data memory registers while in FULLACCESS mode but not in CONFIG_UPDATE mode, if the data memory values have not been overwritten. While in CONFIG_UPDATE mode, the Cell Gain values will read back either with all zeros, if they have not been overwritten, or whatever values have been written to these registers. Upon exiting CONFIG_UPDATE mode, readback of the Cell Gain parameters will provide the values presently used in operation.

The cell voltage calibration can be implemented by applying two precise DC voltages to the cell input (such as 2.5 V and 4.5 V) and averaging multiple raw ADC measurements in 32-bit counts obtained from the *0x0071–0x0074 DASTATUS1–4()* subcommands for each voltage. The gain can then be calculated as:

$$\text{Cell Gain} = \frac{2^{24} \times \left(\text{Voltage\_1}_{\text{in mV}} - \text{Voltage\_2}_{\text{in mV}}\right)}{\left(\text{32-bit ADC counts}\right)_{\text{Voltage\_1}} - \left(\text{32-bit ADC counts}\right)_{\text{Voltage\_2}}}$$

The offset for the cell voltage measurement can now be calculated as shown below:

$$\text{Cell Offset} = \frac{(\text{Cell Gain}) \times (\text{32-bit ADC counts})_{\text{Voltage\_2}}}{2^{24}} - \text{Voltage\_2}_{\text{in mV}}$$

The calibration for the TOS, PACK pin, and LD pin gain measurements can be implemented by similarly applying two precise DC voltages to the input and averaging multiple raw ADC measurements, which are provided in 16-bit counts from the *0xF081 READ_CAL1()* subcommand. Note: one of the voltages can be skipped to reduce calibration time. The gain can then be calculated as:

$$\text{TOS / PACK / LD Gain} = \frac{2^{16} \times \left(\text{Voltage\_1}_{\text{in cV}} - \text{Voltage\_2}_{\text{in cV}}\right)}{(\text{16-bit ADC counts})_{\text{Voltage\_1}} - (\text{16-bit ADC counts})_{\text{Voltage\_2}}}$$

The ADCIN measurement can be calibrated in similar fashion to the cell voltage gain calibration. One or two precise DC voltages can be applied to the selected pin, and the 32-bit counts obtained from the *0x0076 DASTATUS6()* or *0x0077 DASTATUS7()* subcommands for each voltage. The gain can then be calculated as:

$$\text{ADC Gain} = \frac{2^{24} \times \left(\text{Voltage\_1}_{\text{in mV}} - \text{Voltage\_2}_{\text{in mV}}\right)}{(\text{32-bit ADC counts})_{\text{Voltage\_1}} - (\text{32-bit ADC counts})_{\text{Voltage\_2}}}$$

The effective fullscale digital range of the cell measurement is 5 × VREF1, and the effective fullscale digital range of the ADCIN measurement is 1.667 × VREF1, although the voltages applied for these measurement should be limited based on the device electrical specifications. Using a value for VREF1 of 1.212 V, the nominal gain for the cell measurements is 12120, while the nominal gain for the ADCIN measurements is 4040. The reported voltages are calculated as:

Cell # Voltage() = ***Calibration:Voltage:Cell # Gain*** × (16-bit ADC counts) / 65536– ***Calibration:Vcell Offset:Vcell Offset***

Stack Voltage() = ***Calibration:Voltage:TOS Gain*** × (16-bit ADC counts) / 65536– ***Calibration:Vdiv Offset:Vdiv Offset***

PACK Pin Voltage() = ***Calibration:Voltage:Pack Gain*** × (16-bit ADC counts) / 65536– ***Calibration:Vdiv Offset:Vdiv Offset***

LD Pin Voltage() = ***Calibration:Voltage:LD Gain*** × (16-bit ADC counts) / 65536– ***Calibration:Vdiv Offset:Vdiv Offset***

ADCIN Voltage = ***Calibration:Voltage:ADC Gain*** × (16-bit ADC counts) / 65536

Note: *Cell # Voltage()* and ***Calibration:Vcell Offset:Vcell Offset*** both have units of mV. The divider voltages (*Stack Voltage()*, *PACK Pin Voltage()*, and *LD Pin Voltage()*) and ***Calibration:Vdiv Offset:Vdiv Offset*** all have units of userV.

4.11 Voltage Calibration (COV and CUV Protections)

The BQ769142 device includes optional capability for the customer to calibrate the COV (cell overvoltage) and CUV (cell undervoltage) protection thresholds on the production line, in order to improve threshold accuracy in system or to realize a threshold between the preset thresholds available from the device.

This calibration is performed while the device is in CONFIG_UPDATE mode. To calibrate the COV threshold, an external voltage is first applied between VC14 and VC13A that is equal to the desired COV threshold. Next, the *CAL_COV()* subcommand is sent by the host, which causes the BQ769142 device to perform a search for the appropriate calibration coefficients to realize a COV threshold at or close to the applied voltage level. When this search is completed, the resulting calibration coefficient is returned by the subcommand and automatically written into the ***Protections:COV:COV Threshold Override*** configuration parameter. If this parameter is nonzero, the device will not use its factory trim settings but will instead use this value.

The CUV threshold is calibrated similarly, an external voltage is applied between VC14 and VC13A equal to the desired CUV threshold. Next, while in CONFIG_UPDATE mode, the *CAL_CUV()* subcommand is sent by the host, which causes the BQ769142 device to perform a search for the appropriate calibration coefficients to realize a CUV threshold at or close to the applied voltage level. When this search is completed, the resulting calibration coefficient is returned by the subcommand and automatically written into the ***Protections:CUV:CUV Threshold Override*** configuration parameter.

4.12 Current Calibration

The BQ769142 device coulomb counter ADC measures the differential voltage between the SRP and SRN pins to calculate the system current. The device includes the optional capability for the customer to calibrate the coulomb counter offset and current gain on the production line.

The ***Calibration:Current Offset:Board Offset*** configuration register contains an offset value in units of 32-bit coulomb counter ADC counts / ***Calibration:Current Offset:Coulomb Counter Offset Samples***. The value of ***Calibration:Current Offset:Board Offset*** / ***Calibration:Current Offset:Coulomb Counter Offset Samples*** is subtracted from the raw coulomb counter ADC counts, then the result is multiplied by ***Calibration:Current:CC Gain*** and scaled to provide the final result in units of userA.

The BQ769142 device uses the ***Calibration:Current:CC Gain*** and ***Calibration:Current:Capacity Gain*** configuration values to convert from the ADC value to current. The ***CC Gain*** reflects the value of the sense resistor used in the system, while the ***Capacity Gain*** is simply the ***CC Gain*** multiplied by 298261.6178.

Both the ***CC Gain*** and ***Capacity Gain*** are encoded using a 32-bit IEEE-754 floating point format. The value of ***CC Gain*** is given by:

CC Gain = 10^6× VREF2 / (5 × 32768 × Rsense in mΩ)

The nominal value of ***CC Gain*** using the typical value of VREF2 = 1.24 V is given by:

CC Gain = 7.5684 / (Rsense in mΩ)

To optimize the current measurement reported by the device, the value of ***CC Gain*** can be modified on the customer production line to match the actual value of VREF2 in a particular device.

4.13 Temperature Calibration

The BQ769142 device enables the customer to calibrate the internal as well as external temperature measurements on the production line, by storing an offset value which is added to the calculated measurement before reporting. A separate offset for each temperature measurement can be stored in the configuration registers shown below.

Table 4-9. Temperature Calibration Settings

Section	Subsection	Register Description	Comment	Units
Calibration	Temperature	Internal Temp Offset		0.1 K
Calibration	Temperature	CFETOFF Temp Offset	CFETOFF pin thermistor	0.1 K
Calibration	Temperature	DFETOFF Temp Offset	DFETOFF pin thermistor	0.1 K
Calibration	Temperature	ALERT Temp Offset	ALERT pin thermistor	0.1 K
Calibration	Temperature	TS1 Temp Offset	TS1 pin thermistor	0.1 K
Calibration	Temperature	TS2 Temp Offset	TS2 pin thermistor	0.1 K
Calibration	Temperature	TS3 Temp Offset	TS3 pin thermistor	0.1 K
Calibration	Temperature	HDQ Temp Offset	HDQ pin thermistor	0.1 K
Calibration	Temperature	DCHG Temp Offset	DCHG pin thermistor	0.1 K
Calibration	Temperature	DDSG Temp Offset	DDSG pin thermistor	0.1 K

5.1 Protections Overview

An extensive protection subsystem is integrated within BQ769142, which can monitor a variety of parameters, initiate protective actions, and autonomously recover based on conditions. The device also includes a wide range of flexibility, such that the device can be configured to monitor and initiate protective action, but with recovery controlled by the host processor, or such that the device only monitors and alerts the host processor whenever conditions warrant protective action, but with action and recovery fully controlled by the host processor.

The primary protection subsystem includes a suite of individual protections that can be individually enabled and configured, including cell undervoltage and overvoltage, overcurrent in charge, three separate overcurrent in discharge protections, short circuit current in discharge, cell overtemperature and undertemperature in charge and discharge, FET overtemperature, a host processor communication watchdog timeout, and PRECHARGE mode timeout. The cell undervoltage and overvoltage, overcurrent in charge, overcurrent in discharge 1 and 2, and short circuit in discharge protections are based on comparator thresholds, while the remaining protections (such as those involving temperature, host watchdog, and precharging) are based on firmware on the internal controller.

The device integrates NFET drivers for high-side CHG and DSG protection FETs, which can be configured in a series or parallel configuration. An integrated charge pump generates a voltage that is driven onto the NFET gates based on host command or the on-chip protection subsystem settings. Support is also included for high-side PFETs used to implement a precharge and predischarge functionality.

The secondary protection suite within the BQ769142 device can react to more serious faults and take action to permanently disable the pack, by initiating a Permanent Fail (PF). The secondary safety provides protection against safety cell undervoltage and overvoltage, safety overcurrent in charge and discharge, safety overtemperature for cells and FETs, excessive cell voltage imbalance, internal memory faults, and internal diagnostic failures.

When a Permanent Fail has occurred, the BQ769142 device can be configured to either simply provide a flag, or to indefinitely disable the protection FETs, or to assert the FUSE pin to permanently disable the pack. The FUSE pin can be used to blow an in-line fuse and also can monitor if a separate secondary protector IC has attempted to blow the fuse.

5.2 Primary Protections

5.2.1 Primary Protections Overview

The BQ769142 device integrates a broad suite of protections for battery management and provides the capability to enable individual protections, as well as to select which protections will result in autonomous control of the FETs. The ***Settings:Manufacturing:Mfg Status Init[FET_EN]*** configuration bit determines whether the device is in autonomous control mode (when set) or in FET test mode (when cleared). The FET test mode is primarily for use on a customer production line, to test individual FETs. The autonomous control mode is recommended for field operation, which still allows the host to disable FETs through serial communications or using the CFETOFF and DFETOFF pins, and block their reenabling by the device until the host allows.

The individual protections can be enabled by setting the related ***Settings:Protection:Enabled Protections A – C*** configuration registers. The protections controlled by ***Settings:Protection:Enabled Protections A*** are comparator-based, while those in ***Settings:Protection:Enabled Protections B and C*** are firmware-based.

Each protection that has been enabled can also be controlled regarding whether it will disable a particular FET or not by setting related configuration bits. The bits in ***Settings:Protection:CHG FET Protections A – C*** determine which protections will trigger the CHG FET being disabled, while those in ***Settings:Protection:DSG FET Protections A – C*** determine which will trigger the DSG FET being disabled.

Note

Protections configured to disable the CHG FET also disable the precharge FET when it is enabled. Similarly, protections configured to disable the DSG FET also disable the predischarge FET when it is enabled.

Most protections involve the device checking for a violation of a particular condition, such as a voltage or current threshold. As soon as a violating condition is detected for an enabled protection, a safety alert is set. Flags showing which safety alerts may be present are available through the *0x02 Safety Alert A*, *0x04 Safety Alert B*, and *0x06 Safety Alert C* commands, and their presence can generate an interrupt to a host processor on the ALERT pin.

Most protections also include a delay, such that if the violating condition persists for some time interval, a safety fault is triggered. Flags showing which safety faults may be present are available through the *0x03 Safety Status A*, *0x05 Safety Status B*, and *0x07 Safety Status C* commands, and their presence can generate an interrupt to a host processor on the ALERT pin.

The format of the safety alert and safety status commands is shown below.

Table 5-1. Format for *0x02 Safety Alert A()* Command

Bit	Name	Description
7	SCD	Short Circuit in Discharge safety alert is present.
6	OCD2	Overcurrent in Discharge 2 safety alert is present.
5	OCD1	Overcurrent in Discharge 1 safety alert is present.
4	OCC	Overcurrent in Charge safety alert is present.
3	COV	Cell Overvoltage safety alert is present.
2	CUV	Cell Undervoltage safety alert is present.
1	RSVD	Reserved
0	RSVD	Reserved

Table 5-2. Format for *0x03 Safety Status A()* Command

Bit	Name	Description
7	SCD	Short Circuit in Discharge safety fault is present.
6	OCD2	Overcurrent in Discharge 2 safety fault is present.
5	OCD1	Overcurrent in Discharge 1 safety fault is present.
4	OCC	Overcurrent in Charge safety fault is present.
3	COV	Cell Overvoltage safety fault is present.
2	CUV	Cell Undervoltage safety fault is present.
1	RSVD	Reserved
0	RSVD	Reserved

Table 5-3. Format for *0x04 Safety Alert B()* Command

Bit	Name	Description
7	OTF	FET Overtemperature safety alert is present.
6	OTINT	Internal Die Overtemperature safety alert is present.
5	OTD	Overtemperature in Discharge safety alert is present.
4	OTC	Overtemperature in Charge safety alert is present.
3	RSVD	Reserved
2	UTINT	Internal Die Undertemperature safety alert is present.

Table 5-3. Format for *0x04 Safety Alert B()* Command (continued)

Bit	Name	Description
1	UTD	Undertemperature in Discharge safety alert is present.
0	UTC	Undertemperature in Charge safety alert is present.

Table 5-4. Format for *0x05 Safety Status B()* Command

Bit	Name	Description
7	OTF	FET Overtemperature safety fault is present.
6	OTINT	Internal Die Overtemperature safety fault is present.
5	OTD	Overtemperature in Discharge safety fault is present.
4	OTC	Overtemperature in Charge safety fault is present.
3	RSVD	Reserved
2	UTINT	Internal Die Undertemperature safety fault is present.
1	UTD	Undertemperature in Discharge safety fault is present.
0	UTC	Undertemperature in Charge safety fault is present.

Table 5-5. Format for *0x06 Safety Alert C()* Command

Bit	Name	Description
7	OCD3	Overcurrent in Discharge 3 safety alert is present.
6	SCDL	Latched Short Circuit in Discharge safety alert is present.
5	OCDL	Latched Overcurrent in Discharge safety alert is present.
4	COVL	Latched Cell Overvoltage safety alert is present.
3	PTOS	Precharge timer is suspended due to current below ***Protections:PTO:Charge Threshold*** .
2	RSVD	Reserved
1	RSVD	Reserved
0	RSVD	Reserved

Table 5-6. Format for *0x07 Safety Status C()* Command

Bit	Name	Description
7	OCD3	Overcurrent in Discharge 3 safety fault is present.
6	SCDL	Latched Short Circuit in Discharge safety fault is present.
5	OCDL	Latched Overcurrent in Discharge safety fault is present.
4	COVL	Latched Cell Overvoltage safety fault is present.
3	RSVD	Reserved
2	PTO	Precharge Timeout safety fault is present.
1	HWDF	Host watchdog safety fault is present.
0	RSVD	Reserved

5.2.2 High-Side NFET Drivers

The BQ769142 device includes an integrated charge pump and high-side NFET drivers for driving CHG and DSG protection FETs. The charge pump uses an external capacitor connected between the BAT and CP1 pins that is charged to an overdrive voltage when the charge pump is enabled (controlled using the ***Settings:FET:Chg Pump Control[CPEN]*** configuration bit). Due to the time required for the charge pump to bring the overdrive voltage on the external CP1 pin to full voltage, it is recommended to leave the charge pump powered whenever it may be needed quickly to drive the CHG or DSG FETs.

The DSG FET driver includes a special option (denoted source follower mode) to drive the DSG FET with the BAT pin voltage during SLEEP mode. This capability is included to provide low power in SLEEP mode, when there is no significant charge or discharge current flowing. It is recommended to keep the charge pump enabled even when the source follower mode is enabled, so whenever a discharge current is detected, the device can quickly transition to driving the DSG FET using the charge pump voltage. The source follower mode is enabled

by setting the ***Settings:FET:Chg Pump Control[SFMODE_SLEEP]*** configuration bit. The source follower mode is not intended to be used when significant charging or discharging current is flowing, since the FET will exhibit a large drain-source voltage and may undergo excessive heating.

The overdrive level of the charge pump voltage can be set to 5.5 V or 11 V, using the ***Settings:FET:Chg Pump Control[LVEN]*** configuration bit. In general, the 5.5 V setting results in lower power dissipation when a FET is being driven, while the higher 11 V overdrive reduces the on-resistance of the FET. If a FET exhibits significant gate leakage current when driven at the higher overdrive level, this can result in a higher device current for the charge pump to support this. In this case, using the lower overdrive level can reduce the leakage current and thus the device current.

The BQ769142 device supports a system with FETs in a series or parallel configuration, where the parallel configuration includes a separate path for the charger connection versus the discharge (load) connection. The control logic for the device operates slightly differently in these two cases, which is set based on the ***Settings:FET:FET Options[SFET]*** configuration bit. See Section 5.2.3.1 for more information on this operation.

The FET drivers in the BQ769142 device can be controlled in several different manner, depending on customer requirements:

Fully autonomous

The BQ769142 device can detect protection faults and autonomously disable the FETs, monitor for a recovery condition, and autonomously reenable the FETs, without requiring any host processor involvement.

This mode is enabled by setting the ***Settings:Manufacturing:Mfg Status Init[FET_EN]*** configuration bit. The FETs may be disabled when a fault occurs based on settings in ***Settings:Protection:CHG FET Protections A/B/C*** and ***Settings:Protection:DSG FET Protections A/B/C.***

Partially autonomous

The BQ769142 device can detect protection faults and autonomously disable the FETs. When the host receives an interrupt and recognizes the fault, the host can write the *0x0093 DSG_PDSG_OFF()* or *0x0094 CHG_PCHG_OFF()* or *0x0095 ALL_FETS_OFF()* commands to keep the FETs off until the host decides to release them. The *0x0097 FET_CONTROL()* subcommand can also be used to enable or disable each FET individually.

Alternatively, the host can assert the CFETOFF or DFETOFF pins to keep the FETs off. When the host decides to allow the FETs to turn on again, it writes the *0x0096 ALL_FETS_ON()* command, and the BQ769142 device will reenable the FETs if nothing is blocking them being reenabled (such as fault conditions still present, or the CFETOFF or DFETOFF pins are asserted).

Manual control

The BQ769142 device can detect protection faults and provide an interrupt to a host processor over the ALERT pin. The host processor can read the status information of the fault over the communication bus (if desired) and can quickly force the CHG or DSG FETs off by driving the CFETOFF or DFETOFF pins from the host processor, or using the *0x0093 DSG_PDSG_OFF()* or *0x0094 CHG_PCHG_OFF()*, *0x0095 ALL_FETS_OFF()*, or *0x0097 FET_CONTROL()* subcommands.

When the host decides to allow the FETs to turn on again, it writes the *0x0096 ALL_FETS_ON()* command or deasserts the CFETOFF and DFETOFF pins, and the BQ769142 device will reenable the FETs if nothing is blocking them being reenabled.

The status of the FET drivers is provided by the *[DSG_FET]* and *[CHG_FET]* bits in the *0x7F FET Status()* command. Depending on the device mode and fault status, there may be cases when only one FET is enabled, and the other FET is disabled. For example:

During SLEEP mode, the CHG FET may be disabled (if ***Settings:FET:FET Options[SLEEPCHG]*** is cleared), while the DSG FET is enabled.

If a COV fault has occurred, the CHG FET may be disabled, while the DSG FET may still be enabled, to allow discharge.

If a CUV fault has occurred, the DSG FET may be disabled, while the CHG FET may still be enabled, to allow charging.

If the device is in series FET configuration and a single FET is on, it is possible for current to flow through the off-FET body diode. This current can damage the FET if high enough for a long enough time. In this case, when the BQ769142 device is autonomously controlling the FETs, if a current is detected above a level given by ***Settings:Protection:Body Diode Threshold***, the device will automatically turn on the off-FET, to prevent further damage. This configuration register should be a positive value, it is used as a charging current level when deciding to turn on the DSG FET, and it is used as a discharging current level when deciding to turn on the CHG FET.

If the high-side NFET drivers will not be used in the application, the charge pump and FET drivers can be disabled by clearing the ***Settings:FET:Chg Pump Control[CPEN]*** and ***Settings:FET:FET Options[FET_CTRL_EN]*** configuration bits.

5.2.3 Protection FETs Configuration and Control

5.2.3.1 FET Configuration

The BQ769142 device supports both a series configuration and a parallel configuration for the protection FETs in the system, as well as a system which does not use one or both FETs. If the device FET drivers are not used at all, the charge pump should be disabled by clearing ***Settings:FET:Chg Pump Control[CPEN]*** and clearing ***Settings:FET:FET Options[FET_CTRL_EN].*** The ***Settings:FET:FET Options[SFET]*** configuration bit should be set when FETs are used in a series configuration, and should be cleared if FETs are used in a parallel configuration. If the system will only use a single FET (such as a CHG FET with no DSG FET), the device can be configured for parallel configuration with the DFETF Permanent Fail disabled.

When a series FET configuration is used, the BQ769142 device provides body diode protection for the case when one FET is off and one FET is on. This situation might occur in SLEEP mode (when the DSG FET is on and the CHG FET may be off) or in a cell undervoltage fault condition, when the DSG FET may be off, but the CHG FET may still be on.

If the CHG FET is off, the DSG or PDSG FET is on, and a discharge current greater in magnitude than ***Settings:Protection:Body Diode Threshold*** (that is, a significant discharging current) is detected, the device will turn on the CHG FET, to avoid current flowing through the CHG FET body diode and damaging the FET. When the current rises above the threshold (that is, less discharge current flowing), the CHG FET will be turned off again if the reasons for its turn-off are still present.

If the DSG FET is off, the CHG or PCHG FET is on, and a current in excess of +***Settings:Protection:Body Diode Threshold*** (that is, a significant charging current) is detected, the device will turn on the DSG FET, to avoid current flowing through the DSG FET body diode and damaging the FET. When the current falls below the threshold (that is, less charging current flowing), the DSG FET will be turned off again if the reasons for its turn-off are still present.

When a parallel configuration is used (***Settings:FET:FET Options[SFET]*** = 0), the body diode protection is disabled.

5.2.3.2 FET Control

The protection FETs can be controlled in several different ways, depending on system requirements. If FETs will not be used in the system or driven from the device, the ***Settings:FET:FET Options[FET_CTRL_EN]*** bit can be cleared, and the charge pump disabled by clearing the ***Settings:FET:Chg Pump Control[CPEN]*** bit.

The device includes a FET Test mode for use during manufacturing, in which the device will not enable the FETs unless FET Test subcommands are sent. The device may still enable FETs based on body diode protection in this mode. The device is put into FET Test mode by clearing ***Settings:Manufacturing:Mfg Status Init[FET_EN]***. The *0x0022 FET_ENABLE()* subcommand can be used to toggle the [FET_EN] bit setting. The FET Test subcommands are shown below.

Table 5-7. FET Test Mode Subcommands

Subcommand	Description
0x001C PDSGTEST()	Only functional in FET Test mode, toggles PDSG FET state
0x001E PCHGTEST()	Only functional in FET Test mode, toggles PCHG FET state
0x001F CHGTEST()	Only functional in FET Test mode, toggles CHG FET state
0x0020 DSGTEST()	Only functional in FET Test mode, toggles DSG FET state

In normal operation, the FETs can be controlled autonomously by the device or manually using FET Control subcommands from the host. The ***Settings:FET:FET Options[FET_CTRL_EN]*** must be set for the device to enable the FETs at all. When this is set, the device will generally enable the FETs if there is nothing present which would block them, such as a protection fault or control from the host. Even if the host plans to control the FETs manually, the device may still change FET states based on the device settings, such as if body diode protection is enabled. If the intent is for the device to monitor and provide an interrupt or flag for a protection event, but the device is not to autonomously disable a FET in response to it, the appropriate configuration bit in ***Settings:Protection:CHG FET Protections A – C*** and ***Settings:Protection:DSG FET Protections A – C*** can be cleared. In this case, the host can monitor the interrupt or flags and decide whether to manually disable the FET.

For the CHG FET turnoff action to occur immediately when a fault is detected, the value of ***Settings:Protection:CHG FET Protections A*** should only be set to 0x18 or 0x98. Setting it to other values can cause FET turnoff action to be delayed by up to 250 ms in NORMAL mode or 1 second in SLEEP mode.

For the DSG FET turnoff action to occur immediately when a fault is detected, the value of ***Settings:Protection:DSG FET Protections A*** should only be set to 0x80 or 0xE4. Setting it to other values can cause FET turnoff action to be delayed by up to 250 ms in NORMAL mode or 1 second in SLEEP mode.

During normal operation, the host can disable the FETs by asserting the CFETOFF or DFETOFF pins or by sending FET Control subcommands (Table 5-8). When the FET Control subcommands are used to disable a FET, a signal is latched which blocks the FET from being enabled. In order to allow the FET to be reenabled, it is first necessary to clear any signal blocking it. This can be accomplished by sending the appropriate FET Control subcommand (such as *0x0096 ALL_FETS_ON()*) to release a block created by an earlier subcommand. It is also necessary to ensure the CFETOFF or DFETOFF pins are deasserted. The FETs can only be enabled if nothing exists to block them (such as the latched FET Control subcommand signal, or the CFETOFF or DFETOFF signal asserted, or a separate enabled safety fault present).

The FET control subcommands for use during normal operation are shown below.

Table 5-8. FET Control Subcommands

Subcommand	Description
0x0093 DSG_PDSG_OFF()	Causes the DSG and PDSG FETs to be disabled. This subcommand should not be used if the DDSG pin is being used in DDSG mode.
0x0094 CHG_PCHG_OFF()	Causes the CHG and PCHG FETs to be disabled. This subcommand should not be used if the DCHG pin is being used in DCHG mode.
0x0095 ALL_FETS_OFF()	Causes the DSG, PDSG, CHG, and PCHG FETs to be disabled
0x0096 ALL_FETS_ON()	Allows all FETs to be enabled if nothing else is blocking them
0x0097 FET_CONTROL()	An 8-bit field is sent with bits 3:0 matching those in *0x7F FET Status()*. When a bit is set using this subcommand, the corresponding FET is blocked from being enabled. This subcommand should not be used if the DDSG or DCHG pins are being used in DDSG or DCHG mode.

For security purposes, the device can be set to either allow or ignore the host FET Control commands while in SEALED mode using ***Settings:FET:FET Options[HOST_FET_EN]***.

The present status of the FET drivers is provided in *0x0057 Manufacturing Status()* subcommand, which includes the status bits described below.

Table 5-9. *0x0057 Manufacturing Status()* Bit Definitions

Bit	Name	Description
7	OTPW_EN	The OTP is not blocked from being written.
6	PF_EN	Permanent Fails are enabled.
5	PDSG_TEST	PDSG FET is enabled in FET Test mode.
4	FET_EN	FETs are enabled for device operation, otherwise the device is in FET Test mode.
3	RSVD	Reserved
2	DSG_TEST	DSG FET is enabled in FET Test mode.
1	CHG_TEST	CHG FET is enabled in FET Test mode.
0	PCHG_TEST	PCHG FET is enabled in FET Test mode.

5.2.3.2.1 PRECHARGE Mode

The BQ769142 device includes precharge functionality, which can be used to reduce the charging current for an undervoltage battery by charging using a high-side PCHG PFET (driven from the PCHG pin) with series resistor until the battery reaches a programmable voltage level. When the minimum cell voltage is less than ***Settings:FET:Precharge Start Voltage***, the PCHG FET will be used for charging. Setting this threshold to 0 disables PRECHARGE mode. PRECHARGE mode is deactivated when the minimum cell voltage reaches or exceeds a level given by ***Settings:FET:Precharge Stop Voltage***. The status of the PCHG FET is provided in the *0x7F FET Status()[PCHG_FET]* register bit.

5.2.3.2.2 PREDISCHARGE Mode

The BQ769142 device includes predischarge functionality, which can be used to reduce inrush current when the load is initially powered, by first enabling a high-side PDSG PFET (driven from the PDSG pin) with series resistor, which enables the load to slowly charge. If PREDISCHARGE mode is enabled, whenever the DSG FET is turned on to power the load, the device will first enable the PDSG FET, then transition to turn on the DSG FET and turn off the PDSG FET. PREDISCHARGE mode is enabled when ***Settings:FET:FET Options[PDSG_EN]*** is set.

When PREDISCHARGE mode is activated, the device remains in this mode until either a timeout is reached, or the voltage at the LD pin rises to within a programmable delta of the top-of-stack voltage, or both. The timeout can be set from 10 ms to 2550 ms in steps of 10 ms, using ***Settings:FET:Predischarge Timeout***. If the timeout is set to 0, then the device does not use a timeout and exits PREDISCHARGE mode when the voltage condition is met. The voltage delta is programmable from 10 mV to 2550 mV in steps of 10 mV, using ***Settings:FET:Predischarge Stop Delta***. If the voltage delta is set to 0, the device does not use a voltage condition and exits PREDISCHARGE mode based on the timeout.

Note

The voltage delta is checked by the device every 250 ms. The status of the PDSG FET is provided in the *0x7F FET Status()[PDSG_FET]* register bit.

If the ***Settings:FET:FET Options[PDSG_EN]*** bit is set and the DFETOFF or BOTHOFF signal is asserted, the DSG and PDSG FETs are disabled, but the device is initially blocked from entering SLEEP mode (if already in SLEEP mode, the device returns to NORMAL mode when the signal is asserted). SLEEP mode can again be allowed if the host sends the *DSG_PDSG_OFF()* or *ALL_FETS_OFF()* subcommand, or a protection fault occurs (such as a Host Watchdog Fault or an OTF fault).

5.2.4 Cell Overvoltage Protection

The BQ769142 device integrates Cell Overvoltage Protection (COV), monitoring the voltage of every cell using a comparator-based circuit, and triggering a COV alert or fault when a cell voltage exceeds the COV threshold. The COV threshold is programmable from 1.012 V to 5.566 V in 50.6 mV steps and is set by the ***Protections:COV:Threshold*** configuration register. The COV protection is enabled using the ***Settings:Protection:Enabled Protections A:[COV]*** configuration bit.

The COV circuitry triggers an alert signal when an overvoltage event is first detected, then will trigger a fault after a programmable detection delay, COV_DLY, which can be set from 10 ms to 6762 ms in units of 3.3 ms, with the actual delay being 3.3 ms × (2 + setting). The setting 0x0 disables the protection. The delay is set by the ***Protections:COV:Delay*** configuration register.

When a COV fault is triggered, it will recover if the maximum cell voltage drops below the COV threshold by a COV_HYS hysteresis level, which is programmable from 100 mV to 1 V in steps of 50 mV, for ***Protections:Recovery:Time***. The COV_HYS hysteresis level is set by the ***Protections:COV:Recovery Hysteresis*** configuration register.

When an COV fault is triggered, the device will turn off the CHG FET if configured for autonomous FET control based on setting in ***Settings:Protection:CHG FET Protections A[COV]*** (the DSG FET remains enabled if already enabled). The device will recover (if configured for autonomous FET control) based on all cell voltages being below COV threshold – COV_HYS for ***Protections:Recovery:Time***.

The BQ769142 device also includes a Cell Overvoltage Latch (COVL) protection, which can create a fault if multiple COV failures occur within a programmable time window. Whenever a COV fault is triggered, the COVL latch counter is incremented. After the device recovers, it will decrement the COVL counter after a programmable recovery time window (given by ***Protections:COVL:Counter Dec Delay***) if no further COV faults are detected. If the COVL counter reaches a programmable latch limit (given by ***Protections:COVL:Latch Limit***), it will trigger a COVL fault.

The COVL protection recovers after a programmable delay given by ***Protections:COVL:Recovery Time***, but it is important that ***Protections:COVL:Counter Dec Delay*** be set shorter than ***Protections:COVL:Recovery Time***, otherwise COVL would immediately trip again after recovery, since the COVL counter would not have decremented yet. The COVL protection is enabled using the ***Settings:Protection:Enabled Protections C:[COVL]*** configuration bit. Table 5-10 provides further details.

Note

Timing on COV changes while cell balancing is active, as described in *Cell Balancing Loop Slow-down Setting*.

Table 5-10. Overvoltage Protection Operation

Status	Condition	Action
Normal	Max cell voltage < ***Protections:COV:Threshold***	*Safety Alert A()[COV]* = 0 Decrement COVL counter by one after each ***Protections:COVL:Counter Dec Delay*** period if COVL counter > 0
Alert	Max cell voltage ≥ ***Protections:COV:Threshold***	*Safety Alert A()[COV]* = 1
Trip	Max cell voltage ≥ ***Protections:COV:Threshold*** for ***Protections:COV:Delay*** duration	*Safety Alert A()[COV]* = 0 *Safety Status A()[COV]* = 1 *Alarm Raw Status()[XCHG]* = 1 if autonomous FET control is enabled Increment COVL counter
Recovery	*Safety Status A()[COV]* = 1 and Max cell voltage < ***Protections:COV:Threshold***–***Protections:COV:Recovery Hysteresis*** for ***Protections:Recovery:Time***	*Safety Status A()[COV]* = 0 *Alarm Raw Status()[XCHG]* = 0 if autonomous FET control is enabled
Latch Alert	COVL counter > 0	*Safety Alert C()[COVL]* = 1
Latch Trip	COVL counter ≥ ***Protections:COVL:Latch Limit***	*Safety Status C()[COVL]* = 1 *Safety Alert C()[COVL]* = 0 *Alarm Raw Status()[XCHG]* = 1 if autonomous FET control is enabled

Table 5-10. Overvoltage Protection Operation (continued)

Status	Condition	Action
Latch Reset	*SafetyStatus()[COVL]* = 1 for ***Protections:COVL:Recovery Time*** duration	*Safety Status C()[COVL]* = 0 *Alarm Raw Status()[XCHG]* = 0 if *Safety Status A()[COV]* = 0 and autonomous FET control is enabled

When a COV fault is triggered, a snapshot of all cell voltages is captured and can be accessed through the *0x0081 COV_SNAPSHOT()* subcommand, which has the format shown in Table 5-11.

Table 5-11. *0x0081 COV_SNAPSHOT()* Subcommand Format

Subcommand Address	Bytes Within Block	Name	Unit
0x0081	0–1	Cell 1 Voltage at COV	mV
	2–3	Cell 2 Voltage at COV	mv
	4–5	Cell 3 Voltage at COV	mV
	6–7	Cell 4 Voltage at COV	mV
	8–9	Cell 5 Voltage at COV	mV
	10–11	Cell 6 Voltage at COV	mV
	12–13	Cell 7 Voltage at COV	mV
	14–15	Cell 8 Voltage at COV	mV
	16–17	Cell 9 Voltage at COV	mV
	18–19	Cell 10 Voltage at COV	mV
	20–21	Cell 11 Voltage at COV	mV
	22–23	Cell 12 Voltage at COV	mV
	24–25	Reserved	–
	26–27	Cell 13 Voltage at COV	mV
	28–29	Reserved	–
	30–31	Cell 14 Voltage at COV	mV

5.2.5 Cell Undervoltage Protection

The BQ769142 device integrates Cell Undervoltage Protection (CUV), monitoring the voltage of every cell using a comparator-based circuit, and triggering a CUV alert or fault when a cell voltage falls below the CUV threshold. The CUV threshold is programmable from 1.012 V to 4.048 V in 50.6 mV steps and is set by the ***Protections:CUV:Threshold*** configuration register. The CUV protection is enabled using the ***Settings:Protection:Enabled Protections A:[CUV]*** configuration bit.

The CUV circuitry triggers an alert signal when an undervoltage event is first detected, then triggers a fault after a programmable detection delay, CUV_DLY, which can be set from 10 ms to 6765 ms in units of 3.3 ms, with the actual delay being 3.3 ms × (2 + setting). The setting 0x0 disables the protection. The delay is set by the ***Protections:CUV:Delay*** configuration register.

When a CUV fault is triggered, the fault will recover if the voltage rises above the CUV threshold by a value of CUV_HYS, which is programmable from 100 mV to 1 V in steps of 50 mV, for ***Protections:Recovery:Time***. This hysteresis level is set by the ***Protections:CUV:Recovery Hysteresis*** configuration register.

When CUV is triggered, the device turns off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections A[CUV]*** (the CHG FET remains enabled if already enabled). The device recovers (if configured for autonomous recovery), based on all cell voltages being above CUV threshold + CUV_HYS. Table 5-12 provides further details.

Note

Timing on CUV changes while cell balancing is active, as described in *Cell Balancing Loop Slow-down Setting*.

Table 5-12. Undervoltage Protection Operation

Status	Condition	Action
Normal	Min cell voltage > ***Protections:CUV:Threshold***	*Safety Alert A()[CUV]* = 0
Alert	Min cell voltage ≤ ***Protections:CUV:Threshold***	*Safety Alert A()[CUV]* = 1
Trip	Min cell voltage ≤ ***Protections:CUV:Threshold*** for ***Protections:CUV:Delay*** duration	*Safety Alert A()[CUV]* = 0 *Safety Status A()[CUV]* = 1 *Alarm Raw Status()[XDSG]* = 1 if configured for autonomous FET control
Recovery	*Safety Status A()[CUV]* = 1 and Min cell voltage > ***Protections:CUV:Threshold*** + ***Protections:CUV:Recovery Hysteresis*** for ***Protections:Recovery:Time***	*Safety Status A()[CUV]* = 0 *Alarm Raw Status()[XDSG]* = 0 if configured for autonomous FET control

When a CUV fault is triggered, a snapshot of all cell voltages is captured and can be accessed through the *0x0080 CUV_SNAPSHOT()* subcommand, which has the format shown below.

Table 5-13. *0x0080 CUV_SNAPSHOT()* Subcommand Format

Subcommand Address	Bytes Within Block	Name	Unit
0x0080	0–1	Cell 1 Voltage at CUV	mV
	2–3	Cell 2 Voltage at CUV	mV
	4–5	Cell 3 Voltage at CUV	mV
	6–7	Cell 4 Voltage at CUV	mV
	8–9	Cell 5 Voltage at CUV	mV
	10–11	Cell 6 Voltage at CUV	mV
	12–13	Cell 7 Voltage at CUV	mV
	14–15	Cell 8 Voltage at CUV	mV
	16–17	Cell 9 Voltage at CUV	mV
	18–19	Cell 10 Voltage at CUV	mV
	20–21	Cell 11 Voltage at CUV	mV
	22–23	Cell 12 Voltage at CUV	mV
	24–25	Reserved	–
	26–27	Cell 13 Voltage at CUV	mV
	28–29	Reserved	–
	30–31	Cell 14 Voltage at CUV	mV

5.2.6 Short Circuit in Discharge Protection

The BQ769142 device integrates Short Circuit in Discharge Protection (SCD) using a dedicated comparator that monitors the differential voltage across the SRN–SRP pins and triggers an SCD alert or fault when the voltage exceeds a programmable threshold VSCD. The VSCD threshold is programmable as 10 mV, 20 mV, 40 mV, 60 mV, 80 mV, 100 mV, 125 mV, 150 mV, 175 mV, 200 mV, 250 mV, 300 mV, 350 mV, 400 mV, 450 mV, and 500 mV, and is set by the ***Protections:SCD:Threshold*** configuration register. The SCD protection is enabled using the ***Settings:Protection:Enabled Protections A:[SCD]*** configuration bit.

The SCD circuitry triggers an alert signal when a short circuit event is first detected, then triggers a fault after a programmable detection delay, SCD_DLY, which can be set to fastest, or 15 µs to 450 µs in steps of 15 µs. The fastest setting can result in detection of a short circuit with only comparator delay, which may be < 1

µs depending on the overdrive of the threshold. The delay is set by the ***Protections:SCD:Delay*** configuration register.

When an SCD fault is triggered, the device will turn off the DSG FET if configured for autonomous FET control in ***Settings:Protection:DSG FET Protections A***. The CHG FET may also be disabled autonomously, based on the setting in ***Settings:Protection:CHG FET Protections A***. The device recovers (if configured for autonomous recovery) after a programmable delay given by ***Protections:SCD:Recovery Time***.

The BQ769142 device also includes a Short Circuit in Discharge Latch (SCDL) protection, which can create a fault and Permanent Fail (PF) if multiple SCD failures occur within a programmable time window. Whenever an SCD fault is triggered, the SCDL latch counter is incremented. After the device recovers, it decrements the SCDL counter after a programmable time of ***Protections:SCDL:Counter Dec Delay*** if no further SCD faults are detected. If the SCDL counter reaches a programmable latch limit given by ***Protections:SCDL:Latch Limit***, it triggers an SCDL fault and can also trigger an SCDL PF.

The SCDL protection is enabled using the ***Settings:Protection:Enabled Protections C:[SCDL]*** configuration bit. If the SCDL protection fault is triggered, the device begins recovery if the load detect feature (see *Load Detect Functionality*) is enabled and detects the load is removed, or if charging current is detected, or after a programmable time, or the host sends a *0x009C SCDL_RECOVER()* subcommand. In order to recover based on charging current, the ***Settings:Protection:Protection Configuration[SCDL_CURR_RECOV]*** must be set, the device must be in series FET configuration, and the CHG FET must be enabled. The device will begin recovery from SCDL if a current is detected greater than or equal to ***Protections:SCDL:Recovery Threshold*** for ***Protections:SCDL:Recovery Time*** duration. If recovery is preferred based only on time, then the recovery based on charging current can be used, with the current threshold set to a small discharge current.

Note

"Beginning recovery" means the SCDL counter will begin decrementing every ***Protections:SCDL:Counter Dec Delay*** interval if no new SCD faults occur.

Short Circuit in Discharge Protection Operation provides further details.

Table 5-14. Short Circuit in Discharge Protection Operation

Status	Condition	Action
Normal	V_{SRN}–V_{SRP} ≤ setting selected by***Protections:SCD:Threshold***	*Safety Alert A()[SCD]* = 0 *PF Alert B()[SCDL]* = 0 if SCDL counter = 0 *PF Alert B()[SCDL]* = 1 if SCDL counter > 0 Decrement SCDL counter by one after each ***Protections:SCDL:Counter Dec Delay*** period if SCDL counter > 0
Alert	V_{SRN}–V_{SRP} > setting selected by***Protections:SCD:Threshold***	*Safety Alert A()[SCD]* = 1
Trip	V_{SRN}–V_{SRP} > setting selected by***Protections:SCD:Threshold*** for ***Protections:SCD:Delay*** duration	*Safety Alert A()[SCD]* = 0 *Safety Status A()[SCD]* = 1 *Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled *Alarm Raw Status()[XCHG]* = 1 depending on setting Increment SCDL counter
Recovery	*Safety Status A()[SCD]* = 1 and V_{SRN}–V_{SRP} ≤ setting selected by***Protections:SCD:Threshold*** for ***Protections:SCD:Recovery Time*** duration	*Safety Status A()[SCD]* = 0 *Alarm Raw Status()[XDSG]* = 0 if autonomous FET control is enabled *Alarm Raw Status()[XCHG]* = 0 depending on setting
Latch Alert	SCDL counter > 0	*Safety Alert C()[SCDL]* = 1 *PF Alert B()[SCDL]* = 1

Table 5-14. Short Circuit in Discharge Protection Operation (continued)

Status	Condition	Action
Latch Trip	SCDL counter ≥ ***Protections:SCDL:Latch Limit***	*Safety Status C()[SCDL]* = 1 *PF Status B()[SCDL]* = 1 *PF Alert B()[SCDL]* = 0 *Safety Alert C()[SCDL]* = 0 *Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled *Alarm Raw Status()[XCHG]* = 1 depending on setting
Latch Reset (based on Load Detect)	*Safety Status C()[SCDL]* = 1 and load is detected removed using the Load Detect function	Decrement SCDL counter by one after each ***Protections:SCDL:Counter Dec Delay*** period if SCDL counter > 0 *Safety Status C()[SCDL]* = 0 if SCDL counter < ***Protections:SCDL:Latch Limit*** *Alarm Raw Status()[XDSG]* = 0 and *Alarm Raw Status()[XCHG]* = 0 if *Safety Status A()[SCD]* = 0 and autonomous FET control is enabled
Latch Reset (based on charging current and time)	*Safety Status C()[SCDL]* = 1 and CC1 Current ≥ ***Protections:SCDL:Recovery Threshold*** for ***Protections:SCDL:Recovery Time*** duration, if ***Settings:Protection:Protection Configuration[SCDL_CURR_RECOV]*** = 1	Decrement SCDL counter by one after each ***Protections:SCDL:Counter Dec Delay*** period if SCDL counter > 0 *Safety Status C()[SCDL]* = 0 if SCDL counter < ***Protections:SCDL:Latch Limit*** *Alarm Raw Status()[XDSG]* = 0 and *Alarm Raw Status()[XCHG]* = 0 if *Safety Status A()[SCD]* = 0 and autonomous FET control is enabled
Latch Reset (host-command)	*Safety Status C()[SCDL]* = 1 and host sends *0x009C SCDL_RECOVER()*	Decrement SCDL counter by one after each ***Protections:SCDL:Counter Dec Delay*** period if SCDL counter > 0 *Safety Status C()[SCDL]* = 0 if SCDL counter < ***Protections:SCDL:Latch Limit*** *Alarm Raw Status()[XDSG]* = 0 and *Alarm Raw Status()[XCHG]* = 0 if *Safety Status A()[SCD]* = 0 and autonomous FET control is enabled

5.2.7 Overcurrent in Charge Protection

The BQ769142 device integrates Overcurrent in Charge Protection (OCC) using a comparator that monitors the differential voltage across the SRP–SRN pins and triggers an OCC alert or fault when the voltage exceeds a programmable threshold VOCC. The VOCC threshold is programmable from 4 mV to 124 mV in 2 mV steps using the ***Protections:OCC:Threshold*** configuration register. The OCC protection is enabled using the ***Settings:Protection:Enabled Protections A:[OCC]*** configuration bit.

The OCC circuitry triggers an alert signal when an overcurrent in charge event is first detected, then will trigger a fault after a programmable detection delay, OCC_DLY, which can be set from 10 ms to 426 ms in units of 3.3 ms, with the actual delay being 3.3 ms × (2 + setting). The setting 0x0 disables the protection. The delay is set by the ***Protections:OCC:Delay*** configuration register.

When an OCC fault is triggered, the device will turn off the CHG FET if configured for autonomous FET control using ***Settings:Protection:CHG FET Protections A.*** (the DSG FET may remain enabled if already enabled). The device will recover (if configured for autonomous recovery) when the voltage measured on the PACK pin falls at least ***Protections:OCC:PACK-TOS Delta*** below the voltage measured at the top-of-stack for a duration of ***Protections:Recovery:Time***, or a current less than or equal to ***Protections:OCC:Recovery Threshold*** (that is, a discharge current) is present for a duration of ***Protections:Recovery:Time***.

Table 5-15 provides further details.

Table 5-15. Overcurrent in Charge Protection Operation

Status	Condition	Action
Normal	V_{SRP}–V_{SRN} ≤ setting selected by ***Protections:OCC:Threshold***	*Safety Alert A()[OCC]* = 0
Alert	V_{SRP}–V_{SRN} > setting selected by ***Protections:OCC:Threshold***	*Safety Alert A()[OCC]* = 1
Trip	V_{SRP}–V_{SRN} > setting selected by ***Protections:OCC:Threshold*** for ***Protections:OCC:Delay*** duration	*Safety Alert A()[OCC]* = 0 *Safety Status A()[OCC]* = 1 *Alarm Raw Status()[XCHG]* = 1 if autonomous FET control is enabled
Recovery (charger detached)	*Safety Status A()[OCC]* = 1 and *PACK Voltage()* ≤ *Stack Voltage()*–***Protections:OCC:PACK-TOS Delta*** or CC1 Current ≤ ***Protections:OCC:Recovery Threshold*** for ***Protections:Recovery:Time*** duration.	*Safety Status A()[OCC]* = 0 *Alarm Raw Status()[XCHG]* = 0 if autonomous FET control is enabled

5.2.8 Overcurrent in Discharge 1, 2, and 3 Protections

The BQ769142 device integrates Overcurrent in Discharge 1 (OCD1) and Overcurrent in Discharge 2 (OCD2) Protections using a comparator that monitors the differential voltage across the SRN–SRP pins and triggers an OCD1 or OCD2 alert or fault when the voltage exceeds a programmable threshold VOCD1 or VOCD2. The VOCD1 and VOCD2 thresholds are independently programmable from 4 mV to 200 mV in 2-mV steps using the ***Protections:OCD1:Threshold*** and ***Protections:OCD2:Threshold*** configuration registers. The OCD1 and OCD2 protections are enabled using the ***Settings:Protection:Enabled Protections A:[OCD1]*** and ***Settings:Protection:Enabled Protections A:[OCD2]*** configuration bits.

The OCD1 and OCD2 circuitry triggers an alert signal when an overcurrent in discharge event is first detected, then will trigger a fault when this condition persists for a programmable detection delay, OCD1_DLY or OCD2_DLY, which can be independently set from 10 ms to 426 ms in units of 3.3 ms, with the actual delay being 3.3 ms × (2 + setting). The delay is set by the ***Protections:OCD1:Delay*** and ***Protections:OCD2:Delay*** configuration registers.

The device also integrates an Overcurrent in Discharge 3 (OCD3) Protection using the CC1 current measurement from the coulomb counter ADC, triggering an OCD3 alert or fault when the current is more negative (that is, an excessive discharge current) than a programmable threshold given by ***Protections:OCD3:Threshold***. An alert signal is triggered when an overcurrent in discharge event is first detected, then a fault signal is triggered when this condition persists for a programmable detection delay, OCD3_DLY, which can be set from 0 sec to 255 sec in units of 1 sec. The delay is set by the ***Protections:OCD3:Delay*** configuration register. The OCD3 protection is enabled using the ***Settings:Protection:Enabled Protections C:[OCD3]*** configuration bit.

When an OCD1, OCD2, or OCD3 fault is triggered, the device will turn off the DSG FET if configured for autonomous FET control using ***Settings:Protection:DSG FET Protections A[OCD2][OCD1]*** or ***Settings:Protection:DSG FET Protections C[OCD3]*** configuration bits. The device will recover when a charging current is detected greater than or equal to ***Protections:OCD:Recovery Threshold*** for ***Protections:Recovery:Time*** duration.

The BQ769142 device also includes an Overcurrent in Discharge Latch (OCDL) protection, which can create a fault if multiple OCD1 or OCD2 or OCD3 failures occur within a programmable time window. Whenever an OCD1 or OCD2 or OCD3 fault is triggered, the OCDL latch counter is incremented. After the device recovers, it will decrement the OCDL counter after a programmable recovery time of ***Protections:OCDL:Counter Dec Delay*** if

no further OCD1, OCD2, or OCD3 faults are detected. If the OCDL counter exceeds a programmable latch limit given by ***Protections:OCDL:Latch Limit***, it will trigger an OCDL fault. An OCDL alert is generated whenever the OCDL counter is greater than zero.

The OCDL protection is enabled using the ***Settings:Protection:Enabled Protections C:[OCDL]*** configuration bit. If the OCDL protection fault is triggered, the device can recover if the load detect feature (see Section 5.2.18) is enabled and detects the load is removed, or if charging current is detected, or after a programmable time, or the host sends a *0x009B OCDL_RECOVER()* subcommand. In order to recover based on charging current, the ***Settings:Protection:Protection Configuration[OCDL_CURR_RECOV]*** must be set, the device must be in series FET configuration, and the CHG FET must be enabled. The device will then recover from OCDL if a current is detected greater than or equal to ***Protections:OCDL:Recovery Threshold*** for ***Protections:OCDL:Recovery Time*** duration. If recovery is preferred based only on time, then the recovery based on charging current can be used, with the current threshold set to a small discharge current.

Further detail is described in the table below.

Table 5-16. Overcurrent in Discharge 1, 2 and 3 Protection Operation

Status	Condition	Action
Normal	V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:OCD1:Threshold*** V_{SRN}–V_{SRP} ≤ setting selected by ***Protections:OCD2:Threshold*** CC1 Current > ***Protections:OCD3:Threshold***	*Safety Alert A()[OCD1]* = 0 *Safety Alert A()[OCD2]* = 0 *Safety Alert C()[OCD3]* = 0 Decrement OCDL counter by one after each ***Protections:OCDL:Counter Dec Delay*** period if OCDL counter > 0
Alert	V_{SRN}–V_{SRP} > setting selected by ***Protections:OCD1:Threshold***	*Safety Alert A()[OCD1]* = 1
Alert	V_{SRN}–V_{SRP} > setting selected by ***Protections:OCD2:Threshold***	*Safety Alert A()[OCD2]* = 1
Alert	CC1 Current ≤ ***Protections:OCD3:Threshold***	*Safety Alert C()[OCD3]* = 1
Trip	V_{SRN}–V_{SRP} > setting selected by ***Protections:OCD1:Threshold*** for ***Protections:OCD1:Delay*** duration	*Safety Alert A()[OCD1]* = 0 *Safety Status A()[OCD1]* = 1 *Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled; Increment OCDL counter
Trip	V_{SRN}–V_{SRP} > setting selected by ***Protections:OCD2:Threshold*** for ***Protections:OCD2:Delay*** duration	*Safety Alert A()[OCD2]* = 0 *Safety Status A()[OCD2]* = 1 *Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled; Increment OCDL counter
Trip	CC1 Current ≤ ***Protections:OCD3:Threshold*** for ***Protections:OCD3:Delay*** duration	*Safety Alert C()[OCD3]* = 0 *Safety Status C()[OCD3]* = 1 *Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled; Increment OCDL counter
Recovery	*Safety Status A()[OCD1]* = 1 or *Safety Status A()[OCD2]* = 1 or *Safety Status C()[OCD3]* = 1 and CC1 Current > ***Protections:OCD:Recovery Threshold*** for ***Protections:Recovery:Time*** duration	*Safety Status A()[OCD1]* = 0 *Safety Status A()[OCD2]* = 0 *Safety Status C()[OCD3]* = 0 *Alarm Raw Status()[XDSG]* = 0
Latch Alert	OCDL counter > 0	*Safety Alert C()[OCDL]* = 1
Latch Trip	OCDL counter ≥ ***Protections:OCDL:Latch Limit***	*Safety Status C()[OCDL]* = 1 *Safety Alert C()[OCDL]* = 0 *Alarm Raw Status()[XDSG]* = 1 if autonomous FET control is enabled;

Table 5-16. Overcurrent in Discharge 1, 2 and 3 Protection Operation (continued)

Status	Condition	Action
Latch Reset (based on Load Detect)	*Safety Status C()[OCDL]* = 1 and load is detected removed using the Load Detect function	*Safety Status C()[OCDL]* = 0 Reset OCDL counter *Alarm Raw Status()[XDSG]* = 0 if *Safety Status A()[OCD1]* = 0 and *Safety Status A()[OCD2]* = 0 and *Safety Status C()[OCD3]* = 0
Latch Reset (based on charging current)	*Safety Status C()[OCDL]* = 1 and CC1 Current > ***Protections:OCDL:Recovery Threshold***	*Safety Status C()[OCDL]* = 0 Reset OCDL counter *Alarm Raw Status()[XDSG]* = 0 if *Safety Status A()[OCD1]* = 0 and *Safety Status A()[OCD2]* = 0 and *Safety Status C()[OCD3]* = 0
Latch Reset (host-command)	*Safety Status C()[OCDL]* = 1 and host sends *0x009B OCDL_RECOVER()*	*Safety Status C()[OCDL]* = 0 Reset OCDL counter *Alarm Raw Status()[XDSG]* = 0 if *Safety Status A()[OCD1]* = 0 and *Safety Status A()[OCD2]* = 0 and *Safety Status C()[OCD3]* = 0

5.2.9 Overtemperature in Charge Protection

The BQ769142 device integrates an Overtemperature in Charge (OTC) Protection that triggers an alert or fault when the cell temperature is greater than or equal to a programmable threshold TOTC. The TOTC threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:OTC:Threshold*** configuration register. The OTC protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTC]*** configuration bit.

The OTC protection triggers an alert signal when an overtemperature in charge event is first detected, then will trigger a fault after a programmable detection delay, OTC_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:OTC:Delay*** configuration register.

When an OTC fault is triggered, the device will turn off the CHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections B[OTC].*** The device will recover when the temperature is less than or equal to the threshold set by ***Protections:OTC:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the OTC protection is the maximum of all temperature readings that are designated for cell temperature, and can include the internal temperature measurement as well as all external thermistors which are enabled.

5.2.10 Overtemperature in Discharge Protection

The BQ769142 device integrates an Overtemperature in Discharge (OTD) Protection that triggers an alert or fault when the cell temperature is greater than or equal to a programmable threshold TOTD. The TOTD threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:OTD:Threshold*** configuration register. The OTD protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTD]*** configuration bit.

The OTD protection triggers an alert signal when an overtemperature in discharge event is first detected, then will trigger a fault after a programmable detection delay, OTD_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:OTD:Delay*** configuration register.

When an OTD fault is triggered, the device will turn off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections B[OTD]***. The device will recover when the temperature is less than or equal to the temperature set by ***Protections:OTD:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the OTD protection is the maximum of all temperature readings that are designated for cell temperature, and can include the internal temperature measurement as well as all external thermistors which are enabled.

5.2.11 Overtemperature FET Protection

The BQ769142 device integrates an Overtemperature FET (OTF) Protection that triggers an alert or fault when the FET temperature is greater than or equal to a programmable threshold TOTF. The TOTF threshold is programmable from 0°C to 150°C in 1°C steps using the ***Protections:OTF:Threshold*** configuration register. The OTF protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTF]*** configuration bit.

The OTF protection triggers an alert signal when an overtemperature FET event is first detected, then will trigger a fault after a programmable detection delay, OTF_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:OTF:Delay*** configuration register.

When an OTF fault is triggered, the device will turn off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections B[OTF]*** and ***Settings:Protection:CHG FET Protections B[OTF]***. The device will recover (if configured for autonomous recovery) when the temperature is less than or equal to the threshold set by ***Protections:OTF:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the OTF protection is the maximum of all temperature readings that are designated for FET temperature, and can include the internal temperature measurement as well as all external thermistors which are enabled.

5.2.12 Internal Overtemperature Protection

The BQ769142 device integrates an Internal Overtemperature (OTINT) Protection that triggers an alert or fault when the internal temperature is greater than or equal to a programmable threshold TOTINT. The TOTINT threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:OTINT:Threshold*** configuration register. The OTINT protection is enabled using the ***Settings:Protection:Enabled Protections B:[OTINT]*** configuration bit.

The OTINT protection triggers an alert signal when an internal overtemperature event is first detected, then will trigger a fault after a programmable detection delay, OTINT_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:OTINT:Delay*** configuration register.

When an OTINT fault is triggered, the device will turn off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections B[OTINT]*** and ***Settings:Protection:CHG FET Protections B[OTINT]***. The device will recover (if configured for autonomous recovery) when the temperature is less than or equal to the threshold set by ***Protections:OTINT:Recovery*** for ***Protections:Recovery:Time*** duration.

5.2.13 Undertemperature in Charge Protection

The BQ769142 device integrates an Undertemperature in Charge (UTC) Protection that triggers an alert or fault when the cell temperature is less than or equal to a programmable threshold TUTC. The TUTC threshold is programmable from –40°C to 120°C in 1°C steps using the ***Protections:UTC:Threshold*** configuration register. The UTC protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTC]*** configuration bit.

The UTC protection triggers an alert signal when an undertemperature in charge event is first detected, then triggers a fault after a programmable detection delay, UTC_DLY, which can be set from 0 s to 255 s in units of 1 second. The delay is set by the ***Protections:UTC:Delay*** configuration register.

When a UTC fault is triggered, the device turns off the CHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections B[UTC]***. The device recovers when the temperature is greater than or equal to the threshold set by ***Protections:UTC:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the UTC protection is the minimum of all temperature readings that are designated for cell temperature, and can include the internal temperature measurement, as well as all external thermistors that are enabled.

5.2.14 Undertemperature in Discharge Protection

The BQ769142 device integrates an Undertemperature in Discharge (UTD) Protection that triggers an alert or fault when the cell temperature is less than or equal to a programmable threshold TUTD. The TUTD threshold is programmable from –40°C to 120°C in 1°C steps using the ***Protections:UTD:Threshold*** configuration register. The UTD protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTD]*** configuration bit.

The UTD protection triggers an alert signal when an undertemperature in charge event is first detected, then triggers a fault after a programmable detection delay, UTD_DLY, which can be set from 0 s to 255 s in units of 1 second. The delay is set by the ***Protections:UTD:Delay*** configuration register.

When a UTD fault is triggered, the device will turn off the DSG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:DSG FET Protections B[UTD]***. The device recovers when the temperature is greater than or equal to the threshold set by ***Protections:UTD:Recovery*** for ***Protections:Recovery:Time*** duration.

The temperature used by the UTD protection is the minimum of all temperature readings that are designated for cell temperature, and can include the internal temperature measurement, as well as all external thermistors that are enabled.

5.2.15 Internal Undertemperature Protection

The BQ769142 device integrates an Internal Undertemperature (UTINT) Protection that triggers an alert or fault when the internal temperature is less than or equal to a programmable threshold TUTINT. The TUTINT threshold is programmable from -40°C to 120°C in 1°C steps using the ***Protections:UTINT:Threshold*** configuration register. The UTINT protection is enabled using the ***Settings:Protection:Enabled Protections B:[UTINT]*** configuration bit.

The UTINT protection triggers an alert signal when an undertemperature in charge event is first detected, then will trigger a fault after a programmable detection delay, UTINT_DLY, which can be set from 0-sec to 255-sec in units of 1-sec. The delay is set by the ***Protections:UTINT:Delay*** configuration register.

When a UTINT fault is triggered, the device will turn off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections B[UTINT]*** and ***Settings:Protection:CHG FET Protections B[UTINT]***. The device will recover (if configured for autonomous recovery) when the temperature is greater than or equal to the threshold set by ***Protections:UTINT:Recovery*** for ***Protections:Recovery:Time*** duration.

5.2.16 Host Watchdog Protection

The BQ769142 device integrates a Host Watchdog (HWD) Protection that triggers a fault when no communications are received for a programmable delay HWD_DLY. The HWD_DLY delay is programmable from a 0 second to 65535 second in 1-s steps using the ***Protections:HWD:Delay*** configuration register. The HWD protection is enabled using the ***Settings:Protection:Enabled Protections C:[HWDF]*** configuration bit.

When an HWD fault is triggered, the device turns off the DSG FET, the CHG FET, or both FETs if configured for autonomous FET control, based on settings in ***Settings:Protection:DSG FET Protections C[HWDF]*** and ***Settings:Protection:CHG FET Protections C[HWDF]***. The device recovers (if configured for autonomous recovery) when valid communications are received. Note that there is no safety alert for the HWD, only a safety status in *Safety Status C[HWDF]*.

If there is a concern that the HWD fault is caused by the host processor no longer operating properly, the BQ769142 device can be configured to disable or toggle the external REG1 and REG2 LDOs when the fault occurs. Based on ***Settings:Configuration:HWD Regulator Options***, the device can either leave the LDOs unchanged, disable the LDOs indefinitely, or disable the LDOs for a time period up to 15 s, then enable them again. This is controlled using the ***Settings:Configuration:HWD Regulator Options*** configuration register.

Note

If toggling is enabled and the device disables the LDOs after a HWD fault, after the toggle delay is completed the device recovers the LDOs to their state in ***Settings:REG12 Config[REG1_EN] and [REG2_EN]***, which may not be their state when the HWD fault occurred.

5.2.17 Precharge Timeout Protection

The BQ769142 device integrates a Precharge Timeout (PTO) Protection that triggers a fault when the device has been in PRECHARGE mode for a time duration PTO_DLY. The PTO_DLY duration is programmable from 0-sec to 65535-sec in 1-sec steps using the ***Protections:PTO:Delay*** configuration register. The timer for PTO_DLY only increments while the device is in PRECHARGE mode and the CC1 current exceeds a threshold given by ***Protections:PTO:Charge Threshold***. When the device is in PRECHARGE mode and the current is less than or equal to this threshold, the Precharge Timeout Suspend bit (*Safety Alert C()[PTOS]*) is set. If the timer reaches the threshold given by ***Protections:PTO:Delay***, the Precharge Timeout fault is triggered. The PTO timer is reset if a continuous discharge occurs with current larger in magnitude than ***Settings:Current Thresholds:Dsg Current Threshold*** and an amount of charge is accumulated equal or greater than a programmable level given by ***Protections:PTO:Reset***. The PTO protection is enabled using the ***Settings:Protection:Enabled Protections C:[PTO]*** configuration bit.

When a PTO fault is triggered, the device will turn off the PCHG FET if configured for autonomous FET control, based on the setting in ***Settings:Protection:CHG FET Protections C[PTO]***. PRECHARGE mode cannot restart until this fault is cleared by sending the *0x008A PTO_RECOVER()* subcommand.

5.2.18 Load Detect Functionality

When a Short Circuit in Discharge Latch or Overcurrent in Discharge Latch protection fault has occurred and the DSG FET is off, the device can be configured to recover when load removal is detected. This feature is useful if the system has a removable pack, such that the user can remove the pack from the system when a fault occurs, or if the effective system load that remains on the battery pack is higher than ≈20-kΩ when the DSG FET is disabled. The device will periodically enable a current source out the LD pin and will recover the fault if a voltage is detected at the LD pin above a 4 V level. If a low-impedance load is still present on the pack, the voltage the device measures on the LD pin will generally be below 4 V, preventing recovery based on Load Detect. If the pack has been removed from the system and the effective load is high, such that the current source generates a voltage on the LD pin above a 4 V level, then the device can recover from the fault. Note: typically a 10-kΩ resistor is connected between the PACK+ terminal and the LD pin, this resistance should be comprehended when considering the load impedance.

The Load Detect current is enabled for a time duration given by ***Protections:Load Detect:Active Time***, then is disabled for a time duration given by ***Protections:Load Detect:Retry Delay***, with this sequence repeating until the load has been detected as removed, or the accumulated time reaches ***Protections:Load Detect:Timeout***. The timeout is included to prevent the device continuously attempting Load Detect indefinitely and causing long-term drain on the pack. If the timeout is met, the Load Detect function will no longer operate until the latched faults have recovered through another means, or the *0x009D LOAD_DETECT_RESTART()* subcommand to restart the Load Detect is received.

If the ***Protections:Load Detect:Active Time*** is set to 0, then the Load Detect function is disabled. If the ***Protections:Load Detect:Retry Delay*** is set to 0, then the Load Detect current source will remain on continuously until timeout or recovery occurs.

The Load Detect current can be forced on or off through subcommands. If the ***Protections:Load Detect:Active Time*** is set to 0 and the *0x009E LOAD_DETECT_ON()* subcommand is sent, the Load Detect current source will be enabled. If the *0x009F LOAD_DETECT_OFF()* subcommand is sent, the Load Detect current source will be disabled.

When an SCDL or OCDL fault occurs and the DSG FET is disabled, the device may enter SLEEP mode, in which measurements of the LD pin voltage are only taken at intervals given by ***Power:Sleep:Voltage Time***. It is recommended to set the ***Protections:Load Detect:Active Time*** longer than ***Power:Sleep:Voltage Time***, to be sure that during each window when the current source is enabled, at least one measurement of the LD pin

voltage will occur. The status of the Load Detect function is provided in *0x00 Control Status()[LD_TIMEOUT, LD_ON]*.

5.3 Secondary Protections

5.3.1 Secondary Protections Overview

The BQ769142 device integrates a suite of checks on battery operation and status that can trigger a Permanent Fail (PF) if conditions are considered so serious that the pack should be permanently disabled. The various PF checks can be enabled individually based on configuration settings, along with associated thresholds and delays for most checks. When a Permanent Fail has occurred, the BQ769142 device can be configured to either simply provide a flag (see *PF Status A–D()* subcommands), or to indefinitely disable the protection FETs (if the ***Settings:Protection:Protection Configuration[PF_FETS]*** bit is set), or to assert the FUSE pin (if the ***Settings:Protection:Protection Configuration[PF_FUSE]*** bit is set) to permanently disable the pack. The FUSE pin can be used to blow an in-line fuse and also can monitor if a separate secondary protector IC has attempted to blow the fuse.

Since the device stores Permanent Fail status in RAM, that status would be lost when the device resets. To mitigate this, the device can write Permanent Fail status to OTP when the ***Settings:Protection:Protection Configuration[PF_OTP]*** bit is set. OTP programming may be delayed in low-voltage and high-temperature conditions until OTP programming can reliably be accomplished. Note: writes to OTP during operation are only allowed if ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is set. If ***Settings:Protection:Protection Configuration[PF_OTP]*** is set but ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is clear, Permanent Fail status is saved to RAM (and will be preserved during a partial reset) but will not be programmed to OTP. If ***Settings:Protection:Protection Configuration[PF_OTP]*** is not set, Permanent Fail status will be lost on any reset, including a partial reset through the RST_SHUT pin.

The information that can be written to OTP when a Permanent Fail occurs includes the values of *PF Status A ~ D* and a *Fuse Flag* byte, which indicates whether the fuse has been blown or not. This information can be read using the *0x0053 SAVED_PF_STATUS()* subcommand, which reports the information saved in RAM, even if the write to OTP has not yet completed.

Normally, a Permanent Fail causes the FETs to remain off indefinitely and the fuse may be blown. In that situation, no further action would be taken on further monitoring operations, and charging would no longer be possible. To avoid rapidly draining the battery, the device may be configured to enter DEEPSLEEP mode when a Permanent Fail occurs by setting the ***Settings:Protection:Protection Configuration[PF_DPSLP]*** configuration bit. Entrance to DEEPSLEEP mode will still be delayed until after fuse blow and OTP programming are completed, if those options are enabled.

When a Permanent Fail occurs, the device may be configured to either turn the REG1 and REG2 LDOs off (if ***Settings:Protection:Protection Configuration[PF_REGS]*** is set) or to leave them in their present state (if ***Settings:Protection:Protection Configuration[PF_REGS]*** is cleared). Once disabled, they may still be reenabled through command.

The Permanent Fail checks incorporate a programmable delay, to avoid triggering a PF fault on an intermittent condition or measurement. When the threshold is first detected as being met or exceeded by an enabled PF check, the device will set a PF Alert signal, which can be monitored using the *PF Alert A–D()* commands and can also trigger an interrupt on the ALERT pin using the *Alarm Status()[MSK_PFALERT]* register bit and its associated mask settings.

Note: the device only evaluates the conditions for Permanent Fail at one second intervals while in NORMAL and SLEEP modes, it does not continuously compare measurements to the Permanent Fail fault thresholds between intervals. Thus, it is possible for a condition to trigger a PF Alert if detected over threshold, but even if the condition drops back below threshold briefly between the one second interval checks, the PF Alert would not be cleared until it was detected below threshold at a periodic check.

Clear a Permanent Fail by issuing a full reset to the device. The now-obsolete *PF_RESET()* subcommand is no longer recommended for use.

5.3.2 Copper Deposition (CUDEP) Permanent Fail

When a cell is severely overdischarged, copper deposition can occur, resulting in very high impedance. If this occurs while the pack is in operation, the BQ769142 device will typically detect this and disable the pack before cells reach this low voltage (based on a SUV PF). However, if the device is in SHUTDOWN mode for an excessively long time period and the cells become overly discharged, the pack could still wake and enable the FETs if a charger were attached. If the FETs were turned on in this condition, the pack voltage would rise sharply due to the charging current, making the cells appear healthy. The CUDEP Permanent Fail is used to identify this condition and disable the pack. When enabled, this check keeps the FETs disabled at power up from SHUTDOWN mode until each cell voltage is greater than or equal to ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds. If any cell voltage is below ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds, the CUDEP Permanent Fail is triggered. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[CUDEP]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.3 Safety Undervoltage (SUV) Permanent Fail

The BQ769142 device integrates a Safety Undervoltage (SUV) Permanent Fail, which can permanently disable the pack if any cell voltage reaches or falls below a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SUV:Threshold***, and the delay is set by ***Permanent Fail:SUV:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SUV]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.4 Safety Overvoltage (SOV) Permanent Fail

The BQ769142 device integrates a Safety Overvoltage (SOV) Permanent Fail, which can permanently disable the pack if any cell voltage reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOV:Threshold***, and the delay is set by ***Permanent Fail:SOV:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOV]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.5 Safety Overcurrent in Charge (SOCC) Permanent Fail

The BQ769142 device integrates a Safety Overcurrent in Charge (SOCC) Permanent Fail, which can permanently disable the pack if the charging current reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOCC:Threshold***, and the delay is set by ***Permanent Fail:SOCC:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOCC]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.6 Safety Overcurrent in Discharge (SOCD) Permanent Fail

The BQ769142 device integrates a Safety Overcurrent in Discharge (SOCD) Permanent Fail, which can permanently disable the pack if the discharging current reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOCD:Threshold***, and the delay is set by ***Permanent Fail:SOCD:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOCD]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.7 Safety Cell Overtemperature (SOT) Permanent Fail

The BQ769142 device integrates a Safety Cell Overtemperature (SOT) Permanent Fail, which can permanently disable the pack if the maximum cell temperature reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOT:Threshold***, and the delay is set by ***Permanent Fail:SOT:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOT]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.8 Safety FET Overtemperature (SOTF) Permanent Fail

The BQ769142 device integrates a Safety FET Overtemperature (SOT) Permanent Fail, which can permanently disable the pack if the maximum FET temperature reaches or exceeds a programmable threshold for a programmable delay time. The threshold is set by ***Permanent Fail:SOTF:Threshold***, and the delay is set by

Permanent Fail:SOTF:Delay. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF A[SOTF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.9 Charge FET (CFETF) Permanent Fail

The BQ769142 device integrates a Charge FET (CFETF) Permanent Fail, which can permanently disable the pack if a charging current is measured that reaches or exceeds a programmable threshold for a programmable delay time while the charge FET is disabled. The threshold is set by ***Permanent Fail:CFETF:OFF Threshold***, and the delay is set by ***Permanent Fail:CFETF:OFF Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[CFETF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.10 Discharge FET (DFETF) Permanent Fail

The BQ769142 device integrates a Discharge FET (DFETF) Permanent Fail, which can permanently disable the pack if a discharge current is measured that reaches or exceeds a programmable threshold for a programmable delay time while the discharge FET is disabled. The threshold is set by ***Permanent Fail:DFETF:OFF Threshold***, and the delay is set by ***Permanent Fail:DFETF:OFF Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[DFETF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits. The value of ***Permanent Fail:DFETF:OFF Threshold*** should typically be a negative number.

5.3.11 Secondary Protector (2LVL) Permanent Fail

The BQ769142 device integrates a Secondary Protector (2LVL) Permanent Fail, which can permanently disable the pack if an external secondary protector has detected a fault and is attempting to blow the fuse. The BQ769142 device monitors the level of the FUSE pin each second (in NORMAL and SLEEP modes), and if it detects the pin is being asserted by the secondary protector for ***Permanent Fail:2LVL:Delay*** seconds, a 2LVL PF fault is generated. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[2LVL]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.12 Voltage Imbalance in Relax (VIMR) Permanent Fail

The BQ769142 device integrates a Voltage Imbalance in Relax (VIMR) Permanent Fail, which can permanently disable the pack if an excessive level of cell imbalance is detected while the pack is in a relax state, which is determined by the absolute value of measured current being less than ***Permanent Fail:VIMR:Max Relax Current***. The VIMR PF is only checked if the maximum cell voltage is above ***Permanent Fail:VIMR:Check Voltage*** and the absolute value of measured current is less than ***Permanent Fail:VIMR:Max Relax Current*** for a time duration of at least ***Permanent Fail:VIMR:Relax Min Duration***. This check will generate a PF fault when a cell imbalance (that is, the difference in the maximum and minimum cell voltages) is detected that meets or exceeds ***Permanent Fail:VIMR:Threshold*** for a time duration of ***Permanent Fail:VIMR:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[VIMR]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.13 Voltage Imbalance in Active (VIMA) Permanent Fail

The BQ769142 device integrates a Voltage Imbalance in Active (VIMA) Permanent Fail, which can permanently disable the pack if an excessive level of cell imbalance is detected while the pack is in a charging state, which is determined by the measured current meeting or exceeding ***Permanent Fail:VIMA:Min Active Current***. The VIMA PF is only checked if the maximum cell voltage is above ***Permanent Fail:VIMA:Check Voltage*** and the measured current is not less than ***Permanent Fail:VIMA:Min Active Current***. This check will generate a PF fault when a cell imbalance (that is, the difference in the maximum and minimum cell voltages) is detected that meets or exceeds ***Permanent Fail:VIMA:Threshold*** for a time duration of ***Permanent Fail:VIMA:Delay***. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[VIMA]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.14 Short Circuit in Discharge Latched Permanent Fail

The BQ769142 device integrates a Latched Short Circuit in Discharge (SCDL) Permanent Fail, which can permanently disable the pack if an SCDL protection fault occurs (which indicates multiple Short Circuit in Discharge (SCD) protection faults have detected within a programmable time window). The settings that control the SCDL fault are explained in Section 5.2.6. The SCDL Permanent Fail should only be enabled if the SCDL

protection fault is configured to not allow recovery. This PF check is enabled by setting the ***Settings:Permanent Failure:Enabled PF B[SCDL]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.15 OTP Memory Signature Permanent Fail

The BQ769142 device integrates a signature check on the OTP memory that will be checked when the device boots and loads data from OTP, but only if the OTP memory is not entirely empty (which is the default configuration). If the OTP memory signature check fails, the device will not load any settings from OTP, it will instead boot and load the default configuration, which keeps the FETs turned off (but it will not blow the fuse) and the REG1 LDO disabled. Note that the OTP signature does not include the Manufacturing Data (available using the *0x0070 MANU_DATA()* subcommand) nor any PF status data which was written to OTP (which is read using the *0x0053 SAVED_PF_STATUS()* subcommand).

The OTP PF (OTPF) is enabled by default. It can be disabled by clearing the ***Settings:Permanent Failure:Enabled PF C[OTPF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

Note: the device also includes a check on the trim information stored within the device during factory test. If an error is detected in this information during boot, the device will directly begin the SHUTDOWN sequence.

5.3.16 Data ROM Memory Signature Permanent Fail

The BQ769142 device integrates a signature check on the Data ROM, which contains default values for the Data Memory settings. This PF will be checked when the device loads data from the Data ROM, which occurs at initial powerup or device reset. The Data ROM PF (DRMF) can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[DRMF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

A data ROM signature can be calculated on demand by the host sending the *DROM_SIG()* subcommand. The signature returned by this subcommand can be compared to the expected value by the host processor, if periodic checks are required. The device only asserts the DRMF Permanent Fail when the signature check is performed at powerup or reset, it will not assert this if an incorrect signature is returned from the host manually sending the *DROM_SIG()* subcommand.

5.3.17 Instruction ROM Memory Signature Permanent Fail

The BQ769142 device integrates a signature check on the Instruction ROM, which contains internal controller program code. This PF will be checked at initial powerup or device reset. The Instruction ROM PF (IRMF) can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[IRMF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

An instruction ROM signature can be calculated on demand by the host sending the *IROM_SIG()* subcommand. The signature returned by this subcommand can be compared to the expected value by the host processor, if periodic checks are required. Note that the calculation of this signature takes approximately 9 ms, during which time the device will temporarily suspend ADC and coulomb counter measurements and will not respond to serial communications. The device only asserts the IRMF Permanent Fail when the signature check is performed at powerup or reset, it will not assert this if an incorrect signature is returned from the host manually sending the *IROM_SIG()* subcommand.

5.3.18 LFO Oscillator Permanent Fail

The BQ769142 device includes a separate hardware monitor circuit which determines if the LFO oscillator frequency deviates excessively from its expected value. If such a deviation is detected, the device can trigger an LFO Oscillator PF (LFOF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[LFOF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.19 Voltage Reference Permanent Fail

The BQ769142 device integrates a diagnostic check on the voltage references used by the device. VREF2 is used by the coulomb counter and LDOs, including the REG18 LDO. The REG18 LDO voltage is periodically measured using the voltage ADC (using VREF1 as its reference) and can be read back in bytes 0-1 of the *0x0075 DASTATUS5()* subcommand. This command should normally report a value of approximately 29137. If it differs significantly from this, it may indicate that one reference has changed in value significantly relative

to the other, meaning reported measurements may no longer be accurate. This ratio is monitored periodically and, if the value is below 26223 or above 32051 for four seconds, the device can trigger a VREF PF (VREF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[VREF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.20 VSS Permanent Fail

The BQ769142 device integrates a diagnostic check on the ADC input mux by periodically measuring the VSS voltage level using the voltage ADC. This measurement is reported in bytes 2-3 of the *0x0075 DASTATUS5()* subcommand and should normally report a value that is near zero. If it differs significantly from this, it may indicate the ADC input mux has experienced an error, meaning reported measurements may no longer be accurate. This measurement is monitored by the device and, if not as expected, can trigger a VSS PF (VSSF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[VSSF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits, and the fail threshold and delay are set by ***Permanent Fail:VSSF:Fail Threshold*** and ***Permanent Fail:VSSF:Delay***.

5.3.21 Protection Comparator MUX Permanent Fail

The BQ769142 device implements a periodic check on the input mux for the hardware protection comparator subsystem used for the OV, UV, OCC, OCD1, and OCD2 primary protections. If this check fails, it can trigger a Protection Comparator MUX Permanent Fail (HWMX) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[HWMX]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits.

5.3.22 Commanded Permanent Fail

The BQ769142 device includes the capability for the host to force a Permanent Fail by sending the *0x2857 PF_FORCE_A()* subcommand followed by the *0x29A3 PF_FORCE_B()* subcommand within 4 seconds. This PF is only allowed if the ***Settings:Permanent Failure:Enabled PF C[CMDF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits are set.

5.3.23 Top of Stack Measurement Check

The voltage ADC regularly measures the top of stack voltage through an internal divider and reports this in *0x34 Stack Voltage()*. It also compares this measurement to the sum of the individual cell voltage measurements and can trigger a Top of Stack PF (TOSF) and disable the battery pack if they differ excessively. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF D[TOSF]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits, and the fail threshold and delay are set by ***Permanent Fail:TOS:Threshold*** and ***Permanent Fail:TOSF:Delay***. This check is not performed if the current is beyond ***Power:Sleep:Sleep Current***, in order to avoid false triggers due to a dynamic load.

5.3.24 Cell Open Wire

The BQ769142 device supports detection of a broken connection between a cell in the pack and the cell attachment to the PCB containing BQ769142. Without this check, the voltage at the cell input pin of the BQ769142 device may persist for some time on the board-level capacitor, leading to incorrect voltage readings. The cell open wire detection in the BQ769142 device operates by enabling a small current source from each cell to VSS at programmable intervals. If a cell input pin is floating due to an open wire condition, this current will discharge the capacitance, causing the voltage at the pin to slowly drop. This drop in voltage will eventually trigger a cell undervoltage protection fault on that particular cell, as well as a cell overvoltage protection fault on the cell above it. Eventually, the voltage will drop low enough to trigger a safety undervoltage PF on the particular cell, or a safety overvoltage PF on the cell above it. It is important that the undervoltage and overvoltage protections and PFs be enabled with appropriate threshold settings for the open wire condition to be detected and the desired reaction initiated.

The cell open wire current will be enabled at a periodic interval set by the ***Settings:Cell Open-Wire:Check Time*** configuration register, with a setting of 0 disabling this check entirely. The current source is enabled once every interval for a duration of the ADC measurement time (which is 3 ms by default). This provides programmability in the average current drawn from ≈0.65 nA to ≈165 nA, based on the typical current level of 55 µA. After each ***Check Time*** interval completes, during the next measurement loop the cell open wire current

source is enabled on the cell above the cell being measured (with the current source enabled on the lowest cell while the topmost cell is being measured). This is scheduled to avoid the cell open wire current corrupting the cell voltage measurements. During SLEEP mode, the cell open wire current source is enabled in similar fashion during the next set of measurements that occur after the timer has expired.

Note

The cell open wire check can create a cell imbalance, so the settings should be selected appropriately.

6.1 *0x00 Control Status()* and *0x12 Battery Status()* Commands

The BQ769142 device includes *0x00 Control Status()* and *0x12 Battery Status()* commands, which report various status information on the pack. The *0x00 Control Status()* command behaves similarly to 0x3E and 0x3F when written, this functionality is included for legacy auto-detection and is not recommended for customer usage. When this command is read back immediately after it has been written, it will return 0xFFA5 once. Subsequent reads will return the *0x00 Control Status()* data, which is described below with the *0x12 Battery Status()* details.

Table 6-1. *0x00 Control Status()* Bit Definitions

Bit	Name	Description
15–3	RSVD	Reserved
2	DEEPSLEEP	This bit indicates whether or not the device is in DEEPSLEEP mode. DEEPSLEEP = 0: Device is not in DEEPSLEEP mode. DEEPSLEEP = 1: Device is in DEEPSLEEP mode.
1	LD_TIMEOUT	This bit is set when the Load Detect function has timed out and checking has stopped. LD_TIMEOUT = 0: Load Detect function has not timed out or is inactive. LD_TIMEOUT = 1: Load Detection function timed out and was deactivated.
0	LD_ON	This bit indicates whether or not the Load Detect pullup was active during the previous LD pin voltage measurement. LD_ON = 0: LD pullup was not active during the previous LD pin measurement. LD_ON = 1: LD pullup was active during the previous LD pin measurement.

Table 6-2. *0x12 Battery Status()* Bit Definitions

Bit	Name	Description
15	SLEEP	This bit indicates whether or not the device is presently in SLEEP mode. SLEEP = 0: Device is not in SLEEP mode. SLEEP = 1: Device is in SLEEP mode.
14	RSVD	Reserved
13	SDM	SHUTDOWN mode is pending because the *Shutdown()* subcommand was received, or the RST_SHUT pin was asserted for > 1-sec. SDM = 0: Shutdown due to command or pin is not pending. SDM = 1: Shutdown due to command or pin is pending.
12	PF	Indicates whether a Permanent Fail fault has triggered. PF = 0: No Permanent Fail fault has triggered. PF = 1: At least one Permanent Fail fault has triggered.
11	SS	Indicates whether an enabled safety fault has triggered SS = 0: No safety fault is triggered. SS = 1: At least one enabled safety fault is triggered.
10	FUSE	Reports the most recently observed state of the FUSE pin, is updated every second in NORMAL mode. FUSE = 0: FUSE pin was not asserted by device or secondary protector at last sample. FUSE = 1: FUSE pin was asserted by device or secondary protector at last sample.

Table 6-2. *0x12 Battery Status()* Bit Definitions (continued)

Bit	Name	Description
9	SEC1	SEC1:0 indicate the present security state of the device. SEC1:0 = 0: Device has not initialized yet. SEC1:0 = 1: Device is in FULLACCESS mode. SEC1:0 = 2: Device is in UNSEALED mode. SEC1:0 = 3: Device is in SEALED mode. When in SEALED mode, device configuration may not be read or written and some commands are restricted. When in UNSEALED mode, device configuration may normally be read and may be written while in CONFIG_UPDATE mode. When in FULLACCESS mode, unrestricted read and write access is allowed and all commands are accepted.
8	SEC0	
7	OTPB	This bit indicates whether or not voltage and temperature conditions are valid for OTP programming. During normal operation, this bit will always be set if *Manufacturing Status()[OTPW]* is clear. When entering CONFIG_UPDATE mode, conditions will be checked and this bit will reflect whether or not programming is allowed (*Manufacturing Status()[OTPW]* does not apply in CONFIG_UPDATE mode). Once in CONFIG_UPDATE mode, this bit will not change state since no new measurements are being taken. OTPB = 0: OTP writes are allowed. OTPB = 1: Writes to OTP are blocked.
6	OTPW	This bit indicates whether or not some data is waiting to be written to OTP during normal operation. This can occur when, for example, configured to Permanent Fail information to OTP. This bit may remain set until conditions for OTP programming are met and all data is programmed. This bit is not set during OTP programming from CONFIG_UPDATE mode. OTPW = 0: No writes to OTP are pending. OTPW = 1: Writes to OTP are pending.
5	COW_CHK	This bit indicates while cell open-wire checks are occurring. When the feature is disabled, this bit will not set. When the feature is enabled, this bit will set periodically as the checks are performed. COW_CHK = 0: Device is not actively performing a cell open-wire check. COW_CHK = 1: Device is actively performing a cell open-wire check.
4	WD	This bit indicates whether or not the previous device reset was caused by the internal watchdog timer. This is not related to the Host Watchdog protection. WD = 0: Previous reset was normal. WD = 1: Previous reset was caused by the watchdog timer.
3	POR	This bit is set when the device fully resets. It is cleared upon exit of CONFIG_UPDATE mode. It can be used by the host to determine if any RAM configuration changes were lost due to a reset. POR = 0: Full reset has not occurred since last exit of CONFIG_UPDATE mode. POR = 1: Full reset has occurred since last exit of CONFIG_UPDATE and reconfiguration of any RAM settings is required.
2	SLEEP_EN	This bit indicates whether or not SLEEP mode is allowed based on configuration and commands. The ***Settings:Configuration:Power Config[SLEEP_EN]*** bit sets the default state of this bit. The host may send commands to enable or disable SLEEP mode based on system requirements. When this bit is set, the device may transition to SLEEP mode when other SLEEP criteria are met. SLEEP_EN = 0: SLEEP mode is disabled by the host. SLEEP_EN = 1: SLEEP mode is allowed when other SLEEP conditions are met.
1	PCHG_MODE	This bit indicates whether or not the device is in PRECHARGE mode. In PRECHARGE mode, the PCHG FET is turned on instead of the CHG FET. PCHG_MODE = 0: Device is not in PRECHARGE mode. PCHG_MODE = 1: Device is in PRECHARGE mode.
0	CFGUPDATE	This bit indicates whether or not the device is in CONFIG_UPDATE mode. It will be set after the *0x0090 SET_CFGUPDATE()* subcommand is received and fully processed. Configuration settings may be changed only while this bit is set. CFGUPDATE = 0: Device is not in CONFIG_UPDATE mode. CFGUPDATE = 1: Device is in CONFIG_UPDATE mode.

6.2 *0x0070 MANU_DATA()* Subcommand

The BQ769142 device integrates a 32-byte scratchpad memory the customer can use to store manufacturing data, such as serial numbers, production or test dates, and so forth. The scratchpad data can be written into OTP memory on the customer production line. This data can only be written while in FULLACCESS mode, although it can be read in all modes. The data is read or written using the *0x0070 MANU_DATA()* subcommand.

When written, the data is first updated in RAM. If the ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** configuration bit is set, the device then attempts to write the data to OTP when CONFIG_UPDATE mode is

exited or at the completion of the *MANU_DATA()* subcommand, if it was sent while outside of CONFIG_UPDATE mode. The device only writes OTP if the BAT voltage is above the minimum allowed voltage level (the voltage can be above the maximum data sheet value in this case) and the temperature is within the allowed temperature range, as specified in the device data sheet. If conditions do not allow, the write to OTP remains pending and completes when conditions become acceptable.

The restrictions on how bits can be changed using the *MANU_DATA()* subcommand are described below:

- Outside CONFIG_UPDATE mode:
  - Bits can be changed from '0' to '1' or left unchanged.
- In CONFIG_UPDATE mode:
  - Bits can be changed from '0' to '1' or left unchanged.
  - If a bit is still '0' in OTP, it can be changed from '1' to '0'.
  - If a bit has been set in OTP, it cannot be changed from '1' to '0'.

6.3 LDOs

The BQ769142 device contains an integrated 1.8 V LDO (REG18) that provides a regulated 1.8 V supply voltage for the device's internal circuitry and digital logic. This regulator uses an external capacitor connected to the REG18 pin, and it should only be used for internal circuitry.

The device also integrates two separately programmable LDOs (REG1 and REG2) for external circuitry, such as a host processor or external transceiver circuitry, which can be programmed to independent output voltages. The REG1 and REG2 LDOs take their input from the REGIN pin, with this voltage either provided externally or generated by an on-chip pre-regulator (referred to as REG0). The REG1 and REG2 LDOs can provide an output current of up to 45 mA each.

6.3.1 Preregulator Control

The REG1 and REG2 LDOs take their input from the REGIN pin, which should be approximately 5.5 V. This REGIN pin voltage can be supplied externally (such as by a separate DC/DC converter) or using the integrated voltage preregulator (referring to as REG0), which drives the base of an external NPN BJT (using the BREG pin) to provide the 5.5-V REGIN pin voltage. When the preregulator is being used, special care should be taken to ensure the device retains sufficient voltage on its BAT pin, per the device electrical specifications.

The preregulator is only powered if ***Settings:Configuration:REG0 Config[REG0_EN]*** is set, as well as if one of ***Settings:Configuration:REG12 Config[REG1_EN]*** or ***Settings:Configuration:REG12 Config[REG2_EN]*** is set; otherwise, the device does not enable the preregulator.

If neither REG1 nor REG2 will be used in the system, or if the REGIN voltage will be supplied externally, then the ***Settings:Configuration:REG0 Config[REG0_EN]*** configuration bit should be cleared.

Note

There is a diode connection between the REGIN pin (anode) and the BAT pin (cathode), so the voltage on REGIN should not exceed the voltage on BAT.

6.3.2 REG1 and REG2 LDO Controls

The REG1 and REG2 LDOs in the BQ769142 device are for customer use, and their output voltages can be programmed independently to 1.8 V, 2.5 V, 3.0 V, 3.3 V, or 5.0 V. The voltage levels are selected using the ***Settings:Configuration:REG12 Config[REG1V_2:REG1V_0]*** and ***Settings:Configuration:REG12 Config[REG2V_2:REG2V_0]*** configuration bits as shown below. The LDOs are enabled using the ***Settings:Configuration:REG12 Config[REG1_EN]*** and ***Settings:Configuration:REG12 Config[REG2_EN]*** configuration bits, and their settings can be modified during operation using the *0x0098 REG12_CONTROL()* subcommand. This subcommand takes an 8-bit value that matches the bits in the ***Settings:Configuration:REG12 Config*** configuration register. It is important that the voltage selection not be changed in CONFIG_UPDATE mode while the LDO is enabled.

Table 6-3. REG1 and REG2 LDO Voltage Settings

REG1V_2:0, REG2V_2:0	REG1, REG2 Voltage (V)
0x0–0x3	1.8
0x4	2.5
0x5	3.0
0x6	3.3
0x7	5.0

The REG1 and REG2 LDOs and the REG0 pre-regulator are disabled by default in the BQ769142 device, with the REG1 and REG2 pulled to VSS with an internal resistance of ≈2.5-kΩ. If the pull-up resistors for the serial communications are connected to the REG1 voltage output, the REG1 voltage can be overdriven from an external voltage supply on the manufacturing line, to allow communications with the device. The BQ769142 device can then be programmed to enable REG0 and REG1 with the desired configuration, and this setting can be programmed into OTP memory. Thus, at each later powerup, the device will autonomously load the OTP settings and enable the LDO as configured, without requiring communications first.

6.4 Multifunction Pin Controls

The BQ769142 device provides flexibility regarding the multifunction pins on the device, which includes the TS1, TS2, TS3, CFETOFF, DFETOFF, ALERT, HDQ, DCHG, and DDSG pins. Several of the pins can be used as active-high outputs with configurable output level. The digital output driver for these pins can be configured to drive an output powered from the REG1 LDO or from the internal REG18 LDO, and thus when asserted active-high will drive out the voltage of the selected LDO.

Note: the REG18 LDO is not capable of driving high current levels, so it is recommended to only use this LDO to provide a digital output if it will be driving a very high resistance (such as > 1 MΩ) or light capacitive load. Otherwise the REG1 should be powered and used to drive the output signal.

The options supported on each pin include:

ALERT

Alarm interrupt output. It can be configured as follows:

Hi-Z when no alarm is triggered, versus driven low when triggered.

Driven high when no alarm is triggered, versus driven low when triggered.

Driven low when no alarm is triggered, versus driven high when triggered.

HDQ communications

Can be used for HDQ communications with a host processor.

CFETOFF

Input to control the CHG FET (that is, CFETOFF functionality). It can be configured as follows:

A high input forces the CHG FET off, a low input allows the CHG FET to be turned on (by host or device itself).

A low input forces the CHG FET off, a high input allows the CHG FET to be turned on (by host or device itself).

DFETOFF

Input to control the DSG FET (that is, DFETOFF functionality). It can be configured as follows:

A high input forces the DSG FET off, a low input allows the DSG FET to be turned on (by host or device itself).

A low input forces the DSG FET off, a high input allows the DSG FET to be turned on (by host or device itself).

Input to control both the DSG and CHG FETs (that is, BOTHOFF functionality). It can be configured as follows:

A high input forces both FETs off, a low input allows the FETs to be turned on (by host or device itself).

A low input forces both FETs off, a high input allows the FETs to be turned on (by host or device itself).

HDQ

HDQ communications

Can be used for HDQ communications with a host processor

SPI MOSI pin

MOSI pin for SPI communications

DCHG

DCHG functionality

A logic-level output corresponding to a fault, which would normally cause the CHG driver to be disabled.

DDSG

DDSG functionality

A logic-level output corresponding to a fault, which would normally cause the DSG driver to be disabled.

ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG

General purpose digital output

Can be driven high or low by command

Can be configured for an active-high output to be driven from the REG1 LDO or the REG18 LDO

Can be configured to have a weak pull-down to VSS or weak pull-up to REG1 enabled continuously

ALERT, CFETOFF, DFETOFF, TS1, TS2, TS3, HDQ, DCHG, and DDSG

Thermistor temperature measurement

A thermistor can be attached between the pin and VSS.

ADCIN

Pin can be used for general purpose ADC measurement.

These pin configurations are controlled by the ***Settings:Configuration:ALERT Pin Config, CFETOFF Pin Config, DFETOFF Pin Config, TS1 Config, TS2 Config, TS3 Config, HDQ Pin Config, DCHG Pin Config, and DDSG Pin Config*** configuration registers. The [PIN_FXN1:0] bits in each configuration register determine how the pin will be used:

Table 6-4. Multifunction Pin Function Controls

PIN_FXN1	PIN_FXN0	Pin Function
0	0	Pin is used for communications, or not used at all.
0	1	General purpose digital output (GPO)
1	0	Alternate function (ALT)
1	1	Thermistor measurement or general purpose ADC input (AD)

The ALT (Alternate function) setting refers to special functions that are only available on particular pins. The alternate functions available for pins are:

Pin	ALT (Alternate Function)
ALERT	Alarm interrupt output
CFETOFF	CFETOFF functionality (CHG and PCHG FET control)
DFETOFF	DFETOFF functionality (DSG and PDSG FET control)
	BOTHOFF functionality (combined CHG and PCHG, and DSG and PDSG FET control)
DCHG	DCHG functionality (logic-level protection signal)

Pin	ALT (Alternate Function)
DDSG	DDSG functionality (logic-level protection signal)

Each pin configuration register includes ***[OPT5:0]*** bits which set the operation of the pin. When a pin is configured for ALT or GPO, these bits are used as shown below.

Table 6-5. Multifunction Pin Options for ALT or GPO Pins

Bit	Function
OPT[5]	Polarity for ALERT, CFETOFF, DFETOFF. HDQ, DCHG, and DDSG pins only. 0: selects active-high. 1: selects active-low.
OPT[4]	Only used for DFETOFF pin. 0: selects ALT = DFETOFF. 1: selects ALT = BOTHOFF.
OPT[3]	GPO drive level for ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins only. 0: output high drive uses REG18. 1: output high drive uses REG1.
OPT[2]	GPO weak pull-up control for ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins only. 0: weak pull-up to REG1 is disabled. 1: weak pull-up to REG1 is enabled. NOTE–this should only be selected if OPT[3] = 0 and OPT[1] = 0:
OPT[1]	GPO drive mode for ALERT, CFETOFF, DFETOFF, HDQ, DCHG, and DDSG pins only. 0: pin drives tri-state when controlled to be driven "high." 1: pin drives active-high when controlled to be driven "high."
OPT[0]	GPO weak pulldown control for ALERT, CFETOFF, DFETOFF, HDQ, DCHG, DDSG pins only. 0: weak pulldown to VSS is disabled. 1: weak pulldown to VSS is enabled.

When a pin is selected for thermistor or ADCIN functionality, the ***OPT[5:0]*** bits are used as shown below.

Table 6-6. Multifunction Pin Options for Thermistor or ADCIN Pins

Bit	Function
OPT[5:4]	Pull-up control 00: selects 18 kΩ pull-up for thermistor measurement 01: selects 180 kΩ pull-up for thermistor measurement 10: selects no pull-up (used for ADCIN)
OPT[3:2]	Polynomial selection for thermistor temperature measurement 00: selects ***Calibration:18K Temperature Model*** 01: selects ***Calibration:180K Temperature Model*** 10: selects ***Calibration:Custom Temperature Model*** 11: no polynomial is used, raw ADC counts are reported.
OPT[1:0]	Measurement type 00: general purpose ADC input 01: thermistor temperature measurement, used for cell temperature protections 10: thermistor temperature measurement, reported but not used for protections 11: thermistor temperature measurement, used for FET temperature protection

When a pin is configured for use as a general purpose digital output, its output state can be controlled by the subcommands shown below.

Table 6-7. General Purpose Digital Output Control Subcommands

Subcommand	Description
0x2800 CFETOFF_LO()	If the CFETOFF pin is configured as a GPO, this subcommand sets it to drive a low output.
0x2801 DFETOFF_LO()	If the DFETOFF pin is configured as a GPO, this subcommand sets it to drive a low output.
0x2802 ALERT_LO()	If the ALERT pin is configured as a GPO, this subcommand sets it to drive a low output.
0x2806 HDQ_LO()	If the HDQ pin is configured as a GPO, this subcommand sets it to drive a low output.
0x2807 DCHG_LO()	If the DCHG pin is configured as a GPO, this subcommand sets it to drive a low output.

Table 6-7. General Purpose Digital Output Control Subcommands (continued)

Subcommand	Description
0x2808 DDSG_LO()	If the DDSG pin is configured as a GPO, this subcommand sets it to drive a low output.
0x2810 CFETOFF_HI()	If the CFETOFF pin is configured as a GPO, this subcommand sets it to drive a high output.
0x2811 DFETOFF_HI()	If the DFETOFF pin is configured as a GPO, this subcommand sets it to drive a high output.
0x2812 ALERT_HI()	If the ALERT pin is configured as a GPO, this subcommand sets it to drive a high output.
0x2816 HDQ_HI()	If the HDQ pin is configured as a GPO, this subcommand sets it to drive a high output.
0x2817 DCHG_HI()	If the DCHG pin is configured as a GPO, this subcommand sets it to drive a high output.
0x2818 DDSG_HI()	If the DDSG pin is configured as a GPO, this subcommand sets it to drive a high output.

6.5 CFETOFF, DFETOFF, and BOTHOFF Pin Functionality

The BQ769142 device includes two pins (CFETOFF and DFETOFF) which can be used to disable the protection FET drivers quickly, without going through the host serial communications interface. When the selected pin is asserted, the device disables the respective protection FET. Note: when the selected pin is deasserted, the respective FET will only be enabled if there are no other items blocking them being reenabled, such as if the host also sent a *0x0097 FET_CONTROL()* subcommand to disable the FETs using the serial communications interface after setting the selected pin. Both the CFETOFF and DFETOFF pins can be used for other functions if the FET turnoff feature is not required.

The CFETOFF pin can optionally be used to disable the CHG and PCHG FETs, and the DFETOFF pin can optionally be used to disable the DSG and PDSG FETs. The device also includes the option to configure the DFETOFF pin as BOTHOFF functionality, such that if that pin is asserted, the CHG, PCHG, DSG, and PDSG FETs will be disabled. This allows the CFETOFF pin to be used for an additional thermistor in the system, while still providing pin control to disable the FETs.

The CFETOFF or BOTHOFF functionality disables both the CHG FET and the PCHG FET when asserted.

The DFETOFF or BOTHOFF functionality disables both the DSG FET and the PDSG FET when asserted.

6.6 ALERT Pin Operation

The ALERT pin is a multifunction pin that can be configured either as ALERT (to provide an interrupt to a host processor), a thermistor input, a general purpose ADC input, a general purpose digital output, or an HDQ serial communication interface. The pin can be configured as active-high, active-low, or open-drain, to accommodate different system design preferences. When configured as the HDQ interface pin, the pin will operate in open-drain mode.

When the pin is configured to drive an active high output, the output voltage is driven from either the REG18 1.8 V LDO or the REG1 LDO (which can be programmed from 1.8 V to 5.0 V). Note: if a DC or significant transient current may be driven by this pin, then the output should be configured to drive using the REG1 LDO, not the REG18 LDO.

The BQ769142 device includes functionality to generate an alarm signal at the ALERT pin, which can be used as an interrupt to a host processor. This functionality is optional, it can be enabled by setting the ***Settings:Configuration:ALERT Pin Config[PIN_FXN1:0]*** = 0b10. When used for the alarm function, the pin can be programmed to drive the signal as an active-low or hi-Z signal, an active-high or low signal, or an active-low or high signal (that is, inverted polarity). The alarm function within the BQ769142 device includes a programmable mask, to allow the customer to decide which of many flags or events can trigger an alarm. The *0x64 Alarm Raw Status()* command provides the present (unlatched) value of the bits described below:

Table 6-8. *Alarm Raw Status()* Bit Definitions

Bit	Name	Description
15	SSBC	Safety Status—Set if a bit in *Safety Status B–C()* is set.
14	SSA	Hardware Safety Status—Set if a bit in *Safety Status A()* is set.
13	PF	Permanent Fail Status—Set if a bit in *PF Status A–D()* is set.

Table 6-8. *Alarm Raw Status()* Bit Definitions (continued)

Bit	Name	Description
12	MSK_SFALERT	Masked Safety Alerts—Set if a bit in *Safety Alert A–C()* is set and the corresponding bit in ***Settings:Alarm:SF Alert Mask A–C*** is set.
11	MSK_PFALERT	Masked Permanent Fail Alerts—Set if a bit in *PF Alert A–D()* is set and the corresponding bit in ***Settings:Alarm:PF Alert Mask A–D*** is set.
10	INITSTART	Initialization started (sets quickly after device powers up)
9	INITCOMP	Initialization completed (sets after device has powered and completed one measurement scan)
8	RSVD	Reserved
7	FULLSCAN	Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltage measurement loop data (including cell voltages, pin or thermistor voltages, and so forth). This bit sets after the first full scan completes, then remains set.
6	XCHG	CHG FET is off.
5	XDSG	DSG FET is off.
4	SHUTV	Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage***.
3	FUSE	FUSE Pin Driven. The FUSE pin is being driven by either the BQ769142 device or the secondary protector.
2	CB	Cell balancing is active
1	ADSCAN	Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets after the first ADC scan completes, then remains set.
0	WAKE	Wake. Device is wakened from SLEEP mode.

The bits in *0x64 Alarm Raw Status()* can be selected to be latched and included in the alarm interrupt output based on mask registers.

Note

The bits in *0x64 Alarm Raw Status()* are not latched, so they may set only briefly.

When a masked flag transitions from low to high, it latches a corresponding bit in *0x62 Alarm Status()*. The [ADSCAN] and [FULLSCAN] bits are exceptions. They will be latched in *0x62 Alarm Status()* when scans complete if masked, even though the corresponding bits in *0x64 Alarm Raw Status()* do not toggle.

The masking is determined if the corresponding mask bit is set in the ***Settings:Alarm:Default Alarm Mask***, ***Settings:Alarm:SF Alert Mask A–C***, and ***Settings:Alarm:PF Alert Mask A–D*** configuration registers. The host can poll *0x62 Alarm Status()*, or use the alarm interrupt signal (the OR of all bits in *0x62 Alarm Status()*) mapped to the ALERT pin.

When bits are latched into *0x62 Alarm Status()*, the host can read the status and clear those latched bits by writing the *0x62 Alarm Status()* command with a '1' in one or more of the bits to be cleared, and '0s' in all other bits (which leaves the other bits unchanged). This prevents unintentional clearing of any additional *0x62 Alarm Status()* bits that may have been set just before the clearing signal was sent from the host processor.

The *0x66 Alarm Enable()* command can be read to see the present mask applied to the *0x64 Alarm Raw Status()* bits. The *0x66 Alarm Enable()* command can also be written by the host to change the masking during operation.

The status of the ALERT pin is provided in the *0x7F FET Status()[ALRT_PIN]* register bit.

6.7 DDSG and DCHG Pin Operation

The BQ769142 device includes two multifunction pins, DDSG and DCHG, which can be configured as logic-level outputs to provide a fault-related signal to a host processor or external circuitry (that is, DDSG and DCHG functionality), as a thermistor input, a general purpose ADC input, or a general purpose digital output.

When used as a digital output, the pins can be configured to drive an active high output, with the output voltage driven from either the REG18 1.8 V LDO or the REG1 LDO (which can be programmed from 1.8 V to 5.0 V). Note: if a DC or significant transient current may be driven by a pin, then the output should be configured to drive using the REG1 LDO, not the REG18 LDO.

When the pins are configured for DDSG and DCHG functionality, they provide signals related to protection faults that (on the DCHG pin) would normally cause the CHG driver to be disabled, or (on the DDSG pin) would normally cause the DSG driver to be disabled. These signals can be used to control external protection circuitry, if the integrated high-side NFET drivers will not be used in the system. They can also be used as interrupts in manual FET control mode for the host processor to decide whether to disable the FETs using the CFETOFF and DFETOFF pins.

For example, if the DDSG pin is configured for DDSG functionality, and the Cell Overvoltage (COV) protection is enabled, the DDSG pin will be deasserted while there is no fault present. When a COV fault occurs, the DDSG pin will be asserted. When the device recovers from the COV fault, the DDSG pin will be deasserted. The polarity of the drive signal on the pin is also programmable.

When the DDSG and DCHG pins are configured for DDSG and DCHG functionality, they will assert or deassert as described above during NORMAL, SLEEP, and DEEPSLEEP modes of operation. The pins will be high-impedance while the device is in SHUTDOWN mode.

6.8 Fuse Drive

The FUSE pin on the BQ769142 device can be used to blow a chemical fuse in the presence of a Permanent Fail (PF), as well as to detect if an external secondary protector in the system has detected a fault and is attempting to blow the fuse itself. The pin is intended to drive the gate of an NFET, which can be combined with the drive from an external secondary protector, as shown in Figure 6-1. When the FUSE pin is not being asserted by the BQ769142 device, it remains in a high-impedance state and will detect a voltage applied at the pin by a secondary protector. If the Second Level Protector PF is enabled (using the ***Settings:Permanent Failure:Enabled PF B[2LVL]*** and ***Settings:Manufacturing:Mfg Status Init[PF_EN]*** configuration bits), a PF will be generated if the device detects a high signal at the FUSE pin.

The device can be configured to blow the fuse when a PF occurs by setting the ***Settings:Protection:Protection Configuration[PF_FUSE]*** configuration bit. If this is set, the device will only attempt to blow the fuse if the stack voltage is above a threshold given by ***Settings:Fuse:Min Blow Fuse Voltage***, based on a system configuration with the fuse placed between the top of stack and the high-side protection FETs. If instead the fuse is placed between the FETs and the PACK+ connector, then the ***Settings:Protection:Protection Configuration[PACK_FUSE]*** bit should be set, and the device will instead base its decision on the PACK Pin Voltage. This voltage threshold check will be disregarded if a FET Failure PF (CFETF or DFETF) has occurred and the ***Settings:Protection:Protection Configuration[FETF_FUSE]*** bit is set.

When the FUSE pin is asserted to blow the external fuse, it will only stay asserted for a length of time set by the ***Settings:Fuse:Fuse Blow Timeout*** configuration register.

The status of the FUSE pin is provided in the *0x12 Battery Status[FUSE]* bit.

The *0x001D FUSE_TOGGLE()* subcommand can be used to toggle the state of the FUSE pin drive.

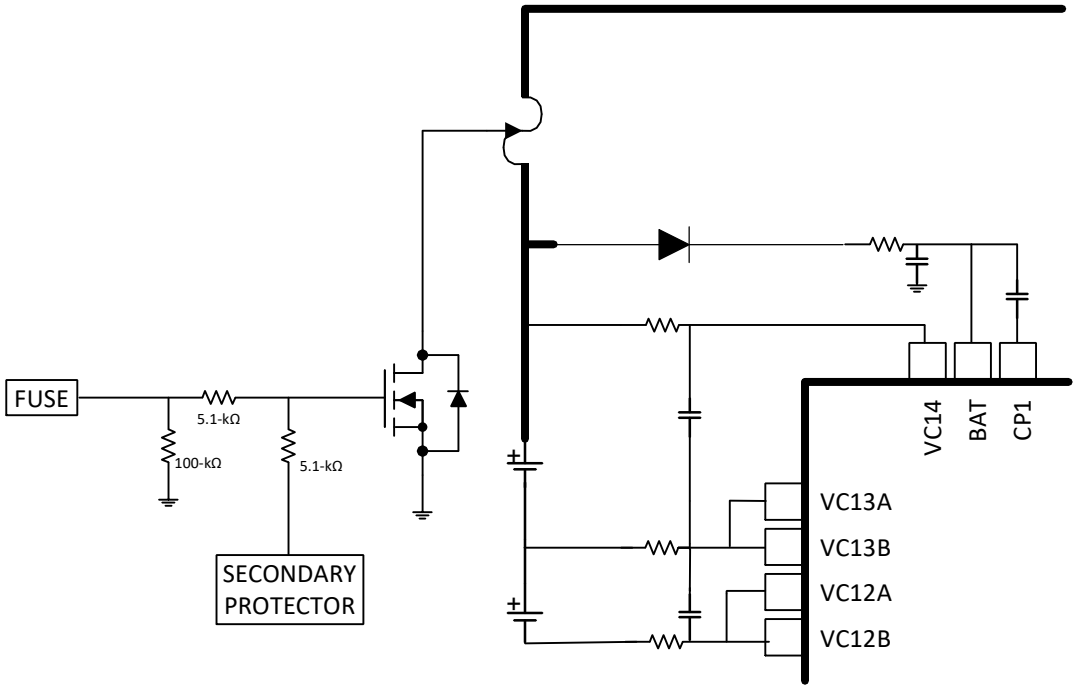


Figure 6-1. FUSE Pin Operation

6.9 Device Event Timing

The timing of events in the BQ769142 device varies based on the specific event. Several events and their associated timing are described below. Timings described below do not include the delays related to individual protections, as described in their respective sections.

Table 6-9. Timing of Events

Event Description	Timing
Alarm Status()[SSA] asserted, ALERT pin asserted due to *Alarm Status()[SSA]*.	Fast response, in NORMAL or SLEEP modes
Data (including cell voltages and *CC2 Current()*) calculated after measurements complete (except for temperature calculations based on thermistor voltage measurements).	Fast response, in NORMAL or SLEEP modes
FET turn-off based on enabled protection fault, with ***Settings:Protection:CHG FET Protections A*** set to 0x98 or 0x18, and ***Settings:Protection:DSG FET Protections A*** set to 0x80 or 0xE4.	Fast response, in NORMAL or SLEEP modes
CHG FET turn-on, and DSG FET changing from source follower mode to charge pump mode, based on current wake detector triggered while in SLEEP mode.	Fast response, in SLEEP mode
FET turn-off based on enabled protection fault, with ***Settings:Protection:CHG FET Protections A*** not set to 0x98 or 0x18, and ***Settings:Protection:DSG FET Protections A*** not set to 0x80 or 0xE4.	Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode
FET turn-on based on a pin (such as CFETOFF or DFETOFF deasserted) or command (such as *ALL_FETS_ON()* sent), while ***Settings:Manufacturing:Mfg Status Init[FET_EN]*** is set.	Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode
Evaluation if SHUTDOWN mode should be entered (due to RST_SHUT held high, temperature beyond ***Power:Shutdown:Shutdown Temperature***, or stack voltage below ***Power:Shutdown:Shutdown Stack Voltage***,	Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode
CC1 Current() is calculated	Evaluated every 250 ms in NORMAL mode, or every 4 second in SLEEP mode
Minimum, maximum, and average voltages calculated	Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode
Temperatures calculated based on measured thermistor voltages	Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode
PRECHARGE mode updated	Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode

Table 6-9. Timing of Events (continued)

Event Description	Timing
Alarm Status() other than *[SSA]* is updated, and ALERT pin asserted accordingly	Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode
Evaluate whether OTP programming can proceed, in response to Permanent Failure status needing to be written, or *MANU_DATA()* write subcommand sent.	Evaluated every 250 ms in NORMAL mode, or every 1 second in SLEEP mode
Firmware safety checks (such as OCD3, temperature protections) and protection recovery checks	Evaluated every 1 second in NORMAL or SLEEP modes
Firmware Permanent Failure checks	Evaluated every 1 second in NORMAL or SLEEP modes
Evaluating entering or exiting SLEEP mode. This is separate from the FETs changing state when current is detected in SLEEP mode (fast response, as described above). When exiting SLEEP mode, this refers to the NORMAL mode measurement loop resuming.	Evaluated every 1 second in NORMAL or SLEEP modes
Cell balancing (to determine if autonomous cell balancing should begin)	Evaluated every 1 second in NORMAL or SLEEP modes (limited in SLEEP by data available every ***Power:Sleep:Voltage Time*** interval)
Cell balancing (to determine if active autonomous cell balancing should continue)	Evaluated every ***Settings:Cell Balancing:Cell Balance Interval*** in NORMAL or SLEEP modes (limited in SLEEP by data available every ***Power:Sleep:Voltage Time*** interval)
RAM integrity check	Evaluated every 1 second in NORMAL or SLEEP modes
Internal watchdog timer	Generates a reset if firmware does not respond every 2 seconds in NORMAL and SLEEP modes, and in DEEPSLEEP mode when the LFO is operating

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7.1 Overview

The BQ769142 device has four operational modes to support optimized features and power dissipation, with the device able to transition between modes either autonomously or controlled by a host processor.

- NORMAL mode: In this mode, the device performs frequent measurements of system current, cell voltages, internal and thermistor temperatures, and various other voltages, operates protections as configured, and provides data and status updates.
- SLEEP mode: In this mode, the DSG FET is enabled, the CHG FET can optionally be disabled, and the device performs measurements, calculations, and data updates in adjustable time intervals. Battery protections are still enabled. Between the measurement intervals, the device is operating in a reduced power stage to minimize total average current consumption.
- DEEPSLEEP mode: In this mode, the CHG, PCHG, DSG, and PDSG FETs are disabled, all battery protections are disabled, and no current or voltage measurements are taken. The REG1 and REG2 LDOs can be kept powered, in order to maintain power to external circuitry, such as a host processor.
- SHUTDOWN mode: The device is completely disabled (including the internal, REG1, and REG2 LDOs), the CHG, PCHG, DSG, and PDSG FETs are all disabled, all battery protections are disabled, and no measurements are taken. This is the lowest power state of the device, which may be used for shipment or long-term storage. All register settings are lost when in SHUTDOWN mode.

The device also includes a CONFIG_UPDATE mode, which is used for parameter updates. Figure 7-1 shows the transitions between operational modes.

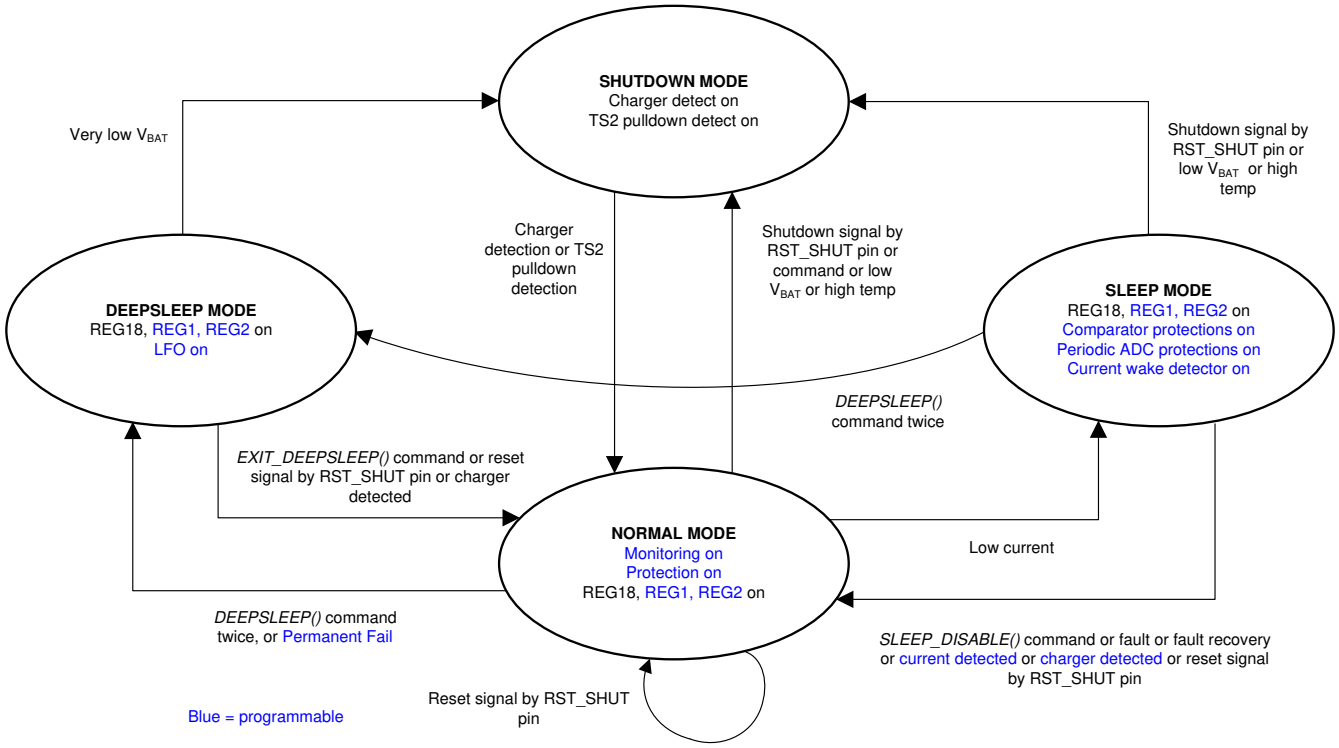

Figure 7-1. Operational Modes

7.2 NORMAL Mode

NORMAL mode is the highest performance mode of the device, in which the device is making regular measurement of voltage, current, and temperature, the LFO (low frequency oscillator) is operating, and the internal processor powers up (as needed) for data processing and control. Full battery protections are operating, based on device configuration settings. System current is measured at intervals of 3 ms, with cell voltages measured at intervals of 63 ms or slower, depending on configuration. If the ***[FASTADC]*** configuration bit is set, the conversion speed for both voltages and currents is doubled, with a reduction in measurement resolution.

The device will generally be in NORMAL mode whenever any active charging or discharging is underway. When the CC1 Current measurement falls below a SLEEP current threshold given by ***Power:Sleep:Sleep Current***, the system is considered in RELAX mode, and the BQ769142 device can autonomously transition into SLEEP mode, depending on the configuration.

7.3 SLEEP Mode

SLEEP mode is a reduced functionality state that can be optionally used to reduce power dissipation when there is little or no system load current or charging in progress, but still provides voltage at the battery pack terminals to keep the system alive. At initial power up, the ***Settings:Configuration:Power Config[SLEEP]*** configuration bit determines whether the device can enter SLEEP mode. After initialization, SLEEP mode can be allowed or disallowed using the *0x0099 SLEEP_ENABLE()* and *0x009A SLEEP_DISABLE()* subcommands. The *0x12 Battery Status()[SLEEP_EN]* bit indicates whether the device is presently allowed to enter SLEEP mode or not, while the *0x12 Battery Status()[SLEEP]* bit indicates whether it is presently in SLEEP mode or not.

When the magnitude of the CC1 Current measurement falls below a current threshold given by ***Power:Sleep:Sleep Current***, the system is considered in RELAX mode, and the BQ769142 device will autonomously transition into SLEEP mode, if settings permit. During SLEEP mode, comparator-based protections operate the same as during NORMAL mode. ADC-based current, voltage, and temperature measurements are taken every ***Power:Sleep:Voltage Time*** seconds. While in SLEEP mode, the device begins a 4-s current measurement 1 s after completing voltage and temperature measurements, therefore it is recommended to set this parameter to 5 s or (4 × n + 1) seconds. All temperature protections use the ADC

measurements taken at the ***Power:Sleep:Voltage Time*** intervals, so they will update at a reduced rate during SLEEP mode.

The BQ769142 device will exit SLEEP mode if a protection fault occurs, or current begins flowing, or a charger is attached, or the *0x009A SLEEP_DISABLE()* subcommand is sent, or if the RST_SHUT pin is asserted for < 1 s. When exiting based on current flow, the device will quickly enable the FETs (if the CHG FET was off, or the DSG FET was in source follower mode), but the standard measurement loop is not restarted until the next 1-s boundary occurs within the device timing. Therefore, new data may not be available for up to ≈1-s after the device exits SLEEP mode.

The coulomb counter ADC operates in a reduced power and speed mode to monitor current during SLEEP mode. The current is measured every 12 ms and, if it exceeds ***Power:Sleep:Wake Comparator Current*** in magnitude, the device quickly transitions back to NORMAL mode. In addition to this check, if the 4-s current measurement taken at each ***Power:Sleep:Voltage Time*** interval exceeds ***Power:Sleep:Sleep Current***, the device will exit SLEEP mode.

The rate at which the coulomb counter ADC operates in this WAKE COMPARATOR mode is programmable using the ***Settings:Configuration:Power Config[WK_SPD_1:0]*** configuration bits. These bits were originally designated reserved, with the bits denoted RSVD_1 and RSVD_0 in BQSTUDIO. By changing the conversion rate, the noise level of the resulting ADC conversions is also modified, with higher noise levels at faster conversion rates. The tables below summarize the bit name changes and settings.

Table 7-1. *Settings:Configuration:Power Config[WK_SPD_1:0]* Bit Names

Bit	Previous Bit Name	New Bit Name
1	RSVD_1	WK_SPD_1
0	RSVD_0	WK_SPD_0

Table 7-2. Wake Comparator Speed Settings

WK_SPD_1	WK_SPD_0	Current Measurement Speed	Measurement Noise Level (One Sigma)(1)	Comment
0	0	48 ms	≈6 µV	Recommended option for best accuracy
0	1	24 ms	≈10 µV	
1	0	12 ms	≈25 µV	Not recommended
1	1	6 ms	≈100 µV	Recommend only when used with thresholds > 1000 µV

(1) The coulomb counter digitizes the differential voltage between the SRP and SRN pins on the device. This measurement is converted to a current value for comparison with the ***Wake Comparator Current*** threshold value. The measurement noise of the ADC is described here as the equivalent voltage measured between the SRP and SRN pins. The approximate noise current can be calculated by dividing this noise voltage level by the value of the sense resistor used in the system.

The setting ***WK_SPD[1:0]*** = 0x0 provides the lowest noise level, with measurements exhibiting a sigma of approximately 6 µV, and a measurement taken every 48 ms. If a faster measurement rate is desired, then the setting 0x1 results in a sigma of approximately 10 µV and a measurement taken every 24 ms. If an even faster measurement rate is needed, the setting 0x3 can be used to provide a measurement every 6 ms. However, the sigma of this measurement is approximately 100 µV, which can result in unintentional wakeup from SLEEP mode if the threshold is set too low. For this reason, this setting is recommended only for use if the ***Power:Sleep:Wake Comparator Current*** is set so that the differential voltage $|V_{SRP} – V_{SRN}|$ > 1000 µV. Note that a six-sigma excursion using the 0x3 setting can cause a wakeup with a current approximately 600µV below the programmed threshold. The setting 0x2 (which is the default setting) may exhibit a large offset level and should not be used.

The device also monitors the PACK pin voltage and the top-of-stack voltage at each ***Power:Sleep:Voltage Time*** measurement interval. If the PACK pin voltage is higher than the top-of-stack voltage by more than ***Power:Sleep:Sleep Charger PACK-TOS Delta*** and the top-of-stack voltage is less than ***Power:Sleep:Sleep Charger Voltage Threshold***, the device will exit SLEEP mode. The BQ769142 device also includes a hysteresis on the SLEEP mode entrance, in order to avoid the device quickly entering and exiting SLEEP mode

based on a dynamic load. After transitioning to NORMAL mode, the device will not enter SLEEP mode again for a number of seconds given by the ***Power:Sleep:Sleep Hysteresis Time*** setting.

During SLEEP mode, the DSG FET can be driven either using the charge pump or in source-follower mode, as described in *High-Side NFET Drivers*. The CHG FET can be disabled or driven using the charge pump, based on the setting of ***Settings:FET:FET Options[SLEEPCHG]***.

7.4 DEEPSLEEP Mode

The BQ769142 device integrates a DEEPSLEEP mode, which is a low power mode that allows the REG1 and REG2 LDOs to remain powered, but disables other subsystems. In this mode, the protection FETs are all disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, and all voltage, current, and temperature measurements are disabled.

DEEPSLEEP mode can be entered by sending the *0x000F DEEPSLEEP()* subcommand twice in a row within a 4-sec time window. The device will exit DEEPSLEEP mode and return to NORMAL mode if the *0x000E EXIT_DEEPSLEEP()* subcommand is sent, or if the RST_SHUT pin is asserted for < 1 s, or if a charger is attached (which is detected by the voltage on the LD pin rising from below $V_{WAKEONLD}$ to exceed it). In addition, if the BAT pin voltage falls below V_{PORA}–V_{PORA_HYS}, the device transitions to SHUTDOWN mode.

When the device exits DEEPSLEEP mode, it first completes a full measurement loop and evaluates conditions relative to enabled protections, to ensure that conditions are acceptable to proceed to NORMAL mode. This may take about 250 ms plus the time for the measurement loop to complete.

The REG1 and REG2 LDOs will maintain their power state when entering DEEPSLEEP mode if the ***Settings:Configuration:Power Config[DPSLP_LDO]*** configuration bit is set. The device also provides the ability to keep the LFO running while in DEEPSLEEP mode, which allows for a faster responsiveness to communications and transition back to NORMAL mode, but will consume additional power. This is controlled by the ***Settings:Configuration:Power Config[DPSLP_LFO]*** configuration bit.

Other than the *0x000E EXIT_DEEPSLEEP()* subcommand, communications with the device over the serial interface will not cause it to exit DEEPSLEEP mode. However, since no measurements are taken while in DEEPSLEEP mode, there is no new information available for readout. To collect measurement data without powering the system the user can do the following:

1. Send the *0x0095 ALL_FETS_OFF()* subcommand to keep the FETs disabled.
2. Send the *0x000E EXIT_DEEPSLEEP()* subcommand to transition back into NORMAL mode.
3. Wait for a measurement cycle to complete by monitoring the *0x62 Alarm Status()[FULLSCAN]* bit.
4. Read the data.
5. Send the *0x000F DEEPSLEEP()* subcommand twice within 4 seconds to return to DEEPSLEEP mode.
6. Send the *0x0096 ALL_FETS_ON()* subcommand to unblock the FETs from being enabled when DEEPSLEEP mode is exited in the future.

7.5 SHUTDOWN Mode

SHUTDOWN mode is the lowest power mode of the BQ769142, which can be used for shipping or long-term storage. In this mode, the device loses all register state information, the internal logic is powered down, and all protection FETs are disabled, so no voltage is provided at the battery pack terminals. All protections are disabled, all voltage, current, and temperature measurements are disabled, and no communications are supported. When the device exits SHUTDOWN, it will boot and read parameters stored in OTP (if that has been written). If the OTP has not been written, the device will power up with default settings, and then settings can be changed by the host writing device registers.

Entering SHUTDOWN mode involves a sequence of steps. The sequence can be initiated manually by sending the *0x0010 SHUTDOWN()* subcommand twice in a row within a 4-s time window if the device is SEALED. If this subcommand is sent twice in a row while the device is UNSEALED, the delays associated with the sequence are skipped. The device can also be configured to enter SHUTDOWN mode automatically based on the top of stack voltage or the minimum cell voltage. If the top-of-stack voltage falls below ***Power:Shutdown:Shutdown Stack Voltage*** or if the minimum cell voltage falls below ***Power:Shutdown:Shutdown Cell Voltage***, the SHUTDOWN

mode sequence is automatically initiated. The shutdown based on cell voltage does not apply to cell input pins being used to measure interconnect, based on settings in ***Settings:Configuration:Vcell mode***.

Note

If this feature is enabled and cell open-wire detection is also enabled, an open-wire condition may result in the device entering SHUTDOWN mode before an open-wire fault can be recorded, unless delays are set appropriately. If an automatic shutdown has been started based on the cell or stack voltage, and the voltage measured on the PACK pin is equal or above the top-of-stack (TOS) voltage by a threshold given by ***Power:Sleep:Sleep Charger PACK-TOS Delta***, the device will return to NORMAL mode, which allows the pack to be charged out of a low voltage condition.

While the BQ769142 device is in NORMAL or SLEEP mode, the device can also be configured to enter SHUTDOWN mode if the internal temperature measurement exceeds ***Power:Shutdown:Shutdown Temperature*** for ***Power:Shutdown:Shutdown Temperature Delay*** seconds.

When the SHUTDOWN mode sequence has been initiated by the *0x0010 SHUTDOWN()* subcommand or the RST_SHUT pin driven high for 1 s, the device will wait for ***Power:Shutdown:FET Off Delay*** then disable the protection FETs. After a delay of ***Power:Shutdown:Shutdown Command Delay*** from when the sequence begins, the device will enter SHUTDOWN mode (so ***Power:Shutdown:Shutdown Command Delay*** should be set longer than ***Power:Shutdown:FET Off Delay***). However, if the voltage on the LD pin is still above the $V_{WAKEONLD}$ level, shutdown will be delayed until the voltage on LD falls below that level.

Note

When SHUTDOWN mode is initiated in this manner, the device will first transition to NORMAL mode and will block entrance to SLEEP mode. If the FETs were initially off (such as if the device was in DEEPSLEEP mode) and ***Power:Shutdown:FET Off Delay*** = 0, the FETs will remain off. However, if ***Power:Shutdown:FET Off Delay*** > 0, the FETs may be enabled (if not blocked) upon entering NORMAL mode, then disabled after the ***Power:Shutdown:FET Off Delay***. If this is not preferred, the host can send the *0x0095 ALL_FETS_OFF()* before entering DEEPSLEEP mode, then can send the *0x0096 ALL_FETS_ON()* when exiting DEEPSLEEP mode.

While the device is in SHUTDOWN mode, a ≈5 V level is provided at the TS2 pin with high source impedance. If the TS2 pin is pulled below $V_{WAKEONTS2}$, such as by a switch to VSS, or if a voltage is applied at the LD pin above $V_{WAKEONLD}$ (such as when a charger is attached in series FET configuration), the device will exit SHUTDOWN mode. Note: If a thermistor is attached from the TS2 pin to VSS, this will prevent the device from ever fully entering SHUTDOWN mode.

To avoid an unintentional wake from SHUTDOWN mode when putting the BQ769142 device into long-term storage, the device can be configured to automatically reenter SHUTDOWN mode after ***Power:Shutdown:Auto Shutdown Time*** minutes if the device boots from SHUTDOWN mode without any valid communications occurring or any charge or discharge current is detected. This feature is disabled by default, so it is necessary to program it enabled in OTP to ensure it is enabled when an unintentional wake occurs. It also does not take effect after a watchdog reset has occurred. See *Power:Shutdown:Auto Shutdown Time* for more details.

The BQ769142 device performs periodic memory integrity checks and forces a watchdog reset if any corruption is detected. To avoid a cycle of resets in the case of a memory fault, the device enters SHUTDOWN mode rather than resetting if a memory error is detected within ***Power:Shutdown:RAM Fail Shutdown Time*** seconds after a watchdog reset occurred.

When the device is wakened from SHUTDOWN, it requires approximately 200-300 ms (if ***Settings:Permanent Failure:Enabled PF A[CUDEP]*** is not enabled) for the internal circuitry to power up, load settings from OTP

memory, perform initial measurements, evaluate those relative to enabled protections, then to enable FETs if conditions allow. This can be much longer if ***[CUDEP]*** is enabled, depending on its associated delay setting in ***Permanent Fail:CUDEP:Delay***.

The BQ769142 device integrates a hardware overtemperature detection circuit, which determines when the die temperature passes an excessive temperature of approximately 120°C. If this detector triggers, the device will automatically begin the sequence to enter SHUTDOWN if the ***Settings:Configuration:Power Config[OTSD]*** configuration bit is set.

If the shutdown sequence was initiated, but the TS2 pin is held below $V_{WAKEONTS2}$ or the voltage at the LD pin is above $V_{WAKEONLD}$, then the device will stay in a "soft shutdown" state until the TS2 pin voltage is no longer below $V_{WAKEONTS2}$, and the LD pin voltage is below $V_{WAKEONLD}$. While in "soft shutdown," FETs are disabled, protections and measurements are stopped, and serial communication is disabled. The device exits "soft shutdown" if the LD voltage is allowed to first fall below $V_{WAKEONLD}$, then is raised above $V_{WAKEONLD}$ by a charger being attached, or if the RST_SHUT pin is transitioned from low to high or the conditions enable the device to continue into SHUTDOWN mode. $V_{WAKEONLD}$ and $V_{WAKEONTS2}$ are specified in *BQ769142 3-Series to 14-Series High Accuracy Battery Monitor and Protector for Li-Ion, Li-Polymer, and LiFePO$_4$ Battery Packs* (SLUSE91).

7.6 CONFIG_UPDATE Mode

The BQ769142 device uses a special CONFIG_UPDATE mode to make changes to the data memory settings. If changes were made to the data memory settings while the firmware was in normal operation, it could result in unexpected operation or consequences if settings used by the firmware changed in the midst of operation. When changes to the data memory settings are needed (which generally should only be done on the customer manufacturing line or in an offline condition), the host should:

Place the device into CONFIG_UPDATE mode by sending the *0x0090 SET_CFGUPDATE()* subcommand. The device will then automatically disable the protection FETs if they are enabled.

Wait for the *0x12 Battery Status()[CFGUPDATE]* flag to set.

Modify settings as needed by writing updated data memory settings (for more information, see *Data Memory Access*).

Send the *0x0092 EXIT_CFGUPDATE()* command to resume firmware operation.

When in CONFIG_UPDATE mode, the device stops normal firmware operation and stops all measurements and protection monitoring. The host can then make changes to data memory settings (either writing registers directly into RAM, or instructing the device to program the RAM data into OTP). After changes are complete, the host then sends the *0x0092 EXIT_CFGUPDATE()* command, at which point the device restarts normal firmware operation using the new data memory settings.

8.1 Overview

The BQ769142 device includes three security modes: SEALED, UNSEALED, and FULLACCESS, which can be used to limit the ability to view or change settings.

In SEALED mode, most data and status can be read using commands and subcommands, but only selected settings can be changed. Data memory settings cannot be read or changed directly.

UNSEALED mode includes SEALED functionality, and also adds the ability to execute additional subcommands and read data memory.

FULLACCESS mode allows capability to read and modify all device settings, including writing OTP memory.

Selected settings in the device can be modified while the device is in operation through supported commands and subcommands, but in order to modify all settings, the device must enter CONFIG_UPDATE mode (see Section 7.6), which stops device operation while settings are being updated. After the update is completed, device operation is restarted using the new settings. CONFIG_UPDATE mode is only available in FULLACCESS mode.

The BQ769142 device implements a key-access scheme to transition among SEALED, UNSEALED, and FULLACCESS modes. Each transition requires that a unique set of keys be sent to the device through the subcommand address (0x3E and 0x3F). The keys must be sent consecutively to 0x3E and 0x3F, with no other data written between the keys. Do not set the two keys to identical values. When in the SEALED mode, the *0x12 Battery Status()[SEC1, SEC0]* bits are set to [1, 1]. When the UNSEAL keys are correctly received by the device, the bits will be set to [1, 0]. When the FULLACCESS keys are correctly received, then the bits will change to [0, 1]. The state [0, 0] is not valid, and only indicates that the state has not yet been loaded. The device must first transition from SEALED mode to UNSEALED mode before it can then transition to FULL ACCESS mode.

The unseal keys are stored in data memory in ***Security:Keys:Unseal Key Step 1*** and ***Security:Keys:Unseal Key Step 2***. The FULLACCESS keys are stored in ***Security:Keys:Full Access Key Step 1*** and ***Security:Keys:Full Access Key Step 2***. The access keys are changed during operation using the *0x0035 SECURITY_KEYS()* subcommand. This subcommand enables a R/W of the 4 key words (8 bytes). Each word is sent in big endian order using this subcommand, with the first two words being the unseal code and the remaining two words being the full access codes.

When using the codes by writing them to 0x3E and 0x3F, they must be sent in little endian order; therefore, if 0x1234 and 0x5678 are written as the unseal codes to *0x0035 SECURITY_KEYS()*, then to unseal requires writing 0x34 and 0x12 to 0x3E and 0x3F, followed by writing 0x78 and 0x56 to 0x3E and 0x3F. The two codes must be written within 4 s of each other to succeed.

To read the keys:

1. Write 0x35 and 0x00 to 0x3E and 0x3F
2. Read back 8 bytes from the transfer buffer at 0x40–0x47.

To write the keys:

1. Write 0x35 and 0x00 to 0x3E and 0x3F.
2. Write the data in big endian format to the transfer buffer at 0x40–0x47.
3. Write the checksum to 0x60. The checksum is the complement of the sum of the data and command bytes.

4. Write the length of 0x0A to 0x61. The length includes the command, data, checksum, and length bytes.

To set the device into SEALED mode when initially powering up, the ***Security:Settings:Security Settings[SEAL]*** configuration bit can be set. During operation, the device can be put into SEALED mode by sending the *0x0030 SEAL()* subcommand.

The BQ769142 device includes additional means to limit further modification of device settings. If the ***Security:Settings:Security Settings[LOCK_CFG]*** configuration bit is set, the data memory settings can no longer be modified when the device is in CONFIG_UPDATE mode. If the ***Security:Settings:Security Settings[PERM_SEAL]*** bit is set, the device cannot be unsealed after it has been sealed.

The device provides additional checks which can be used to optimize system robustness:

The *0x0004 IROM_SIG()* subcommand calculates a digital signature of the integrated instruction ROM, and the *0x0009 DROM_SIG()* subcommand calculates a similar signature of the integrated data ROM (which contains the default values for the device). These signatures should never change for a particular product. If these were to change, it would indicate an error, either that the ROM had been corrupted, or the readback of the ROM or calculation of the signature experienced an error.

The *0x0005 STATIC_CFG_SIG()* subcommand calculates a digital signature for the static configuration data (which excludes calibration values) and compares it to a stored value. If the result does not match the stored signature, the MSB returned is set.

9.1 Serial Communications Overview

The BQ769142 device integrates three serial communication interfaces an I^{2}C bus, which supports 100-kHz and 400-kHz modes with an optional CRC check, an SPI bus with an optional CRC check, which supports a clock rate up to 2 MHz, and a single-wire HDQ interface. The BQ769142 device is the configured default in I^{2}C mode with CRC enabled, and can be changed to SPI or HDQ mode by programming either the register or OTP configuration accordingly. The customer can program the device's integrated OTP on the manufacturing line to set the desired communications speed and protocol to be used at power up in operation.

The ***Settings:Configuration:Comm Type*** configuration register controls the active communication mode of the BQ769142 device. These settings are shown below.

Table 9-1. Comm Type Data Memory Settings

Comm Type Setting	Description
0x00	Default (I^{2}C Fast with CRC enabled)
0x03	HDQ using the ALERT pin
0x04	HDQ using the HDQ pin
0x07	I^{2}C (for use up to 100 kHz bus speed)
0x08	I^{2}C Fast (for use above 100 kHz bus speed)
0x09	I^{2}C Fast with timeouts (for use above 100 kHz bus speed)
0x0F	SPI
0x10	SPI with CRC
0x11	I^{2}C with CRC (for use up to 100 kHz bus speed)
0x12	I^{2}C Fast with CRC (for use above 100 kHz bus speed)
0x1E	I^{2}C with timeouts (for use with 100 kHz bus speed)
0xFF	I^{2}C Fast (for use above 100 kHz bus speed)
All other values	Reserved. Do not use.

9.2 I^{2}C Communications Subsystem

The I^{2}C serial communications interface in the BQ769142 device acts as a responder device and supports rates up to 400 kHz with an optional CRC check. If the OTP has not been programmed, the BQ769142 will initially power up by default in 400 kHz I^{2}C mode with CRC enabled. The OTP setting can be programmed on the manufacturing line, then when the device powers up, it will automatically enter the selected mode per OTP setting. The host can also change the I^{2}C speed setting while in CONFIG_UPDATE mode, then the new speed setting will take effect upon exit of CONFIG_UPDATE mode. Alternatively, the host can write the *0x29e7 SWAP_TO_I2C()* subcommand to change the communications interface to I^{2}C fast mode (***Settings:Configuration:Comm Type*** = 8) immediately, without needing to enter CONFIG_UPDATE mode. The *0x29BC SWAP_COMM_MODE()* subcommand can be sent to transition the device to the communications mode selected by the setting in ***Settings:Configuration:Comm Type***.

The I^{2}C device address is set by default as 0x10 (write), 0x11 (read), which can be changed by programming ***Settings:Configuration:I2C Address*** with the desired write address.

The communications interface includes optional timeout capability which can be enabled based on the ***Comm Type*** setting. The ***Comm Type*** settings with timeouts should only be used if the bus will be operating at 100 kHz or 400 kHz. If ***Comm Type***= 0x1E (100 kHz mode with timeouts enabled), then the device will reset the communications interface logic if a clock is detected low longer than a $t_{TIMEOUT}$ of 25 ms to 35 ms, or if the cumulative clock low responder extend time exceeds ≈25 ms, or if the cumulative clock low controller extend time exceeds 10 ms. If ***Comm Type***= 0x09 (400 kHz mode with timeouts enabled), then the device will reset the communications interface logic if a clock is detected low longer than $t_{TIMEOUT}$ of 5 ms to 20 ms. The bus also includes a long-term timeout if the SCL pin is detected low for more than 2 seconds, which applies whether the ***Comm Type*** setting includes timeouts or not.

An I²C write transaction is shown in Figure 9-1. Block writes are allowed by sending additional data bytes before the Stop. The I²C logic will auto-increment the register address after each data byte.

When enabled, the CRC is calculated as follows:

- In a single-byte write transaction, the CRC is calculated over the responder address, register address, and data.
- In a block write transaction, the CRC for the first data byte is calculated over the responder address, register address, and data. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the responder detects a bad CRC, the I²C responder will NACK the CRC, which causes the I²C responder to go to an idle state.

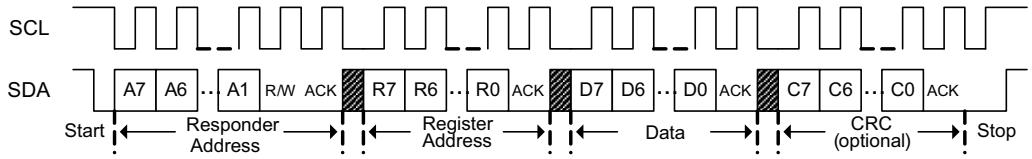

Figure 9-1. I²C Write

Figure 9-2 shows a read transaction using a Repeated Start.

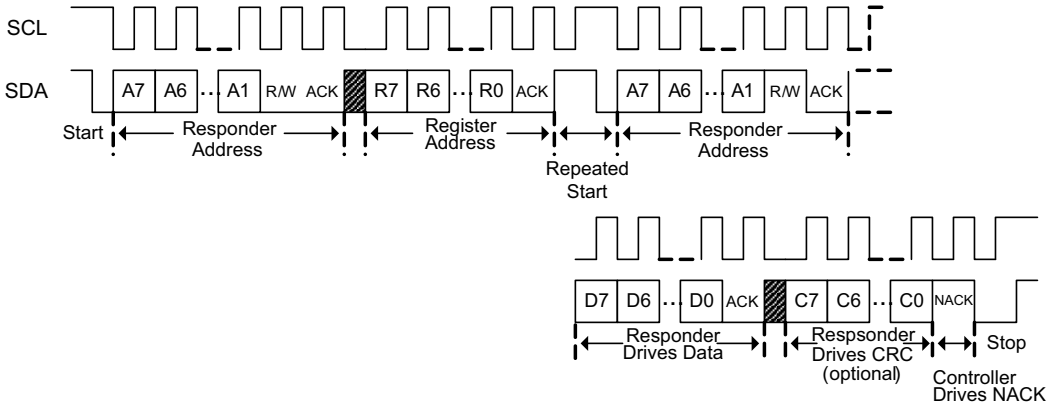

Figure 9-2. I²C Read with Repeated Start

Figure 9-3 shows a read transaction where a Repeated Start is not used, for example if not available in hardware. For a block read, the controller ACKs each data byte except the last and continues to clock the interface. The I²C block will auto-increment the register address after each data byte.

When enabled, the CRC for a read transaction is calculated as follows:

- In a single-byte read transaction, the CRC is calculated beginning at the first start, so will include the responder address, the register address, then the responder address with read bit set, then the data byte.
- In a block read transaction, the CRC for the first data byte is calculated beginning at the first start and will include the responder address, the register address, then the responder address with read bit set, then the

data byte. The CRC resets after each data byte and after each stop. The CRC for subsequent data bytes is calculated over the data byte only.

The CRC polynomial is $x^8 + x^2 + x + 1$, and the initial value is 0.

When the controller detects a bad CRC, the I²C controller will NACK the CRC, which causes the I²C responder to go to an idle state.

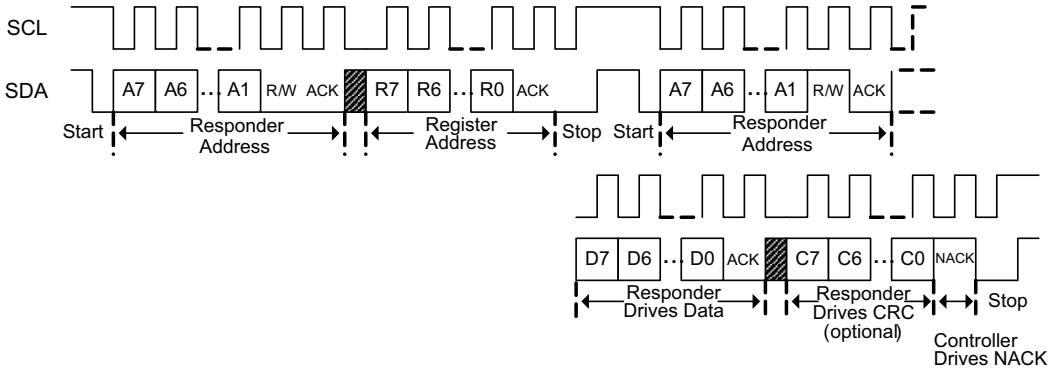

Figure 9-3. I²C Read Without Repeated Start

When the host sends a read transaction, the device may clock stretch while it fetches the data and prepares to send it. However, when subcommands that require the device to fetch data and load it into the 0x40–0x5F transfer buffer are sent, the device does not clock stretch during this time. The timing required for the device to fetch the data depends on the specific subcommand and any other processing underway within the device, so it will vary during operation. The approximate times required for the device to fetch the data for subcommands are described in Table 9-2. When sending a subcommand, it is recommended to wait long enough for the device to fetch the data, then read 0x3E/0x3F again. If the initial subcommand is echoed back from this read, then the fetched data is available and can be read from the transfer buffer.

9.3 SPI Communications Interface

The SPI interface in the BQ769142 device operates as a responder-only interface and supports rates up to 2 MHz with an optional CRC check. If the OTP has not been programmed, the BQ769142 will initially power up by default in 400 kHz I²C mode with CRC enabled. The OTP setting to select SPI mode in the BQ769142 (set by ***Settings:Configuration:Comm Type***) can be programmed on the manufacturing line to select SPI mode, then when the device powers up, it will automatically enter SPI mode. The host can also change the serial communication setting while in CONFIG_UPDATE mode, although the device will not immediately change communication mode upon exit of CONFIG_UPDATE mode, in order to avoid losing communications during evaluation or production. The host can write the *0x7C35 SWAP_TO_SPI()* subcommand to change the communications interface to SPI with CRC (***Settings:Configuration:Comm Type*** = 16) immediately, without needing to change the setting in CONFIG_UPDATE mode. Alternatively, the *0x29BC SWAP_COMM_MODE()* subcommand can be sent to transition the device to the communications mode selected by the setting in ***Settings:Configuration:Comm Type***.

The SPI interface logic operates with clock polarity (CPOL) = 0 and clock phase (CPHA) = 0, as shown in the figure below.

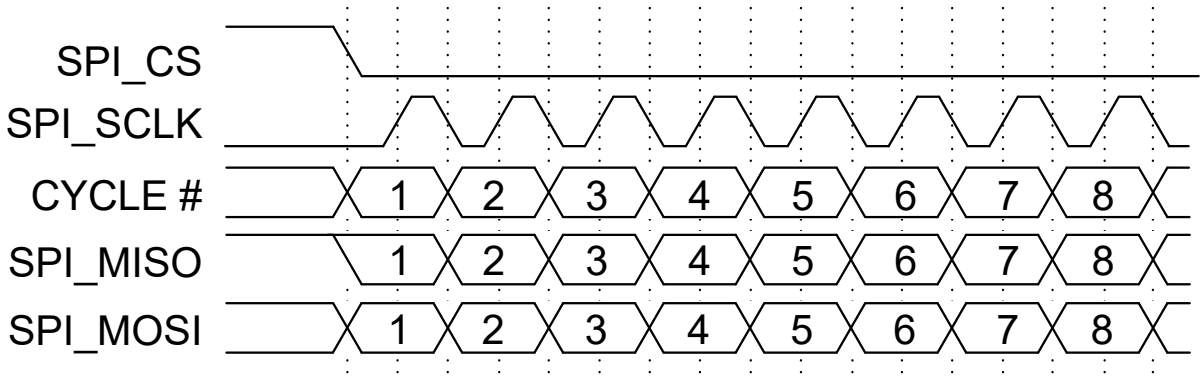

Figure 9-4. SPI with CPOL = 0 and CPHA = 0

The device also includes an optional 8-bit CRC using polynomial $x^8 + x^2 + x + 1$. The interface must use 16-bit transactions if CRC is not enabled, and must use 24-bit transactions when CRC is enabled. CRC mode is enabled or disabled based on the setting of ***Settings:Configuration:Comm Type***. Based on control settings, the logic will:

(a) only work with CRC, will not accept data without valid CRC, or

(b) will only accept transactions without CRC (so the host must only clock 16-bits per transaction, the device will detect an error if more or less clocks are sent).

If the host performs a write with CRC and the CRC is not correct, then the incoming data is not transferred to the incoming buffer, and the outgoing buffer (used for the next transaction) is also reset to 0xFFFF. This transaction is considered invalid. On the next transaction, the CRC (if clocked out) will be 0xAA, so the 0xFFFFAA will indicate to the controller that a CRC error was detected.

The internal oscillator in the BQ769142 device may not be running when the host initiates a transaction (for example, this can occur if the device is in SLEEP mode). If this occurs, the interface will drive out 0xFFFF on SPI_MISO for the first 16-bits clocked out. It will also drive out 0xFF for the third (CRC) byte as well, if CRC is enabled. So the 0xFFFFFF will indicate to the controller that the internal oscillator is not ready yet. The address 0x7F used in the device is defined in such a manner that there should be no valid transaction to write 0xFF into this address. Thus the two-byte pattern 0xFFFF should never occur as a valid sequence in the first two bytes of a transaction (that is, it is only used as a flag that something is wrong, similar to an I^2C NACK).

If the internal HFO oscillator is not running in the device, it will be automatically wakened at the falling edge of SPI_CS (this is true while in NORMAL, SLEEP, or DEEPSLEEP modes, but not in SHUTDOWN mode). In NORMAL mode or SLEEP mode, the HFO may take ≈ 135 µs to stabilize and be available for use by the SPI interface logic. In DEEPSLEEP mode, the HFO will take ≈ 4.5 ms to stabilize and be available. This delay means that requested data generally cannot be provided back to the host during the first SPI transaction when the HFO was initially off. Thus, in cases when the HFO is likely initially off, it is recommended that the host first write a "dummy" SPI transaction to waken the HFO, then wait at least 135 µs while in NORMAL or SLEEP modes, or 4.5 ms while in DEEPSLEEP mode, before sending the intended SPI transaction. If an SPI transaction returns 0xFFFF (in 16-bit mode) or 0xFFFFFF (in 24-bit mode) while in NORMAL or SLEEP modes, the host should retry the transaction again after a delay of at least 135 µs, or 4.5 ms after initial powerup or while in DEEPSLEEP mode. This allows time for the HFO to waken, if it was initially off, and for the device to prepare the data requested and have it ready for readout.

It is recommended to set the ***Settings:Configuration:Comm Idle Time*** to a level of 1 second or higher when using SPI mode, which causes the HFO to stay powered for a programmable number of seconds after it is wakened by a falling edge on SPI_CS. The host can set this to a longer time (up to 255 seconds) and maintain regular communications within this window, causing the HFO to stay powered, so the device can respond quickly to SPI transactions. However, keeping the HFO running continuously will cause the device to consume additional

supply current (≈ 30 µA) beyond what it would consume if there were minimal communications. In order to avoid this extra supply current, the host can send initially send a "dummy" SPI transaction (such as reading command *CONTROL_STATUS()*) to cause the HFO to waken, and continue this until a valid response is returned on SPI_MISO. At this point, the host can begin sending the intended SPI transactions. Afterward, the host can write 0xAA to the 0x7F address, which will cause the HFO to turn off.

Note

0x7F FET Status() is a read-only command. This special case of sending 0xAA to that command address is unrelated to the *0x7F FET Status()* command.

The device includes ability to detect a frozen or disconnected SPI bus condition, and it then resets the bus logic. This condition is recognized when the SPI_CS is low and the SPI_SCLK is static and not changing for a two-second timeout.

9.3.1 SPI Protocol

The first byte of a SPI transaction consists of an R/W bit (R=0, W=1), followed by a 7-bit address, MSB first. If the controller (host) is writing, then the second byte will be the data to be written. If the controller is reading, then the second byte sent on SPI_MOSI is ignored (except for CRC calculation).

If CRC is enabled, then the controller must send as the third byte the 8-bit CRC code, which is calculated over the first two bytes. If the CRC is correct, then the values clocked in will be put into the incoming buffer. If the CRC is not correct, then the outgoing buffer will be set to 0xFFFF, and the outgoing CRC will be set to 0xAA (these are clocked out on the next transaction).

During this transaction, the logic will clock out the contents of the outgoing buffer. If the outgoing buffer has not been updated since the last transaction, then the logic will clock out 0xFFFF, and if the CRC is clocked, it will clock out 0x00 for the CRC (if enabled). Thus the 0xFFFF00 will indicate to the controller that the outgoing buffer was not updated by the internal logic before the transaction occurred. This can occur when the device did not have sufficient time to update the buffer between consecutive transactions.

When the internal logic takes the write-data from the interface logic and processes it, it also causes the R/W bit, address, and data to be copied into the outgoing buffer. On the next transaction, this data is clocked back to the controller.

When the controller is initiating a read, the internal logic will place the R/W bit and address into the outgoing buffer, along with the data requested. The interface will compute the CRC on the two bytes in the outgoing buffer and clock that back to the controller if CRC is enabled (with the exceptions associated with 0xFFFF as noted above). A diagram of three transaction sequences with and without CRC are shown below, using CPOL=0.

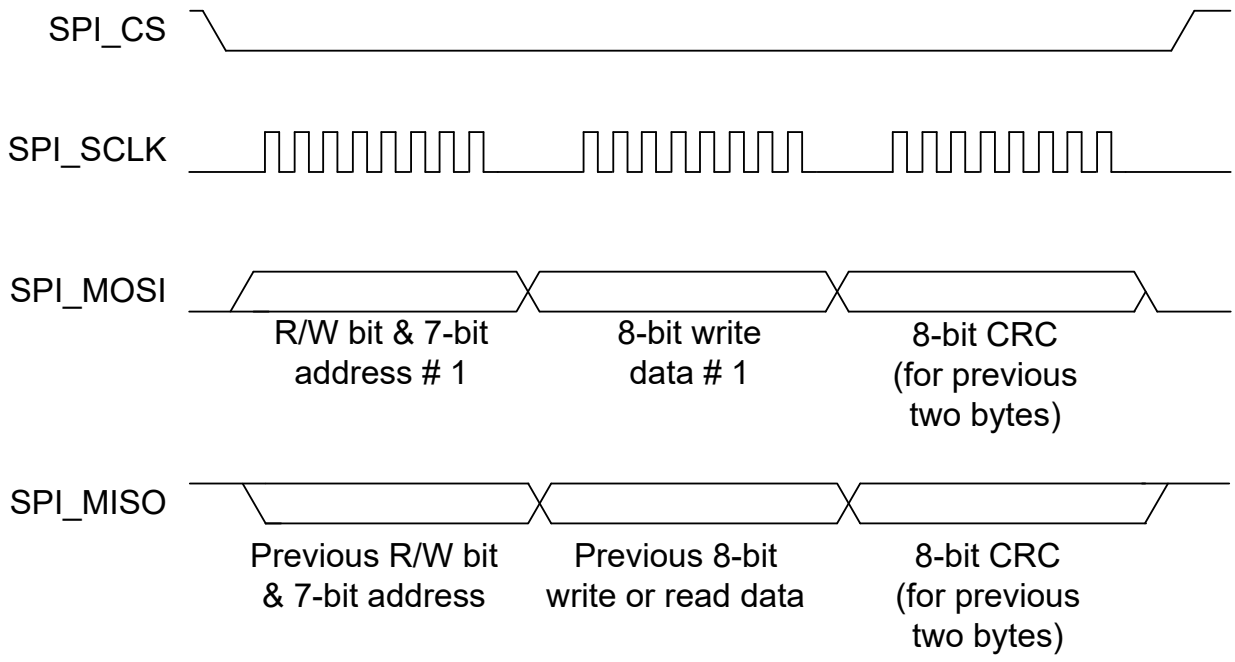

Figure 9-5. SPI Transaction #1 Using CRC

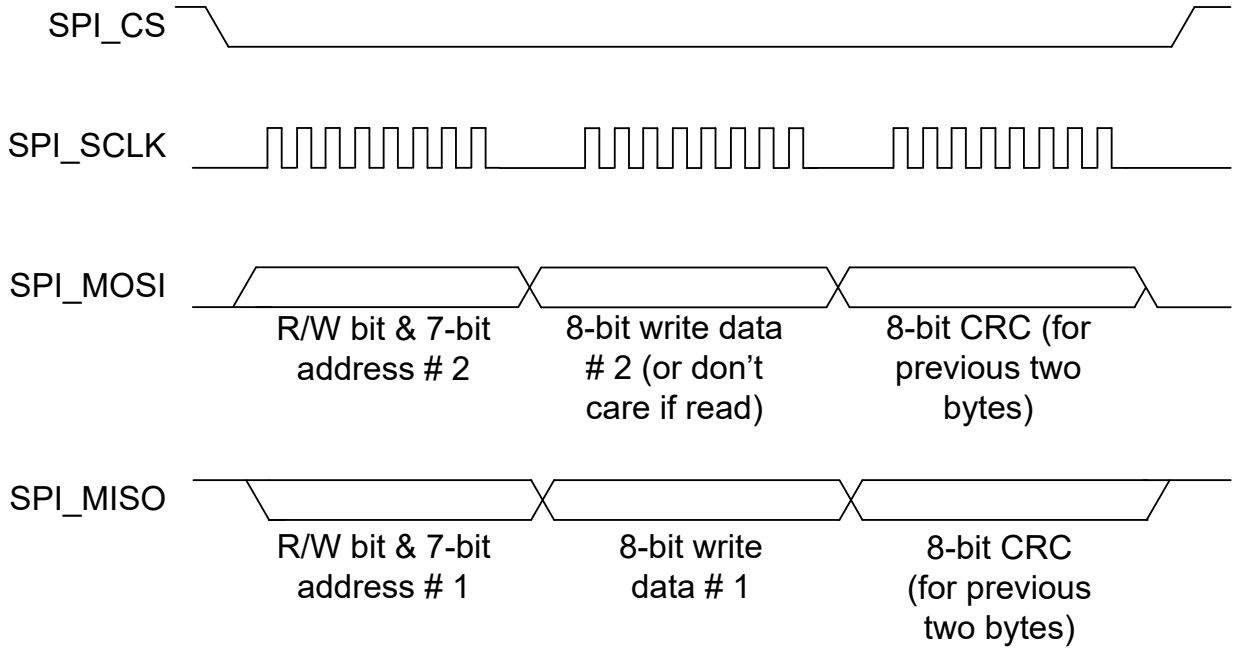

Figure 9-6. SPI Transaction #2 Using CRC

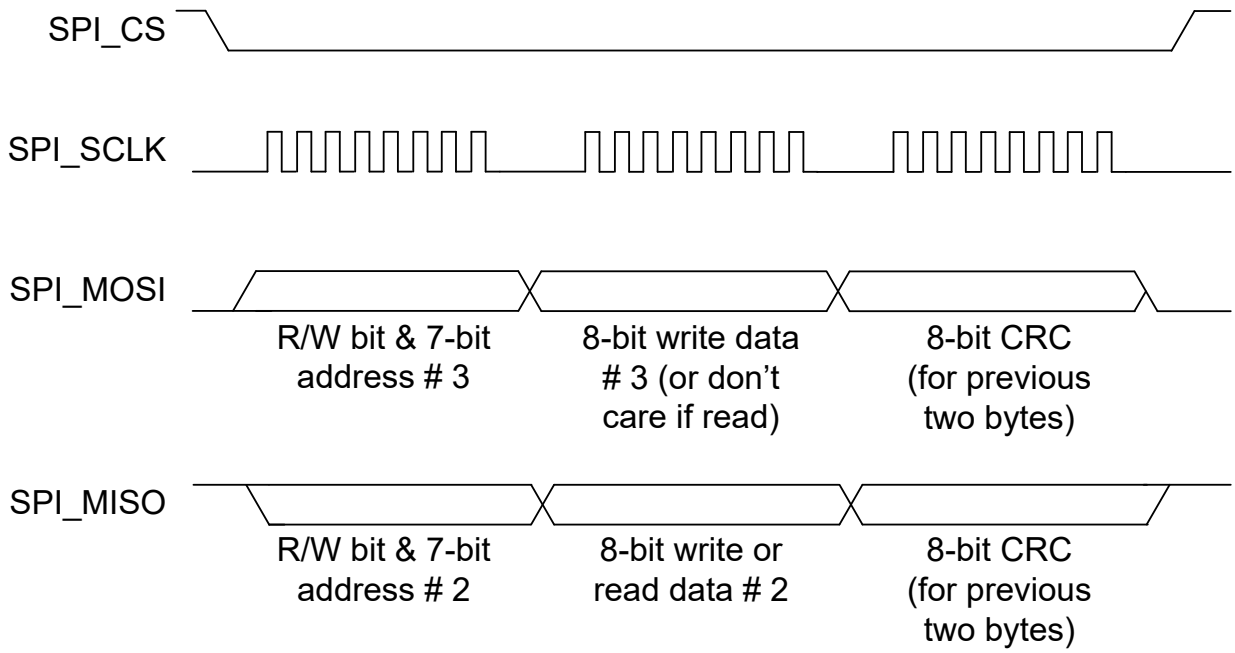

Figure 9-7. SPI Transaction #3 Using CRC

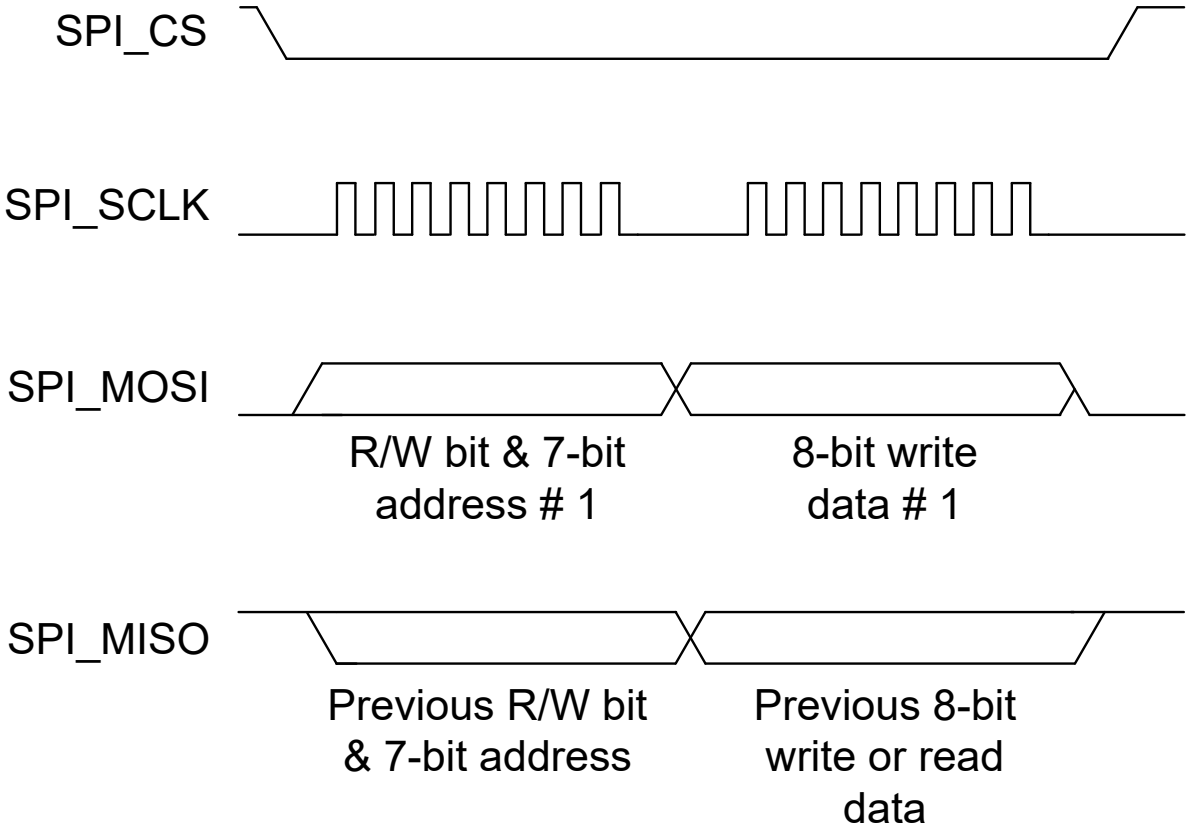

Figure 9-8. SPI Transaction #1 Without CRC

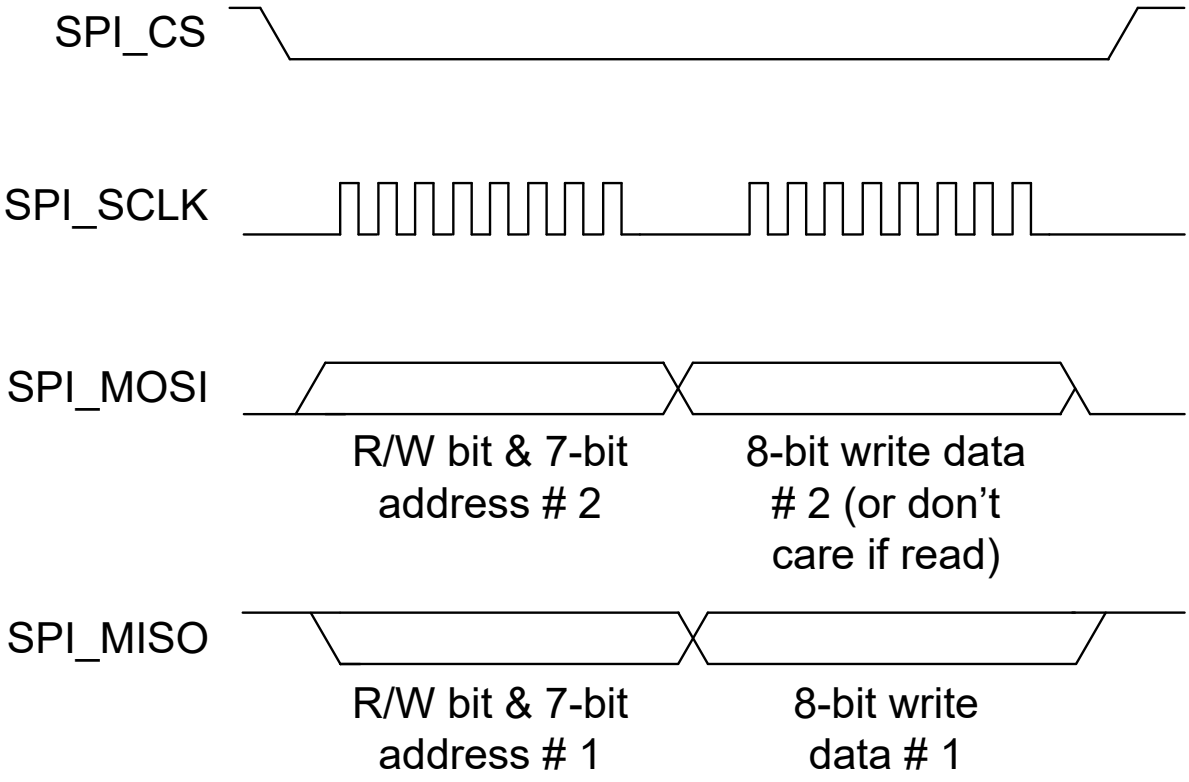

Figure 9-9. SPI Transaction #2 Without CRC

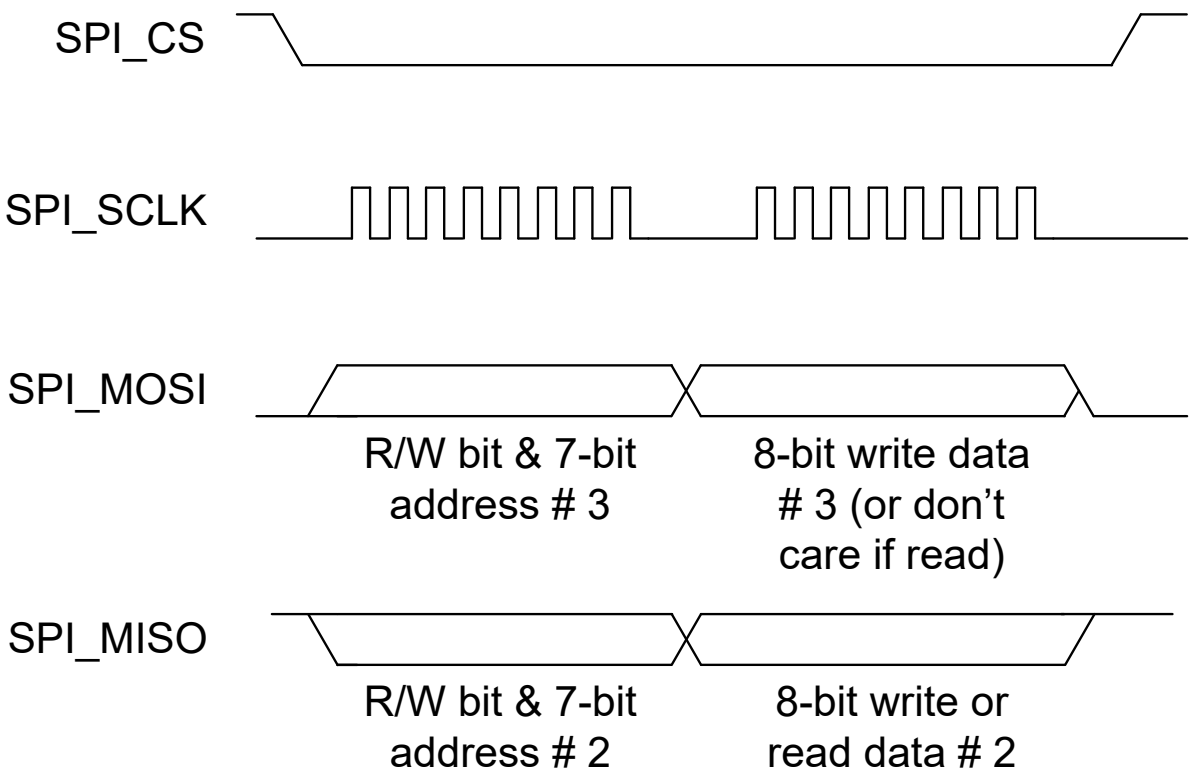

Figure 9-10. SPI Transaction #3 Without CRC

The time required for the device to process commands and subcommands differs based on the specifics of each. For example, when the *0x0071 DASTATUS1()* subcommand is sent, the device requires approximately 200 µs to load the 32-byte data into the internal subcommand buffer. If the host provides sufficient time for this load to complete before beginning to read the buffer (readback from addresses 0x40 to 0x5F), the device will respond with valid data, rather than 0xFFFF00. When data has already been loaded into the subcommand buffer, this data can be read back with approximately 50 µs interval between SPI transactions. Note that some commands or subcommands may take longer than 200 µs to complete. A notable exception is the *IROM_SIG()* subcommand, which takes approximately 9 ms to complete.

The host software should incorporate a scheme to retry transactions that may not be successful. For example, if the device returns 0xFFFFFF on SPI_MISO, then the internal clock was not powered, and the transaction will need to be retried. Similarly, if the device returns 0xFFFFAA on a transaction, this indicates the previous transaction encountered a CRC error, and so the previous transaction must be retried. And as described above, if the device returns 0xFFFF00, then the previous transaction had not completed when the present transaction was sent, which may mean the previous transaction should be retried, or at least needs more time to complete.

The approximate time required to complete an operation based on the particular command or subcommand is shown below. Note that these times are only approximate and may vary depending on system operation at the time. Therefore, it is important that the host processor incorporate a retry scheme from the host processor, to handle communications errors or delays that may occur during operation.

Table 9-2. Command/Subcommand Operation Time

Command/Subcommand Address	Command/Subcommand Name	Time to Complete Operation (Approximate)
0x00	Control Status()	50 µs
0x02–0x07	Safety Alert() and Safety Status()	50 µs

Table 9-2. Command/Subcommand Operation Time (continued)

Command/Subcommand Address	Command/Subcommand Name	Time to Complete Operation (Approximate)
0x0A–0x11	PF Alert() and PF Status()	50 µs
0x12	Battery Status()	50 µs
0x14–0x32	Cell Voltages()	50 µs
0x34	Stack Voltage()	50 µs
0x36	PACK Pin Voltage()	50 µs
0x38	LD Pin Voltage()	50 µs
0x3A	CC2 Current()	50 µs
0x62	Alarm Status()	50 µs
0x64	Alarm Raw Status()	50 µs
0x66	Alarm Enable()	50 µs
0x68	Internal Temperature()	50 µs
0x6A–0x7A	Thermistor Temperatures()	50 µs
0x0001	DEVICE_NUMBER()	400 µs
0x0002	FW_VERSION()	400 µs
0x0003	HW_VERSION()	400 µs
0x0004	IROM_SIG()	8500 µs
0x0005	STATIC_CFG_SIG()	450 µs
0x0009	DROM_SIG()	650 µs
0x000E	EXIT_DEEPSLEEP()	500 µs
0x000F	DEEPSLEEP()	500 µs
0x0010	SHUTDOWN()	500 µs
0x001C	PDSGTEST()	550 µs
0x001D	FUSE_TOGGLE()	500 µs
0x001E	PCHGTEST()	900 µs
0x001F	CHGTEST()	550 µs
0x0020	DSGTEST()	550 µs
0x0022	FET_ENABLE()	500 µs
0x0024	PF_ENABLE()	500 µs
0x0030	SEAL()	500 µs
0x0053	SAVED_PF_STATUS()	500 µs
0x0057	MANUFACTURING STATUS()	500 µs
0x0070	MANU_DATA()	660 µs
0x0071–0x0077	DASTATUS1-7()	660 µs
0x0080	CUV_SNAPSHOT()	660 µs
0x0081	COV_SNAPSHOT()	660 µs
0x0082	RESET_PASSQ()	600 µs
0x0083	CB_ACTIVE_CELLS()	560 µs
0x0084	CB_SET_LVL()	480 µs

Table 9-2. Command/Subcommand Operation Time (continued)

Command/Subcommand Address	Command/Subcommand Name	Time to Complete Operation (Approximate)
0x0085–0x0087	CBSTATUS1-3()	575 µs
0x008A	PTO_RECOVER()	500 µs
0x0090	SET_CFGUPDATE()	2000 µs
0x0092	EXIT_CFGUPDATE()	1000 µs
0x0093	DSG_PDSG_OFF()	550 µs
0x0094	CHG_PCHG_OFF()	550 µs
0x0095	ALL_FETS_OFF()	550 µs
0x0096	ALL_FETS_ON()	500 µs
0x0097	FET_CONTROL()	495 µs
0x0098	REG12_CONTROL()	450 µs
0x0099	SLEEP_ENABLE()	500 µs
0x009A	SLEEP_DISABLE()	500 µs
0x009B	OCDL_RECOVER()	500 µs
0x009C	SCDL_RECOVER()	500 µs
0x009D	LOAD_DETECT_RESTART()	500 µs
0x009E	LOAD_DETECT_ON()	500 µs
0x009F	LOAD_DETECT_OFF()	500 µs
0x00A0	OTP_WR_CHECK()	580 µs
0x2800–0x2818	GPO HI and LO Subcommands	500 µs
0x2857	PF_FORCE_A()	500 µs
0x29A3	PF_FORCE_B()	800 µs
0x29BC	SWAP_COMM_MODE()	500 µs
0x29E7	SWAP_TO_I2C()	500 µs
0x7C35	SWAP_TO_SPI()	500 µs
0x7C40	SWAP_TO_HDQ()	500 µs
0xF081	READ_CAL1()	630 µs

9.4 HDQ Communications Interface

The HDQ interface is an asynchronous return-to-one protocol where a processor communicates with the BQ769142 device using a single-wire connection to either the ALERT pin (***Settings:Configuration:Comm Type*** = 3) or the HDQ pin (***Settings:Configuration:Comm Type*** = 4). Note that the selected pin must be configured for use as the HDQ interface. Both the controller (host device) and responder (BQ769142) drive the HDQ interface using an open-drain driver, with a pull-up resistor from the HDQ interface to a supply voltage required on the circuit board. The BQ769142 device can be changed from the default I^2C communication mode to HDQ communication mode by sending the *0x7C40 SWAP_TO_HDQ()* subcommand (at which point the device switches to HDQ mode using the ALERT pin immediately). Alternatively, the mode can be changed by setting the ***Settings:Configuration:Comm Type*** configuration register in CONFIG_UPDATE mode, then exiting CONFIG_UPDATE mode, then sending the *0x29BC SWAP_COMM_MODE()* subcommand, at which point the device switches to the selected mode.

With HDQ, the least significant bit (LSB) of a data byte (command) or word (data) is transmitted first.

The 8-bit command code consists of two fields: the 7-bit HDQ command code (bits 0–6) and the 1-bit R/W field (MSB Bit 7). The R/W field directs the device to do one of the following:

- Accept the next 8 bits as data from the host to the device, or
- Output 8 bits of data from the device to the host in response to the 7-bit command.

The HDQ peripheral on the BQ769142 device can transmit and receive data as an HDQ responder only.

The return-to-one data bit frame of HDQ consists of the following sections:

1. The first section is used to start the transmission by the host sending a Break (the host drives the HDQ interface to a logic-low state for a time $t_{(B)}$) followed by a Break Recovery (the host releases the HDQ interface for a time $t_{(BR)}$).
2. The next section is for host command transmission, where the host transmits 8 bits by driving the HDQ interface for 8 $T_{(CYCH)}$ time slots. For each time slot, the HDQ line is driven low for a time $T_{(HW0)}$ (host writing a "0") or $T_{(HW1)}$ (host writing a "1"). The HDQ pin is then released and remains high to complete each $T_{(CYCH)}$ time slot.
3. The next section is for data transmission where the host (if a write was initiated) or device (if a read was initiated) transmits 8 bits by driving the HDQ interface for 8 $T_{(CYCH)}$ (if host is driving) or $T_{(CYCD)}$ (if device is driving) time slots. The HDQ line is driven low for a time $T_{(HW0)}$ (host writing a "0"), $T_{(HW1)}$ (host writing a "1"), $T_{(DW0)}$ (device writing a "0"), or $T_{(DW1)}$ (device writing a "1"). The HDQ pin is then released and remains high to complete the time slot. The HDQ interface does not auto-increment, so a separate transaction must be sent for each byte to be transferred.

10.1 Cell Balancing Operation

The BQ769142 device supports passive cell balancing by bypassing the current of selected cells during charging or at rest, using either integrated bypass switches between cells, or external bypass transistors. The device incorporates a voltage-based balancing algorithm which can optionally balance cells autonomously without requiring any interaction with a host processor. Or if preferred, balancing can be entirely controlled manually from a host processor. For autonomous balancing, the device will only balance non-adjacent cells in use (it does not consider inputs used to measure interconnect as cells in use). In order to avoid excessive power dissipation within the BQ769142 device, the maximum number of cells allowed to balance simultaneously can be limited by setting ***Settings:Cell Balancing Config:Cell Balance Max Cells***. For host-controlled balancing, adjacent as well as non-adjacent cells can be balanced.

Host-controlled balancing can be controlled using specific subcommands (described below) sent by the host. These subcommands are also accessible in SEALED mode, to avoid the need for the pack to be unsealed in operation in order to initiate balancing. If host-controlled balancing will not be used, access to these subcommands can be disabled by setting the ***Settings:Cell Balancing Config:Balancing Configuration[CB_NO_CMD]*** configuration bit.

The subcommands the host uses to control cell balancing are described below.

Table 10-1. Host-Controlled Cell Balancing Subcommands

Subcommand	Description
0x0083 CB_ACTIVE_CELLS()	When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Write 0x0000 to turn balancing off. This command may take up to approximately 1 second to take effect.
0x0084 CB_SET_LVL()	When written with a 16-bit cell voltage threshold in mV, the device begins balancing one or more of the highest voltage cells if above the written threshold.

The device also returns status information regarding how long cells have been balanced through the subcommands described below.

Table 10-2. Cell Balancing Status Subcommands

Subcommand	Description
0x0085 CBSTATUS1()	When read, returns the 16-bit time in seconds that balancing has been active.
0x0086 CBSTATUS2()	When read, returns a block containing the 32-bit cumulative balancing times in seconds for each of cells 1–8. These values will reset if a device reset occurs, or the device enters CONFIG_UPDATE mode.
0x0087 CBSTATUS3()	When read, returns a block containing the 32-bit cumulative balancing times in seconds for each of cells 9–14. These values will reset if a device reset occurs, or the device enters CONFIG_UPDATE mode.

When host-controlled balancing is initiated using the subcommands above, the device starts a timer and continues balancing until the timer reaches a value of ***Settings:Cell Balancing Config:Cell Balance Interval***, or a new balancing subcommand is issued (which resets the timer). This is included as a precaution, in case the host processor initiated balancing but then stopped communication with the BQ769142 device, so that balancing would not continue indefinitely.

The BQ769142 device can automatically balance cells using a voltage-based algorithm based on environmental and system conditions. Several settings are provided to control when balancing is allowed, as described below.

Temperature—The device will disable balancing (both autonomous and host-controlled) if the cell temperature is below ***Settings:Cell Balancing Config:Min Cell Temp*** or above ***Settings:Cell Balancing Config:Max Cell Temp*** or the internal die temperature of the device is above ***Settings:Cell Balancing Config:Max Internal Temp***.

Charge versus Relax—Autonomous balancing can be allowed during charging by setting ***Settings:Cell Balancing Config:Balancing Configuration[CB_CHG]***, or in a relaxed condition by setting ***Settings:Cell Balancing Config:Balancing Configuration[CB_RLX]***, or both. If ***Settings:Cell Balancing Config:Balancing Configuration[CB_CHG]*** is set, autonomous balancing is allowed while the CC1 Current is above ***Settings:Current Thresholds:Chg Current Threshold***. If ***Settings:Cell Balancing Config:Balancing Configuration[CB_RLX]*** is set, autonomous balancing is allowed while the current is below ***Settings:Current Thresholds:Chg Current Threshold*** and above the negative of ***Settings:Current Thresholds:Dsg Current Threshold***. The device evaluates the conditions for continuing balancing every ***Settings:Cell Balancing Config:Cell Balance Interval***. For example, if the device is configured to avoid balancing during charge, and while balancing the pack begins charging, balancing will continue until the interval timer expires before it is disabled.

Cell Voltage—If autonomous balancing during charge is enabled, the device will allow balancing if the minimum cell voltage is above ***Settings:Cell Balancing Config:Cell Balance Min Cell V (Charge)*** and the difference between the maximum and minimum cell voltages is greater than ***Settings:Cell Balancing Config:Cell Balance Min Delta (Charge)***. Similarly, if autonomous balancing during relax is enabled, the device will allow balancing if the minimum cell voltage is above ***Settings:Cell Balancing Config:Cell Balance Min Cell V (Relax)*** and the difference between the maximum and minimum cell voltages is greater than ***Settings:Cell Balancing Config:Cell Balance Min Delta (Relax)***.

While balancing during relax, when the device reevaluates the cell status at the end of each timer interval, it will cease balancing if all cell voltages are within ***Settings:Cell Balancing Config:Cell Balance Stop Delta (Relax)*** of the minimum cell voltage. This ***Cell Balance Stop Delta*** reduces the risk of over-balancing a higher voltage cell to slightly below the minimum voltage cell, and thereby slowly draining the pack. Operation while balancing during charge is similar, instead using the ***Settings:Cell Balancing Config:Cell Balance Stop Delta (Charge)*** configuration value. The ***Cell Balance Stop Delta*** parameters should be set to a lower level than the ***Cell Balance Min Delta*** parameters, then the device will have a hysteresis that delays restarting balancing until the level of imbalance again exceeds the higher ***Cell Balance Min Delta*** level. Note that when balancing is enabled because at least one cell voltage exceeds ***Cell Balance Min Delta***, the device will still attempt to balance all cells that are above the ***Cell Balance Stop Delta***.

NORMAL versus SLEEP Mode—The BQ769142 device can also be configured to avoid autonomous balancing while in SLEEP mode by clearing the ***Settings:Cell Balancing Config:Balancing Configuration[CB_SLEEP]*** configuration bit. The device can also be prevented from entering SLEEP mode while balancing if the ***Settings:Cell Balancing Config:Balancing Configuration[CB_NOSLEEP]*** bit is set. The functionality based on these bits is described in the table below.

Table 10-3. Cell Balancing CB_SLEEP and CB_NOSLEEP Configuration Settings

CB_SLEEP	CB_NOSLEEP	Description
0	0	Cell balancing is not allowed to occur while in SLEEP mode. If balancing were active when the device entered SLEEP mode, balancing would stop at the end of the present ***Cell Balance Interval*** and could not restart until the device returned to NORMAL mode.
0	1	This setting is not allowed. When CB_NOSLEEP is set, CB_SLEEP should also be set.
1	0	Cell balancing is allowed to begin and continue while the device is in SLEEP mode.
1	1	If the device is in SLEEP mode and cell balancing is deemed necessary, the device will exit SLEEP mode to begin balancing. The device is prevented from re-entering SLEEP mode while balancing is active.

Note

Balancing is disabled immediately (without waiting for the interval timer to expire) if any of the following events occur:

- The device enters CONFIG_UPDATE mode.
- An enabled protection alert from ***Settings:Protections:Enabled Protections A*** occurs.
- An enabled protection fault from ***Settings:Protections:Enabled Protections A*** occurs except for a COV fault.
- An enabled Permanent Fail fault occurs.
- The device enters DEEPSLEEP mode.
- The device enters SHUTDOWN mode.

To disable autonomous cell balancing, the ***Settings:Cell Balancing Config:Balancing Configuration[CB_CHG]*** and ***Settings:Cell Balancing Config:Balancing Configuration[CB_RLX]*** configuration bits should be cleared.

Cell voltage measurements cannot be performed while balancing is underway, due to the IR drop across the external cell input resistors significantly reducing the voltage at the device VC pins. Therefore, the device autonomously interrupts balancing briefly to allow cell voltage measurements to occur. During a measurement scan, the device disables balancing on any cell being measured, as well as any cell adjacent to that cell. Balancing is also disabled on the top cell while the top-of-stack voltage is being measured.

The COV and CUV protection checks for each cell normally operate every 3.3 ms when balancing is not enabled. In order to avoid balancing causing a protection alert or fault, the device disables the typical COV and CUV protection schedule while balancing is active. Every 1 second while balancing is active, the device briefly stops balancing of all cells, allows all COV and CUV protection checks to occur, then re-starts balancing again.

The device draws current through the VC14 pin to enable the balancing switches when balancing is active, resulting in approximately 35 uA flowing into the VC14 pin times the number of cells being balanced. In order to avoid this current affecting the cell 14 voltage measurements while balancing is active, it is recommended to minimize the cell 14 input resistor to reduce the IR drop across this resistor.

10.2 Cell Balancing Timing

Due to the current that flows into the cell input pins on the BQ769142 device while balancing is active, the measurement of cell voltages and evaluation of cell voltage protections by the device is modified during balancing. During the regular measurement loop, balancing is temporarily disabled on the cell that is being measured by the ADC. Balancing is also temporarily disabled on the cells adjacent to the cell being measured. Similarly, balancing on the top cell is disabled while the stack voltage measurement is underway. This occurs on every measurement loop, and so can result in significant reduction in the average balancing current that flows. In order to help alleviate this, the ***Settings:Configuration:Power Config[CB_LOOP_SLOW_1:0]*** configuration bits cause the device to slow the measurement loop speed when cell balancing is active, as shown below. The BQ769142 device will insert current-only measurements after each voltage and temperature scan loop to slow down voltage measurements and thereby increase the average balancing current.

Table 10-4. Cell Balancing Loop Slow-Down Setting

CB_LOOP_SLOW_1	CB_LOOP_SLOW_0	Description
0	0	Measurement loop runs at full speed during balancing.
0	1	Measurement loop runs at half speed during balancing.
1	0	Measurement loop runs at quarter speed during balancing.
1	1	Measurement loop runs at eighth speed during balancing.

Note that the ***[LOOP_SLOW]*** and ***[CB_LOOP_SLOW]*** settings operate independently. The ***[LOOP_SLOW]*** setting determines the speed of the regular measurement loop while balancing is not active. The ***[CB_LOOP_SLOW]*** setting determines the speed of the regular measurement loop only while balancing is active (the two settings do not combine together during balancing).

In order to avoid the balancing current causing a protection alert or fault, the device modifies the timing on the CUV check on an actively balanced cell and the COV checks on adjacent cells, disabling balancing briefly every 1 second to allow these checks to occur. If a CUV or COV alert is detected at the 1-s check, balancing is immediately disabled. Note: the device will therefore have a different delay (≈1 second) in triggering a CUV or COV alert or fault on these cells while balancing is active. Timing for CUV and COV on other cells besides these being actively balanced or adjacent are not modified.

The device includes an internal die temperature check to disable balancing if the die temperature exceeds a programmable threshold. The customer, however, should still carefully analyze the thermal effect of the balancing on the device in a system. Based on the planned ambient temperature of the device during operation and the thermal properties of the package, the maximum power should be calculated that can be dissipated within the device and still ensure the operation remains within the recommended operating temperature range. The cell balancing configuration can then be determined such that the device power remains below this level by limiting the maximum number of cells that can be balanced simultaneously, or by reducing the balancing current of each cell by appropriate selection of the external resistance in series with each cell.

While autonomous cell balancing is underway, the conditions related to continuing or stopping balancing are reevaluated at each ***Settings:Cell Balancing Config:Cell Balance Interval***. During SLEEP mode, this reevaluation uses the data available at the time, which is only updated every ***Power:Sleep:Voltage Time***. Thus, there may be some delay related to these settings before balancing is changed based on the data.

11.1 Diagnostics Overview

The BQ769142 device includes a suite of diagnostic tests that the system can use to improve operation robustness.

11.2 VREF2 Versus VREF1 Check

The VREF2, which is used by the coulomb counter and LDOs, is measured indirectly using the voltage ADC (which uses VREF1) to measure the REG18 voltage (which is based on VREF2) and can be read back in bytes 0-1 of the *0x0075 DASTATUS5()* subcommand. This command should normally report a value of approximately 29137. If it differs significantly from this, it may indicate that one reference has changed in value significantly relative to the other, meaning reported measurements may no longer be accurate. This ratio is monitored periodically and, if the value is below 26223 or above 32051 for four seconds, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[VREF]*** configuration bit.

11.3 VSS Measurement

The voltage ADC regularly measures the VSS signal and reports the result in bytes 2-3 of the *0x0075 DASTATUS5()* subcommand. This command should normally report a value that is near zero. If it differs significantly from this, it may indicate the ADC input mux has experienced an error, meaning reported measurements may no longer be accurate. This measurement is monitored by the device and, if not as expected, can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[VSSF]*** configuration bit, and the fail threshold and delay are set by ***Permanent Fail:VSSF:Fail Threshold*** and ***Permanent Fail:VSSF:Delay***.

11.4 Top of Stack Measurement Check

The voltage ADC regularly measures the top of stack voltage through an internal divider and reports this in *0x34 Stack Voltage()*. It also compares this measurement to the sum of the individual cell voltage measurements and can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF D[TOSF]*** configuration bit, and the fail threshold and delay are set by ***Permanent Fail:TOS:Threshold*** and ***Permanent Fail:TOSF:Delay***. This check is not performed if the current is beyond ***Power:Sleep:Sleep Current***, in order to avoid false triggers due to a dynamic load.

11.5 LFO Oscillator Monitor

The BQ769142 device includes a separate hardware monitor circuit, which determines if the LFO oscillator frequency deviates excessively from its expected value. If such a deviation is detected, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[LFOF]*** configuration bit.

11.6 Protection Comparator Mux Check

The BQ769142 device implements a periodic check on the input mux for the hardware protection comparator subsystem used for the OV, UV, OCC, OCD1, and OCD2 primary protections. If this check fails, it can trigger a Permanent Fail (PF) and disable the battery pack. This PF can be enabled by setting the ***Settings:Permanent Failure:Enabled PF C[HWMX]*** configuration bit.

11.7 Internal Watchdog Reset

The BQ769142 device integrates an internal watchdog circuit for the internal processor that will trigger a watchdog fault if it is not serviced by the processor at regular intervals. A watchdog fault may occur if the internal processor is unexpectedly halted or overloaded with tasks, such as servicing excessive serial communications. When a watchdog fault occurs, the internal processor is reset, and the *0x12 Battery Status()[WD]* bit will be set after the reset is complete.

There are additional checks performed by the device which can also trigger a watchdog reset. The BQ769142 device incorporates an ADC measurement watchdog, which monitors whether the ADC and coulomb counter measurements are completing as expected, and if not will trigger a watchdog fault. A RAM integrity check is also performed periodically and forces a watchdog reset if corruption is detected. If the device detects a RAM error within a programmable time (set by ***Power:Shutdown:RAM Fail Shutdown Time***) after a watchdog reset, the device enters SHUTDOWN mode instead of resetting to avoid unwanted reset loops in the case of a RAM failure.

11.8 Internal Memory Checks

The BQ769142 device implements a signature check on the instruction ROM for the internal processor at initial power up or upon reset. If this check fails, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF is enabled by setting the ***Settings:Permanent Failure:Enabled PF C[IRMF]*** configuration bit (this bit is enabled by default).

The device also implements a signature check at initial power up or after reset on the internal processor data ROM, which holds default values for the device configuration. If this check fails, the device can trigger a Permanent Fail (PF) and disable the battery pack. This PF is enabled by setting the ***Settings:Permanent Failure:Enabled PF C[DRMF]*** configuration bit (this bit is enabled by default).

The device also implements a signature check at initial power up or after reset on the internal OTP memory, which may contain customer configuration data. If the OTP memory signature check fails, the device will not load customer settings from OTP, it will instead load the default configuration, trigger a Permanent Fail (PF), which keeps the FETs turned off (but will not blow the fuse) and the REG1 LDO disabled. This PF is enabled by setting the ***Settings:Permanent Failure:Enabled PF C[OTPF]*** configuration bit (this bit is enabled by default). Note that the OTP signature does not include the Manufacturing Data (available using the *0x0070 MANU_DATA()* subcommand) nor any PF status data which was previously written to OTP (which is read using the *0x0053 SAVED_PF_STATUS()* subcommand).

The BQ769142 device implements a signature check of the factory trim information within the device after initial powerup and any device reset. If this check fails, the device begins the transition into SHUTDOWN mode.

12.1 Direct Commands

Table 12-1. Direct Commands Table

Command	Name	Units	Type	Access	Description
0x00	Control Status	Hex	H2	Sealed: R/W Unsealed: R/W Full Access: R/W	When read, this command provides device status bits. This command behaves similarly to 0x3E/0x3F when written. When read back immediately after word write, it will return 0xFFA5 once. Subsequent reads will return Control Status. Writing this command is used for legacy auto-detection, and it is not recommended for customers to write to it. Bit descriptions can be found in Control Status Register.
0x02	Safety Alert A	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual alert signals when enabled safety alerts have triggered. Bit descriptions can be found in Safety Alert A Register.
0x03	Safety Status A	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual fault signals when enabled safety faults have triggered. Bit descriptions can be found in Safety Status A Register.
0x04	Safety Alert B	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual alert signals when enabled safety alerts have triggered. Bit descriptions can be found in Safety Alert B Register.
0x05	Safety Status B	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual fault signals when enabled safety faults have triggered. Bit descriptions can be found in Safety Status B Register.
0x06	Safety Alert C	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual alert signals when enabled safety alerts have triggered. Bit descriptions can be found in Safety Alert C Register.
0x07	Safety Status C	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual fault signals when enabled safety faults have triggered. Bit descriptions can be found in Safety Status C Register.
0x0A	PF Alert A	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual alert signals when enabled Permanent Fail alerts have triggered. Bit descriptions can be found in PF Alert A Register.
0x0B	PF Status A	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual fault signals when enabled Permanent Fail faults have triggered. Bit descriptions can be found in PF Status A Register.
0x0C	PF Alert B	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual alert signals when enabled Permanent Fail alerts have triggered. Bit descriptions can be found in PF Alert B Register.
0x0D	PF Status B	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual fault signals when enabled Permanent Fail faults have triggered. Bit descriptions can be found in PF Status B Register.
0x0E	PF Alert C	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual alert signals when enabled Permanent Fail alerts have triggered. Bit descriptions can be found in PF Alert C Register.
0x0F	PF Status C	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual fault signals when enabled Permanent Fail faults have triggered. Bit descriptions can be found in PF Status C Register.
0x10	PF Alert D	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual alert signals when enabled Permanent Fail alerts have triggered. Bit descriptions can be found in PF Alert D Register.

Table 12-1. Direct Commands Table (continued)

Command	Name	Units	Type	Access	Description
0x11	PF Status D	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides individual fault signals when enabled Permanent Fail faults have triggered. Bit descriptions can be found in PF Status D Register.
0x12	Battery Status	Hex	H2	Sealed: R Unsealed: R Full Access: R	Flags related to battery status Bit descriptions can be found in Battery Status Register.
0x14	Cell 1 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 1
0x16	Cell 2 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 2
0x18	Cell 3 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 3
0x1A	Cell 4 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 4
0x1C	Cell 5 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 5
0x1E	Cell 6 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 6
0x20	Cell 7 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 7
0x22	Cell 8 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 8
0x24	Cell 9 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 9
0x26	Cell 10 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 10
0x28	Cell 11 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 11
0x2A	Cell 12 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 12
0x2E	Cell 13 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 13
0x32	Cell 14 Voltage	mV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on cell 14
0x34	Stack Voltage	userV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on top of stack
0x36	PACK Pin Voltage	userV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on PACK pin
0x38	LD Pin Voltage	userV	I2	Sealed: R Unsealed: R Full Access: R	16-bit voltage on LD pin
0x3A	CC2 Current	userA	I2	Sealed: R Unsealed: R Full Access: R	16-bit CC2 current
0x62	Alarm Status	Hex	H2	Sealed: R/W Unsealed: R/W Full Access: R/W	Latched signal used to assert the ALERT pin. Write a bit high to clear the latch. Bit descriptions can be found in Alarm Status Register.

Table 12-1. Direct Commands Table (continued)

Command	Name	Units	Type	Access	Description
0x64	Alarm Raw Status	Hex	H2	Sealed: R Unsealed: R Full Access: R	Unlatched value of flags which can be selected to be latched (using *Alarm Enable()*) and used to assert the ALERT pin. Bit descriptions can be found in Alarm Raw Status Register.
0x66	Alarm Enable	Hex	H2	Sealed: R/W Unsealed: R/W Full Access: R/W	Mask for *Alarm Status()*. Can be written to change during operation to change which alarm sources are enabled. The default value of this parameter is set by ***Settings:Alarm:Default Alarm Mask***. Bit descriptions can be found in Alarm Enable Register.
0x68	Int Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	This is the most recent measured internal die temperature.
0x6A	CFETOFF Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the CFETOFF pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the CFETOFF pin in millivolts.
0x6C	DFETOFF Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the DFETOFF pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the DFETOFF pin in millivolts.
0x6E	ALERT Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the ALERT pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the ALERT pin in millivolts.
0x70	TS1 Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the TS1 pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the TS1 pin in millivolts.
0x72	TS2 Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the TS2 pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the TS2 pin in millivolts.
0x74	TS3 Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the TS3 pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the TS3 pin in millivolts.
0x76	HDQ Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the HDQ pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the HDQ pin in millivolts.
0x78	DCHG Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the DCHG pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the DCHG pin in millivolts.
0x7A	DDSG Temperature	0.1K	I2	Sealed: R Unsealed: R Full Access: R	When the DDSG pin is configured as a thermistor input, this reports its most recent temperature measurement. When configured as ADCIN, this instead reports the measured voltage at the DDSG pin in millivolts.
0x7F	FET Status	Hex	H1	Sealed: R Unsealed: R Full Access: R	Provides flags showing status of FETs and ALERT pin. Bit descriptions can be found in FET Status Register.

12.2 Bitfield Definitions for Direct Commands

12.2.1 Control Status Register

15	14	13	12	11	10	9	8
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0
7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	DEEPSLEEP	LD_TIMEOUT	LD_ON

Description: When read, this command provides device status bits. This command behaves similarly to 0x3E/0x3F when written. When read back immediately after word write, it will return 0xFFA5 once. Subsequent reads will return Control Status. Writing this command is used for legacy auto-detection, and it is not recommended for customers to write to it.

Table 12-2. Control Status Register Field Descriptions

Bit	Field	Description
2	DEEPSLEEP	This bit indicates whether or not the device is in DEEPSLEEP mode. 0 = Device is not in DEEPSLEEP mode. 1 = Device is in DEEPSLEEP mode.
1	LD_TIMEOUT	This bit is set when the Load Detect function has timed out and checking has stopped. 0 = Load Detect function has not timed out or is inactive. 1 = Load Detection function timed out and was deactivated.
0	LD_ON	This bit indicates whether or not the Load Detect pullup was active during the previous LD pin voltage measurement. 0 = LD pullup was not active during the previous LD pin measurement. 1 = LD pullup was active during the previous LD pin measurement.

12.2.2 Safety Alert A Register

7	6	5	4	3	2	1	0
SCD	OCD2	OCD1	OCC	COV	CUV	RSVD_0	RSVD_0

Description: Provides individual alert signals when enabled safety alerts have triggered.

Table 12-3. Safety Alert A Register Field Descriptions

Bit	Field	Description
7	SCD	Short Circuit in Discharge Protection 0 = Alert is not triggered. 1 = Alert is triggered.
6	OCD2	Overcurrent in Discharge 2nd Tier Protection 0 = Alert is not triggered. 1 = Alert is triggered.
5	OCD1	Overcurrent in Discharge 1st Tier Protection 0 = Alert is not triggered. 1 = Alert is triggered.
4	OCC	Overcurrent in Charge Protection 0 = Alert is not triggered. 1 = Alert is triggered.
3	COV	Cell Overvoltage Protection 0 = Alert is not triggered. 1 = Alert is triggered.
2	CUV	Cell Undervoltage Protection 0 = Alert is not triggered. 1 = Alert is triggered.

12.2.3 Safety Status A Register

7	6	5	4	3	2	1	0
SCD	OCD2	OCD1	OCC	COV	CUV	RSVD_0	RSVD_0

Description: Provides individual fault signals when enabled safety faults have triggered.

Table 12-4. Safety Status A Register Field Descriptions

Bit	Field	Description
7	SCD	Short Circuit in Discharge Protection 0 = Fault is not triggered. 1 = Fault is triggered.
6	OCD2	Overcurrent in Discharge 2nd Tier Protection 0 = Fault is not triggered. 1 = Fault is triggered.
5	OCD1	Overcurrent in Discharge 1st Tier Protection 0 = Fault is not triggered. 1 = Fault is triggered.
4	OCC	Overcurrent in Charge Protection 0 = Fault is not triggered. 1 = Fault is triggered.
3	COV	Cell Overvoltage Protection 0 = Fault is not triggered. 1 = Fault is triggered.
2	CUV	Cell Undervoltage Protection 0 = Fault is not triggered. 1 = Fault is triggered.

12.2.4 Safety Alert B Register

7	6	5	4	3	2	1	0
OTF	OTINT	OTD	OTC	RSVD_0	UTINT	UTD	UTC

Description: Provides individual alert signals when enabled safety alerts have triggered.

Table 12-5. Safety Alert B Register Field Descriptions

Bit	Field	Description
7	OTF	FET Overtemperature 0 = Alert is not triggered. 1 = Alert is triggered.
6	OTINT	Internal Overtemperature 0 = Alert is not triggered. 1 = Alert is triggered.
5	OTD	Overtemperature in Discharge 0 = Alert is not triggered. 1 = Alert is triggered.
4	OTC	Overtemperature in Charge 0 = Alert is not triggered. 1 = Alert is triggered.
2	UTINT	Internal Undertemperature 0 = Alert is not triggered. 1 = Alert is triggered.
1	UTD	Undertemperature in Discharge 0 = Alert is not triggered. 1 = Alert is triggered.
0	UTC	Undertemperature in Charge 0 = Alert is not triggered. 1 = Alert is triggered.

12.2.5 Safety Status B Register

7	6	5	4	3	2	1	0
OTF	OTINT	OTD	OTC	RSVD_0	UTINT	UTD	UTC

Description: Provides individual fault signals when enabled safety faults have triggered.

Table 12-6. Safety Status B Register Field Descriptions

Bit	Field	Description
7	OTF	FET Overtemperature 0 = Fault is not triggered. 1 = Fault is triggered.
6	OTINT	Internal Overtemperature 0 = Fault is not triggered. 1 = Fault is triggered.
5	OTD	Overtemperature in Discharge 0 = Fault is not triggered. 1 = Fault is triggered.
4	OTC	Overtemperature in Charge 0 = Fault is not triggered. 1 = Fault is triggered.
2	UTINT	Internal Undertemperature 0 = Fault is not triggered. 1 = Fault is triggered.
1	UTD	Undertemperature in Discharge 0 = Fault is not triggered. 1 = Fault is triggered.
0	UTC	Undertemperature in Charge 0 = Fault is not triggered. 1 = Fault is triggered.

12.2.6 Safety Alert C Register

7	6	5	4	3	2	1	0
OCD3	SCDL	OCDL	COVL	PTOS	RSVD_0	RSVD_0	RSVD_0

Description: Provides individual alert signals when enabled safety alerts have triggered.

Table 12-7. Safety Alert C Register Field Descriptions

Bit	Field	Description
7	OCD3	Overcurrent in Discharge 3rd Tier Protection 0 = Alert is not triggered. 1 = Alert is triggered.
6	SCDL	Short Circuit in Discharge Latch 0 = Alert is not triggered. 1 = Alert is triggered.
5	OCDL	Overcurrent in Discharge Latch 0 = Alert is not triggered. 1 = Alert is triggered.

Table 12-7. Safety Alert C Register Field Descriptions (continued)

Bit	Field	Description
4	COVL	Cell Overvoltage Latch 0 = Alert is not triggered. 1 = Alert is triggered.
3	PTOS	Precharge Timeout Suspend 0 = Precharge timeout protection is not suspended. 1 = Precharge timeout protection is suspended.

12.2.7 Safety Status C Register

7	6	5	4	3	2	1	0
OCD3	SCDL	OCDL	COVL	RSVD_0	PTO	HWDF	RSVD_0

Description: Provides individual fault signals when enabled safety faults have triggered.

Table 12-8. Safety Status C Register Field Descriptions

Bit	Field	Description
7	OCD3	Overcurrent in Discharge 3rd Tier Protection 0 = Fault is not triggered. 1 = Fault is triggered.
6	SCDL	Short Circuit in Discharge Latch 0 = Fault is not triggered. 1 = Fault is triggered.
5	OCDL	Overcurrent in Discharge Latch 0 = Fault is not triggered. 1 = Fault is triggered.
4	COVL	Cell Overvoltage Latch 0 = Fault is not triggered. 1 = Fault is triggered.
2	PTO	Precharge Timeout 0 = Fault is not triggered. 1 = Fault is triggered.
1	HWDF	Host Watchdog Fault 0 = Fault is not triggered. 1 = Fault is triggered.

12.2.8 PF Alert A Register

7	6	5	4	3	2	1	0
CUDEP	SOTF	RSVD_0	SOT	SOCD	SOCC	SOV	SUV

Description: Provides individual alert signals when enabled Permanent Fail alerts have triggered.

Table 12-9. PF Alert A Register Field Descriptions

Bit	Field	Description
7	CUDEP	Copper Deposition Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.

Table 12-9. PF Alert A Register Field Descriptions (continued)

Bit	Field	Description
6	SOTF	Safety Overtemperature FET Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
4	SOT	Safety Overtemperature Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
3	SOCD	Safety Overcurrent in Discharge Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
2	SOCC	Safety Overcurrent in Charge Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
1	SOV	Safety Cell Overvoltage Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
0	SUV	Safety Cell Undervoltage Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.

12.2.9 PF Status A Register

7	6	5	4	3	2	1	0
CUDEP	SOTF	RSVD_0	SOT	SOCD	SOCC	SOV	SUV

Description: Provides individual fault signals when enabled Permanent Fail faults have triggered.

Table 12-10. PF Status A Register Field Descriptions

Bit	Field	Description
7	CUDEP	Copper Deposition Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
6	SOTF	Safety Overtemperature FET Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
4	SOT	Safety Overtemperature Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
3	SOCD	Safety Overcurrent in Discharge Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
2	SOCC	Safety Overcurrent in Charge Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
1	SOV	Safety Cell Overvoltage Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
0	SUV	Safety Cell Undervoltage Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.

12.2.10 PF Alert B Register

7	6	5	4	3	2	1	0
SCDL	RSVD_0	RSVD_0	VIMA	VIMR	2LVL	DFETF	CFETF

Description: Provides individual alert signals when enabled Permanent Fail alerts have triggered.

Table 12-11. PF Alert B Register Field Descriptions

Bit	Field	Description
7	SCDL	Short Circuit in Discharge Latch Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
4	VIMA	Voltage Imbalance Active Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
3	VIMR	Voltage Imbalance at Rest Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
2	2LVL	Second Level Protector Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
1	DFETF	Discharge FET Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
0	CFETF	Charge FET Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.

12.2.11 PF Status B Register

7	6	5	4	3	2	1	0
SCDL	RSVD_0	RSVD_0	VIMA	VIMR	2LVL	DFETF	CFETF

Description: Provides individual fault signals when enabled Permanent Fail faults have triggered.

Table 12-12. PF Status B Register Field Descriptions

Bit	Field	Description
7	SCDL	Short Circuit in Discharge Latch Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
4	VIMA	Voltage Imbalance Active Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
3	VIMR	Voltage Imbalance at Rest Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
2	2LVL	Second Level Protector Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.

Table 12-12. PF Status B Register Field Descriptions (continued)

Bit	Field	Description
1	DFETF	Discharge FET Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
0	CFETF	Charge FET Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.

12.2.12 PF Alert C Register

7	6	5	4	3	2	1	0
RSVD_0	HWMX	VSSF	VREF	LFOF	RSVD_0	RSVD_0	RSVD_0

Description: Provides individual alert signals when enabled Permanent Fail alerts have triggered.

Table 12-13. PF Alert C Register Field Descriptions

Bit	Field	Description
6	HWMX	Hardware Mux Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
5	VSSF	Internal VSS Measurement Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
4	VREF	Internal Voltage Reference Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.
3	LFOF	Internal LFO Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.

12.2.13 PF Status C Register

7	6	5	4	3	2	1	0
CMDF	HWMX	VSSF	VREF	LFOF	IRMF	DRMF	OTPF

Description: Provides individual fault signals when enabled Permanent Fail faults have triggered.

Table 12-14. PF Status C Register Field Descriptions

Bit	Field	Description
7	CMDF	Commanded Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
6	HWMX	Hardware Mux Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
5	VSSF	Internal VSS Measurement Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.

Table 12-14. PF Status C Register Field Descriptions (continued)

Bit	Field	Description
4	VREF	Internal Voltage Reference Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
3	LFOF	Internal LFO Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
2	IRMF	Instruction ROM Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
1	DRMF	Data ROM Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.
0	OTPF	OTP Memory Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.

12.2.14 PF Alert D Register

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	TOSF

Description: Provides individual alert signals when enabled Permanent Fail alerts have triggered.

Table 12-15. PF Alert D Register Field Descriptions

Bit	Field	Description
0	TOSF	Top of Stack vs Cell Sum Permanent Fail 0 = Alert is not triggered. 1 = Alert is triggered.

12.2.15 PF Status D Register

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	TOSF

Description: Provides individual fault signals when enabled Permanent Fail faults have triggered.

Table 12-16. PF Status D Register Field Descriptions

Bit	Field	Description
0	TOSF	Top of Stack vs Cell Sum Permanent Fail 0 = Fault is not triggered. 1 = Fault is triggered.

12.2.16 Battery Status Register

15	14	13	12	11	10	9	8
SLEEP	RSVD_0	SD_CMD	PF	SS	FUSE	SEC1	SEC0

7	6	5	4	3	2	1	0
OTPB	OTPW	COW_CHK	WD	POR	SLEEP_EN	PCHG_MODE	CFGUPDATE

Description: Flags related to battery status

Table 12-17. Battery Status Register Field Descriptions

Bit	Field	Description
15	SLEEP	This bit indicates whether or not the device is presently in SLEEP mode. 0 = Device is not in SLEEP mode. 1 = Device is in SLEEP mode.
13	SD_CMD	This bit is set when shutdown is pending because the command was received or the RST_SHUT pin was asserted for at least one second. 0 = Shutdown due to command or pin is not pending. 1 = Shutdown due to command or pin is pending.
12	PF	This bit indicates whether or not an enabled Permanent Fail fault has triggered. 0 = No Permanent Fail fault has triggered. 1 = At least one Permanent Fail fault has triggered.
11	SS	This bit indicates whether or not an enabled safety fault is triggered. 0 = No safety fault is triggered. 1 = At least one enabled safety fault is triggered.
10	FUSE	This bit reports the most recently observed state of the FUSE pin and is updated every second. 0 = FUSE pin was not asserted by device or secondary protector at last sample. 1 = FUSE pin was asserted by device or secondary protector at last sample.
9–8	SEC1–SEC0	These bits indicate the present security state of the device. When in SEALED mode, device configuration may not be read or written and some commands are restricted. When in UNSEALED mode, device configuration may normally be read and may be written while in CONFIG_UPDATE mode. When in FULLACCESS mode, unrestricted read and write access is allowed and all commands are accepted. Even in FULLACCESS mode, changes to device configuration should only be changed while also in CONFIG_UPDATE mode. 0 = Device has not initialized yet. 1 = Device is in FULLACCESS mode. 2 = Device is in UNSEALED mode. 3 = Device is in SEALED mode.
7	OTPB	This bit indicates whether or not voltage and temperature conditions are valid for OTP programming. During normal operation, this bit will always be set if *Manufacturing Status() [OTPW]* is clear. When entering CONFIG_UPDATE mode, conditions will be checked and this bit will reflect whether or not programming is allowed (*Manufacturing Status()[OTPW]* does not apply in CONFIG_UPDATE mode). Once in CONFIG_UPDATE mode, this bit will not change state since no new measurements are being taken. 0 = OTP writes are allowed. 1 = Writes to OTP are blocked.
6	OTPW	This bit indicates whether or not some data is waiting to be written to OTP during normal operation. This can occur when, for example, configured to Permanent Fail information to OTP. This bit may remain set until conditions for OTP programming are met and all data is programmed. This bit is not set during OTP programming from CONFIG_UPDATE mode. 0 = No writes to OTP are pending. 1 = Writes to OTP are pending.
5	COW_CHK	This bit indicates while cell open-wire checks are occurring. When the feature is disabled, this bit will not set. When the feature is enabled, this bit will set periodically as the checks are performed. 0 = Device is not actively performing a cell open-wire check. 1 = Device is actively performing a cell open-wire check.

Table 12-17. Battery Status Register Field Descriptions (continued)

Bit	Field	Description
4	WD	This bit indicates whether or not the previous device reset was caused by the internal watchdog timer. This is not related to the Host Watchdog protection. 0 = Previous reset was normal. 1 = Previous reset was caused by the watchdog timer.
3	POR	This bit is set when the device fully resets. It is cleared upon exit of CONFIG_UPDATE mode. It can be used by the host to determine if any RAM configuration changes were lost due to a reset. 0 = Full reset has not occurred since last exit of CONFIG_UPDATE mode. 1 = Full reset has occurred since last exit of CONFIG_UPDATE and reconfiguration of any RAM settings is required.
2	SLEEP_EN	This bit indicates whether or not SLEEP mode is allowed based on configuration and commands. The ***Settings:Configuration:Power Config[SLEEP]*** bit sets the default state of this bit. The host may send commands to enable or disable SLEEP mode based on system requirements. When this bit is set, the device may transition to SLEEP mode when other SLEEP criteria are met. 0 = SLEEP mode is disabled by the host. 1 = SLEEP mode is allowed when other SLEEP conditions are met.
1	PCHG_MODE	This bit indicates whether or not the device is in precharge mode. In precharge mode, the PCHG FET is turned on instead of the CHG FET. 0 = Device is not in precharge mode. 1 = Device is in precharge mode.
0	CFGUPDATE	This bit indicates whether or not the device is in CONFIG_UPDATE mode. It will be set after the SET_CFGUPDATE command is received and fully processed. Configuration settings may be changed only while this bit is set. 0 = Device is not in CONFIG_UPDATE mode. 1 = Device is in CONFIG_UPDATE mode.

12.2.17 Alarm Status Register

15	14	13	12	11	10	9	8
SSBC	SSA	PF	MSK_SFALERT	MSK_PFALERT	INITSTART	INITCOMP	RSVD_0
7	6	5	4	3	2	1	0
FULLSCAN	XCHG	XDSG	SHUTV	FUSE	CB	ADSCAN	WAKE

Description: Latched signal used to assert the ALERT pin. Write a bit high to clear the latch.

Table 12-18. Alarm Status Register Field Descriptions

Bit	Field	Description
15	SSBC	This bit is set when a bit is set in *Safety Status B()* or *Safety Status C()*.
14	SSA	This bit is set when a bit is set in *Safety Status A()*.
13	PF	This bit is set when an enabled Permanent Fail fault triggers.
12	MSK_SFALERT	This bit is set when a safety alert is triggered that is also enabled in the corresponding ***Settings:Alarm:SF Alert Mask A***, ***Settings:Alarm:SF Alert Mask B***, or ***Settings:Alarm:SF Alert Mask C*** register.
11	MSK_PFALERT	This bit is set when a Permanent Fail alert is triggered that is also enabled in the corresponding ***Settings:Alarm:PF Alert Mask A***, ***Settings:Alarm:PF Alert Mask B***, ***Settings:Alarm:PF Alert Mask C***, or ***Settings:Alarm:PF Alert Mask D*** register.
10	INITSTART	Initialization started (sets quickly after device powers up).
9	INITCOMP	Initialization completed (sets after the device has powered and completed one measurement scan).

Table 12-18. Alarm Status Register Field Descriptions (continued)

Bit	Field	Description
7	FULLSCAN	Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltag emeasurement loop data (including cell voltages, pin or thermistor voltages, etc). This bit sets each time a full scan completes (when enabled).
6	XCHG	This bit is set when the CHG FET is off.
5	XDSG	This bit is set when the DSG FET is off.
4	SHUTV	Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage***.
3	FUSE	FUSE Pin Driven. FUSE pin is being driven by either the device or the secondary protector.
2	CB	This bit is set when cell balancing is active.
1	ADSCAN	Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets each time a scan completes (when enabled).
0	WAKE	This bit is set when the device is wakened from SLEEP mode.

12.2.18 Alarm Raw Status Register

15	14	13	12	11	10	9	8
SSBC	SSA	PF	MSK_SFALERT	MSK_PFALERT	INITSTART	INITCOMP	RSVD_0
7	6	5	4	3	2	1	0
FULLSCAN	XCHG	XDSG	SHUTV	FUSE	CB	ADSCAN	WAKE

Description: Unlatched value of flags which can be selected to be latched (using *Alarm Enable()*) and used to assert the ALERT pin.

Table 12-19. Alarm Raw Status Register Field Descriptions

Bit	Field	Description
15	SSBC	This bit is set when a bit is set in *Safety Status B()* or *Safety Status C()*.
14	SSA	This bit is set when a bit is set in *Safety Status A()*.
13	PF	This bit is set when an enabled Permanent Fail fault triggers.
12	MSK_SFALERT	This bit is set when a safety alert is triggered that is also enabled in the corresponding ***Settings:Alarm:SF Alert Mask A***, ***Settings:Alarm:SF Alert Mask B***, or ***Settings:Alarm:SF Alert Mask C*** register.
11	MSK_PFALERT	This bit is set when a Permanent Fail alert is triggered that is also enabled in the corresponding ***Settings:Alarm:PF Alert Mask A***, ***Settings:Alarm:PF Alert Mask B***, ***Settings:Alarm:PF Alert Mask C***, or ***Settings:Alarm:PF Alert Mask D*** register.
10	INITSTART	Initialization started (sets quickly after device powers up).
9	INITCOMP	Initialization completed (sets after the device has powered and completed one measurement scan).
7	FULLSCAN	Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltage measurement loop data (including cell voltages, pin or thermistor voltages, etc). This bit sets after the first full scan completes, then remains set.
6	XCHG	This bit is set when the CHG FET is off.
5	XDSG	This bit is set when the DSG FET is off.
4	SHUTV	Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage***.
3	FUSE	FUSE Pin Driven. FUSE pin is being driven by either the device or the secondary protector.
2	CB	This bit is set when cell balancing is active.
1	ADSCAN	Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets after the first ADC scan completes, then remains set.
0	WAKE	This bit is set when the device is wakened from SLEEP mode.

12.2.19 Alarm Enable Register

15	14	13	12	11	10	9	8
SSBC	SSA	PF	MSK_SFALERT	MSK_PFALERT	INITSTART	INITCOMP	RSVD_0
7	6	5	4	3	2	1	0
FULLSCAN	XCHG	XDSG	SHUTV	FUSE	CB	ADSCAN	WAKE

Description: Mask for *Alarm Status()*. Can be written to change during operation to change which alarm sources are enabled. The default value of this parameter is set by ***Settings:Alarm:Default Alarm Mask***.

Table 12-20. Alarm Enable Register Field Descriptions

Bit	Field	Description
15	SSBC	Setting this bit causes the *Alarm Status()[SSBC]* to be set and latched when *Alarm Raw Status()[SSBC]* is asserted.
14	SSA	Setting this bit causes the *Alarm Status()[SSA]* to be set and latched when *Alarm Raw Status()[SSA]* is asserted.
13	PF	Setting this bit causes the *Alarm Status()[PF]* to be set and latched when *Alarm Raw Status()[PF]* is asserted.
12	MSK_SFALERT	Setting this bit causes the *Alarm Status()[MSK_SFALERT]* to be set and latched when *Alarm Raw Status()[MSK_SFALERT]* is asserted.
11	MSK_PFALERT	Setting this bit causes the *Alarm Status()[MSK_PFALERT]* to be set and latched when *Alarm Raw Status()[MSK_PFALERT]* is asserted.
10	INITSTART	Setting this bit causes the *Alarm Status()[INITSTART]* to be set and latched when *Alarm Raw Status()[INITSTART]* is asserted.
9	INITCOMP	Setting this bit causes the *Alarm Status()[INITCOMP]* to be set and latched when *Alarm Raw Status()[INITCOMP]* is asserted.
7	FULLSCAN	Setting this bit causes the *Alarm Status()[FULLSCAN]* to be set and latched when *Alarm Raw Status()[FULLSCAN]* is asserted.
6	XCHG	Setting this bit causes the *Alarm Status()[XCHG]* to be set and latched when *Alarm Raw Status()[XCHG]* is asserted.
5	XDSG	Setting this bit causes the *Alarm Status()[XDSG]* to be set and latched when *Alarm Raw Status()[XDSG]* is asserted.
4	SHUTV	Setting this bit causes the *Alarm Status()[SHUTV]* to be set and latched when *Alarm Raw Status()[SHUTV]* is asserted.
3	FUSE	Setting this bit causes the *Alarm Status()[FUSE]* to be set and latched when *Alarm Raw Status()[FUSE]* is asserted.
2	CB	Setting this bit causes the *Alarm Status()[CB]* to be set and latched when *Alarm Raw Status()[CB]* is asserted.
1	ADSCAN	Setting this bit causes the *Alarm Status()[ADSCAN]* to be set and latched when *Alarm Raw Status()[ADSCAN]* is asserted.
0	WAKE	Setting this bit causes the *Alarm Status()[WAKE]* to be set and latched when *Alarm Raw Status()[WAKE]* is asserted.

12.2.20 FET Status Register

7	6	5	4	3	2	1	0
RSVD_0	ALRT_PIN	DDSG_PIN	DCHG_PIN	PDSG_FET	DSG_FET	PCHG_FET	CHG_FET

Description: Provides flags showing status of FETs and ALERT pin.

Table 12-21. FET Status Register Field Descriptions

Bit	Field	Description
6	ALRT_PIN	Indicates the status of the ALERT pin. 0 = The ALERT pin is not asserted. 1 = The ALERT pin is asserted.
5	DDSG_PIN	Indicates the status of the DDSG pin. 0 = The DDSG pin is not asserted. 1 = The DDSG pin is asserted.
4	DCHG_PIN	Indicates the status of the DCHG pin. 0 = The DCHG pin is not asserted. 1 = The DCHG pin is asserted.
3	PDSG_FET	Indicates the status of the PDSG FET. 0 = The PDSG FET is off. 1 = The PDSG FET is on.
2	DSG_FET	Indicates the status of the DSG FET. 0 = The DSG FET is off. 1 = The DSG FET is on.
1	PCHG_FET	Indicates the status of the PCHG FET. 0 = The PCHG FET is off. 1 = The PCHG FET is on.
0	CHG_FET	Indicates the status of the CHG FET. 0 = The CHG FET is off. 1 = The CHG FET is on.

12.3 Command-Only Subcommands

Table 12-22. Command-Only Subcommands

Command	Name	Access	Description
0x000E	EXIT_DEEPSLEEP	Sealed: W Unsealed: W Full Access: W	Exit DEEPSLEEP mode
0x000F	DEEPSLEEP	Sealed: W Unsealed: W Full Access: W	Enter DEEPSLEEP mode. Must be sent twice in a row within 4 s to take effect
0x0010	SHUTDOWN	Sealed: W Unsealed: W Full Access: W	Start SHUTDOWN sequence. Must be sent twice in a row within 4s to take effect if sealed. If sent twice while unsealed, the shutdown delays are skipped.
0x0012	RESET	Sealed: — Unsealed: W Full Access: W	Resets the device
0x001C	PDSGTEST	Sealed: — Unsealed: W Full Access: W	In FET Test mode, toggles the PDSG FET enable
0x001D	FUSE_TOGGLE	Sealed: — Unsealed: W Full Access: W	Toggle FUSE state
0x001E	PCHGTEST	Sealed: — Unsealed: W Full Access: W	In FET Test mode, toggles the PCHG FET enable
0x001F	CHGTEST	Sealed: — Unsealed: W Full Access: W	In FET Test mode, toggles the CHG FET enable
0x0020	DSGTEST	Sealed: — Unsealed: W Full Access: W	In FET Test mode, toggles the DSG FET enable
0x0022	FET_ENABLE	Sealed: — Unsealed: W Full Access: W	Toggle FET_EN in Manufacturing Status. FET_EN = 0 means FET Test Mode. FET_EN = 1 means Firmware FET Control.

Table 12-22. Command-Only Subcommands (continued)

Command	Name	Access	Description
0x0024	PF_ENABLE	Sealed: — Unsealed: W Full Access: W	Toggle PF_EN in Manufacturing Status
0x0030	SEAL	Sealed: — Unsealed: W Full Access: W	Places the device in SEALED mode
0x0082	RESET_PASSQ	Sealed: W Unsealed: W Full Access: W	Resets the integrated charge and timer. Charge resets to 0.5 userAh so that the integer portion is rounded.
0x008A	PTO_RECOVER	Sealed: W Unsealed: W Full Access: W	Triggers recovery from a Precharge Timeout (PTO) safety event. This also resets the timeout timer for an ongoing precharge cycle.
0x0090	SET_CFGUPDATE	Sealed: — Unsealed: W Full Access: W	Enters CONFIG_UPDATE mode
0x0092	EXIT_CFGUPDATE	Sealed: W Unsealed: W Full Access: W	Exits CONFIG_UPDATE mode. This also clears the *Battery Status()[POR]* and *Battery Status()[WD]* bits.
0x0093	DSG_PDSG_OFF	Sealed: W Unsealed: W Full Access: W	Disables DSG and PDSG FET drivers. This subcommand should not be used if the DCHG pin is being used in DCHG mode.
0x0094	CHG_PCHG_OFF	Sealed: W Unsealed: W Full Access: W	Disables CHG and PCHG FET drivers. This subcommand should not be used if the DDSG pin is being used in DDSG mode.
0x0095	ALL_FETS_OFF	Sealed: W Unsealed: W Full Access: W	Disables CHG, DSG, PCHG, and PDSG FET drivers
0x0096	ALL_FETS_ON	Sealed: W Unsealed: W Full Access: W	Allows all four FETs to be on if other safety conditions are met. This clears the states set by the DSG_PDSG_OFF, CHG_PCHG_OFF, and ALL_FETS_OFF commands.
0x0099	SLEEP_ENABLE	Sealed: W Unsealed: W Full Access: W	Enable SLEEP mode. The default is loaded from data memory, after which this command can change the setting.
0x009A	SLEEP_DISABLE	Sealed: W Unsealed: W Full Access: W	Disable SLEEP mode. The default is loaded from data memory, after which this command can change the setting.
0x009B	OCDL_RECOVER	Sealed: W Unsealed: W Full Access: W	Recovers Overcurrent in Discharge Latch (OCDL) in the next execution of the safety engine (about 1 second).
0x009C	SCDL_RECOVER	Sealed: W Unsealed: W Full Access: W	Recovers Short Circuit in Discharge Latch (SCDL) in the next execution of the safety engine (about 1 second).
0x009D	LOAD_DETECT_RESTART	Sealed: W Unsealed: W Full Access: W	Restarts the timeout on the Load Detect (LD) pin current source if it has already triggered
0x009E	LOAD_DETECT_ON	Sealed: W Unsealed: W Full Access: W	Forces the Load Detect (LD) pin current source to be ON. This command has no effect when the device is configured for autonomous control of the current source (***Protections:Load Detect:Active Time*** > 0).
0x009F	LOAD_DETECT_OFF	Sealed: W Unsealed: W Full Access: W	Force the Load Detect (LD) pin current source to be OFF. This command has no effect when the device is configured for autonomous control of the current source (***Protections:Load Detect:Active Time*** > 0).
0x2800	CFETOFF_LO	Sealed: W Unsealed: W Full Access: W	Drives the CFETOFF pin to a low state if it is configured as a GPO
0x2801	DFETOFF_LO	Sealed: W Unsealed: W Full Access: W	Drives the DFETOFF pin to a low state if it is configured as a GPO
0x2802	ALERT_LO	Sealed: W Unsealed: W Full Access: W	Drives the ALERT pin to a low state if it is configured as a GPO
0x2806	HDQ_LO	Sealed: W Unsealed: W Full Access: W	Drives the HDQ pin to a low state if it is configured as a GPO

Table 12-22. Command-Only Subcommands (continued)

Command	Name	Access	Description
0x2807	DCHG_LO	Sealed: W Unsealed: W Full Access: W	Drives the DCHG pin to a low state if it is configured as a GPO
0x2808	DDSG_LO	Sealed: W Unsealed: W Full Access: W	Drives the DDSG pin to a low state if it is configured as a GPO
0x2810	CFETOFF_HI	Sealed: W Unsealed: W Full Access: W	Drives the CFETOFF pin to a high state if it is configured as a GPO
0x2811	DFETOFF_HI	Sealed: W Unsealed: W Full Access: W	Drives the DFETOFF pin to a high state if it is configured as a GPO
0x2812	ALERT_HI	Sealed: W Unsealed: W Full Access: W	Drives the ALERT pin to a high state if it is configured as a GPO
0x2816	HDQ_HI	Sealed: W Unsealed: W Full Access: W	Drives the HDQ pin to a high state if it is configured as a GPO.
0x2817	DCHG_HI	Sealed: W Unsealed: W Full Access: W	Drives the DCHG pin to a high state if it is configured as a GPO
0x2818	DDSG_HI	Sealed: W Unsealed: W Full Access: W	Drives the DDSG pin to a high state if it is configured as a GPO
0x2857	PF_FORCE_A	Sealed: W Unsealed: W Full Access: W	First part of two-word command to force the command-based PF. Must be followed by PF_FORCE_B within 4s with no writes in between
0x29A3	PF_FORCE_B	Sealed: W Unsealed: W Full Access: W	Second part of two-word command to force the command-based PF. Must be preceded by PF_FORCE_A within 4 s with no writes in between
0x29BC	SWAP_COMM_MODE	Sealed: — Unsealed: W Full Access: W	Changes to the communications mode previously configured by changing ***Settings:Configuration:Comm Type*** in CONFIG_UPDATE_MODE
0x29E7	SWAP_TO_I2C	Sealed: — Unsealed: W Full Access: W	Selects I^2C Fast mode (***Settings:Configuration:Comm Type*** = 8) in data memory and immediately start using I^2C
0x7C35	SWAP_TO_SPI	Sealed: — Unsealed: W Full Access: W	Selects SPI with CRC mode (***Settings:Configuration:Comm Type*** = 16) in data memory and immediately start using SPI
0x7C40	SWAP_TO_HDQ	Sealed: — Unsealed: W Full Access: W	Selects HDQ using ALERT pin mode (***Settings:Configuration:Comm Type*** = 3) in data memory and immediately start using HDQ

12.4 Subcommands with Data

Table 12-23. Subcommands Table

Command	Name	Access	Offset	Data	Units	Type	Description
0x0001	DEVICE_NUMBER	Sealed: R Unsealed: R Full Access: R	0	Device Number	Hex	U2	Reports the device number that identifies the product. The data is returned in little-endian format.
0x0002	FW_VERSION	Sealed: R Unsealed: R Full Access: R	0	Device Number (Big-Endian)	Hex	U2	Device number in big-endian format for compatibility with legacy products
			2	Firmware Version (Big-Endian)	Hex	U2	Device firmware major and minor version number (Big-Endian)
			4	Build Number (Big-Endian)	Hex	U2	Firmware build number in big-endian, binary-coded decimal format for compatibility with legacy products
0x0003	HW_VERSION	Sealed: R Unsealed: R Full Access: R	0	Hardware Version	Hex	U2	Reports the device hardware version number.
0x0004	IROM_SIG	Sealed: R Unsealed: R Full Access: R	0	Instruction ROM Signature	Hex	U2	Calculates and reports the device instruction ROM signature.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x0005	STATIC_CFG_SIG	Sealed: R Unsealed: R Full Access: R	0	Static Configuration Signature	Hex	U2	The lower 15-bits report the signature of static (non-calibration) configuration data memory. If this does not match the stored ***System Data:Integrity:Config RAM Signature***, the MSBit is set.
0x0007	PREV_MACWRITE	Sealed: R Unsealed: R Full Access: R	0	Previous Mac Write	Hex	U2	Reports the previously written MAC command. This is primarily for use by TI software tools to restore any data after performing background operations.
0x0009	DROM_SIG	Sealed: R Unsealed: R Full Access: R	0	Data ROM Signature	Hex	U2	Calculates and reports the device data ROM signature.
0x0035	SECURITY_KEYS	Sealed: — Unsealed: — Full Access: R/W	0	Unseal Key Step 1	Hex	U2	This is the first word of the security key that must be sent to transition from SEALED to UNSEALED mode.
			2	Unseal Key Step 2	Hex	U2	This is the second word of the security key that must be sent to transition from SEALED to UNSEALED mode. It must be sent within 5 seconds of the first word of the key and with no other commands in between.
			4	Full Access Key Step 1	Hex	U2	This is the second word of the security key that must be sent to transition from UNSEALED to FULLACCESS mode.
			6	Full Access Key Step 2	Hex	U2	This is the second word of the security key that must be sent to transition from UNSEALED to FULLACCESS mode. It must be sent within 5 seconds of the first word of the key and with no other commands in between.
0x0053	SAVED_PF_STATUS	Sealed: R Unsealed: R Full Access: R	0	PF Status A	Hex	U1	Saved Permanent Failure Status A Bit descriptions can be found in PF Status A Register.
			1	PF Status B	Hex	U1	Saved Permanent Failure Status B Bit descriptions can be found in PF Status B Register.
			2	PF Status C	Hex	U1	Saved Permanent Failure Status D Bit descriptions can be found in PF Status C Register.
			3	PF Status D	Hex	U1	Saved Permanent Failure Status D Bit descriptions can be found in PF Status D Register.
			4	Fuse Flag	Hex	U1	This is used to track whether or not the fuse has already been blown. This byte is normally zero but is set to 0x72 after the fuse is blown.
0x0057	MANUFACTURING STATUS	Sealed: R Unsealed: R Full Access: R	0	Manufacturing Status	Hex	H2	Provides flags for use during manufacturing. Bit descriptions can be found in Manufacturing Status Register.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x0070	MANU_DATA	Sealed: R Unsealed: R Full Access: R/W	0	Manufacturer Data 0	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			1	Manufacturer Data 1	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			2	Manufacturer Data 2	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			3	Manufacturer Data 3	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			4	Manufacturer Data 4	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			5	Manufacturer Data 5	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			6	Manufacturer Data 6	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			7	Manufacturer Data 7	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			8	Manufacturer Data 8	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			9	Manufacturer Data 9	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			10	Manufacturer Data 10	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			11	Manufacturer Data 11	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			12	Manufacturer Data 12	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			13	Manufacturer Data 13	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			14	Manufacturer Data 14	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			15	Manufacturer Data 15	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x0070	MANU_DATA	Sealed: R Unsealed: R Full Access: R/W	16	Manufacturer Data 16	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			17	Manufacturer Data 17	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			18	Manufacturer Data 18	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			19	Manufacturer Data 19	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			20	Manufacturer Data 20	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			21	Manufacturer Data 21	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			22	Manufacturer Data 22	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			23	Manufacturer Data 23	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			24	Manufacturer Data 24	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			25	Manufacturer Data 25	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			26	Manufacturer Data 26	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			27	Manufacturer Data 27	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			28	Manufacturer Data 28	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			29	Manufacturer Data 29	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			30	Manufacturer Data 30	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.
			31	Manufacturer Data 31	Hex	U1	Manufacturer Data Scratchpad. Can be configured to save this data to OTP. Must be in FULLACCESS mode to write.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x0071	DASTATUS1	Sealed: R Unsealed: R Full Access: R	0	Cell 1 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			4	Cell 1 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			8	Cell 2 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			12	Cell 2 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			16	Cell 3 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			20	Cell 3 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			24	Cell 4 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			28	Cell 4 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
0x0072	DASTATUS2	Sealed: R Unsealed: R Full Access: R	0	Cell 5 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			4	Cell 5 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			8	Cell 6 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			12	Cell 6 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			16	Cell 7 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			20	Cell 7 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			24	Cell 8 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			28	Cell 8 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
0x0073	DASTATUS3	Sealed: R Unsealed: R Full Access: R	0	Cell 9 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			4	Cell 9 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			8	Cell 10 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			12	Cell 10 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			16	Cell 11 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			20	Cell 11 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			24	Cell 12 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			28	Cell 12 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
0x0074	DASTATUS4	Sealed: R Unsealed: R Full Access: R	8	Cell 13 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			12	Cell 13 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.
			24	Cell 14 Voltage Counts	—	I4	32-bit ADC counts for cell voltage measurement.
			28	Cell 14 Current Counts	—	I4	32-bit ADC counts for current measurement taken during the cell voltage measurement.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x0075	DASTATUS5	Sealed: R Unsealed: R Full Access: R	0	VREG18	—	I2	16-bit ADC count of the VREG18 measurement, which is used as a proxy to check the coulomb counter reference voltage. This is measured for diagnostic purposes.
			2	VSS	—	I2	16-bit ADC count of the VSS pin. This is measured for diagnostic purposes to ensure the ADC input mux is working properly.
			4	Max Cell Voltage	mV	I2	Maximum Cell Voltage
			6	Min Cell Voltage	mV	I2	Minimum Cell Voltage
			8	Battery Voltage Sum	userV	I2	Sum of cell voltages (including interconnects). This can be compared to the *Stack Voltage()* for diagnostic purposes. Note, however, that these measurements are taken at different times which may cause variation.
			10	Cell Temperature	0.1K	I2	Reports the cell temperature being used for features depending on a single temperature threshold. Note many features (such as protections) use minimum or maximum cell temperature instead.
			12	FET Temperature	0.1K	I2	Reports the FET temperature given by the maximum of all measured FET temperatures.
			14	Max Cell Temperature	0.1K	I2	Reports the maximum of all measured cell temperatures.
			16	Min Cell Temperature	0.1K	I2	Reports the minimum of all measured cell temperatures.
			18	Avg Cell Temperature	0.1K	I2	Reports the average of all measured cell temperatures.
			20	CC3 Current	userA	I2	Reports the CC3 Current, which is obtained by averaging a configurable number of CC2 current measurements.
			22	CC1 Current	userA	I2	Reports the CC1 current, which is updated every 250 ms in NORMAL mode. In SLEEP mode, this is updated every 4 seconds beginning one second after voltage measurements end. See the documentation on power modes for further details.
			24	CC2 Counts	—	I4	Raw 32-bit count value for the latest CC2 measurement.
			28	CC3 Counts	—	I4	Raw 32-bit count value for the latest CC3 measurement.
0x0076	DASTATUS6	Sealed: R Unsealed: R Full Access: R	0	Accum Charge	userAh	I4	Reports the integer portion of accumulated passed charge in userAmp-hours.
			4	Accum Charge Fraction	—	U4	Reports the fractional portion of accumulated passed charge. This is initialized to 0.5 userAh to facilitate appropriate rounding of the integer portion.
			8	Accum Time	s	U4	Reports the number of seconds over which passed charge has been integrated.
			12	CFETOFF Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the CFETOFF pin.
			16	DFETOFF Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the DFETOFF pin.
			20	ALERT Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the ALERT pin.
			24	TS1 Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the TS1 pin.
			28	TS2 Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the TS2 pin.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x0077	DASTATUS7	Sealed: R Unsealed: R Full Access: R	0	TS3 Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the TS3 pin.
			4	HDQ Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the HDQ pin.
			8	DCHG Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the DCHG pin.
			12	DDSG Counts	—	I4	Reports the 32-bit ADC counts for the most recent measurement on the DDSG pin.
0x0080	CUV_SNAPSHOT	Sealed: R Unsealed: R Full Access: R	0	Cell 1 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			2	Cell 2 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			4	Cell 3 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			6	Cell 4 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			8	Cell 5 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			10	Cell 6 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			12	Cell 7 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			14	Cell 8 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			16	Cell 9 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			18	Cell 10 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			20	Cell 11 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			22	Cell 12 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			26	Cell 13 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.
			30	Cell 14 Voltage at CUV Event	mV	I2	Records the cell voltage measurement made just after the latest CUV event.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x0081	COV_SNAPSHOT	Sealed: R Unsealed: R Full Access: R	0	Cell 1 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			2	Cell 2 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			4	Cell 3 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			6	Cell 4 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			8	Cell 5 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			10	Cell 6 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			12	Cell 7 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			14	Cell 8 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			16	Cell 9 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			18	Cell 10 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			20	Cell 11 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			22	Cell 12 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			26	Cell 13 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
			30	Cell 14 Voltage at COV Event	mV	I2	Records the cell voltage measurement made just after the latest COV event.
0x0083	CB_ACTIVE_CELLS	Sealed: R/W Unsealed: R/W Full Access: R/W	0	Cell Balancing Active Cells	—	U2	When read, reports a bit mask of which cells are being actively balanced. When written, starts balancing on the specified cells. Bits 0–11 correspond to cell-1 through cell-12. Bit 13 corresponds to cell-13, bit 15 corresponds to cell-14. Bits 12 and 14 should only be written with a "0".Write 0x0000 to turn all balancing off.
0x0084	CB_SET_LVL	Sealed: W Unsealed: W Full Access: W	0	Cell Balancing Set Level	mV	I2	Start balancing cells that are above the written voltage threshold. This will not balance adjacent cells or more cells than the programmed limit.
0x0085	CBSTATUS1	Sealed: R Unsealed: R Full Access: R	0	Cell Balancing Present Time	s	U2	Reports the number of seconds that balancing has been continuously active.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x0086	CBSTATUS2	Sealed: R Unsealed: R Full Access: R	0	Cell 1 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			4	Cell 2 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			8	Cell 3 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			12	Cell 4 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			16	Cell 5 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			20	Cell 6 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			24	Cell 7 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			28	Cell 8 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
0x0087	CBSTATUS3	Sealed: R Unsealed: R Full Access: R	0	Cell 9 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			4	Cell 10 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			8	Cell 11 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			12	Cell 12 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			20	Cell 13 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
			28	Cell 14 Total Balancing Time	s	U4	Reports the cumulative number of seconds that balancing has been active on this cell since the last device reset.
0x0097	FET_CONTROL	Sealed: W Unsealed: W Full Access: W	0	FET Control	Hex	H1	Allows host control of individual FET drivers. This subcommand should not be used if the DDSG or DCHG pin is being used in DDSG/DCHG mode. Bit descriptions can be found in FET Control Register.
0x0098	REG12_CONTROL	Sealed: W Unsealed: W Full Access: W	0	REG12 Control	Hex	H1	Changes voltage regulator settings Bit descriptions can be found in REG12 Control Register.
0x00a0	OTP_WR_CHECK	Sealed: — Unsealed: R Full Access: R	0	OTP Write Check Result	Hex	H1	Reports whether or not OTP programming is allowed. Bit descriptions can be found in OTP Write Check Result Register.
			1	OTP Write Check Data Fail Addr	Hex	U2	When data cannot be programmed to OTP because no XOR bits remain, this will contain the address of the first data value which could not be programmed.

Table 12-23. Subcommands Table (continued)

Command	Name	Access	Offset	Data	Units	Type	Description
0x00a1	OTP_WRITE	Sealed: — Unsealed: R Full Access: R	0	OTP Write Result	Hex	H1	Reports whether or not OTP programming is allowed. Bit descriptions can be found in OTP Write Result Register.
			1	OTP Write Data Fail Addr	Hex	U2	When data cannot be programmed to OTP because no XOR bits remain, this will contain the address of the first data value which could not be programmed.
0xf081	READ_CAL1	Sealed: — Unsealed: R Full Access: R	0	Calibration Data Counter	—	I2	Sample counter that is incremented when buffer is updated. Used to ensure unique measurement samples are taken when averaging is required.
			2	CC2 Counts	—	I4	32-bit CC2 Counts from the most recent current measurement.
			6	PACK pin ADC Counts	—	I2	16-bit ADC counts from previous PACK pin voltage measurement.
			8	Top of Stack ADC Counts	—	I2	16-bit ADC counts from previous Top of Stack voltage measurement.
			10	LD pin ADC Counts	—	I2	16-bit ADC counts from previous Top of Stack voltage measurement.
0xf090	CAL_CUV	Sealed: — Unsealed: R Full Access: R	0	CUV Threshold Override	Hex	U2	Calibrates CUV using the top cell input to set ***Calibration:COV:COV Threshold Override***. By using this calibration command, threshold levels between the normal 50-mV steps can be set. Only available in CONFIG_UPDATE mode.
0xf091	CAL_COV	Sealed: — Unsealed: R Full Access: R	0	COV Threshold Override	Hex	U2	Calibrates COV using the top cell input to set ***Calibration:COV:COV Threshold Override***. By using this calibration command, threshold levels between the normal 50-mV steps can be set. Only available in CONFIG_UPDATE mode.

12.5 Bitfield Definitions for Subcommands

12.5.1 PF Status A Register

7	6	5	4	3	2	1	0
CUDEP	SOTF	RSVD_0	SOT	SOCD	SOCC	SOV	SUV

Description: Saved Permanent Failure Status A

Table 12-24. PF Status A Register Field Descriptions

Bit	Field	Description
7	CUDEP	0 = Copper Deposition Permanent Fail did not occur 1 = Copper Deposition Permanent Fail occurred
6	SOTF	0 = Safety FET Overtemperature Permanent Fail did not occur 1 = Safety FET Overtemperature Permanent Fail occurred
4	SOT	0 = Safety Cell Overtemperature Permanent Fail did not occur 1 = Safety Cell Overtemperature Permanent Fail occurred
3	SOCD	0 = Safety Overcurrent in Discharge Permanent Fail did not occur 1 = Safety Overcurrent in Discharge Permanent Fail occurred
2	SOCC	0 = Safety Overcurrent in Charge Permanent Fail did not occur 1 = Safety Overcurrent in Charge Permanent Fail occurred
1	SOV	0 = Safety Cell Overvoltage Permanent Fail did not occur 1 = Safety Cell Overvoltage Permanent Fail occurred

Table 12-24. PF Status A Register Field Descriptions (continued)

Bit	Field	Description
0	SUV	0 = Safety Cell Undervoltage Permanent Fail did not occur 1 = Safety Cell Undervoltage Permanent Fail occurred

12.5.2 PF Status B Register

7	6	5	4	3	2	1	0
SCDL	RSVD_0	RSVD_0	VIMA	VIMR	2LVL	DFETF	CFETF

Description: Saved Permanent Failure Status B

Table 12-25. PF Status B Register Field Descriptions

Bit	Field	Description
7	SCDL	0 = Latched Short Circuit in Discharge Permanent Fail did not occur 1 = Latched Short Circuit in Discharge Permanent Fail occurred
4	VIMA	0 = Voltage Imbalance in Active Permanent Fail did not occur 1 = Voltage Imbalance in Active Permanent Fail occurred
3	VIMR	0 = Voltage Imbalance in Relax Permanent Fail did not occur 1 = Voltage Imbalance in Relax Permanent Fail occurred
2	2LVL	0 = Secondary Protector Permanent Fail did not occur 1 = Secondary Protector Permanent Fail occurred
1	DFETF	0 = DSG FET Fail Permanent Fail did not occur 1 = DSG FET Fail Permanent Fail occurred
0	CFETF	0 = CHG FET Fail Permanent Fail did not occur 1 = CHG FET Fail Permanent Fail occurred

12.5.3 PF Status C Register

7	6	5	4	3	2	1	0
CMDF	HWMX	VSSF	VREF	LFOF	IRMF	DRMF	OTPF

Description: Saved Permanent Failure Status D

Table 12-26. PF Status C Register Field Descriptions

Bit	Field	Description
7	CMDF	0 = Commanded Permanent Fail did not occur 1 = Commanded Permanent Fail occurred
6	HWMX	0 = Protection Comparator MUX Permanent Fail did not occur 1 = Protection Comparator MUX Permanent Fail occurred
5	VSSF	0 = VSS Permanent Fail did not occur 1 = VSS Permanent Fail occurred
4	VREF	0 = VREF Permanent Fail did not occur 1 = VREF Permanent Fail occurred
3	LFOF	0 = Low Frequency Oscillator Monitor Permanent Fail did not occur 1 = Low Frequency Oscillator Monitor Permanent Fail occurred

Table 12-26. PF Status C Register Field Descriptions (continued)

Bit	Field	Description
2	IRMF	0 = Instruction ROM Permanent Fail did not occur 1 = Instruction ROM Permanent Fail occurred
1	DRMF	0 = Data ROM Permanent Fail did not occur 1 = Data ROM Permanent Fail occurred
0	OTPF	0 = OTP Memory Permanent Fail did not occur 1 = OTP Memory Permanent Fail occurred

12.5.4 PF Status D Register

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	TOSF

Description: Saved Permanent Failure Status D

Table 12-27. PF Status D Register Field Descriptions

Bit	Field	Description
0	TOSF	0 = Top-of-Stack Permanent Fail did not occur 1 = Top-of-Stack Permanent Fail occurred

12.5.5 Manufacturing Status Register

15	14	13	12	11	10	9	8
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0

7	6	5	4	3	2	1	0
OTPW_EN	PF_EN	PDSG_TEST	FET_EN	RSVD_0	DSG_TEST	CHG_TEST	PCHG_TEST

Description: Provides flags for use during manufacturing.

Table 12-28. Manufacturing Status Register Field Descriptions

Bit	Field	Description
7	OTPW_EN	This bit enables or disables writes to OTP during normal operation. The device can program bits in OTP when a PF occurs or when the fuse is blown to retain state after a full reset. It also can program MANU_DATA upon request (if in FULLACCESS mode). This bit enables the device to program this runtime data to OTP. Programming will only occur when the stack voltage and temperature are within allowed limits. If this bit is not set, programming may still be done in CONFIG_UPDATE mode. 0 = Device will not program OTP during normal operation 1 = Device may program OTP during normal operation
6	PF_EN	This bit enables or disables Permanent Failure checks. Clearing this bit prevents Permanent Failure from triggering which is useful during manufacturing. 0 = Permanent Failure checks are disabled 1 = Permanent Failure checks are enabled
5	PDSG_TEST	This bit indicates whether the PDSG FET is enabled in FET Test Mode. This bit is controlled using the PDSGTEST() subcommand. 0 = PDSG FET is not enabled in FET Test Mode 1 = PDSG FET is enabled in FET Test Mode

Table 12-28. Manufacturing Status Register Field Descriptions (continued)

Bit	Field	Description
4	FET_EN	This bit enables or disables FET Test mode. In FET Test mode, the FET states are controlled by the FET Test subcommands. This is typically used during manufacturing to test FET circuitry. Note that safety checks still may force FETs off (or for body diode protection, on) in FET Test mode. 0 = Normal FET control is disabled. FET Test mode is enabled. Device will not turn on FETs unless FET Test subcommands instruct it to do so 1 = Normal FET control is enabled. FET Test mode is disabled. Device will ignore FET Test subcommands
2	DSG_TEST	This bit indicates whether the DSG FET is enabled in FET Test Mode. This bit is controlled using the DSGTEST() subcommand. 0 = DSG FET is not enabled in FET Test Mode 1 = DSG FET is enabled in FET Test Mode
1	CHG_TEST	This bit indicates whether the CHG FET is enabled in FET Test Mode. This bit is controlled using the CHGTEST() subcommand. 0 = CHG FET is not enabled in FET Test Mode 1 = CHG FET is enabled in FET Test Mode
0	PCHG_TEST	This bit indicates whether the PCHG FET is enabled in FET Test Mode. This bit is controlled using the PCHGTEST() subcommand. 0 = PCHG FET is not enabled in FET Test Mode 1 = PCHG FET is enabled in FET Test Mode

12.5.6 FET Control Register

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	PCHG_OFF	CHG_OFF	PDSG_OFF	DSG_OFF

Description: Allows host control of individual FET drivers. This subcommand should not be used if the DDSG or DCHG pin is being used in DDSG/DCHG mode.

Table 12-29. FET Control Register Field Descriptions

Bit	Field	Description
3	PCHG_OFF	0 = PCHG FET is allowed to turn on if other conditions are met 1 = PCHG FET driver is forced off
2	CHG_OFF	0 = CHG FET is allowed to turn on if other conditions are met 1 = CHG FET driver is forced off
1	PDSG_OFF	0 = PDSG FET is allowed to turn on if other conditions are met 1 = PDSG FET driver is forced off
0	DSG_OFF	0 = DSG FET is allowed to turn on if other conditions are met 1 = DSG FET driver is forced off

12.5.7 REG12 Control Register

7	6	5	4	3	2	1	0
REG2V_2	REG2V_1	REG2V_0	REG2_EN	REG1V_2	REG1V_1	REG1V_0	REG1_EN

Description: Changes voltage regulator settings

Table 12-30. REG12 Control Register Field Descriptions

Bit	Field	Description
7–5	REG2V_2–REG2V_0	Selects voltage level for REG2 0–3 = 1.8 V 4 = 2.5 V 5 = 3 V 6 = 3.3 V 7 = 5 V
4	REG2_EN	Enables or disables REG2 0 = REG2 Disabled 1 = REG2 Enabled
3–1	REG1V_2–REG1V_0	Selects voltage level for REG1 0–3 = 1.8 V 4 = 2.5 V 5 = 3 V 6 = 3.3 V 7 = 5 V
0	REG1_EN	Enables or disables REG1 0 = REG1 Disabled 1 = REG1 Enabled

12.5.8 OTP Write Check Result Register

7	6	5	4	3	2	1	0
OK	RSVD_0	LOCK	NOSIG	NODATA	HT	LV	HV

Description: Reports whether or not OTP programming is allowed.

Table 12-31. OTP Write Check Result Register Field Descriptions

Bit	Field	Description
7	OK	This bit is set whenever programming conditions are met. None of the other bits will be set when this bit is set. 0 = OTP programming not allowed 1 = OTP programming ok
5	LOCK	The device is not in FULLACCESS and CONFIG_UPDATE mode, or the OTP Lock bit has been set to prevent further modification. 0 = OTP not locked 1 = OTP locked
4	NOSIG	OTP signature cannot be written (indicating that the signature has already been written too many times). 0 = OTP signature can be programmed 1 = OTP signature could not be programmed
3	NODATA	Could not program data into OTP (indicating data has been programmed too many times, no XOR bits left). When this bit is set, the following bytes will indicate the address of the first failing parameter. 0 = Data can be programmed into OTP 1 = Data could not be programmed into OTP
2	HT	The measured internal temperature is above the allowed OTP programming temperature range. 0 = Temperature is within the allowed range 1 = Temperature is too high to program OTP

Table 12-31. OTP Write Check Result Register Field Descriptions (continued)

Bit	Field	Description
1	LV	The measured stack voltage is below the allowed OTP programming voltage. 0 = The measured stack voltage is above the minimum OTP programming voltage 1 = The measured stack voltage is below the minimum OTP programming voltage
0	HV	The measured stack voltage is above the allowed OTP programming voltage. 0 = The measured stack voltage is below the maximum OTP programming voltage 1 = The measured stack voltage is above the maximum OTP programming voltage

12.5.9 OTP Write Result Register

7	6	5	4	3	2	1	0
OK	RSVD_0	LOCK	NOSIG	NODATA	HT	LV	HV

Description: Reports whether or not OTP programming is allowed.

Table 12-32. OTP Write Result Register Field Descriptions

Bit	Field	Description
7	OK	This bit is set whenever programming conditions are met. None of the other bits will be set when this one is. 0 = OTP programming not allowed 1 = OTP programming ok
5	LOCK	The device is not in FULLACCESS and CONFIG_UPDATE mode, or the OTP Lock bit has been set to prevent further modification. 0 = OTP not locked 1 = OTP locked
4	NOSIG	Signature cannot be written (indicating that the signature has already been written too many times). 0 = OTP signature can be programmed 1 = OTP signature could not be programmed
3	NODATA	Could not program OTP data (indicating data has been programmed too many times, no XOR bits left). When this bit is set, the following bytes will indicate the address of the first failing parameter. 0 = Data can be programmed 1 = Data could not be programmed
2	HT	The measured internal temperature is above the allowed OTP programming temperature range. 0 = Temperature is within the allowed range 1 = Temperature is too high to program OTP
1	LV	The measured stack voltage is below the allowed OTP programming voltage. 0 = The measured stack voltage is above the minimum OTP programming voltage 1 = The measured stack voltage is below the minimum OTP programming voltage
0	HV	The measured stack voltage is above the allowed OTP programming voltage. 0 = The measured stack voltage is below the maximum OTP programming voltage 1 = The measured stack voltage is above the maximum OTP programming voltage

13.1 Data Memory Access

The data memory values in BQ769142 are accessed in similar fashion to subcommands, using the address for a data value rather than the subcommand address. For example, to write the ***Calibration:Voltage:Cell 1 Gain*** to a value of 12410 (0x307A), determine the register address from the Data Memory Summary Table, which shows this address is 0x9180. Then the data is written as shown below:

1. Write lower byte of address to 0x3E (0x80 in this example).
2. Write upper byte of address to 0x3F (0x91 in this example).
3. Write the data memory value in little endian format into the transfer buffer (0x40 to 0x5F). Note: up to 32 bytes of data memory can be written in one block write. In this example, write 0x7A to 0x40, write 0x30 to 0x41.
4. Write the checksum of data written (0x44 in this example) into 0x60, and the length of data (0x06 in this example) into 0x61.
5. The data can be verified by reading it back. Write the lower byte of address to 0x3E (0x80), write the upper byte of address to 0x3F (0x91).
6. Read the length of response from 0x61. The transfer buffer will be populated with a 32-byte block of data, so length will be 36-bytes, or 0x24 for this example.
7. Read buffer starting at 0x40 for the length of data. The new value for ***Calibration:Voltage:Cell 1 Gain*** is seen in 0x40 (0x7A) and 0x41 (0x30).
8. Read the checksum at 0x60 and verify it matches the data read for the full transfer buffer.

Note: 0x61 provides the length of the buffer data + 4 (that is, length of buffer data + length of 0x3E and 0x3F + length of 0x60 and 0x61).

The checksum is calculated over 0x3E and 0x3F and the buffer data, it does not include the checksum or length in 0x60 and 0x61.

The configuration settings for the BQ769142 device are shown in the following sections.

13.2 Calibration

13.2.1 Calibration:Voltage

13.2.1.1 Calibration:Voltage:Cell 1 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 1 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.2 Calibration:Voltage:Cell 2 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 2 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.3 Calibration:Voltage:Cell 3 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 3 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.4 Calibration:Voltage:Cell 4 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 4 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.5 Calibration:Voltage:Cell 5 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 5 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.6 Calibration:Voltage:Cell 6 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 6 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.7 Calibration:Voltage:Cell 7 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 7 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.8 Calibration:Voltage:Cell 8 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 8 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.9 Calibration:Voltage:Cell 9 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 9 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.10 Calibration:Voltage:Cell 10 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 10 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.11 Calibration:Voltage:Cell 11 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 11 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.12 Calibration:Voltage:Cell 12 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 12 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.13 Calibration:Voltage:Cell 13 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 13 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.14 Calibration:Voltage:Cell 14 Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Cell 14 Gain	I2	–32767	32767	0	—

Description: Cell voltage calculations use a linear gain set by this value. Gain is factory-calibrated but can be modified by adjusting this value. While in CONFIG_UPDATE mode, this value will reflect the programmed setting. While not in CONFIG_UPDATE mode, this value will reflect the value that is being used in calculations.

0 = Use factory-calibrated value.

All other values = Use specified value.

13.2.1.15 Calibration:Voltage:Pack Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	Pack Gain	U2	0	65535	0	—

Description: The PACK pin voltage calculation uses a linear gain set by this value.

13.2.1.16 Calibration:Voltage:TOS Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	TOS Gain	U2	0	65535	0	—

Description: The Top-of-Stack voltage calculation uses a linear gain set by this value.

13.2.1.17 Calibration:Voltage:LD Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	LD Gain	U2	0	65535	0	—

Description: The LD pin voltage calculation uses a linear gain set by this value.

13.2.1.18 Calibration:Voltage:ADC Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Voltage	ADC Gain	I2	–32767	32767	0	—

Description: Pins configured as ADCIN use this linear gain value to convert ADC counts to millivolts.

13.2.2 Calibration:Current

13.2.2.1 Calibration:Current:CC Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current	CC Gain	F4	1.00E–02	10.00E+02	7.4768	—

Description: This parameter sets the gain factor used to convert coulomb counter raw count measurements to current. The value is given by

Calibration:Current:CC Gain = 7.4768 / (Rsense in mOhm)

This value should be adjusted based on the sense resistor value in the system and can be further calibrated, if desired.

13.2.2.2 Calibration:Current:Capacity Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current	Capacity Gain	F4	2.98262E+03	4.193046E+08	2230042.463	—

Description: This parameter sets the gain factor used to convert coulomb counter raw count measurements to passed charge. The value is given by

Calibration:Current:Capacity Gain = ***Calibration:Current:CC Gain*** x 298261.6178

This should be adjusted based on the sense resistor value in the system and can be further calibrated, if desired.

13.2.3 Calibration:Vcell Offset

13.2.3.1 Calibration:Vcell Offset:Vcell Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Vcell Offset	Vcell Offset	I2	–32767	32767	0	mV

Description: This offset is subtracted from all cell voltage measurement values and can be used to calibrate out offset error.

13.2.4 Calibration:V Divider Offset

13.2.4.1 Calibration:V Divider Offset:Vdiv Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	V Divider Offset	Vdiv Offset	I2	–32767	32767	0	userV

Description: This offset is subtracted from all *Stack Voltage()*, *PACK Pin Voltage()*, and *LD Pin Voltage()* measurements and can be used to calibrate out offset error.

13.2.5 Calibration:Current Offset

13.2.5.1 Calibration:Current Offset:Coulomb Counter Offset Samples

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current Offset	Coulomb Counter Offset Samples	U2	0	65535	64	—

Description: Sets the scale of ***Calibration:Current Offset:Board Offset***. That parameter is defined as how many counts of offset error would accumulate over this many coulomb counter conversions.

13.2.5.2 Calibration:Current Offset:Board Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current Offset	Board Offset	I2	–32768	32767	0	—

Description: This board-level offset is subtracted from the coulomb counter conversion results in current calculations. To enable higher-resolution calibration, this value is divided by ***Calibration:Current Offset:Coulomb Counter Offset Samples*** before being used. This enables subtraction of fractional-count offsets.

13.2.6 Calibration:Temperature

13.2.6.1 Calibration:Temperature:Internal Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	Internal Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to internal temperature measurements to increase accuracy.

13.2.6.2 Calibration:Temperature:CFETOFF Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	CFETOFF Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.6.3 Calibration:Temperature:DFETOFF Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	DFETOFF Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.6.4 Calibration:Temperature:ALERT Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	ALERT Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.6.5 Calibration:Temperature:TS1 Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	TS1 Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.6.6 Calibration:Temperature:TS2 Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	TS2 Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.6.7 Calibration:Temperature:TS3 Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	TS3 Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.6.8 Calibration:Temperature:HDQ Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	HDQ Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.6.9 Calibration:Temperature:DCHG Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	DCHG Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.6.10 Calibration:Temperature:DDSG Temp Offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Temperature	DDSG Temp Offset	I1	–128	127	0	0.1°C

Description: This offset is added to temperature measurements when this pin is used as a thermistor and a polynomial is enabled. This is not applied if the pin is configured as ADCIN or when using no polynomial.

13.2.7 Calibration:Internal Temp Model

13.2.7.1 Calibration:Internal Temp Model:Int Gain

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Internal Temp Model	Int Gain	I2	–32768	32767	25390	—

Description: The internal temperature calculation uses a linear gain set by this value.

13.2.7.2 Calibration:Internal Temp Model:Int base offset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Internal Temp Model	Int base offset	I2	–32768	32767	3032	—

Description: The internal temperature calculation adds this offset to the result after gain is applied.

13.2.7.3 Calibration:Internal Temp Model:Int Maximum AD

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Internal Temp Model	Int Maximum AD	I2	–32768	32767	16383	—

Description: The internal temperature calculation accuracy is limited when counts exceed a certain value. When the counts are greater than that value, a fixed value is reported for internal temperature. This parameter specifies that threshold. This value should not normally be changed.

13.2.7.4 Calibration:Internal Temp Model:Int Maximum Temp

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Internal Temp Model	Int Maximum Temp	I2	0	32767	6379	0.1K

Description: When the internal temperature ADC measurement's counts exceed ***Calibration:Internal Temp Model:Int Maximum AD***, this temperature is reported for internal temperature. This value should not normally be changed.

13.2.8 Calibration:18K Temperature Model

13.2.8.1 Calibration:18K Temperature Model:Coeff a1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff a1	I2	–32768	32767	–15524	—

Description: This is the coefficient of the 4th power element of the first temperature polynomial.

13.2.8.2 Calibration:18K Temperature Model:Coeff a2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff a2	I2	–32768	32767	26423	—

Description: This is the coefficient of the 3rd power element of the first temperature polynomial.

13.2.8.3 Calibration:18K Temperature Model:Coeff a3

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff a3	I2	–32768	32767	–22664	—

Description: This is the coefficient of the 2nd power element of the first temperature polynomial.

13.2.8.4 Calibration:18K Temperature Model:Coeff a4

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff a4	I2	–32768	32767	28834	—

Description: This is the coefficient of the 1st power element of the first temperature polynomial.

13.2.8.5 Calibration:18K Temperature Model:Coeff a5

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff a5	I2	–32768	32767	672	—

Description: This is the coefficient of the 0th power element of the first temperature polynomial.

13.2.8.6 Calibration:18K Temperature Model:Coeff b1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff b1	I2	–32768	32767	–371	—

Description: This is the coefficient of the 3rd power element of the second temperature polynomial.

13.2.8.7 Calibration:18K Temperature Model:Coeff b2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff b2	I2	–32768	32767	708	—

Description: This is the coefficient of the 2nd power element of the second temperature polynomial.

13.2.8.8 Calibration:18K Temperature Model:Coeff b3

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff b3	I2	–32768	32767	–3498	—

Description: This is the coefficient of the 1st power element of the second temperature polynomial.

13.2.8.9 Calibration:18K Temperature Model:Coeff b4

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Coeff b4	I2	–32768	32767	5051	—

Description: This is the coefficient of the 0th power element of the second temperature polynomial.

13.2.8.10 Calibration:18K Temperature Model:Adc0

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	18K Temperature Model	Adc0	I2	–32768	32767	11703	—

Description: Temperature correction factor corresponding to actual ADC measurement at the calibration temperature, with a scale factor included. With the thermistor attached to TS1 at the calibration temperature, the TS1 Raw ADC Counts (in 32-bit format) is divided by 256, then multiplied by 5/3, and used for this setting.

13.2.9 Calibration:180K Temperature Model

13.2.9.1 Calibration:180K Temperature Model:Coeff a1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff a1	I2	–32768	32767	–17513	—

Description: This is the coefficient of the 4th power element of the first temperature polynomial.

13.2.9.2 Calibration:180K Temperature Model:Coeff a2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff a2	I2	–32768	32767	25759	—

Description: This is the coefficient of the 3rd power element of the first temperature polynomial.

13.2.9.3 Calibration:180K Temperature Model:Coeff a3

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff a3	I2	–32768	32767	–23593	—

Description: This is the coefficient of the 2nd power element of the first temperature polynomial.

13.2.9.4 Calibration:180K Temperature Model:Coeff a4

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff a4	I2	–32768	32767	32175	—

Description: This is the coefficient of the 1st power element of the first temperature polynomial.

13.2.9.5 Calibration:180K Temperature Model:Coeff a5

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff a5	I2	–32768	32767	2090	—

Description: This is the coefficient of the 0th power element of the first temperature polynomial.

13.2.9.6 Calibration:180K Temperature Model:Coeff b1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff b1	I2	–32768	32767	–2055	—

Description: This is the coefficient of the 3rd power element of the second temperature polynomial.

13.2.9.7 Calibration:180K Temperature Model:Coeff b2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff b2	I2	–32768	32767	2955	—

Description: This is the coefficient of the 2nd power element of the second temperature polynomial.

13.2.9.8 Calibration:180K Temperature Model:Coeff b3

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff b3	I2	–32768	32767	–3427	—

Description: This is the coefficient of the 1st power element of the second temperature polynomial.

13.2.9.9 Calibration:180K Temperature Model:Coeff b4

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Coeff b4	I2	–32768	32767	4385	—

Description: This is the coefficient of the 0th power element of the second temperature polynomial.

13.2.9.10 Calibration:180K Temperature Model:Adc0

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	180K Temperature Model	Adc0	I2	–32768	32767	17246	—

Description: Temperature correction factor corresponding to actual ADC measurement at the calibration temperature, with a scale factor included. With the thermistor attached to TS1 at the calibration temperature, the TS1 Raw ADC Counts (in 32-bit format) is divided by 256, then multiplied by 5/3, and used for this setting.

13.2.10 Calibration:Custom Temperature Model

13.2.10.1 Calibration:Custom Temperature Model:Coeff a1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff a1	I2	–32768	32767	0	—

Description: This is the coefficient of the 4th power element of the first temperature polynomial.

13.2.10.2 Calibration:Custom Temperature Model:Coeff a2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff a2	I2	–32768	32767	0	—

Description: This is the coefficient of the 3rd power element of the first temperature polynomial.

13.2.10.3 Calibration:Custom Temperature Model:Coeff a3

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff a3	I2	–32768	32767	0	—

Description: This is the coefficient of the 2nd power element of the first temperature polynomial.

13.2.10.4 Calibration:Custom Temperature Model:Coeff a4

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff a4	I2	–32768	32767	0	—

Description: This is the coefficient of the 1st power element of the first temperature polynomial.

13.2.10.5 Calibration:Custom Temperature Model:Coeff a5

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff a5	I2	–32768	32767	0	—

Description: This is the coefficient of the 0th power element of the first temperature polynomial.

13.2.10.6 Calibration:Custom Temperature Model:Coeff b1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff b1	I2	–32768	32767	0	—

Description: This is the coefficient of the 3rd power element of the second temperature polynomial.

13.2.10.7 Calibration:Custom Temperature Model:Coeff b2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff b2	I2	–32768	32767	0	—

Description: This is the coefficient of the 2nd power element of the second temperature polynomial.

13.2.10.8 Calibration:Custom Temperature Model:Coeff b3

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff b3	I2	–32768	32767	0	—

Description: This is the coefficient of the 1st power element of the second temperature polynomial.

13.2.10.9 Calibration:Custom Temperature Model:Coeff b4

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Coeff b4	I2	–32768	32767	0	—

Description: This is the coefficient of the 0th power element of the second temperature polynomial.

13.2.10.10 Calibration:Custom Temperature Model:Rc0

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Rc0	I2	–32768	32767	0	—

Description: Temperature correction factor corresponding to ideal ADC measurement at the calibration temperature after scaling by 5/3. For example, using calibration temperature of 25C, assuming thermistor value of 10-kOhm, pull-up resistor of 18-kOhm, this is calculated as Rthermistor / (Rthermistor + Rpull-up) * 32767.

13.2.10.11 Calibration:Custom Temperature Model:Adc0

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Custom Temperature Model	Adc0	I2	–32768	32767	0	—

Description: Temperature correction factor corresponding to actual ADC measurement at the calibration temperature, with a scale factor included. With the thermistor attached to TS1 at the calibration temperature, the TS1 Raw ADC Counts (in 32-bit format) is divided by 256, then multiplied by 5/3, and used for this setting.

13.2.11 Calibration:Current Deadband

13.2.11.1 Calibration:Current Deadband:Coulomb Counter Deadband

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	Current Deadband	Coulomb Counter Deadband	U1	0	255	9	234nV

Description: To enable accurate charge accumulation, a deadband threshold is used to filter out signals below the expected noise floor. When the average coulomb counter output is below the deadband threshold, the charge is discarded instead of accumulated. This normally should not be changed.

13.2.12 Calibration:CUV

13.2.12.1 Calibration:CUV:CUV Threshold Override

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	CUV	CUV Threshold Override	U2	0x0000	0xFFFF	0xFFFF	Hex

Description: By default, CUV uses a threshold code calculated from settings and TI factory trim. These trims may be overridden by customer-calibrated values if extra precision is required. The CAL_CUV command performs this calibration and writes this value.

0xffff = Use calculated values based on ***Protections:CUV:Threshold***.

All other values = Use specified threshold code from CAL_CUV command.

13.2.13 Calibration:COV

13.2.13.1 Calibration:COV:COV Threshold Override

Class	Subclass	Name	Type	Min	Max	Default	Unit
Calibration	COV	COV Threshold Override	U2	0x0000	0xFFFF	0xFFFF	Hex

Description: By default, COV uses a threshold code calculated from settings and TI factory trim. These trims may be overridden by customer-calibrated values if extra precision is required. The CAL_COV command performs this calibration and writes this value.

0xffff = Use calculated values based on ***Protections:COV:Threshold***.

All other values = Use specified threshold code from CAL_COV command.

13.3 Settings

13.3.1 Settings:Fuse

13.3.1.1 Settings:Fuse:Min Blow Fuse Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Fuse	Min Blow Fuse Voltage	I2	0	32767	500	10mV

Description: The device will normally attempt to blow the fuse only if the stack voltage is above this threshold. If ***Settings:Protection:Protection Configuration[PACK_FUSE]*** is set, pack voltage is used instead of stack voltage. However, if FET failure (CFETF or DFETF) is detected and ***Settings:Protection:Protection Configuration[FETF_FUSE]*** is set, this voltage threshold is ignored.

13.3.1.2 Settings:Fuse:Fuse Blow Timeout

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Fuse	Fuse Blow Timeout	U1	0	255	30	s

Description: When blowing the fuse, the device will assert the fuse blow output for this duration.

0 = Drive fuse blow output indefinitely (no timeout)

All other values = Drive fuse blow output for this many seconds when blowing the fuse

13.3.2 Settings:Configuration

13.3.2.1 Settings:Configuration:Power Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Power Config	H2	0x0000	0xFFFF	0x2982	Hex

15	14	13	12	11	10	9	8
RSVD_0	RSVD_0	DPSLP_OT	SHUT_TS2	DPSLP_PD	DPSLP_LDO	DPSLP_LFO	SLEEP
7	6	5	4	3	2	1	0
OTSD	FASTADC	CB_LOOP_SLOW_1	CB_LOOP_SLOW_0	LOOP_SLOW_1	LOOP_SLOW_0	WK_SPD_1	WK_SPD_0

Table 13-1. Power Config Register Field Descriptions

Bit	Field	Default	Description
13	DPSLP_OT	1	Enables transition from DEEPSLEEP to SHUTDOWN based on on-chip overtemperature detection. 0 = In DEEPSLEEP, on-chip OT is disabled 1 = On-chip OT is enabled in DEEPSLEEP, allowing transition to SHUTDOWN
12	SHUT_TS2	0	When TS2 is used as a thermistor or has some other external pulldown, SHUTDOWN mode cannot be used. If TS2 is externally pulled down, this bit should be set to prevent the device from immediately exiting SHUTDOWN mode in some circumstances. When this bit is set and SHUTDOWN conditions are met, the device will instead enter a low power state waiting for a rising edge on the LD pin. 0 = Standard SHUTDOWN mode behavior is selected. 1 = SHUTDOWN mode replaced by low-power state waiting for rising edge on LD pin
11	DPSLP_PD	1	Enables wake from DEEPSLEEP based on charger attach. When clear, DEEPSLEEP mode must be exited via host command. 0 = DEEPSLEEP not exited on rising edge on LD pin 1 = A rising edge on the LD pin exits DEEPSLEEP
10	DPSLP_LDO	0	Determines whether or not REG1 and REG2 are disabled in DEEPSLEEP mode 0 = Disables REG1 and REG2 when entering DEEPSLEEP mode 1 = Leaves REG1 and REG2 in present state when entering DEEPSLEEP
9	DPSLP_LFO	0	Determines whether or not to disable the Low Frequency Oscillator in DEEPSLEEP mode to conserve power. 0 = Disables the Low Frequency Oscillator in DEEPSLEEP mode (recommended) 1 = Enables the Low Frequency Oscillator in DEEPSLEEP mode
8	SLEEP	1	Sets the default value of *BatteryStatus()[SLEEP_EN]* which enables or disables SLEEP mode. After initialization, SLEEP_EN can stil be changed via the SLEEP_ENABLE and SLEEP_DISABLE subcommands. 0 = Disables SLEEP mode by default 1 = Enables SLEEP mode by default
7	OTSD	1	Enables or disables the on-chip overtemperature detection circuit to shut down the device in case of a severe on-chip overtemperature condition. 0 = Disables SHUTDOWN from on-chip overtemperature detection circuit (not recommended) 1 = Enters SHUTDOWN mode when an on-chip overtemperature condition is detected

Table 13-1. Power Config Register Field Descriptions (continued)

Bit	Field	Default	Description
6	FASTADC	0	Selects ADC conversion speed for voltage and simultaneous current measurements. Higher speed results in lower accuracy. 0 = 3 ms per conversion 1 = 1.5 ms per conversion
5–4	CB_LOOP_SLOW_1–CB_LOOP_SLOW_0	0	Selects ADC scan loop speed while cell balancing is active by inserting current-only measurements after each voltage and temperature scan loop. This can be used to slow down voltage measurements while balancing to increase the duty-cycle, since balancing must be paused during measurement of the cell. 0 = Full speed 1 = Half speed 2 = Quarter speed 3 = Eighth speed
3–2	LOOP_SLOW_1–LOOP_SLOW_0	0	Selects normal ADC scan loop speed by inserting current-only measurements after each voltage and temperature scan loop. This setting is only used while cell balancing is not active. 0 = Full speed 1 = Half speed 2 = Quarter speed 3 = Eighth speed
1–0	WK_SPD_1–WK_SPD_0	2	Selects the coulomb counter conversion speed used in SLEEP mode for the current wake comparator function. Slower conversion speed results in lower noise. Setting 0x2 may exhibit a large offset and should be avoided. Setting 0x3 results in ~100µV (1-sigma) noise level, so should only be used when the Wake Comparator Current is set to a level such that $\lvert V_{SRP} - V_{SRN} \rvert$ > 1000 µV. 0x0 = 48 ms conversion rate 0x1 = 24 ms conversion rate 0x2 = 12 ms conversion rate 0x3 = 6 ms conversion rate

13.3.2.2 Settings:Configuration:REG12 Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	REG12 Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
REG2V_2	REG2V_1	REG2V_0	REG2_EN	REG1V_2	REG1V_1	REG1V_0	REG1_EN

Description: Configuration options for the voltage regulator outputs

Table 13-2. REG12 Config Register Field Descriptions

Bit	Field	Default	Description
7–5	REG2V_2–REG2V_0	0	Selects voltage level for REG2 This setting should not be changed while REG2 is enabled. 0–3 = 1.8 V 4 = 2.5 V 5 = 3 V 6 = 3.3 V 7 = 5 V
4	REG2_EN	0	Configure default state for REG2 output. This setting is reapplied when initializing after reset or DEEPSLEEP mode. 0 = REG2 Disabled 1 = REG2 Enabled

Table 13-2. REG12 Config Register Field Descriptions (continued)

Bit	Field	Default	Description
3–1	REG1V_2–REG1V_0	0	Selects voltage level for REG1 This setting should not be changed while REG1 is enabled. 0–3 = 1.8 V 4 = 2.5 V 5 = 3 V 6 = 3.3 V 7 = 5 V
0	REG1_EN	0	Configure default state for REG1 output. This setting is reapplied when initializing after reset or DEEPSLEEP mode. 0 = REG1 Disabled 1 = REG1 Enabled

13.3.2.3 Settings:Configuration:REG0 Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	REG0 Config	H1	0x00	0x03	0x00	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD	REG0_EN

Description: REG0 (pre-regulator) can be enabled with this configuration option. This must be enabled if the regulator output is used and REGIN is not supplied externally.

Table 13-3. REG0 Config Register Field Descriptions

Bit	Field	Default	Description
0	REG0_EN	0	Enable or disable pre-regulator for REG1 and REG2 0 = Pre-regulator is disabled 1 = Pre-regulator is enabled

13.3.2.4 Settings:Configuration:HWD Regulator Options

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	HWD Regulator Options	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	TOGGLE_OPT_1	TOGGLE_OPT_0	TOGGLE_TIME_3	TOGGLE_TIME_2	TOGGLE_TIME_1	TOGGLE_TIME_0

Description: Configures the action to be taken when the Host Watchdog protection is triggered. This can be configured turn the REG1 and REG2 output off and on to potentially reset a host microcontroller that has stopped communicating.

Table 13-4. HWD Regulator Options Register Field Descriptions

Bit	Field	Default	Description
5–4	TOGGLE_OPT_1– TOGGLE_OPT_0	0	Action to take when HWD protection is triggered 0 = Take no action on REG1 and REG2 regulators 1 = Turn REG1 and REG2 regulators off 2 = Turn REG1 and REG2 regulators off for configured duration and then back on again 3 = Reserved. Do not use.

Table 13-4. HWD Regulator Options Register Field Descriptions (continued)

Bit	Field	Default	Description
3–0	TOGGLE_TIME_3–TOGGLE_TIME_0	0	How long to keep REG1 and REG2 regulators off when configured to toggle 0 = Turn REG1 and REG2 regulators off and do not turn back on again 1–15 = Turn REG1 and REG2 regulators back on again after this many seconds

13.3.2.5 Settings:Configuration:Comm Type

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Comm Type	U1	0x00	0x1F	0	—

Description: Selects the active communication mode. This mode is applied on reset or when the SWAP_COMM_MODE command is received. The default mode may be different depending on the device version (bq769x2 vs bq769x201 vs bq769x202, etc).

0x00 = Default

0xff = Default

0x03 = HDQ (using ALERT pin)

0x04 = HDQ (using HDQ pin)

0x07 = I^2C (for use up to 100 kHz bus speed)

0x08 = I^2C Fast (for use above 100 kHz bus speed)

0x09 = I^2C Fast with Timeouts (for use above 100 kHz bus speed)

0x0f = SPI

0x10 = SPI with CRC

0x11 = I^2C with CRC (for use up to 100 kHz bus speed)

0x12 = I^2C Fast with CRC (for use above 100 kHz bus speed)

0x1e = I^2C with Timeouts (for use up to 100 kHz bus speed)

All other values = Reserved. Do not use

13.3.2.6 Settings:Configuration:I2C Address

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	I2C Address	U1	0x00	0xFF	0	—

Description: Sets the device address for I^2C-based communication modes. This applied on reset or when SWAP_COMM_MODE subcommand is received.

0 = Use default I^2C device address (0x10)

All other values = Use specified I^2C device address

13.3.2.7 Settings:Configuration:SPI Configuration

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	SPI Configuration	H1	0x00	0x7F	0x20	—

7	6	5	4	3	2	1	0
RSVD_0	MISO_REG1	FILT	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0

Table 13-5. SPI Configuration Register Field Descriptions

Bit	Field	Default	Description
6	MISO_REG1	0	Configures SPI MISO pin to use REG1 output drive level 0 = SPI MISO uses 1.8V output level 1 = SPI MISO uses REG1 output level
5	FILT	1	Configures digital filters on SPI input pins 0 = Disable digital filters on SPI input pins (recommended for high-frequency operation) 1 = Enable digital filters on SPI input pins

13.3.2.8 Settings:Configuration:Comm Idle Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Comm Idle Time	U1	0	255	0	s

Description: Configures the number of seconds to leave the High-Frequency Oscillator enabled after communications. Note that the one-second timer is asynchronous to communications, so the oscillator may turn off up to one second after than this delay. For I^2C, this can reduce clock stretching at the expense of higher power consumption. For SPI, setting this parameter to a nonzero value enables a shorter time between Chip Select assertion and the first clock edge after the first transaction.

0 = High-Frequency Oscillator not left enabled for extra time after communications.

All other values = High-Frequency Oscillator left enabled for up to this many seconds after communications.

13.3.2.9 Settings:Configuration:CFETOFF Pin Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	CFETOFF Pin Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the CFETOFF pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

Table 13-6. CFETOFF Pin Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	0	These bits configure the options for the selected pin function. OPT[5]: --- Polarity when configured for CFETOFF (does not affect GPO mode) --- --- 0 = selects active-high --- --- 1 = selects active-low OPT[4]: --- Unused OPT[3]: --- 0 = output high drive uses REG18 --- 1 = output high drive uses REG1 OPT[2]: --- 0 = weak pull-up to REG1 is disabled --- 1 = weak pull-up to REG1 is enabled --- NOTE - this should not be selected if OPT3=1 OPT[1]: --- 0 = pin drives tri-state when controlled to be driven "hi" (not available when OPT[3] is set) --- 1 = pin drives active-high when controlled to be driven "hi" OPT[0]: --- 0 = weak pulldown to VSS is disabled --- 1 = weak pulldown to VSS is enabled When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	0	These bits configure which function this pin is used for. 0 = SPI_CS or Unused 1 = General Purpose Output 2 = CFETOFF 3 = ADC Input or Thermistor

13.3.2.10 Settings:Configuration:DFETOFF Pin Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	DFETOFF Pin Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the DFETOFF pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

Table 13-7. DFETOFF Pin Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	0	These bits configure the options for the selected pin function. OPT[5]: --- Polarity when configured for DFETOFF (does not affect GPO mode) --- --- 0 = selects active-high --- --- 1 = selects active-low OPT[4]: --- 0 = selects DFETOFF functionality --- 1 = selects BOTHOFF functionality OPT[3]: --- 0 = output high drive uses REG18 --- 1 = output high drive uses REG1 OPT[2]: --- 0 = weak pull-up to REG1 is disabled --- 1 = weak pull-up to REG1 is enabled --- NOTE - this should not be selected if OPT3=1 OPT[1]: --- 0 = pin drives tri-state when controlled to be driven "hi" (not available when OPT[3] is set) --- 1 = pin drives active-high when controlled to be driven "hi" OPT[0]: --- 0 = weak pulldown to VSS is disabled --- 1 = weak pulldown to VSS is enabled When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	0	These bits configure which function this pin is used for. 0 = Unused 1 = General Purpose Output 2 = DFETOFF or BOTHOFF 3 = ADC Input or Thermistor

13.3.2.11 Settings:Configuration:ALERT Pin Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	ALERT Pin Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the ALERT pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

Table 13-8. ALERT Pin Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	0	These bits configure the options for the selected pin function. OPT[5]: --- Polarity when configured for ALERT (does not affect GPO mode) --- --- 0 = selects active-high --- --- 1 = selects active-low OPT[4]: --- Unused OPT[3]: --- 0 = output high drive uses REG18 --- 1 = output high drive uses REG1 OPT[2]: --- 0 = weak pull-up to REG1 is disabled --- 1 = weak pull-up to REG1 is enabled --- NOTE - this should not be selected if OPT3=1 OPT[1]: --- 0 = pin drives tri-state when controlled to be driven "hi" (not available when OPT[3] is set) --- 1 = pin drives active-high when controlled to be driven "hi" OPT[0]: --- 0 = weak pulldown to VSS is disabled --- 1 = weak pulldown to VSS is enabled When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	0	These bits configure which function this pin is used for. 0 = HDQ or Unused 1 = General Purpose Output 2 = ALERT 3 = ADC Input or Thermistor

13.3.2.12 Settings:Configuration:TS1 Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	TS1 Config	H1	0x00	0xFF	0x07	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the TS1 pin functionality.

Table 13-9. TS1 Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	1	The OPT[5:0] bits configure the options for the TS1 pin function. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	3	These bits configure which function this pin is used for. 0 = Unused 1 = Unused 2 = Unused 3 = ADC Input or Thermistor

13.3.2.13 Settings:Configuration:TS2 Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	TS2 Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the TS2 pin functionality.

Table 13-10. TS2 Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	0	The OPT[5:0] bits configure the options for the TS2 pin function. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	0	These bits configure which function this pin is used for. 0 = Unused 1 = Unused 2 = Unused 3 = ADC Input or Thermistor

13.3.2.14 Settings:Configuration:TS3 Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	TS3 Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the TS3 pin functionality.

Table 13-11. TS3 Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	0	The OPT[5:0] bits configure the options for the TS3 pin function. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	0	These bits configure which function this pin is used for. 0 = Unused 1 = Unused 2 = Unused 3 = ADC Input or Thermistor

13.3.2.15 Settings:Configuration:HDQ Pin Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	HDQ Pin Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the HDQ pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

Table 13-12. HDQ Pin Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	0	These bits configure the options for the selected pin function. OPT[5]: --- Polarity when configured for HDQ (does not affect GPO mode) --- --- 0 = selects active-high --- --- 1 = selects active-low OPT[4]: --- Unused OPT[3]: --- 0 = output high drive uses REG18 --- 1 = output high drive uses REG1 OPT[2]: --- 0 = weak pull-up to REG1 is disabled --- 1 = weak pull-up to REG1 is enabled --- NOTE - this should not be selected if OPT3=1 OPT[1]: --- 0 = pin drives tri-state when controlled to be driven "hi" (not available when OPT[3] is set) --- 1 = pin drives active-high when controlled to be driven "hi" OPT[0]: --- 0 = weak pulldown to VSS is disabled --- 1 = weak pulldown to VSS is enabled When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	0	These bits configure which function this pin is used for. 0 = HDQ or SPI_MOSI or Unused 1 = General Purpose Output 2 = Unused 3 = ADC Input or Thermistor

13.3.2.16 Settings:Configuration:DCHG Pin Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	DCHG Pin Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the DCHG pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

Table 13-13. DCHG Pin Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	0	These bits configure the options for the selected pin function. OPT[5]: --- Polarity when configured for DCHG (does not affect GPO mode) --- --- 0 = selects active-high (DCHG is high when CHG is disabled) --- --- 1 = selects active-low (DCHG is low when CHG is disabled) OPT[4]: --- Unused OPT[3]: --- 0 = output high drive uses REG18 --- 1 = output high drive uses REG1 OPT[2]: --- 0 = weak pull-up to REG1 is disabled --- 1 = weak pull-up to REG1 is enabled --- NOTE - this should not be selected if OPT3=1 OPT[1]: --- 0 = pin drives tri-state when controlled to be driven "hi" (not available when OPT[3] is set) --- 1 = pin drives active-high when controlled to be driven "hi" OPT[0]: --- 0 = weak pulldown to VSS is disabled --- 1 = weak pulldown to VSS is enabled When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	0	These bits configure which function this pin is used for. 0 = Unused 1 = General Purpose Output 2 = DCHG 3 = ADC Input or Thermistor

13.3.2.17 Settings:Configuration:DDSG Pin Config

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	DDSG Pin Config	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OPT5	OPT4	OPT3	OPT2	OPT1	OPT0	PIN_FXN1	PIN_FXN0

Description: This parameter configures the DDSG pin functionality. Depending on the pin function selected, the meaning of the OPT bitfield changes.

Table 13-14. DDSG Pin Config Register Field Descriptions

Bit	Field	Default	Description
7–2	OPT5–OPT0	0	These bits configure the options for the selected pin function. OPT[5]: --- Polarity when configured for DDSG (does not affect GPO mode) --- --- 0 = selects active-high (DDSG is high when DSG is disabled) --- --- 1 = selects active-low (DDSG is low when DSG is disabled) OPT[4]: --- Unused OPT[3]: --- 0 = output high drive uses REG18 --- 1 = output high drive uses REG1 OPT[2]: --- 0 = weak pull-up to REG1 is disabled --- 1 = weak pull-up to REG1 is enabled --- NOTE - this should not be selected if OPT3=1 OPT[1]: --- 0 = pin drives tri-state when controlled to be driven "hi" (not available when OPT[3] is set) --- 1 = pin drives active-high when controlled to be driven "hi" OPT[0]: --- 0 = weak pulldown to VSS is disabled --- 1 = weak pulldown to VSS is enabled When a pin is selected for ADCIN or thermistor functionality, the OPT[5:0] bits are used as shown below. OPT[5:4] --- Pull-up control --- --- 00 = selects 18-kOhm pull-up for thermistor measurement --- --- 01 = selects 180-kOhm pull-up for thermistor measurement --- --- 10 = selects no pull-up (used for ADCIN functionality) OPT[3:2] --- Polynomial selection for thermistor temperature measurement --- --- 00 = selects the 18K Temperature Model --- --- 01 = selects the 180K Temperature Model --- --- 10 = selects the Custom Temperature Model --- --- 11 = no polynomial is used, raw ADC counts are reported OPT[1:0] --- Measurement type --- --- 00 = general purpose ADC input --- --- 01 = thermistor temperature measurement, used for cell temperature protections --- --- 10 = thermistor temperature measurement, reported but not used for protections --- --- 11 = thermistor temperature measurement, used for FET temperature protection
1–0	PIN_FXN1–PIN_FXN0	0	These bits configure which function this pin is used for. 0 = Unused 1 = General Purpose Output 2 = DDSG 3 = ADC Input or Thermistor

13.3.2.18 Settings:Configuration:DA Configuration

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	DA Configuration	H1	0x00	0xFF	0x05	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	TINT_FETT	TINT_EN	USER_VOLTS_CV	USER_AMPS_1	USER_AMPS_0

Table 13-15. DA Configuration Register Field Descriptions

Bit	Field	Default	Description
4	TINT_FETT	0	TINT_FETT enables the internal temperature source to be used as the "FET Temperature". TINT_EN must also be set for this to apply. When TINT_EN = 0, this bit is ignored. When configured for FET temperature, it is not factored into minimum, maximum, and average cell temperature calculations. 0 = Internal temperature is not used for "FET Temperature" 1 = Internal temperature is used for "FET Temperature" if TINT_EN is also set
3	TINT_EN	0	TINT_EN enables the internal temperature source to be used as the “Cell Temperature” for protections and logic that use minimum, maximum, or average temperature. 0 = Internal temperature is not used for "Cell Temperature" 1 = Internal temperature is used for "Cell Temperature"
2	USER_VOLTS_CV	1	Some of the BQ769x2 family of devices support high voltages. To ensure the Top-of-Stack, PACK, and LD pin voltages fit in a signed 16-bit integer type, their units are configurable. This configurable unit is called user-volts and can be set to either centivolts or millivolts. For applications which will not exceed 32 Volts, millivolts may be used. Other applications should use centivolts to avoid saturating at 32767 mV. 0 = Millivolt (1 mV) units are selected for user-volts 1 = Centivolt (10 mV) units are selected for user-volts
1–0	USER_AMPS_1–USER_AMPS_0	1	In order to support a wide range of applications, the device allows its units of current to be configurable. This configurable unit is called user-amps and can be mapped to different units of current. This extends the range of the reported 16-bit current to allow it to scale with the anticipated load. 0 = Decimilliamp (0.1 mA) units are selected for user-amps. 1 = Milliamp (1 mA) units are selected for user-amps. 2 = Centiamp (10 mA) units are selected for user-amps. 3 = Deciamp (100 mA) units are selected for user-amps.

13.3.2.19 Settings:Configuration:Vcell Mode

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	Vcell Mode	H2	0x0000	0xFFFF	0x0000	Hex

15	14	13	12	11	10	9	8
Cell 14 Mode	RSVD_0	Cell 13 Mode	RSVD_0	Cell 12 Mode	Cell 11 Mode	Cell 10 Mode	Cell 9 Mode

7	6	5	4	3	2	1	0
Cell 8 Mode	Cell 7 Mode	Cell 6 Mode	Cell 5 Mode	Cell 4 Mode	Cell 3 Mode	Cell 2 Mode	Cell 1 Mode

Description: Not every system will use all of the cell input pins. If the system has fewer cells than the device supports, some VC input pins may be shorted together or used to measure interconnect resistance between cells. To prevent action being taken for cell under-voltage conditions on pins that are shorted or used to measure interconnect resistance, the corresponding Vcell Mode bit should be cleared. If all Vcell Mode bits are cleared, then all inputs are considered as cell connections.

Note

This parameter has been written in OTP by TI with value = 0xAFFF, which modified this parameter from its original hardware default value of 0x0000 (which is shown below). This programming step used one of the eight available OTP signature settings, leaving seven remaining signature settings for customer use. The bits in this parameter programmed by TI to a "1" can be programmed back to a "0" by the customer using the second OTP XOR image, but after that they cannot be changed back to a "1" again.

Table 13-16. Vcell Mode Register Field Descriptions

Bit	Field	Default	Description
15	Cell 14 Mode	0	0 = A cell is not connected between VC14 and VC13. Disable protections on Cell 14. 1 = A cell is connected between VC14 and VC13. Enable protections on Cell 14.
13	Cell 13 Mode	0	0 = A cell is not connected between VC13 and VC12. Disable protections on Cell 13. 1 = A cell is connected between VC13 and VC12. Enable protections on Cell 13.
11	Cell 12 Mode	0	0 = A cell is not connected between VC12 and VC11. Disable protections on Cell 12. 1 = A cell is connected between VC12 and VC11. Enable protections on Cell 12.
10	Cell 11 Mode	0	0 = A cell is not connected between VC11 and VC10. Disable protections on Cell 11. 1 = A cell is connected between VC11 and VC10. Enable protections on Cell 11.
9	Cell 10 Mode	0	0 = A cell is not connected between VC10 and VC9. Disable protections on Cell 10. 1 = A cell is connected between VC10 and VC9. Enable protections on Cell 10.
8	Cell 9 Mode	0	0 = A cell is not connected between VC9 and VC8. Disable protections on Cell 9. 1 = A cell is connected between VC9 and VC8. Enable protections on Cell 9.
7	Cell 8 Mode	0	0 = A cell is not connected between VC8 and VC7. Disable protections on Cell 8. 1 = A cell is connected between VC8 and VC7. Enable protections on Cell 8.
6	Cell 7 Mode	0	0 = A cell is not connected between VC7 and VC6. Disable protections on Cell 7. 1 = A cell is connected between VC7 and VC6. Enable protections on Cell 7.
5	Cell 6 Mode	0	0 = A cell is not connected between VC6 and VC5. Disable protections on Cell 6. 1 = A cell is connected between VC6 and VC5. Enable protections on Cell 6.
4	Cell 5 Mode	0	0 = A cell is not connected between VC5 and VC4. Disable protections on Cell 5. 1 = A cell is connected between VC5 and VC4. Enable protections on Cell 5.
3	Cell 4 Mode	0	0 = A cell is not connected between VC4 and VC3. Disable protections on Cell 4. 1 = A cell is connected between VC4 and VC3. Enable protections on Cell 4.
2	Cell 3 Mode	0	0 = A cell is not connected between VC3 and VC2. Disable protections on Cell 3. 1 = A cell is connected between VC3 and VC2. Enable protections on Cell 3.
1	Cell 2 Mode	0	0 = A cell is not connected between VC2 and VC1. Disable protections on Cell 2. 1 = A cell is connected between VC2 and VC1. Enable protections on Cell 2.
0	Cell 1 Mode	0	0 = A cell is not connected between VC1 and VC0. Disable protections on Cell 1. 1 = A cell is connected between VC1 and VC0. Enable protections on Cell 1.

13.3.2.20 Settings:Configuration:CC3 Samples

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Configuration	CC3 Samples	U1	2	255	80	Num

Description: The device provides an averaged current reading (CC3) over a configurable number of CC2 Current samples. This parameter defines the number of samples that are accumulated before calculating a new average.

13.3.3 Settings:Protection

13.3.3.1 Settings:Protection:Protection Configuration

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Protection Configuration	H2	0x0000	0x07FF	0x0002	Hex

15	14	13	12	11	10	9	8
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	SCDL_CURR_RECOV	OCDL_CURR_RECOV	FETF_FUSE
7	6	5	4	3	2	1	0
PACK_FUSE	RSVD_0	PF_OTP	PF_FUSE	PF_DPSLP	PF_REGS	PF_FETS	RSVD_0

Table 13-17. Protection Configuration Register Field Descriptions

Bit	Field	Default	Description
10	SCDL_CURR_RECOV	0	The SCD Latch fault may recover based on load removal detection on the LD pin, by host command, or by charge current. When the current-based recovery mechanism is not desired, it can be disabled by clearing this bit. 0 = SCDL does not recover based on charge current. 1 = SCDL recovers when current is greater than or equal to ***Protections:SCDL:Recovery Threshold*** for ***Protections:SCDL:Recovery Time***.
9	OCDL_CURR_RECOV	0	The OCD Latch fault may recover based on load removal detection on the LD pin, by host command, or by charge current. When the current-based recovery mechanism is not desired, it can be disabled by clearing this bit. 0 = OCDL does not recover based on charge current. 1 = OCDL recovers when current is greater than or equal to ***Protections:OCDL:Recovery Threshold*** for ***Protections:OCDL:Recovery Time***.
8	FETF_FUSE	0	When a Permanent Failure has been detected, the device may be configured to blow the fuse. This normally requires the voltage being above ***Settings:Fuse:Min Blow Fuse Voltage***. When this bit is set and a FET failure occurs (CFETF or DFETF), the voltage requirement is bypassed. 0 = Voltage must be above a threshold to blow the fuse when CFETF or DFETF trips. 1 = If configured to blow the fuse and CFETF or DFETF occurs, fuse blow is attempted regardless of voltage.
7	PACK_FUSE	0	The fuse is typically located on the BAT side of the FETs, so the device monitors the Top of Stack voltage to determine if fuse blow is possible. However, some systems may place the fuse on the PACK side, in which case the PACK pin voltage should be monitored to determine if fuse blow is possible. Setting this bit causes the device to use the PACK pin voltage instead of the Top of Stack pin voltage for this comparison. 0 = Top of Stack voltage must be above ***Settings:Fuse:Min Blow Fuse Voltage*** in order to blow the fuse. 1 = PACK voltage must be above ***Settings:Fuse:Min Blow Fuse Voltage*** in order to blow the fuse.

Table 13-17. Protection Configuration Register Field Descriptions (continued)

Bit	Field	Default	Description
5	PF_OTP	0	Since the device stores Permanent Failure status in RAM, that status would be lost when the device resets. To mitigate this, the device can write Permanent Failure status to OTP when this bit is set. OTP programming may be delayed in low-voltage and high-temperature conditions until OTP programming can reliably be accomplished. Note that writes to OTP during operation are only allowed if ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is set. If this bit is set but ***Settings:Manufacturing:Mfg Status Init[OTPW_EN]*** is clear, Permanent Failure status is saved to RAM that is preserved across a partial reset but will not be programmed to OTP. If this bit is not set, Permanent Failure status will be lost on any reset, including a partial reset via the RST_SHUT pin. 0 = Permanent Failure status is lost on reset. 1 = Permanent Failure status is preserved across reset when possible.
4	PF_FUSE	0	When a Permanent Failure occurs, the device may be configured to blow the fuse when voltage conditions are met. 0 = Permanent Failure does not cause the device to blow the fuse. 1 = Permanent Failure causes the device to blow the fuse.
3	PF_DPSLP	0	Normally, a Permanent Failure causes the FETs to remain off indefinitely and the fuse may be blown. In that situation, there is no further action that would be taken on further monitoring operations. Additionally, charging would no longer be possible. To avoid rapidly draining the battery, the device may be configured to enter DEEPSLEEP mode when a Permanent Failure occurs. DEEPSLEEP will still be delayed until after fuse blow and OTP programming are completed if those options are enabled. 0 = Device does not automatically enter DEEPSLEEP mode when a Permanent Failure occurs. 1 = Device automatically enters DEEPSLEEP mode when a Permanent Failure occurs.
2	PF_REGS	0	When a Permanent Failure occurs, the device may be configured to either turn the regulators off or to leave them in their present state. Once disabled, they may still be reenabled via command. 0 = Permanent Failure does not cause the device to turn the regulators off. 1 = Permanent Failure causes the device to turn the regulators off.
1	PF_FETS	1	When a Permanent Failure occurs, the device normally will turn the FETs off. An option is provided to disable this behavior if the host wants to maintain greater control. 0 = Permanent Failure does not cause the device to turn the FETs off. 1 = Permanent Failure causes the device to turn the FETs off.

13.3.3.2 Settings:Protection:Enabled Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Enabled Protections A	U1	0x00	0xFF	0x88	Hex

7	6	5	4	3	2	1	0
SCD	OCD2	OCD1	OCC	COV	CUV	RSVD_0	RSVD_0

Description: This bitfield enables or disables various protections. Protections which are enabled will set their corresponding Safety Status flags. Note that ***Settings:Protection:CHG FET Protections A*** and ***Settings:Protection:DSG FET Protections A*** must be appropriately configured to control the FET action taken when these faults are detected.

Table 13-18. Enabled Protections A Register Field Descriptions

Bit	Field	Default	Description
7	SCD	1	Short Circuit in Discharge Protection 0 = Disabled 1 = Enabled
6	OCD2	0	Overcurrent in Discharge 2nd Tier Protection 0 = Disabled 1 = Enabled
5	OCD1	0	Overcurrent in Discharge 1st Tier Protection 0 = Disabled 1 = Enabled
4	OCC	0	Overcurrent in Charge Protection 0 = Disabled 1 = Enabled
3	COV	1	Cell Overvoltage Protection 0 = Disabled 1 = Enabled
2	CUV	0	Cell Undervoltage Protection 0 = Disabled 1 = Enabled

13.3.3.3 Settings:Protection:Enabled Protections B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Enabled Protections B	U1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OTF	OTINT	OTD	OTC	RSVD_0	UTINT	UTD	UTC

Description: This bitfield enables or disables various protections. Protections which are enabled will set their corresponding Safety Status flags. Note that ***Settings:Protection:CHG FET Protections B*** and ***Settings:Protection:DSG FET Protections B*** must be appropriately configured to control the FET action taken when these faults are detected.

Table 13-19. Enabled Protections B Register Field Descriptions

Bit	Field	Default	Description
7	OTF	0	FET Overtemperature 0 = Disabled 1 = Enabled
6	OTINT	0	Internal Overtemperature 0 = Disabled 1 = Enabled
5	OTD	0	Overtemperature in Discharge 0 = Disabled 1 = Enabled
4	OTC	0	Overtemperature in Charge 0 = Disabled 1 = Enabled
2	UTINT	0	Internal Undertemperature 0 = Disabled 1 = Enabled

Table 13-19. Enabled Protections B Register Field Descriptions (continued)

Bit	Field	Default	Description
1	UTD	0	Undertemperature in Discharge 0 = Disabled 1 = Enabled
0	UTC	0	Undertemperature in Charge 0 = Disabled 1 = Enabled

13.3.3.4 Settings:Protection:Enabled Protections C

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Enabled Protections C	U1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
OCD3	SCDL	OCDL	COVL	RSVD	PTO	HWDF	RSVD_0

Description: This bitfield enables or disables various protections. Protections which are enabled will set their corresponding Safety Status flags. Note that ***Settings:Protection:CHG FET Protections C*** and ***Settings:Protection:DSG FET Protections C*** must be appropriately configured to control the FET action taken when these faults are detected.

Table 13-20. Enabled Protections C Register Field Descriptions

Bit	Field	Default	Description
7	OCD3	0	Overcurrent in Discharge 3rd Tier Protection 0 = Disabled 1 = Enabled
6	SCDL	0	Short Circuit in Discharge Latch 0 = Disabled 1 = Enabled
5	OCDL	0	Overcurrent in Discharge Latch 0 = Disabled 1 = Enabled
4	COVL	0	Cell Overvoltage Latch 0 = Disabled 1 = Enabled
2	PTO	0	Precharge Timeout 0 = Disabled 1 = Enabled
1	HWDF	0	Host Watchdog Fault 0 = Disabled 1 = Enabled

13.3.3.5 Settings:Protection:CHG FET Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	CHG FET Protections A	U1	0x00	0xFF	0x98	Hex

7	6	5	4	3	2	1	0
SCD	RSVD_0	RSVD_0	OCC	COV	RSVD_0	RSVD_0	RSVD_0

Description: This bitfield configures which protections will disable the CHG FET. NOTE - For the CHG FET turnoff action to occur immediately when a fault is detected, this value should only be set to 0x98 or 0x18. Setting it to other values can cause FET turnoff action to be delayed by up to 250 ms in NORMAL mode or 1 second in SLEEP mode.

Table 13-21. CHG FET Protections A Register Field Descriptions

Bit	Field	Default	Description
7	SCD	1	Short Circuit in Discharge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
4	OCC	1	Overcurrent in Charge Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
3	COV	1	Cell Overvoltage Protection 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.

13.3.3.6 Settings:Protection:CHG FET Protections B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	CHG FET Protections B	U1	0x00	0xFF	0xD5	Hex

7	6	5	4	3	2	1	0
OTF	OTINT	RSVD_0	OTC	RSVD_0	UTINT	RSVD_0	UTC

Description: This bitfield configures which protections will disable the CHG FET. CHG FET action for any non-reserved bits may be individually selected.

Table 13-22. CHG FET Protections B Register Field Descriptions

Bit	Field	Default	Description
7	OTF	1	FET Overtemperature 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
6	OTINT	1	Internal Overtemperature 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
4	OTC	1	Overtemperature in Charge 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
2	UTINT	1	Internal Undertemperature 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
0	UTC	1	Undertemperature in Charge 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.

13.3.3.7 Settings:Protection:CHG FET Protections C

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	CHG FET Protections C	U1	0x00	0xFF	0x56	Hex

7	6	5	4	3	2	1	0

RSVD_0	SCDL	RSVD_0	COVL	RSVD_0	PTO	HWDF	RSVD_0

Description: This bitfield configures which protections will disable the CHG FET. CHG FET action for any non-reserved bits may be individually selected.

Table 13-23. CHG FET Protections C Register Field Descriptions

Bit	Field	Default	Description
6	SCDL	1	Short Circuit in Discharge Latch 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
4	COVL	1	Cell Overvoltage Latch 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
2	PTO	1	Precharge Timeout 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.
1	HWDF	1	Host Watchdog Fault 0 = CHG FET is not disabled when protection is triggered. 1 = CHG FET is disabled when protection is triggered.

13.3.3.8 Settings:Protection:DSG FET Protections A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	DSG FET Protections A	U1	0x00	0xFF	0xE4	Hex

7	6	5	4	3	2	1	0
SCD	OCD2	OCD1	RSVD_0	RSVD_0	CUV	RSVD_0	RSVD_0

Description: This bitfield configures which protections will disable the DSG FET. NOTE - For the DSG FET turnoff action to occur immediately when a fault is detected, this value should only be set to 0x80 or 0xE4. Setting it to other values can cause FET turnoff action to be delayed by up to 250 ms in NORMAL mode or 1 second in SLEEP mode

Table 13-24. DSG FET Protections A Register Field Descriptions

Bit	Field	Default	Description
7	SCD	1	Short Circuit in Discharge Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
6	OCD2	1	Overcurrent in Discharge 2nd Tier Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
5	OCD1	1	Overcurrent in Discharge 1st Tier Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
2	CUV	1	Cell Undervoltage Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.

13.3.3.9 Settings:Protection:DSG FET Protections B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	DSG FET Protections B	U1	0x00	0xFF	0xE6	Hex

7	6	5	4	3	2	1	0
OTF	OTINT	OTD	RSVD_0	RSVD_0	UTINT	UTD	RSVD_0

Description: This bitfield configures which protections will disable the DSG FET. DSG FET action for any non-reserved bits may be individually selected.

Table 13-25. DSG FET Protections B Register Field Descriptions

Bit	Field	Default	Description
7	OTF	1	FET Overtemperature 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
6	OTINT	1	Internal Overtemperature 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
5	OTD	1	Overtemperature in Discharge 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
2	UTINT	1	Internal Undertemperature 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
1	UTD	1	Undertemperature in Discharge 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.

13.3.3.10 Settings:Protection:DSG FET Protections C

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	DSG FET Protections C	U1	0x00	0xFF	0xE2	Hex

7	6	5	4	3	2	1	0
OCD3	SCDL	OCDL	RSVD_0	RSVD_0	RSVD_0	HWDF	RSVD_0

Description: This bitfield configures which protections will disable the DSG FET. DSG FET action for any non-reserved bits may be individually selected.

Table 13-26. DSG FET Protections C Register Field Descriptions

Bit	Field	Default	Description
7	OCD3	1	Overcurrent in Discharge 3rd Tier Protection 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
6	SCDL	1	Short Circuit in Discharge Latch 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
5	OCDL	1	Overcurrent in Discharge Latch 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.
1	HWDF	1	Host Watchdog Fault 0 = DSG FET is not disabled when protection is triggered. 1 = DSG FET is disabled when protection is triggered.

13.3.3.11 Settings:Protection:Body Diode Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Protection	Body Diode Threshold	I2	0	32767	50	mA

Description: To minimize power dissipation in the FET body diode, the FET is turned on when reverse current is detected and the other FET is on. When measured discharge current is greater in magnitude than ***Settings:Protection:Body Diode Threshold*** and the DSG FET or PDSG FET is on, the CHG FET is turned on, and the PCHG FET is turned off. When measured charge current is greater than ***Settings:Protection:Body Diode Threshold*** and the CHG FET or PCHG FET is on, the DSG FET is turned on, and the PDSG FET is turned off. When in parallel FET mode (***Settings:FET:FET Options[SFET]*** = 0), body diode protection is disabled and a FET will not be turned on in response to reverse current.

13.3.4 Settings:Alarm

13.3.4.1 Settings:Alarm:Default Alarm Mask

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Alarm	Default Alarm Mask	H2	0x0000	0xFFFF	0xF800	Hex

15	14	13	12	11	10	9	8
SSBC	SSA	PF	MSK_SFALERT	MSK_PFALERT	INITSTART	INITCOMP	RSVD_0
7	6	5	4	3	2	1	0
FULLSCAN	XCHG	XDSG	SHUTV	FUSE	CB	ADSCAN	WAKE

Description: This parameter sets the default value of the *AlarmEnable()* register. The default value is reloaded at reset and at exit of CONFIG_UPDATE mode.

Table 13-27. Default Alarm Mask Register Field Descriptions

Bit	Field	Default	Description
15	SSBC	1	This bit is set when a bit is set in *Safety Status B()* or *Safety Status C()*.
14	SSA	1	This bit is set when a bit is set in *Safety Status A()*.
13	PF	1	This bit is set when an enabled Permanent Fail fault triggers.
12	MSK_SFALERT	1	This bit is set when a safety alert is triggered that is also enabled in the corresponding ***Settings:Alarm:SF Alert Mask A***, ***Settings:Alarm:SF Alert Mask B***, or ***Settings:Alarm:SF Alert Mask C*** register.
11	MSK_PFALERT	1	This bit is set when a Permanent Fail alert is triggered that is also enabled in the corresponding ***Settings:Alarm:PF Alert Mask A***, ***Settings:Alarm:PF Alert Mask B***, ***Settings:Alarm:PF Alert Mask C***, or ***Settings:Alarm:PF Alert Mask D*** register.
10	INITSTART	0	Initialization started (sets quickly after device powers up).
9	INITCOMP	0	Initialization completed (sets after the device has powered and completed one measurement scan).
7	FULLSCAN	0	Full Voltage Scan Complete. The necessary multiple ADC scans have been completed to collect the full voltag emeasurement loop data (including cell voltages, pin or thermistor voltages, etc). This bit sets each time a full scan completes (when enabled).
6	XCHG	0	This bit is set when the CHG FET is off.
5	XDSG	0	This bit is set when the DSG FET is off.
4	SHUTV	0	Stack voltage is below ***Power:Shutdown:Shutdown Stack Voltage***.
3	FUSE	0	FUSE Pin Driven. FUSE pin is being driven by either the device or the secondary protector.
2	CB	0	This bit is set when cell balancing is active.

Table 13-27. Default Alarm Mask Register Field Descriptions (continued)

Bit	Field	Default	Description
1	ADSCAN	0	Voltage ADC Scan Complete. A single ADC scan is complete (cell voltages are measured on each scan). This bit sets each time a scan completes (when enabled).
0	WAKE	0	This bit is set when the device is wakened from SLEEP mode.

13.3.4.2 Settings:Alarm:SF Alert Mask A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Alarm	SF Alert Mask A	U1	0x00	0xFF	0xFC	Hex

7	6	5	4	3	2	1	0
SCD	OCD2	OCD1	OCC	COV	CUV	RSVD_0	RSVD_0

Description: This parameter selects which protections influence the setting of *AlarmRawStatus() [MSK_SFALERT]*. When the bitwise and of ***Settings:Alarm:SF Alert Mask A*** and *SafetyAlertA()* is nonzero, *AlarmRawStatus()[MSK_SFALERT]* is set.

13.3.4.3 Settings:Alarm:SF Alert Mask B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Alarm	SF Alert Mask B	U1	0x00	0xFF	0xF7	Hex

7	6	5	4	3	2	1	0
OTF	OTINT	OTD	OTC	RSVD_0	UTINT	UTD	UTC

Description: This parameter selects which protections influence the setting of *AlarmRawStatus() [MSK_SFALERT]*. When the bitwise and of ***Settings:Alarm:SF Alert Mask B*** and *SafetyAlertB()* is nonzero, *AlarmRawStatus()[MSK_SFALERT]* is set.

13.3.4.4 Settings:Alarm:SF Alert Mask C

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Alarm	SF Alert Mask C	U1	0x00	0xFF	0xF4	Hex

7	6	5	4	3	2	1	0
OCD3	SCDL	OCDL	COVL	RSVD_0	PTO	RSVD_1	RSVD_0

Description: This parameter selects which protections influence the setting of *AlarmRawStatus() [MSK_SFALERT]*. When the bitwise and of ***Settings:Alarm:SF Alert Mask C*** and *SafetyAlertC()* is nonzero, *AlarmRawStatus()[MSK_SFALERT]* is set.

13.3.4.5 Settings:Alarm:PF Alert Mask A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Alarm	PF Alert Mask A	U1	0x00	0xFF	0x5F	Hex

7	6	5	4	3	2	1	0
CUDEP	SOTF	RSVD_0	SOT	SOCD	SOCC	SOV	SUV

Description: This parameter selects which protections influence the setting of *AlarmRawStatus() [MSK_PFALERT]*. When the bitwise and of ***Settings:Alarm:PF Alert Mask A*** and *PFAlertA()* is nonzero, *AlarmRawStatus()[MSK_PFALERT]* is set.

13.3.4.6 Settings:Alarm:PF Alert Mask B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Alarm	PF Alert Mask B	U1	0x00	0xFF	0x9F	Hex

7	6	5	4	3	2	1	0
SCDL	RSVD_0	RSVD_0	VIMA	VIMR	2LVL	DFETF	CFETF

Description: This parameter selects which protections influence the setting of *AlarmRawStatus() [MSK_PFALERT]*. When the bitwise and of ***Settings:Alarm:PF Alert Mask B*** and *PFAlertB()* is nonzero, *AlarmRawStatus()[MSK_PFALERT]* is set.

13.3.4.7 Settings:Alarm:PF Alert Mask C

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Alarm	PF Alert Mask C	U1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
RSVD_0	HWMX	VSSF	VREF	LFOF	RSVD_0	RSVD_0	RSVD_0

Description: This parameter selects which protections influence the setting of *AlarmRawStatus() [MSK_PFALERT]*. When the bitwise and of ***Settings:Alarm:PF Alert Mask C*** and *PFAlertC()* is nonzero, *AlarmRawStatus()[MSK_PFALERT]* is set.

13.3.4.8 Settings:Alarm:PF Alert Mask D

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Alarm	PF Alert Mask D	U1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	TOSF

Description: This parameter selects which protections influence the setting of *AlarmRawStatus() [MSK_PFALERT]*. When the bitwise and of ***Settings:Alarm:PF Alert Mask D*** and *PFAlertD()* is nonzero, *AlarmRawStatus()[MSK_PFALERT]* is set.

13.3.5 Settings:Permanent Failure

13.3.5.1 Settings:Permanent Failure:Enabled PF A

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Permanent Failure	Enabled PF A	U1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
CUDEP	SOTF	RSVD_0	SOT	SOCD	SOCC	SOV	SUV

Table 13-28. Enabled PF A Register Field Descriptions

Bit	Field	Default	Description
7	CUDEP	0	Copper Deposition Permanent Fail 0 = Disabled 1 = Enabled

Table 13-28. Enabled PF A Register Field Descriptions (continued)

Bit	Field	Default	Description
6	SOTF	0	Safety Overtemperature FET Permanent Fail 0 = Disabled 1 = Enabled
4	SOT	0	Safety Overtemperature Permanent Fail 0 = Disabled 1 = Enabled
3	SOCD	0	Safety Overcurrent in Discharge Permanent Fail 0 = Disabled 1 = Enabled
2	SOCC	0	Safety Overcurrent in Charge Permanent Fail 0 = Disabled 1 = Enabled
1	SOV	0	Safety Cell Overvoltage Permanent Fail 0 = Disabled 1 = Enabled
0	SUV	0	Safety Cell Undervoltage Permanent Fail 0 = Disabled 1 = Enabled

13.3.5.2 Settings:Permanent Failure:Enabled PF B

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Permanent Failure	Enabled PF B	U1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
SCDL	RSVD_0	RSVD_0	VIMA	VIMR	2LVL	DFETF	CFETF

Table 13-29. Enabled PF B Register Field Descriptions

Bit	Field	Default	Description
7	SCDL	0	Short Circuit in Discharge Latch Permanent Fail 0 = Disabled 1 = Enabled
4	VIMA	0	Voltage Imbalance Active Permanent Fail 0 = Disabled 1 = Enabled
3	VIMR	0	Voltage Imbalance at Rest Permanent Fail 0 = Disabled 1 = Enabled
2	2LVL	0	Second Level Protector Permanent Fail 0 = Disabled 1 = Enabled
1	DFETF	0	Discharge FET Permanent Fail 0 = Disabled 1 = Enabled
0	CFETF	0	Charge FET Permanent Fail 0 = Disabled 1 = Enabled

13.3.5.3 Settings:Permanent Failure:Enabled PF C

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Permanent Failure	Enabled PF C	U1	0x00	0xFF	0x07	Hex

7	6	5	4	3	2	1	0
CMDF	HWMX	VSSF	VREF	LFOF	IRMF	DRMF	OTPF

Table 13-30. Enabled PF C Register Field Descriptions

Bit	Field	Default	Description
7	CMDF	0	Commanded Permanent Fail 0 = Disabled 1 = Enabled
6	HWMX	0	Internal Stuck Hardware Mux Permanent Fail 0 = Disabled 1 = Enabled
5	VSSF	0	Internal VSS Measurement Permanent Fail 0 = Disabled 1 = Enabled
4	VREF	0	Internal Voltage Reference Permanent Fail 0 = Disabled 1 = Enabled
3	LFOF	0	Internal LFO Permanent Fail 0 = Disabled 1 = Enabled
2	IRMF	1	Instruction ROM Permanent Fail 0 = Disabled 1 = Enabled
1	DRMF	1	Data ROM Permanent Fail 0 = Disabled 1 = Enabled
0	OTPF	1	OTP Memory Permanent Fail 0 = Disabled 1 = Enabled

13.3.5.4 Settings:Permanent Failure:Enabled PF D

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Permanent Failure	Enabled PF D	U1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	TOSF

Table 13-31. Enabled PF D Register Field Descriptions

Bit	Field	Default	Description
0	TOSF	0	Top of Stack vs Cell Sum Permanent Fail 0 = Disabled 1 = Enabled

13.3.6 Settings:FET

13.3.6.1 Settings:FET:FET Options

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	FET	FET Options	H1	0x00	0xFF	0x0D	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	FET_INIT_OFF	PDSG_EN	FET_CTRL_EN	HOST_FET_EN	SLEEPCHG	SFET

Table 13-32. FET Options Register Field Descriptions

Bit	Field	Default	Description
5	FET_INIT_OFF	0	The host has the option to send commands to turn the FETs off or allow them to be turned on. This bit may be set for the device to wait for a host command before turning FETs on. 0 = Default host FET control state allows FETs to be on 1 = Default host FET control state forces FETs off
4	PDSG_EN	0	To reduce inrush current when the DSG FET turns on, the PDSG FET can be enabled for a short time first to charge up the load through a higher-resistance path. This bit enables this operation. 0 = PDSG FET is not used 1 = PDSG FET is turned on before DSG
3	FET_CTRL_EN	1	In systems where the device's FET drivers are not used, the charge pump should be disabled in ***Settings:FET:Chg Pump Control*** and this bit should be cleared to prevent the device from attempting to turn the FETs on. 0 = FETs will not be turned on 1 = FETs are controlled by the device
2	HOST_FET_EN	1	Some systems need the ability to override the device's FET control and force the FETs to turn off through commands. If that functionality is not needed, it can be disabled to prevent commands from turning the FETs off. 0 = Host FET control commands are ignored 1 = Host FET control commands are allowed
1	SLEEPCHG	0	The CHG FET can be disabled while in SLEEP mode to conserve power. This bit configures whether or not to allow the CHG FET to be enabled in SLEEP mode. 0 = CHG FET is turned off in SLEEP mode 1 = CHG FET may be enabled in SLEEP mode
0	SFET	1	The device supports both series and parallel FET configurations. When the CHG and DSG FETs are in series, current may flow through the body diode of one of the FETs when the other is enabled. In this configuration, body diode protection is used to turn the FET on when current above a threshold is detected to be flowing through that FET. When the system has separate DSG and CHG paths and parallel FETs, body diode protection is not needed and should be disabled. 0 = Parallel FET mode: Body diode protection is disabled 1 = Series FET mode: Body diode protection is enabled

13.3.6.2 Settings:FET:Chg Pump Control

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	FET	Chg Pump Control	U1	0x00	0xFF	0x01	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	SFMODE_SLEEP	LVEN	CPEN

Table 13-33. Chg Pump Control Register Field Descriptions

Bit	Field	Default	Description
2	SFMODE_SLEEP	0	To conserve power in SLEEP mode, the DSG FET driver may be configured to enter source-follower mode. This is normally only used when ***Settings:FET:FET Options[SLEEPCHG]*** is set to zero. When current is detected by the CC2 Wake Comparator, source-follower mode is disabled and the FET driver operates normally. Source-follower mode is also disabled when SLEEP mode is exited via other means. 0 = Source-follower mode is not enabled on the DSG FET driver 1 = Source-follower mode is enabled on the DSG FET driver while in SLEEP mode
1	LVEN	0	This bit selects the charge pump overdrive level. 0 = Charge pump high overdrive level (11 V) is selected 1 = Charge pump low overdrive level (5.5 V) is selected
0	CPEN	1	This bit enables or disables the charge pumps for the FET drivers. If FET drivers are not to be used at all, ***Settings:FET:FET Options[FET_CTRL_EN]*** should also be set to zero. 0 = Charge pumps for FET drivers are disabled 1 = Charge pumps for FET drivers are enabled

13.3.6.3 Settings:FET:Precharge Start Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	FET	Precharge Start Voltage	I2	0	32767	0	mV

Description: Precharge mode can be used to provide lower-current charging through the PCHG FET instead of the CHG FET for an under-voltage battery. When the minimum cell voltage is less than this threshold, precharge mode is activated. To disable precharge mode, set this value to 0.

13.3.6.4 Settings:FET:Precharge Stop Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	FET	Precharge Stop Voltage	I2	0	32767	0	mV

Description: Precharge mode can be used to provide lower-current charging through the PCHG FET instead of the CHG FET for an under-voltage battery. When the minimum cell voltage is greater than or equal to this threshold, precharge mode is deactivated. To disable precharge mode, set this value to 0.

13.3.6.5 Settings:FET:Predischarge Timeout

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	FET	Predischarge Timeout	U1	0	255	5	10ms

Description: When predischarge mode is enabled, the maxiumum duration of predischarge mode can be set in 10-ms increments.

0 = No timeout. Predischarge mode is exited when voltage conditions are met.

All other values = Predischarge mode is exited and DSG is turned on after configured timeout.

13.3.6.6 Settings:FET:Predischarge Stop Delta

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	FET	Predischarge Stop Delta	U1	0	255	50	10mV

Description: Every 250ms, the device checks the last measured LD pin and top-of-stack voltages if in predischarge mode. Predischarge mode is exited if the voltage on the LD pin is greater than or equal to the top-of-stack voltage minus this delta.

0 = Predischarge voltage check disabled. Predischarge mode is exited for timeout.

All other values = Predischarge mode exited when the LD pin voltage is measured within this delta of the top-of-stack voltage.

13.3.7 Settings:Current Thresholds

13.3.7.1 Settings:Current Thresholds:Dsg Current Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Current Thresholds	Dsg Current Threshold	I2	0	32767	100	userA

Description: Certain device features depend upon whether the system is in a discharge state or not. The system is considered to be discharging when measured negative current is larger in magnitude than this threshold.

13.3.7.2 Settings:Current Thresholds:Chg Current Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Current Thresholds	Chg Current Threshold	I2	0	32767	50	userA

Description: Certain device features depend upon whether the system is in a charging state or not. The system is considered to be charging when measured positive current is larger in magnitude than this threshold.

13.3.8 Settings:Cell Open-Wire

13.3.8.1 Settings:Cell Open-Wire:Check Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Open-Wire	Check Time	U1	0	255	5	s

Description: If a cell connection to the device is detached, the capacitance on the node may maintain the voltage for some time. To detect this condition, the device can periodically enable a current source to VSS on each cell connection to drain the charge on the node. When a cell is detached, that node voltage is discharged, and an over-voltage or under-voltage event will be triggered on that cell or an adjacent cell differential measurement. The current source is enabled for the duration of an ADC measurement (3 ms by default) once per the interval defined by this parameter. A longer interval decreases the average current consumption at the cost of detection time. When using this feature, cell balancing should be considered as well since the current flows from the cell pin to VSS, resulting in a higher average current drawn from lower cells.

0 = Cell open-wire check is disabled.

All other values = Cell open-wire check current source is enabled briefly for each cell on this interval.

13.3.9 Settings:Interconnect Resistances

13.3.9.1 Settings:Interconnect Resistances:Cell 1 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 1 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.2 Settings:Interconnect Resistances:Cell 2 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 2 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.3 Settings:Interconnect Resistances:Cell 3 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 3 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.4 Settings:Interconnect Resistances:Cell 4 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 4 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.5 Settings:Interconnect Resistances:Cell 5 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 5 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.6 Settings:Interconnect Resistances:Cell 6 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 6 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.7 Settings:Interconnect Resistances:Cell 7 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 7 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.8 Settings:Interconnect Resistances:Cell 8 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 8 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.9 Settings:Interconnect Resistances:Cell 9 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 9 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.10 Settings:Interconnect Resistances:Cell 10 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 10 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.11 Settings:Interconnect Resistances:Cell 11 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 11 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.12 Settings:Interconnect Resistances:Cell 12 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 12 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.13 Settings:Interconnect Resistances:Cell 13 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 13 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.9.14 Settings:Interconnect Resistances:Cell 14 Interconnect

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Interconnect Resistances	Cell 14 Interconnect	I2	0	32767	0	mΩ

Description: When a significant interconnect resistance exists between cells, this parameter can be used to account for it in cell voltage measurements. Cell voltage calcualtions utilize the simultaneous current measurement and this resistance value to accurately calculate the cell voltage.

13.3.10 Settings:Manufacturing

13.3.10.1 Settings:Manufacturing:Mfg Status Init

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Manufacturing	Mfg Status Init	H2	0x0000	0xFFFF	0x0040	Hex

15	14	13	12	11	10	9	8
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
OTPW_EN	PF_EN	RSVD_0	FET_EN	RSVD_0	RSVD_0	RSVD_0	RSVD_0

Description: This is the initial Value loaded to Manufacturing Status when the device resets or receives the SEAL or SET_CFGUPDATE commands.

Table 13-34. Mfg Status Init Register Field Descriptions

Bit	Field	Default	Description
7	OTPW_EN	0	This bit enables or disables writes to OTP during operation. The device can program diagnostic information in OTP when a PF occurs or when the fuse is blown to retain state after a full reset. It also can program MANU_DATA upon request (if in FULLACCESS mode). This bit enables the device to program this runtime data to OTP. Programming will only occur when the stack voltage and temperature are within allowed limits. If this bit is not set, programming may still be done in CONFIG_UPDATE mode. 0 = Device will not program OTP during operation. 1 = Device may program OTP during operation.
6	PF_EN	1	This bit enables or disables Permanent Failure checks. Clearing this bit prevents Permanent Failure from triggering which is useful during manufacturing. 0 = Permanent Failure checks are disabled. 1 = Permanent Failure checks are enabled.
4	FET_EN	0	This bit enables or disables FET Test mode. In FET Test mode, the FET states are controlled by the FET Test subcommands. This is typically used during manufacturing to test FET circuitry. Note that safety checks still may force FETs off (or for body diode protection, on) in FET Test mode. 0 = Normal FET control is disabled. FET Test mode is enabled. Device will not turn on FETs unless FET Test subcommands instruct it to do so. 1 = Normal FET control is enabled. FET Test mode is disabled. Device will ignore FET Test subcommands.

13.3.11 Settings:Cell Balancing Config

13.3.11.1 Settings:Cell Balancing Config:Balancing Configuration

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Balancing Configuration	H1	0x00	0xFF	0x00	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	CB_NO_CMD	CB_NOSLEEP	CB_SLEEP	CB_RLX	CB_CHG

Table 13-35. Balancing Configuration Register Field Descriptions

Bit	Field	Default	Description
4	CB_NO_CMD	0	This bit allows blocking of cell balancing commands if host-controlled balancing is not desired. 0 = Host-controlled balancing commands are accepted. 1 = Host-controlled balancing commands are ignored.

Table 13-35. Balancing Configuration Register Field Descriptions (continued)

Bit	Field	Default	Description
3	CB_NOSLEEP	0	This bit configures the device to exit sleep mode to perform cell balancing. When this bit is set, CB_SLEEP should also be set. 0 = SLEEP mode is allowed while cell balancing is active. 1 = SLEEP is prevented while cell balancing is active.
2	CB_SLEEP	0	This bit configures whether or not the device is allowed to perform cell balancing while in SLEEP mode. 0 = Cell balancing is not performed in SLEEP mode. 1 = Cell balancing may be performed while in SLEEP mode.
1	CB_RLX	0	This bit enables cell balancing while current is under ***Settings:Current Thresholds:Chg Current Threshold*** and above -***Settings:Current Thresholds:Dsg Current Threshold***. Note that this only applies to automatic cell balancing. Host-controlled balancing is not affected by this bit. 0 = Cell balancing is not allowed in relax conditions. 1 = Cell balancing is allowed in relax conditions.
0	CB_CHG	0	This bit enables cell balancing while current is above ***Settings:Current Thresholds:Chg Current Threshold***. Note that this only applies to automatic cell balancing. Host-controlled balancing is not affected by this bit. 0 = Cell balancing is not allowed while charging. 1 = Cell balancing is allowed while charging.

13.3.11.2 Settings:Cell Balancing Config:Min Cell Temp

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Min Cell Temp	I1	–128	127	–20	°C

Description: When the minimum cell temperature is below this value, cell balancing is not allowed. This affects both host-controlled balancing and automatic cell balancing.

13.3.11.3 Settings:Cell Balancing Config:Max Cell Temp

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Max Cell Temp	I1	–128	127	60	°C

Description: When the maximum cell temperature is above this value, cell balancing is not allowed. This affects both host-controlled balancing and automatic cell balancing.

13.3.11.4 Settings:Cell Balancing Config:Max Internal Temp

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Max Internal Temp	I1	–128	127	70	°C

Description: When the internal temperature is above this value, cell balancing is not allowed. This affects both host-controlled balancing and automatic cell balancing.

13.3.11.5 Settings:Cell Balancing Config:Cell Balance Interval

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Cell Balance Interval	U1	1	255	20	s

Description: The cell balancing algorithm recalculates which cell to balance after this many seconds. Once a cell is chosen, balancing on that cell will continue for this interval unless one of the conditions which blocks balancing is present. This interval is also used with the commands for host-controlled balancing. A command to balance a cell will keep balancing active for this amount of time. The host may send the command again before the timer expires to reset it and continue balancing.

13.3.11.6 Settings:Cell Balancing Config:Cell Balance Max Cells

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Cell Balance Max Cells	U1	0	16	1	Num

Description: This limits how many cells may be automatically balanced in parallel or balanced via the CB_SET_LVL command. With host-controlled balancing, the host may specify more cells than this and the limit is ignored.

13.3.11.7 Settings:Cell Balancing Config:Cell Balance Min Cell V (Charge)

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Cell Balance Min Cell V (Charge)	I2	0	5000	3900	mV

Description: While charging, automatic cell balancing is disabled if the minimum cell voltage is less than this threshold.

13.3.11.8 Settings:Cell Balancing Config:Cell Balance Min Delta (Charge)

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Cell Balance Min Delta (Charge)	U1	0	255	40	mV

Description: While charging, the delta between the maximum and minimum cell voltages must be greater than this value for automatic cell balancing to begin.

13.3.11.9 Settings:Cell Balancing Config:Cell Balance Stop Delta (Charge)

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Cell Balance Stop Delta (Charge)	U1	0	255	20	mV

Description: While balancing in charge, this value is used as the target voltage delta to balance to. Once the delta between the minimum and maximum cell voltages falls below this threshold, balancing stops. This provides some hysteresis around the delta threshold. Note that to prevent balancing from draining the pack, the stop threshold is calculated when balancing begins and will not decrease if the minimum cell voltage drops. This means that in some conditions, balancing will stop will a greater delta than this.

13.3.11.10 Settings:Cell Balancing Config:Cell Balance Min Cell V (Relax)

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Cell Balance Min Cell V (Relax)	I2	0	5000	3900	mV

Description: While not charging or discharging, automatic cell balancing is disabled if the minimum cell voltage is less than this threshold.

13.3.11.11 Settings:Cell Balancing Config:Cell Balance Min Delta (Relax)

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Cell Balance Min Delta (Relax)	U1	0	255	40	mV

Description: While not charging or discharging, the delta between the maximum and minimum cell voltages must be greater than this value for automatic cell balancing to begin.

13.3.11.12 Settings:Cell Balancing Config:Cell Balance Stop Delta (Relax)

Class	Subclass	Name	Type	Min	Max	Default	Unit
Settings	Cell Balancing Config	Cell Balance Stop Delta (Relax)	U1	0	255	20	mV

Description: While balancing in relax, this value is used as the target voltage delta to balance to. Once the delta between the minimum and maximum cell voltages falls below this threshold, balancing stops. This provides some hysteresis around the delta threshold. Note that to prevent balancing from draining the pack, the stop threshold is calculated when balancing begins and will not decrease if the minimum cell voltage drops. This means that in some conditions, balancing will stop will a greater delta than this.

13.4 Power

13.4.1 Power:Shutdown

13.4.1.1 Power:Shutdown:Shutdown Cell Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Cell Voltage	I2	0	32767	0	mV

Description: Configures the cell voltage threshold at which the device will enter SHUTDOWN mode. This threshold does not apply to VC pins configured as interconnects.

Note: Consider setting this parameter to zero if the cell open wire feature is enabled, since an open wire will result in a low voltage on the disconnected cell, and the device may shut down before the open wire event is recorded.

0 = Cell-Voltage-based shutdown disabled

All other values = Cell voltage shutdown threshold

13.4.1.2 Power:Shutdown:Shutdown Stack Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Stack Voltage	I2	0	32767	600	10mV

Description: Configures the pack voltage threshold at which the device will enter SHUTDOWN mode

13.4.1.3 Power:Shutdown:Low V Shutdown Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Low V Shutdown Delay	U1	0	63	1	s

Description: Configures the number of seconds the device must measure voltage below ***Power:Shutdown:Shutdown Stack Voltage*** or ***Power:Shutdown:Shutdown Cell Voltage*** to enter SHUTDOWN mode. A value of 0 means that shutdown will be entered with a single low voltage sample.

13.4.1.4 Power:Shutdown:Shutdown Temperature

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Temperature	U1	0	150	85	°C

Description: Configures the internal temperature threshold at which the device will shut down

0 = Shutdown based on measured internal temperature disabled

All other values = Shutdown Internal Temperature threshold

13.4.1.5 Power:Shutdown:Shutdown Temperature Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Temperature Delay	U1	0	254	5	s

Description: Configures the number of consecutive seconds the device must measure an internal temperature above ***Power:Shutdown:Shutdown Temperature*** to enter SHUTDOWN mode.

13.4.1.6 Power:Shutdown:FET Off Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	FET Off Delay	U1	0	127	0	0.25s

Description: When the SHUTDOWN command is received or the RST_SHUT pin is detected high for one second, the FETs are turned off after this delay.

13.4.1.7 Power:Shutdown:Shutdown Command Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Shutdown Command Delay	U1	0	254	0	0.25s

Description: When the SHUTDOWN command is received or the RST_SHUT pin is detected high for one second, the device will enter SHUTDOWN after this delay. If the LD pin voltage is still high after this delay, the device will delay entering SHUTDOWN further until that voltage is no longer present.

13.4.1.8 Power:Shutdown:Auto Shutdown Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	Auto Shutdown Time	U1	0	250	0	min

Description: As a countermeasure to inadvertent wake from SHUTDOWN, the device can be configured to automatically enter SHUTDOWN again after a number of minutes defined by this parameter. If communications occur after the first second, or if charge current is detected, or if discharge current above the SLEEP current threshold is detected after one minute, automatic shutdown is cancelled. If none of those events occur, after this number of minutes, the FETs will be turned off for up to five seconds. During that 5 seconds, if the PACK and LD pin voltages fall, the device will enter shutdown. If the voltage on those pins remain above their respective thresholds, auto-shutdown is cancelled based on a conclusion that a charger is present.

0 = Auto-shutdown feature is disabled.

All other values = Auto-shutdown occurs after this many minutes if it is not cancelled.

13.4.1.9 Power:Shutdown:RAM Fail Shutdown Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Shutdown	RAM Fail Shutdown Time	U1	0	255	5	s

Description: The device performs periodic RAM integrity checks and forces a watchdog reset if corruption is detected. To avoid unwanted reset loops in case of a failure, the device will enter SHUTDOWN mode instead of resetting if it detects a RAM error within this number of seconds of a watchdog reset.

13.4.2 Power:Sleep

13.4.2.1 Power:Sleep:Sleep Current

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Sleep Current	I2	0	32767	20	mA

Description: Configures the current threshold above which the device will not enter SLEEP mode. If current is measured above this value during a periodic measurement in SLEEP mode, SLEEP mode will be exited.

13.4.2.2 Power:Sleep:Voltage Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Voltage Time	U1	1	255	5	s

Description: This parameter sets how often the device wakes to measure voltages and temperatures while in SLEEP mode. While in sleep mode, the device begins 4-second current measurements one second after measuring voltages and temperatures. These measurements interrupt the 4-second current measurement and start it over. That means that setting this parameter to a value less than 5 seconds will result in no completed 4-second current measurements in sleep. The most common settings of this parameter are 1 second, 5 seconds, or (4 * n + 1) seconds.

13.4.2.3 Power:Sleep:Wake Comparator Current

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Wake Comparator Current	I2	500	32767	500	mA

Description: Configures the current wake comparator threshold in sleep mode. Note that the default wake comparator conversion speed (12 ms) results in lower accuracy conversions than the normal current measurements. The smallest recommended threshold at this speed is 500mA.

13.4.2.4 Power:Sleep:Sleep Hysteresis Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Sleep Hysteresis Time	U1	0	255	10	s

Description: After transitioning to NORMAL mode, the device will not enter SLEEP mode again until this number of seconds has passed.

13.4.2.5 Power:Sleep:Sleep Charger Voltage Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Sleep Charger Voltage Threshold	I2	0	32767	2000	10mV

Description: The Top-of-Stack voltage must be below this threshold to block SLEEP mode based on charger presence.

13.4.2.6 Power:Sleep:Sleep Charger PACK-TOS Delta

Class	Subclass	Name	Type	Min	Max	Default	Unit
Power	Sleep	Sleep Charger PACK-TOS Delta	I2	10	8500	200	10mV

Description: If the PACK pin voltage is higher than the Top-of-Stack by more than this threshold and the Top-of-Stack voltage is less than ***Power:Sleep:Sleep Charger Voltage Threshold***, SLEEP mode is not allowed. This threshold is also used for charger detection when delaying voltage-based shutdown.

13.5 System Data

13.5.1 System Data:Integrity

13.5.1.1 System Data:Integrity:Config RAM Signature

Class	Subclass	Name	Type	Min	Max	Default	Unit
System Data	Integrity	Config RAM Signature	U2	0x0000	0x7FFF	0	Hex

Description: The lower 15 bits of the signature of static configuration options (which is returned by the STATIC_CFG_SIG subcommand) should be programmed into this parameter. When the STATIC_CFG_SIG subcommand is sent, the response will be checked against this value. If the value does not match, the top bit will be set in the response returned. This enables the system to validate the static config signature without having knowledge of the signature itself.

13.6 Protections

13.6.1 Protections:CUV

13.6.1.1 Protections:CUV:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	CUV	Threshold	U1	20	90	50	50.6mV

Description: This parameter sets the Cell Undervoltage Protection threshold in units of 50.6mV.

13.6.1.2 Protections:CUV:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	CUV	Delay	U2	1	2047	74	3.3 ms

Description: This parameter sets the Cell Undervoltage Protection delay in units of 3.3 ms with a 6.6ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

13.6.1.3 Protections:CUV:Recovery Hysteresis

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	CUV	Recovery Hysteresis	U1	2	20	2	50.6mV

Description: This parameter sets the Cell Undervoltage Protection hysteresis threshold in units of 50.6mV. The minimum cell voltage must be greater than or equal to the CUV threshold plus this hysteresis for ***Protections:Recovery:Time*** to recover from a CUV condition.

13.6.2 Protections:COV

13.6.2.1 Protections:COV:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	COV	Threshold	U1	20	110	86	50.6mV

Description: This parameter sets the Cell Overvoltage Protection threshold in units of 50.6mV.

13.6.2.2 Protections:COV:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	COV	Delay	U2	1	2047	74	3.3 ms

Description: This parameter sets the Cell Overvoltage Protection delay in units of 3.3 ms with a 6.6ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

13.6.2.3 Protections:COV:Recovery Hysteresis

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	COV	Recovery Hysteresis	U1	2	20	2	50.6mV

Description: This parameter sets the Cell Overvoltage Protection hysteresis threshold in units of 50.6mV. The maximum cell voltage must be less than or equal to the COV threshold minus this hysteresis for ***Protections:Recovery:Time*** to recover from a COV condition.

13.6.3 Protections:COVL

13.6.3.1 Protections:COVL:Latch Limit

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	COVL	Latch Limit	U1	0	255	0	—

Description: Whenever a COV event occurs, the COV latch counter is incremented. If the latch counter reaches this limit, the Cell Overvoltage Latch Protection is triggered. This protection allows for a longer recovery time when repeated COV events occur because the action of turning the CHG FET off cause the voltage to drop enough to recover.

13.6.3.2 Protections:COVL:Counter Dec Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	COVL	Counter Dec Delay	U1	0	255	10	s

Description: Whenever a COV event occurs, the COV latch counter is incremented. While the counter is nonzero, it will be decremented after the delay set by this parameter. This parameter should be set to a value larger than ***Protections:Recovery:Time*** to ensure that repeated COV events can increment the counter faster than this would decrement it. This parameter should be set to a value smaller than ***Protections:COVL:Recovery Time*** to ensure that the latch counter is decremented before recovering. Otherwise, the protection would trigger again since the latch counter is still at the limit.

13.6.3.3 Protections:COVL:Recovery Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	COVL	Recovery Time	U1	0	255	15	s

Description: This parameter sets the delay after which the Cell Overvoltage Latch Protection will recover. It should be set longer than ***Protections:COVL:Counter Dec Delay*** to ensure that the latch counter is decremented before recovering. Otherwise, the protection will trigger again since the latch counter is still at the limit.

13.6.4 Protections:OCC

13.6.4.1 Protections:OCC:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCC	Threshold	U1	2	62	2	2mV

Description: This parameter sets the Overcurrent in Charge Protection threshold for the sense resistor voltage in units of 2mV.

13.6.4.2 Protections:OCC:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCC	Delay	U1	1	127	4	3.3 ms

Description: This parameter sets the delay before the fault is triggered in units of 3.3 ms with a 6.6ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

13.6.4.3 Protections:OCC:Recovery Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCC	Recovery Threshold	I2	–32768	32767	–200	mA

Description: This sets the recovery threshold for the Overcurrent in Charge Protection. If measured current is less than or equal to this threshold for ***Protections:Recovery:Time***, recovery occurs.

13.6.4.4 Protections:OCC:PACK-TOS Delta

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCC	PACK-TOS Delta	I2	10	8500	200	10mV

Description: This parameter configures an alternate recovery mechanism for Overcurrent in Charge. If the PACK pin voltage is less than or equal to the Top-of-Stack voltage minus this delta for ***Protections:Recovery:Time*** second, recovery occurs.

13.6.5 Protections:OCD1

13.6.5.1 Protections:OCD1:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCD1	Threshold	U1	2	100	4	2mV

Description: This parameter sets the Overcurrent in Discharge 1st Tier Protection threshold for the sense resistor voltage in units of 2mV.

13.6.5.2 Protections:OCD1:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCD1	Delay	U1	1	127	1	3.3 ms

Description: This parameter sets the delay before the fault is triggered in units of 3.3 ms with a 6.6ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

13.6.6 Protections:OCD2

13.6.6.1 Protections:OCD2:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCD2	Threshold	U1	2	100	3	2mV

Description: This parameter sets the Overcurrent in Discharge 2nd Tier Protection threshold for the sense resistor voltage in units of 2mV.

13.6.6.2 Protections:OCD2:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCD2	Delay	U1	1	127	7	3.3 ms

Description: This parameter sets the delay before the fault is triggered in units of 3.3 ms with a 6.6ms offset. This means a setting of 1 gives 10 ms, 2 gives 13.3 ms, and so on.

13.6.7 Protections:SCD

13.6.7.1 Protections:SCD:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	SCD	Threshold	U1	0	15	0	—

Description: This parameter sets the Short Circuit in Discharge Protection threshold for the sense resistor voltage.

0 = 10 mV

1 = 20 mV

2 = 40 mV

3 = 60 mV

4 = 80 mV

5 = 100 mV

6 = 125 mV

7 = 150 mV

8 = 175 mV

9 = 200 mV

10 = 250 mV

11 = 300 mV

12 = 350 mV

13 = 400 mV

14 = 450 mV

15 = 500 mV

13.6.7.2 Protections:SCD:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	SCD	Delay	U1	1	31	2	15µs

Description: This parameter sets the delay before the fault is triggered in units of 15 µs.

1 = Protection is enabled with no delay.

All other values = Enabled with a delay of (value - 1) * 15 µs

13.6.7.3 Protections:SCD:Recovery Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	SCD	Recovery Time	U1	0	255	5	s

Description: This parameter configures the delay after which the Short Circuit in Discharge Protection recovers. If time-based recovery from SCD is not desired, the Short Circuit in Discharge Latch protection can be used with a ***Protections:SCDL:Latch Limit*** of 1.

13.6.8 Protections:OCD3

13.6.8.1 Protections:OCD3:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCD3	Threshold	I2	–32768	0	–4000	userA

Description: This parameter sets the Overcurrent in Discharge 3rd Tier Protection threshold. Units of reported current are configurable. This parameter uses the same units as reported current, so it is in units of user-amps.

13.6.8.2 Protections:OCD3:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCD3	Delay	U1	0	255	2	s

Description: This parameter sets the delay for Overcurrent in Discharge 3rd Tier to trigger in units of seconds.

13.6.9 Protections:OCD

13.6.9.1 Protections:OCD:Recovery Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCD	Recovery Threshold	I2	–32768	32767	200	mA

Description: This sets the recovery threshold for Overcurrent in Discharge 1st, 2nd, and 3rd Tier Protections. Measured current must be greater than or equal to this threshold for ***Protections:Recovery:Time*** to recover. Note the sign of current when configuring this parameter; by default it requires charge current above this threshold.

13.6.10 Protections:OCDL

13.6.10.1 Protections:OCDL:Latch Limit

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCDL	Latch Limit	U1	0	255	0	—

Description: Whenever an OCD event occurs, the OCD latch counter is incremented. If the latch counter reaches this limit, the Overcurrent Latch Protection is triggered. This protection allows for alternate recovery conditions when repeated Overcurrent in Discharge events occur.

13.6.10.2 Protections:OCDL:Counter Dec Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCDL	Counter Dec Delay	U1	0	255	10	s

Description: Whenever an OCD event occurs, the OCD latch counter is incremented. While the counter is nonzero, it will be decremented after the delay set by this parameter. This parameter should be set to a value larger than ***Protections:Recovery:Time*** to ensure that repeated OCD events can increment the counter faster than this would decrement it.

13.6.10.3 Protections:OCDL:Recovery Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCDL	Recovery Time	U1	0	255	15	s

Description: This parameter sets the recovery delay for the Overcurrent in Discharge Latch Protection. Measured current must be greater than or equal to the ***Protections:OCDL:Recovery Threshold*** for this many seconds for recovery to occur via this mechanism. This recovery mechanism is disabled when ***Settings:Protection:Protection Configuration[OCDL_CURR_RECOV]*** is not set.

13.6.10.4 Protections:OCDL:Recovery Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OCDL	Recovery Threshold	I2	–32768	32767	200	mA

Description: This parameter sets the recovery threshold for the Overcurrent in Discharge Latch Protection. Measured current must be greater than or equal to this value for ***Protections:OCDL:Recovery Time*** seconds for recovery to occur via this mechanism. This recovery mechanism is disabled when ***Settings:Protection:Protection Configuration[OCDL_CURR_RECOV]*** is not set.

13.6.11 Protections:SCDL

13.6.11.1 Protections:SCDL:Latch Limit

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	SCDL	Latch Limit	U1	0	255	0	—

Description: Whenever an SCD event occurs, the SCD latch counter is incremented. If the latch counter reaches this limit, the Short Circuit in Discharge Latch Protection is triggered. This protection allows for alternate recovery conditions when repeated Short Circuit in Discharge events occur.

13.6.11.2 Protections:SCDL:Counter Dec Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	SCDL	Counter Dec Delay	U1	0	255	10	s

Description: Whenever an SCD event occurs, the SCD latch counter is incremented. While the counter is nonzero, it will be decremented after the delay set by this parameter. This parameter should be set to a value larger than ***Protections:SCD:Recovery Time*** to ensure that repeated SCD events can increment the counter faster than this would decrement it.

13.6.11.3 Protections:SCDL:Recovery Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	SCDL	Recovery Time	U1	0	255	15	s

Description: This parameter sets the recovery delay for the Short Circuit in Discharge Latch Protection. Measured current must be greater than or equal to the ***Protections:SCDL:Recovery Threshold*** for this many seconds for recovery to occur via this mechanism. This recovery mechanism is disabled when ***Settings:Protection:Protection Configuration[SCDL_CURR_RECOV]*** is not set.

13.6.11.4 Protections:SCDL:Recovery Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	SCDL	Recovery Threshold	I2	–32768	32767	200	mA

Description: This parameter sets the recovery threshold for the Short Circuit in Discharge Latch Protection. Measured current must be greater than or equal to this value for ***Protections:SCDL:Recovery Time*** seconds for recovery to occur via this mechanism. This recovery mechanism is disabled when ***Settings:Protection:Protection Configuration[SCDL_CURR_RECOV]*** is not set.

13.6.12 Protections:OTC

13.6.12.1 Protections:OTC:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTC	Threshold	I1	–40	120	55	°C

Description: This parameter sets the Overtemperature in Charge Protection threshold. When the maximum cell temperature is greater than or equal to this threshold for ***Protections:OTC:Delay*** seconds, the protection is triggered. Note that charging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which charging should not be allowed, not an indicator of if charging happened at this temperature.

13.6.12.2 Protections:OTC:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTC	Delay	U1	0	255	2	s

Description: This parameter sets the Overtemperature in Charge Protection delay. When the maximum cell temperature is greater than or equal to ***Protections:OTC:Threshold*** for this many seconds, the protection is triggered. Note that charging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which charging should not be allowed, not an indicator of if charging happened at this temperature.

13.6.12.3 Protections:OTC:Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTC	Recovery	I1	–40	120	50	°C

Description: This parameter sets the Overtemperature in Charge Protection recovery threshold. Recovery occurs when the maximum cell temperature is less than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

13.6.13 Protections:OTD

13.6.13.1 Protections:OTD:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTD	Threshold	I1	–40	120	60	°C

Description: This parameter sets the Overtemperature in Discharge Protection threshold. When the maximum cell temperature is greater than or equal to this threshold for ***Protections:OTD:Delay*** seconds, the protection is triggered. Note that discharging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which discharging should not be allowed, not an indicator of if discharging happened at this temperature.

13.6.13.2 Protections:OTD:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTD	Delay	U1	0	255	2	s

Description: This parameter sets the Overtemperature in Discharge Protection delay. When the maximum cell temperature is greater than or equal to ***Protections:OTD:Threshold*** for this many seconds, the protection is triggered. Note that discharging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which discharging should not be allowed, not an indicator of if discharging happened at this temperature.

13.6.13.3 Protections:OTD:Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTD	Recovery	I1	–40	120	55	°C

Description: This parameter sets the Overtemperature in Discharge Protection recovery threshold. Recovery occurs when the maximum cell temperature is less than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

13.6.14 Protections:OTF

13.6.14.1 Protections:OTF:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTF	Threshold	U1	0	150	80	°C

Description: This parameter sets the FET Overtemperature threshold. When the FET temperature is greater than or equal to this threshold for ***Protections:OTF:Delay*** seconds, the protection is triggered.

13.6.14.2 Protections:OTF:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTF	Delay	U1	0	255	2	s

Description: This parameter sets the FET Overtemperature Protection delay. When the FET temperature is greater than or equal to ***Protections:OTF:Threshold*** for this many seconds, the protection is triggered.

13.6.14.3 Protections:OTF:Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTF	Recovery	U1	0	150	65	°C

Description: This parameter sets the FET Overtemperature Protection recovery threshold. Recovery occurs when the FET temperature is less than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

13.6.15 Protections:OTINT

13.6.15.1 Protections:OTINT:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTINT	Threshold	I1	–40	120	85	°C

Description: This parameter sets the Internal Overtemperature threshold. When the internal temperature is greater than or equal to this threshold for ***Protections:OTINT:Delay*** seconds, the protection is triggered.

13.6.15.2 Protections:OTINT:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTINT	Delay	U1	0	255	2	s

Description: This parameter sets the Internal Overtemperature Protection delay. When the internal temperature is greater than or equal to ***Protections:OTINT:Threshold*** for this many seconds, the protection is triggered.

13.6.15.3 Protections:OTINT:Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	OTINT	Recovery	I1	–40	120	80	°C

Description: This parameter sets the Internal Overtemperature Protection recovery threshold. Recovery occurs when the internal temperature is less than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

13.6.16 Protections:UTC

13.6.16.1 Protections:UTC:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTC	Threshold	I1	–40	120	0	°C

Description: This parameter sets the Undertemperature in Charge Protection threshold. When the minimum cell temperature is less than or equal to this threshold for ***Protections:UTC:Delay*** seconds, the protection is triggered. Note that charging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which charging should not be allowed, not an indicator of if charging happened at this temperature.

13.6.16.2 Protections:UTC:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTC	Delay	U1	0	255	2	s

Description: This parameter sets the Undertemperature in Charge Protection delay. When the minimum cell temperature is less than or equal to ***Protections:UTC:Threshold*** for this many seconds, the protection is triggered. Note that charging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which charging should not be allowed, not an indicator of if charging happened at this temperature.

13.6.16.3 Protections:UTC:Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTC	Recovery	I1	–40	120	5	°C

Description: This parameter sets the Undertemperature in Charge Protection recovery threshold. Recovery occurs when the minimum cell temperature is greater than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

13.6.17 Protections:UTD

13.6.17.1 Protections:UTD:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTD	Threshold	I1	–40	120	0	°C

Description: This parameter sets the Undertemperature in Discharge Protection threshold. When the minimum cell temperature is less than or equal to this threshold for ***Protections:UTD:Delay*** seconds, the protection is triggered. Note that discharging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which discharging should not be allowed, not an indicator of if discharging happened at this temperature.

13.6.17.2 Protections:UTD:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTD	Delay	U1	0	255	2	s

Description: This parameter sets the Undertemperature in Discharge Protection delay. When the minimum cell temperature is less than or equal to ***Protections:UTD:Threshold*** for this many seconds, the protection is triggered. Note that discharging does not need to be occurring for this protection to trigger. It is intended to be the threshold at which discharging should not be allowed, not an indicator of if discharging happened at this temperature.

13.6.17.3 Protections:UTD:Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTD	Recovery	I1	–40	120	5	°C

Description: This parameter sets the Undertemperature in Discharge Protection recovery threshold. Recovery occurs when the minimum cell temperature is greater than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

13.6.18 Protections:UTINT

13.6.18.1 Protections:UTINT:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTINT	Threshold	I1	–40	120	–20	°C

Description: This parameter sets the Internal Undertemperature threshold. When the internal temperature is less than or equal to this threshold for ***Protections:UTINT:Delay*** seconds, the protection is triggered.

13.6.18.2 Protections:UTINT:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTINT	Delay	U1	0	255	2	s

Description: This parameter sets the Internal Undertemperature Protection delay. When the internal temperature is less than or equal to ***Protections:UTINT:Threshold*** for this many seconds, the protection is triggered.

13.6.18.3 Protections:UTINT:Recovery

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	UTINT	Recovery	I1	–40	120	–15	°C

Description: This parameter sets the Internal Undertemperature Protection recovery threshold. Recovery occurs when the internal temperature is greater than or equal to this threshold for ***Protections:Recovery:Time*** seconds.

13.6.19 Protections:Recovery

13.6.19.1 Protections:Recovery:Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Recovery	Time	U1	0	255	3	s

Description: This parameter configures the recovery time used by several protections in units of seconds. The recovery criteria must be met for this delay for recovery to occur.

13.6.20 Protections:HWD

13.6.20.1 Protections:HWD:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	HWD	Delay	U2	0	65535	60	s

Description: This parameter configures the Host Watchdog timeout. If communications are not received for this many seconds, the Host Watchdog Fault is triggered.

13.6.21 Protections:Load Detect

13.6.21.1 Protections:Load Detect:Active Time

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Load Detect	Active Time	U1	0	255	0	s

Description: The Short Circuit in Discharge Latch and Overcurrent in Discharge Latch protections can be configured to recover when the load removal is detected. The device can enable a current source on the LD pin and checks for the voltage level rising above 3V. This parameter controls how long the current source is enabled before waiting ***Protections:Load Detect:Retry Delay*** seconds and trying again. This should be set longer than ***Power:Sleep:Voltage Time*** to ensure that voltage is measured while the current source is enabled.

0 = Recovery based on Load Detect functionality is disabled.

All other values = Load Detect current source is enabled for this many seconds at a time.

13.6.21.2 Protections:Load Detect:Retry Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Load Detect	Retry Delay	U1	0	255	50	s

Description: The Short Circuit in Discharge Latch and Overcurrent in Discharge Latch protections can be configured to recover when the load removal is detected. The device can enable a current source on the LD pin and checks for the voltage level rising above 3V. The current source is enabled only temporarily to save power. This parameter controls the delay between periods when the LD current source is active.

0 = Load Detect current source stays on until ***Protections:Load Detect:Timeout*** or recovery.

All other values = Load detect current source is disabled for this many seconds before trying again.

13.6.21.3 Protections:Load Detect:Timeout

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	Load Detect	Timeout	U2	0	65535	1	hrs

Description: To prevent the Load Detect function from indefinitely operating and draining the battery, a timeout may be configured. This timeout starts when Load Detect is first enabled to check recovery and is measured in hours. After this timeout, Load Detect is no longer checked until the latch faults have recovered or a command to retry is received.

13.6.22 Protections:PTO

13.6.22.1 Protections:PTO:Charge Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	PTO	Charge Threshold	I2	–32768	32767	250	mA

Description: This parameter sets the current threshold for the Precharge Timeout Protection. When in Precharge mode but the current is less than or equal to this threshold, the timeout timer is not incremented and the Precharge Timeout Suspend (PTOS) bit is set.

13.6.22.2 Protections:PTO:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	PTO	Delay	U2	0	65535	1800	s

Description: This parameter sets the Precharge Timeout threshold. When in Precharge mode with current above ***Protections:PTO:Charge Threshold***, a timer is incremented. If the timer reaches this value, the Precharge Timeout Protection is triggered. This should be set to a value sufficiently long enough for Precharge to complete and normal charge to start.

13.6.22.3 Protections:PTO:Reset

Class	Subclass	Name	Type	Min	Max	Default	Unit
Protections	PTO	Reset	I2	0	10000	2	userAh

Description: The timer for the Precharge Timeout Protection is reset when a continuous discharge of this much capacity occurs. This discharge must be larger in magnitude than ***Settings:Current Thresholds:Dsg Current Threshold*** for long enough to accumulate this amount of charge. Note that the units of this parameter scale with the selected units for reported current (user-amps).

13.7 Permanent Fail

13.7.1 Permanent Fail:CUDEP

13.7.1.1 Permanent Fail:CUDEP:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	CUDEP	Threshold	I2	0	32767	1500	mV

Description: When a cell is severely overdischarged, copper deposition can occur, resulting in very high impedance. Normally the device is shut down before the cells reach this low voltage, but in certain configurations the device may wake with a charger attached. If the FETs were turned on at this point, the voltage would rise sharply and the cells would appear to be fine due to the high charging current flowing. When enabled, the copper deposition check holds the FETs off until the voltage is greater than or equal to ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds. If the voltage is below ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds, the CUDEP Permanent Fail is triggered.

13.7.1.2 Permanent Fail:CUDEP:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	CUDEP	Delay	U1	0	255	2	s

Description: When a cell is severely overdischarged, copper deposition can occur, resulting in very high impedance. Normally the device is shut down before the cells reach this low voltage, but in certain configurations the device may wake with a charger attached. If the FETs were turned on at this point, the voltage would rise sharply and the cells would appear to be fine due to the high charging current flowing. When enabled, the copper deposition check holds the FETs off until the voltage is greater than or equal to ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds. If the voltage is below ***Permanent Fail:CUDEP:Threshold*** for ***Permanent Fail:CUDEP:Delay*** seconds, the CUDEP Permanent Fail is triggered.

13.7.2 Permanent Fail:SUV

13.7.2.1 Permanent Fail:SUV:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SUV	Threshold	I2	0	32767	2200	mV

Description: This parameter sets the Safety Undervoltage Permanent Fail threshold. When the minimum cell voltage is less than or equal to ***Permanent Fail:SUV:Threshold*** for ***Permanent Fail:SUV:Delay*** seconds, the SUV Permanent Fail is triggered.

13.7.2.2 Permanent Fail:SUV:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SUV	Delay	U1	0	255	5	s

Description: This parameter sets the Safety Undervoltage Permanent Fail delay. When the minimum cell voltage is less than or equal to***Permanent Fail:SUV:Threshold*** for ***Permanent Fail:SUV:Delay*** seconds, the SUV Permanent Fail is triggered.

13.7.3 Permanent Fail:SOV

13.7.3.1 Permanent Fail:SOV:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOV	Threshold	I2	0	32767	4500	mV

Description: This parameter sets the Safety Overvoltage Permanent Fail threshold. When the maximum cell voltage is greater than or equal to ***Permanent Fail:SOV:Threshold*** for ***Permanent Fail:SOV:Delay*** seconds, the SOV Permanent Fail is triggered.

13.7.3.2 Permanent Fail:SOV:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOV	Delay	U1	0	255	5	s

Description: This parameter sets the Safety Undervoltage Permanent Fail delay. When the maximum cell voltage is greater than or equal to ***Permanent Fail:SOV:Threshold*** for ***Permanent Fail:SOV:Delay*** seconds, the SOV Permanent Fail is triggered.

13.7.4 Permanent Fail:TOS

13.7.4.1 Permanent Fail:TOS:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	TOS	Threshold	I2	0	32767	500	mV

Description: This parameter sets the Top of Stack vs Cell Sum Permanent Fail threshold. The threshold is based on cell voltage, so it is multiplied by the number of used cells before the comparison. The device compares the measured Top of Stack voltage to the sum of individually measured cell voltages. When the absolute value of the difference is greater than or equal to the number of used cells times the ***Permanent Fail:TOS:Threshold*** for ***Permanent Fail:TOS:Delay*** seconds, the TOSF Permanent Fail is triggered. This check is skipped when the current reading during any of these voltage measurements is above ***Power:Sleep:Sleep Current*** to avoid false triggers due to changing loads.

13.7.4.2 Permanent Fail:TOS:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	TOS	Delay	U1	0	255	5	s

Description: This parameter sets the Top of Stack vs Cell Sum Permanent Fail threshold. The device compares the measured Top of Stack voltage to the sum of individually measured cell voltages. When the absolute value of the difference is greater than or equal to the number of used cells times the ***Permanent Fail:TOS:Threshold*** for ***Permanent Fail:TOS:Delay*** seconds, the TOSF Permanent Fail is triggered. This check is skipped when the current reading during any of these voltage measurements is above ***Power:Sleep:Sleep Current*** to avoid false triggers due to changing loads.

13.7.5 Permanent Fail:SOCC

13.7.5.1 Permanent Fail:SOCC:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOCC	Threshold	I2	–32768	32767	10000	userA

Description: This parameter sets the Safety Overcurrent in Charge Permanent Fail threshold. When the measured current is greater than or equal to ***Permanent Fail:SOCC:Threshold*** for ***Permanent Fail:SOCC:Delay*** seconds, the SOCC Permanent Fail is triggered.

13.7.5.2 Permanent Fail:SOCC:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOCC	Delay	U1	0	255	5	s

Description: This parameter sets the Safety Overcurrent in Charge Permanent Fail delay. When the measured current is greater than or equal to ***Permanent Fail:SOCC:Threshold*** for ***Permanent Fail:SOCC:Delay*** seconds, the SOCC Permanent Fail is triggered.

13.7.6 Permanent Fail:SOCD

13.7.6.1 Permanent Fail:SOCD:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOCD	Threshold	I2	–32768	32767	–32000	userA

Description: This parameter sets the Safety Overcurrent in Discharge Permanent Fail threshold. When the measured current is greater than or equal to ***Permanent Fail:SOCD:Threshold*** for ***Permanent Fail:SOCD:Delay*** seconds, the SOCD Permanent Fail is triggered.

13.7.6.2 Permanent Fail:SOCD:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOCD	Delay	U1	0	255	5	s

Description: This parameter sets the Safety Overcurrent in Discharge Permanent Fail delay. When the measured current is greater than or equal to ***Permanent Fail:SOCD:Threshold*** for ***Permanent Fail:SOCD:Delay*** seconds, the SOCD Permanent Fail is triggered.

13.7.7 Permanent Fail:SOT

13.7.7.1 Permanent Fail:SOT:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOT	Threshold	I1	–40	120	65	°C

Description: This parameter sets the Safety Overtemperature Permanent Fail threshold. When the maximum cell temperature is greater than or equal to ***Permanent Fail:SOT:Threshold*** for ***Permanent Fail:SOT:Delay*** seconds, the SOT Permanent Fail is triggered.

13.7.7.2 Permanent Fail:SOT:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOT	Delay	U1	0	255	5	s

Description: This parameter sets the Safety Overtemperature Permanent Fail delay. When the maximum cell temperature is greater than or equal to ***Permanent Fail:SOT:Threshold*** for ***Permanent Fail:SOT:Delay*** seconds, the SOT Permanent Fail is triggered.

13.7.8 Permanent Fail:SOTF

13.7.8.1 Permanent Fail:SOTF:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOTF	Threshold	U1	0	150	85	°C

Description: This parameter sets the Safety Overtemperature FET Permanent Fail threshold. When the FET temperature is greater than or equal to ***Permanent Fail:SOTF:Threshold*** for ***Permanent Fail:SOTF:Delay*** seconds, the SOTF Permanent Fail is triggered.

13.7.8.2 Permanent Fail:SOTF:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	SOTF	Delay	U1	0	255	5	s

Description: This parameter sets the Safety Overtemperature FET Permanent Fail delay. When the FET temperature is greater than or equal to ***Permanent Fail:SOTF:Threshold*** for ***Permanent Fail:SOTF:Delay*** seconds, the SOTF Permanent Fail is triggered.

13.7.9 Permanent Fail:VIMR

13.7.9.1 Permanent Fail:VIMR:Check Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMR	Check Voltage	I2	0	5500	3500	mV

Description: The Voltage Imbalance at Rest Permanent Fail is not checked when the maximum cell voltage is less than this threshold. This is because at lower states of charge, the voltage differences for a smaller imbalance are amplified.

13.7.9.2 Permanent Fail:VIMR:Max Relax Current

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMR	Max Relax Current	I2	10	32767	10	mA

Description: The Voltage Imbalance at Rest Permanent Fail is not checked when the absolute value of measured current is greater than or equal to this threshold.

13.7.9.3 Permanent Fail:VIMR:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMR	Threshold	I2	0	5500	500	mV

Description: This parameter sets the Voltage Imbalance at Rest Permanent Fail threshold. When the delta between the maximum and minimum cell voltages is greater than or equal to ***Permanent Fail:VIMR:Threshold*** for ***Permanent Fail:VIMR:Delay*** seconds while VIMR check conditions are met, the VIMR Permanent Fail is triggered.

13.7.9.4 Permanent Fail:VIMR:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMR	Delay	U1	0	255	5	s

Description: This parameter sets the Voltage Imbalance at Rest Permanent Fail delay. When the delta between the maximum and minimum cell voltages is greater than or equal to ***Permanent Fail:VIMR:Threshold*** for ***Permanent Fail:VIMR:Delay*** seconds while VIMR check conditions are met, the VIMR Permanent Fail is triggered.

13.7.9.5 Permanent Fail:VIMR:Relax Min Duration

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMR	Relax Min Duration	U2	0	65535	100	s

Description: The Voltage Imbalance at Rest Permanent Fail is not checked unless the ***Permanent Fail:VIMR:Check Voltage*** and ***Permanent Fail:VIMR:Max Relax Current*** conditions have been met for this duration.

13.7.10 Permanent Fail:VIMA

13.7.10.1 Permanent Fail:VIMA:Check Voltage

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMA	Check Voltage	I2	0	5500	3700	mV

Description: The Voltage Imbalance Active Permanent Fail is not checked when the maximum cell voltage is less than this threshold. This is because at lower states of charge, the voltage differences for a smaller imbalance are amplified.

13.7.10.2 Permanent Fail:VIMA:Min Active Current

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMA	Min Active Current	I2	10	32767	50	mA

Description: The Voltage Imbalance Active Permanent Fail is not checked when the absolute value of measured current is less than this threshold.

13.7.10.3 Permanent Fail:VIMA:Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMA	Threshold	I2	0	5500	200	mV

Description: This parameter sets the Voltage Imbalance Active Permanent Fail threshold. When the delta between the maximum and minimum cell voltages is greater than or equal to ***Permanent Fail:VIMA:Threshold*** for ***Permanent Fail:VIMA:Delay*** seconds while VIMA check conditions are met, the VIMA Permanent Fail is triggered.

13.7.10.4 Permanent Fail:VIMA:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VIMA	Delay	U1	0	255	5	s

Description: This parameter sets the Voltage Imbalance Active Permanent Fail delay. When the delta between the maximum and minimum cell voltages is greater than or equal to ***Permanent Fail:VIMA:Threshold*** for ***Permanent Fail:VIMA:Delay*** seconds while VIMA check conditions are met, the VIMA Permanent Fail is triggered.

13.7.11 Permanent Fail:CFETF

13.7.11.1 Permanent Fail:CFETF:OFF Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	CFETF	OFF Threshold	I2	10	5000	20	mA

Description: This parameter sets the Charge FET Permanent Fail current threshold. When the measured current is greater than or equal to ***Permanent Fail:CFETF:OFF Threshold*** for ***Permanent Fail:CFETF:OFF Delay*** seconds while the CHG FET is off, the CFETF Permanent Fail is triggered.

13.7.11.2 Permanent Fail:CFETF:OFF Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	CFETF	OFF Delay	U1	0	255	5	s

Description: This parameter sets the Charge FET Permanent Fail delay. When the measured current is greater than or equal to ***Permanent Fail:CFETF:OFF Threshold*** for ***Permanent Fail:CFETF:OFF Delay*** seconds while the CHG FET is off, the CFETF Permanent Fail is triggered.

13.7.12 Permanent Fail:DFETF

13.7.12.1 Permanent Fail:DFETF:OFF Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	DFETF	OFF Threshold	I2	–5000	–10	–20	mA

Description: This parameter sets the Discharge FET Permanent Fail current threshold. When the measured current is less (more negative) than or equal to ***Permanent Fail:DFETF:OFF Threshold*** for ***Permanent Fail:DFETF:OFF Delay*** seconds while the DSG FET is off, the DFETF Permanent Fail is triggered.

13.7.12.2 Permanent Fail:DFETF:OFF Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	DFETF	OFF Delay	U1	0	255	5	s

Description: This parameter sets the Discharge FET Permanent Fail delay. When the measured current is less (more negative) than or equal to ***Permanent Fail:DFETF:OFF Threshold*** for ***Permanent Fail:DFETF:OFF Delay*** seconds while the DSG FET is off, the DFETF Permanent Fail is triggered.

13.7.13 Permanent Fail:VSSF

13.7.13.1 Permanent Fail:VSSF:Fail Threshold

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VSSF	Fail Threshold	I2	1	32767	100	—

Description: This parameter sets the Internal VSS Measurement Permanent Fail threshold. When the ADC count value measured for the internal VSS channel is greater than or equal to ***Permanent Fail:VSSF:Fail Threshold*** for ***Permanent Fail:VSSF:Delay*** seconds, the VSSF Permanent Fail is triggered.

13.7.13.2 Permanent Fail:VSSF:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	VSSF	Delay	U1	0	255	5	s

Description: This parameter sets the Internal VSS Measurement Permanent Fail delay. When the ADC count value measured for the internal VSS channel is greater than or equal to ***Permanent Fail:VSSF:Fail Threshold*** for ***Permanent Fail:VSSF:Delay*** seconds, the VSSF Permanent Fail is triggered.

13.7.14 Permanent Fail:2LVL

13.7.14.1 Permanent Fail:2LVL:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	2LVL	Delay	U1	0	255	5	s

Description: This parameter sets the Second Level Protector Permanent Fail delay. The device checks the FUSE pin each second, and if it is asserted by the second level protector for ***Permanent Fail:2LVL:Delay*** seconds, the 2LVL PF is triggered.

13.7.15 Permanent Fail:LFOF

13.7.15.1 Permanent Fail:LFOF:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	LFOF	Delay	U1	0	255	5	s

Description: This parameter sets the Internal LFO Permanent Fail delay. The device monitors the output of its Low-Frequency Oscillator integrity check. If the error bit is set for ***Permanent Fail:LFOF:Delay*** seconds, the LFOF Permanent Failure is triggered. If ***Permanent Fail:LFOF:Delay*** = 0, FETs are automatically turned off when LFO Failure is detected, regardless of the ***Settings:Permanent Failure:Enabled PF C[LFOF]*** setting.

13.7.16 Permanent Fail:HWMX

13.7.16.1 Permanent Fail:HWMX:Delay

Class	Subclass	Name	Type	Min	Max	Default	Unit
Permanent Fail	HWMX	Delay	U1	0	255	5	s

Description: This parameter sets the Hardware Mux Permanent Fail delay. The device periodically performs an integrity check of the input mux for the hardware protection comparator subsystem, which is used for the OV, UV, OCC, OCD1, and OCD2 primary protections. If this check fails for ***Permanent Fail:HWMX:Delay*** seconds, the Hardware Mux Permanent Failure is triggered.

13.8 Security

13.8.1 Security:Settings

13.8.1.1 Security:Settings:Security Settings

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Settings	Security Settings	H1	0x00	0x07	0x00	Hex

7	6	5	4	3	2	1	0
RSVD_0	RSVD_0	RSVD_0	RSVD_0	RSVD_0	PERM_SEAL	LOCK_CFG	SEAL

Description: This parameter contains security-related configuration options.

Table 13-36. Security Settings Register Field Descriptions

Bit	Field	Default	Description
2	PERM_SEAL	0	Setting this bit prevents unsealing the device once it is sealed. If this is not programmed to OTP, this setting will be lost on a full reset and the device will again be able to UNSEAL. 0 = The device can be unsealed by sending the correct security keys. 1 = The device cannot be unsealed.
1	LOCK_CFG	0	Setting this bit prevents entry into CONFIG_UPDATE and FULLACCESS modes. This prevents further modifications to the device configuration after CONFIG_UPDATE mode is exited. 0 = Configuration parameters can be changed in CONFIG_UPDATE mode. 1 = Configuration parameters cannot be changed.
0	SEAL	0	Setting this bit causes the device to enter SEALED mode when reset or exiting CONFIG_UPDATE and DEEPSLEEP modes. In production systems, this bit should be set for security purposes. 0 = Device does not default to SEALED mode. 1 = Device default state is SEALED.

13.8.2 Security:Keys

13.8.2.1 Security:Keys:Unseal Key Step 1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Keys	Unseal Key Step 1	U2	0x0100	0xFFFF	0x0414	Hex

Description: This is the first word of the security key that must be sent to transition from SEALED to UNSEALED mode.

13.8.2.2 Security:Keys:Unseal Key Step 2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Keys	Unseal Key Step 2	U2	0x0100	0xFFFF	0x3672	Hex

Description: This is the second word of the security key that must be sent to transition from SEALED to UNSEALED mode. It must be sent within 5 seconds of the first word of the key and with no other commands in between.

13.8.2.3 Security:Keys:Full Access Key Step 1

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Keys	Full Access Key Step 1	U2	0x0100	0xFFFF	0xFFFF	Hex

Description: This is the second word of the security key that must be sent to transition from UNSEALED to FULLACCESS mode.

13.8.2.4 Security:Keys:Full Access Key Step 2

Class	Subclass	Name	Type	Min	Max	Default	Unit
Security	Keys	Full Access Key Step 2	U2	0x0100	0xFFFF	0xFFFF	Hex

Description: This is the second word of the security key that must be sent to transition from UNSEALED to FULLACCESS mode. It must be sent within 5 seconds of the first word of the key and with no other commands in between.

13.9 Data Memory Summary

Table 13-37. Data Memory Table

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Calibration	Voltage	0x9180	Cell 1 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x9182	Cell 2 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x9184	Cell 3 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x9186	Cell 4 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x9188	Cell 5 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x918A	Cell 6 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x918C	Cell 7 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x918E	Cell 8 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x9190	Cell 9 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x9192	Cell 10 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x9194	Cell 11 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x9196	Cell 12 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x919A	Cell 13 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x919E	Cell 14 Gain	I2	–32767	32767	0	—
Calibration	Voltage	0x91A0	Pack Gain	U2	0	65535	0	—
Calibration	Voltage	0x91A2	TOS Gain	U2	0	65535	0	—
Calibration	Voltage	0x91A4	LD Gain	U2	0	65535	0	—

Table 13-37. Data Memory Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Calibration	Voltage	0x91A6	ADC Gain	I2	–32767	32767	0	—
Calibration	Current	0x91A8	CC Gain	F4	1.00E–02	10.00E+02	7.4768	—
Calibration	Current	0x91AC	Capacity Gain	F4	2.98262E+03	4.193046E+08	2230042.463	—
Calibration	Vcell Offset	0x91B0	Vcell Offset	I2	–32767	32767	0	mV
Calibration	V Divider Offset	0x91B2	Vdiv Offset	I2	–32767	32767	0	userV
Calibration	Current Offset	0x91C6	Coulomb Counter Offset Samples	U2	0	65535	64	—
Calibration	Current Offset	0x91C8	Board Offset	I2	–32768	32767	0	—
Calibration	Temperature	0x91CA	Internal Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91CB	CFETOFF Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91CC	DFETOFF Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91CD	ALERT Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91CE	TS1 Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91CF	TS2 Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91D0	TS3 Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91D1	HDQ Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91D2	DCHG Temp Offset	I1	–128	127	0	0.1°C
Calibration	Temperature	0x91D3	DDSG Temp Offset	I1	–128	127	0	0.1°C
Calibration	Internal Temp Model	0x91E2	Int Gain	I2	–32768	32767	25390	—
Calibration	Internal Temp Model	0x91E4	Int base offset	I2	–32768	32767	3032	—
Calibration	Internal Temp Model	0x91E6	Int Maximum AD	I2	–32768	32767	16383	—
Calibration	Internal Temp Model	0x91E8	Int Maximum Temp	I2	0	32767	6379	0.1K
Calibration	18K Temperature Model	0x91EA	Coeff a1	I2	–32768	32767	–15524	—
Calibration	18K Temperature Model	0x91EC	Coeff a2	I2	–32768	32767	26423	—
Calibration	18K Temperature Model	0x91EE	Coeff a3	I2	–32768	32767	–22664	—
Calibration	18K Temperature Model	0x91F0	Coeff a4	I2	–32768	32767	28834	—
Calibration	18K Temperature Model	0x91F2	Coeff a5	I2	–32768	32767	672	—
Calibration	18K Temperature Model	0x91F4	Coeff b1	I2	–32768	32767	–371	—
Calibration	18K Temperature Model	0x91F6	Coeff b2	I2	–32768	32767	708	—
Calibration	18K Temperature Model	0x91F8	Coeff b3	I2	–32768	32767	–3498	—
Calibration	18K Temperature Model	0x91FA	Coeff b4	I2	–32768	32767	5051	—
Calibration	18K Temperature Model	0x91FE	Adc0	I2	–32768	32767	11703	—
Calibration	180K Temperature Model	0x9200	Coeff a1	I2	–32768	32767	–17513	—
Calibration	180K Temperature Model	0x9202	Coeff a2	I2	–32768	32767	25759	—
Calibration	180K Temperature Model	0x9204	Coeff a3	I2	–32768	32767	–23593	—
Calibration	180K Temperature Model	0x9206	Coeff a4	I2	–32768	32767	32175	—
Calibration	180K Temperature Model	0x9208	Coeff a5	I2	–32768	32767	2090	—

Table 13-37. Data Memory Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Calibration	180K Temperature Model	0x920A	Coeff b1	I2	–32768	32767	–2055	—
Calibration	180K Temperature Model	0x920C	Coeff b2	I2	–32768	32767	2955	—
Calibration	180K Temperature Model	0x920E	Coeff b3	I2	–32768	32767	–3427	—
Calibration	180K Temperature Model	0x9210	Coeff b4	I2	–32768	32767	4385	—
Calibration	180K Temperature Model	0x9214	Adc0	I2	–32768	32767	17246	—
Calibration	Custom Temperature Model	0x9216	Coeff a1	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x9218	Coeff a2	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x921A	Coeff a3	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x921C	Coeff a4	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x921E	Coeff a5	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x9220	Coeff b1	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x9222	Coeff b2	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x9224	Coeff b3	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x9226	Coeff b4	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x9228	Rc0	I2	–32768	32767	0	—
Calibration	Custom Temperature Model	0x922A	Adc0	I2	–32768	32767	0	—
Calibration	Current Deadband	0x922D	Coulomb Counter Deadband	U1	0	255	9	234nV
Calibration	CUV	0x91D4	CUV Threshold Override	U2	0x0000	0xFFFF	0xFFFF	Hex
Calibration	COV	0x91D6	COV Threshold Override	U2	0x0000	0xFFFF	0xFFFF	Hex
Settings	Fuse	0x9231	Min Blow Fuse Voltage	I2	0	32767	500	10mV
Settings	Fuse	0x9233	Fuse Blow Timeout	U1	0	255	30	s
Settings	Configuration	0x9234	Power Config	H2	0x0000	0xFFFF	0x2982	Hex
Settings	Configuration	0x9236	REG12 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x9237	REG0 Config	H1	0x00	0x03	0x00	Hex
Settings	Configuration	0x9238	HWD Regulator Options	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x9239	Comm Type	U1	0x00	0x1F	0	—
Settings	Configuration	0x923A	I2C Address	U1	0x00	0xFF	0	—
Settings	Configuration	0x923C	SPI Configuration	H1	0x00	0x7F	0x20	—
Settings	Configuration	0x923D	Comm Idle Time	U1	0	255	0	s
Settings	Configuration	0x92FA	CFETOFF Pin Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x92FB	DFETOFF Pin Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x92FC	ALERT Pin Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x92FD	TS1 Config	H1	0x00	0xFF	0x07	Hex
Settings	Configuration	0x92FE	TS2 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x92FF	TS3 Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x9300	HDQ Pin Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x9301	DCHG Pin Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x9302	DDSG Pin Config	H1	0x00	0xFF	0x00	Hex
Settings	Configuration	0x9303	DA Configuration	H1	0x00	0xFF	0x05	Hex

Table 13-37. Data Memory Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Settings	Configuration	0x9304	Vcell Mode	H2	0x0000	0xFFFF	0x0000	Hex
Settings	Configuration	0x9307	CC3 Samples	U1	2	255	80	Num
Settings	Protection	0x925F	Protection Configuration	H2	0x0000	0x07FF	0x0002	Hex
Settings	Protection	0x9261	Enabled Protections A	U1	0x00	0xFF	0x88	Hex
Settings	Protection	0x9262	Enabled Protections B	U1	0x00	0xFF	0x00	Hex
Settings	Protection	0x9263	Enabled Protections C	U1	0x00	0xFF	0x00	Hex
Settings	Protection	0x9265	CHG FET Protections A	U1	0x00	0xFF	0x98	Hex
Settings	Protection	0x9266	CHG FET Protections B	U1	0x00	0xFF	0xD5	Hex
Settings	Protection	0x9267	CHG FET Protections C	U1	0x00	0xFF	0x56	Hex
Settings	Protection	0x9269	DSG FET Protections A	U1	0x00	0xFF	0xE4	Hex
Settings	Protection	0x926A	DSG FET Protections B	U1	0x00	0xFF	0xE6	Hex
Settings	Protection	0x926B	DSG FET Protections C	U1	0x00	0xFF	0xE2	Hex
Settings	Protection	0x9273	Body Diode Threshold	I2	0	32767	50	mA
Settings	Alarm	0x926D	Default Alarm Mask	H2	0x0000	0xFFFF	0xF800	Hex
Settings	Alarm	0x926F	SF Alert Mask A	U1	0x00	0xFF	0xFC	Hex
Settings	Alarm	0x9270	SF Alert Mask B	U1	0x00	0xFF	0xF7	Hex
Settings	Alarm	0x9271	SF Alert Mask C	U1	0x00	0xFF	0xF4	Hex
Settings	Alarm	0x92C4	PF Alert Mask A	U1	0x00	0xFF	0x5F	Hex
Settings	Alarm	0x92C5	PF Alert Mask B	U1	0x00	0xFF	0x9F	Hex
Settings	Alarm	0x92C6	PF Alert Mask C	U1	0x00	0xFF	0x00	Hex
Settings	Alarm	0x92C7	PF Alert Mask D	U1	0x00	0xFF	0x00	Hex
Settings	Permanent Failure	0x92C0	Enabled PF A	U1	0x00	0xFF	0x00	Hex
Settings	Permanent Failure	0x92C1	Enabled PF B	U1	0x00	0xFF	0x00	Hex
Settings	Permanent Failure	0x92C2	Enabled PF C	U1	0x00	0xFF	0x07	Hex
Settings	Permanent Failure	0x92C3	Enabled PF D	U1	0x00	0xFF	0x00	Hex
Settings	FET	0x9308	FET Options	H1	0x00	0xFF	0x0D	Hex
Settings	FET	0x9309	Chg Pump Control	U1	0x00	0xFF	0x01	Hex
Settings	FET	0x930A	Precharge Start Voltage	I2	0	32767	0	mV
Settings	FET	0x930C	Precharge Stop Voltage	I2	0	32767	0	mV
Settings	FET	0x930E	Predischarge Timeout	U1	0	255	5	10ms
Settings	FET	0x930F	Predischarge Stop Delta	U1	0	255	50	10mV
Settings	Current Thresholds	0x9310	Dsg Current Threshold	I2	0	32767	100	userA
Settings	Current Thresholds	0x9312	Chg Current Threshold	I2	0	32767	50	userA
Settings	Cell Open-Wire	0x9314	Check Time	U1	0	255	5	s
Settings	Interconnect Resistances	0x9315	Cell 1 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x9317	Cell 2 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x9319	Cell 3 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x931B	Cell 4 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x931D	Cell 5 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x931F	Cell 6 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x9321	Cell 7 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x9323	Cell 8 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x9325	Cell 9 Interconnect	I2	0	32767	0	mΩ

Table 13-37. Data Memory Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Settings	Interconnect Resistances	0x9327	Cell 10 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x9329	Cell 11 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x932B	Cell 12 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x932F	Cell 13 Interconnect	I2	0	32767	0	mΩ
Settings	Interconnect Resistances	0x9333	Cell 14 Interconnect	I2	0	32767	0	mΩ
Settings	Manufacturing	0x9343	Mfg Status Init	H2	0x0000	0xFFFF	0x0040	Hex
Settings	Cell Balancing Config	0x9335	Balancing Configuration	H1	0x00	0xFF	0x00	Hex
Settings	Cell Balancing Config	0x9336	Min Cell Temp	I1	–128	127	–20	°C
Settings	Cell Balancing Config	0x9337	Max Cell Temp	I1	–128	127	60	°C
Settings	Cell Balancing Config	0x9338	Max Internal Temp	I1	–128	127	70	°C
Settings	Cell Balancing Config	0x9339	Cell Balance Interval	U1	1	255	20	s
Settings	Cell Balancing Config	0x933A	Cell Balance Max Cells	U1	0	16	1	Num
Settings	Cell Balancing Config	0x933B	Cell Balance Min Cell V (Charge)	I2	0	5000	3900	mV
Settings	Cell Balancing Config	0x933D	Cell Balance Min Delta (Charge)	U1	0	255	40	mV
Settings	Cell Balancing Config	0x933E	Cell Balance Stop Delta (Charge)	U1	0	255	20	mV
Settings	Cell Balancing Config	0x933F	Cell Balance Min Cell V (Relax)	I2	0	5000	3900	mV
Settings	Cell Balancing Config	0x9341	Cell Balance Min Delta (Relax)	U1	0	255	40	mV
Settings	Cell Balancing Config	0x9342	Cell Balance Stop Delta (Relax)	U1	0	255	20	mV
Power	Shutdown	0x923F	Shutdown Cell Voltage	I2	0	32767	0	mV
Power	Shutdown	0x9241	Shutdown Stack Voltage	I2	0	32767	600	10mV
Power	Shutdown	0x9243	Low V Shutdown Delay	U1	0	63	1	s
Power	Shutdown	0x9244	Shutdown Temperature	U1	0	150	85	°C
Power	Shutdown	0x9245	Shutdown Temperature Delay	U1	0	254	5	s
Power	Shutdown	0x9252	FET Off Delay	U1	0	127	0	0.25s
Power	Shutdown	0x9253	Shutdown Command Delay	U1	0	254	0	0.25s
Power	Shutdown	0x9254	Auto Shutdown Time	U1	0	250	0	min
Power	Shutdown	0x9255	RAM Fail Shutdown Time	U1	0	255	5	s
Power	Sleep	0x9248	Sleep Current	I2	0	32767	20	mA
Power	Sleep	0x924A	Voltage Time	U1	1	255	5	s
Power	Sleep	0x924B	Wake Comparator Current	I2	500	32767	500	mA
Power	Sleep	0x924D	Sleep Hysteresis Time	U1	0	255	10	s
Power	Sleep	0x924E	Sleep Charger Voltage Threshold	I2	0	32767	2000	10mV
Power	Sleep	0x9250	Sleep Charger PACK-TOS Delta	I2	10	8500	200	10mV
System Data	Integrity	0x91E0	Config RAM Signature	U2	0x0000	0x7FFF	0	Hex
Protections	CUV	0x9275	Threshold	U1	20	90	50	50.6mV
Protections	CUV	0x9276	Delay	U2	1	2047	74	3.3 ms
Protections	CUV	0x927B	Recovery Hysteresis	U1	2	20	2	50.6mV

Table 13-37. Data Memory Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Protections	COV	0x9278	Threshold	U1	20	110	86	50.6mV
Protections	COV	0x9279	Delay	U2	1	2047	74	3.3 ms
Protections	COV	0x927C	Recovery Hysteresis	U1	2	20	2	50.6mV
Protections	COVL	0x927D	Latch Limit	U1	0	255	0	—
Protections	COVL	0x927E	Counter Dec Delay	U1	0	255	10	s
Protections	COVL	0x927F	Recovery Time	U1	0	255	15	s
Protections	OCC	0x9280	Threshold	U1	2	62	2	2mV
Protections	OCC	0x9281	Delay	U1	1	127	4	3.3 ms
Protections	OCC	0x9288	Recovery Threshold	I2	–32768	32767	–200	mA
Protections	OCC	0x92B0	PACK-TOS Delta	I2	10	8500	200	10mV
Protections	OCD1	0x9282	Threshold	U1	2	100	4	2mV
Protections	OCD1	0x9283	Delay	U1	1	127	1	3.3 ms
Protections	OCD2	0x9284	Threshold	U1	2	100	3	2mV
Protections	OCD2	0x9285	Delay	U1	1	127	7	3.3 ms
Protections	SCD	0x9286	Threshold	U1	0	15	0	—
Protections	SCD	0x9287	Delay	U1	1	31	2	15µs
Protections	SCD	0x9294	Recovery Time	U1	0	255	5	s
Protections	OCD3	0x928A	Threshold	I2	–32768	0	–4000	userA
Protections	OCD3	0x928C	Delay	U1	0	255	2	s
Protections	OCD	0x928D	Recovery Threshold	I2	–32768	32767	200	mA
Protections	OCDL	0x928F	Latch Limit	U1	0	255	0	—
Protections	OCDL	0x9290	Counter Dec Delay	U1	0	255	10	s
Protections	OCDL	0x9291	Recovery Time	U1	0	255	15	s
Protections	OCDL	0x9292	Recovery Threshold	I2	–32768	32767	200	mA
Protections	SCDL	0x9295	Latch Limit	U1	0	255	0	—
Protections	SCDL	0x9296	Counter Dec Delay	U1	0	255	10	s
Protections	SCDL	0x9297	Recovery Time	U1	0	255	15	s
Protections	SCDL	0x9298	Recovery Threshold	I2	–32768	32767	200	mA
Protections	OTC	0x929A	Threshold	I1	–40	120	55	°C
Protections	OTC	0x929B	Delay	U1	0	255	2	s
Protections	OTC	0x929C	Recovery	I1	–40	120	50	°C
Protections	OTD	0x929D	Threshold	I1	–40	120	60	°C
Protections	OTD	0x929E	Delay	U1	0	255	2	s
Protections	OTD	0x929F	Recovery	I1	–40	120	55	°C
Protections	OTF	0x92A0	Threshold	U1	0	150	80	°C
Protections	OTF	0x92A1	Delay	U1	0	255	2	s
Protections	OTF	0x92A2	Recovery	U1	0	150	65	°C
Protections	OTINT	0x92A3	Threshold	I1	–40	120	85	°C
Protections	OTINT	0x92A4	Delay	U1	0	255	2	s
Protections	OTINT	0x92A5	Recovery	I1	–40	120	80	°C
Protections	UTC	0x92A6	Threshold	I1	–40	120	0	°C
Protections	UTC	0x92A7	Delay	U1	0	255	2	s
Protections	UTC	0x92A8	Recovery	I1	–40	120	5	°C
Protections	UTD	0x92A9	Threshold	I1	–40	120	0	°C
Protections	UTD	0x92AA	Delay	U1	0	255	2	s
Protections	UTD	0x92AB	Recovery	I1	–40	120	5	°C
Protections	UTINT	0x92AC	Threshold	I1	–40	120	–20	°C
Protections	UTINT	0x92AD	Delay	U1	0	255	2	s
Protections	UTINT	0x92AE	Recovery	I1	–40	120	–15	°C
Protections	Recovery	0x92AF	Time	U1	0	255	3	s

Table 13-37. Data Memory Table (continued)

Class	Subclass	Address	Name	Type	Min Value	Max Value	Default	Units
Protections	HWD	0x92B2	Delay	U2	0	65535	60	s
Protections	Load Detect	0x92B4	Active Time	U1	0	255	0	s
Protections	Load Detect	0x92B5	Retry Delay	U1	0	255	50	s
Protections	Load Detect	0x92B6	Timeout	U2	0	65535	1	hrs
Protections	PTO	0x92BA	Charge Threshold	I2	–32768	32767	250	mA
Protections	PTO	0x92BC	Delay	U2	0	65535	1800	s
Protections	PTO	0x92BE	Reset	I2	0	10000	2	userAh
Permanent Fail	CUDEP	0x92C8	Threshold	I2	0	32767	1500	mV
Permanent Fail	CUDEP	0x92CA	Delay	U1	0	255	2	s
Permanent Fail	SUV	0x92CB	Threshold	I2	0	32767	2200	mV
Permanent Fail	SUV	0x92CD	Delay	U1	0	255	5	s
Permanent Fail	SOV	0x92CE	Threshold	I2	0	32767	4500	mV
Permanent Fail	SOV	0x92D0	Delay	U1	0	255	5	s
Permanent Fail	TOS	0x92D1	Threshold	I2	0	32767	500	mV
Permanent Fail	TOS	0x92D3	Delay	U1	0	255	5	s
Permanent Fail	SOCC	0x92D4	Threshold	I2	–32768	32767	10000	userA
Permanent Fail	SOCC	0x92D6	Delay	U1	0	255	5	s
Permanent Fail	SOCD	0x92D7	Threshold	I2	–32768	32767	–32000	userA
Permanent Fail	SOCD	0x92D9	Delay	U1	0	255	5	s
Permanent Fail	SOT	0x92DA	Threshold	I1	–40	120	65	°C
Permanent Fail	SOT	0x92DB	Delay	U1	0	255	5	s
Permanent Fail	SOTF	0x92DC	Threshold	U1	0	150	85	°C
Permanent Fail	SOTF	0x92DD	Delay	U1	0	255	5	s
Permanent Fail	VIMR	0x92DE	Check Voltage	I2	0	5500	3500	mV
Permanent Fail	VIMR	0x92E0	Max Relax Current	I2	10	32767	10	mA
Permanent Fail	VIMR	0x92E2	Threshold	I2	0	5500	500	mV
Permanent Fail	VIMR	0x92E4	Delay	U1	0	255	5	s
Permanent Fail	VIMR	0x92E5	Relax Min Duration	U2	0	65535	100	s
Permanent Fail	VIMA	0x92E7	Check Voltage	I2	0	5500	3700	mV
Permanent Fail	VIMA	0x92E9	Min Active Current	I2	10	32767	50	mA
Permanent Fail	VIMA	0x92EB	Threshold	I2	0	5500	200	mV
Permanent Fail	VIMA	0x92ED	Delay	U1	0	255	5	s
Permanent Fail	CFETF	0x92EE	OFF Threshold	I2	10	5000	20	mA
Permanent Fail	CFETF	0x92F0	OFF Delay	U1	0	255	5	s
Permanent Fail	DFETF	0x92F1	OFF Threshold	I2	–5000	–10	–20	mA
Permanent Fail	DFETF	0x92F3	OFF Delay	U1	0	255	5	s
Permanent Fail	VSSF	0x92F4	Fail Threshold	I2	1	32767	100	—
Permanent Fail	VSSF	0x92F6	Delay	U1	0	255	5	s
Permanent Fail	2LVL	0x92F7	Delay	U1	0	255	5	s
Permanent Fail	LFOF	0x92F8	Delay	U1	0	255	5	s
Permanent Fail	HWMX	0x92F9	Delay	U1	0	255	5	s
Security	Settings	0x9256	Security Settings	H1	0x00	0x07	0x00	Hex
Security	Keys	0x9257	Unseal Key Step 1	U2	0x0100	0xFFFF	0x0414	Hex
Security	Keys	0x9259	Unseal Key Step 2	U2	0x0100	0xFFFF	0x3672	Hex
Security	Keys	0x925B	Full Access Key Step 1	U2	0x0100	0xFFFF	0xFFFF	Hex
Security	Keys	0x925D	Full Access Key Step 2	U2	0x0100	0xFFFF	0xFFFF	Hex

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (November 2021) to Revision C (May 2022)	Page
• Described effects of ADC saturation	17
• Corrected the VREF1 value used in calculations	20
• Clarified the requirement to send *RESET_PASSQ()*	20
• Clarified units for ADC counts. Corrected names of pin raw counts entries	22
• Corrected VREF1 voltage level and associated calculations	26
• Added the instruction to do a full reset to clear PFs	47
• Updated description	55
• Clarified the requirement to first transition from SEALED mode to UNSEALED mode before transitioning to FULLACCESS mode	71
• Removed the *PF_RESET()* subcommand, which is no longer recommended for use	77
• Updated bit descriptions	105
• Removed the *PF_RESET()* subcommand, which is no longer recommended for use	106

Changes from Revision A (May 2021) to Revision B (November 2021)	Page
• Updated *Subcommands with Data*	108

Changes from Revision * (January 2021) to Revision A (May 2021)	Page
• Clarified reserved bits	13
• Updated addresses of cell voltage commands	17
• Clarified the measurement loop slowdown feature	17
• Updated the description of units for ADC counts	21
• Updated the description of the units for ADC counts	22
• Modified the ***CC Gain*** formula. Changed "CC Offset" to "Board Offset"	28
• Removed reference to zero delay setting	41
• Updated the description of the timing of cell open wire checks	51
• Expanded description of *MANU_DATA()* subcommand	54
• Deleted information about disabling FETs using commands	60
• Added a FET turn-on timing description	62
• Detailed settings for Wake Comparator speed	66
• Updated the subcommand usage in UNSEALED and FULLACCESS modes and the ***Auto Shutdown Time*** operation descriptions	68
• Clarified delays associated with commands and subcommands, and updated terminology	73
• Updated terminology	75
• Updated the command/subcommand timing table, as well as terminology	77
• Updated terminology	83
• Updated the *CB_ACTIVE_CELLS()* timing description, added more details associated with cell balancing	85
• Changed reserved bits to WK_SPD bits	135

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265