Application Report
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Adaptive Constant On-Time (D-CAP™) Control Study in Notebook Applications

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ABSTRACT

The buck converters with adopted voltage mode, current mode, constant on-time control, and adaptive on time control (D-CAP™ mode) are discussed in detail in terms of their control methods, and their transient performances. The advantages of the D-CAP™ mode applicable to the portable applications are presented based on this analysis. The jitter mechanism in the D-CAP™ mode is studied, and an improvement method is introduced. The comparison of the jitter performance is presented with TPS51124 which implemented the silicon solution of ramp compensation.

1 Introduction

There are varieties of control techniques used for buck converters. These control approaches consist of voltage mode, current mode, hysteretic mode, constant on-time mode, constant off time mode, and adaptive on-time mode (D-CAP™ mode). Both voltage mode and current mode require loop compensation circuitry for achieving a stable operation at the wide range of input voltage range and are must be redesigned based on the different power stage design.

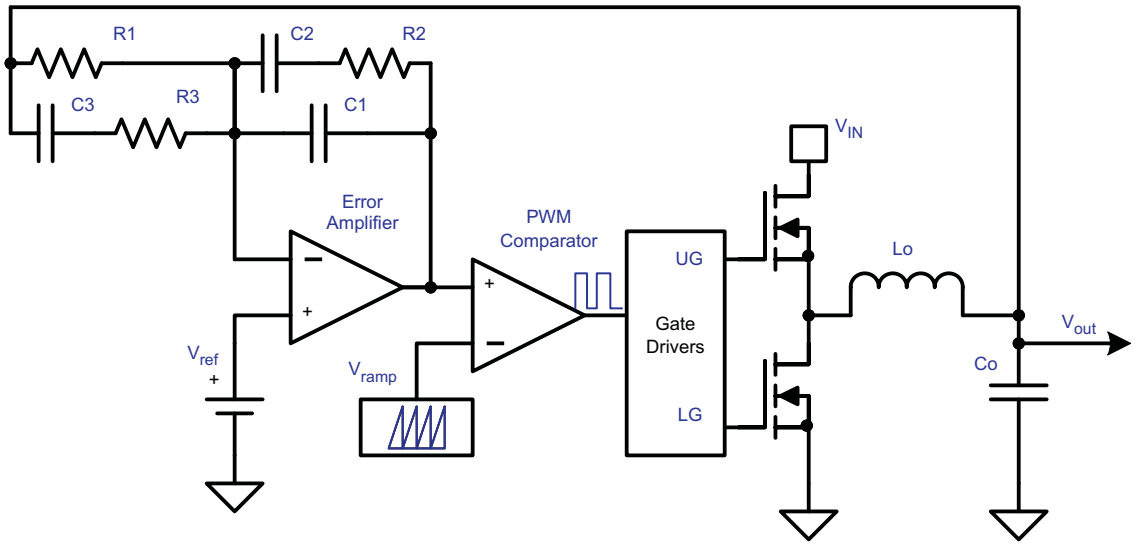

Figure 1. Voltage Mode

Also both control modes need a high performance Error Amplifier which increases the operation current of IC[1] as shown in Figure 1 and Figure 2. This is an obstacle to achieving high efficiency at light load operation.

In the present mobile application market, the fast transient is one of the most critical design parameters to meet while minimizing the output capacitance and cost.

D-CAP is a trademark of Texas Instruments.

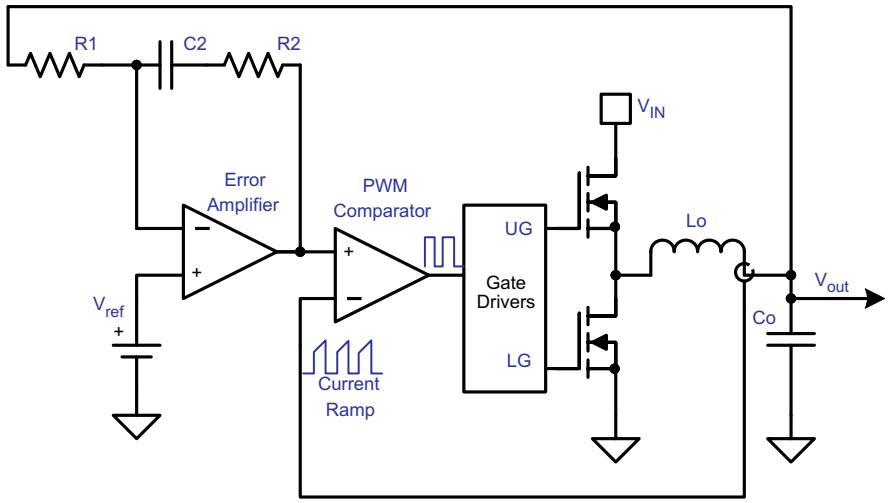

Figure 2. Peak Current Mode

Another important requirement is the light load efficiency for extending the battery run-time. In order to get high light load efficiency, the mode change is needed for both voltage mode and current mode. The emulated diode mode in the discontinuous conduction mode (DCM) with fixed switching frequency does not meet the light load efficiency requirement due to its relative high switching losses. Normally, the hysteresis control mode or pulse frequency modulation (PFM) is used at DCM to reduce the switching loss, gate drive loss, and to improve the light load efficiency as shown in Figure 4.

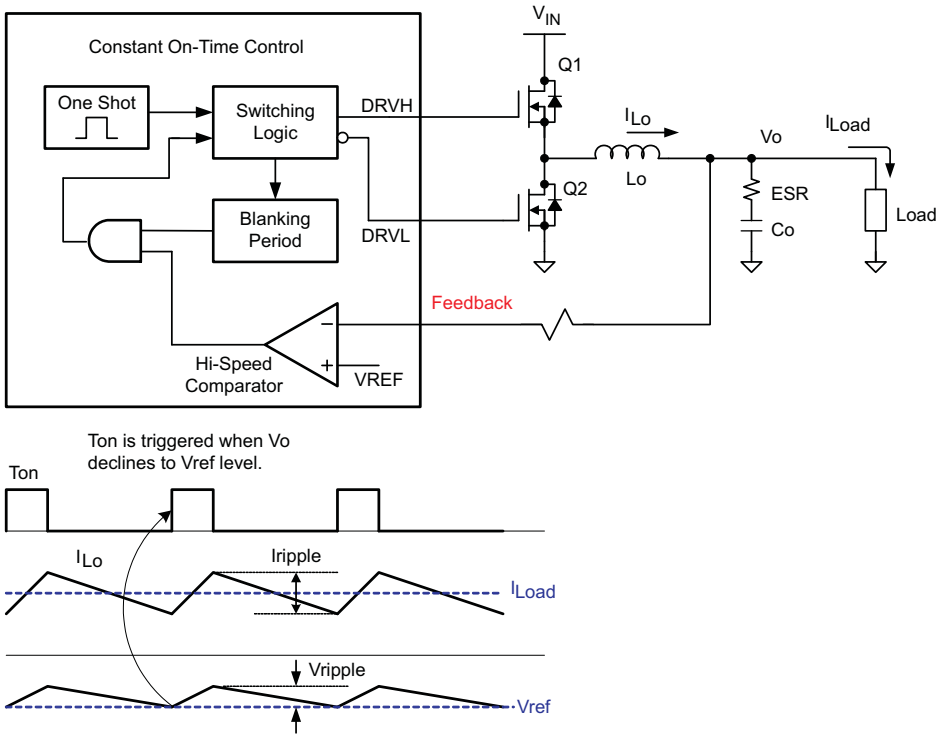

Figure 3. Constant on Time Mode

This architecture has inherent drawbacks during the PFM mode to PWM mode transition. The transition is not smooth due to the comparator to Error Amplifier switching during the mode change, In order to achieve good light load efficiency, the Error Amplifier works in the idle condition in the skip mode. Because of this, during the mode transition, the Error Amplifier can not respond fast enough to the mode change. It causes an additional voltage dip due to the circuit wake-up delay as shown in Figure 5.

Figure 3 shows the constant on-time control block diagram. This control method uses the output ripple as a PWM ramp signal to compare with the reference voltage to regulate the voltage, It has several advantages over voltage mode and current mode. First, it does not require loop compensation network and makes design easier. Second, it can achieve a fast transient response because it no longer employs the error amplifier for voltage regulation. In addition, it has seamless transition from PFM in the light load condition to pseudo PWM mode in the heavy load condition as shown in Figure 6. However, the switching frequency changes with input voltage and load condition which makes this kind of control modes unattractive in the portable application. Adaptive on-time control (D-CAP™ mode) is able to dynamically adjust the on-time duration based on the input voltage, output voltage, and load current so that it can achieve relative constant frequency operation. It not only inherits the merit of ripple mode control scheme mentioned above, but also keeps relatively stable switching frequency during its static operation which minimizes the EMI interference at some sensitive bands of certain frequencies in the system. Figure 7 shows the simplified block diagram of a buck converter using D-CAP™ mode.

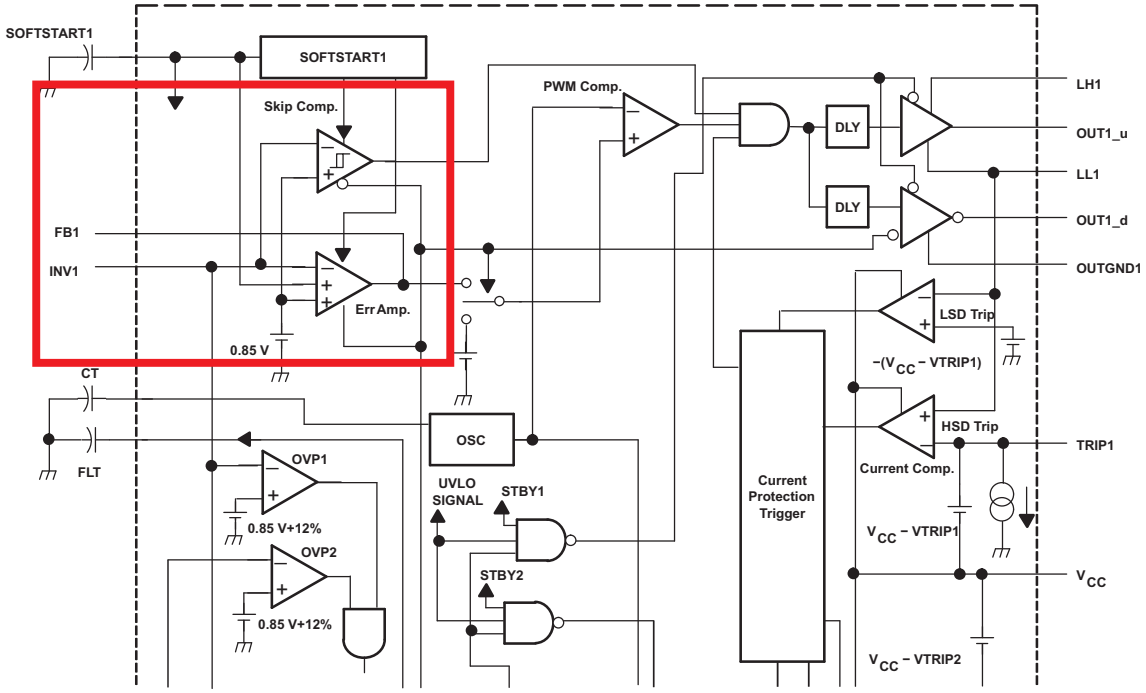

Figure 4. Voltage Mode Controller With Hysteretic Control Mode at Light Load

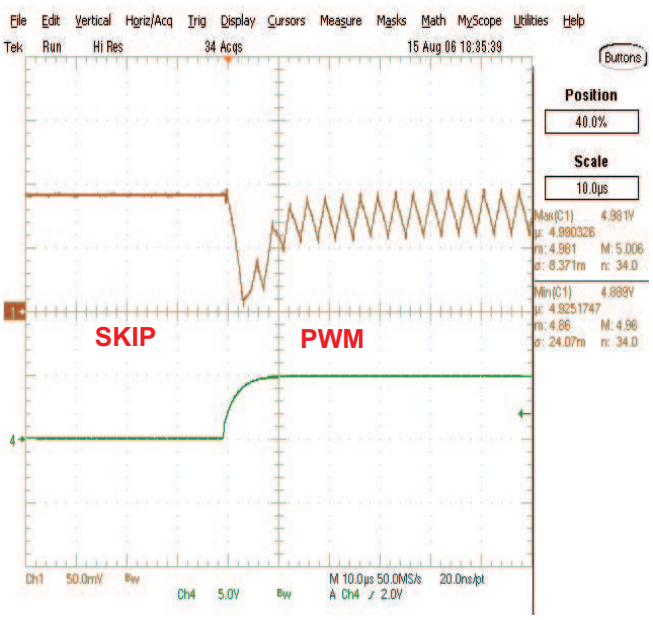

Figure 5. Voltage Mode IC

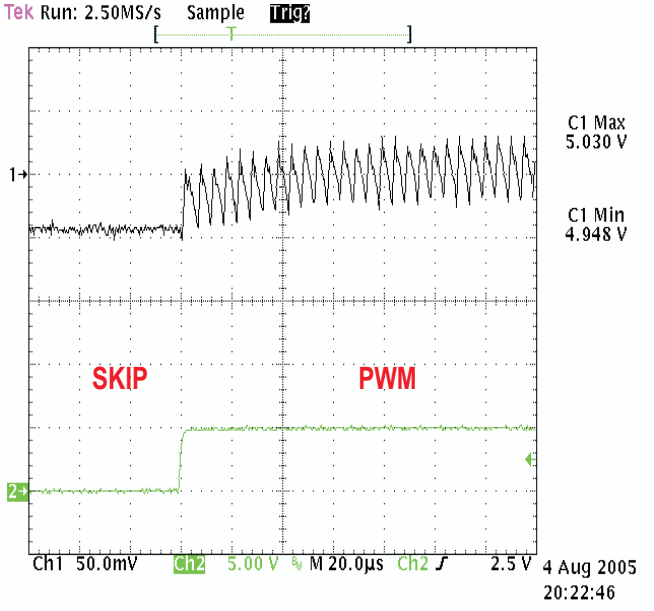

Figure 6. Adaptive On-Time Mode IC

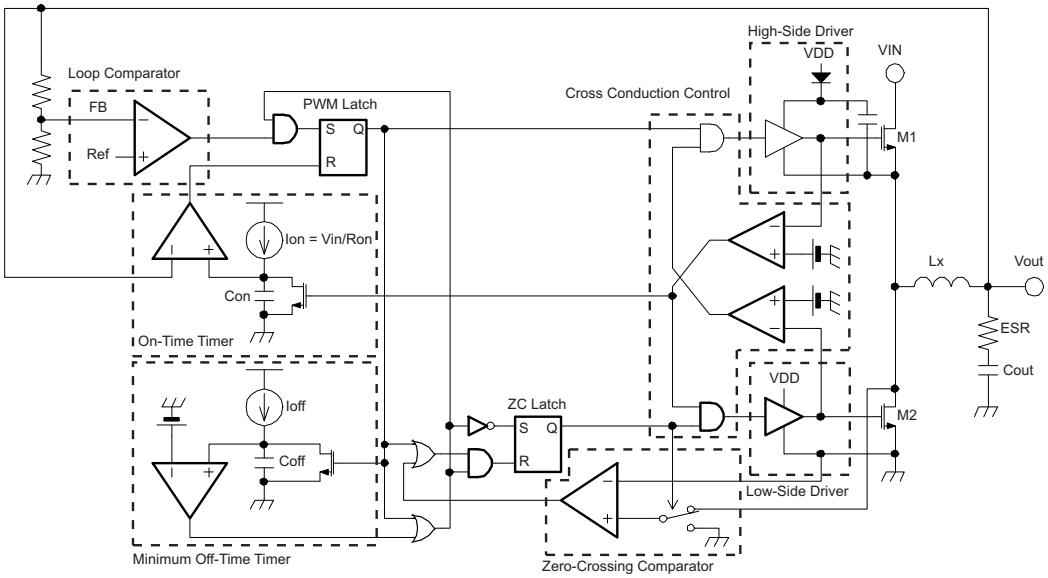

Figure 7. D-CAP™ Mode Block Diagram

1.1 D-CAP™ Mode Operation[3]

D-CAP™ mode means *Direct connection to the output CAPacitor*

Basic Operation Principle

At the beginning of each cycle, the high side MOSFET (M1) is turned on. M1 is turned off after internal one shot timer expires. This one shot time is determined by feed forwarding input voltage VIN and output voltage VOUT to keep frequency fairly constant over input voltage range. Hence, it is called adaptive on-time control. M1 is turned on again when feedback voltage is below the reference voltage. The synchronous rectified MOSFET (M2) is turned on when the M1 is in OFF state to minimize the conduction loss. M2 is turned off when inductor current reaches to zero current. This enables seamless transition to the reduced frequency operation at light load condition so that high efficiency is kept over broad range of load current.

1.2 Stability Consideration

Typically, the loop transfer function is derived as a function of the output voltage. If in D-CAP™ mode, the output voltage is directly compared by the PWM comparator. Theoretically, the gain and the bandwidth of a comparator are infinite. As a result, the loop gain from the output node becomes infinite. This means that the loop transfer function which uses the output node voltage as a state variable is not derivable and is not measurable as well. As for the loop transfer function for stability analysis, a loop transfer function which uses an intrinsic capacitance node voltage as a state variable is derivable.

Figure 8 shows a simple block diagram of D-CAP™ mode DC/DC converter. In the steady-state, the output voltage is given by:

$$Vo = Vc + I_C \times ESR = const. \quad (1)$$

Figure 9 shows a simple block diagram of current mode DC/DC converter. In the steady-state, the voltage before the sensing resistor is given by:

$$Vx = Vo + I_L \times Rs = const. \quad (2)$$

Basically, both equations are the same excluding effects from the load. As far as stability consideration, this means that D-CAP™ mode is same as current mode which uses ESR as sensing resistor.

The pulse width modulator including the inductor is linearized as a transconductance of $1/R_{ESR}$. The loop transfer function is given by the next equation.

$$H(s) = \frac{1}{s \times R_{ESR} \times Co} \quad (3)$$

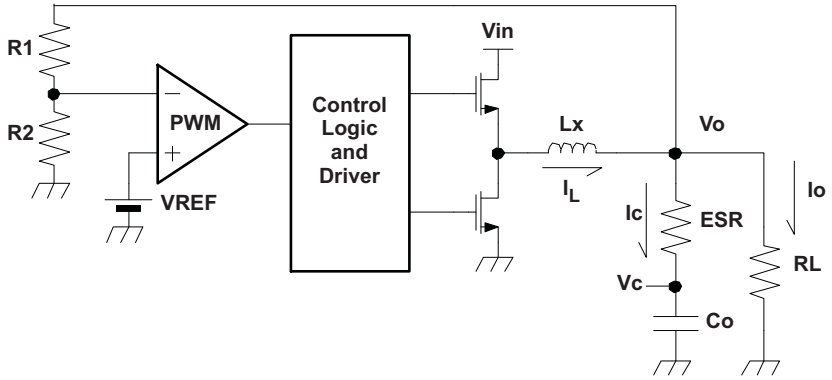

Figure 8. D-CAP™ Mode Converter Simple Diagram

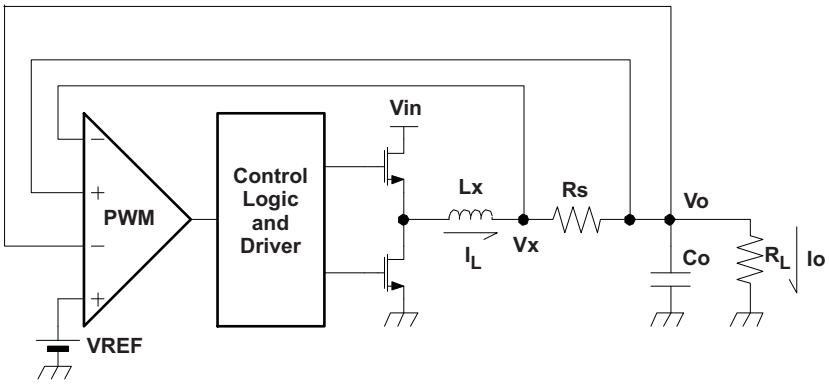

Figure 9. Current Mode Converter Simple Diagram

The equation is usable up to half of the switching frequency because of state averaging method limitation. The sufficient condition of stability can be achieved by setting the 0-dB frequency below half of the switching limitation as below.

$$\frac{f_{SW}}{K} > \frac{1}{2\pi \times R_{ESR} \times Co} \quad (4)$$

The value from 3 to 4 is appropriate for K.

1.3 Jitter at D-CAP™ Mode

Compared to the other topologies, adaptive constant on-time control shows great advantages from the load transient performance. However, its jitter performance still needs to be optimized. It requires minimum output ripple in order to be stable. There is a misunderstanding on how to reduce the jitter because of this requirement.

Does the jitter performance directly relate to the magnitude of the ripple? To answer this question, go back to determine how it regulates the output voltage. The turn-on of the top side MOSFET occurs when the falling edge of the scaled output ripple drops to the reference voltage. Essentially, the noise added on the down slope of the output ripple will affect when the top side MOSFET is being turned on. If this noise is significant, turn-on edge jitter can be significant as well.

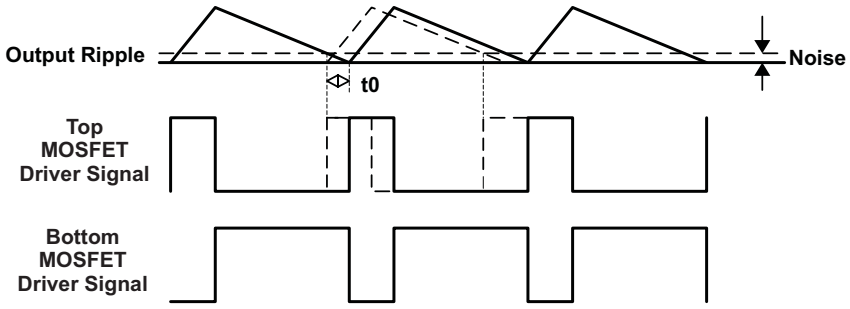

Figure 10.

As shown in Figure 10, due to noise on the down slope of the output ripple, t0 period of uncertainty can be observed at turn-on edge of the top MOSFET. This uncertainty causes the on-time jitter. From the above analysis, it is clear the magnitude of the output ripple does not affect the jitter. Then, why are most ripple mode converters requiring the minimum amount of output ripple as stated in many of our competitor's data sheets?

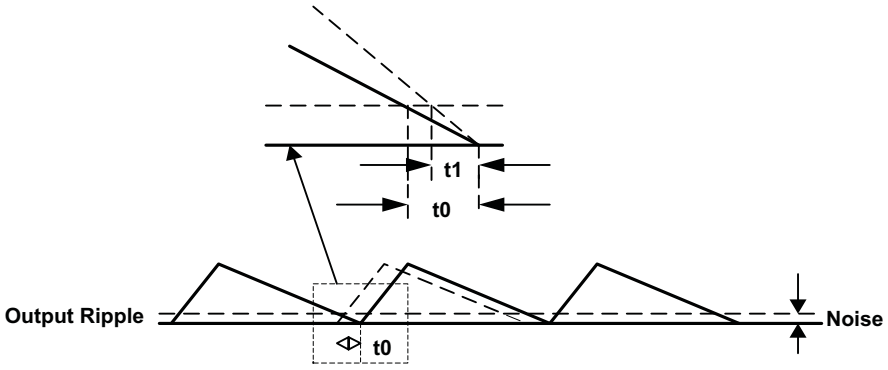

Figure 11.

Zoom in the turn on edge of top MOSFET in the Figure 11, by increasing the down slope of the output ripple, jitter time is reduced from t0 to t1. The down slope of the output ripple of the feedback pin is described by the following equations.

$$L \times \frac{di}{dt} = -Vo \quad (5)$$

Where L is the output filter inductance, Vo is output voltage. Equation 5 describes the relationship between the output voltage and the inductor current rate of change during off-time. Move L to the left and multiply Esr on the both side of the equation, where Esr is ESR value of the output cap, provides the following equation.

$$Esr \frac{di}{dt} = \frac{-Esr \times Vo}{L} \tag{6}$$

Shuffle Equation 6.

$$Esr \times di = \frac{-Esr \times Vo \times dt}{L} \tag{7}$$

The assumption used here is that the output capacitance is big enough so that the out ripple will only be decided by the ripple current and ESR of the output cap. Rearrange Equation 7 and multiply R2/(R1+R2) on both sides of the equation, where R1, R2 are the voltage divider resistors shown in Figure 1.

$$Sr = \frac{-Esr \times Vo}{L} \times \frac{R2}{R1 + R2} \tag{8}$$

Where Sr is down slope of the scaled output ripple on feedback pin

since $Vref = Vo \times \frac{R2}{R1 + R2}$

$$Sr = \frac{-Esr \times Vref}{L} \tag{9}$$

From Equation 9 and Equation 7, it is discovered that Sr and the magnitude of the output ripple both are proportional to $\frac{Esr}{L}$. However, in order for the ripple mode converter to be stable, it is not the magnitude of the output ripple that matters, but the down slope of the feedback voltage.

1.4 Ramp Compensation in the D-CAP™Mode

After analyzing the mechanism of the jitter in the D-CAP™ mode, ramp compensation is chosen to improve the jitter performance.

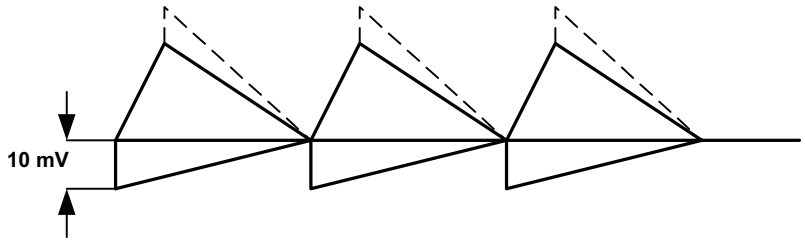

Figure 12.

In Figure 12, 10-mV ramp compensation is added on the feedback pin. The down slope of the scaled output ripple on the feedback pin is increased which helps the jitter performance of the D-CAP™ mode. Figure 13 shows two waveforms, one with ramp compensation and the other without. The one with the ramp compensation shows much improved jitter performance.

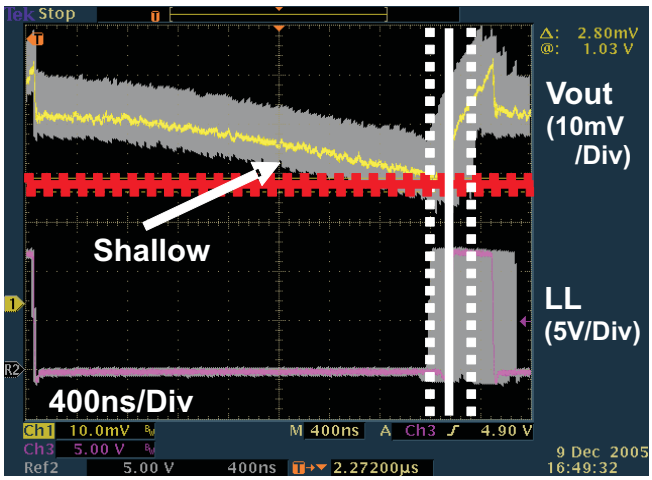

Figure 13. Without Ramp Compensation

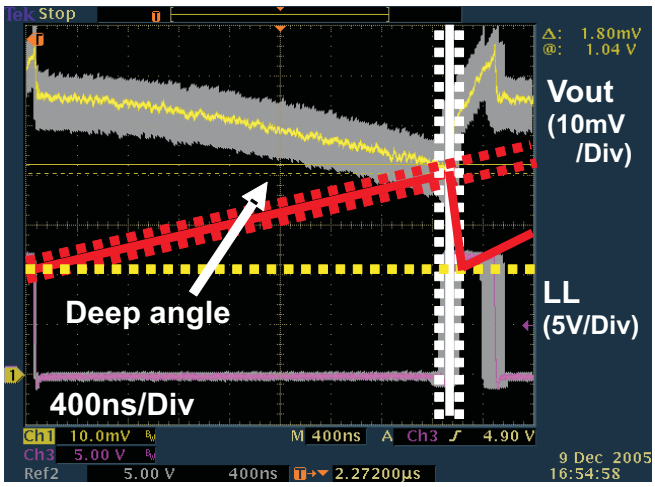

Figure 14. With Ramp Compensation on Vout1 10mv/DIV 1.05V Offset

2 Conclusion

TI's D-CAP™ for mobile application has the stable switching frequency at normal operation, smooth transition between skip mode to PWM mode, fast transient response, easy of use and improved jitter performance.

3 Reference

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2. R. Redl and N.O.Sokal, *Current-mode control, five different types, used with the three basic classes of power converters: Small-signal ac and large-signal dc characterization, stability requirements, and implementation of practical circuits*, in IEEE Power Electron. Spec. Conf. Rec., 1985, pp.771-785
3. Tetsuo Tateishi *The D-CAPT™ mode operation and an implementation of the OOATM skip mode*, TI's Integrated Power conference 2005

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