Application Report
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A Power-Distribution Switch With Latched Overcurrent Protection

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ABSTRACT

Power-distribution switches, like the TPS203x, operate in retry mode in an overload, but some applications require the switch to latch off. The latch-off function can be implemented using the simple circuit described in this application report.

1 Introduction

The Texas Instruments TPS202x, TPS203x, TPS204x, TPS205x, TPS206x, TPS208x, and TPS209x power distribution switches limit the current into a fault by switching to constant-current mode. If a fault causes the switch junction-temperature to rise above a preset level, then a thermal protection circuit shuts off the switch to prevent damage. Recovery from thermal shutdown is automatic once the switch has cooled sufficiently. In a sustained fault, the switch cycles between current limit and thermal shutdown. In some systems, it may be preferable to simply latch off the switch under this condition. In a battery-powered system like a laptop computer, for example, latching off the switch has the advantage of eliminating unnecessary battery drain by a *dead* load. This latch-off function can be implemented with a few inexpensive and readily available logic gates around the switch.

2 Latching Off Is Easy

The circuit in Figure 1 uses a SN74HC00 quad-NAND gate to implement overcurrent latch off. The SN74HC00 high-speed CMOS logic gate is selected for this application, not for its speed, but because it operates over the 2.7-V to 5.5-V range of the TPS2034D switch.

The TPS2034D switch is active-high enable. An active-low enable switch like the TPS2014 must be driven by the U1:A output instead of U1:B output.

At power up, ENABLE must be at logic 0 until VCC is stable to ensure that the switch initializes in the off state. After VCC is stable, logic 1 at ENABLE turns on the switch. In an overcurrent condition, OC# momentarily pulls low which latches FAULT# at logic 0 and disables the switch. The host can monitor FAULT# for an overcurrent condition. Toggling ENABLE resets FAULT# and re-enables the switch.

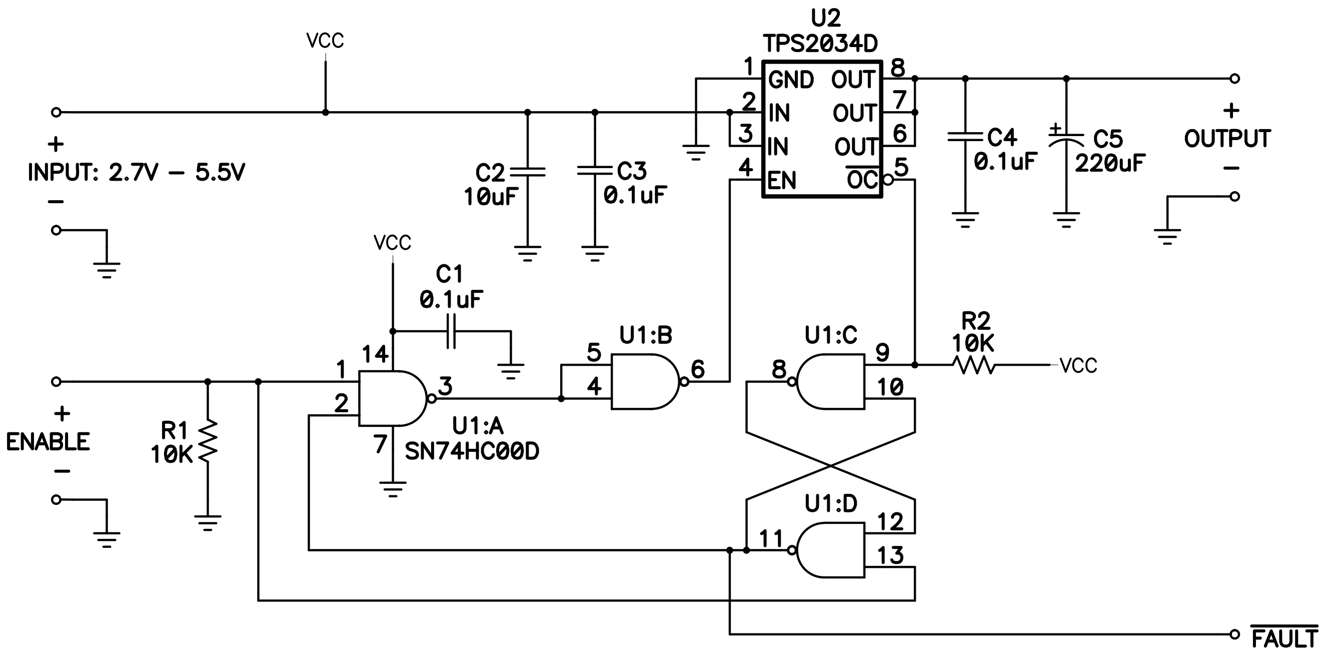

Figure 1. Overcurrent Latch Off Using Quad-NAND Gate

3 Circuit Performance

For the waveforms in Figure 2 through Figure 4, CH1 = ENABLE, CH2 = OC#, CH3 = FAULT#, and CH4 = Current at the 2.7-V to 5.5-V input.

Figure 2 shows the circuit waveforms if the switch is enabled into a 2-Ω load.

Figure 3 shows the circuit waveforms if the switch is enabled into a dead short.

Figure 4 shows the circuit waveforms if the enabled-switch output is short circuited. The input-power distribution resistance specific to this set-up and the high surge current cause the channel 1 and channel 2 voltages to droop when the switch output is short circuited.

Note that OC# (channel 2) pulls to logic 0 for a brief period in an overcurrent condition. The OC# output is not as useful a fault indicator as is the FAULT# output.

The load inrush-current must be less than the short-circuit output current (I_{OS}) of the switch to prevent the switch from turning off prematurely when enabled. This can limit the amount of load bypass-capacitance.

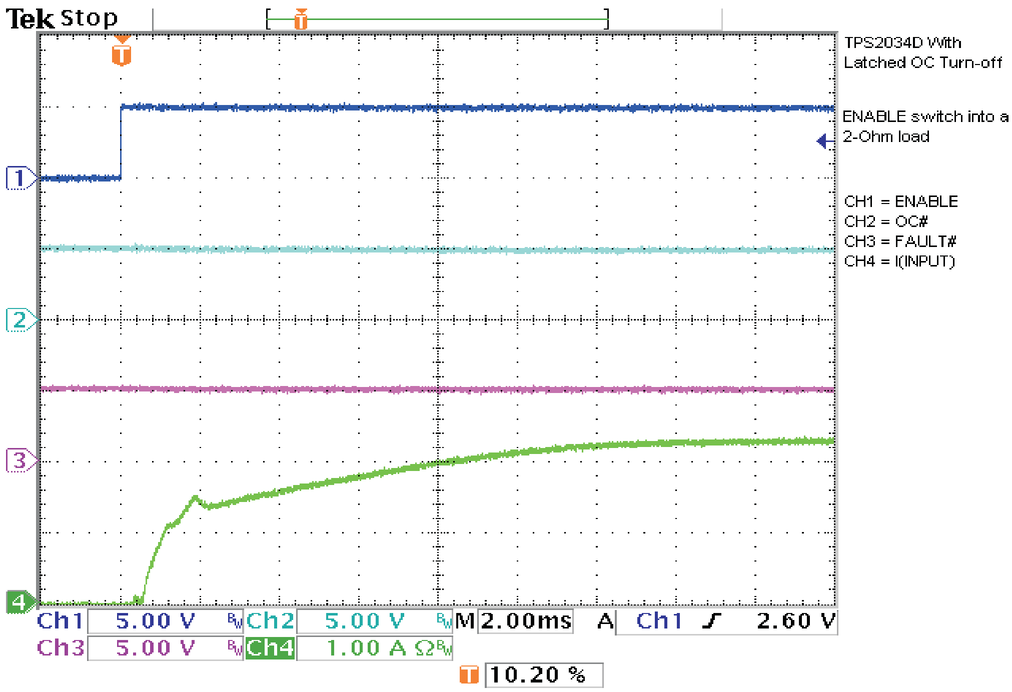

Figure 2. Switch Is Enabled Into 2-Ω Load

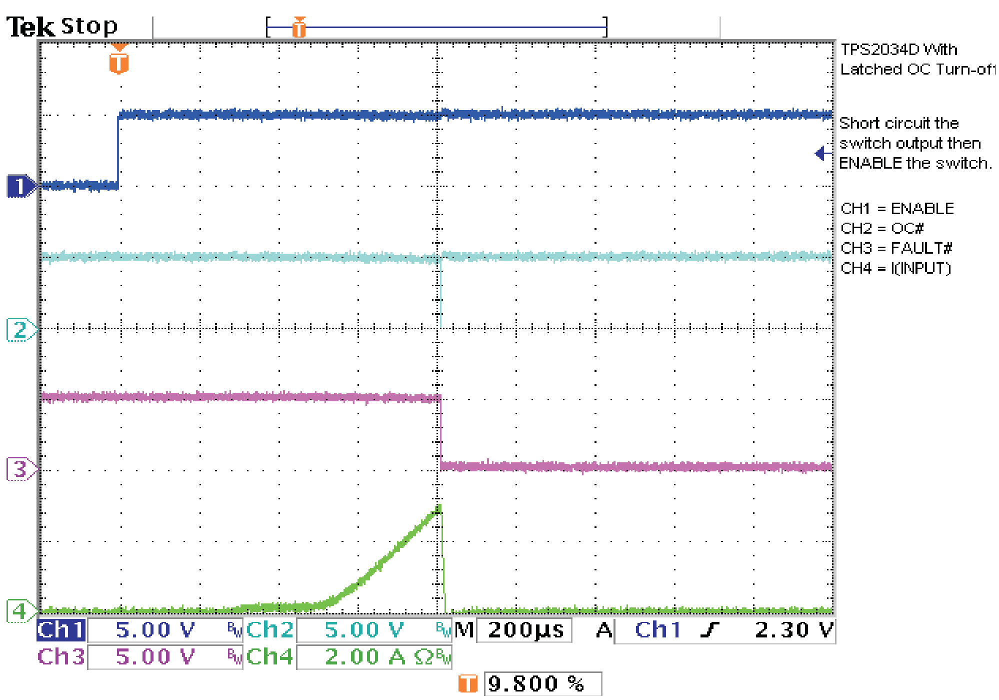

Figure 3. Switch Is Enabled Into Short Circuit

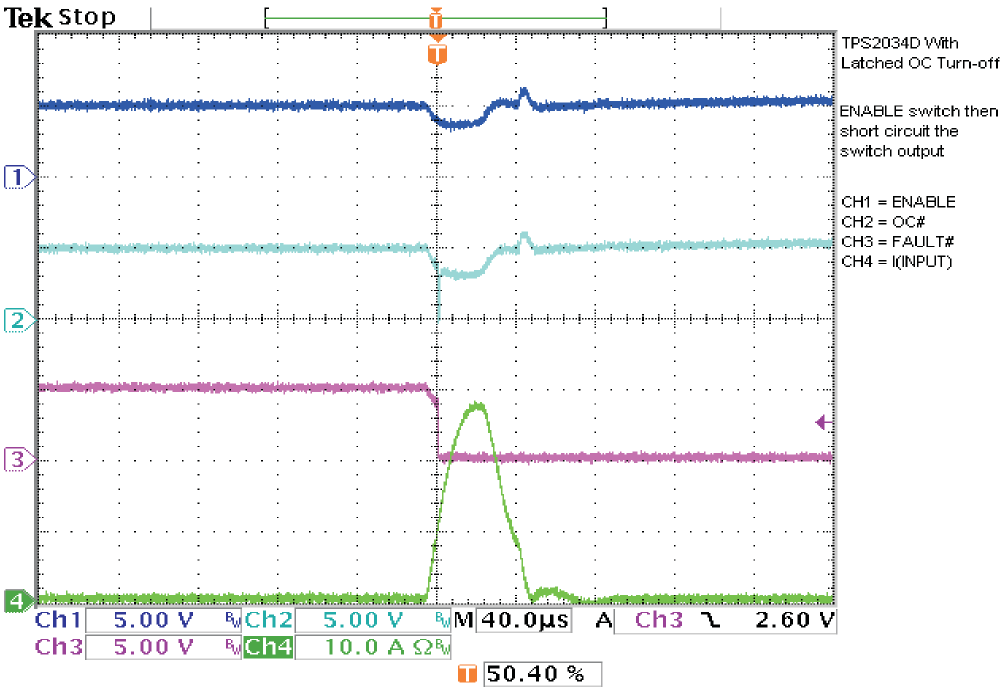

Figure 4. Enabled-Switch Output Is Short Circuited

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