Application Report
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Create an Inverting Power Supply Using a TPS54202 Buck Converter With Internal Compensation

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ABSTRACT

The TPS54202 device is a 4.5-V to 28-V input voltage range, 2-A synchronous buck converter. By integrating MOSFETs, internal loop compensation, internal 5-ms soft start, and employing the SOT-23 package, the TPS54202 device achieves high power density and offers a small footprint on the PCB. This device is well-suited for applications such as a 12-V, 24-V distributed power-bus supply, white goods, audio, STB, DTV, and printers. Moreover, with its internal compensation, the TPS54202 device can be configured in an inverting buck-boost topology, where the output voltage is inverted or negative with respect to ground, even without any more compensation components. This application report describes the TPS54202 device in an inverting buck-boost topology, for use in low-current negative rails for an operational amplifier, optical module biasing, or line drivers and other low-power applications. This application report also discusses how to choose an output LC filter in the buck-boost topology to achieve applicable transient and steady performance.

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1 Configuring the Buck Converter for Inverting Buck-Boost Topology Application

The inverting buck-boost topology is similar to the buck topology. In the buck configuration, shown in Figure 1, the positive connection (V_{OUT}) is connected to the inductor, and the return connection is connected to the integrated circuit (IC) ground (GND). However, in the inverting buck-boost configuration, shown in Figure 2, the IC GND is used as the negative output voltage pin. What was the positive output in the buck configuration is used as the GND. This inverting topology allows the output voltage to be inverted and always lower than the GND.

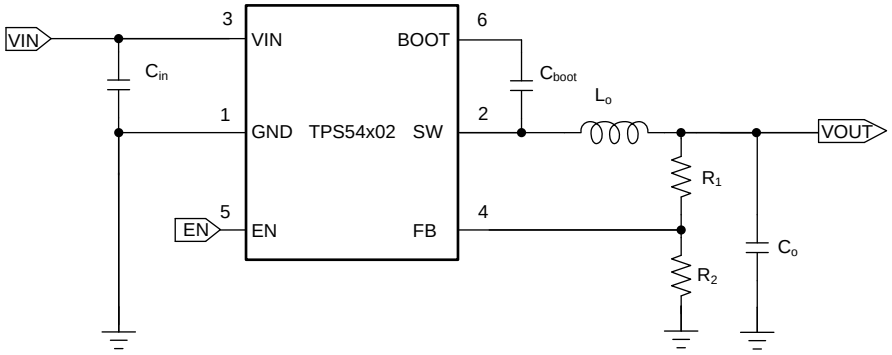

Figure 1. Buck Converter Application

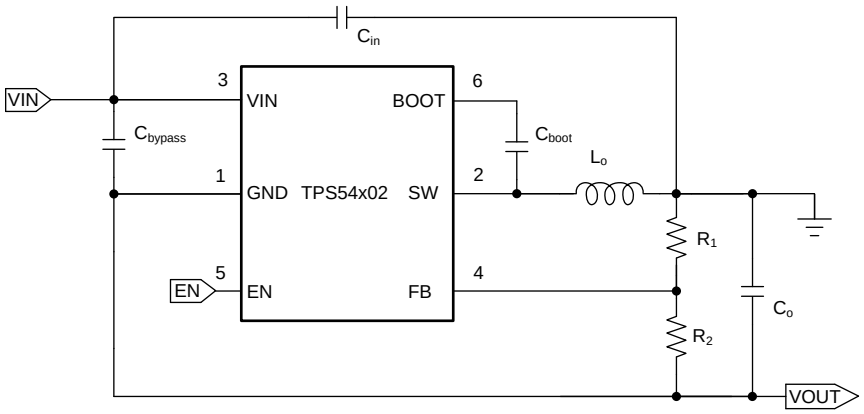

Figure 2. Buck-Boost Converter Application

The circuit operation in the inverting buck-boost topology is different from the buck topology. Figure 3 (a) shows that the output voltage terminals are reversed, though the components are wired the same as a buck converter. During the on time of the control MOSFET, shown in Figure 3 (b), the inductor is charged with current while the output capacitor supplies the load current. The inductor does not provide current to the load during that time. During the off time of the control MOSFET and the on time of the synchronous MOSFET, shown in Figure 3 (c), the inductor provides current to the load and the output capacitor. These changes affect many parameters as described in the upcoming sections.

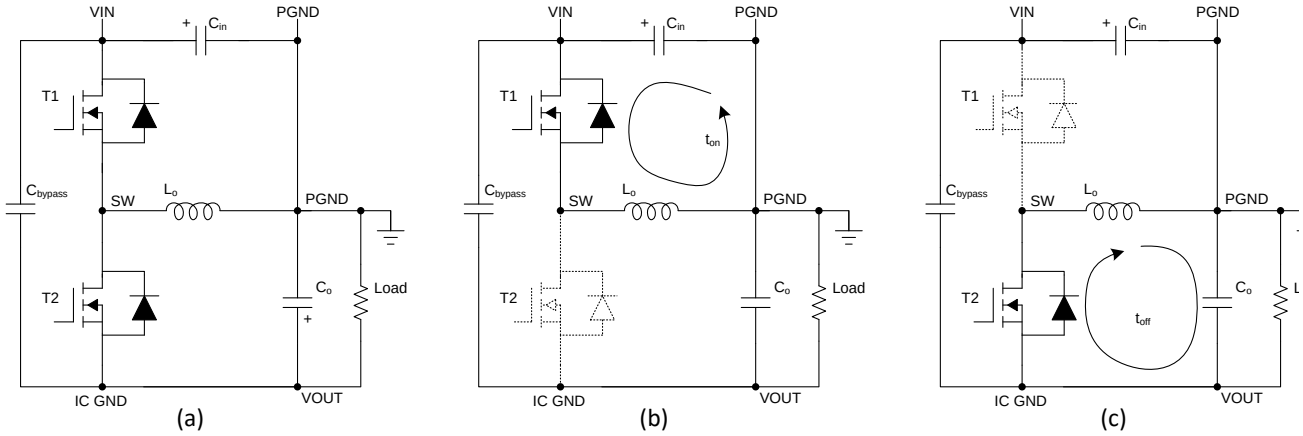

Figure 3. Inverting Buck Boost Configuration

2 Choosing the Right Buck Converter for Inverting Power Application

When choosing the TPS54202 device for inverting power application, you must confirm whether this device can withstand the I/O voltage and output current of the inverting power application.

2.1 Output Voltage Range

The output voltage range is the same as when configured as a buck converter, but negative. So, the output voltage for the inverting buck boost topology should be set between –0.6 V and –26 V. The output voltage is set the same way as in the buck configuration, with two resistors connected to the FB pin. Due to the increased noise of the inverting buck boost topology, and for a more robust design, use smaller value resistors than what are used for the buck configuration.

2.2 Input Voltage Range

The input voltage that can be applied to an inverting buck boost converter IC is less than the input voltage that can be applied to the same buck converter IC. This is because the ground pin of the IC is connected to the (negative) output voltage. Therefore, the input voltage across the device is V_{IN} to V_{OUT}, not V_{IN} to ground. Thus, the input voltage range of the TPS54202 device is 4.5 V to 28 V – V_{OUT}, where V_{OUT} is a positive value.

2.3 Output Current Range

In the buck configuration, the average inductor current equals the average output current because the inductor always supplies current to the load during both the on and off times of the control MOSFET. However, in the inverting buck boost configuration, the load is supplied with current only from the output capacitor and is completely disconnected from the inductor during the on time of the control MOSFET. During the off time, the inductor connects to both the output capacitor and the load (see Figure 3).

So, the peak current of the MOSFET and inductor can easily be calculated, as follows in Equation 1, Equation 2, Equation 3, and Equation 4.

$$I_{peak} = I_{Lavg} + \frac{\Delta I_L}{2} \quad (1)$$

Where:

$$I_{Lavg} = \frac{I_{OUT}}{1 - D} \quad (2)$$

$$\Delta I_L = \frac{V_{IN} \times D}{f_S \times L} = \frac{V_{OUT} \times (1 - D)}{f_S \times L} \quad (3)$$

$$D = \frac{V_{OUT}}{V_{IN} + V_{OUT}} \quad (4)$$

When V_{IN} is increased and V_{OUT} is kept constant, the duty cycle, D, and I_{Lavg} decrease, while ΔI_L increases. You can see that the sum of I_{Lavg} and ΔI_L decreases. So, when V_{IN} is at the minimum, you can get the maximum I_{peak}. You must choose an applicable inductor, L, to keep the maximum I_{peak} lower than the minimum current limit, $I_{cl(min)}$ of the device. Therefore, you get Equation 5, as follows:

$$I_{OUTmax} < (1 - D_{max}) I_{LIM\_HS} - \frac{V_{INmin} D_{max} (1 - D_{max})}{2 f_S L} \quad (5)$$

You can get the I_{OUTmax} versus L_{min} graph of the TPS54202 device, shown in Figure 4. For the TPS54202 device, I_{lim_HS} = 2.5 A and f_s = 500 kHz. From Figure 4, you can see that by increasing the inductor and V_{INmin}, or decreasing the output voltage level, this device can hold more output current in the buck-boost application.

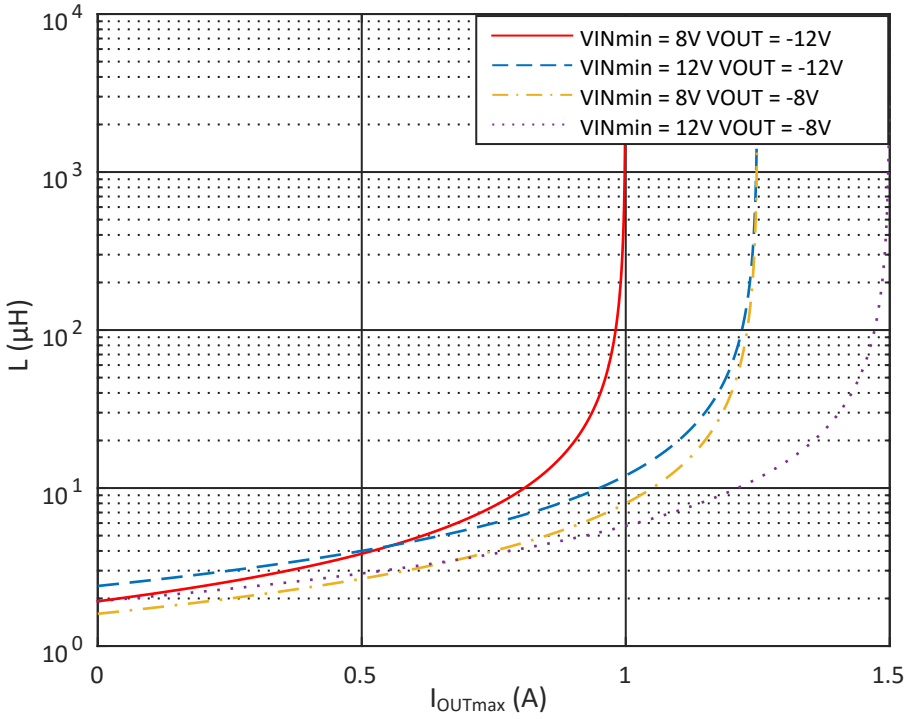

Figure 4. Output Current Range Versus Inductor L

3 Selecting Applicable External Components for Inverting Power Application

When the appropriate buck converter is chosen, shown in Figure 5, you must choose the correct external components such as a resistor divider, inductor, input capacitor, output capacitor, and bypass capacitor, for high, steady, and transient performance.

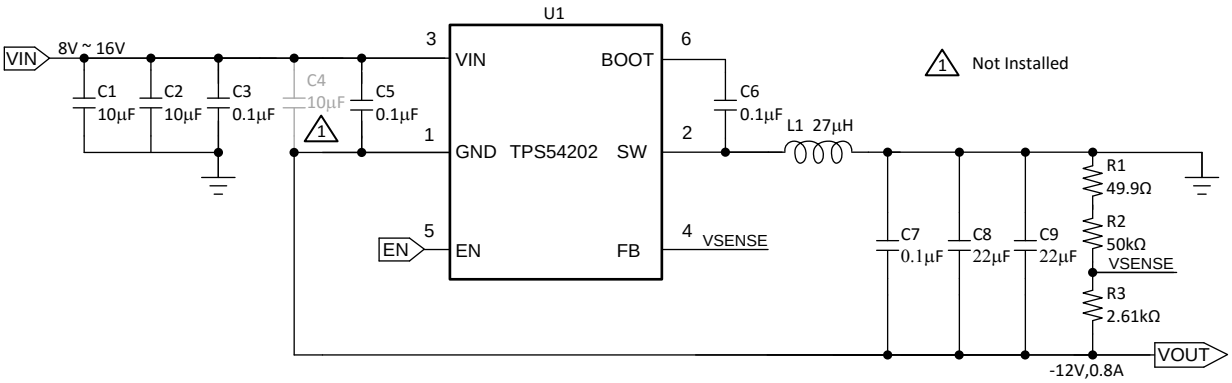

Figure 5. 12 V To –12 V Reference Design

For this design example, use the input parameters listed in Table 1.

Table 1. Design Parameters

Design Parameter	Example Value
Input voltage range	12-V nominal 8 V to 16 V
Output voltage range	–12 V
Transient response, 50% load step	ΔV_O = 2.5%
Output ripple voltage	1%
Output current rating	Maximum 0.8 A

3.1 Resistor Divider

The output voltage of the TPS54202 device is externally adjustable using a resistor divider network. In this example, this divider network is comprised of R2 and R3. Use Equation 6 to calculate the relationship of the output voltage to the resistor divider.

$$R_3 = \frac{R_2 \times V_{ref}}{V_{OUT} - V_{ref}} \quad (6)$$

As previously discussed, due to the increased noise of the inverting buck boost topology, and for a more robust design, use smaller value resistors than what are used for the buck configuration. For this design, V_{ref} = 0.6 V, set R_2 = 50 kΩ and R_3 = 2.61 kΩ. The 49.9-Ω resistor, R_1, is provided as a convenient location to break the control loop for stability testing.

3.2 Inductor and Output Capacitor Selection

The inductor and output capacitor must be selected based on the needs of the application and the stability criteria of the device. The selection criterion for the inductor and output capacitor are different from the buck converter.

3.2.1 Inductor Selection

3.2.1.1 Output Current

When selecting the inductor value for the inverting buck boost topology, you must select a large enough inductor to keep I_{Lmax} lower than the minimum current limit value (2.5 A) of the device for a reliable design. From Figure 4 and Equation 5 for this example, you can see that an at least 9.6-µH inductor is needed for a 0.8-A output application.

3.2.1.2 Inductor Current Ripple

Considering the current ripple in the inductor, when the inductor value is too small, then the current ripple will be so large that it causes more power loss in the inductor and capacitors, and also reduces the lifetime of the components. Too large of an inductor value causes a larger size and it is not good for the power density. Usually, you can choose an applicable inductor value that lets r = 0.4, to get Equation 7.

$$\Delta I_{Lmax} = \frac{V_{INmax} \times D_{min}}{L_{min} \times f_S} \leq 0.4 \times \frac{I_{OUTmax}}{1 - D_{min}} \tag{7}$$

For this example, V_{INmax} = 16 V, V_{OUT} = –12 V, I_{OUTmax} = 0.8 A, and f_s = 500 kHz, so L_{min} = 24.5 µH.

3.2.2 Output Capacitor Selection

3.2.2.1 Large Load Transient

The desired response to a large change in the load current is the first criterion. The output capacitor must supply the load with current when the converter cannot. Usually the converter requires two or more switching periods for the control loop to notice the change in load current and output voltage, and to adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change, during which the capacitor voltage droops at the same time. Use Equation 8 to calculate the minimum required output capacitance.

$$C_{OUT} \geq \frac{\Delta I_{OUT} \times 3T_S}{\Delta V_{droop}} \tag{8}$$

Where ΔI_{OUT} is the change of output current, T_s is the switching period of the converter, and ΔV_{droop} is the allowable change in the output voltage.

For this example, ΔI_{OUT} = 50% × I_{OUT} = 0.4 A, T_s = 1/f_s, and ΔV_{droop} = 2.5% × V_{OUT} = 0.3 V, so you need at least 8 µF for the large load transient condition.

3.2.2.2 Output Ripple Voltage

The output capacitor must supply the current when the high-side switch is off. Use the minimum input voltage to calculate the output capacitance needed. This is when the duty cycle and the peak-to-peak current in the output capacitor are the maximum. Using the 1% voltage ripple specification and Equation 9, C_{OUTmin} is 8 µF. Use Equation 10 to calculate the maximum ESR an output capacitor can have to meet the output-voltage ripple specification. Equation 10 indicates the ESR should be less than 53.2 mΩ. In this case, the ESR of the ceramic capacitor is much smaller than 53.2 mΩ.

$$C_{OUTmin} \geq \frac{I_{OUTmax} \times D_{max}}{f_S \times V_{ripple}} \tag{9}$$

$$R_{ESR} \leq \frac{V_{ripple}}{\frac{I_{OUTmax}}{1-D_{max}} + \frac{V_{INmin} \times D_{max}}{2 \times f_S \times L}} \tag{10}$$

An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS value of the maximum ripple current. Use Equation 11 to calculate the RMS ripple current that the output capacitor must support. For this application, Equation 11 yields 0.98 A for the output capacitor.

$$I_{Coutrms} = I_{OUTmax} \times \sqrt{\frac{D_{max}}{1-D_{max}}} \tag{11}$$

3.2.3 Selecting L and C_{OUT} for Stability

Because the TPS54202 device includes internal loop compensation, the compensation cannot be changed externally. So the stability and transient performance are only determined by the power stage, which means that selecting the applicable inductor and output capacitor is very important. Also, using a buck boost regulator to generate a negative output voltage does not close the feedback loop, because a buck power supply does. So, a different design method is needed.

From the *TPS54202 4.5-V to 28-V Input, 2-A Output, EMI Friendly Synchronous Step Down Converter Data Sheet*, you can get information about the internal loop compensation. The internal loop compensator has 1 original pole, 1 negative pole, and 1 negative zero. The transfer function of the internal loop compensator is shown in Equation 12, Equation 13, Equation 14, and Equation 15.

$$C(S) = G_O \times \frac{1 + \frac{\omega_z}{s}}{1 + \frac{s}{\omega_p}} \tag{12}$$

Where:

$$G_O = \frac{gmea \times R_C \times R_3}{R_2 + R_3} \tag{13}$$

$$\omega_Z = \frac{1}{R_C C_C} \tag{14}$$

$$\omega_p = \frac{1}{R_C C_{C2}} \tag{15}$$

With known parameters, the bode plot of the internal compensation can be obtained, as shown in Figure 6. From the bode plot of the internal compensator, you can see that there is a pole at 2.42 kHz and a zero at 2640 kHz, which gives a –9 dB gain between them.

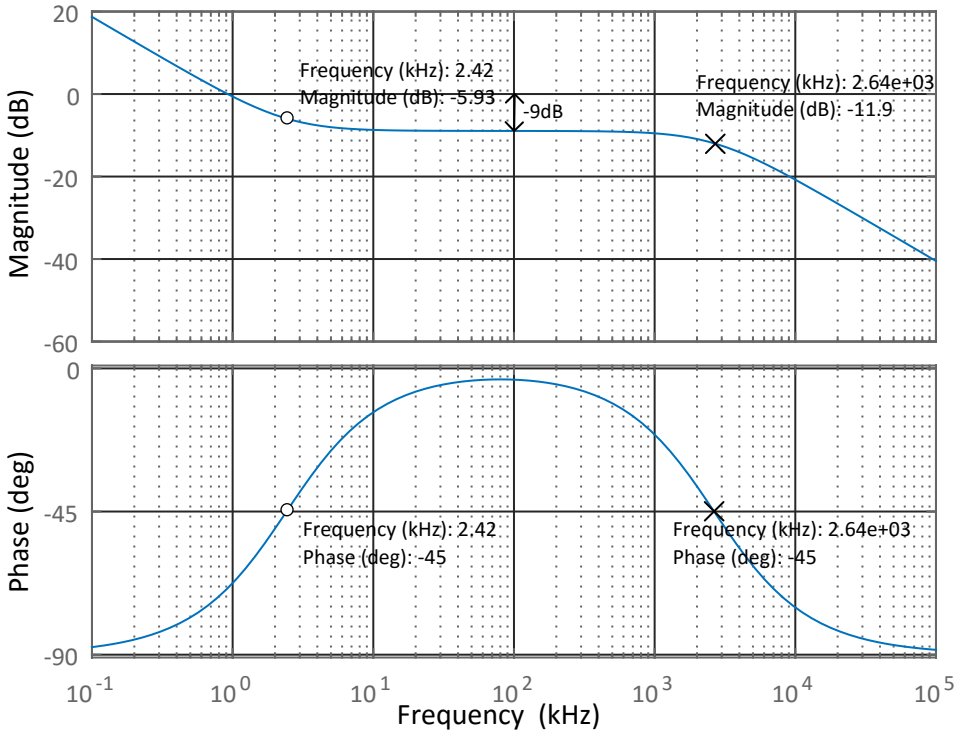

Figure 6. Bode Plot of Internal Compensator

Now let us see the inverting power supply transfer function. In the usual case, you can change the external compensator to set the cross frequency below ¼ of RHPZ, and also assume that the slope compensation pole is high frequency, so that they can neglect the influence of it. However, because of the internal compensation and relatively larger inductor, compared with the Buck application, you cannot just neglect the influence of the RHPZ and the slope compensation pole. Figure 7 shows three kinds of models of the Buck-Boost topology. The third model is the most accurate one, and it reveals that the buck-boost topology has three poles. There is one $R_{load}C_{out}$ pole, which is the dominant pole, one slope compensation pole and one high frequency pole, one RHPZ zero, and one ESR zero. The first model is the most simplified one, and it neglects the high frequency pole and the slope compensation pole, which lets the phase differ from the real one more. The second simplified model only neglects the high frequency pole and can converge with the real one at up to 200 kHz. This report applies the second model to discuss the selection of L and C. For a detailed information about the three models, see Section 6 [1] [2] [3].

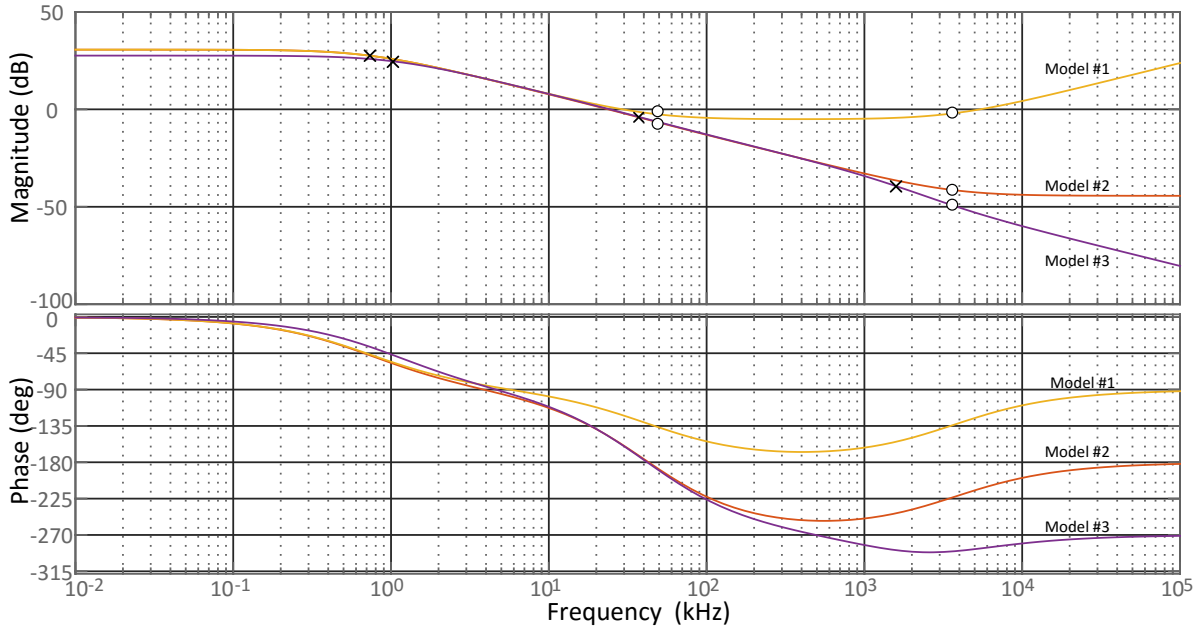

Figure 7. Models of Buck-Boost Converter

Equation 16 shows the transfer function of the second model. The ESR zero, ω_{z1}, is the same as in a buck regulator, see Equation 17, and is a function of the output capacitor and its ESR. The other zero is a right half-plane zero, ω_{zRHP}. The frequency response of ω_{zRHP} results in an increasing gain and a decreasing phase. The ω_{zRHP} frequency is a function of the duty cycle, output current, and inductor, see Equation 18. The dominant pole, ω_{P1}, is a function of the load current, output capacitor, and duty cycle, see Equation 19. The slope compensation pole, ω_{pL}, is a function of the input and output voltage, slope voltage, and inductor, see Equation 20. G_{PS0} is the DC gain which is only determined by the input and output voltage and the load current, see Equation 21. The gmps variable is the transconductance of the power stage, which is 6.8 A/V for the TPS54202 device.

$$G_{PS}(s) = G_{PS0} \times \frac{\left(1+\frac{s}{\omega_{z1}}\right)\times\left(1-\frac{s}{\omega_{zRHP}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{pL}}\right)} \quad (16)$$

Where:

$$\omega_{z1} = \frac{1}{ESR \times C_0} \quad (17)$$

$$\omega_{zRHP} = \frac{(1-D)^2 \times \frac{V_{OUT}}{I_{OUT}}}{D \times L} \quad (18)$$

$$\omega_{P1} = \frac{1+D}{\frac{V_{OUT}}{I_{OUT}} \times C_{OUT}} \quad (19)$$

$$\omega_{pL} = \frac{V_{IN} + V_{OUT}}{V_{SLOPE} \times gmps \times L} \quad (20)$$

$$G_{PS0} = \frac{V_{IN} \times \frac{V_{OUT}}{I_{OUT}}}{V_{IN} + 2 \times V_{OUT}} \times gmps \tag{21}$$

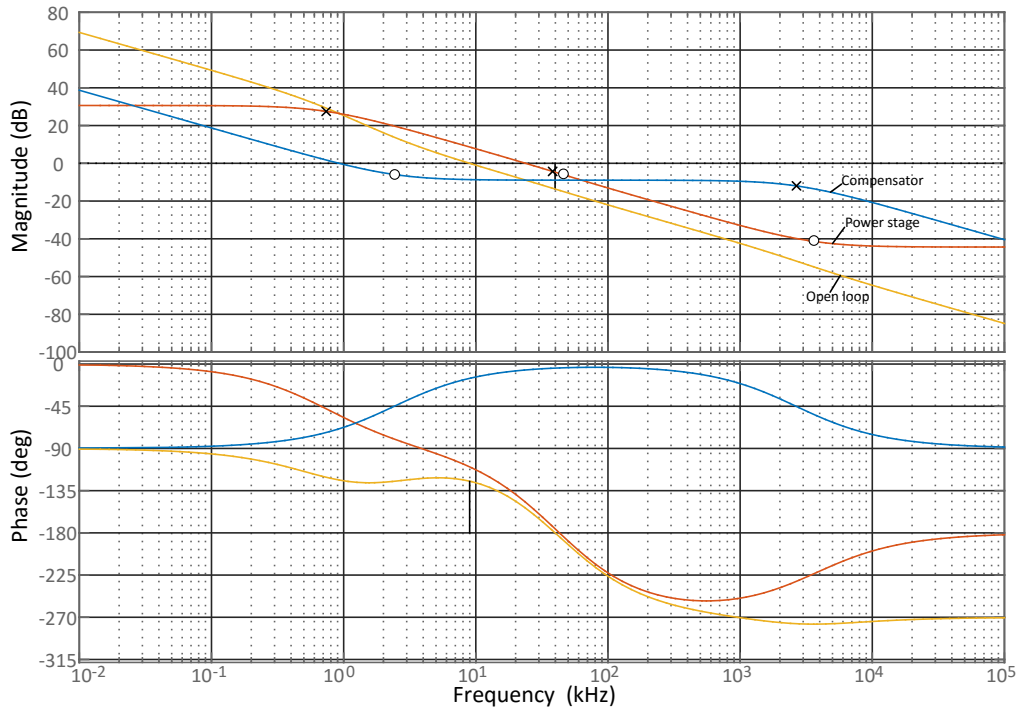

Figure 8. Bode Plot of the Buck-Boost Converter

You can see that the inductor L determines the RHPZ, ω_{zRHP}, and the slope compensation pole, ω_{pL}. The larger L is, the closer ω_{zRHP} is to ω_{pL}. The capacitor C_{OUT} with the load determines the dominant pole, ω_{P1}. Now you can get the general bode plot of the loop gain as Figure 8 shows. At low frequency, the dominant pole of the power stage determines the beginning frequency which the gain starts to slew down at, so C_{OUT} mainly determines the cross frequency. You can use Equation 22 to estimate the relationship between C_{OUT} and the cross frequency, from which you know that when C_{OUT} is doubled, the cross frequency approximately decreases by half.

$$\omega_{cross} = \frac{G_{PS0} \times \omega_{P1}}{1/G_{C0}} \tag{22}$$

By substituting parameters, you can see that by using a 22-µF C_{OUT}, the cross frequency estimated is 8.75 kHz, which is close to 8.98 kHz (the real cross frequency).

In Figure 9 and Figure 10, as for in the phase margin, when C_{OUT} is increased from a small value, ω_{P1} and ω_{z1} decrease, so that the phase starts to decrease at a lower frequency. But when C_{OUT} is too small (10 µF), then the cross frequency is so high that it is close to the slope compensation pole and RHP zero, and the phase is too small. Then, when C_{OUT} is increased, the cross frequency decreases so that the phase increases first. When you go on increasing C_{OUT}, the cross frequency decreases more so that the phase starts to decrease at a lower frequency, and the phase at the cross frequency then decreases a little. Here, considering the phase margin, TI recommends a 15 µF to 80 µF capacitor to make the cross frequency at a applicable value between the dominant pole and the slope compensation pole/RHPZ.

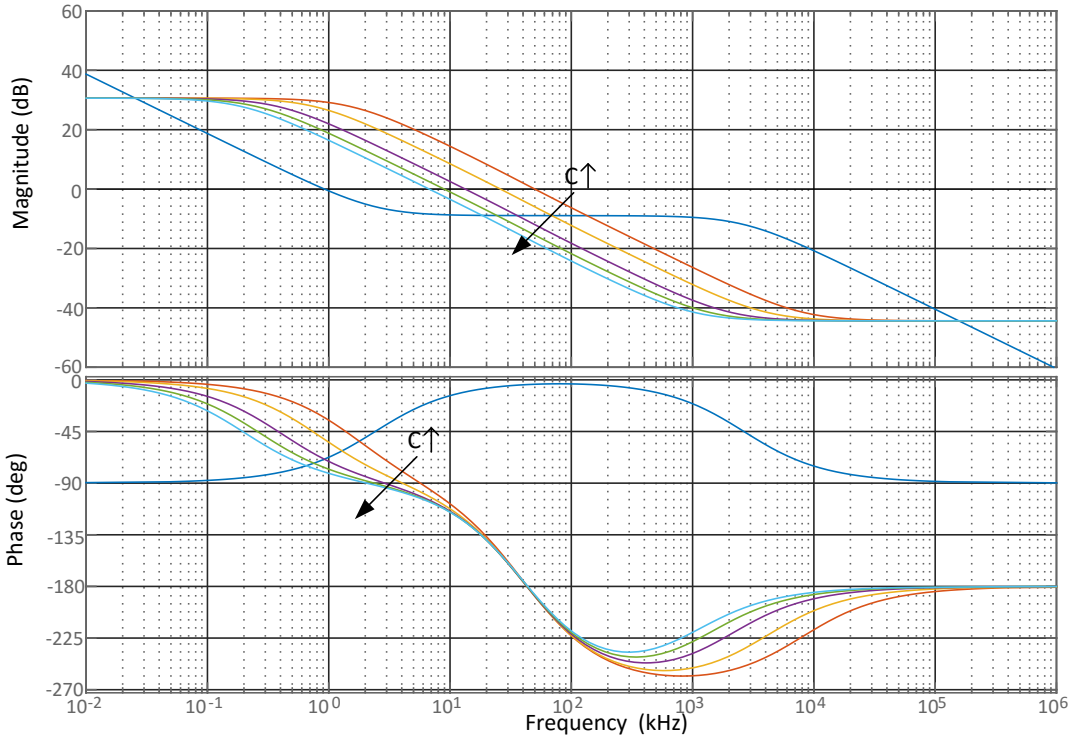

Figure 9. Bode Plot of Power Stage Versus C_{OUT}

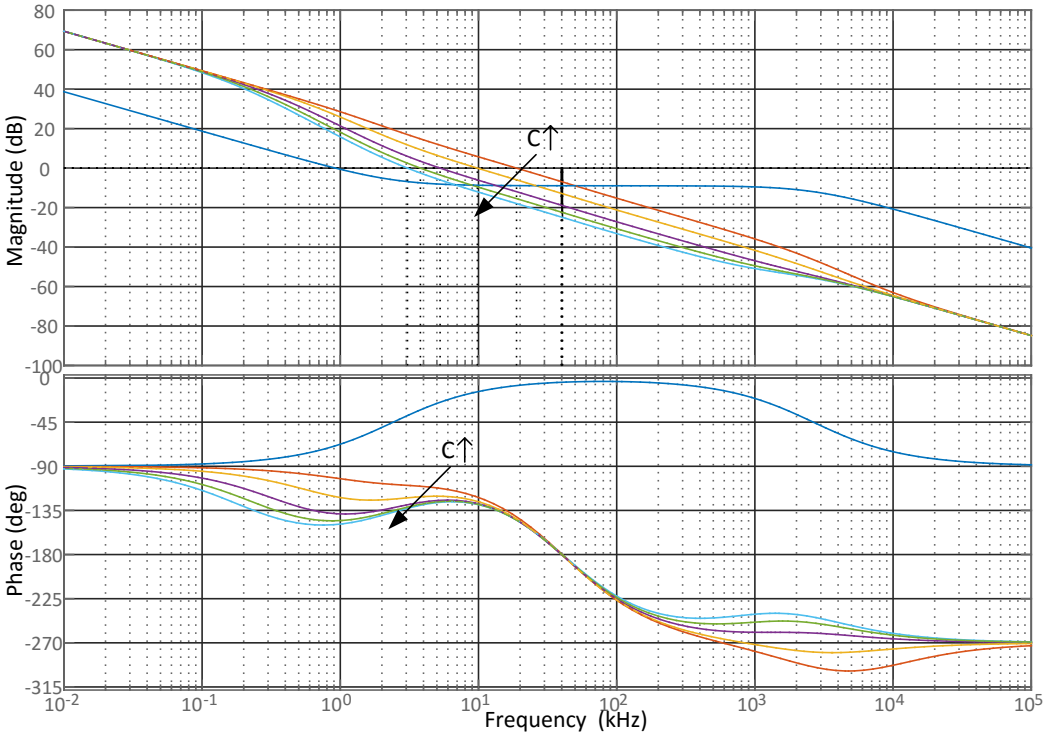

Figure 10. Bode Plot of Open Loop Versus C_{OUT}

The phase of the power stage decreases by 180 degrees in total when the frequency sweeps from the slope compensation pole to the RHPZ. In Figure 11 and Figure 12, you can see that when the inductor L is increased, the RHPZ, ω_{zRHP}, and the slope compensation pole, ω_{pL}, are decreased, which makes the phase start to decrease at a lower frequency and they are also closer at the same time. It causes the phase margin of the open loop to be lower and the gain margin is also lower too. To get enough phase margin and gain margin, a lower inductor L must be guaranteed.

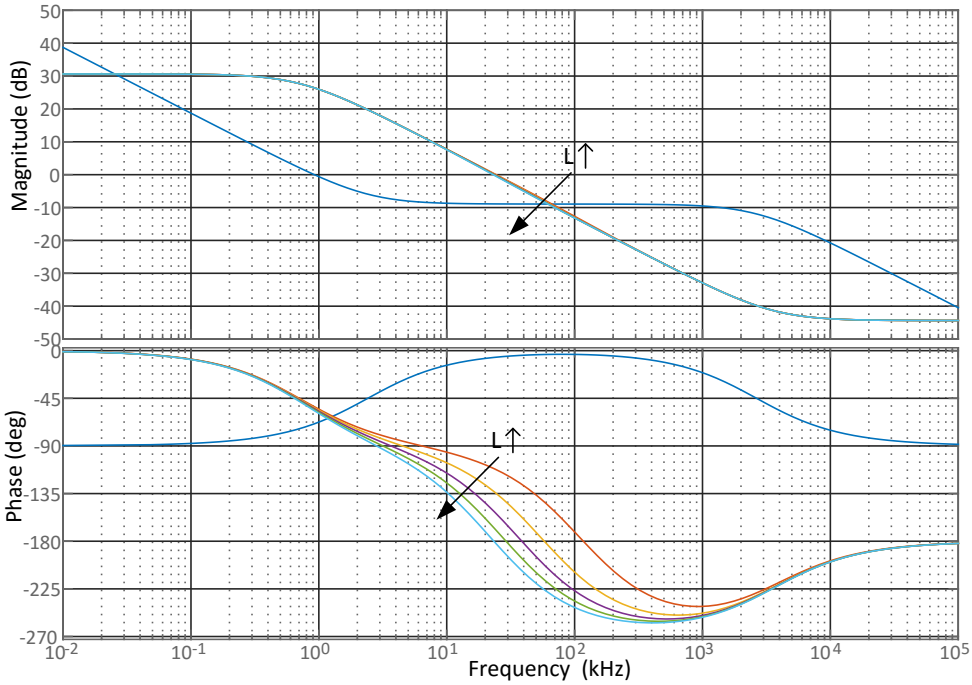

Figure 11. Bode Plot of Power Stage Versus L

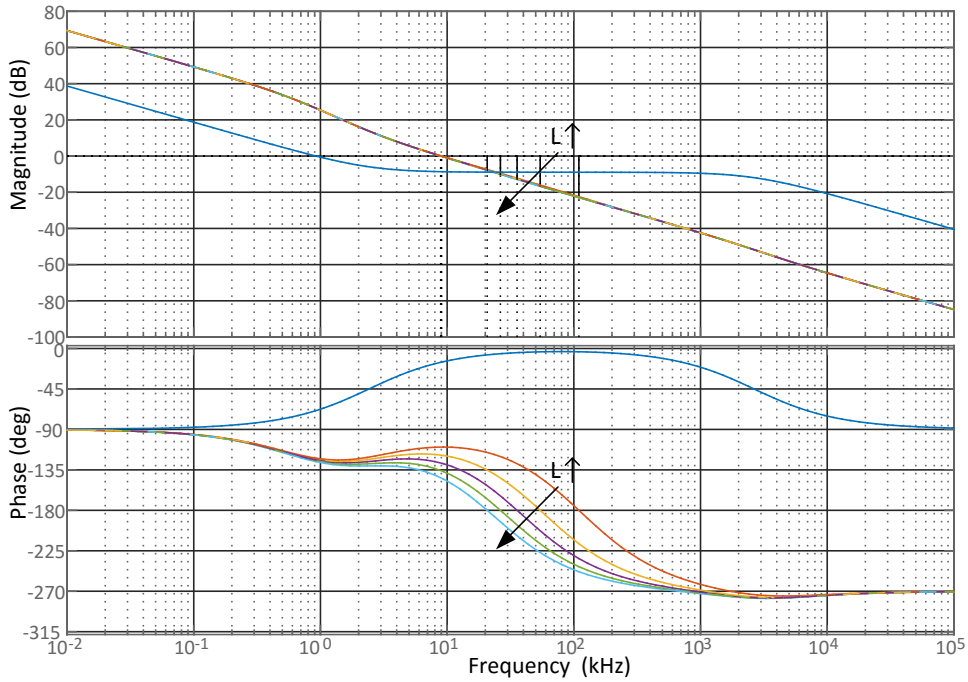

Figure 12. Bode Plot of Open Loop Versus L

So, combined with the boundaries previously derived, and considering the derating of the ceramic capacitor, you can choose two 22-µF ceramic capacitors for enough bandwidth, and a 27-µH inductor (DCR = 40 mΩ) for enough phase margin and gain margin.

From Equation 23 and Equation 24, when a 27-µH inductor is used, the peak current of the inductor is 2.1 A and the maximum rms current is 2.02 A.

$$I_{peak} = \frac{I_{OUT}}{1-D_{max}} + \frac{V_{IN(min)} \times D_{max}}{2 \times f_s \times L} \quad (23)$$

$$I_{Lrms} = \sqrt{\left(\frac{I_{OUT}}{1-D}\right)^2 + \frac{1}{12} \times \left(\frac{V_{IN} \times D}{f_s \times L}\right)^2} \quad (24)$$

At last, the criterion can be summarized when choosing L and C for Buck-Boost application of the TPS54202 device:

- Inductor L selection criterion:
  - Output current ability: must be large enough to keep the peak current lower than the minimum HSlim of the IC.
  - Inductor ripple current: must be large enough to keep the ripple lower than 0.4 times of the inductor average current.
  - Phase margin and gain margin: must be small enough to get enough phase margin and gain margin.
- Output Capacitor C_{OUT} selection criterion:
  - Large load transient: must be large enough to hold the output voltage before the control system works.
  - Output ripple voltage: must be large enough to keep the output ripple voltage lower than the specific demand.
  - Applicable cross frequency: must be selected to achieve an applicable frequency.

3.3 Input Capacitors

The input capacitors between V_{IN} and ground are used to limit the voltage ripple of the input supply. Equation 25 to Equation 28 are used to estimate the capacitance, maximum ESR, and current rating for the input capacitor, C_{IN}. Using Equation 26, the estimated average input current is 1.2 A. Using Equation 25 and Equation 27, the minimum required input capacitance is 12 µF, and the maximum ESR is 66.7 mΩ. Using Equation 28, the input capacitor needs at least a 0.98-A current rating. Two, 10-µF, 35-V X7R in parallel are used for the input capacitor, because of the low ESR and size.

$$C_{IN} = \frac{I_{OUT} \times D_{max}}{\Delta V_{IN} \times f_{sw}} \quad (25)$$

$$I_{INavg} = \frac{I_{OUT} \times D_{max}}{1-D_{max}} \quad (26)$$

$$ESR_{cin} \le \frac{\Delta V_{IN}}{I_{INavg}} \quad (27)$$

$$I_{INrms} \approx I_{OUT} \sqrt{\frac{D}{1-D}} \quad (28)$$

3.4 Bypass Capacitor

The TPS54202 device needs a tightly coupled, ceramic bypass capacitor, connected to the V_{IN} and GND pin of the device. Because the device GND is the power supply output voltage, the voltage rating of the capacitor must be greater than the differences in the maximum input and output voltage of the power supply. The voltage of the V_{IN} to GND pin is at least the V_{OUT} voltage, and the input capacitor and output capacitor in series can supply the V_{IN} and GND pin of the TPS54202 device, so there is no need to add another 10-µF capacitor from the V_{IN} pin to GND in this case. Another 0.1-µF capacitor can be added as a bypass capacitor to clear high-frequency noise.

3.5 Enabling and Adjusting UVLO

The TPS54202 device is enabled when the voltage at the EN pin trips its threshold, and the input voltage is above the UVLO threshold. It stops operation when the voltage on the EN pin falls below its threshold, or the input voltage falls below the UVLO threshold. However, when configured as a Buck-Boost application, the GND pin of the TPS54202 device is tied to the negative output voltage and not the zero voltage (system ground), which can cause difficulties enabling or disabling the device. So, level-shifting circuitry is needed to solve the problem, as shown in Figure 13.

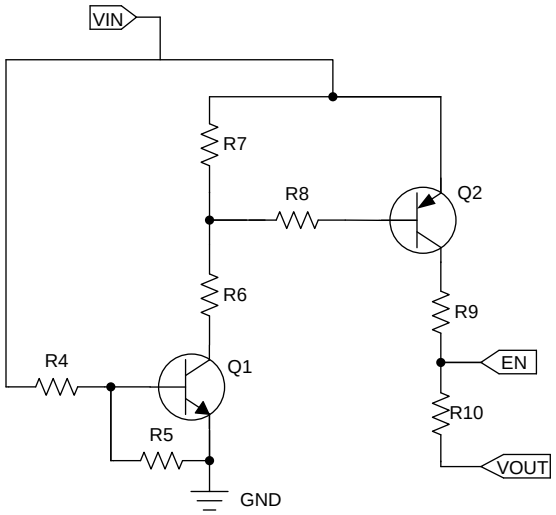

Figure 13. Enabling and Adjusting UVLO Circuit

R_9 and R_{10} are used to divide the input voltage into a small one, to ensure the EN pin can take the normal action while not exceeding the maximum pin rating of 7 V.

$$\left(\left(V_{IN}+V_{OUT}\right)\times\frac{R_{10}}{R_9+R_{10}}\right)_{min}=V_{START}\times\frac{R_{10}}{R_9+R_{10}}\geq V_{EN\_RISING(max)}=1.28V \quad (29)$$

$$\left(\left(V_{IN}+V_{OUT}\right)\times\frac{R_{10}}{R_9+R_{10}}\right)_{max}=\left(V_{INmax}+V_{OUT}\right)\times\frac{R_{10}}{R_9+R_{10}}\leq 7V \quad (30)$$

Because of the internal pull-up current source of the TPS54202 device, Equation 29 and Equation 30 are a little smaller than the real EN pin voltage. So, keeping R_9 and R_{10} small helps the accuracy of the setup for V_{START}. Here for example, you can set V_{START} = 7.5 V for the 8-V minimum input voltage to get Equation 31. So for V_{START} = 7.5 V, you can choose R_{10} = 13.2 kΩ and R_9 = 62.2 kΩ.

$$\frac{64}{375}\leq\frac{R_{10}}{R_9+R_{10}}\leq\frac{1}{4} \quad (31)$$

R_4 and R_5 form a voltage divider to set the V_{STOP} voltage. When Q1 turns on, R_6 and R_7 form a voltage divider to turn Q2 on. Then, the voltage of the EN pin equals the value Equation 30 gets. When Q1 turns off, Q2 turns off, and the voltage of the EN pin equals the V_{OUT} voltage. Then, the IC turns off at once. From the MMBT2222A data sheet, the minimum V_{BE} saturation voltage is 0.6 V. Given this value and the stop voltage, Equation 32 and Equation 33 are derived as follows:

$$V_{STOP} \times \frac{R_5}{R_4 + R_5} = 0.6V \tag{32}$$

$$V_{STOP} \times \frac{R_7}{R_6 + R_7} \geq 0.6V \tag{33}$$

Here for example, set V_{STOP} = 7 V, to get Equation 34 and Equation 35. Here, R_5 = 12 kΩ, R_4 = 128 kΩ, R_7=12kΩ, and R_6 = 72kΩ was chosen.

$$\frac{R_5}{R_4 + R_5} = \frac{3}{35} \tag{34}$$

$$\frac{R_7}{R_6 + R_7} \geq \frac{3}{35} \tag{35}$$

4 Experimental Results

The design shown in Figure 5 was used to generate –12-V output from 12-V input. Figure 14 to Figure 19 show some typical measured waveforms of this design.

Table 2 lists the experimental results regarding the comparison of different L and C_{OUT}. Figure 14 shows the bode plot when L = 27 µH and C_{OUT} = 22 µF × 2.

Table 2. Different L and C_{OUT} Comparison

L (µH)	C_{OUT} (µF)	Cross Frequency (kHz)	Phase Margin (°)	Gain Margin (dB)
27	10	22.01	16.61	2.15
	22	12.14	37.09	6.81
	22 × 2	7.03	42.21	11.78
	22 × 4	4.36	38.57	17.48
15	22 × 2	7.31	52.1	16.12
27		7.03	42.21	11.78
33		7.7	38.1	9.89
47		7.83	22.51	5.6

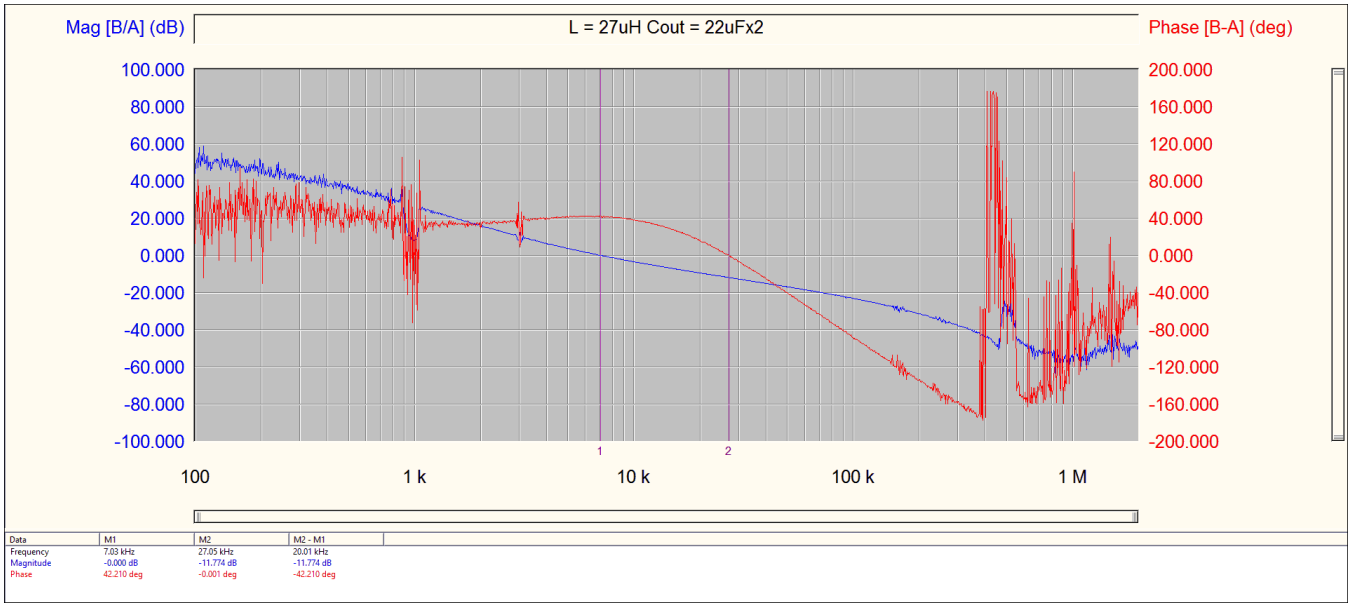

Figure 14. Bode Plot Measurement Result

Figure 15 and Figure 16 show comparisons of the load transient waveforms from 0.4 A to 0.8 A. Table 2 shows that there are some deviations from the theoretical calculation, due to the DC bias rating and ESR-frequency curve of the ceramic capacitors. From Table 2, you can see that when C_{OUT} is increased, the cross frequency decreases and the phase margin first increases and then decreases. Also, the gain margin increases too. When you increase L, the cross frequency almost does not change, and the phase margin and gain margin decrease significantly.Figure 15 shows that too small a C_{OUT} creates a high cross frequency, but also a lack of phase margin. Figure 16 shows that too large an L creates a poor phase margin.

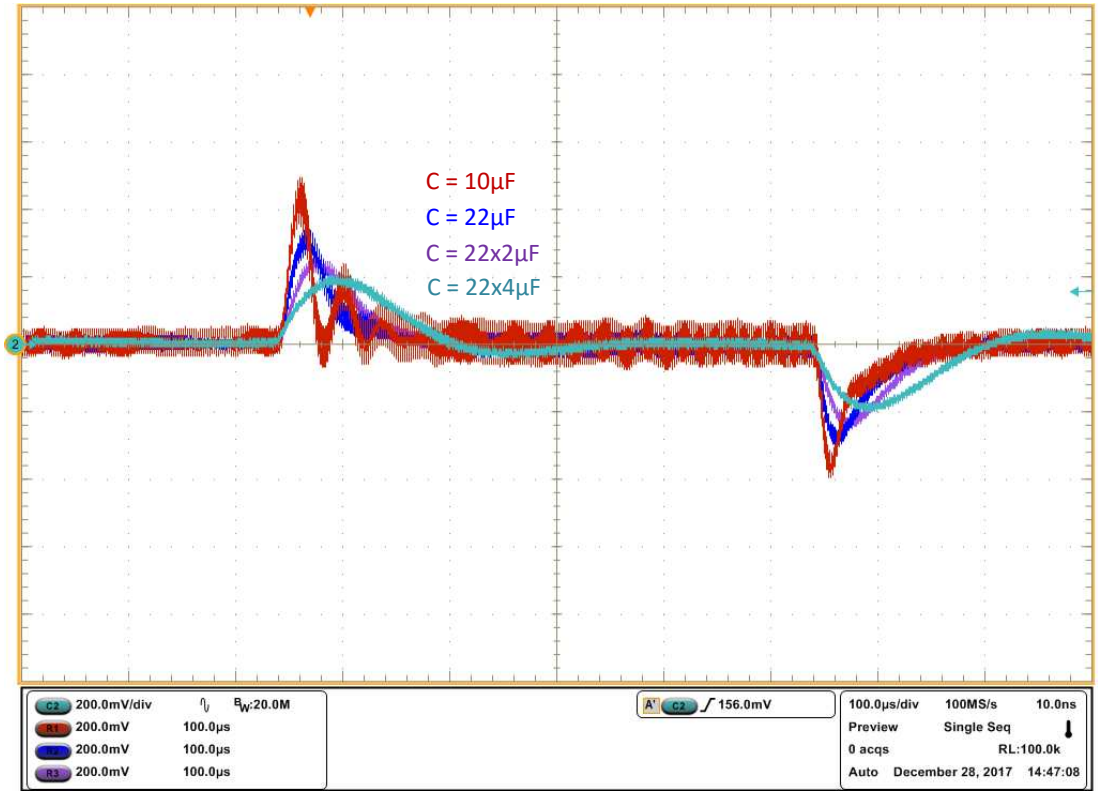

Figure 15. Load Transient, L = 27 µH

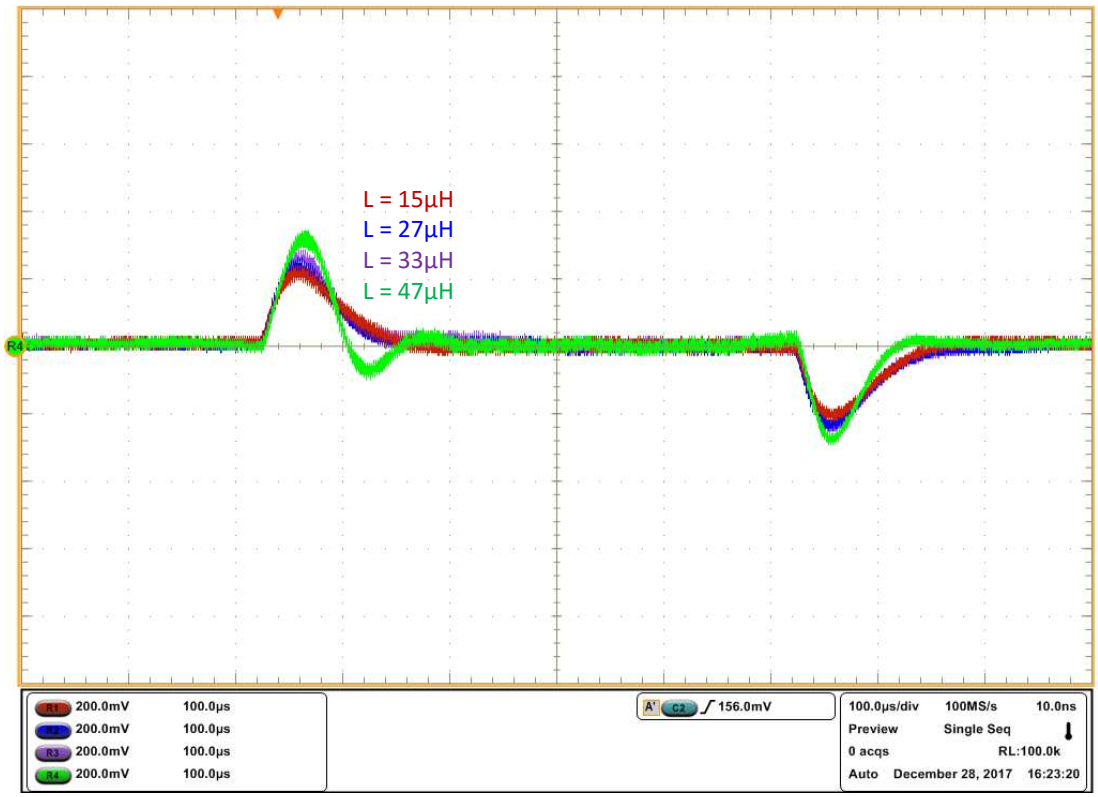

Figure 16. Load Transient, C = 22 µF × 2

Figure 17 to Figure 19 show the steady state of the Buck-Boost converter, which shows that the output ripples are small when the load is 0 A, 0.4 A, and 0.8 A. Also, while the load is light, the converter works at Eco-Mode which increases the efficiency significantly.

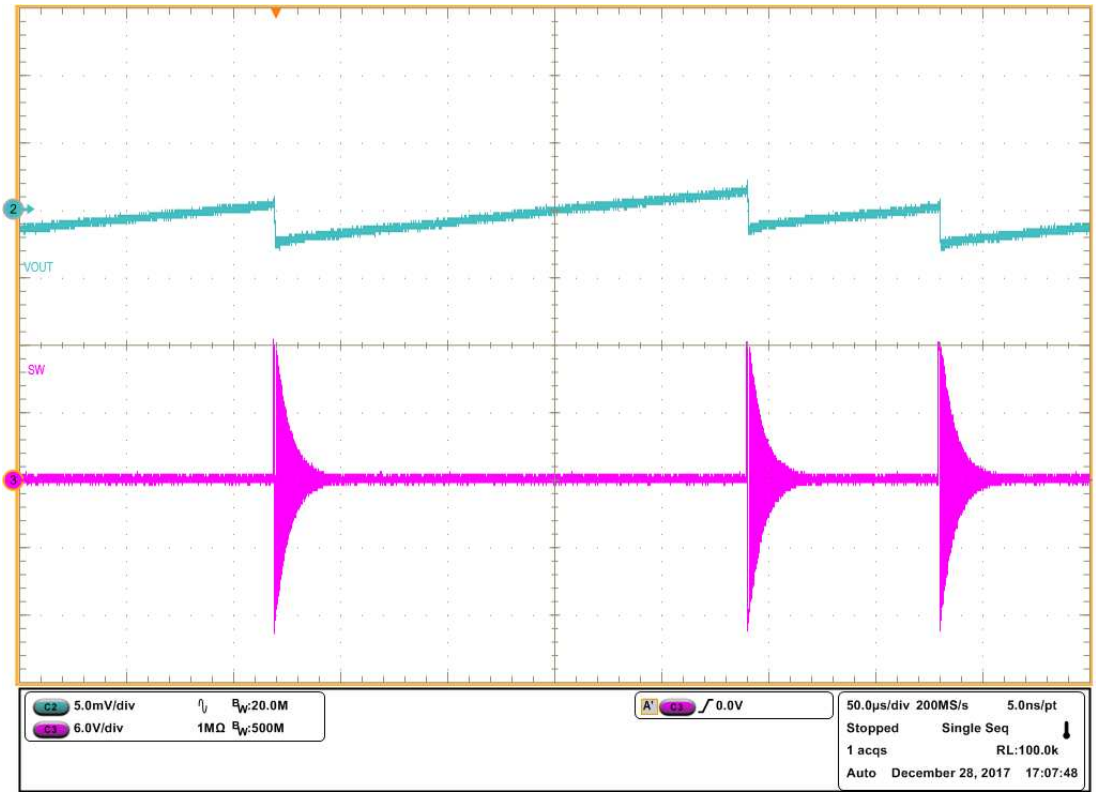

Figure 17. Output Voltage Ripple, I_{load} = 0 A

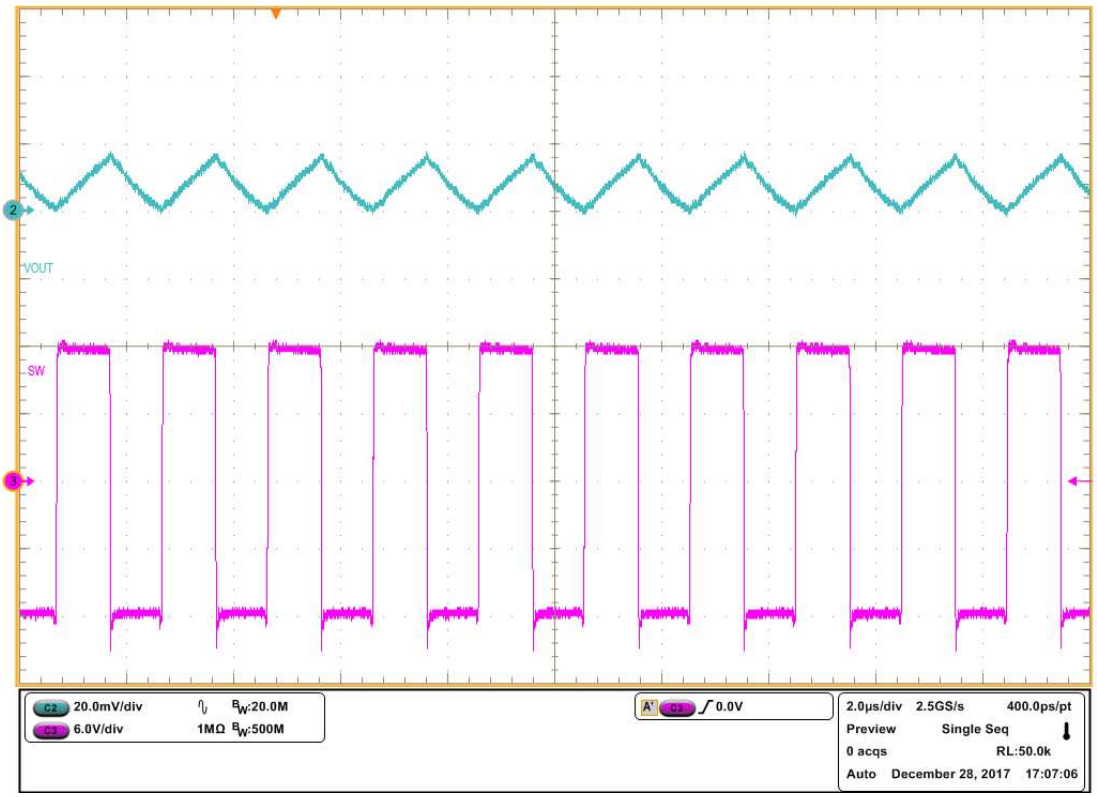

Figure 18. Output Voltage Ripple, I_{load} = 0.4 A

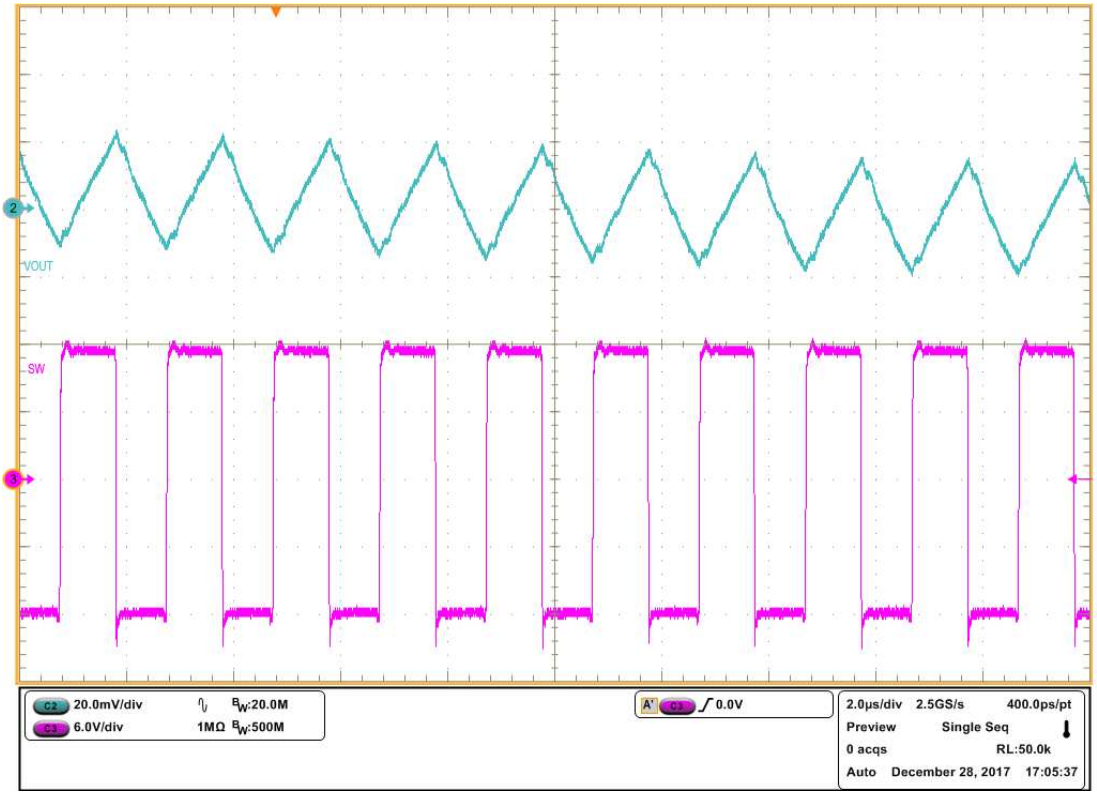

Figure 19. Output Voltage Ripple, I_{load} = 0.8 A

5 Summary

The TPS54202 buck converter can be configured as an inverting buck boost converter to generate a negative output voltage. This application report explains, due to the internal compensation, how to select an applicable LC value and other external components. Measured data from the example design is provided. This application report also applies to the TPS54302 and TPS54202H devices.

6 References

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3. Texas Instruments, *Using the TPS54335A to Create an Inverting Power Supply, Milo Zhu*
4. Texas Instruments, *TPS54202 4.5-V to 28-V Input, 2-A Output, EMI Friendly Synchronous Step Down Converter Data Sheet*

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