Application Brief

How to Approach a Power-Supply Design – Part 4

Markus Zehendner

This application brief introduces the single-ended primary inductance converter (SEPIC) and Zeta converter. Both topologies can be a cost-effective alternative to a buck-boost converter in the power range up to 25 W.

SEPICs

The SEPIC topology can step up and step down the input voltage. The energy transfers from the input to the output when switch Q1 is not conducting. Figure 1 shows the schematic of a nonsynchronous SEPIC.

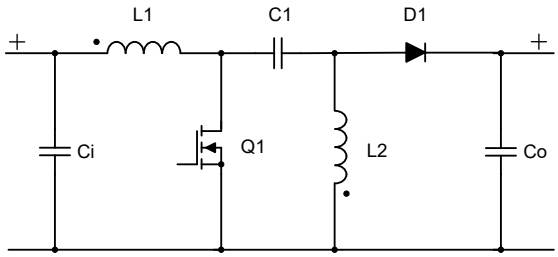

Figure 1. Nonsynchronous SEPIC Schematic

Equation 1 calculates the duty cycle in continuous conduction mode (CCM) as:

$$D = \frac{V_{OUT} + V_f}{V_{OUT} + V_f + V_{IN}} \quad (1)$$

Equation 2 calculates the maximum metal-oxide semiconductor field-effect transistor (MOSFET) stress as:

$$V_{Q1} = V_{IN} + V_{OUT} + V_f + \frac{V_{C1,ripple}}{2} \quad (2)$$

Equation 3 gives the maximum diode stress as:

$$V_{D1} = V_{IN} + V_{OUT} + \frac{V_{C1,ripple}}{2} \quad (3)$$

where

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- V_f is the diode forward voltage
- $V_{C1,ripple}$ is the voltage ripple across the coupling capacitor

The inductor-capacitor (LC) filter L1 and Ci is pointing to the input of the SEPIC. This leads to a smaller ripple at the input due to the continuous current flow. At the output, the ripple is bigger because there is a pulsed output current.

A nonsynchronous SEPIC costs less than a buck-boost topology because only one gate driver (compared to two for a two-switch buck-boost converter) and only two semiconductor components (instead of four) is needed. Another advantage of a SEPIC over a buck-boost topology is the better electromagnetic interference (EMI)

behavior when both converters are operating in buck mode as a result of the continuous input current of the SEPIC.

A SEPIC is easily built by using a boost controller because MOSFET Q1 needs to be driven on the low side.

The right half-plane zero (RHPZ) is the limiting factor for the achievable regulation bandwidth of a SEPIC. The maximum bandwidth is roughly one-fifth the RHPZ frequency. Equation 4 calculates an estimation of the single RHPZ frequency of the transfer function of the SEPIC:

$$f_{RHPZ} = \frac{V_{OUT} \times (1 - D)^2}{2 \times \pi \times D^2 \times L_2 \times I_{OUT}} \quad (4)$$

Solving Equation 5 for *s* has either one or two more RHPZs as a result:

$$1 - s \times \frac{C_1 \times (L_1 + L_2) \times \frac{V_{OUT}}{I_{OUT}}}{L_1} \times \frac{(1 - D)^2}{D^2} + s^2 \times \frac{L_2 \times C_1}{D} = 0 \quad (5)$$

where

- V_{OUT} is the output voltage
- D is the duty cycle
- I_{OUT} is the output current
- L_1 is the inductance of inductor L1
- L_2 is the inductance of inductor L2
- C_1 is the capacitance of coupling capacitor C1 and s is the complex frequency variable

Figure 2 through Figure 11 show voltage and current waveforms in CCM for FET Q1, inductor L1, coupling capacitor C1, diode D1, and inductor L2 in a nonsynchronous SEPIC.

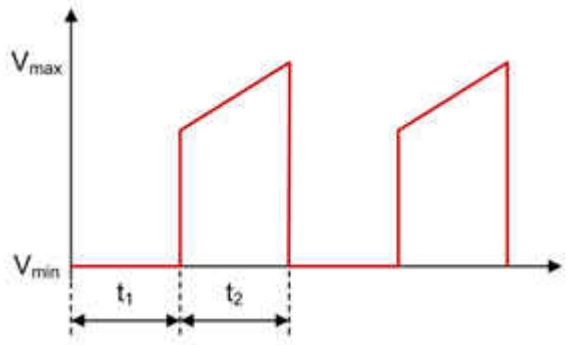

Figure 2. SEPIC FET Q1 Voltage Waveform in CCM

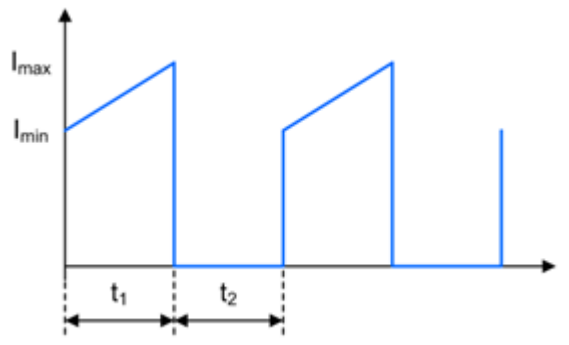

Figure 3. SEPIC FET Q1 Current Waveform in CCM

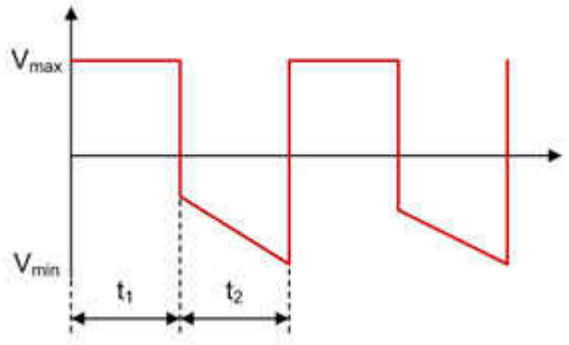

Figure 4. SEPIC Inductor L1 Voltage Waveform in CCM

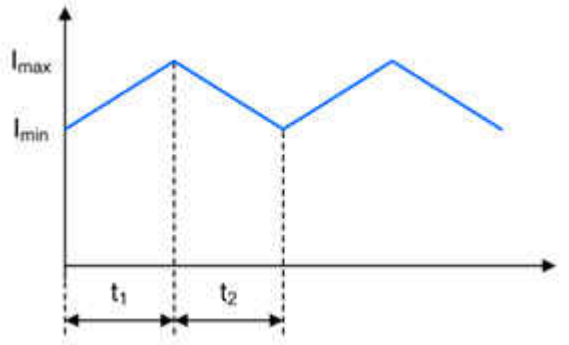

Figure 5. SEPIC Inductor L1 Current Waveform in CCM

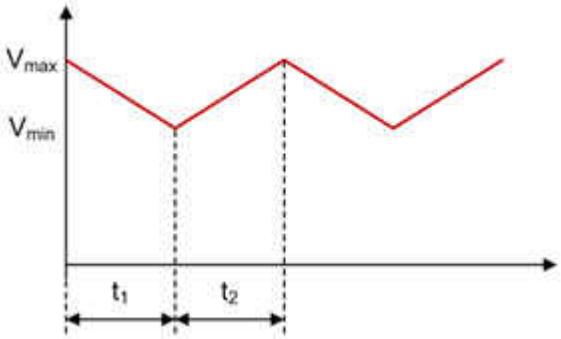

Figure 6. SEPIC Coupling Capacitor C1 Voltage Waveform in CCM

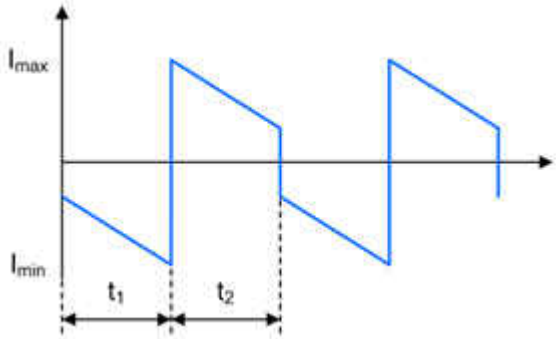

Figure 7. SEPIC Coupling Capacitor C1 Current Waveform in CCM

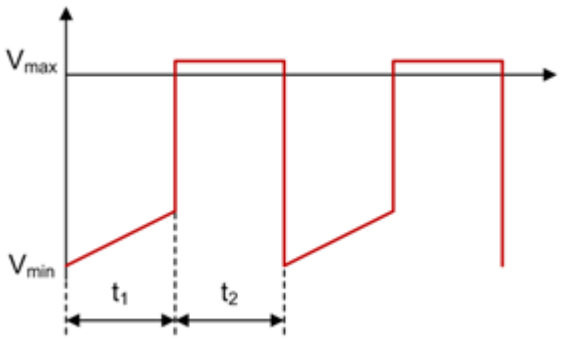

Figure 8. SEPIC Diode D1 Voltage Waveform in CCM

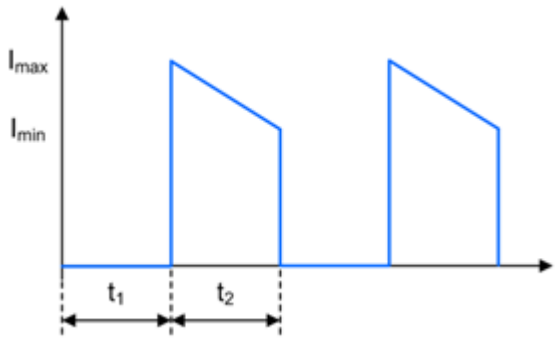

Figure 9. SEPIC Diode D1 Current Waveform in CCM

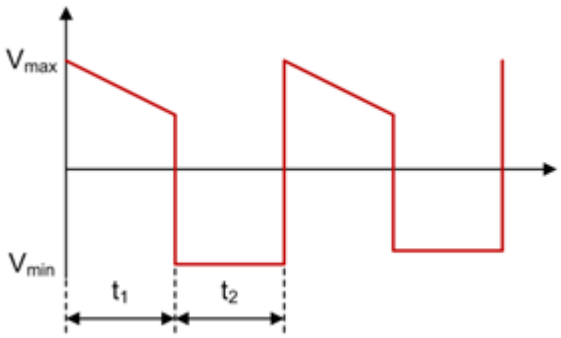

Figure 10. SEPIC Inductor L2 Voltage Waveform in CCM

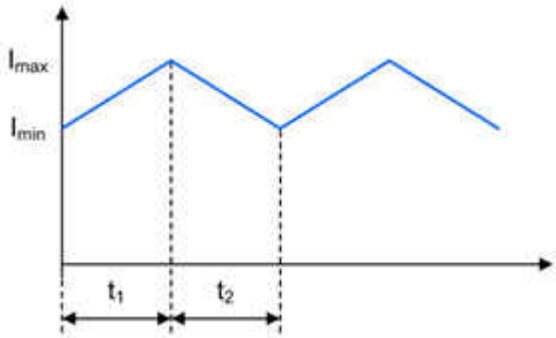

Figure 11. SEPIC Inductor L2 Current Waveform in CCM

Zeta Converters

The Zeta topology can step up and step down the input voltage. The energy transfers from the input to the output when switch Q1 is conducting. Figure 12 shows the schematic of a nonsynchronous Zeta converter.

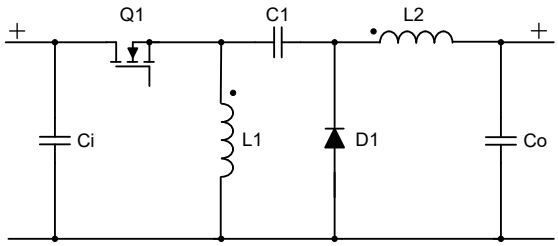

Figure 12. Nonsynchronous Zeta Converter Schematic

Equation 6 calculates the duty cycle in CCM as:

$$D = \frac{V_{OUT} + V_f}{V_{OUT} + V_f + V_{IN}} \quad (6)$$

Equation 7 calculates the maximum MOSFET stress as:

$$V_{Q1} = V_{IN} + V_{OUT} + V_f + \frac{V_{C1,ripple}}{2} \quad (7)$$

Equation 8 gives the maximum diode stress as:

$$V_{D1} = V_{IN} + V_{OUT} + \frac{V_{C1,ripple}}{2} \quad (8)$$

where

- V_{IN} is the input voltage
- V_{OUT} is the output voltage
- V_f is the diode forward voltage
- $V_{C1,ripple}$ is the voltage ripple across the coupling capacitor

The LC filter L2 and Co in a Zeta converter is pointing to the output. As a result, the output ripple is smaller compared to the input ripple, because the output current is continuous and the input current is pulsed. Using the Zeta topology for very sensitive loads is recommended, where a SEPIC or buck-boost converter does not fit due to their higher output ripple. The Zeta topology has the same advantage regarding cost and component count over the buck-boost converter as the SEPIC.

A Zeta converter can be built by using a buck controller or converter; a P-channel MOSFET or high-side MOSFET driver is needed.

The Zeta converter does not have a RHPZ, because the controller can immediately react to changes at the output. Therefore, higher bandwidths with a Zeta converter can be achieved than with a SEPIC or buck-boost converter while using less output capacitance.

Figure 13 through Figure 22 show voltage and current waveforms in CCM for FET Q1, inductor L1, coupling capacitor C1, diode D1, and inductor L2 in a nonsynchronous Zeta converter.

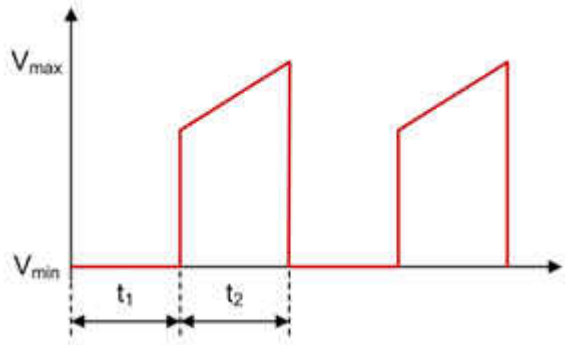

Figure 13. Zeta FET Q1 Voltage Waveform in CCM

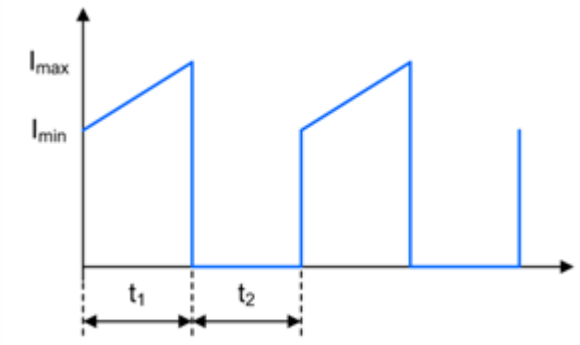

Figure 14. Zeta FET Q1 Current Waveform in CCM

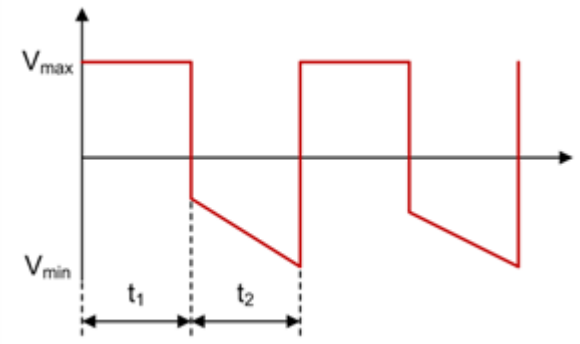

Figure 15. Zeta Inductor L1 Voltage Waveform in CCM

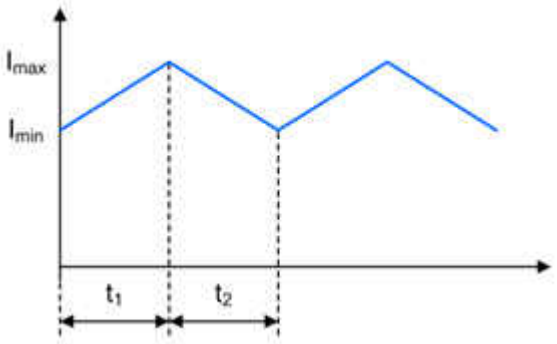

Figure 16. Zeta Inductor L1 Current Waveform in CCM

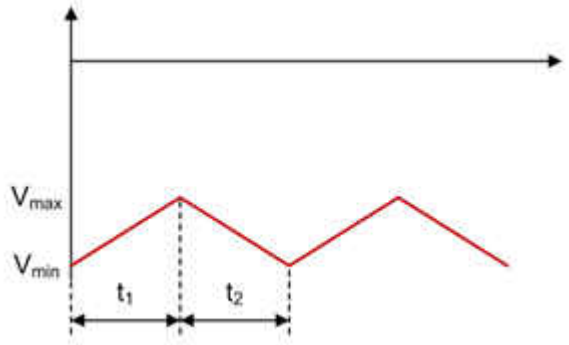

Figure 17. Zeta Coupling Capacitor C1 Voltage Waveform in CCM

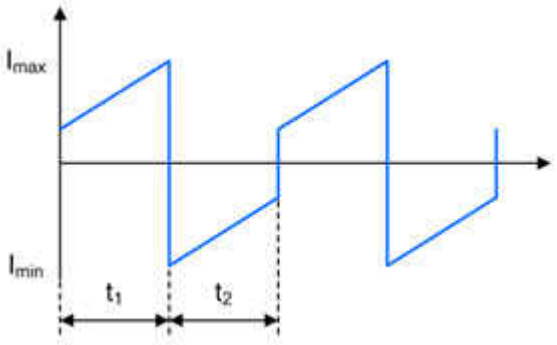

Figure 18. Zeta Coupling Capacitor C1 Current Waveform in CCM

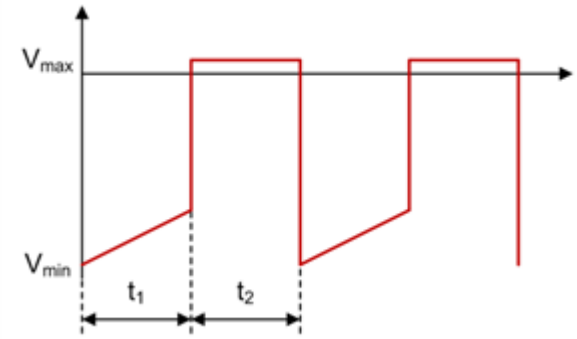

Figure 19. Zeta Diode D1 Voltage Waveform in CCM

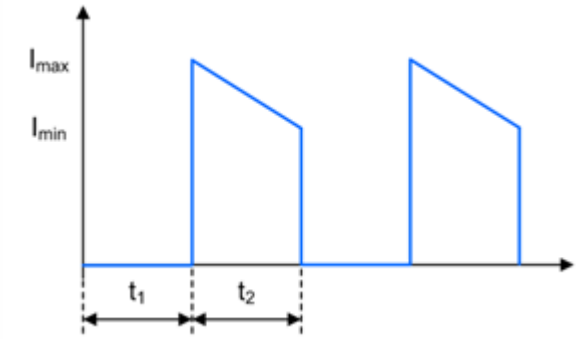

Figure 20. Zeta Diode D1 Current Waveform in CCM

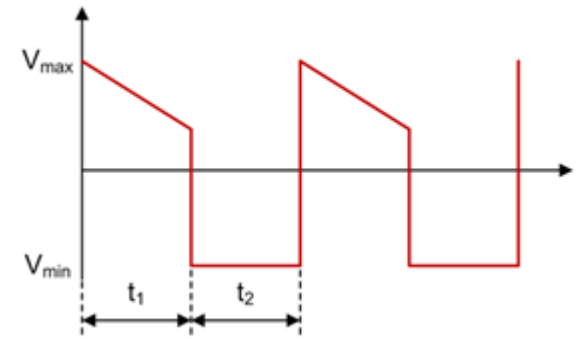

Figure 21. Zeta Inductor L2 Voltage Waveform in CCM

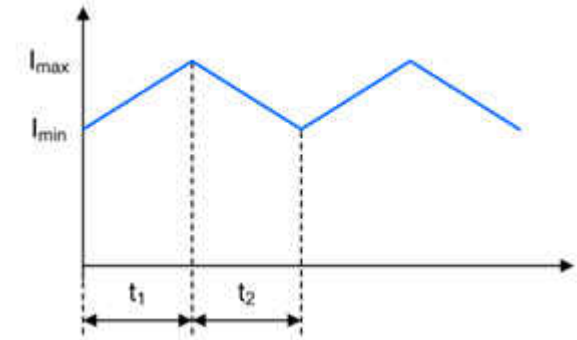

Figure 22. Zeta Inductor L2 Current Waveform in CCM

For both topologies, using coupled inductors instead of two separate inductors has two advantages. The first advantage is that only half the inductance is required for a similar current ripple (compared to a two-inductor design) because of ripple cancellation by coupling the windings. The second advantage is that the resonance in the transfer function caused by the two inductors and the coupling capacitor can be removed. Dampen this resonance with a resistor-capacitor (RC) network in parallel with coupling capacitor C1, if needed.

One drawback to using coupled inductors is that the same inductance value for both inductors must be used. Another limitation is typically their current rating. Single inductors can sometimes be needed for applications with high output currents.

It is possible to configure both topologies as a converter with synchronous rectification. But if this method is used, you must AC-couple the high-side gate-drive signal, because many controllers require that you connect them to the switch node. Both topologies have two switch nodes each, so take care to avoid negative voltage-rating violations on the switch pin. Two examples with a synchronous SEPIC and a synchronous Zeta converter are the *12V@5A Synchronous SEPIC Converter Reference Design* and the *40W Synchronous Zeta Converter with Two Inductors Reference Design*, respectively.

Additional Resources

- Watch these TI training videos:
  - Topology Tutorial: What is a SEPIC?
  - Topology Tutorial: What is a Zeta Converter?
- Read these Analog Applications Journal articles:
  - Benefits of a coupled-inductor SEPIC converter
  - Designing DC/DC converters based on Zeta topology
- Design your power stage with Power Stage Designer.
- Download the Power Topologies Handbook and Power Topologies Quick Reference Guide.

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