LP2951-Q1 Automotive, Adjustable Micropower Voltage Regulators With Shutdown

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: −40°C to +125°C, T_A
- Wide input range: Up to 35V
- Rated output current: 100mA
- Low dropout: 380mV (typ) at 100mA
- Low quiescent current: 75µA (typ)
- Tight line regulation: 0.03% (typ)
- Tight load regulation: 0.04% (typ)
- High V_O accuracy:
  - 1% at 25°C
  - 2% over temperature
- Can be used as a regulator or reference
- Stable with low ESR (>12mΩ) capacitors
- Current- and thermal-limiting features
- 8-pin package:
  - Fixed voltages: 5V/ADJ and 3.3V/ADJ
  - Low-voltage error signal on falling output
  - Shutdown capability
  - Remote sense capability for optimal output regulation and accuracy

2 Applications

- Infotainment and clusters
- HEV/EV battery-management systems (BMS)
- HEV/EV inverters and motor controls
- HEV/EV onboard chargers (OBC) and wireless chargers
- HEV/EV DC/DC converters

3 Description

The LP2951-Q1 is a bipolar, low-dropout voltage regulator that can accommodate a wide input supply-voltage range of up to 35V. The 8-pin LP2951-Q1 is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, and the FEEDBACK and V_{TAP} pins together, the LP2951-Q1 outputs a fixed 5V and 3.3V (depending on the version). Alternatively, by leaving the SENSE and V_{TAP} pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 1.235V to 30V.

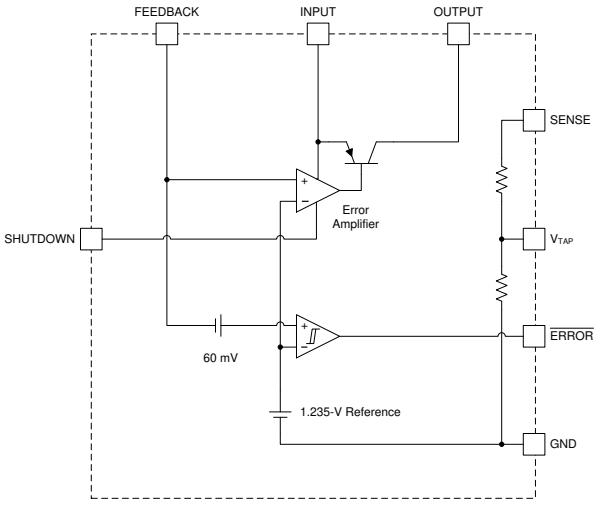
The LP2951-Q1 device is designed to minimize all error contributions to the output voltage. With a tight output tolerance (0.5% at 25°C), a very low output voltage temperature coefficient (20ppm typical), extremely good line and load regulation (0.3% and 0.4% typical), and remote sensing capability, the device can be used as either a low-power voltage reference or a 100mA regulator.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
LP2951-33-Q1	DRG (WSON, 8)	3mm × 3mm
LP2951-50-Q1		
LP2951-50-Q1	D (SOIC, 8)	4.9mm × 6mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Block Diagram

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4 Pin Configuration and Functions

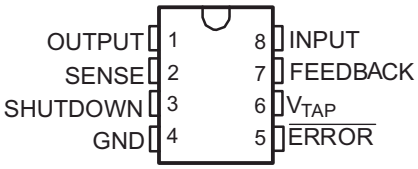


Figure 4-1. D Package (LP2951-50-Q1), 8-Pin SOIC (Top View)

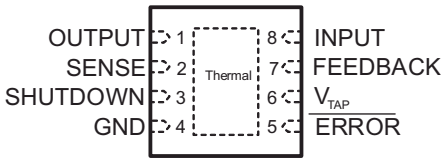


Figure 4-2. DRG Package, 8-Pin WSON With Exposed Thermal Pad (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{ERROR}$	5	O	Active-low, open-collector error output. Goes low when V_{OUT} drops by 6% of the nominal value.
FEEDBACK	7	I	Determines the output voltage. Connect to V_{TAP} (with OUTPUT tied to SENSE) to output the fixed voltage corresponding to the device version, or connect to a resistor divider to adjust the output voltage.
GND	4	—	Ground
INPUT	8	I	Supply input
OUTPUT	1	O	Voltage output
SENSE	2	I	Senses the output voltage. Connect to OUTPUT (with FEEDBACK tied to V_{TAP}) to output the voltage corresponding to the device version.
SHUTDOWN	3	I	Active-high input. Shuts down the device.
V_{TAP}	6	O	Tie to FEEDBACK to output the fixed voltage corresponding to the device version.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	35	V
V_{SHDN}	SHUTDOWN input voltage	–1.5	35	V
	$\overline{\text{ERROR}}$ comparator output voltage(2)	–1.5	30	V
V_{FDBK}	FEEDBACK input voltage(2) (3)	–1.5	30	V
T_J	Operating virtual-junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Can possibly exceed input supply voltage.
(3) If load is returned to a negative power supply, the output must be diode clamped to GND.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) (2)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 4, 8, and 5)	±1000	
			Other pins	±1000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) The LP2951-50QDRQ1 FEEDBACK pin survives up to 1500-V HBM.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Supply input voltage	See (1)		30	V
T_A	Operating temperature	–40		125	°C

(1) Minimum V_{IN} is the greater of:
a. 2 V (25°C), 2.3 V (over temperature), or
b. $V_{OUT(MAX)}$ + Dropout (max) at rated I_L.

5.4 Thermal Information

THERMAL METRIC(1)		LP2951-30-Q1, LP2951-50-Q1	LP2951-50-Q1	UNIT
		DRG (WSON)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	55.7	121.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66.5	69.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.2	61.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.1	22.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	30.4	61.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	10	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application note.

5.5 Electrical Characteristics

V_{IN} = V_{OUT} (nominal) + 1 V, I_L = 100 µA, C_L = 1 µF (5-V versions) or C_L = 2.2 µF (3.3-V versions), 8-pin version: FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, $V_{SHUTDOWN}$ ≤ 0.7 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
3.3-V VERSION (LP2951-33-Q1)							
V_{OUT}	Output voltage	I_L = 100 µA	25°C	3.267	3.3	3.333	V
			–40°C to 125°C	3.234	3.3	3.366	
5-V VERSION (LP2951-50-Q1)							
V_{OUT}	Output voltage	I_L = 100 µA	25°C	4.950	5	5.050	V
			–40°C to 125°C	4.900	5	5.100	
ALL VOLTAGE OPTIONS							
	Output voltage temperature coefficient(1)	I_L = 100 µA	–40°C to 125°C		20	100	ppm/°C
	Line regulation(2)	V_{IN} = [$V_{OUT(NOM)}$ + 1 V] to 30 V	25°C		0.03	0.2	%/V
			–40°C to 125°C			0.4	
	Load regulation(2)	I_L = 100 µA to 100 mA	25°C		0.04%	0.2%	
			–40°C to 125°C			0.3%	
V_{IN} – V_{OUT}	Dropout voltage(3)	I_L = 100 µA	25°C		50	80	mV
			–40°C to 125°C			150	
		I_L = 100 mA	25°C		380	450	
			–40°C to 125°C			600	
I_{GND}	GND current	I_L = 100 µA	25°C		75	120	µA
			–40°C to 125°C			140	
		I_L = 100 mA	25°C		8	12	mA
			–40°C to 125°C			14	
	Dropout ground current	V_{IN} = $V_{OUT(NOM)}$ – 0.5 V, I_L = 100 µA	25°C		110	170	µA
			–40°C to 125°C			200	
	Current limit	V_{OUT} = 0 V	25°C		160	200	mA
			–40°C to 125°C			220	
	Thermal regulation(4)	I_L = 100 µA	25°C		0.05	0.2	%/W
	Output noise (RMS), 10 Hz to 100 kHz	C_L = 1 µF (5 V only)	25°C		430		µV
		C_L = 200 µF			160		
		LP2951-50-Q1: C_L = 3.3 µF, C_{Bypass} = 0.01 µF between pins 1 and 7			100		
	Reference voltage(6)	V_{OUT} = V_{REF} to (V_{IN} – 1 V), V_{IN} = 2.3 V to 30 V, I_L = 100 µA to 100 mA	–40°C to 125°C	1.200		1.272	V
	Reference voltage temperature coefficient(1)		25°C		20		ppm/°C
$\overline{\text{ERROR}}$ COMPARATOR							
	Output leakage current	V_{OUT} = 30 V	25°C		0.01	1	µA
			–40°C to 125°C			2	
	Output low voltage	V_{IN} = $V_{OUT(NOM)}$ – 0.5 V, I_{OL} = 400 µA	25°C		150	250	mV
			–40°C to 125°C			400	
	Upper threshold voltage ($\overline{\text{ERROR}}$ output high)(5)		25°C	40	60		mV
			–40°C to 125°C	25			
	Lower threshold voltage ($\overline{\text{ERROR}}$ output low)(5)		25°C		75	95	mV
			–40°C to 125°C			140	
	Hysteresis(5)		25°C		15		mV
SHUTDOWN INPUT							
	Input logic voltage	Low (regulator ON)	–40°C to 125°C			0.7	V
		High (regulator OFF)		2			

5.5 Electrical Characteristics (continued)

V_{IN} = V_{OUT} (nominal) + 1 V, I_L = 100 µA, C_L = 1 µF (5-V versions) or C_L = 2.2 µF (3.3-V versions), 8-pin version: FEEDBACK tied to V_{TAP}, OUTPUT tied to SENSE, $V_{SHUTDOWN}$ ≤ 0.7 V

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
	SHUTDOWN input current	V_{TAP} = 2.4 V	25°C		30	50	µA
			–40°C to 125°C			100	
		V_{TAP} = 30 V	25°C		450	600	
			–40°C to 125°C			750	
	Regulator output current in shutdown	$V_{SHUTDOWN}$ ≥ 2 V, V_{IN} ≤ 30 V, V_{OUT} = 0, FEEDBACK tied to V_{TAP}	25°C		3	10	µA
			–40°C to 125°C			20	

(1) Output or reference voltage temperature coefficient is defined as the worst-case voltage change divided by the total temperature range.
(2) Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output voltage resulting from heating effects are covered under the specification for thermal regulation.
(3) Dropout voltage is defined as the input-to-output differential at which the output voltage drops 100 mV, below the value measured at 1-V differential. The minimum input supply voltage of 2 V (2.3 V over temperature) must be observed.
(4) Thermal regulation is defined as the change in output voltage at a time (T) after a change in power dissipation is applied, excluding load or line regulation effects. Specifications are for a 50-mA load pulse at V_{IN} = 30 V, V_{OUT} = 5 V (1.25-W pulse) for t = 10 ms.
(5) Comparator thresholds are expressed in terms of a voltage differential equal to the nominal reference voltage (measured at V_{IN} – V_{OUT} = 1 V) minus FEEDBACK terminal voltage. To express these thresholds in terms of output voltage change, multiply by the error amplifier gain = V_{OUT} / V_{REF} = (R1 + R2) / R2. For example, at a programmed output voltage of 5 V, the $\overline{\text{ERROR}}$ output is specified to go low when the output drops by 95 mV × 5 V / 1.235 V = 384 mV. Thresholds remain constant as a percentage of V_{OUT} (as V_{OUT} is varied), with the low-output warning occurring at 6% below nominal (typical) and 7.7% (maximum).
(6) For the LP2951-50QDR in the SOIC package, V_{REF} is tested at V_{IN} = 6 V and I_{OUT}=100 µA.

5.6 Typical Characteristics

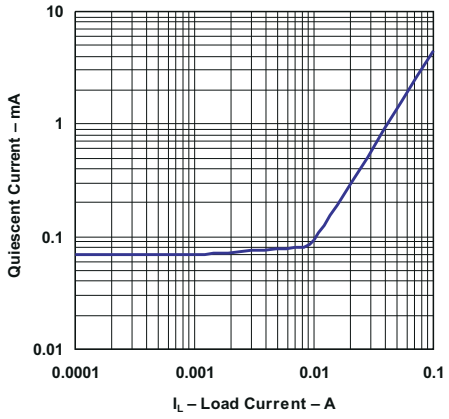


Figure 5-1. Quiescent Current vs Load Current

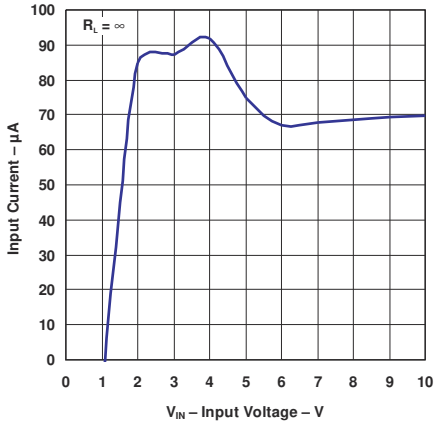


Figure 5-2. Input Current vs Input Voltage

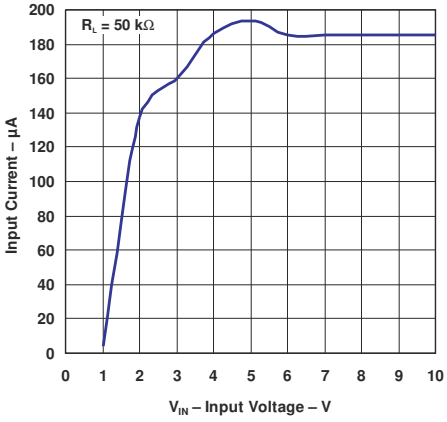


Figure 5-3. Input Current vs Input Voltage

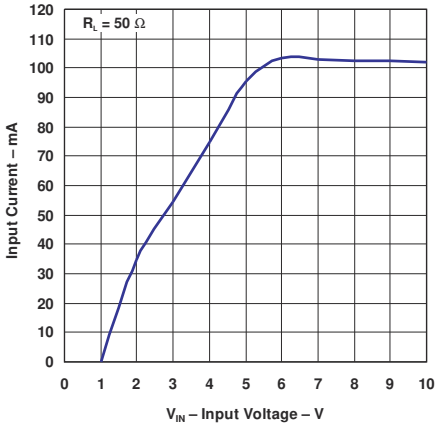


Figure 5-4. Input Current vs Input Voltage

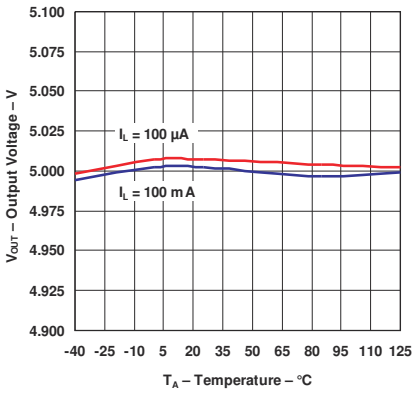


Figure 5-5. Output Voltage vs Temperature

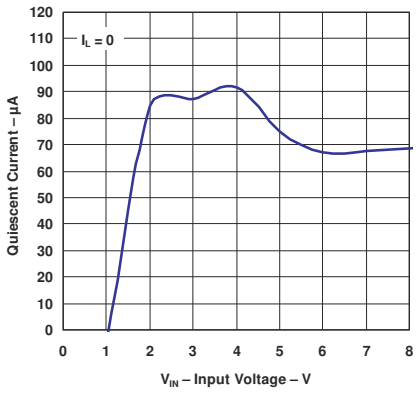


Figure 5-6. Quiescent Current vs Input Voltage

5.6 Typical Characteristics (continued)

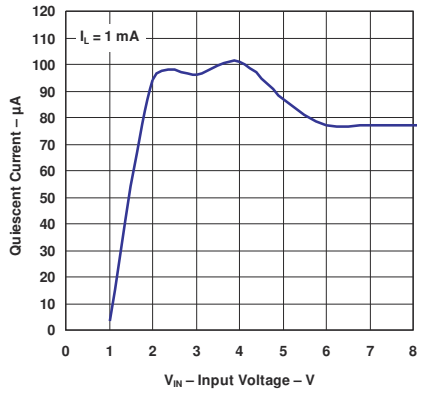


Figure 5-7. Quiescent Current vs Input Voltage

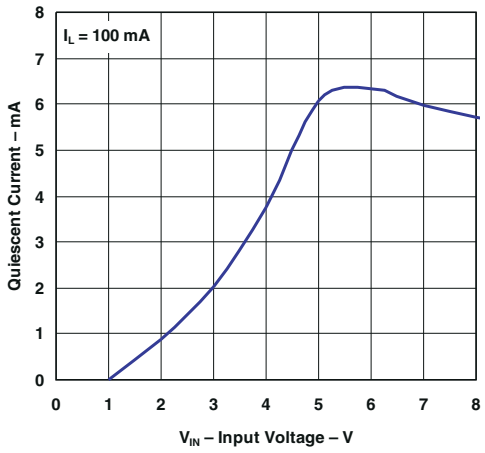


Figure 5-8. Quiescent Current vs Input Voltage

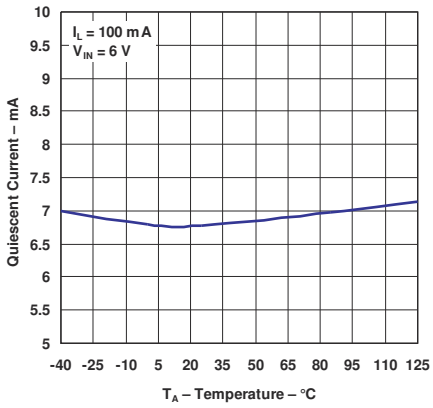


Figure 5-9. Quiescent Current vs Temperature

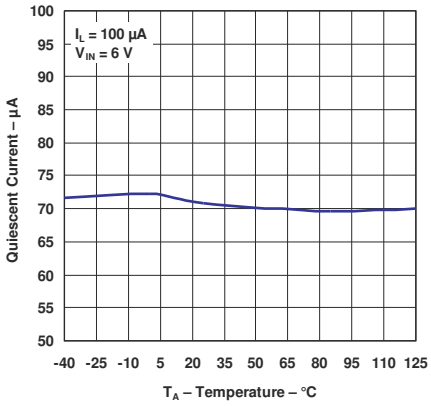


Figure 5-10. Quiescent Current vs Temperature

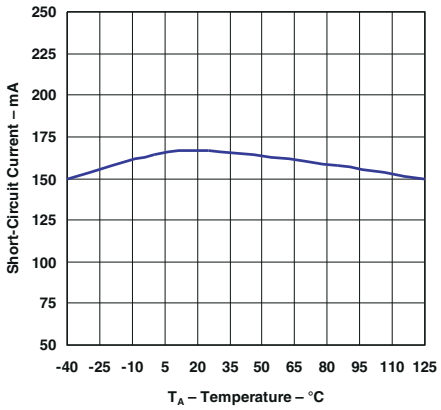


Figure 5-11. Short-Circuit Current vs Temperature

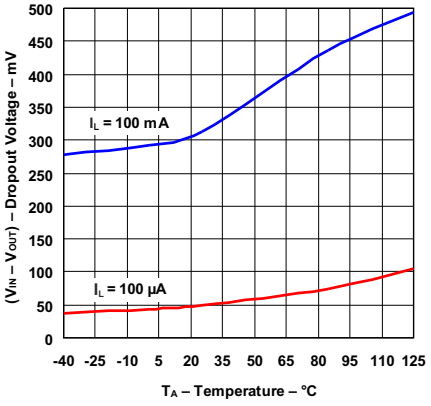


Figure 5-12. Dropout Voltage vs Temperature

5.6 Typical Characteristics (continued)

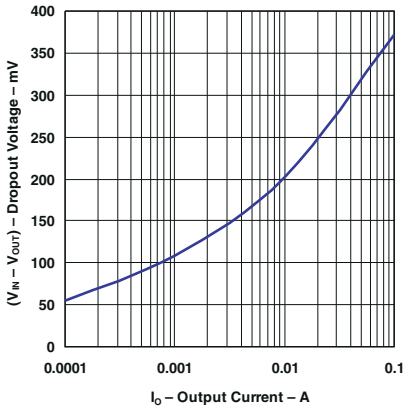


Figure 5-13. Dropout Voltage vs Output Current

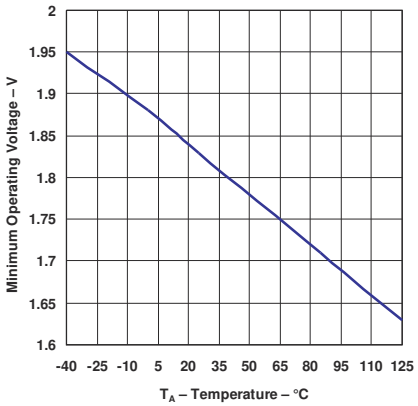


Figure 5-14. Minimum Operating Voltage vs Temperature

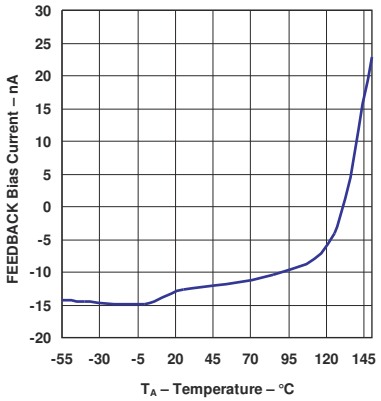


Figure 5-15. Feedback Bias Current vs Temperature

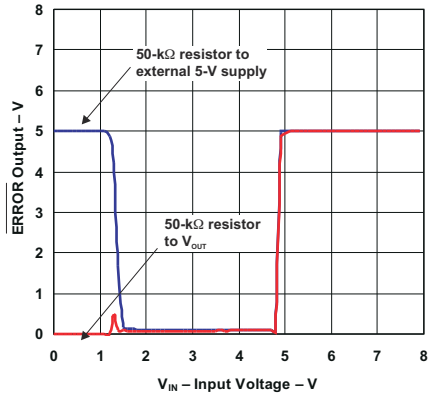


Figure 5-16. $\overline{\text{ERROR}}$ Comparator Output vs Input Voltage

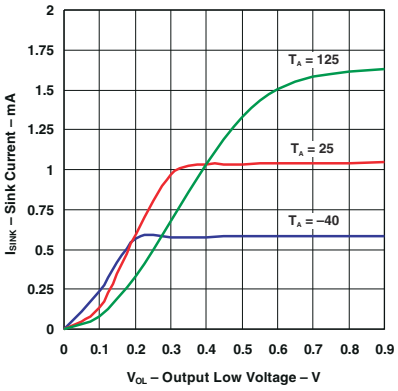


Figure 5-17. $\overline{\text{ERROR}}$ Comparator Sink Current vs Output Low Voltage

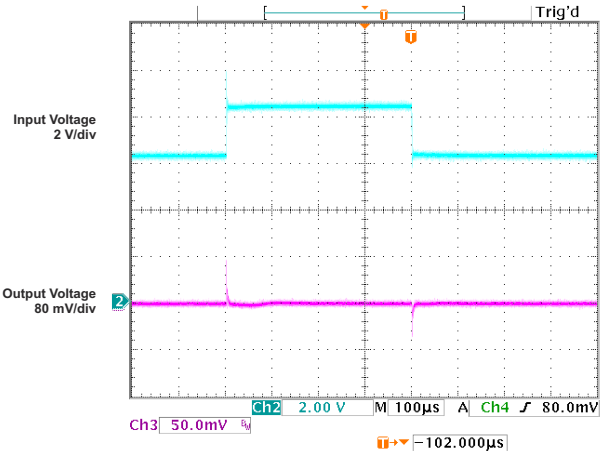
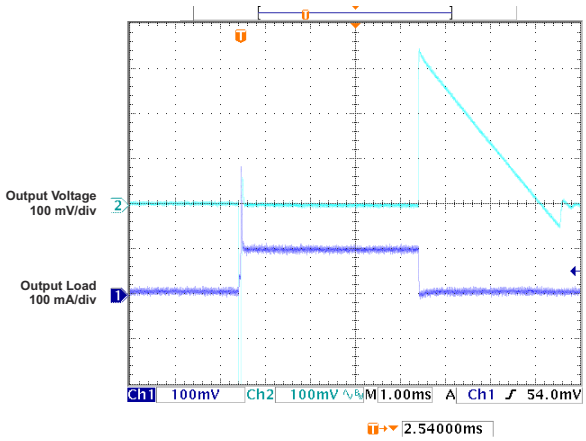


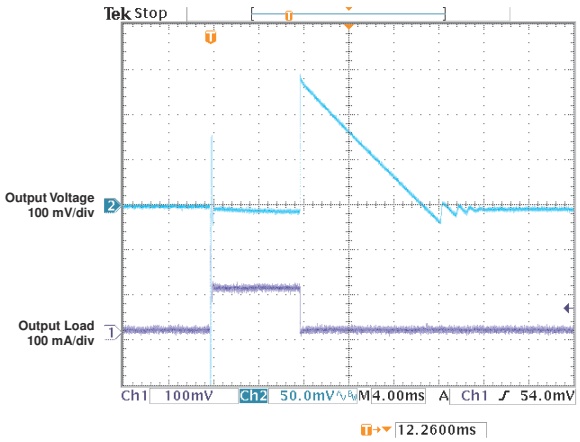
Figure 5-18. Line Transient Response vs Time

5.6 Typical Characteristics (continued)



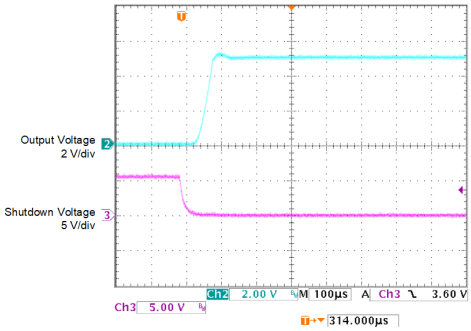
V_{OUT} = 5 V, C_L = 1 µF

Figure 5-19. Load Transient Response vs Time



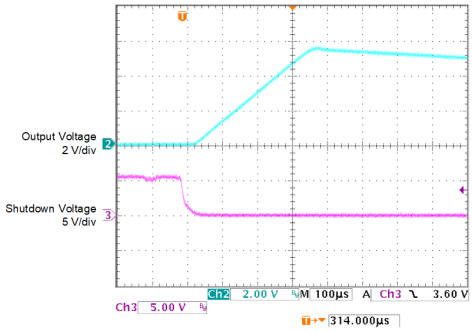
V_{OUT} = 5 V, C_L = 10 µF

Figure 5-20. Load Transient Response vs Time



C_L = 1 µF, I_L = 1 mA

Figure 5-21. Shutdown Transient Response vs Time



C_L = 10 µF, I_L = 1 mA

Figure 5-22. Shutdown Transient Response vs Time

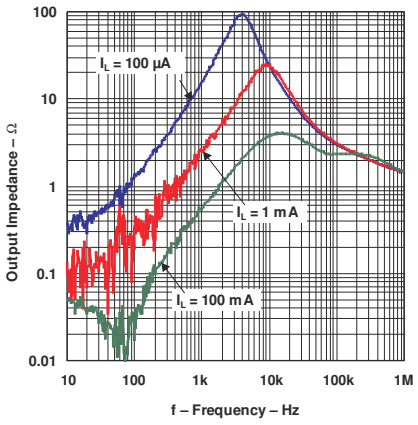


Figure 5-23. Output Impedance vs Frequency

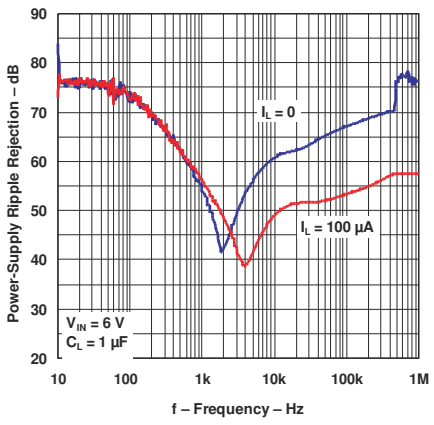


Figure 5-24. Ripple Rejection vs Frequency

5.6 Typical Characteristics (continued)

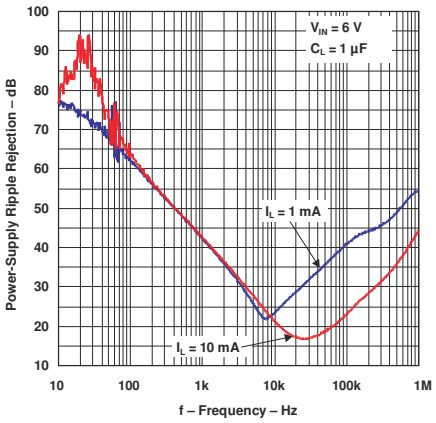


Figure 5-25. Ripple Rejection vs Frequency

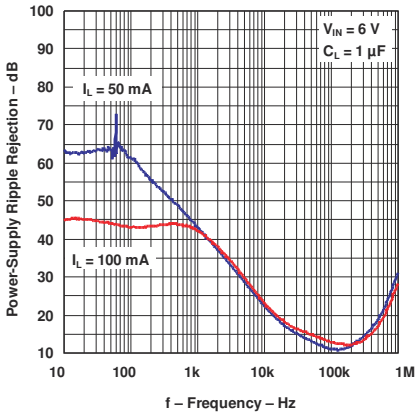


Figure 5-26. Ripple Rejection vs Frequency

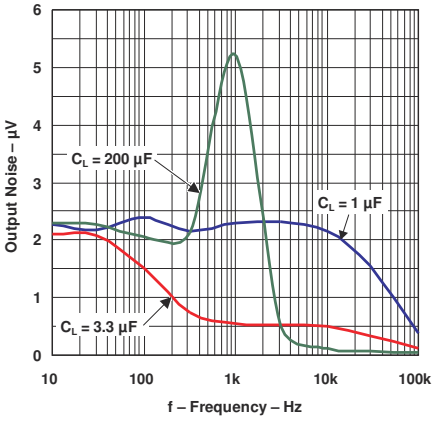


Figure 5-27. Output Noise vs Frequency

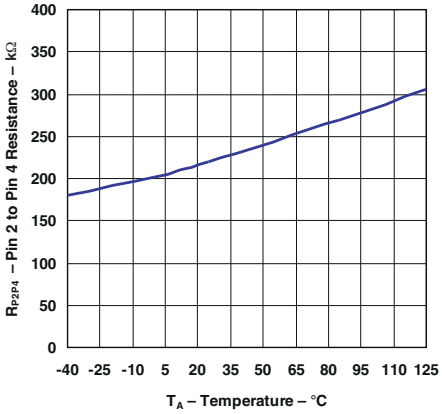


Figure 5-28. Divider Resistance vs Temperature

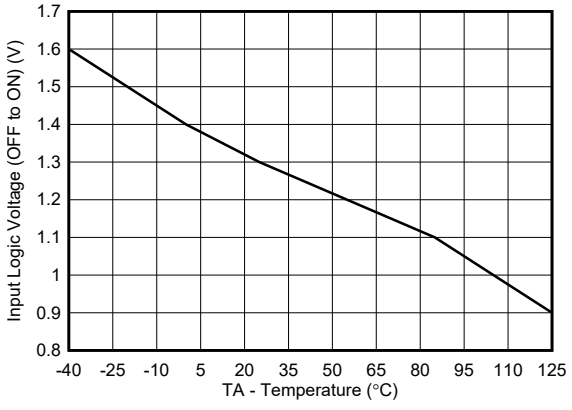


Figure 5-29. Shutdown Threshold Voltage (OFF to ON) vs Temperature

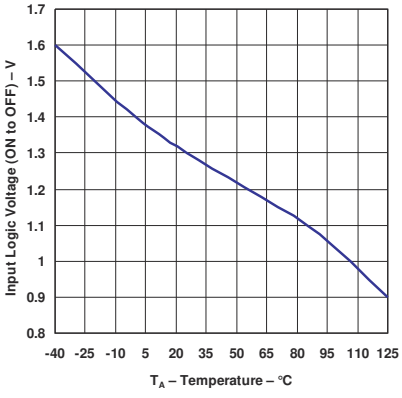


Figure 5-30. Shutdown Threshold Voltage (ON to OFF) vs Temperature

5.6 Typical Characteristics (continued)

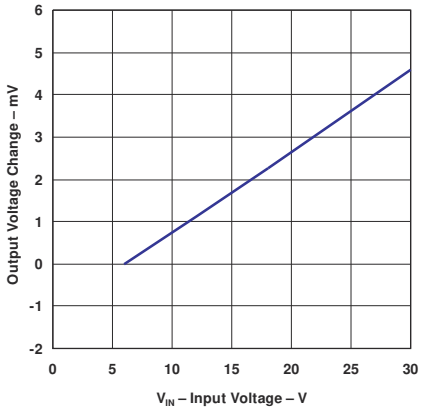


Figure 5-31. Line Regulation vs Input Voltage

6 Detailed Description

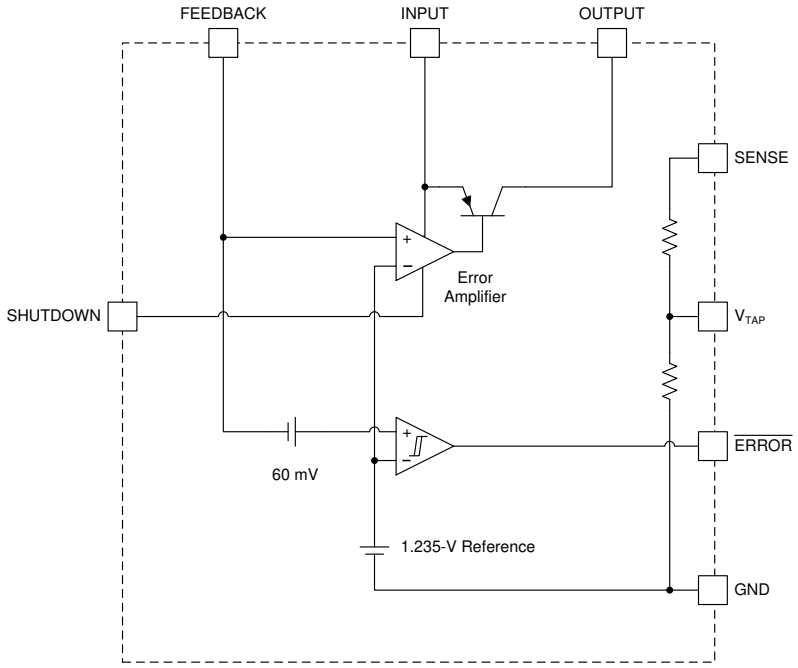
6.1 Overview

The LP2951-Q1 is a bipolar, low-dropout voltage regulator that can accommodate a wide input supply voltage range of up to 30 V. The 8-pin LP2951-Q1 is able to output either a fixed or adjustable output from the same device. By tying the OUTPUT and SENSE pins together, and the FEEDBACK and V_{TAP} pins together, the LP2951-Q1 outputs a fixed 5 V, 3.3 V, or 3 V (depending on the version). Alternatively, by leaving the SENSE and V_{TAP} pins open and connecting FEEDBACK to an external resistor divider, the output can be set to any value between 1.235 V to 30 V.

The 8-pin LP2951-Q1 also offers additional functionality that makes this device particularly designed for battery-powered applications. For example, a logic-compatible shutdown feature allows the regulator to be put in standby mode for power savings. In addition, there is a built-in supervisor reset function in which the $\overline{\text{ERROR}}$ output goes low when V_{OUT} drops by 6% of the nominal value for whatever reason (for example, such as a drop in V_{IN}, current limiting, or thermal shutdown).

The LP2951-Q1 is designed to minimize all error contributions to the output voltage. With a tight output tolerance (0.5% at 25°C), a very low output voltage temperature coefficient (20 ppm typical), extremely good line and load regulation (0.3% and 0.4% typical), and remote sensing capability, the device can be used as either a low-power voltage reference or a 100-mA regulator.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 $\overline{\text{ERROR}}$ Function

The LP2951-Q1 has a low-voltage detection comparator that outputs a logic low when the output voltage drops by approximately 6% from the nominal value, and outputs a logic high when V_{OUT} has reached approximately 95% of the nominal value. This 95% of nominal figure is obtained by dividing the built-in offset of approximately 60 mV by the 1.235-V band-gap reference, and remains independent of the programmed output voltage. For example, the trip-point threshold ($\overline{\text{ERROR}}$ output goes high) typically is 4.75 V for a 5-V output and 11.4 V for a 12-V output. Typically, there is a hysteresis of 15 mV between the thresholds for a high and low $\overline{\text{ERROR}}$ output.

A timing diagram is shown in Figure 6-1 for $\overline{\text{ERROR}}$ vs V_{OUT} (5 V), as V_{IN} is ramped up and down. $\overline{\text{ERROR}}$ becomes valid (low) when V_{IN} is approximately 1.3 V. When V_{IN} is approximately 5 V, V_{OUT} = 4.75 V, causing $\overline{\text{ERROR}}$ to go high. Because the dropout voltage is load dependent, the output trip-point threshold is reached at different values of V_{IN}, depending on the load current. For instance, at higher load current, $\overline{\text{ERROR}}$ goes high at a slightly higher value of V_{IN}, and vice versa for lower load current. The output-voltage trip point remains at approximately 4.75 V, regardless of the load. When $V_{IN} \leq$ 1.3 V, the $\overline{\text{ERROR}}$ comparator output is turned off and pulled high to the pullup voltage. If V_{OUT} is used as the pullup voltage, rather than an external 5-V source, $\overline{\text{ERROR}}$ typically is approximately 1.2 V. In this condition, an equal resistor divider (10 kΩ is acceptable) can be tied to $\overline{\text{ERROR}}$ to divide down the voltage to a valid logic low during any fault condition, while still enabling a logic high during normal operation.

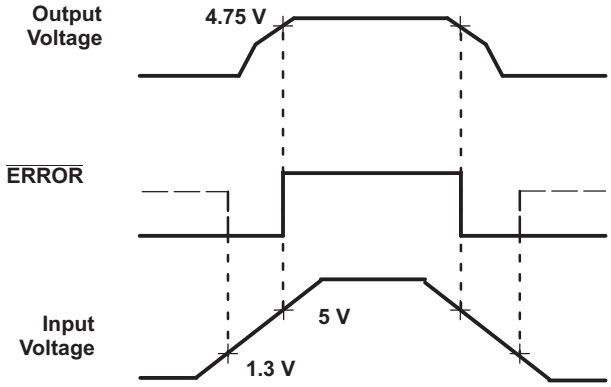


Figure 6-1. $\overline{\text{ERROR}}$ Output Timing

Because the $\overline{\text{ERROR}}$ comparator has an open-collector output, an external pullup resistor is required to pull the output up to V_{OUT} or another supply voltage (up to 30 V). The output of the comparator is rated to sink up to 400 µA. An acceptable range of values for the pullup resistor is from 100 kΩ to 1 MΩ. If $\overline{\text{ERROR}}$ is not used, this pin can be left open.

6.3.2 Programming Output Voltage

A unique feature of the LP2951-Q1 is the ability to output either a fixed voltage or an adjustable voltage, depending on the external pin connections. To output the internally programmed fixed voltage, tie the SENSE pin to the OUTPUT pin and the FEEDBACK pin to the V_{TAP} pin. Alternatively, a user-programmable voltage ranging from the internal 1.235-V reference to a 30-V max can be set by using an external resistor divider pair. The resistor divider is tied to V_{OUT}, and the divided-down voltage is tied directly to FEEDBACK for comparison against the internal 1.235-V reference. To satisfy the steady-state condition in which the two inputs are equal, the error amplifier drives the output to equal Equation 1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R1}{R2}\right) - I_{FB}R_1 \quad (1)$$

where:

- V_{REF} = 1.235 V applied across R2 (see Figure 6-2)
- I_{FB} = FEEDBACK bias current, typically 20 nA

A minimum regulator output current of 1 µA must be maintained. Thus, in an application where a no-load condition is expected (for example, CMOS circuits in standby), this 1-µA minimum current must be provided by the resistor pair, effectively imposing a maximum value of R2 = 1.2 MΩ (1.235 V / 1.2 MΩ ≠ 1 µA).

I_{FB} = 20 nA introduces an error not approximately equal to 0.02% in V_{OUT}. This error can be offset by trimming R1. Alternatively, increasing the divider current makes I_{FB} less significant, thus, reducing the error contribution. For instance, using R2 = 100 kΩ reduces the error contribution of I_{FB} to 0.17% by increasing the divider current to not approximately equal to 12 µA. This increase in the divider current still is small compared to the 600-µA typical quiescent current of the LP2951-Q1 under no load.

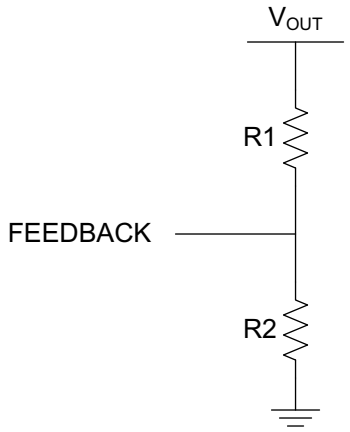


Figure 6-2. Adjusting the Feedback on the LP2951-Q1

6.4 Device Functional Modes

6.4.1 Shutdown Mode

This device can be placed in shutdown mode with a logic high at the SHUTDOWN pin. Return the logic level low to restore operation or tie SHUTDOWN to ground if the feature is not being used.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The LP2951-Q1 is used as a low-dropout regulator with a wide range of input voltages.

7.2 Typical Application

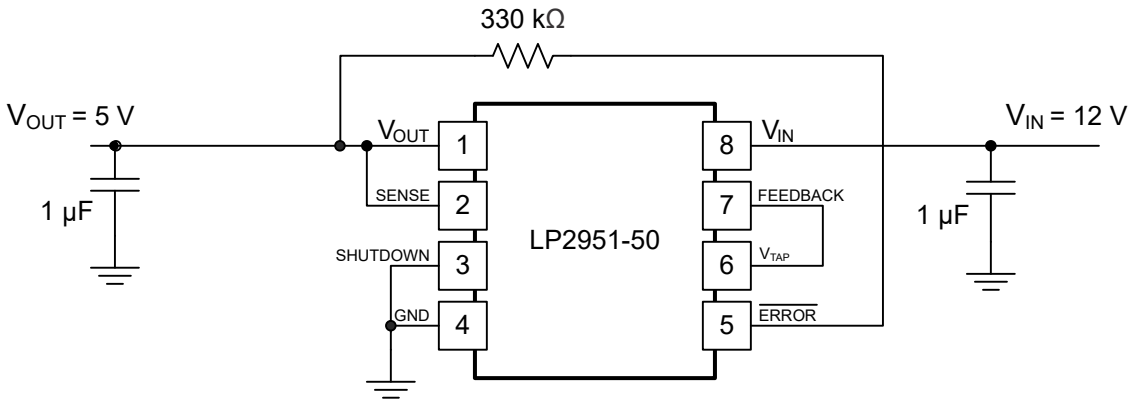


Figure 7-1. 12-V to 5-V Converter

7.2.1 Design Requirements

7.2.1.1 Input Capacitor (C_{IN})

Place a 1-µF (tantalum, ceramic, or aluminum) electrolytic capacitor locally at the input of the LP2951-Q1 if there is, or can be, significant impedance between the ac filter capacitor and the input; for example, if a battery is used as the input or if the ac filter capacitor is located more than 10 inches away. There are no ESR requirements for this capacitor, and the capacitance can be increased without limit.

7.2.1.2 Output Capacitor (C_{OUT})

As with most PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range.

7.2.2 Detailed Design Procedure

7.2.2.1 Capacitance Value

For V_{OUT} ≥ 5 V, a minimum of 1 µF is required. For lower V_{OUT}, the regulator loop gain is running closer to unity gain and, thus, has lower phase margins. Consequently, a larger capacitance is needed for stability.

For V_{OUT} = 3 V or 3.3 V, a minimum of 2.2 µF is recommended. For worst case, V_{OUT} = 1.23 V (using the ADJ version), a minimum of 3.3 µF is recommended. C_{OUT} can be increased without limit and only improves the regulator stability and transient response. Regardless of the value, the output capacitor must have a resonant frequency greater than 500 kHz.

The minimum capacitance values given in this section are for a maximum load current of 100 mA. If the maximum expected load current is less than 100 mA, then lower values of C_{OUT} can be used. For instance, if I_{OUT} < 10 mA, then only 0.33 µF is required for C_{OUT}. For I_{OUT} < 1 mA, 0.1 µF is sufficient for stability requirements. Thus, for a worst-case condition of 100-mA load and V_{OUT} = V_{REF} = 1.235 V (representing the highest load current and lowest loop gain), a minimum C_{OUT} of 3.3 µF is recommended.

For the LP2951-Q1, no load stability is inherent in the design — a desirable feature in CMOS circuits that are put in standby (such as RAM keep-alive applications). If the LP2951-Q1 is used with external resistors to set the output voltage, a minimum load current of 1 µA is recommended through the resistor divider.

7.2.2.2 Capacitor Types

Most tantalum or aluminum electrolytics are acceptable for use at the input. Film-type capacitors also work but at higher cost. When operating at low temperature, care must be taken with aluminum electrolytics, because these electrolytes often freeze at –30°C. For this reason, use solid tantalum capacitors at temperatures below –25°C.

Ceramic capacitors can be used, but because of the low ESR (as low as 5 mΩ to 10 mΩ), these capacitors can possibly not meet the minimum ESR requirement previously discussed. If a ceramic capacitor is used, a series resistor between 0.1 Ω to 2 Ω must be added to meet the minimum ESR requirement. In addition, ceramic capacitors have one glaring disadvantage that must be taken into account — a poor temperature coefficient, where the capacitance can vary significantly with temperature. For instance, a large-value ceramic capacitor (≥ 2.2 µF) can lose more than half of the capacitance as temperature rises from 25°C to 85°C. Thus, a 2.2-µF capacitor at 25°C drops well below the minimum C_{OUT} required for stability as ambient temperature rises. For this reason, select an output capacitor that maintains the minimum 2.2 µF required for stability for the entire operating temperature range.

7.2.2.3 C_{BYPASS}: Noise and Stability Improvement

In the LP2951-Q1, an external FEEDBACK pin directly connected to the error amplifier noninverting input can allow stray capacitance to cause instability by shunting the error amplifier feedback to GND, especially at high frequencies. This instability is worsened if high-value external resistors are used to set the output voltage, because a high resistance allows the stray capacitance to play a more significant role (that is, a larger RC time delay is introduced between the output of the error amplifier and the FEEDBACK input, leading to more phase shift and lower phase margin). A solution is to add a 100-pF bypass capacitor (C_{BYPASS}) between OUTPUT and FEEDBACK; because C_{BYPASS} is in parallel with R1, this capacitor lowers the impedance introduced at FEEDBACK at high frequencies, in effect offsetting the effect of the parasitic capacitance by providing more feedback at higher frequencies. More feedback forces the error amplifier to work at a lower loop gain, so C_{OUT} must be increased to a minimum of 3.3 µF to improve the regulator phase margin.

C_{BYPASS} can be also used to reduce output noise in the LP2951-Q1. This bypass capacitor reduces the closed-loop gain of the error amplifier at the high frequency, so noise no longer scales with the output voltage. This improvement is more noticeable with higher output voltages, where loop-gain reduction is greatest. An acceptable C_{BYPASS} is calculated as shown in Equation 2:

$$f_{(CBYPASS)} \simeq 200\ Hz \rightarrow C_{(BYPASS)} = \frac{1}{2\pi \times R1 \times 200\ Hz} \quad (2)$$

7.2.2.4 ESR Range

The regulator control loop relies on the ESR of the output capacitor to provide a zero to add sufficient phase margin to ensure unconditional regulator stability; this condition requires the closed-loop gain to intersect the open-loop response in a region where the open-loop gain rolls off at 20 dB/decade. This roll off ensures that the phase is always less than 180° (phase margin greater than 0°) at unity gain. Thus, a minimum-maximum range for the ESR must be observed.

The upper limit of this ESR range is established by the fact that an ESR that is too high can result in the zero occurring too soon, causing the gain to roll off too slowly. This effect, in turn, allows a third pole to appear before unity gain and introduces enough phase shift to cause instability. This phase shift typically limits the maximum ESR to approximately 5 Ω.

Conversely, the lower limit of the ESR range is tied to the fact that an ESR that is too low shifts the zero too far out, past unity gain, which allows the gain to roll off at 40 dB/decade at unity gain, resulting in a phase shift of greater than 180°. Typically, limiting the minimum ESR to approximately 20 mΩ to 30 mΩ.

7.2.3 Application Curves

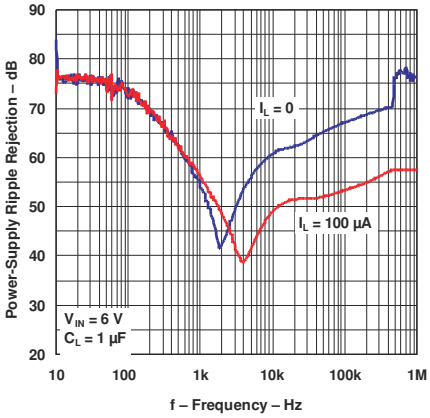


Figure 7-2. Ripple Rejection vs Frequency

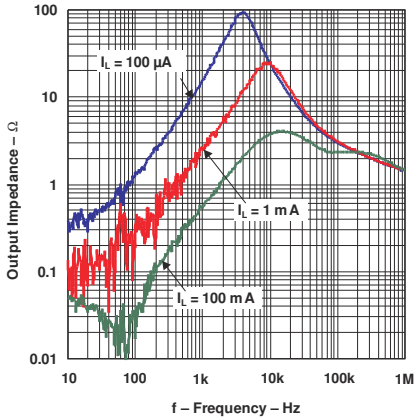


Figure 7-3. Output Impedance vs Frequency

7.3 Power Supply Recommendations

Limit maximum input voltage to 30 V for proper operation. Place input and output capacitors as close to the device as possible to take advantage of the high-frequency, noise-filtering properties.

7.4 Layout

7.4.1 Layout Guidelines

Make sure that traces on the input and outputs of the device are wide enough to handle the desired currents. For this device, the output trace must be larger in order to accommodate the larger available current.

Place input and output capacitors as close to the device as possible to take advantage of the high-frequency, noise-filtering properties.

7.4.2 Layout Example

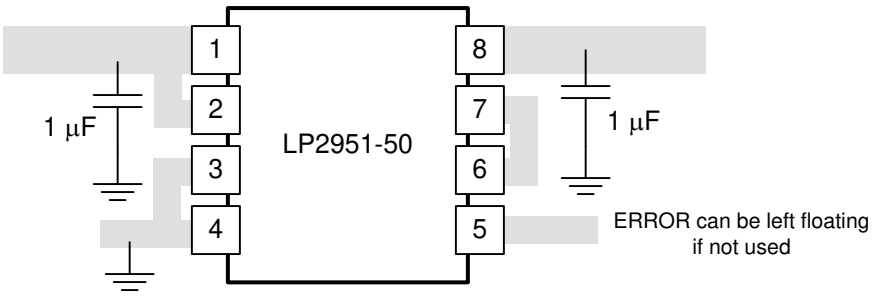


Figure 7-4. Layout Example (D Package)

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (August 2023) to Revision G (April 2024)	Page
• Added correct temperature grade 1 range to AEC-Q100 *Features* bullet	1
• Changed *LP2591-50-Q1* to *LP2951-50-Q1* in *Package Information* table and D package pinout drawing	1

Changes from Revision E (November 2014) to Revision F (August 2023)	Page
• Changed the numbering format for tables, figures, and cross-references throughout the document	1
• Changed device name to *LP2951-Q1* from *LP2951-50-Q1 and LP2951-33-Q1* throughout document	1
• Changed automotive-specific bullets in *Features* section	1
• Changed accuracy feature to correct typical accuracy specification	1
• Added links to *Applications* section	1
• Changed *Device Information* table to match package offering	1
• Changed front-page image	1
• Changed *Enable* to *Shutdown* in *Shutdown Transient Response vs Time* curves	7
• Changed *Application Curves* section	18

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2951-33QDRGRQ1	ACTIVE	SON	DRG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	RACQ	Samples
LP2951-50QDRGRQ1	ACTIVE	SON	DRG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	ZUFQ	Samples
LP2951-50QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	KY515Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP2951-Q1 :

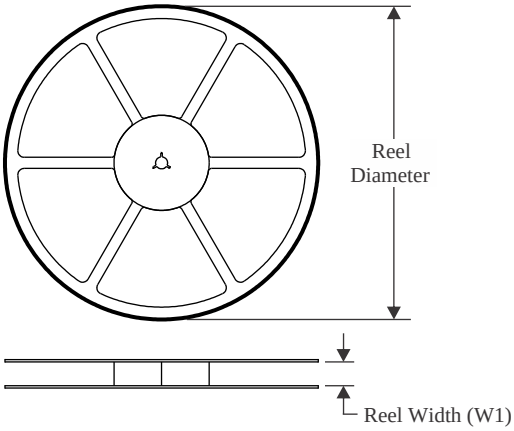
- Catalog : LP2951

NOTE: Qualified Version Definitions:

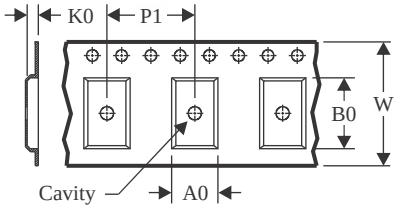
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

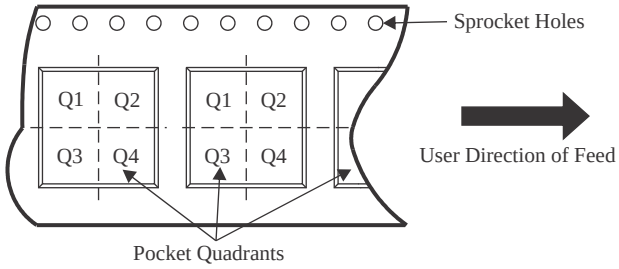


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

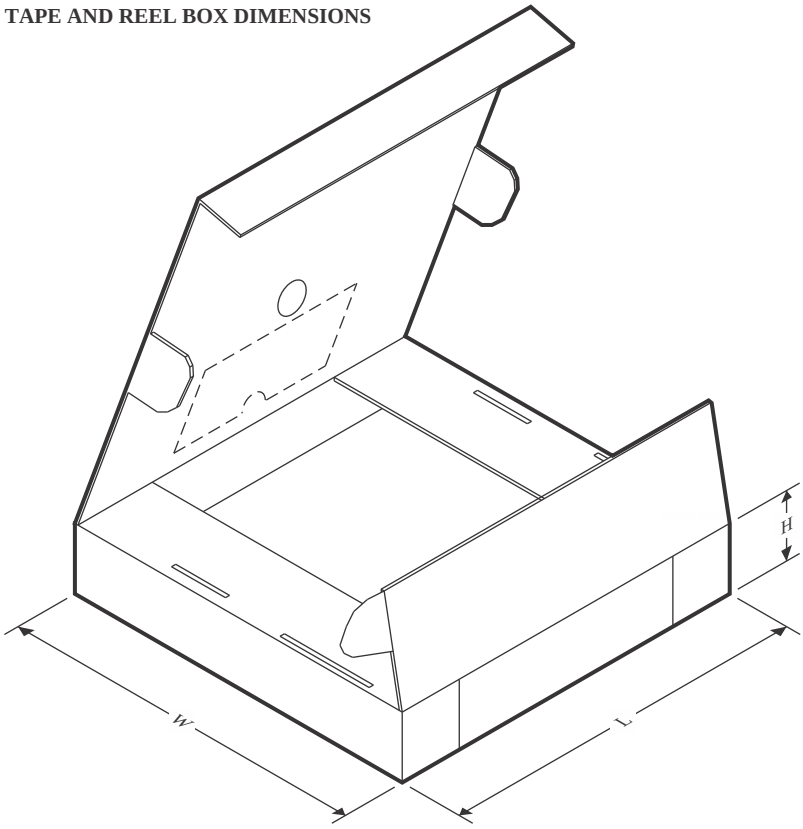
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

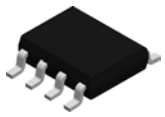
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2951-33QDRGRQ1	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP2951-50QDRGRQ1	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
LP2951-50QDRQ1	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2951-33QDRGRQ1	SON	DRG	8	3000	367.0	367.0	35.0
LP2951-50QDRGRQ1	SON	DRG	8	3000	367.0	367.0	35.0
LP2951-50QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0

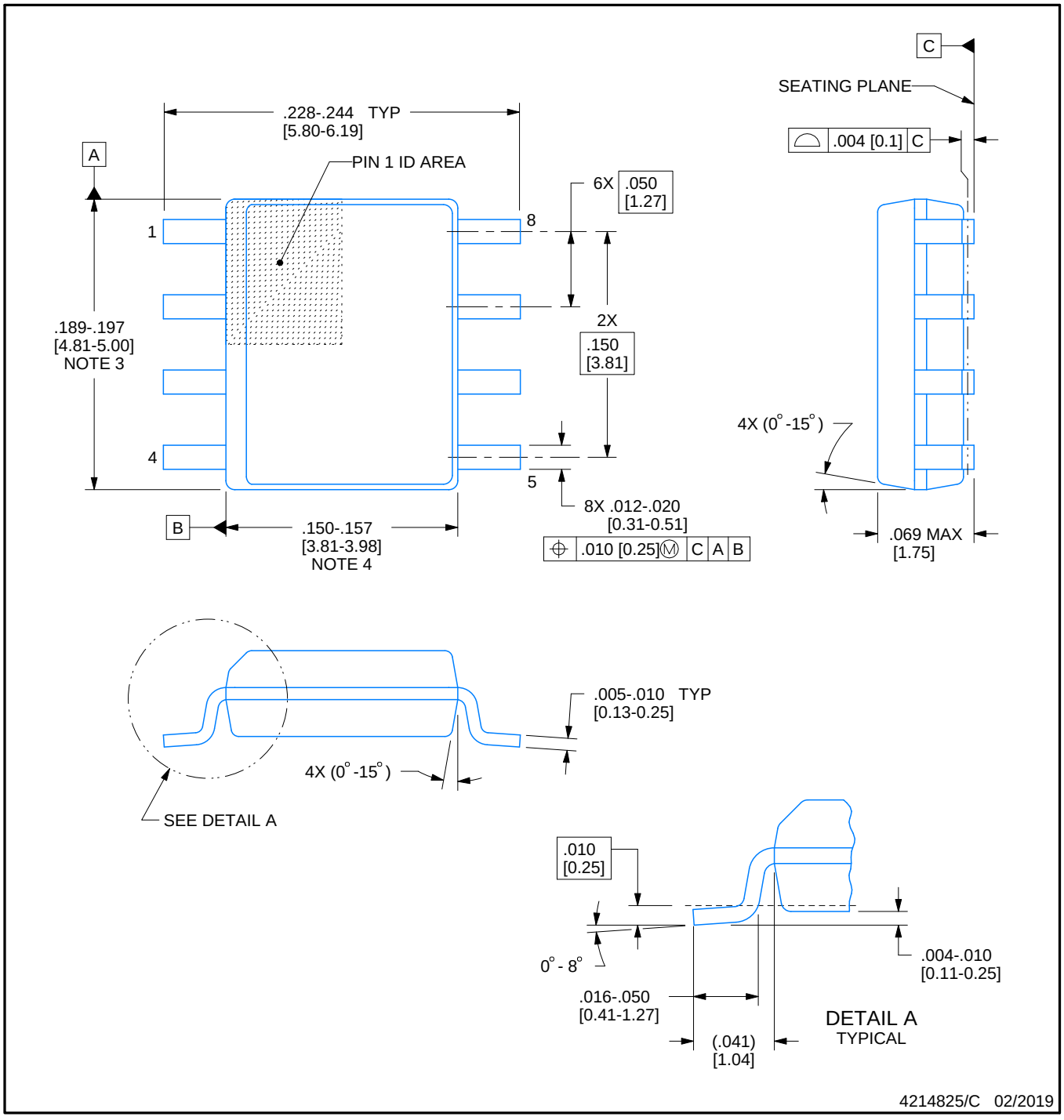


PACKAGE OUTLINE

D0008A

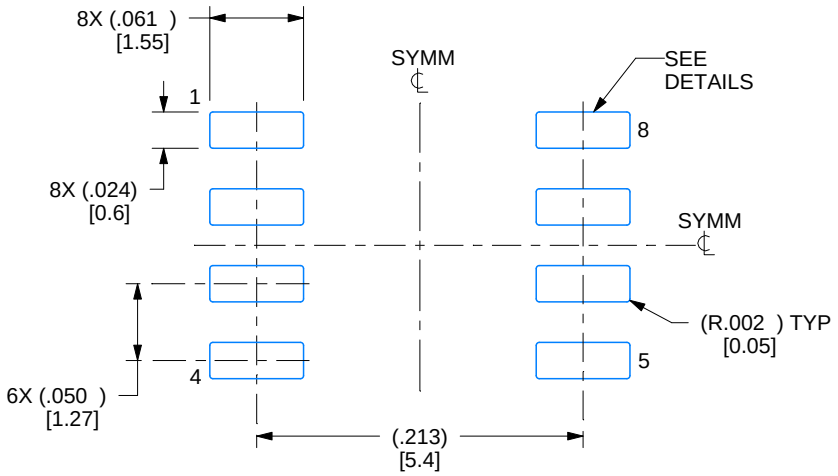
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

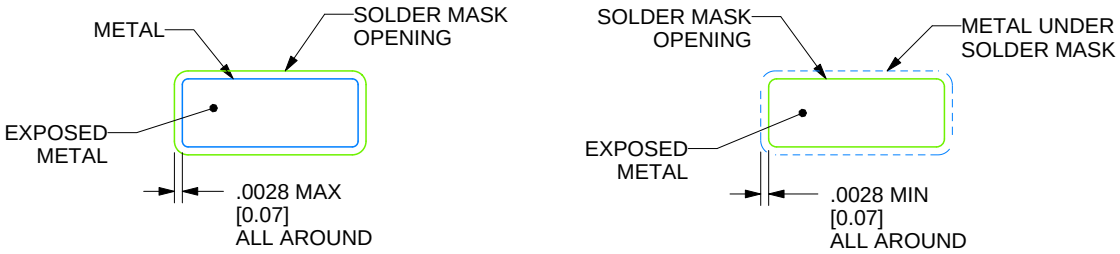


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

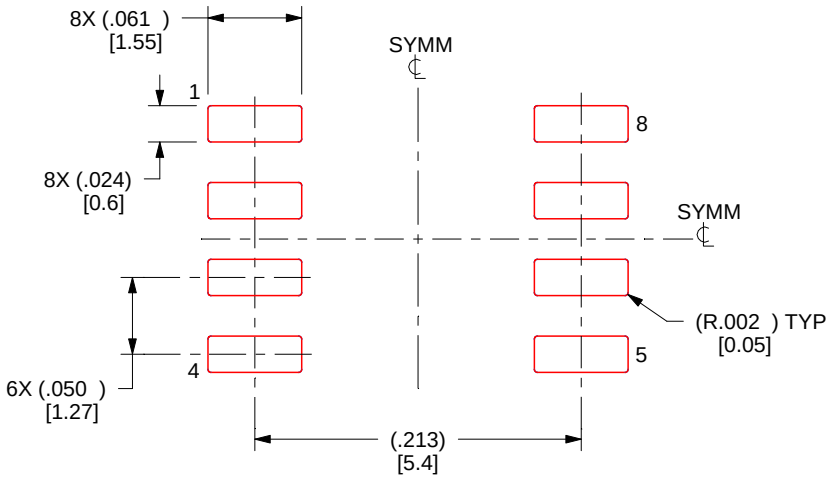
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



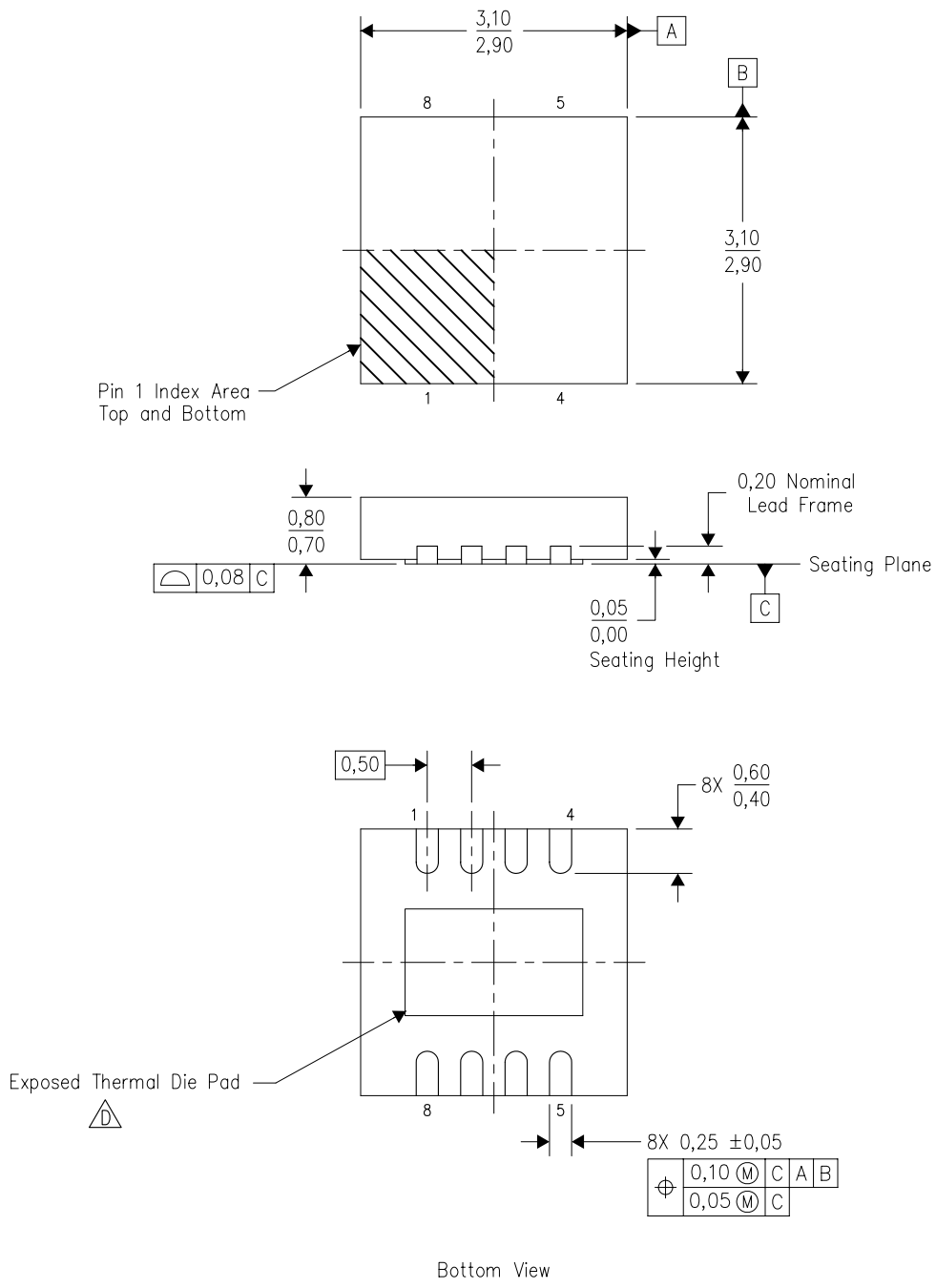
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



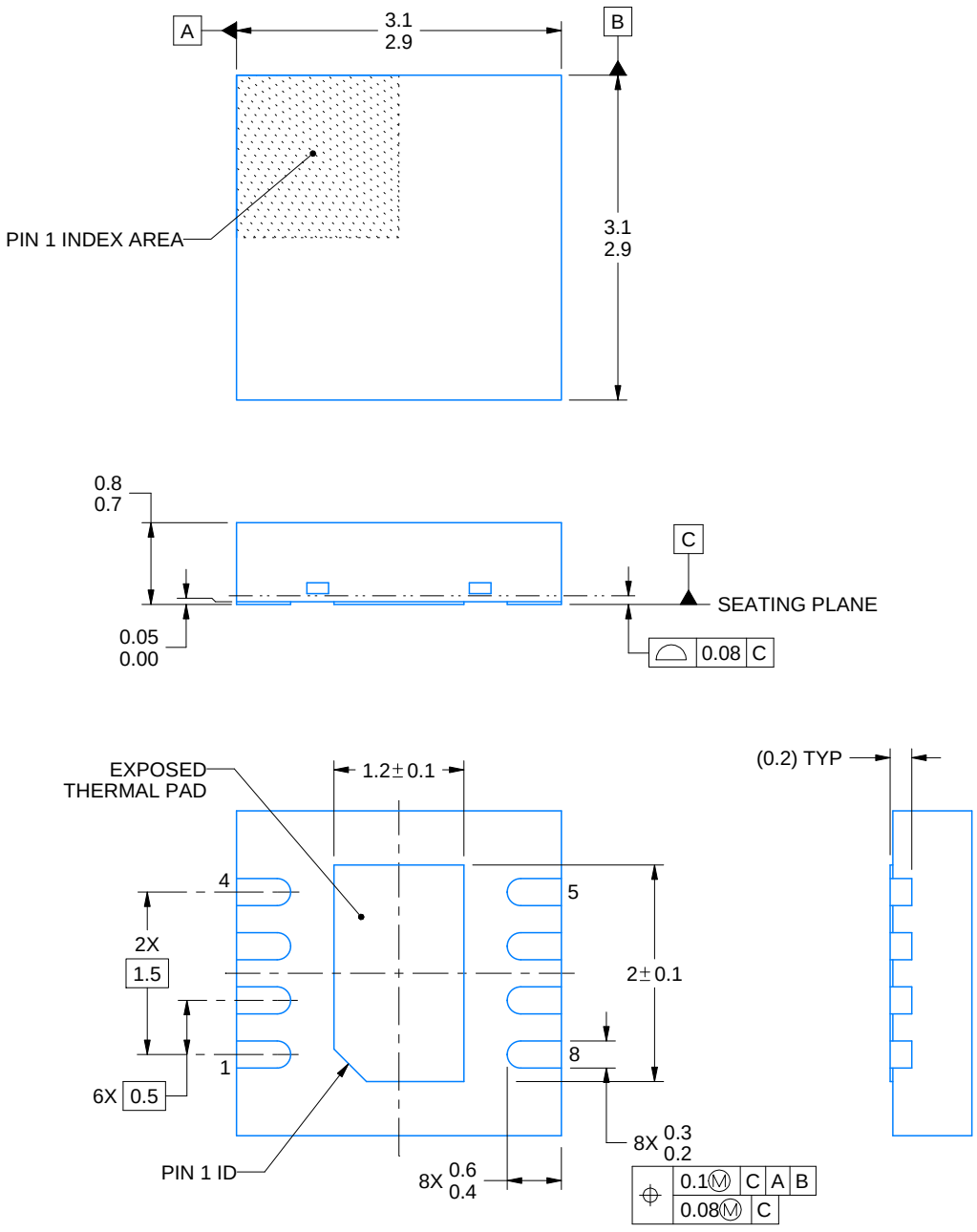
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

PACKAGE OUTLINE

DRG0008A

WSON - 0.8 mm max height

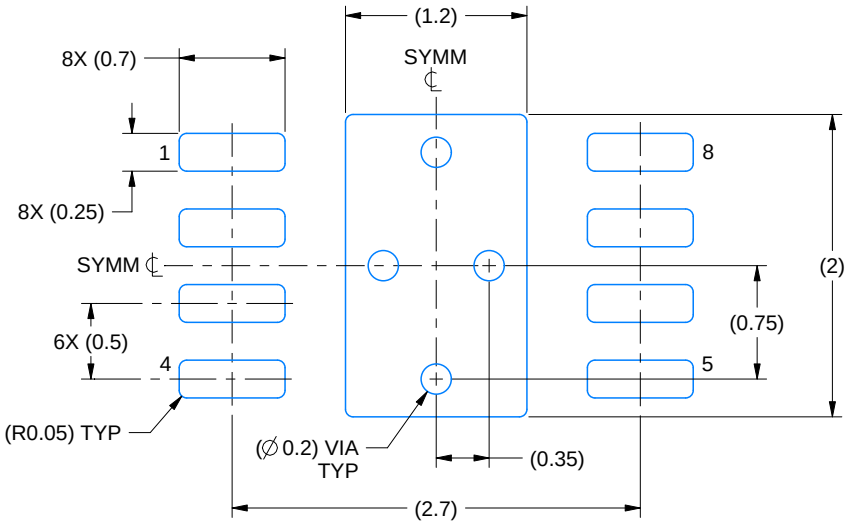
PLASTIC SMALL OUTLINE - NO LEAD



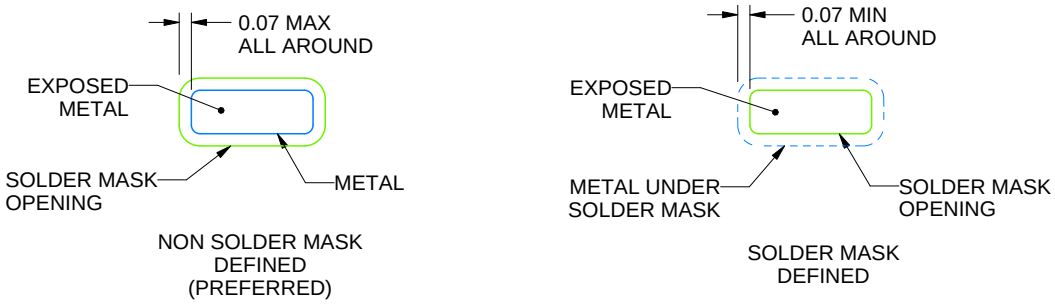
4218885/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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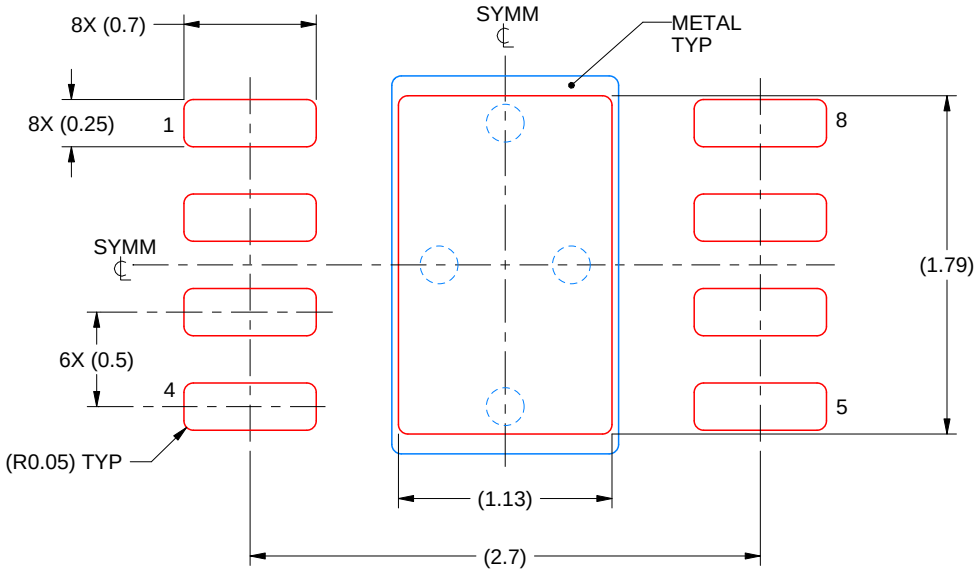
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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