TPS25947xx, 2.7-V–23-V, 5.5-A, 28-mΩ True Reverse Current Blocking eFuse with Input Reverse Polarity Protection

1 Features

- Wide operating input voltage range: 2.7 V to 23 V
  - 28-V absolute maximum
  - Withstands negative voltages up to –15 V
- Integrated back-to-back FETs with low on-resistance: R_{ON} = 28.3 mΩ (typ.)
- Ideal diode operation with true reverse current blocking
- Fast overvoltage protection
  - Overvoltage clamp (OVC) with pin-selectable threshold (3.8 V, 5.7 V, 13.8 V) and 5-µs (typ.) response time OR
  - Adjustable overvoltage lockout (OVLO) with 1.2-µs (typ.) response time
- Overcurrent protection with load current monitor output (ILM)
  - Active current limit OR circuit-breaker options
  - Adjustable threshold (I_{LIM}) 0.5 A–6 A
    - ±10% accuracy for I_{LIM} > 1 A
  - Adjustable transient blanking timer (ITIMER) to allow peak currents up to 2 × I_{LIM}
  - Output load current monitor accuracy: ±6% (I_{OUT} ≥ 1 A)
- Fast-trip response for short-circuit protection
  - 500-ns (typ.) response time
  - Adjustable (2 × I_{LIM}) and fixed thresholds
- Active high enable input with adjustable undervoltage lockout threshold (UVLO)
- Adjustable output slew rate control (dVdt)
- Overtemperature protection
- Digital outputs
  - Priority power MUX control (AUXOFF) and fault indication ($\overline{FLT}$) or
  - Power Good indication (PG) with adjustable threshold (PGTH)
- UL 2367 recognition
  - File No. E339631
  - R_{ILM} ≥ 750 Ω
- IEC 62368-1 CB certified
- Small footprint: QFN 2 mm × 2 mm, 0.45-mm pitch

2 Applications

- Power MUX/ORing
- Adapter input protection
- USB PD protection – PC, notebook, monitors, docks
- Server, PC motherboard, and add-on cards
- Enterprise storage – RAID/HBA/SAN/eSSD
- Patient monitors

3 Description

The TPS25947xx family of eFuses is a highly integrated circuit protection and power management solution in a small package. The devices provide multiple protection modes using very few external components and are a robust defense against overloads, short-circuits, voltage surges, reverse polarity and excessive inrush current. With integrated back-to-back FETs, reverse current flow from output to input is blocked at all times, making the devices well suited for power MUX/ORing applications as well as systems which need load side energy hold up storage in case input power supply fails. The devices use linear ORing based scheme to ensure almost zero DC reverse current and emulate ideal diode behavior with minimum forward voltage drop and power dissipation.

Output slew rate and inrush current can be adjusted using a single external capacitor. Loads are protected from input overvoltage conditions either by clamping the output to a safe fixed maximum voltage (pin selectable), or by cutting off the output if input exceeds an adjustable overvoltage threshold. The devices respond to output overload by actively limiting the current or breaking the circuit. The output current limit threshold as well as the transient overcurrent blanking timer are user adjustable. The current limit control pin also functions as an analog load current monitor.

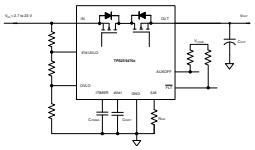
The devices are available in a 2-mm × 2-mm, 10-pin HotRod QFN package for improved thermal performance and reduced system footprint.

The devices are characterized for operation over a junction temperature range of –40°C to +125°C.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
TPS25947xxRPW	QFN (10)	2 mm × 2 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (March 2021) to Revision B (March 2022)	Page
• Updated the UIL/IEC certification status	1
• Corrected the ESD Ratings to show CDM testing was per JS-002	6
• Updated image formatting	12
• Updated Table 8-5	37

Changes from Revision * (October 2020) to Revision A (March 2021)	Page
• Changed status from "Advance Information" to "Production Data"	1

5 Device Comparison Table

Part Number	Overvoltage Response	Overcurrent Response	AUXOFF or PG	$\overline{\text{FLT}}$ or PGTH	Response to Fault
TPS259470ARPW	Adjustable OVLO	Active Current Limit	AUXOFF	$\overline{\text{FLT}}$	Auto-Retry
TPS259470LRPW					Latch-Off
TPS259472ARPW	Pin Selectable OVC (3.8 V/5.7 V/13.8 V)		PG	PGTH	Auto-Retry
TPS259472LRPW					Latch-Off
TPS259474ARPW	Adjustable OVLO	Circuit Breaker			Auto-Retry
TPS259474LRPW					Latch-Off

6 Pin Configuration and Functions

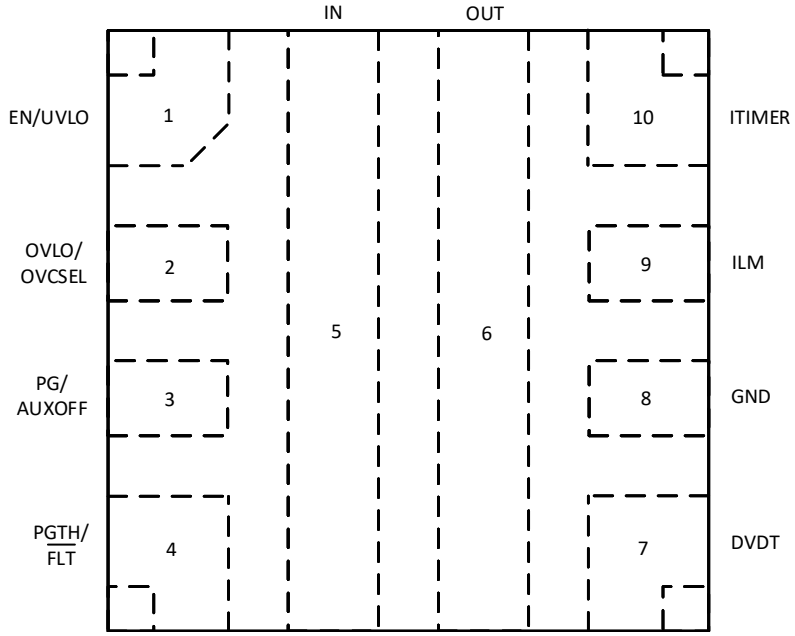


Figure 6-1. TPS25947xx RPW Package 10-Pin QFN Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active High Enable for the device. A Resistor Divider on this pin from input supply to GND can be used to adjust the Undervoltage Lockout threshold. *Do not leave floating.* Refer to Section 8.3.2 for details.
OVLO	2	Analog Input	**TPS259470x, TPS259474x:** A Resistor Divider on this pin from supply to GND can be used to adjust the Overvoltage Lockout threshold. This pin can also be used as an Active Low Enable for the device. *Do not leave floating.* Refer to Section 8.3.3 for details.
OVCSEL		Analog Input	**TPS259472x:** Overvoltage Clamp Threshold Select Pin. Refer to Section 8.3.4 for details.
PG	3	Digital Output	**TPS259472x, TPS259474x:** Power Good indication. This pin is an Open Drain signal which is asserted High when the internal powerpath is fully turned ON and PGTH input exceeds a certain threshold. Refer to Section 8.3.11 for more details.
AUXOFF		Digital Output	**TPS259470x:** Auxiliary channel control signal. This pin is an Open Drain signal which is asserted High when the input supply is valid and channel has completed inrush sequence. This can be used to enable/disable the auxiliary supply eFuse to facilitate smooth switchover in a Priority power MUXing configuration. Refer to Section 8.3.10 for more details.
$\overline{\text{FLT}}$	4	Digital Output	**TPS259470x:** Active low Fault event indicator. This pin is an Open Drain signal which will be pulled low when a fault is detected. Refer to Section 8.3.9 for more details.
PGTH		Analog Input	**TPS259472x, TPS259474x:** Power Good Threshold. Refer to Section 8.3.11 for more details.
IN	5	Power	Power input
OUT	6	Power	Power output
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to Section 8.3.5.1 for details.
GND	8	Ground	This pin is the ground reference for all internal circuits and must be connected to system GND.

Table 6-1. Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
ILM	9	Analog Output	This pin is a dual function pin used to limit and monitor the output current. An external resistor from this pin to GND sets the output current limit threshold during start-up as well as steady state. The pin voltage can also be used as analog output load current monitor signal. *Do not leave floating.* Refer to Section 8.3.5.2 or Section 8.3.5.3 for more details.
ITIMER	10	Analog Output	A capacitor from this pin to GND sets the overcurrent blanking interval during which the output current can temporarily exceed set current limit (but lower than fast-trip threshold) before the device overcurrent response takes action. Leave this pin open for fastest response to overcurrent events. Refer to Section 8.3.5.2 or Section 8.3.5.3 for more details.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range, –40°C ≤ T_J ≤ 125°C	IN	max(–15, V_{OUT} – 21)	28	V
	Maximum Input Voltage Range, –10°C ≤ T_J ≤ 125°C		max(–15, V_{OUT} – 22)	28	V
V_{OUT}	Maximum Output Voltage Range, –40°C ≤ T_J ≤ 125°C	OUT	–0.3	min (28, V_{IN} + 21)	
	Maximum Output Voltage Range, –10°C ≤ T_J ≤ 125°C		–0.3	min (28, V_{IN} + 22)	
$V_{OUT,PLS}$	Minimum Output Voltage Pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable Pin Voltage Range (2)	EN/UVLO	–0.3	6.5	V
V_{OVLO}	Maximum OVLO Pin Voltage Range (TPS259470x/4x) (2)	OVLO	–0.3	6.5	V
V_{OVCSEL}	Maximum OVCSEL Pin Voltage Range (TPS259472x)	OVCSEL	Internally Limited		V
V_{dVdT}	Maximum dVdT Pin Voltage Range	dVdt	Internally Limited		V
V_{ITIMER}	Maximum ITIMER Pin Voltage Range	ITIMER	Internally Limited		V
V_{PGTH}	Maximum PGTH Pin Voltage Range (TPS259472x/4x) (2)	PGTH	–0.3	6.5	V
V_{AUXOFF}	Maximum AUXOFF Pin Voltage Range (TPS259470x)	AUXOFF	–0.3	6.5	V
V_{PG}	Maximum PG Pin Voltage Range (TPS259472x/4x)	PG	–0.3	6.5	V
V_{FLTB}	Maximum $\overline{FLT}$ Pin Voltage Range (TPS259470x) (2)	$\overline{FLT}$	–0.3	6.5	V
V_{ILM}	Maximum ILM Pin Voltage Range	ILM	Internally Limited		V
I_{MAX}	Maximum Continuous Switch Current	IN to OUT	Internally Limited		A
T_J	Junction temperature		Internally Limited		°C
T_{LEAD}	Maximum Lead Temperature			300	°C
T_{STG}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) If this pin has a pull-up up to V_{IN}, it is recommended to use a resistance of 350 kΩ or higher to limit the current under conditions where IN can be exposed to reverse polarity.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input Voltage Range	IN	2.7	23 (1)	V
V_{OUT}	Output Voltage Range	OUT		min (23, V_{IN} + 20)	V
$V_{EN/UVLO}$	Enable Pin Voltage Range	EN/UVLO		5 (2)	V
V_{OVLO}	OVLO Pin Voltage Range (TPS259470x/4x)	OVLO	0.5	1.5	V
V_{dVdT}	dVdt Capacitor Voltage Rating	dVdt	V_{IN} + 5 V (3)		V
V_{FLTB}	$\overline{FLT}$ Pin Voltage Range (TPS259470x)	$\overline{FLT}$		5 (4)	V
V_{PGTH}	PGTH Pin Voltage Range (TPS259472x/4x)	PGTH		5 (4)	V
V_{AUXOFF}	AUXOFF Pin Voltage Range (TPS259470x)	AUXOFF		5 (4)	V
V_{PG}	PG Pin Voltage Range (TPS259472x/4x)	PG		5 (4)	V
V_{ITIMER}	ITIMER Pin Capacitor Voltage Rating	ITIMER	4		V
R_{ILM}	ILM Pin Resistance	ILM	549	6650	Ω
I_{MAX}	Continuous Switch Current, T_J ≤ 125°C	IN to OUT		5.5	A
T_J	Junction temperature		–40	125	°C

(1) For TPS259472x variants, the input operating voltage should be limited to the selected Output Voltage Clamp threshold as listed in the Electrical Characteristics section
(2) For supply voltages below 5V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5V or systems which can be exposed to reverse polarity on input supply, it is recommended to use a pull-up resistor with a minimum value of 350 kΩ.
(3) In a PowerMUX/ORing scenario with unequal supplies, the dVdt capacitor rating for each device should be chosen based on the highest of the 2 rails.
(4) For systems which can be exposed to reverse polarity on input supply, if this pin is referred to input supply, it is recommended to use a pull-up resistor with a minimum value of 350 kΩ to limit the current through the pin.

7.4 Thermal Information

THERMAL METRIC (1)		TPS25947xx RPW (QFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.7 (2)	°C/W
		74.5 (3)	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20 (2)	°C/W
		27.6 (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device
(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device

7.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V for TPS259470x/4x, OVCSEL = 390 kΩ to GND for TPS259472x, R_{ILM} = 549 Ω , dVdT = Open, ITIMER = Open, AUXOFF = Open for TPS259470x, $\overline{FLT}$ = Open for TPS259470x, PGTH = Open for TPS259472x/4x, PG = Open for TPS259472x/4x. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$V_{UVP(R)}$	IN Supply UVP Rising threshold	2.44	2.53	2.64	V
$V_{UVP(F)}$	IN Supply UVP Falling threshold	2.35	2.42	2.55	V
$I_{Q(ON)}$	IN Supply Quiescent Current (TPS259470x)		428	610	µA
	IN Supply Quiescent Current (TPS259472x)		426	610	µA
	IN Supply Quiescent Current (TPS259474x)		428	610	µA
	IN Supply Quiescent Current during RCB, V_{OUT} = V_{IN} + 1 V		193		µA
	IN Supply Current during OVC (TPS259472x)		445	625	µA
$I_{Q(OFF)}$	IN Supply disabled State Current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		73	130	µA
I_{SD}	IN Supply Shutdown Current (V_{EN} < $V_{SD(F)}$)		4.4	28.7	µA
$I_{Q(OVLO)}$	IN Supply OFF Current (OVLO condition), V_{OUT} = V_{IN} + 1 V		190	267	µA
$I_{INLKG(IRPP)}$	IN Supply Leakage Current (V_{IN} = –14 V, V_{OUT} = 0 V)		–3.7		µA
$I_{OUTLKG(OVLO)}$	OUT Leakage Current (OVLO condition), V_{OUT} > V_{IN}		319	443	µA
ON RESISTANCE (IN - OUT)					
R_{ON}	V_{IN} = 12 V, I_{OUT} = 3 A, T_J = 25°C		28.2		mΩ
	2.7 ≤ V_{IN} ≤ 23 V, I_{OUT} = 3 A, –40°C ≤ T_J ≤ 125°C			45	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	UVLO Rising threshold	1.183	1.20	1.223	V
$V_{UVLO(F)}$	UVLO Falling threshold	1.076	1.09	1.116	V
$V_{SD(F)}$	EN/UVLO Falling Threshold for lowest shutdown current	0.45	0.74		V
I_{ENLKG}	EN/UVLO leakage current	–0.1		0.1	µA
OVERVOLTAGE LOCKOUT (OVLO) - TPS259470x/4x					
$V_{OV(R)}$	OVLO Rising threshold	1.183	1.20	1.223	V
$V_{OV(F)}$	OVLO Falling threshold	1.076	1.09	1.116	V
I_{OVLKG}	OVLO pin leakage current, 0.5 V < V_{OVLO} < 1.5 V	–0.1		0.1	µA
OUTPUT VOLTAGE CLAMP (OUT) - TPS259472x					
V_{OVC}	Overvoltage Clamp Threshold, OVCSEL = Shorted to GND	3.65	3.88	4.1	V
	Overvoltage Clamp Threshold, OVCSEL = Open	5.25	5.74	6.2	V
	Overvoltage Clamp Threshold, OVCSEL = 390 kΩ to GND	13.2	13.85	14.5	V
V_{CLAMP}	Output Voltage During Clamping, OVCSEL = Shorted to GND, I_{OUT} = 10 mA	3.2	3.82	4.2	V
	Output Voltage During Clamping, OVCSEL = Open, I_{OUT} = 10 mA	5.0	5.68	6.12	V
	Output Voltage During Clamping, OVCSEL = 390 kΩ to GND, I_{OUT} = 10 mA	13.0	13.79	14.6	V
OVERCURRENT PROTECTION (OUT)					
I_{LIM}	Overcurrent Threshold, R_{ILM} = 6.65 kΩ	0.425	0.500	0.575	A
	Overcurrent Threshold, R_{ILM} = 3.32 kΩ	0.850	1.007	1.150	A
	Overcurrent Threshold, R_{ILM} = 1.65 kΩ	1.800	2.028	2.200	A
	Overcurrent Threshold, R_{ILM} = 750 Ω	3.960	4.452	4.840	A
	Overcurrent Threshold, R_{ILM} = 549 Ω	5.400	6.068	6.600	A

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V for TPS259470x/4x, OVCSEL = 390 kΩ to GND for TPS259472x, R_{ILM} = 549 Ω , dVdT = Open, ITIMER = Open, AUXOFF = Open for TPS259470x, $\overline{FLT}$ = Open for TPS259470x, PGTH = Open for TPS259472x/4x, PG = Open for TPS259472x/4x. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
I_{FLT}	Circuit Breaker Threshold, ILM Pin Open (Single point failure)		0.1		A
	Circuit Breaker Threshold, ILM Pin Shorted to GND (Single point failure)		1.1	2.1	A
I_{SCGain}	Scalable Fast Trip Threshold (I_{SC}) : I_{LIM} Ratio		201		%
I_{FT}	Fixed Fast-trip current threshold		22.2		A
V_{FB}	V_{OUT} threshold to exit Current Limit Foldback		1.9		V
OVERCURRENT FAULT TIMER (ITIMER)					
V_{INT}	ITIMER pin internal pull-up voltage	2.3	2.57	2.72	V
R_{ITIMER}	ITIMER pin internal pull-up resistance		15		kΩ
I_{ITIMER}	ITIMER pin internal discharge current, I_{OUT} > I_{LIM}	1.2	1.8	2.5	µA
ΔV_{ITIMER}	ITIMER discharge differential voltage threshold	1.286	1.51	1.741	V
OUTPUT LOAD CURRENT MONITOR (ILM)					
G_{IMON}	Analog Load Current Monitor Gain (I_{MON} : I_{OUT}), I_{OUT} = 0.5 A to 1 A, I_{OUT} < I_{LIM}	165	182	200	µA/A
	Analog Load Current Monitor Gain (I_{MON} : I_{OUT}), I_{OUT} = 1 A to 5.5 A, I_{OUT} < I_{LIM}	165	182	200	µA/A
REVERSE CURRENT BLOCKING (IN - OUT)					
V_{FWD}	V_{IN} – V_{OUT} Forward regulation voltage, I_{OUT} = 10 mA	4.7	16.9		mV
V_{REVTH}	V_{IN} – V_{OUT} threshold for fast BFET turn off (enter reverse current blocking)	–36.45	–29.3	–22.3	mV
V_{FWDTH}	V_{IN} – V_{OUT} threshold for fast BFET turn on (exit reverse current blocking)	83	104.1	125	mV
$I_{REVLKG(OFF)}$	OUT Leakage Current during unpowered condition (V_{OUT} = 12 V, V_{IN} = 0 V)		4.86		µA
I_{REVLKG}	Reverse leakage current, (V_{OUT} – V_{IN}) = 21.5 V		10.1		µA
$I_{OUTLKG(RCB)}$	OUT Leakage Current during ON state with RCB, V_{OUT} = V_{IN} + 1 V		234		µA
POWER GOOD INDICATION (PG) - TPS259472x/4x or AUXILIARY CHANNEL CONTROL (AUXOFF) - TPS259470x					
V_{PGD}	PG/AUXOFF pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Weak pull-up (I_{PG} = 26 µA)		0.67	1	V
	PG/AUXOFF pin voltage while de-asserted, V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Strong pull-up (I_{PG} = 242 µA)		0.79	1	V
	PG/AUXOFF pin voltage while de-asserted, V_{IN} > $V_{UVP(R)}$		0		V
I_{PGLKG}	PG/AUXOFF Pin leakage current, PG/AUXOFF asserted		0.9	3	µA
POWERGOOD THRESHOLD (PGTH) - TPS259472x/4x					
$V_{PGTH(R)}$	PGTH Rising threshold	1.183	1.20	1.223	V
$V_{PGTH(F)}$	PGTH Falling threshold	1.076	1.09	1.116	V
$I_{PGTHLKG}$	PGTH leakage current	–0.1		0.3	µA
FAULT INDICATION ($\overline{FLT}$) - TPS259470x					
I_{FLTLKG}	$\overline{FLT}$ leakage current	–1		1	µA
R_{FLT}	$\overline{FLT}$ Internal Pull down resistance		12.3		Ω
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown Rising Threshold, T_J↑		154		°C

7.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V for TPS259470x/4x, OVCSEL = 390 kΩ to GND for TPS259472x, R_{ILM} = 549 Ω , dVdT = Open, ITIMER = Open, AUXOFF = Open for TPS259470x, $\overline{FLT}$ = Open for TPS259470x, PGTH = Open for TPS259472x/4x, PG = Open for TPS259472x/4x. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
TSD_{HYS}	Thermal Shutdown Hysteresis, T_J↓		10		°C
DVDT					
I_{dVdt}	dVdt Pin Charging Current	0.81	2.21	3.82	µA

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time (TPS259470x/4x)	V_{OVLO} > $V_{OV(R)}$ to V_{OUT}↓		1.2		µs
t_{OVC}	Overvoltage clamp response time (TPS259472x)	V_{IN} > V_{OVC} to V_{OUT}↓		5		µs
t_{CB}	Circuit-Breaker response time (TPS259474x)	I_{OUT} > 1.2 × I_{LIM} & ITIMER expired to I_{OUT}↓		2		µs
t_{LIM}	Current limit response time (TPS259470x/2x)	I_{OUT} > 1.2 × I_{LIM} & ITIMER expired to I_{OUT} settling to within 5 % of I_{LIM}		400		µs
t_{SC}	Scalable fast-trip response time	I_{OUT} > 3 × I_{LIM} to I_{OUT}↓		500		ns
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT}↓		500		ns
t_{RST}	Auto-Retry Interval after fault (TPS25947xA)			110		ms
t_{SWOV}	OVLO fast recovery response time (TPS259470x)	V_{OVLO} < $V_{OV(F)}$ to V_{OUT}↑		90		µs
t_{SWRCB}	Reverse Current Blocking recovery time	(V_{IN} – V_{OUT}) > V_{FWDTH} to V_{OUT} ↑		50		µs
t_{RCB}	Reverse Current Blocking comparator response time	(V_{OUT} – V_{IN}) > 1.3 × V_{REVTH} to BFET OFF		1		µs
t_{PGA}	PG Assertion de-glitch (TPS259472x/4x)			12		µs
t_{PGD}	PG De-assertion de-glitch (TPS259472x/4x)			12		µs

7.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it will slow the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady state condition and the load voltage is completely discharged before the device is enabled.Typical Values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNIT
SR_{ON}	Output Rising slew rate	2.7 V	12.14	0.87	0.5	V/ms
		12 V	28.1	1.09	0.61	
		23 V	44.78	1.25	0.71	
$t_{D,ON}$	Turn on delay	2.7 V	0.09	0.6	0.97	ms
		12 V	0.1	1.32	2.35	
		23 V	0.11	1.99	3.69	
t_R	Rise time	2.7 V	0.17	2.51	4.33	ms
		12 V	0.35	8.1	15.37	
		23 V	0.40	14.4	25.89	
t_{ON}	Turn on time	2.7 V	0.27	3.11	5.31	ms
		12 V	0.45	10.08	17.72	
		23 V	0.50	16.41	29.57	
$t_{D,OFF}$	Turn off delay	2.7 V	64.44	64.44	64.44	µs
		12 V	25.32	25.32	25.32	
		23 V	23.02	23.02	23.02	

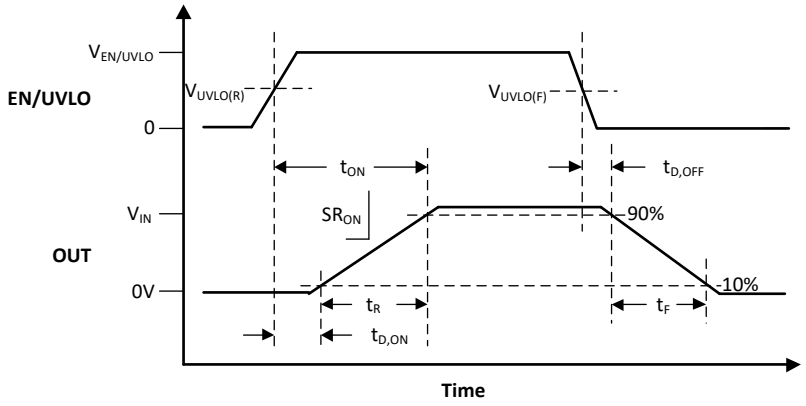


Figure 7-1. TPS25947xx Switching Times

7.8 Typical Characteristics

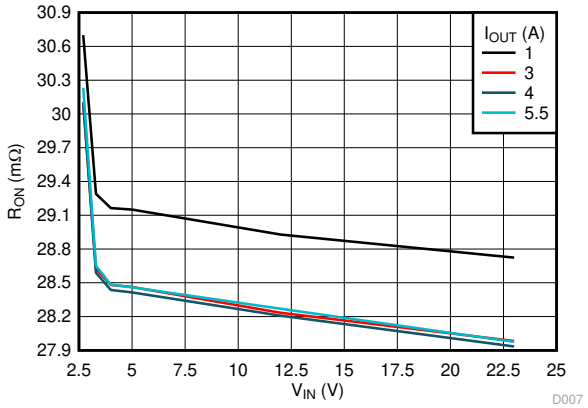


Figure 7-2. ON-Resistance vs Supply Voltage

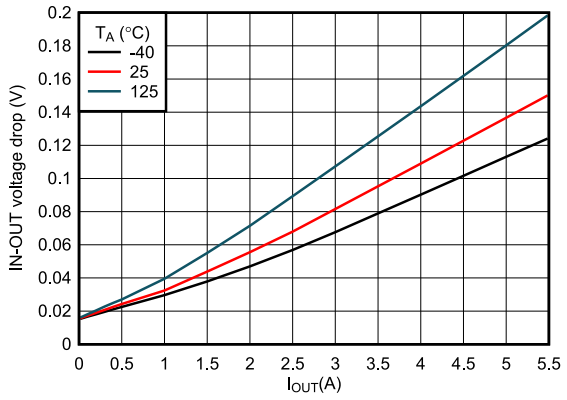


Figure 7-3. Forward Voltage Drop vs Load Current

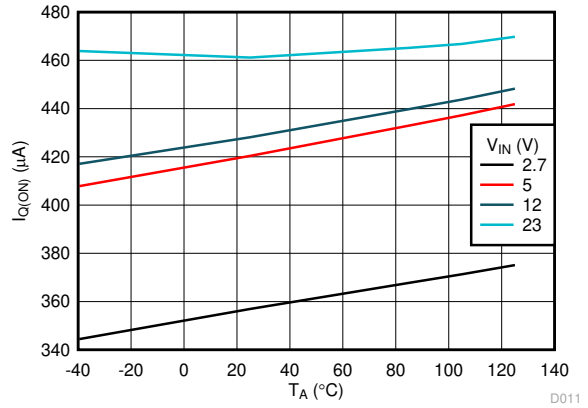


Figure 7-4. IN Quiescent Current vs Temperature (TPS259470x, TPS2594704x Variants)

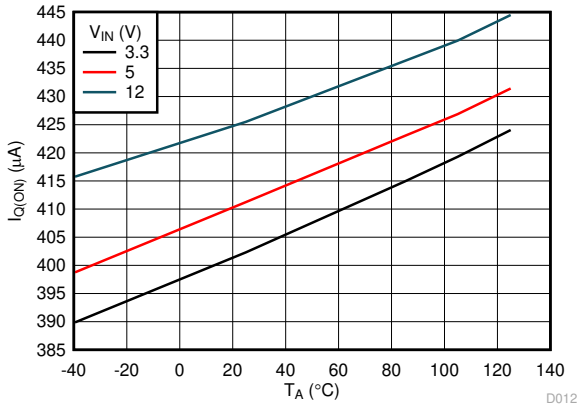


Figure 7-5. IN Quiescent Current vs Temperature (TPS259472x Variant)

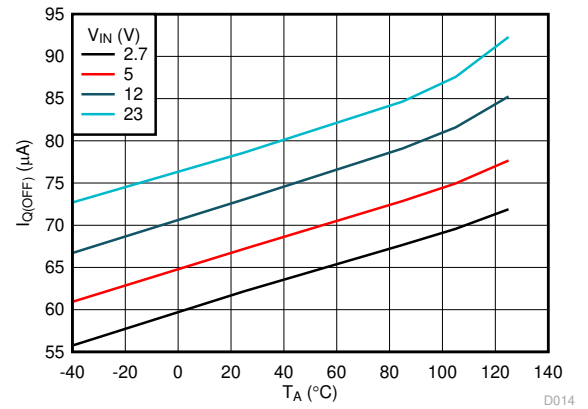


Figure 7-6. IN OFF State (UVLO) Current vs Temperature

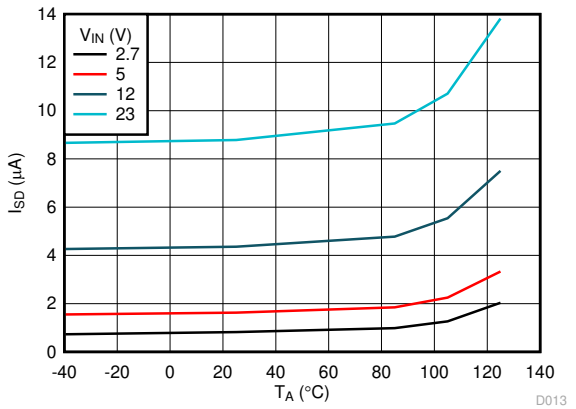


Figure 7-7. IN Shutdown Current vs Temperature

7.8 Typical Characteristics (continued)

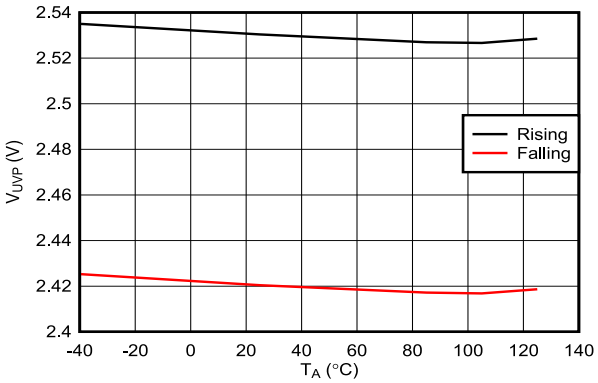


Figure 7-8. IN Undervoltage Threshold vs Temperature

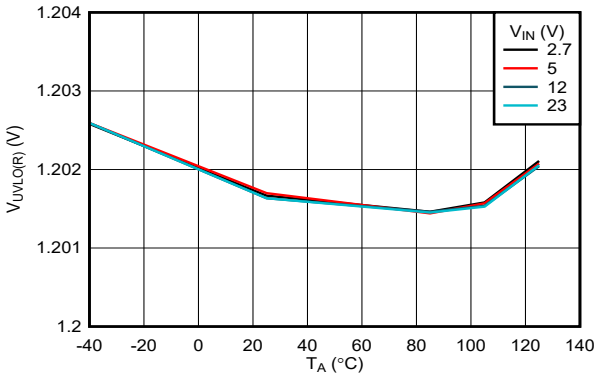


Figure 7-9. EN/UVLO Rising Threshold vs Temperature

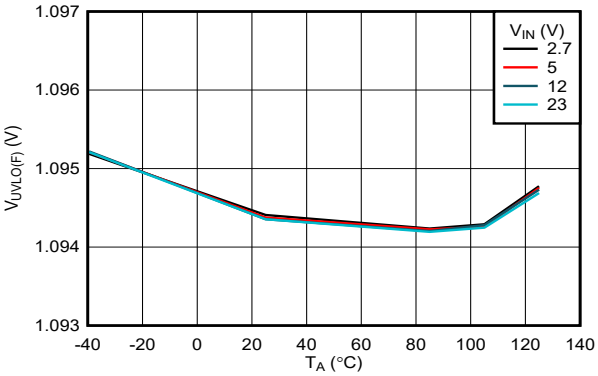


Figure 7-10. EN/UVLO Falling Threshold vs Temperature

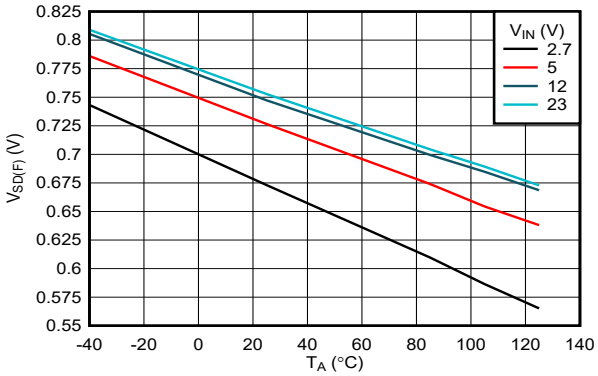


Figure 7-11. EN/UVLO Shutdown Falling Threshold vs Temperature

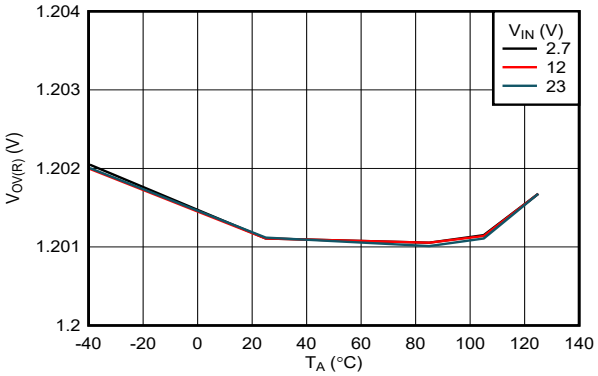


Figure 7-12. OVLO Rising Threshold vs Temperature

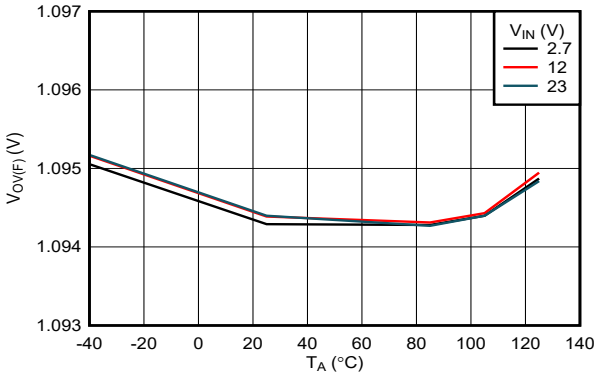


Figure 7-13. OVLO Falling Threshold vs Temperature

7.8 Typical Characteristics (continued)

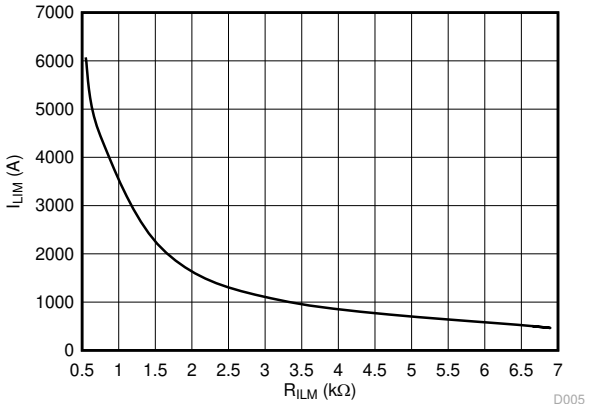


Figure 7-14. Overcurrent Threshold vs ILM Resistor

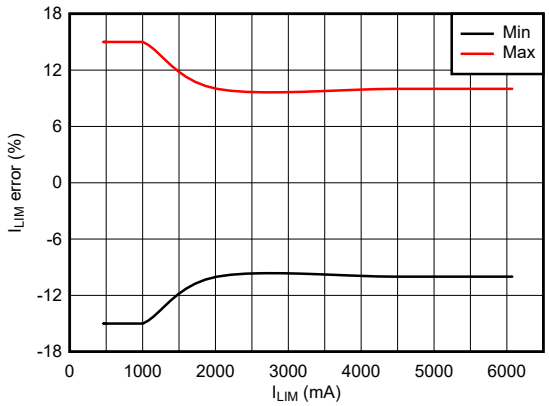


Figure 7-15. Overcurrent Threshold Accuracy (Across Process, Voltage and Temperature)

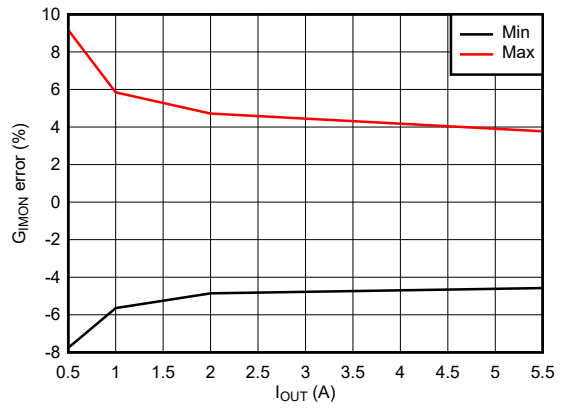


Figure 7-16. Analog Current Monitor Gain Accuracy

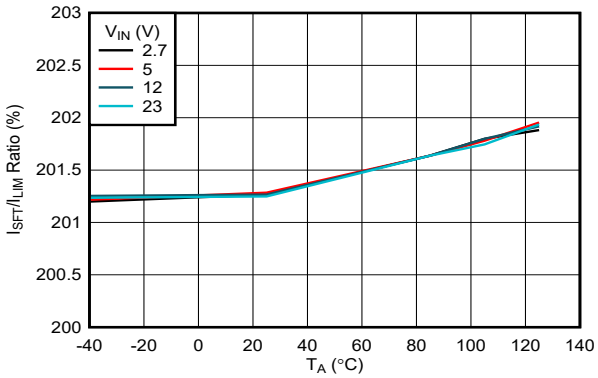


Figure 7-17. Scalable Fast-Trip Threshold: Current Limit Threshold (I_{LIM}) Ratio vs Temperature

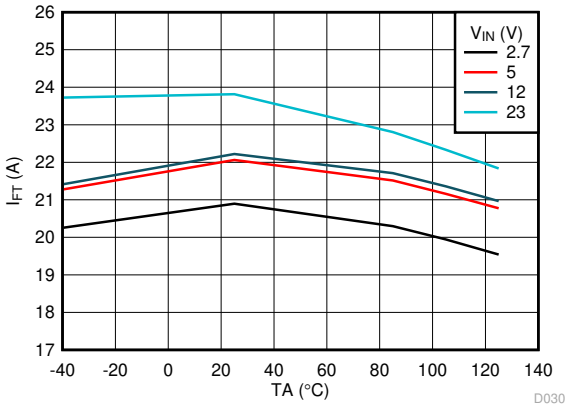


Figure 7-18. Steady State Fixed Fast-Trip Current Threshold vs Temperature

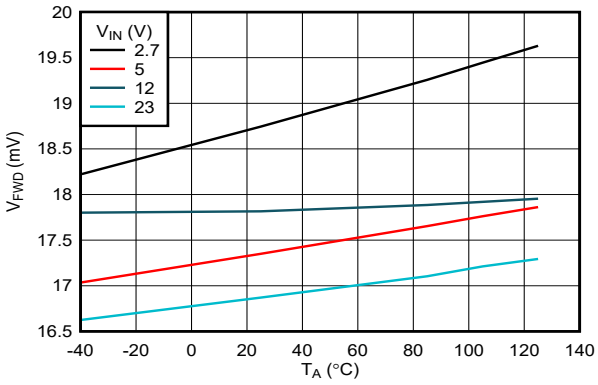


Figure 7-19. RCB - Forward Regulation Voltage vs Temperature

7.8 Typical Characteristics (continued)

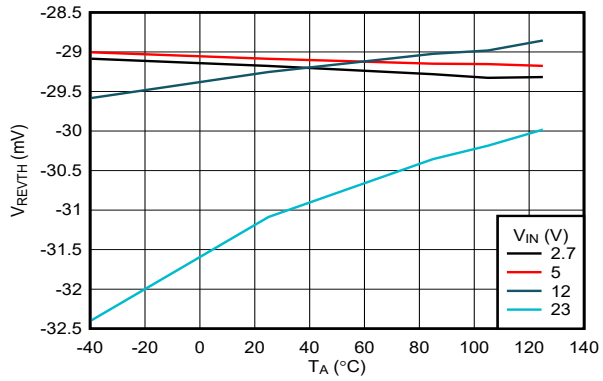


Figure 7-20. RCB - Reverse Comparator Threshold vs Temperature

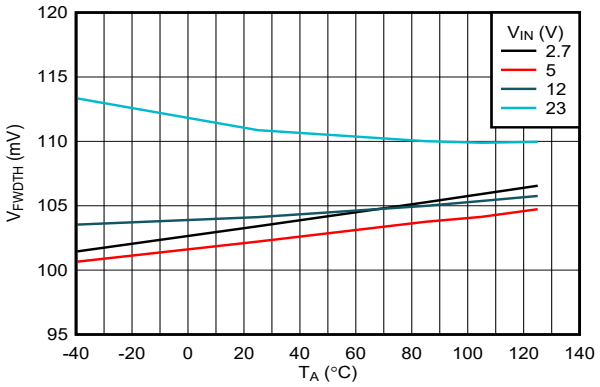


Figure 7-21. RCB - Forward Comparator Threshold vs Temperature

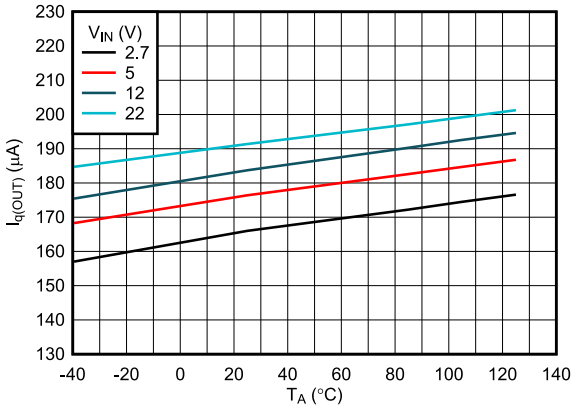


Figure 7-22. OUT Leakage Current During ON-State Reverse Current Blocking

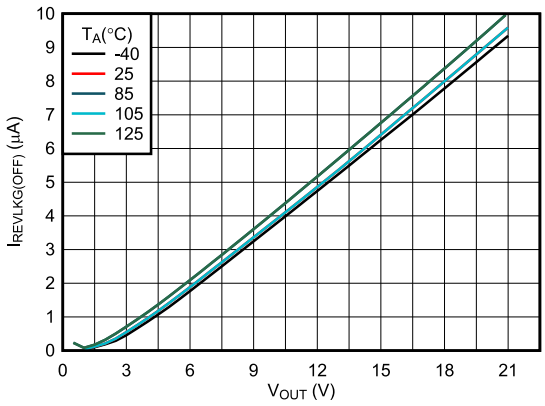


Figure 7-23. Reverse Leakage Current During OFF-State

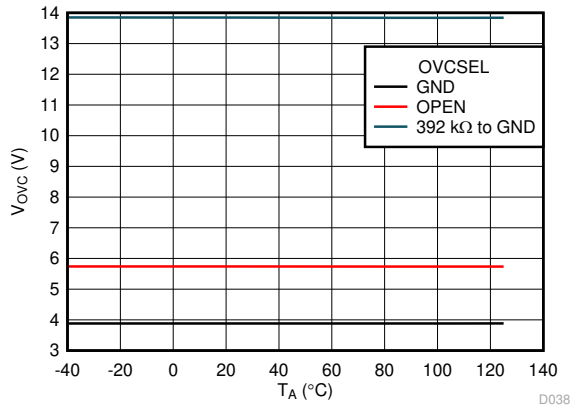


Figure 7-24. OVC Threshold vs Temperature

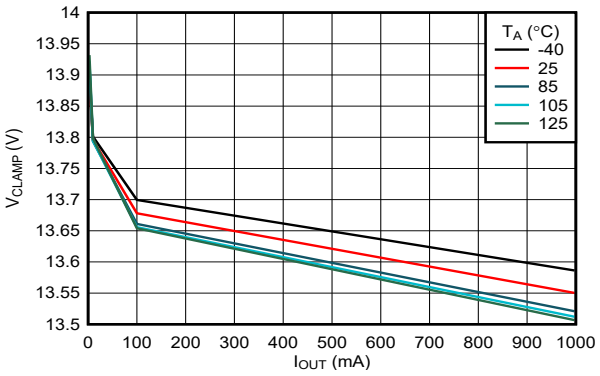


Figure 7-25. OVC Clamping Voltage (OVCSEL = 392 kΩ to GND) vs Load Current

7.8 Typical Characteristics (continued)

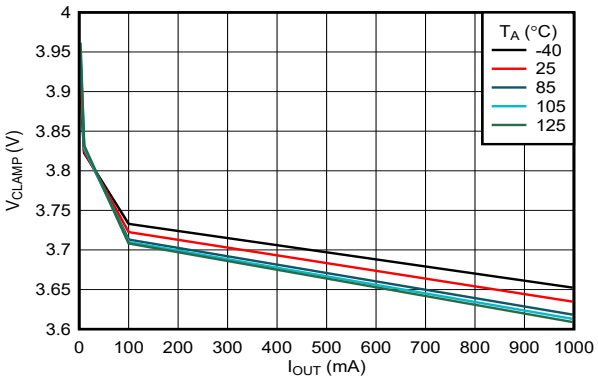


Figure 7-26. OVC Clamping Voltage (OVCSEL = GND) vs Load Current

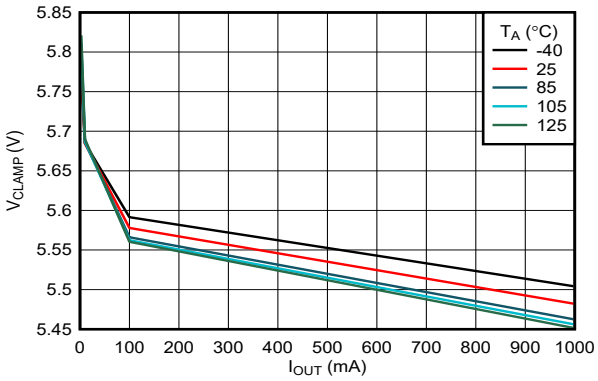


Figure 7-27. OVC Clamping Voltage (OVCSEL = Open) vs Load Current

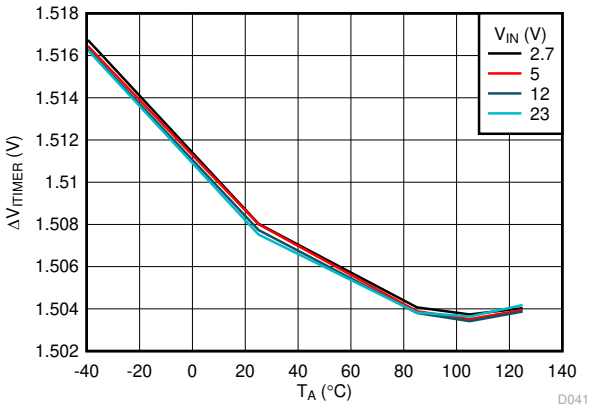


Figure 7-28. ITIMER Discharge Differential Voltage Threshold vs Temperature

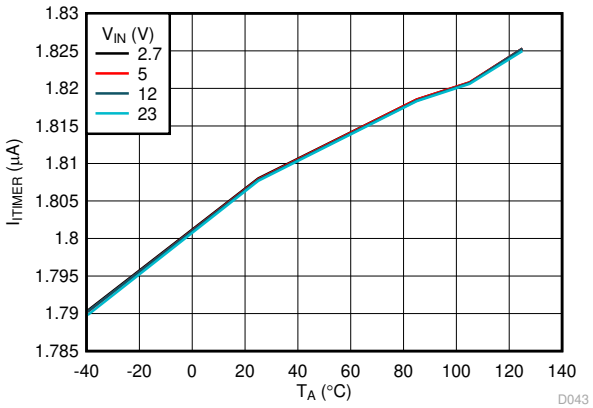


Figure 7-29. ITIMER Discharge Current vs Temperature

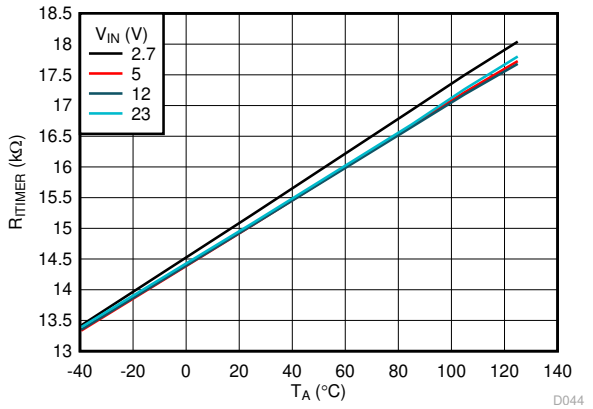


Figure 7-30. ITIMER Internal Pullup Resistance vs Temperature

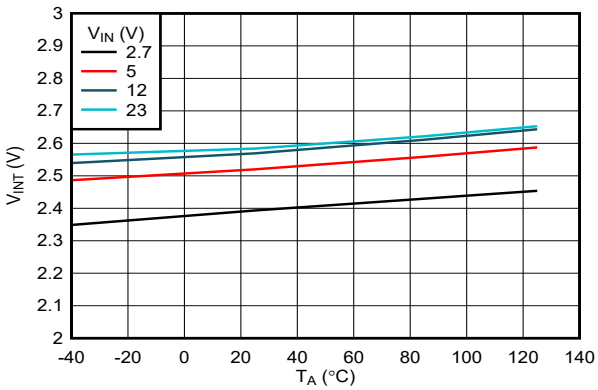


Figure 7-31. ITIMER Internal Pullup Voltage vs Temperature

7.8 Typical Characteristics (continued)

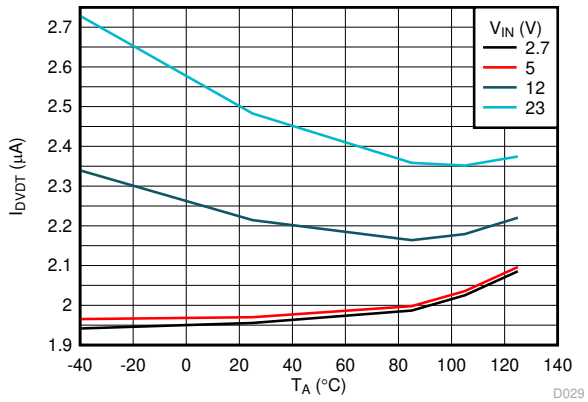


Figure 7-32. DVDT Charging Current vs Temperature

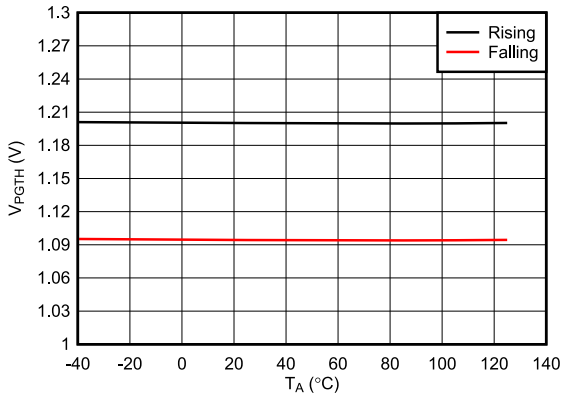


Figure 7-33. PGTH Threshold vs Temperature

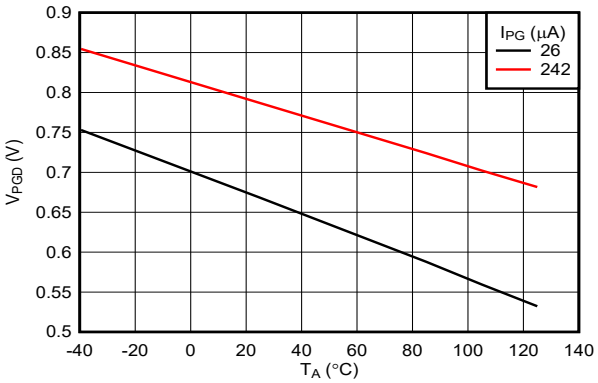


Figure 7-34. PG Low Voltage Without Input Supply vs Temperature

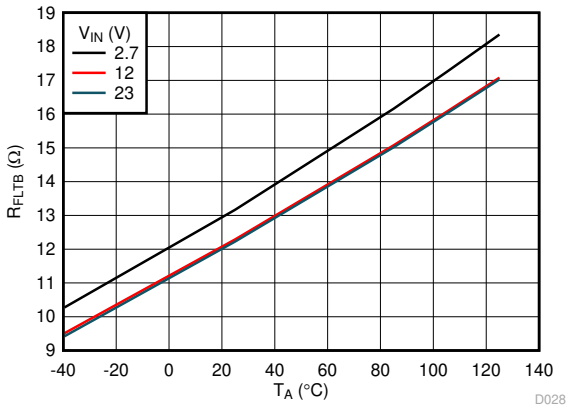


Figure 7-35. FLTb Pin Pulldown Resistance vs Temperature

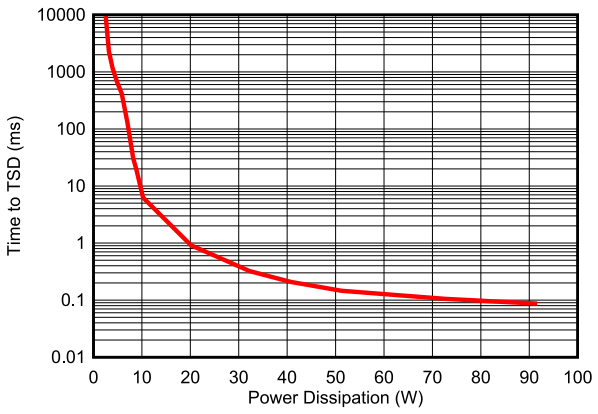


Figure 7-36. Time to Thermal Shut-Down During Inrush State

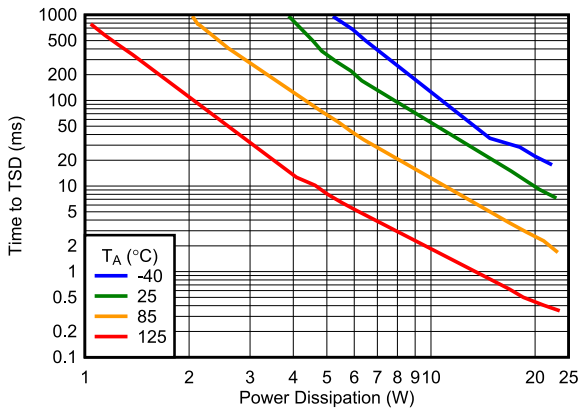
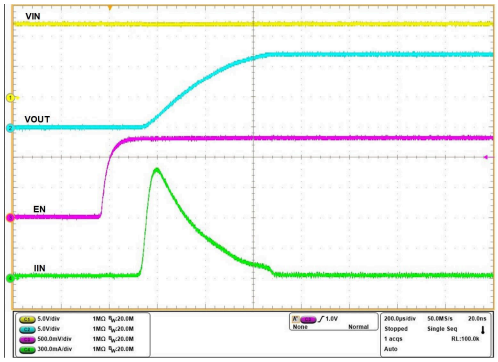


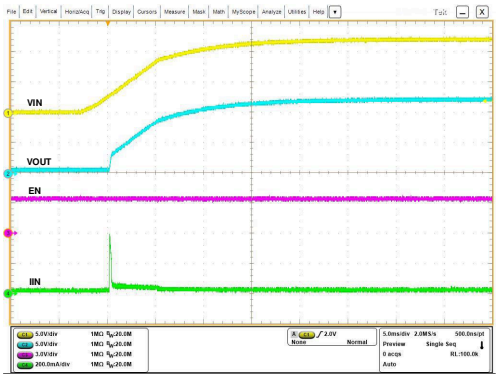
Figure 7-37. Time to Thermal Shut-Down During Steady State

7.8 Typical Characteristics (continued)



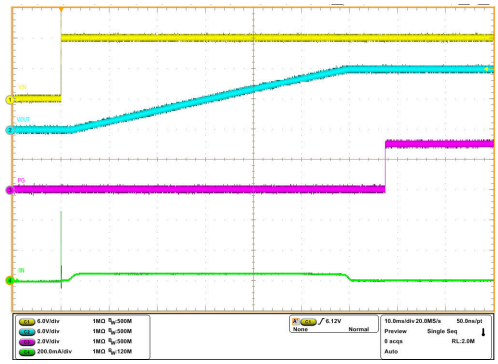
V_{IN} = 12 V, C_{OUT} = 30 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 1.4 V

Figure 7-38. Start-Up with Enable



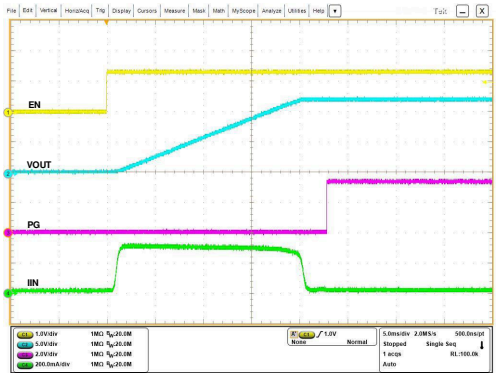
$V_{EN/UVLO}$ = 3.3 V, C_{OUT} = 30 µF, C_{dVdt} = Open, V_{IN} ramped up to 12 V

Figure 7-39. Start-Up with Supply



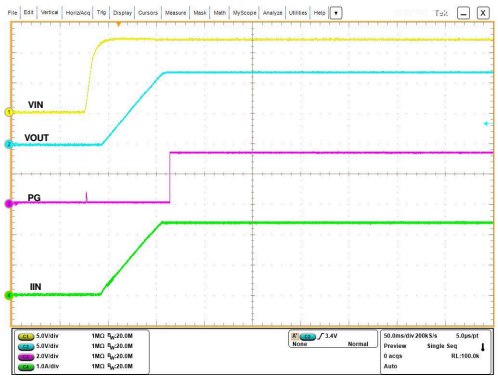
C_{OUT} = 220 µF, C_{dVdt} = 10 nF, EN/UVLO connected to IN through resistor ladder, 12 V hot-plugged to IN

Figure 7-40. Input Hot-Plug



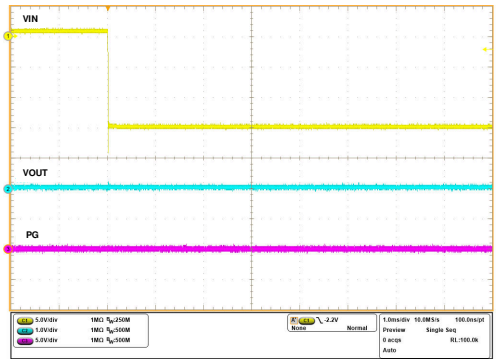
V_{IN} = 12 V, C_{OUT} = 470 µF, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

Figure 7-41. Inrush Current with Capacitive Load



V_{IN} = 12 V, C_{OUT} = 470 µF, R_{OUT} = 5 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

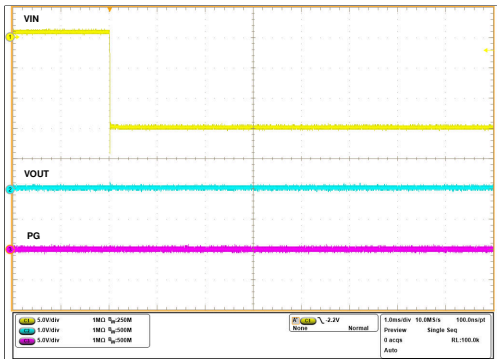
Figure 7-42. Inrush Current with Resistive and Capacitive Load



C_{OUT} = 220 µF, PG pulled up to 3 V, -15 V hot-plugged to IN

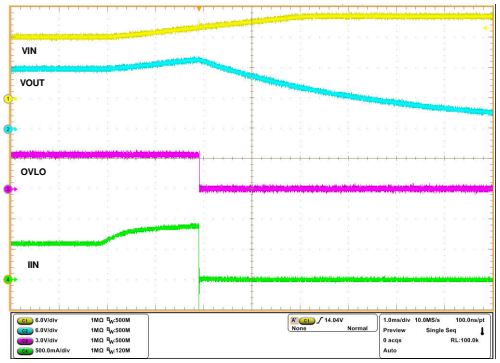
Figure 7-43. Input Reverse Polarity Protection - Fast Ramp

7.8 Typical Characteristics (continued)



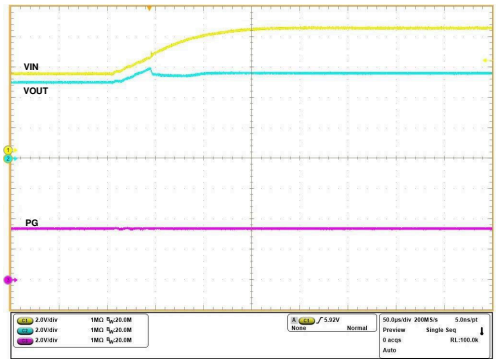
C_{OUT} = 220 µF, PG pulled up to 3 V, V_{IN} ramped down from 0 V to -15 V and then ramped up to 0 V

Figure 7-44. Input Reverse Polarity Protection - Slow Ramp



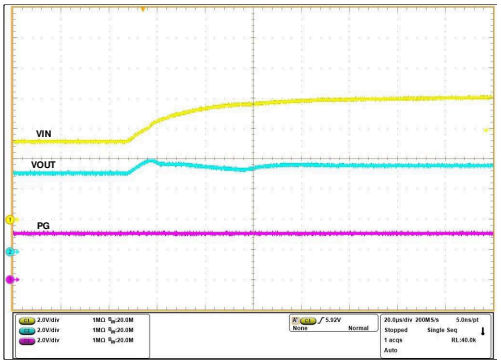
C_{OUT} = 220 µF, R_{OUT} = 20 Ω, V_{IN} Overvoltage threshold set to 13.2 V, V_{IN} ramped up from 12 V to 16 V

Figure 7-45. Overvoltage Lockout Response - TPS259470x/4x



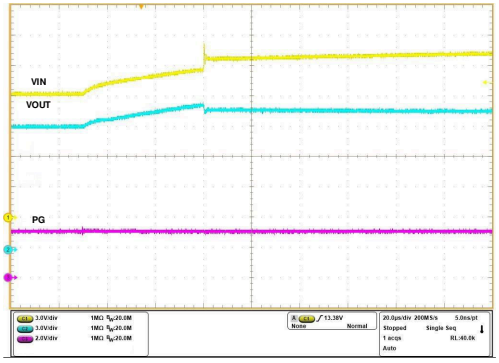
R_{OVCSEL} = GND, C_{OUT} = 220 µF, I_{OUT} = 120 mA, V_{IN} ramped up from 3.3 V to 6 V

Figure 7-46. Overvoltage Clamp Response - TPS259472x



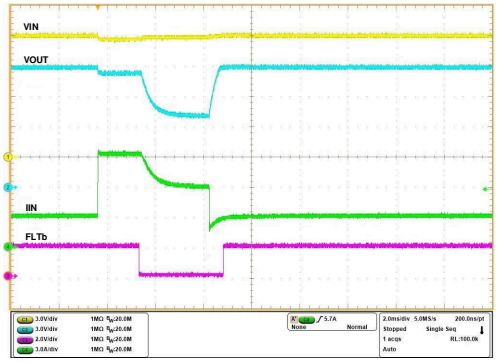
R_{OVCSEL} = Open, C_{OUT} = 220 µF, I_{OUT} = 150 mA, V_{IN} ramped up from 5 V to 8 V

Figure 7-47. Overvoltage Clamp Response - TPS259472x



R_{OVCSEL} = 390 kΩ, C_{OUT} = 220 µF, I_{OUT} = 300 mA, V_{IN} ramped up from 12 V to 16.5 V

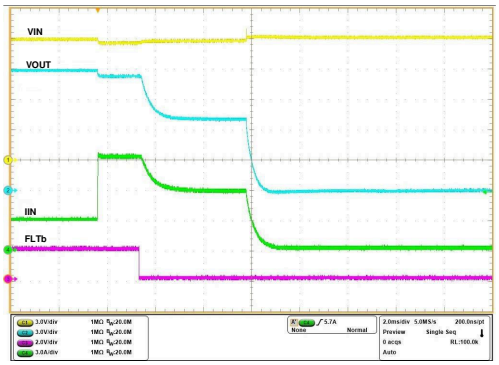
Figure 7-48. Overvoltage Clamp Response - TPS259472x



V_{IN} = 12 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 220 µF, R_{ILM} = 549 Ω, I_{OUT} stepped from 3 A → 9 A → 3 A within 5 ms

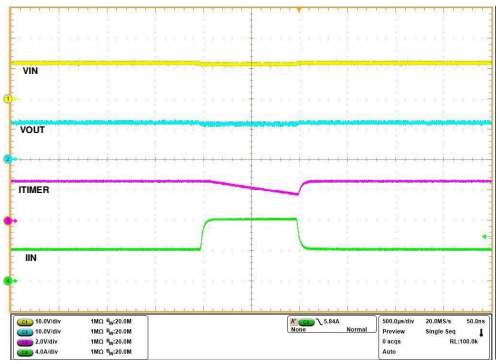
Figure 7-49. Active Current Limit Response - TPS259470x

7.8 Typical Characteristics (continued)



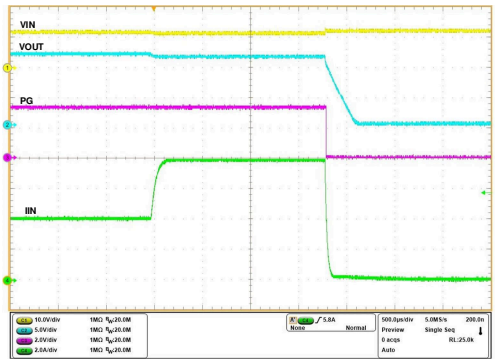
V_{IN} = 12 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 220 µF, R_{ILM} = 549 Ω, I_{OUT} stepped from 3 A → 9 A

Figure 7-50. Active Current Limit Response Followed by TSD - TPS259470x



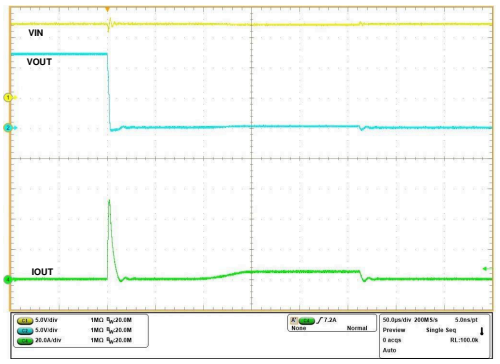
V_{IN} = 12 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 470 µF, R_{ILM} = 549 Ω, I_{OUT} ramped from 4 A → 8 A→ 4 A within 1 ms

Figure 7-51. Transient Overcurrent Blanking Timer Response - TPS259474x



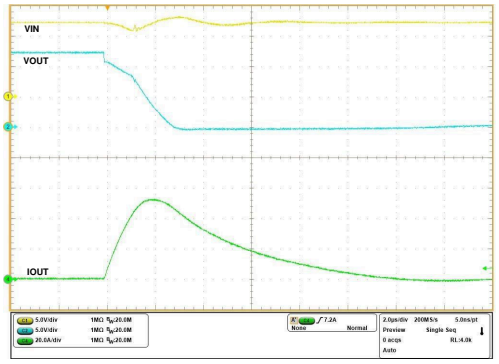
V_{IN} = 12 V, C_{ITIMER} = 2.2 nF, C_{OUT} = 470 µF, R_{ILM} = 549 Ω, I_{OUT} ramped from 4 A → 8 A

Figure 7-52. Circuit Breaker Response - TPS259474x



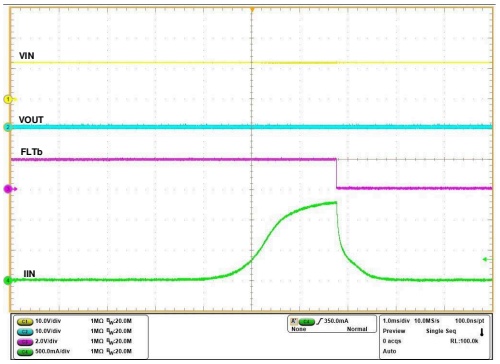
V_{IN} = 12 V, R_{ILM} = 549 Ω, $V_{EN/UVLO}$ = 3.3 V, OUT stepped from Open → Short-circuit to GND

Figure 7-53. Output Short-Circuit During Steady State



V_{IN} = 12 V, R_{ILM} = 549 Ω, $V_{EN/UVLO}$ = 3.3 V, OUT stepped from Open → Short-circuit to GND

Figure 7-54. Output Short-Circuit During Steady State (Zoomed In)



V_{IN} = 12 V, C_{OUT} = Open, OUT short-circuit to GND, R_{ILM} = 1650 Ω, $V_{EN/UVLO}$ stepped from 0 V to 3.3 V

Figure 7-55. Power Up into Short-Circuit

8 Detailed Description

8.1 Overview

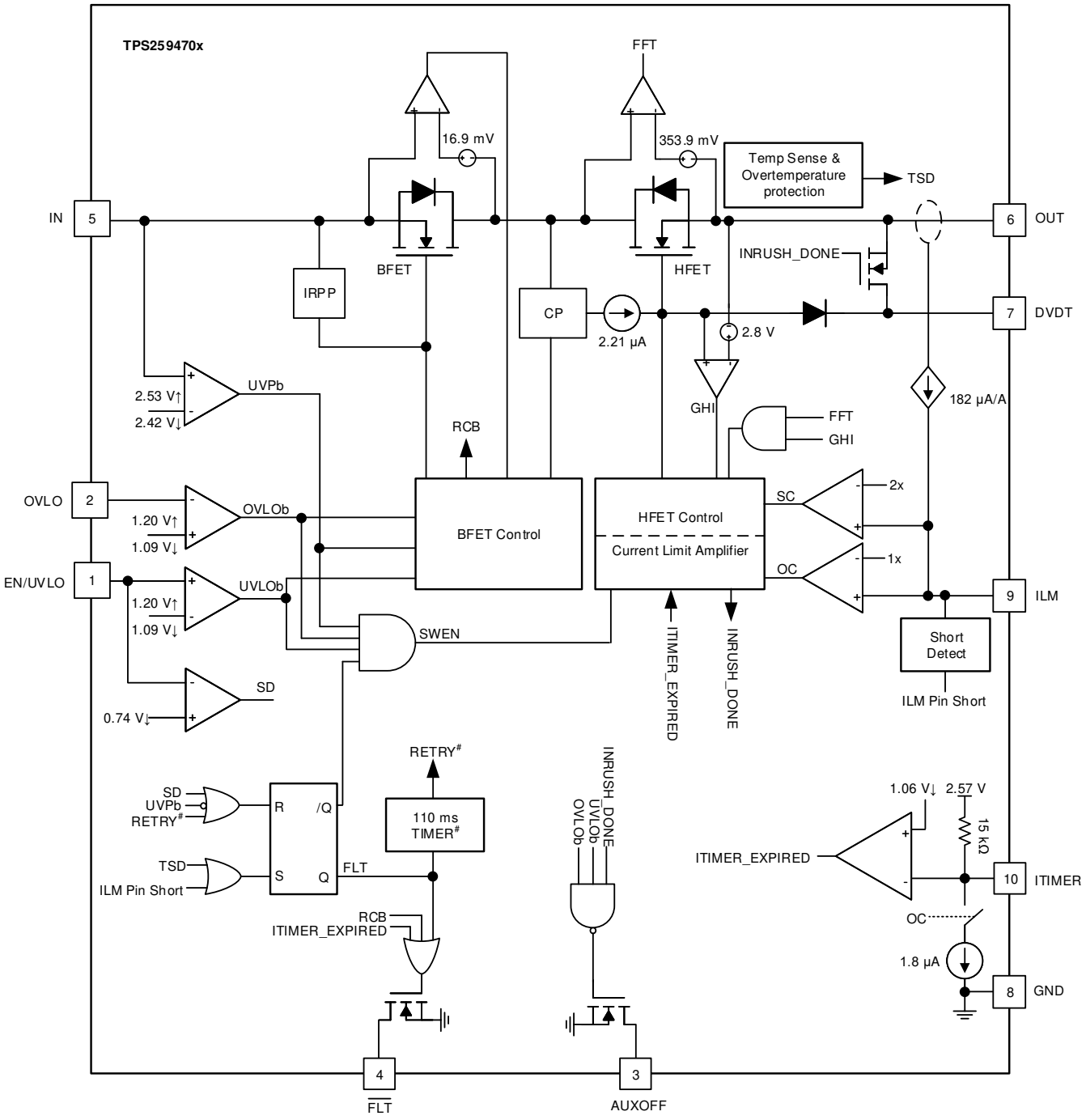
The TPS25947xx is an eFuse with integrated power path that is used to ensure safe power delivery in a system. The device starts its operation by monitoring the IN bus. When the input supply voltage (VIN) exceeds the Undervoltage Protection threshold (VUVP), the device samples the EN/UVLO pin. A high level (> VUVLO) on this pin enables the internal power path (BFET+HFET) to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low (< VUVLO), the internal power path is turned off. In case of reverse voltages appearing at the input, the power path remains OFF thereby protecting the output load.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, and controls the internal HFET to ensure that the user adjustable overcurrent limit threshold (I_{LIM}) is not exceeded and overvoltage spikes are either safely clamped to the selected threshold voltage (V_{OVC}) or cut-off after they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). The device also provides fast protection against severe overcurrent during short-circuit events. This keeps the system safe from harmful levels of voltage and current. At the same time, a user adjustable overcurrent blanking timer allows the system to pass moderate transient peaks in the load current profile without tripping the eFuse. This ensures a robust protection solution against real faults which is also immune to transients, thereby ensuring maximum system uptime.

The device has integrated reverse current blocking FET (BFET) which operates like an ideal diode. The BFET is linearly regulated to maintain a small constant forward drop (V_{FWD}) in forward conduction mode and turned off completely to block reverse current if output voltage exceeds the input voltage.

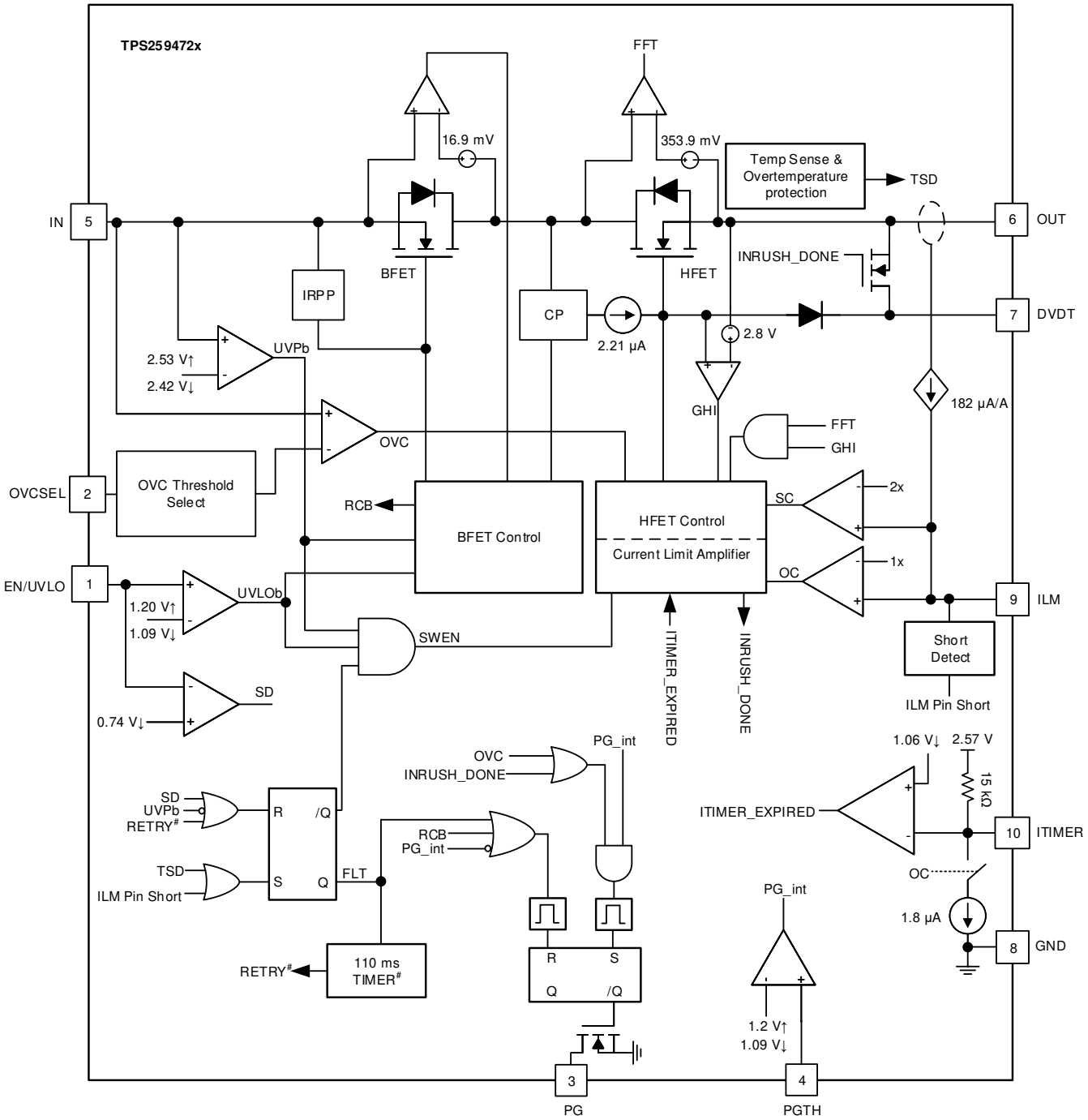
The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

8.2 Functional Block Diagram



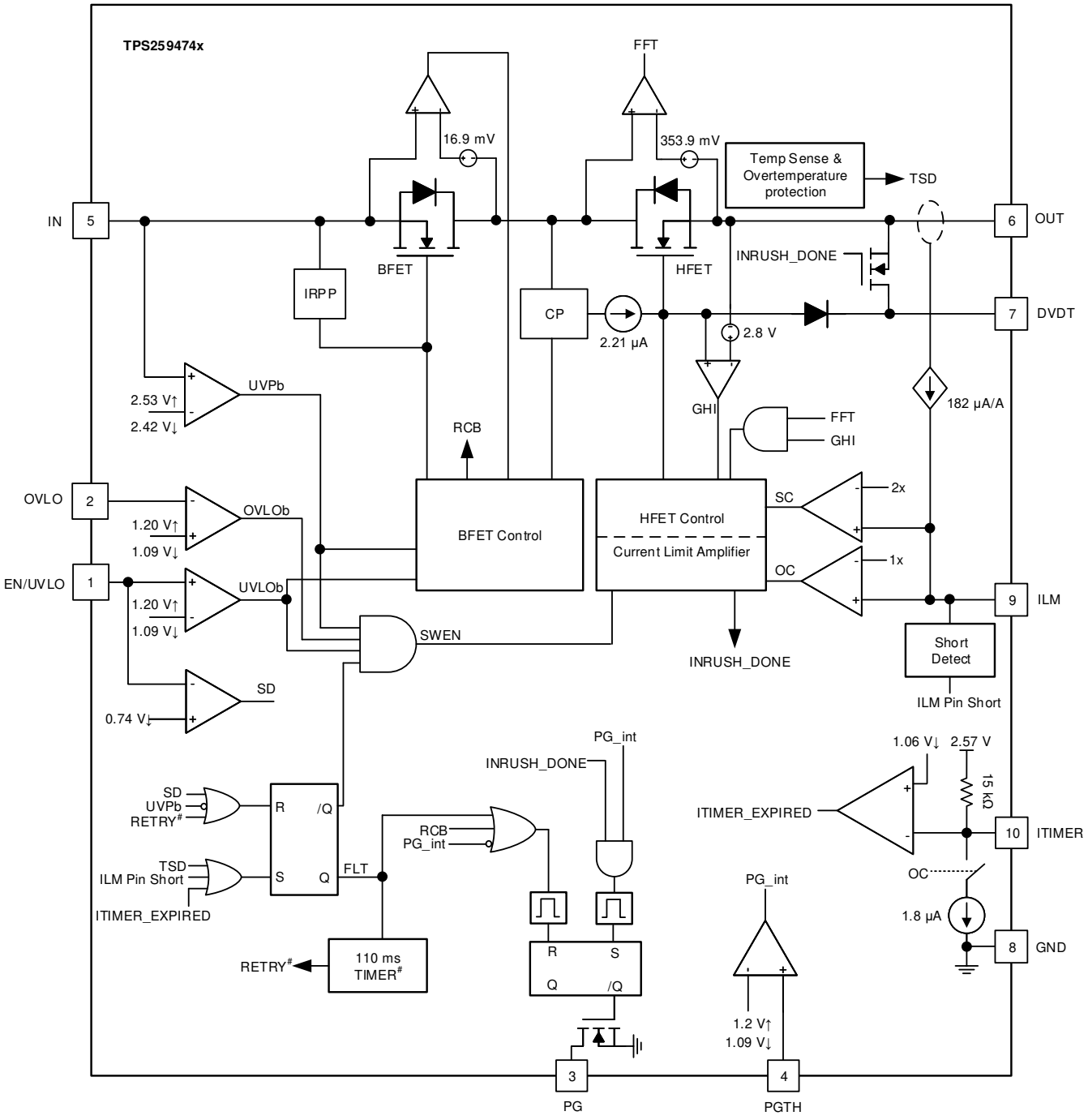
Not applicable to Latch-off variants (TPS259470L)

Figure 8-1. TPS259470x Block Diagram



Not applicable to Latch-off variants (TPS259472L)

Figure 8-2. TPS259472x Block Diagram



Not applicable to Latch-off variants (TPS259474L)

Figure 8-3. TPS259474x Block Diagram

8.3 Feature Description

The TPS25947xx eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

8.3.1 Input Reverse Polarity Protection

The TPS25947xx device is internally protected against steady state negative voltages applied at the input supply pin. The device blocks the negative voltage from appearing at the output, thereby protecting the load circuits. There's no reverse current flowing from output to the input in this condition. The lowest negative voltage the device can handle at the input is limited to -15 V or V_{OUT} – 21 V, whichever is higher. It's also recommended that all signal pins (e.g. EN/UVLO, OVLO, PGTH) which are connected to input supply must have a sufficiently large pull-up resistor to limit the current flowing out of these pins during reverse polarity conditions. Please refer to *Absolute Maximum Ratings* table for more details.

8.3.2 Undervoltage Lockout (UVLO and UVP)

The TPS25947xx implements Undervoltage Protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The Undervoltage Protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the Undervoltage Protection threshold to be externally adjusted to a user defined value. The Figure 8-4 and Equation 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

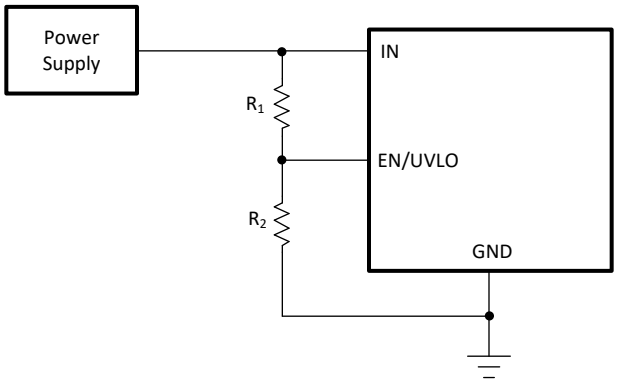


Figure 8-4. Adjustable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO} \times (R1 + R2)}{R2} \quad (1)$$

8.3.3 Overvoltage Lockout (OVLO)

The TPS259470x/4x variants allow the user to implement Overvoltage Lockout to protect the load from input overvoltage conditions. The OVLO comparator on the OVLO pin allows the Overvoltage Protection threshold to be adjusted to a user defined value. After the voltage at the OVLO pin crosses the OVLO rising threshold $V_{OV(R)}$, the device turns off the power to the output. Thereafter, the devices wait for the voltage at the OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the output power is turned ON again. The rising and falling thresholds are slightly different to provide hysterisis. The Figure 8-5 and Equation 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.

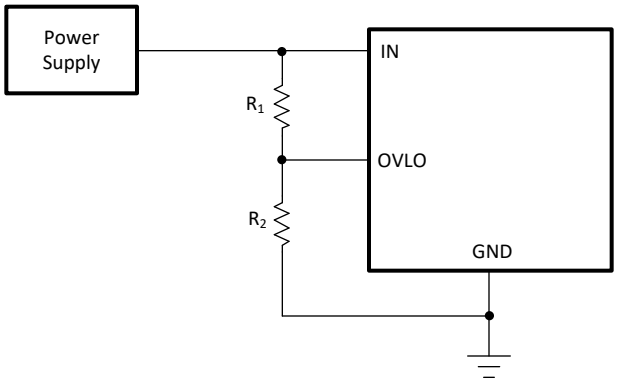


Figure 8-5. Adjustable Overvoltage Protection

$$V_{IN(OV)} = \frac{V_{OV} \times (R1 + R2)}{R2} \quad (2)$$

While recovering from a OVLO event, the TPS259470x variants bypass the inrush control (dVdt) and start up in a current limited manner to provide faster turn ON and minimize power supply droop.

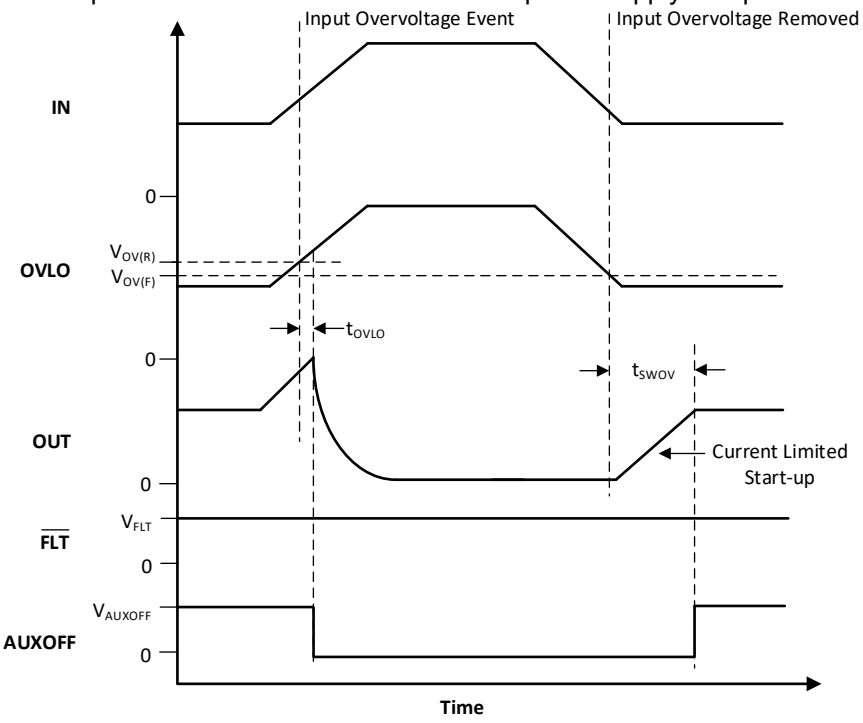


Figure 8-6. TPS259470x Overvoltage Lockout and Recovery

While recovering from a OVLO event, the TPS259474x variants start up with inrush control (dVdt).

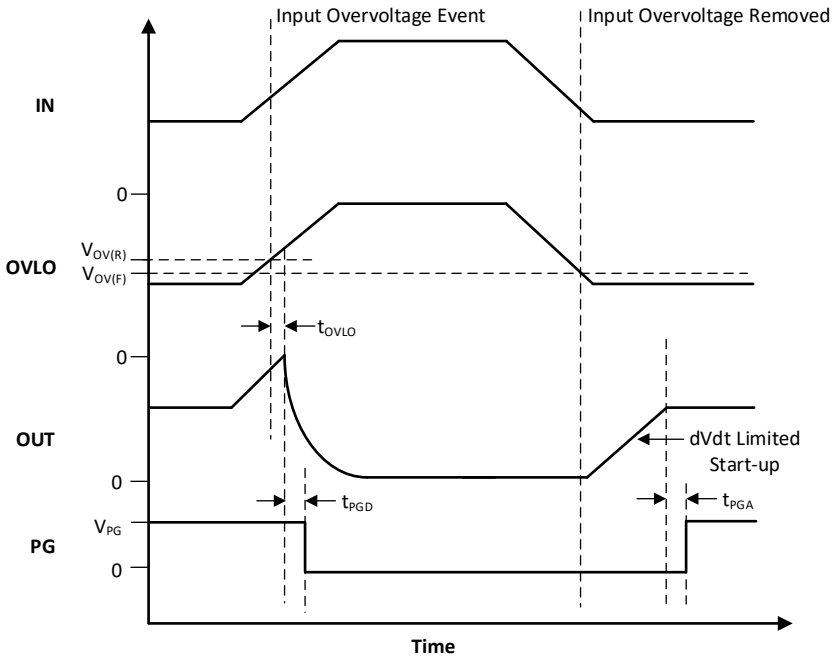
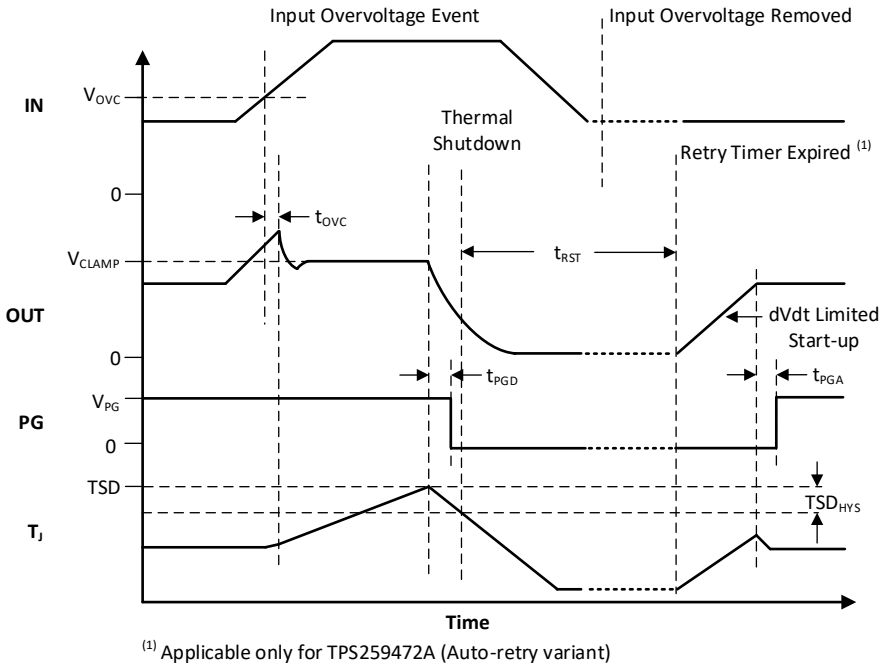


Figure 8-7. TPS259474x Overvoltage Lockout and Recovery

8.3.4 Overvoltage Clamp (OVC)

The TPS259472x variants implement a voltage clamp on the output to protect the system in the event of input overvoltage. When the device detects the input has exceeded the Overvoltage Clamp Threshold (V_{OVC}), it quickly responds within t_{OVC} and stops the output from rising further and then regulates the HFET linearly to clamp the output voltage below V_{CLAMP} as long as an overvoltage condition is present on the input.

If the part stays in clamping state for an extended period of time, there is a higher power dissipation inside the part which can eventually lead to thermal shut-down (TSD). After the part shuts down due to TSD fault, it can either stay latched off (TPS259472L variant) or restart automatically after a fixed delay (TPS259472A variant). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.



(1) Applicable only for TPS259472A (Auto-retry variant)

Figure 8-8. TPS259472x Overvoltage Response (Auto-Retry)

There are 3 available overvoltage clamp threshold options which can be configured using the OVCSEL pin.

Table 8-1. TPS259472x Overvoltage Clamp Threshold Selection

OVCSEL Pin Connection	Overvoltage Clamp Threshold
Shorted to GND	3.8 V
Open	5.7 V
Connected to GND through a 390-kΩ resistor	13.8 V

8.3.5 Inrush Current, Overcurrent, and Short Circuit Protection

TPS25947xx incorporates four levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Adjustable threshold (I_{LIM}) for overcurrent protection during start-up or steady-state
3. Adjustable threshold (I_{SC}) for fast-trip response to severe overcurrent during start-up or steady-state
4. Fixed threshold (I_{FT}) for fast-trip response to quickly protect against hard output short-circuits during steady-state

8.3.5.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and/or cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn-on is directly proportional to the load capacitance and rising slew rate. Equation 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR\,(V/ms) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{3}$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn-on. The required C_{dVdt} capacitance to produce a given slew rate can be calculated using Equation 4.

$$C_{dVdt}\,(pF) = \frac{2000}{SR\,(V/ms)} \quad (4)$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

Note

For C_{dVdt} > 10 nF, TI recommends to add a 100-Ω resistor in series with the capacitor on the dVdt pin.

8.3.5.2 Circuit-Breaker

The TPS259474x (Circuit-Breaker) variants respond to output overcurrent conditions by turning off the output after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the fast-trip threshold (2 x I_{LIM}), the device starts discharging the ITIMER pin capacitor using an internal 1.8-µA pull-down current. If the load current drops below I_{LIM} before the ITIMER pin capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the circuit breaker action is not engaged. This allows short load transient pulses to pass through the device without tripping the circuit. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and after it discharges by ΔV_{ITIMER}, the circuit breaker action turns off the HFET immediately. At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This ensures the full blanking timer interval is provided for every overcurrent event. Equation 5 can be used to calculate the R_{ILM} value for a overcurrent threshold.

$$R_{ILM}\,(\Omega) = \frac{3334}{I_{LIM}\,(A)} \quad (5)$$

Note

1. Leaving the ILM pin open sets the current limit to nearly zero and results in the part breaking the circuit with the slightest amount of loading at the output.
2. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There is a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The C_{ITIMER} value needed to set the desired transient overcurrent blanking interval can be calculated using Equation 6.

$$t_{ITIMER}\,(ms) = \frac{\Delta V_{ITIMER}\,(V) \times C_{ITIMER}\,(nF)}{I_{ITIMER}\,(\mu A)} \quad (6)$$

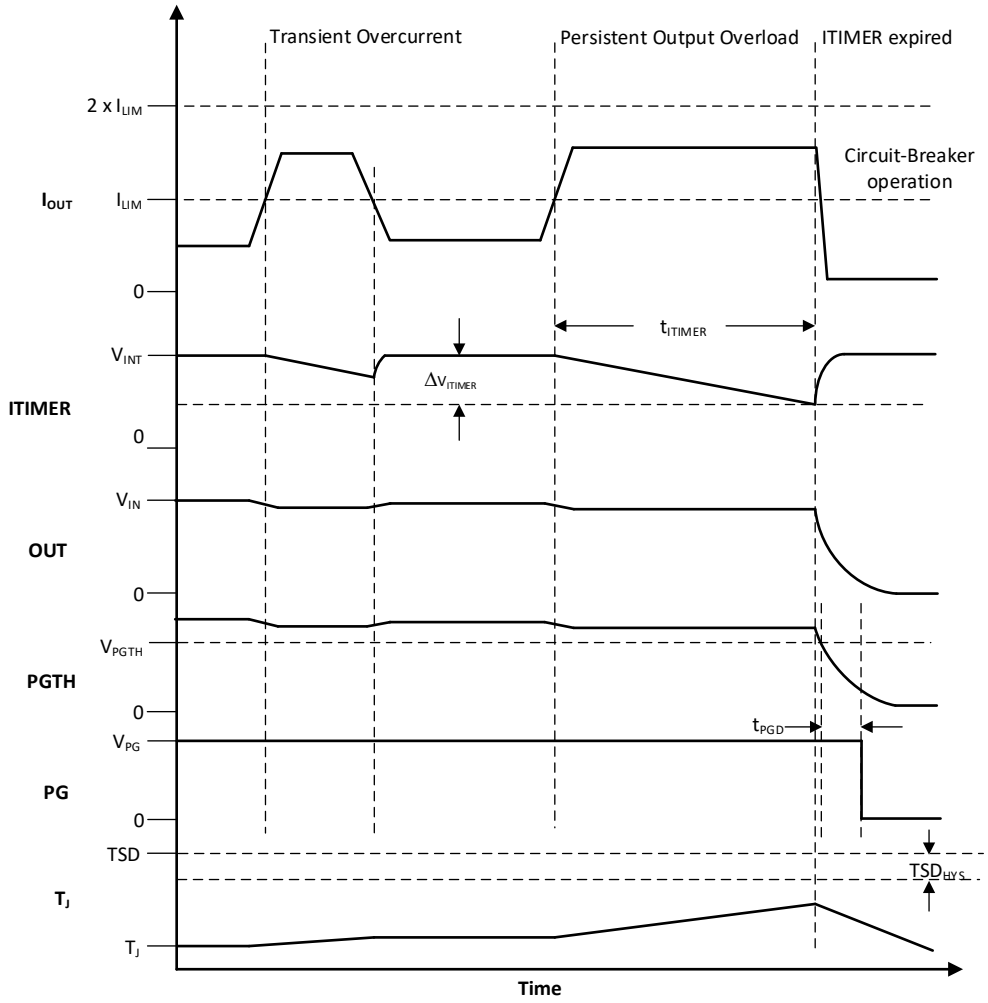


Figure 8-9. TPS259474x Overcurrent Response

Note

1. Leave the ITIMER pin open to allow the part to break the circuit with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This is not a recommended mode of operation.
3. Increasing the ITIMER cap value extends the overcurrent blanking interval, but it also extends the time needed for the ITIMER cap to recharge up to V_{INT}. If the next overcurrent event occurs before the ITIMER cap is recharged fully, it takes lesser time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.

After the part shuts down due to a Circuit Breaker fault, it can either stay latched off (TPS259474L variant) or restart automatically after a fixed delay (TPS259474A variant).

8.3.5.3 Active Current Limiting

The TPS259470x/2x (Active Current Limit) variants respond to output overcurrent conditions by actively limiting the current after a user adjustable transient fault blanking interval. When the load current exceeds the set overcurrent threshold (I_{LIM}) set by the ILM pin resistor (R_{ILM}), but stays lower than the short-circuit threshold (2 × I_{LIM}), the device starts discharging the ITIMER pin capacitor using an internal 1.8-µA pulldown current. If the load current drops below the overcurrent threshold before the ITIMER capacitor (C_{ITIMER}) discharges by ΔV_{ITIMER}, the ITIMER is reset by pulling it up to V_{INT} internally and the current limit action is not engaged. This allows

short load transient pulses to pass through the device without getting current limited. If the overcurrent condition persists, the C_{ITIMER} continues to discharge and after it discharges by ΔV_{ITIMER}, the current limit starts regulating the HFET to actively limit the current to the set overcurrent threshold (I_{LIM}). At the same time, the C_{ITIMER} is charged up to V_{INT} again so that it is at its default state before the next overcurrent event. This ensures the full blanking timer interval is provided for every overcurrent event. Equation 7 can be used to calculate the R_{ILM} value for a desired overcurrent threshold.

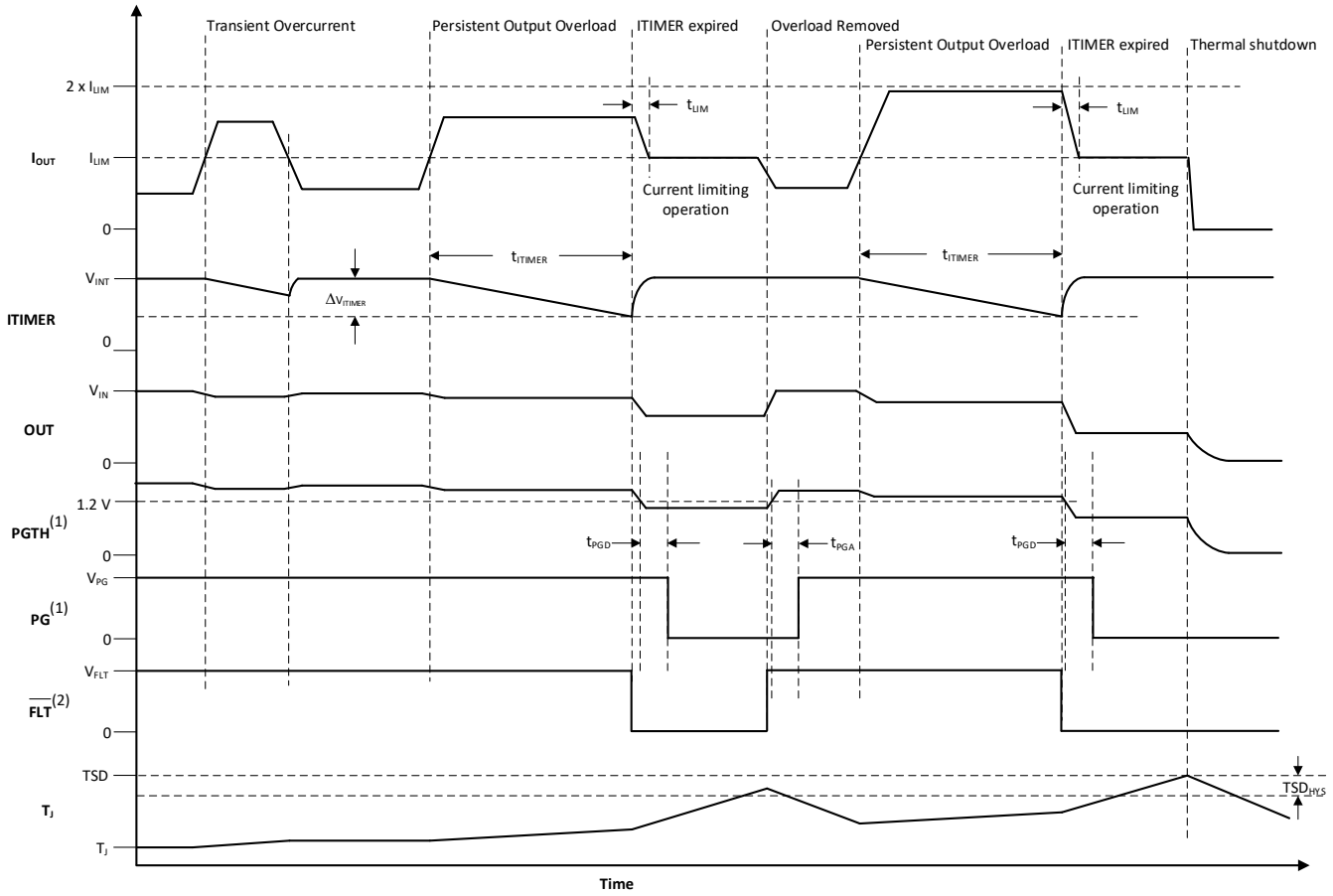
$$R_{ILM}\,(\Omega) = \frac{3334}{I_{LIM}\,(A)} \tag{7}$$

Note

1. Leaving the ILM pin open sets the current limit to nearly zero and results in the part entering current limit with the slightest amount of loading at the output.
2. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the steady state current limit threshold (I_{LIM}).
3. Shorting the ILM pin to ground at any point during normal operation is detected as a fault and the part shuts down. There's a minimum current (I_{FLT}) which the part allows in this condition before the pin short condition is detected.

The duration for which transients are allowed can be adjusted using an appropriate capacitor value from ITIMER pin to ground. The C_{ITIMER} value needed to set the desired transient overcurrent blanking interval can be calculated using Equation 8 below.

$$t_{ITIMER}\,(ms) = \frac{\Delta V_{ITIMER}\,(V) \times C_{ITIMER}\,(nF)}{I_{ITIMER}\,(\mu A)} \tag{8}$$



(1) Applicable only to TPS259472x/4x variants
(2) Applicable only to TPS259470x variants

Figure 8-10. TPS259470x/2x Active Current Limit Response

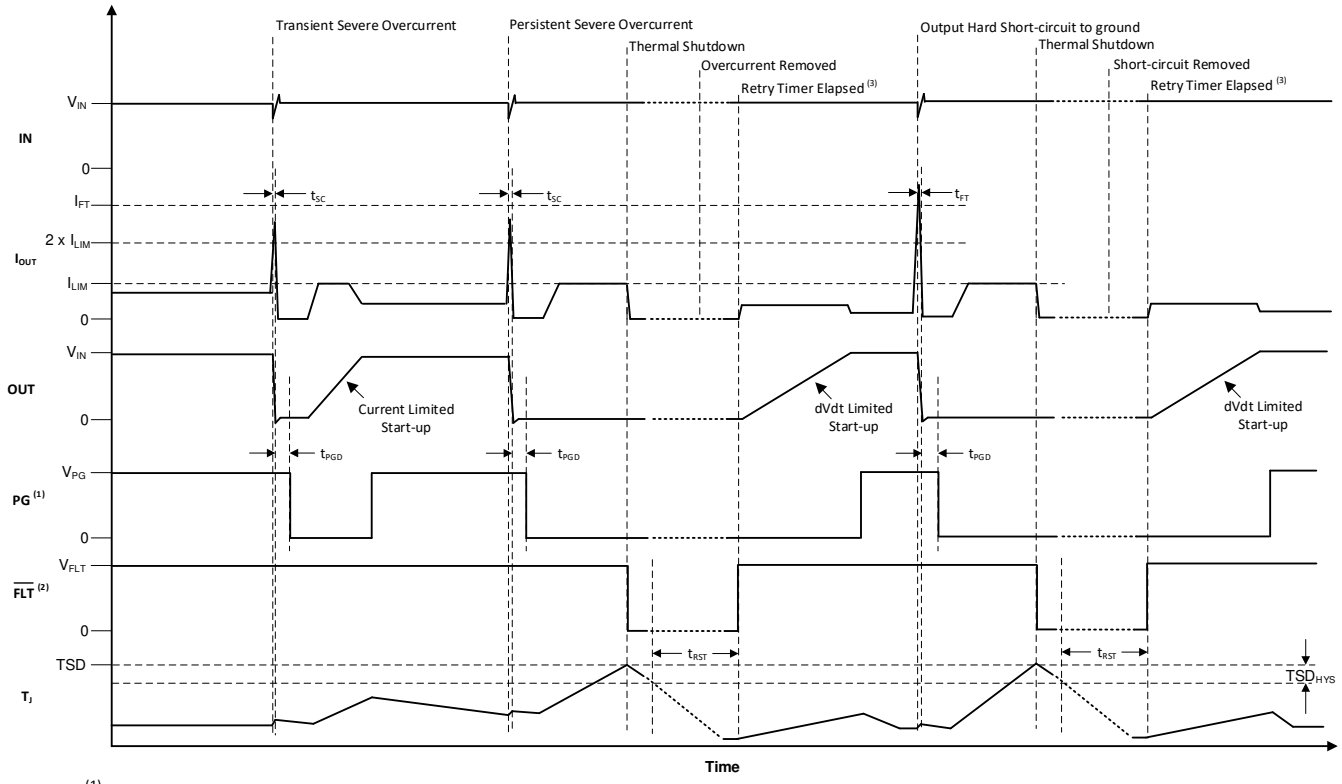
Note

1. Leave the ITIMER pin open to allow the part to limit the current with the minimum possible delay.
2. Shorting the ITIMER pin to ground results in minimum overcurrent response delay (similar to ITIMER pin open condition), but increases the device current consumption. This is not a recommended mode of operation.
3. Active current limiting based on R_{ILM} is active during start-up for both TPS259470x/2x (Current Limit) and TPS259474x (Circuit-Breaker) variants. In case the start-up current exceeds I_{LIM}, the device regulates the current to the set limit. However, during start-up the current limit is engaged without waiting for the ITIMER delay.
4. For the TPS259472x variants, during overvoltage clamp condition, if an overcurrent event occurs, the current limit is engaged without waiting for the ITIMER delay.
5. Increasing the C_{ITIMER} value extends the overcurrent blanking interval, but it also extends the time needed for the C_{ITIMER} to recharge up to V_{INT}. If the next overcurrent event occurs before the C_{ITIMER} is recharged fully, it takes less time to discharge to the ITIMER expiry threshold, thereby providing a shorter blanking interval than intended.

During active current limit, the output voltage drops resulting in increased device power dissipation across the HFET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the HFET is turned off. After the part shuts down due to TSD fault, it can either stay latched off (TPS25947xL variants) or restart automatically after a fixed delay (TPS25947xA variants). See *Overtemperature Protection (OTP)* for more details on device response to overtemperature.

8.3.5.4 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the device triggers a fast-trip response to limit the current to a safe level. The internal fast-trip comparator employs a scalable threshold (I_{SC}) which is equal to 2 × I_{LIM}. This enables the user to adjust the fast-trip threshold rather than using a fixed threshold which can be too high for some low current systems. The device also employs a fixed fast-trip threshold (I_{FT}) to protect fast protection against hard short-circuits during steady state. The fixed fast-trip threshold is higher than the maximum recommended user adjustable scalable fast-trip threshold. After the current exceeds I_{SC} or I_{FT}, the HFET is turned off completely within t_{FT}. Thereafter, the devices tries to turn the HFET back on after a short de-glitch interval (30 µs) in a current limited manner instead of a dVdt limited manner. This ensures that the HFET has a faster recovery after a transient overcurrent event and minimizes the output voltage droop. However, if the fault is persistent, the device stays in current limit causing the junction temperature to rise and eventually enter thermal shutdown. See *Overtemperature Protection (OTP)* section for details on the device response to overtemperature.



(1) Applicable only to TPS259472x/4x variants
(2) Applicable only to TPS259470x variants
(3) Applicable only to TPS25947xA variants

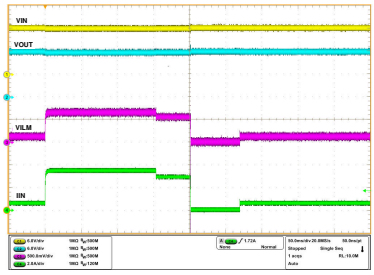
Figure 8-11. TPS25947xx Short-Circuit Response

8.3.6 Analog Load Current Monitor

The device allows the system to accurately monitor the output load current by providing an analog current sense output on the ILM pin which is proportional to the current through the FET. The user can sense the voltage (V_{ILM}) across the R_{ILM} to get a measure of the output load current.

$$I_{OUT}\,(A) = \frac{V_{ILM}\,(\mu V)}{R_{ILM}\,(\Omega) \times G_{IMON}\,(\mu A/A)} \tag{9}$$

The waveform below shows the ILM signal response to a load step at the output.



V_{IN} = 12 V, C_{OUT} = 22 µF, R_{ILM} = 1150 Ω, I_{OUT} varied dynamically between 0A and 3.5 A

Figure 8-12. Analog Load Current Monitor Response

Note

The ILM pin is sensitive to capacitive loading. Careful design and layout is needed to ensure the parasitic capacitive loading on the ILM pin is < 50 pF for stable operation.

8.3.7 Reverse Current Protection

The device functions like an ideal diode and blocks reverse current flow from OUT to IN under all conditions. The device has integrated back-to-back MOSFETs connected in a common drain configuration. The voltage drop between the IN and OUT pins is constantly monitored and the gate drive of the blocking FET (BFET) is adjusted as needed to regulate the forward voltage drop at V_{FWD}. This closed loop regulation scheme (linear ORing control) enables graceful turn off of the MOSFET during a reverse current event and ensures there is no DC reverse current flow.

The device also uses a conventional comparator (V_{REVTH}) based reverse blocking mechanism to provide fast response (t_{RCB}) to transient reverse currents. After the device enters reverse current blocking condition, it waits for the (V_{IN} – V_{OUT}) forward drop to exceed the V_{FWDTH} before it performs a fast recovery to reach full forward conduction state. This provides sufficient hysterisis to prevent supply noise or ripple from affecting the reverse current blocking response. The recovery from reverse current blocking is very fast (t_{SWRCB}). This ensures minimum supply droop which is helpful in applications such as supply MUXing/ORing and USB Fast Role Swap (FRS).

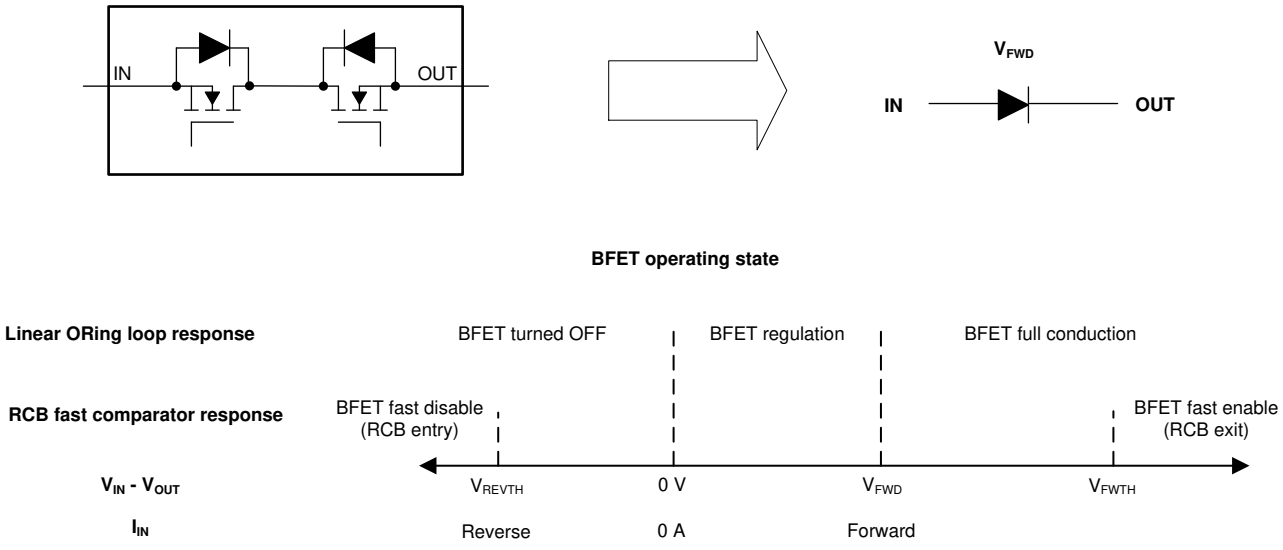


Figure 8-13. Reverse Current Blocking Response

The waveforms below illustrate the reverse current blocking performance in various scenarios.

During fast voltage step at output (for example. hot-plug), the fast comparator based reverse blocking mechanism ensures minimum jump/glitch on the input rail.

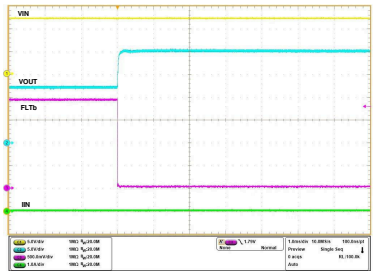


Figure 8-14. Reverse Current Blocking Performance During Fast Voltage Step at Output

During slow voltage ramp at output, the linear ORing based reverse blocking mechanism ensures there is no DC current flow from OUT to IN, thereby avoiding input rail from getting slowly charged up to output voltage.

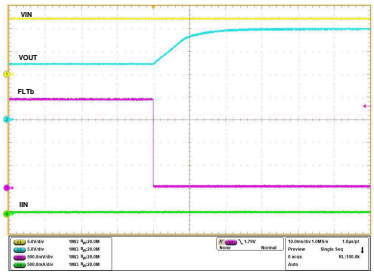


Figure 8-15. Reverse Current Blocking Performance During Slow Voltage Ramp at Output

When the input supply droops or gets disconnected while the output storage element (bulk capacitor or super capacitor) is charged to the full voltage, the linear ORing scheme minimizes the self-discharge from OUT to IN. This ensures maximum hold-up time for the output storage element in critical power back-up applications.

It also prevents incorrect supply presence indication in applications which sense the input voltage to detect if the supply is connected.

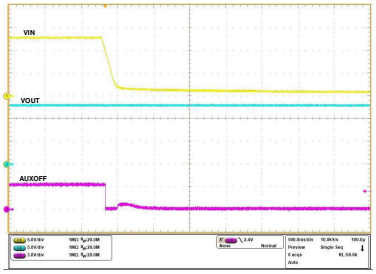


Figure 8-16. Reverse Current Blocking Performance During Input Supply Failure

8.3.8 Overtemperature Protection (OTP)

The device monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device does not turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD – TSD_{HYS}).

When the TPS25947xL (latch-off variant) detects thermal overload, it is shut down and remain latched-off until the device is power cycled or re-enabled. When the TPS25947xA (auto-retry variant) detects thermal overload, it remains off until it has cooled down by TSD_{HYS}. Thereafter, the device remains off for an additional delay of t_{RST} after which it automatically retries to turn on if it is still enabled.

Table 8-2. Thermal Shutdown

Device	Enter TSD	Exit TSD
TPS25947xL (Latch-Off)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$
TPS25947xA (Auto-Retry)	$T_J \geq TSD$	$T_J < TSD - TSD_{HYS}$ V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ OR EN/UVLO toggled below $V_{SD(F)}$ OR t_{RST} timer expired

8.3.9 Fault Response and Indication ($\overline{FLT}$)

The following table summarizes the device response to various fault conditions. Additionally, an active low external fault indication ($\overline{FLT}$) pin is available on the TPS259470x variants.

Table 8-3. Fault Summary

Event	Protection Response	Fault Latched Internally	$\overline{FLT}$ Pin Status (1)	$\overline{FLT}$ Assertion Delay(1)
Overtemperature	Shutdown	Y	L	
Undervoltage (UVP or UVLO)	Shutdown	N	H	
Input Reverse Polarity	Shutdown	N	H	
Input Overvoltage	Shutdown(1) (2)	N	H	
	Voltage Clamp(2)	N	N/A	
Transient Overcurrent ($I_{LIM} < I_{OUT} < 2 \times I_{LIM}$)	None	N	N	
Persistent Overcurrent	Circuit Breaker(3)	Y	N/A	
Persistent Overcurrent	Current Limit(4)	N	L	t_{ITIMER}
Output Short-Circuit to GND	Circuit Breaker followed by Current Limit	N	H	
ILM Pin Open (During Steady State)	Shutdown	N	L	t_{ITIMER}
ILM Pin Shorted to GND	Shutdown	Y	L	t_{ITIMER}
Reverse Current ($(V_{OUT} - V_{IN}) > V_{REVTH}$)	Reverse Current Blocking	N	L	

(1) Applicable to TPS259470x variants only.
(2) Applicable to TPS259472x variants only.
(3) Applicable to TPS259474x variants only.
(4) Applicable to TPS259470x/2x variants only.

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below V_{SD}. This also releases the $\overline{FLT}$ pin for the TPS259470x variants and resets the t_{RST} timer for the TPS25947xA (auto-retry) variants.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device. This is true for both TPS25947xL (latch-off) and TPS25947xA (auto-retry) variants.

For TPS25947xA (auto-retry) variants, on expiry of the t_{RST} timer after a fault, the device restarts automatically and the $\overline{FLT}$ pin is de-asserted (TPS259470A variant).

8.3.10 Auxiliary Channel Control (AUXOFF)

The TPS259470x variants provide an active high digital output (AUXOFF) which is asserted to indicate when the priority input supply is in a valid range (above UVP/UVLO and below OVLO thresholds) and the device has

successfully completed its inrush sequence. The AUXOFF pin is an open-drain signal which must be pulled up to an external supply.

After power up, AUXOFF pin is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the FET gate voltage has reached the full overdrive indicating that the inrush sequence is complete and device is capable of delivering full power, the AUXOFF pin is asserted high. Thereafter, the AUXOFF pin is de-asserted only if the input supply becomes invalid (below UVP/UVLO or above OVLO thresholds). No load side events/faults have any control over the AUXOFF de-assertion.

This pin is used to control the auxiliary channel when 2 TPS259470x devices are connected in a priority power MUX configuration. It can also be used as a supply valid status indication to the downstream load or system supervisor.

Table 8-4. TPS259470x AUXOFF Indication Summary

Event	AUXOFF Pin
Undervoltage (UVP or UVLO)	L
Input Reverse Polarity	L
Overvoltage (OVLO)	L
Inrush	L
Steady State	H
Overcurrent	H
Short-Circuit	H
ILM Pin Open	H
ILM Pin Shorted to GND	H
Reverse current ($(V_{OUT} – V_{IN}) > V_{REVTH}$)	H
Overtemperature	H

When there is no supply to the device, the AUXOFF pin is expected to stay low. However, there is no active pull-down in this condition to drive this pin all the way down to 0 V. If the AUXOFF pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition. This also ensures that the auxiliary channel is not turned off inadvertently in a priority power MUX configuration.

8.3.11 Power Good Indication (PG)

The TPS259472x, TPS259474x variants provide an active high digital output (PG) which serves as a power good indication signal and is asserted high depending on the voltage at the PGTH pin along with the device state information. The PG is an open-drain pin and must be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the HFET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the voltage at PGTH is above $V_{PGTH(R)}$, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time during normal operation, the voltage at PGTH falls below $V_{PGTH(F)}$, or the device detects a fault (except overcurrent). The PG de-assertion de-glitch time is t_{PGD}.

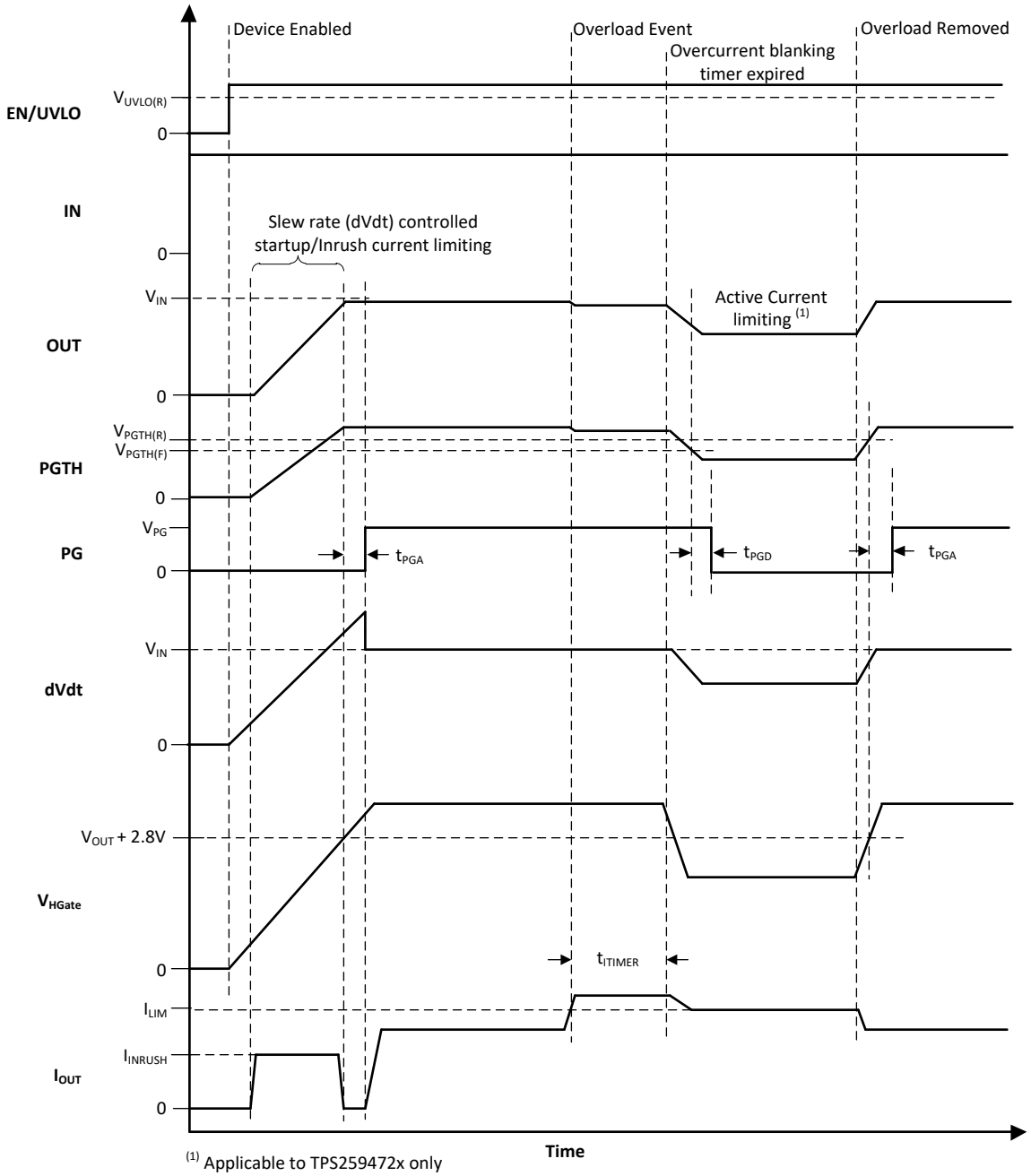


Figure 8-17. TPS259472x, TPS259474x PG Timing Diagram

Table 8-5. TPS259472x, TPS259474x PG Indication Summary

Event	Protection Response	PG Pin	PG Delay
Undervoltage (UVP or UVLO)	Shutdown	L	
Input Reverse Polarity	Shutdown	L	
Overvoltage (OVC) (TPS259472x only)	Clamp	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Overvoltage (OVLO) (TPS259474x only)	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}

Table 8-5. TPS259472x, TPS259474x PG Indication Summary (continued)

Event	Protection Response	PG Pin	PG Delay
Steady State	NA	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Transient overcurrent	NA	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Persistent overload (TPS259472x only)	Current Limiting	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Persistent overload (TPS259474x only)	Shutdown	L	
Output Short-Circuit to GND	Fast trip followed by Current Limit	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
ILM Pin Open	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}
ILM Pin Shorted to GND	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}
Reverse current ((V_{OUT} – V_{IN}) > V_{REVTH})	Reverse current blocking	L	t_{PGD}
Overtemperature	Shutdown	L	

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pull-down in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pull-up supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

8.4 Device Functional Modes

Table 8-6. TPS259472x Overvoltage Clamp Threshold Selection

OVCSEL Pin Connection	Overvoltage Clamp Threshold
Shorted to GND	3.8 V
Open	5.7 V
Connected to GND through a 390-kΩ resistor	13.8 V

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TPS25947xx is a 2.7-V to 23-V, 5.5-A eFuse that is typically used for power rail protection applications. The device operates from 2.7 V to 23 V with adjustable overvoltage and undervoltage protection. The device provides ability to control inrush current and protection against input reverse polarity as well as reverse current conditions. The device can be used in a variety of systems such as adapter input protection, USB PD port protection, server/PC motherboard/add-on cards, enterprise storage – RAID/HBA/SAN/eSSD, monitors, docks. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, *TPS25947xx Design Calculator*, is available in the web product folder.

9.2 Single Device, Self-Controlled

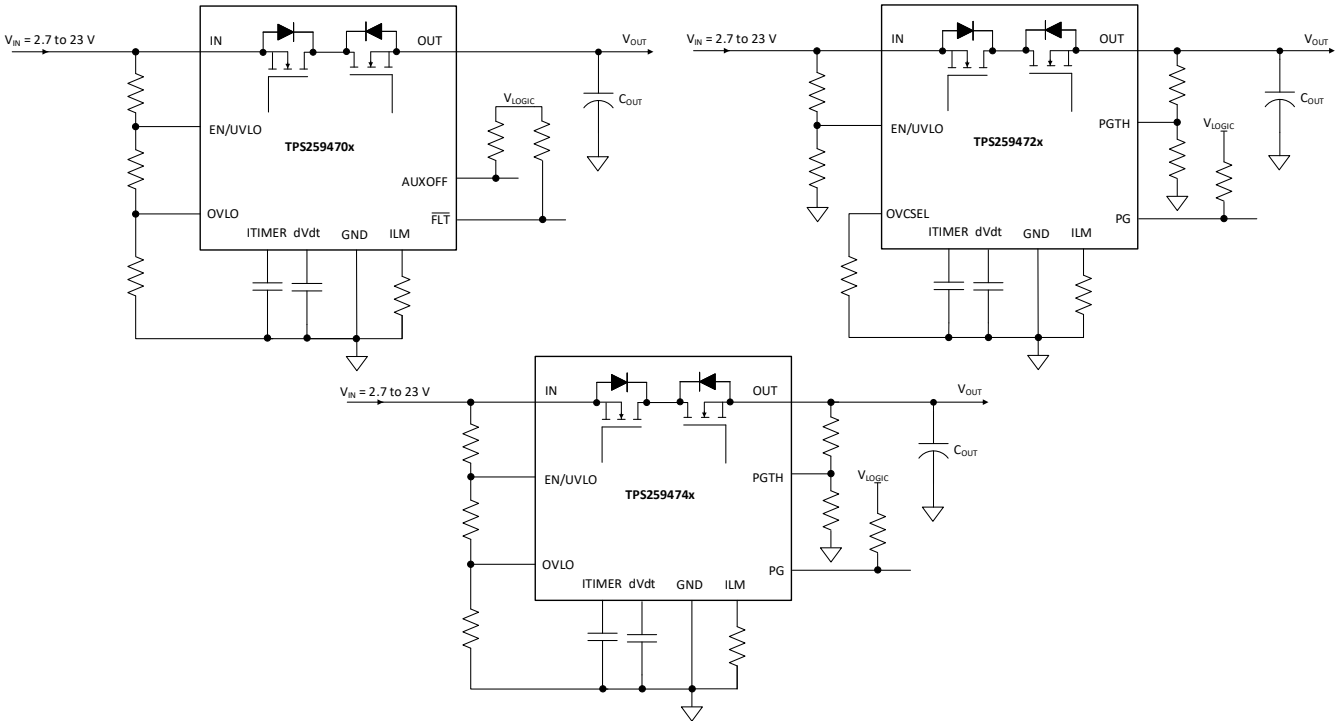


Figure 9-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

ILM pin can be connected to the MCU ADC input for current monitoring purpose.

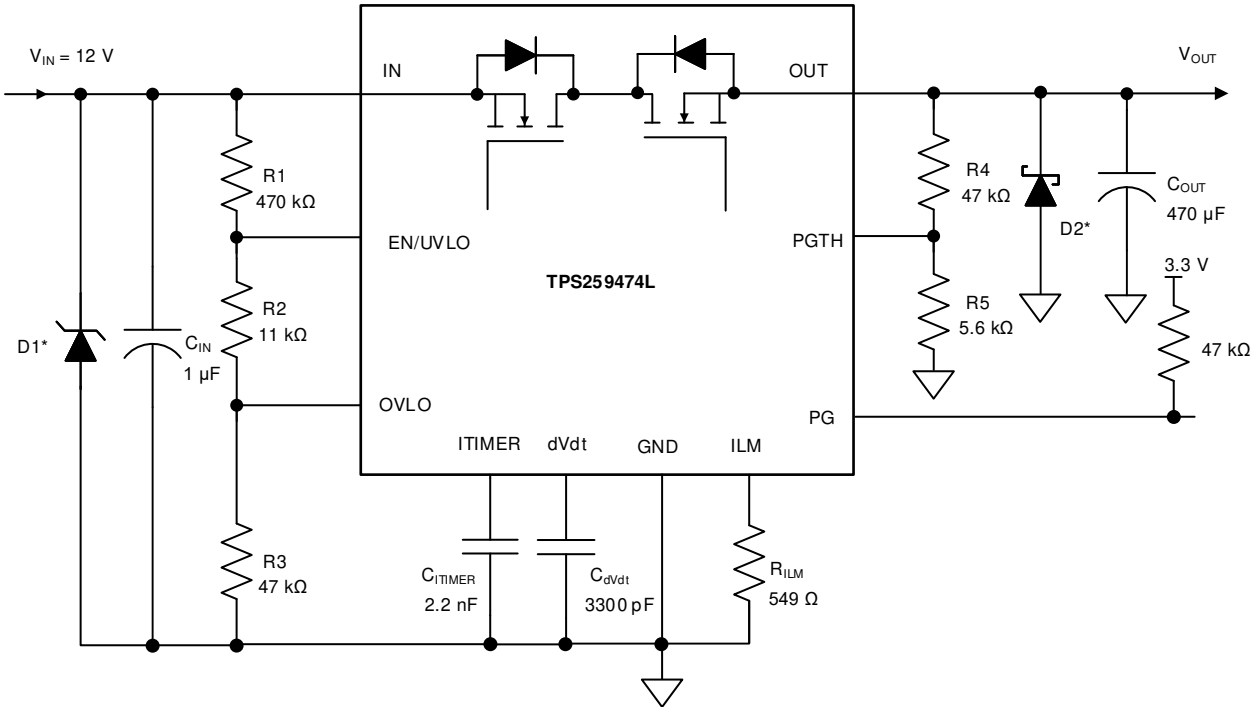
Note

TI recommends to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation.

For the TPS259472x/4x variants, either V_{IN} or V_{OUT} can be used to drive the PGTH resistor divider depending on which supply must be monitored for power good indication.

9.3 Typical Application

TPS259474x can be used for PCIe card input power protection. A full-sized ×16 graphics card can draw up to 5.5 A at +12 V (66 W). A typical PCIe slot has the capacity of providing current up to 6 A. During overcurrent or short-circuit event at load side, TPS259474x can quickly respond to this fault event by turning off the device and thus protect the load from damage as well as prevent input supply from drooping. The ITIMER feature allows short duration peak currents to pass through without tripping the eFuse, thereby meeting the transient load current profile of graphics cards.



* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

Figure 9-2. PCIe Card Input Power Protection

9.3.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	VALUE
Input supply voltage (V_{IN})	12 V
Undervoltage threshold ($V_{IN(UV)}$)	10.8 V
Overvoltage threshold ($V_{IN(OV)}$)	13.2 V
Output power good threshold (V_{PG})	11.4 V
Max continuous current	5.5 A
Load transient blanking interval (t_{ITIMER})	2 ms
Output capacitance (C_{OUT})	470 µF
Output rise time (t_R)	20 ms

Table 9-1. Design Parameters (continued)

PARAMETER	VALUE
Overcurrent threshold (I_{LIM})	6 A
Overcurrent response	Circuit breaker
Fault response	Latch-off

9.3.2 Detailed Design Procedure

9.3.2.1 Device Selection

Because the application requires circuit-breaker response to overcurrent with latch-off response after a fault, the TPS259474L variant is selected after refering to the *Device Comparison Table*.

9.3.2.2 Setting Undervoltage and Overvoltage Thresholds

The supply undervoltage and overvoltage thresholds are set using the resistors R1, R2 and R3 whose values can be calculated using Equation 10 and Equation 11:

$$V_{IN(UV)} = \frac{V_{UVLO(R)} \times (R1 + R2 + R3)}{R2 + R3} \tag{10}$$

$$V_{IN(OV)} = \frac{V_{OV(R)} \times (R1 + R2 + R3)}{R3} \tag{11}$$

Where $V_{UVLO(R)}$ is the UVLO rising threshold and $V_{OV(R)}$ is the OVLO rising threshold. Because R1, R2 and R3 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current from input power supply V_{IN}. The current drawn by R1, R2 and R3 from the power supply is IR123 = V_{IN} / (R1 + R2 + R3). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the leakage current expected on the EN/UVLO and OVLO pins.

From the device electrical specifications, both the EN/UVLO and OVLO leakage currents are 0.1 µA (maximum), $V_{OV(R)}$ = 1.2 V and $V_{UVLO(R)}$ = 1.2 V. From design requirements, $V_{IN(OV)}$ = 13.2 V and $V_{IN(UV)}$ = 10.8 V. To solve the equation, first choose the value of R1 = 470 kΩ and use the above equations to solve for R2 = 10.7 kΩ and R3 = 48 kΩ.

Using the closest standard 1% resistor values, we get R1 = 470 kΩ, R2 = 11 kΩ, and R3 = 47 kΩ.

9.3.2.3 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$SR\,(V/ms) = \frac{V_{IN}\,(V)}{t_R\,(ms)} = \frac{12\ V}{20\ ms} = 0.6\ V/ms \tag{12}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$C_{dVdt}\,(pF) = \frac{2000}{SR\,(V/ms)} = \frac{2000}{0.6} = 3333\ pF \tag{13}$$

Choose the nearest standard capacitor value as 3300 pF.

For this slew rate, the inrush current can be calculated as:

$$I_{INRUSH}\,(mA) = SR\,(V/ms) \times C_{OUT}\,(\mu F) = 0.6 \times 470 = 282\ mA \quad (14)$$

The average power dissipation inside the part during inrush can be calculated as:

$$PD_{INRUSH}\,(W) = \frac{I_{INRUSH}\,(A) \times V_{IN}\,(V)}{2} = \frac{0.282 \times 12}{2} = 1.69\ W \quad (15)$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. Figure 9-3 shows the thermal shutdown limit, for 1.69 W of power, the shutdown time is more than 10 s which is very large as compared to t_R = 20 ms. Therefore, it is safe to use 20 ms as the startup time for this application.

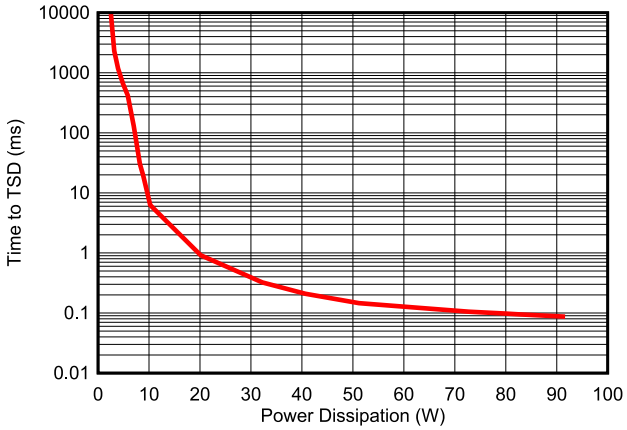


Figure 9-3. Thermal Shut-Down Plot During Inrush

9.3.2.4 Setting Power Good Assertion Threshold

The Power Good assertion threshold can be set using the resistors R4 and R5 connected to the PGTH pin whose values can be calculated as:

$$V_{PG} = \frac{V_{PGTH(R)} \times (R4 + R5)}{R5} \quad (16)$$

Because R4 and R5 leak the current from the output rail V_{OUT}, these resistors must be selected to minimize the leakage current. The current drawn by R4 and R5 from the power supply is IR45 = V_{OUT} / (R4 + R5). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the PGTH leakage current expected.

From the device electrical specifications, PGTH leakage current is 1 µA (maximum), $V_{PGTH(R)}$ = 1.2 V and from design requirements, V_{PG} = 11.4 V. To solve the equation, first choose the value of R4 = 47 kΩ and calculate R5 = 5.52 kΩ. Choose nearest 1% standard resistor value as R5 = 5.6 kΩ.

9.3.2.5 Setting Overcurrent Threshold (I_{LIM})

The overcurrent protection (Circuit Breaker) threshold can be set using the R_{ILM} resistor whose value can be calculated as:

$$R_{ILM}\,(\Omega) = \frac{3334}{I_{LIM}\,(A)} = \frac{3334}{6\ A} = 555.6\ \Omega \quad (17)$$

Choose nearest 1% standard resistor value as 549 Ω.

9.3.2.6 Setting Overcurrent Blanking Interval (t_{ITIMER})

The overcurrent blanking timer interval can be set using the C_{ITIMER} capacitor whose value can be calculated as:

$$C_{ITIMER}\,(nF) = \frac{t_{ITIMER}\,(ms) \times I_{ITIMER}\,(\mu A)}{\Delta V_{ITIMER}\,(V)} = \frac{2 \times 1.8}{1.51} = 2.38\ nF \quad (18)$$

Choose nearest standard capacitor value as 2.2 nF.

9.3.3 Application Curves

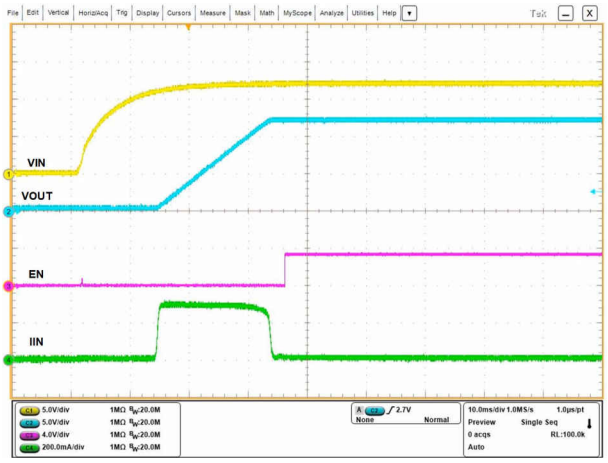


Figure 9-4. Power Up

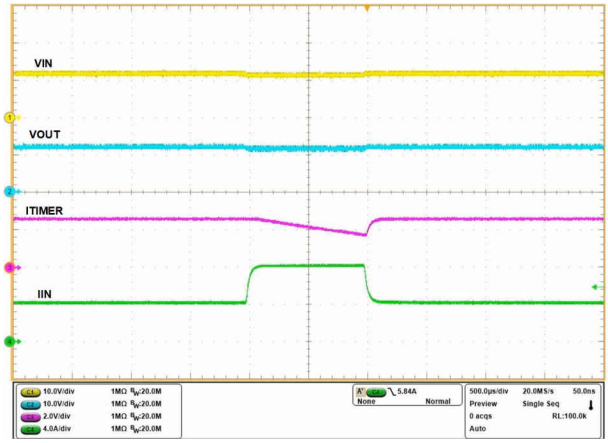


Figure 9-5. Transient Overload

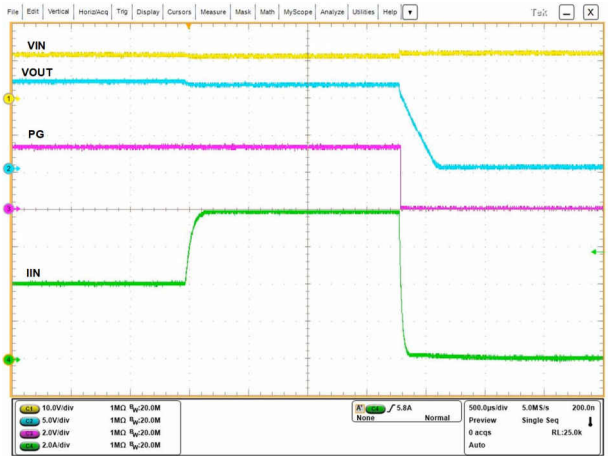


Figure 9-6. Circuit Breaker Response

9.4 Active ORing

A typical redundant power supply configuration is shown in Figure 9-7 below. Schottky ORing diodes have been popular for connecting parallel power supplies, such as parallel operation of wall adapter with a battery or a hold-up storage capacitor. The disadvantage of using ORing diodes is high voltage drop and associated power loss. The TPS259470x/4x with integrated, low-ohmic, back-to-back FETs provide a simple and efficient solution. Figure 9-7 below shows the Active ORing implementation using TPS249474x devices.

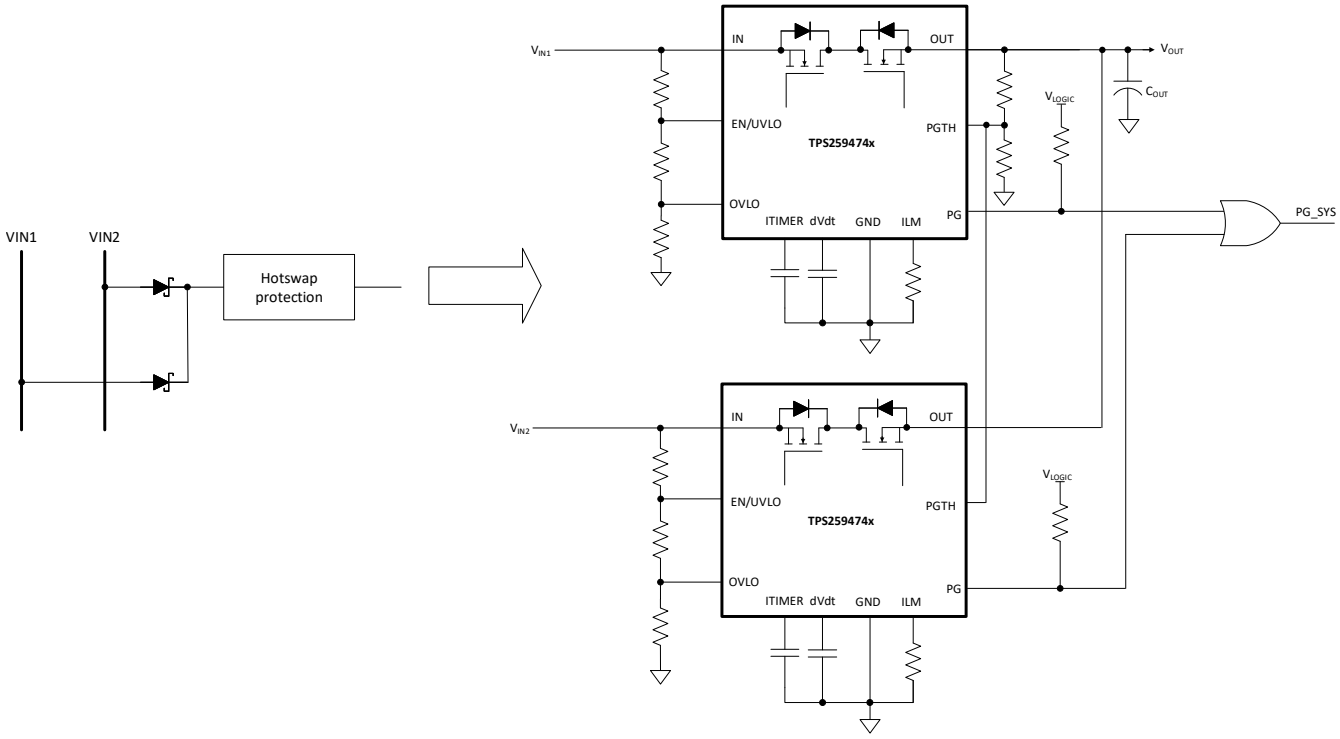


Figure 9-7. Two Devices, Active ORing Configuration

The linear ORing mechanism in TPS25947xx ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

The following waveform illustrates the active ORing behavior when the supply rails are being ramped up sequentially.

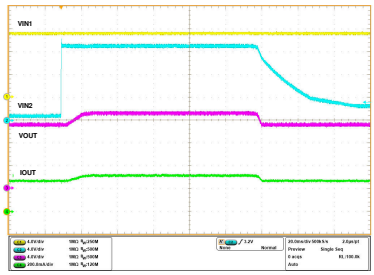


Figure 9-8. Active ORing Response

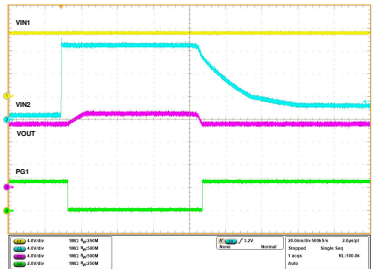


Figure 9-9. Active ORing Response

When the bus voltages (IN1 and IN2) are matched, device in each path sees a forward voltage drop and is ON delivering the load current. During this period, current is shared between the rails in the ratio of differential voltage drop across each device.

In addition to supply ORing, the devices protect the system from overvoltage, excessive inrush current, overload and short-circuit faults at all times.

Note

1. The TPS259472x (OVC variants) are not recommended for use in ORing applications. While the device is in clamping state, if the output is forced to a higher voltage by the other channel, the device can get damaged.
2. ORing can be done either between two similar rails or between dissimilar rails. For ORing cases with skewed voltage combinations, care must be taken to design circuit components on PGTH/EN/OVLO pins for the lower voltage channel devices such that the Absolute maximum ratings on those pins are not exceeded when higher voltage is present on the other channel. Also, the dVdt pin capacitor rating must be chosen based on the highest of the 2 supplies. Refer to Recommended Operating Conditions table for more details.

9.5 Priority Power MUXing

Applications having two energy sources such as PCIe cards, Tablets and Portable battery powered equipment require preference of one source to another. For example, mains power (wall-adapter) has the priority over the internal battery back-up power. These applications demand for switchover from mains power to backup power only when main input voltage falls below a user defined threshold. The TPS25947xx devices provide a simple solution for priority power multiplexing needs.

Figure 9-10 below shows a typical priority power multiplexing implementation using TPS259470x devices. When primary (priority) power source (IN1) is present and within the valid range (not in UV/OV condition), the primary path device path powers the OUT bus irrespective of whether auxiliary supply voltage (V_{IN2}) is greater than, equal to or less than primary supply voltage (V_{IN1}). The device in auxiliary path is held in off condition by forcing its OVLO pin to high using the AUXOFF signal from the primary path device.

After the primary supply voltage falls outside the user-defined valid operating range (UV/OV condition), the primary path device de-asserts the AUXOFF which signals the auxiliary path device to turn on and the system starts operating from the auxiliary supply. During this transition, the auxiliary path device bypasses its dVdt limited startup and performs a fast recovery to start delivering power within t_{SWOV}.

When the primary supply is restored, the primary path device turns on fully at a defined slew rate and then asserts its AUXOFF pin high to turn the auxiliary path device off, allowing a seamless transition from auxiliary to the primary supply with minimal output voltage droop and with no shoot-through current.

A key consideration in power MUXing applications is the minimum voltage the output bus droops to during the switchover from one supply to another. This in turn depends on multiple factors including the output load current (I_{LOAD}), output bus hold-up capacitance (C_{OUT}) and switchover time (t_{SW}).

While switching from primary supply (V_{IN1}) to auxiliary supply (V_{IN2}), the minimum bus voltage can be calculated using Equation 19. Here, the switchover time (t_{SW}) is equal to the fast OVLO recovery time (t_{SWOV}) taken by the TPS259470x variants to turn on fully and start delivering current to the load.

$$V_{OUT(min)}(V) = \min\left(V_{IN1}, V_{IN2}\right) - \frac{t_{SW}(\mu s) \times I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (19)$$

While switching from auxiliary supply (V_{IN2}) to primary supply (V_{IN1}), the minimum bus voltage can be calculated using Equation 20. Here the maximum switchover time is equal to the RCB recovery time (t_{SWRCB}), depending on whether V_{IN1} is equal to or lower than V_{IN2} to start with.

$$V_{OUT(min)}(V) = \min\left(V_{IN1}, V_{IN2}\right) - V_{FWDTH}(V) - \frac{t_{SWRCB}(\mu s) \times I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (20)$$

The AUXOFF pins of the devices can be used as a digital indication to identify which of the 2 supplies is active and delivering power to the load.

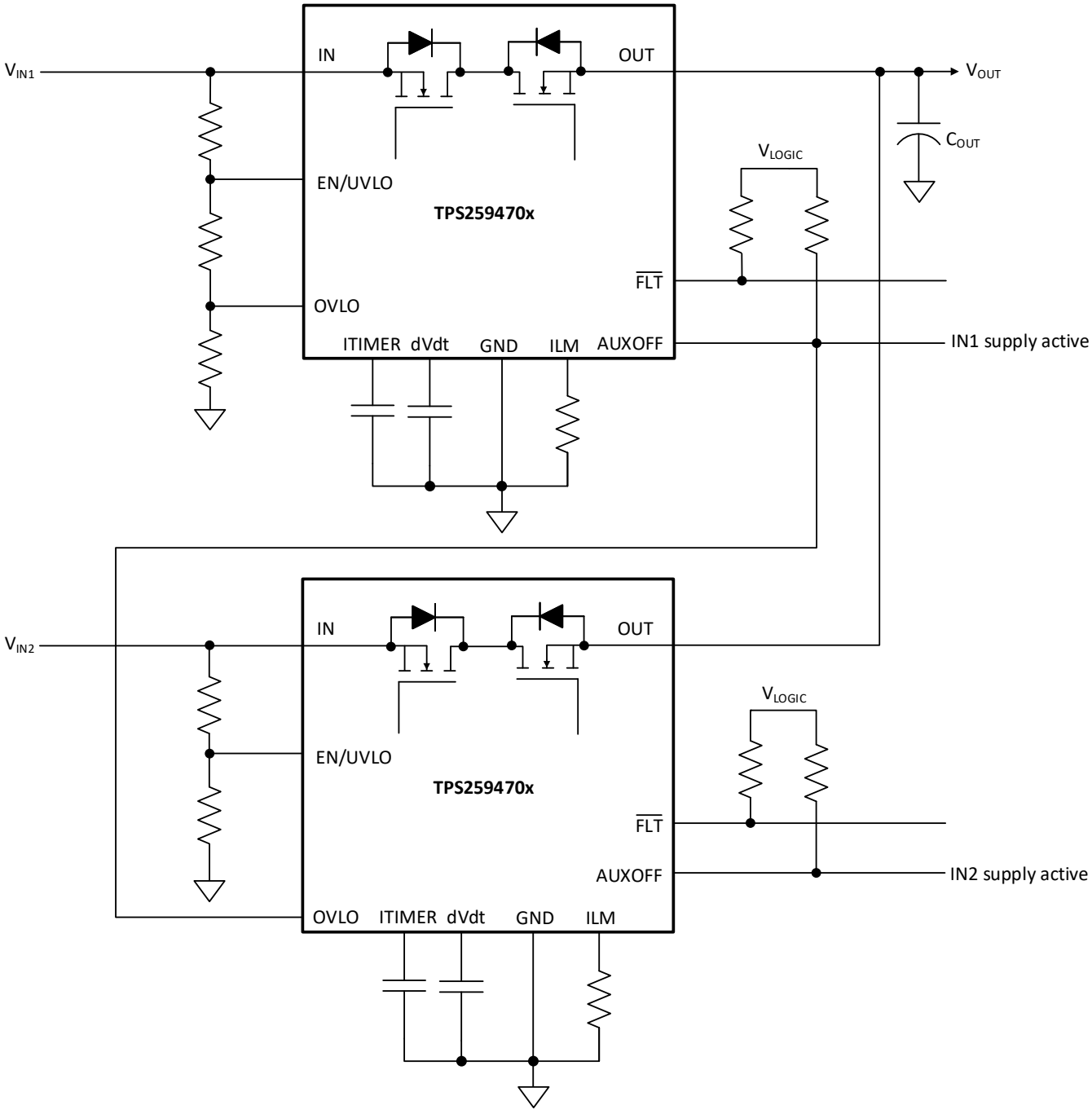


Figure 9-10. Priority Power MUXing with 2 × TPS259470x - Option 1

This configuration provides the most compact priority power MUXing solution with multiple benefits, including active current limit protection on both channels as well as overvoltage protection on primary channel. It also provides the fastest switchover time from primary to auxiliary, but at the cost of a slightly increased quiescent current on the auxiliary path while primary path is active. Also, it uses the fewest external components, but at the cost of bypassing overvoltage protection on auxiliary channel.

The following waveforms illustrate the TPS259470x performance in a priority power MUXing configuration.

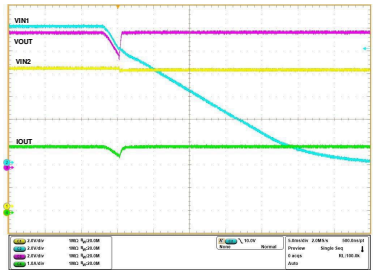


Figure 9-11. TPS259470x Power MUX - Switchover from Primary to Auxiliary Supply

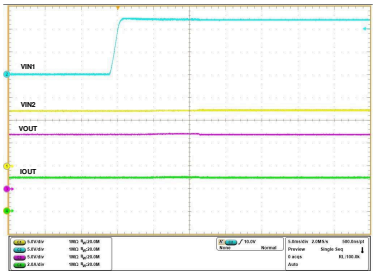


Figure 9-12. TPS259470x Power MUX - Switchover from Auxiliary to Primary Supply

There's a possible variation to the above configuration in case overvoltage protection is needed on both channels. This needs an additional signal N-FET to drive the OVLO pin of the auxiliary path device as shown in Figure 9-13 below. The switchover times are similar to the previous configuration.

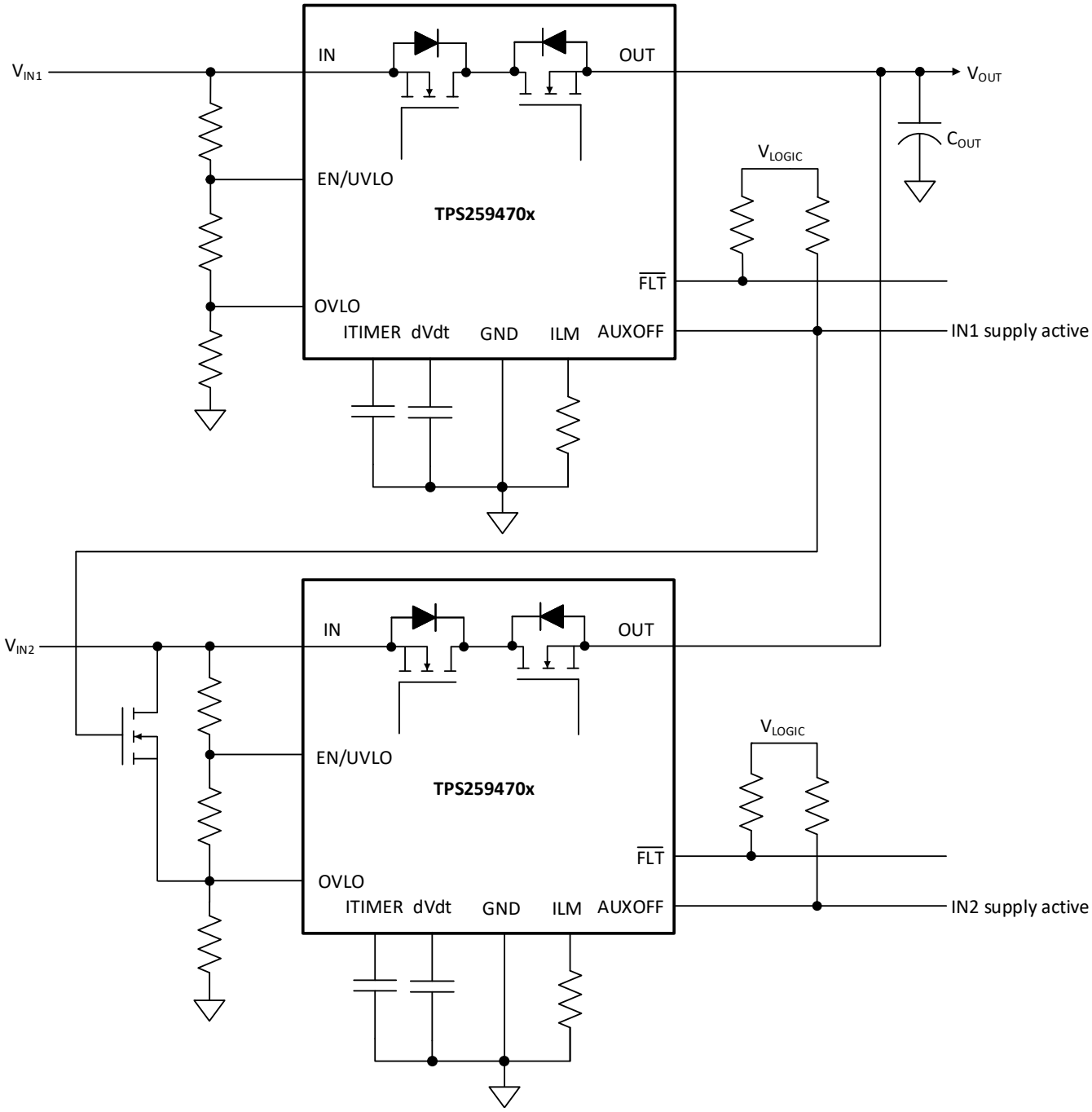


Figure 9-13. Priority Power MUXing with 2 × TPS259470x - Option 2

Another variation of the previous configuration ensures minimum quiescent current on the auxiliary chanel while primary channel is active, but at the cost of additional N-FET to drive the EN/UVLO pin of auxiliary path device as shown in Figure 9-14 below. At the same time, it has a higher switchover delay from primary to auxiliary supply as compared to the previous configuration.

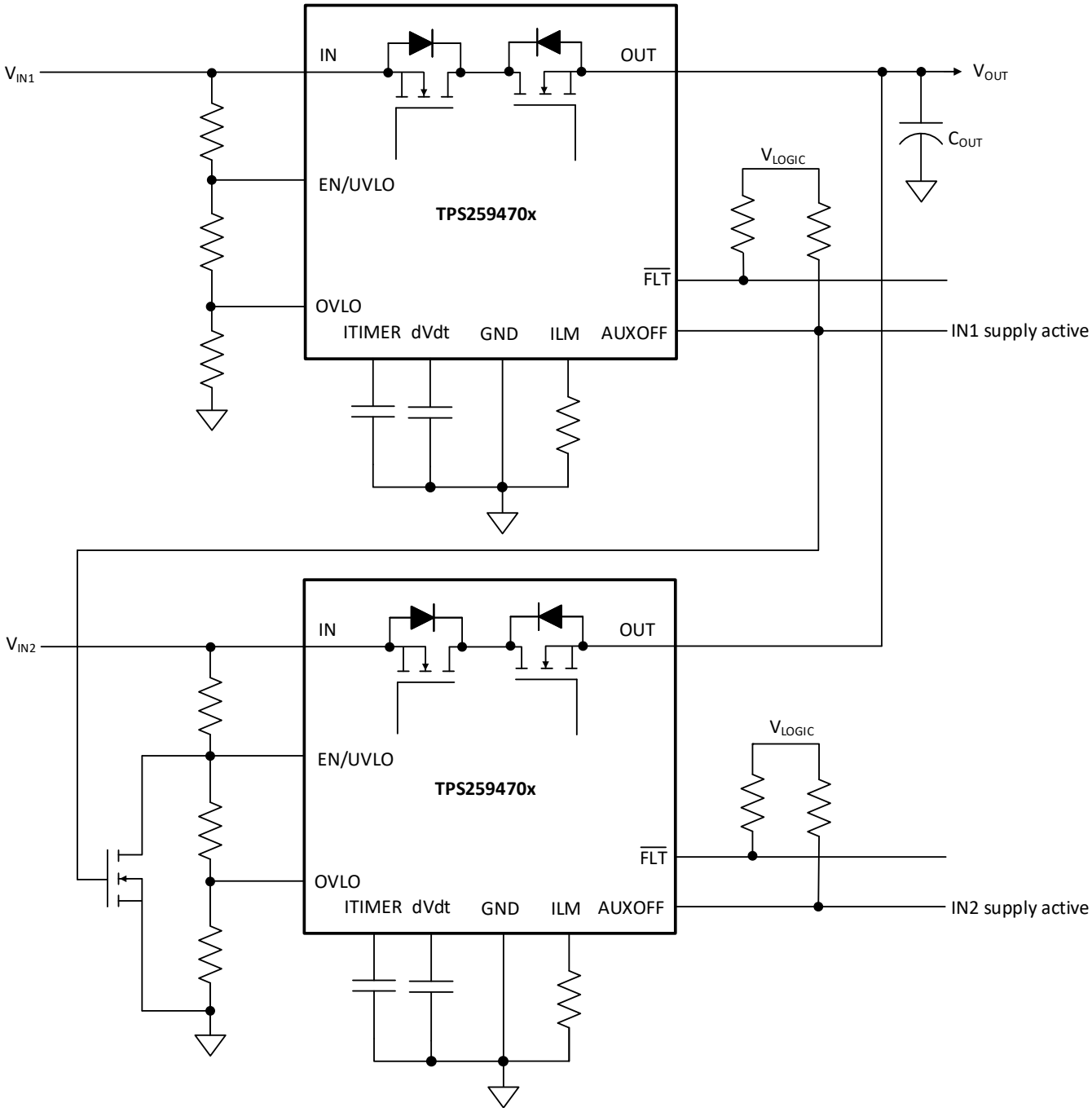


Figure 9-14. Priority Power MUXing with 2 × TPS259470x - Option 3

While switching from a higher supply rail to lower supply rail, the minimum bus voltage can be calculated using Equation 21. Here, the switchover time is equal to the time taken by the device to come out of reverse current blocking state (t_{SWRCB}).

$$V_{OUT(min)}(V) = \min\left(V_{IN1}, V_{IN2}\right) - V_{FWDTH}(V) - \frac{t_{SWRCB}(\mu s) \times I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (21)$$

While switching from a lower supply rail to higher supply rail, the minimum bus voltage can be calculated using Equation 22. Here, the switchover time (t_{SW}) is the time taken by the device to turn on fully and start delivering

current to the load, which is equal to the device turn-on time (t_{ON}), which in turn includes the turn-on delay ($t_{D,ON}$) and rise time (t_R) determined by the dVdt capacitor (C_{dVdt}) and bus voltage.

$$V_{OUT(min)}\left(V\right) = \min\left(V_{IN1}, V_{IN2}\right) - \frac{t_{SW}\left(\mu s\right) \times I_{LOAD}\left(A\right)}{C_{OUT}\left(\mu F\right)} \quad (22)$$

All the preceding configurations provide a priority power MUXing solution with active current limit protection response. In case circuit breaker response is prefered, it is possible to implement a solution using TPS259474x devices as shown in Figure 9-15 below. Here, the EN/UVLO signal of the primary path device is used to control the OVLO of the auxiliary path device. This ensures that auxiliary path device is turned on only when the primary supply falls below a user-defined undervoltage (UVLO) threshold. In this configuration, supply overvoltage protection is not available on both channels. The PG pins of the devices can be used as a digital indication to identify which of the 2 supplies is active and delivering power to the load.

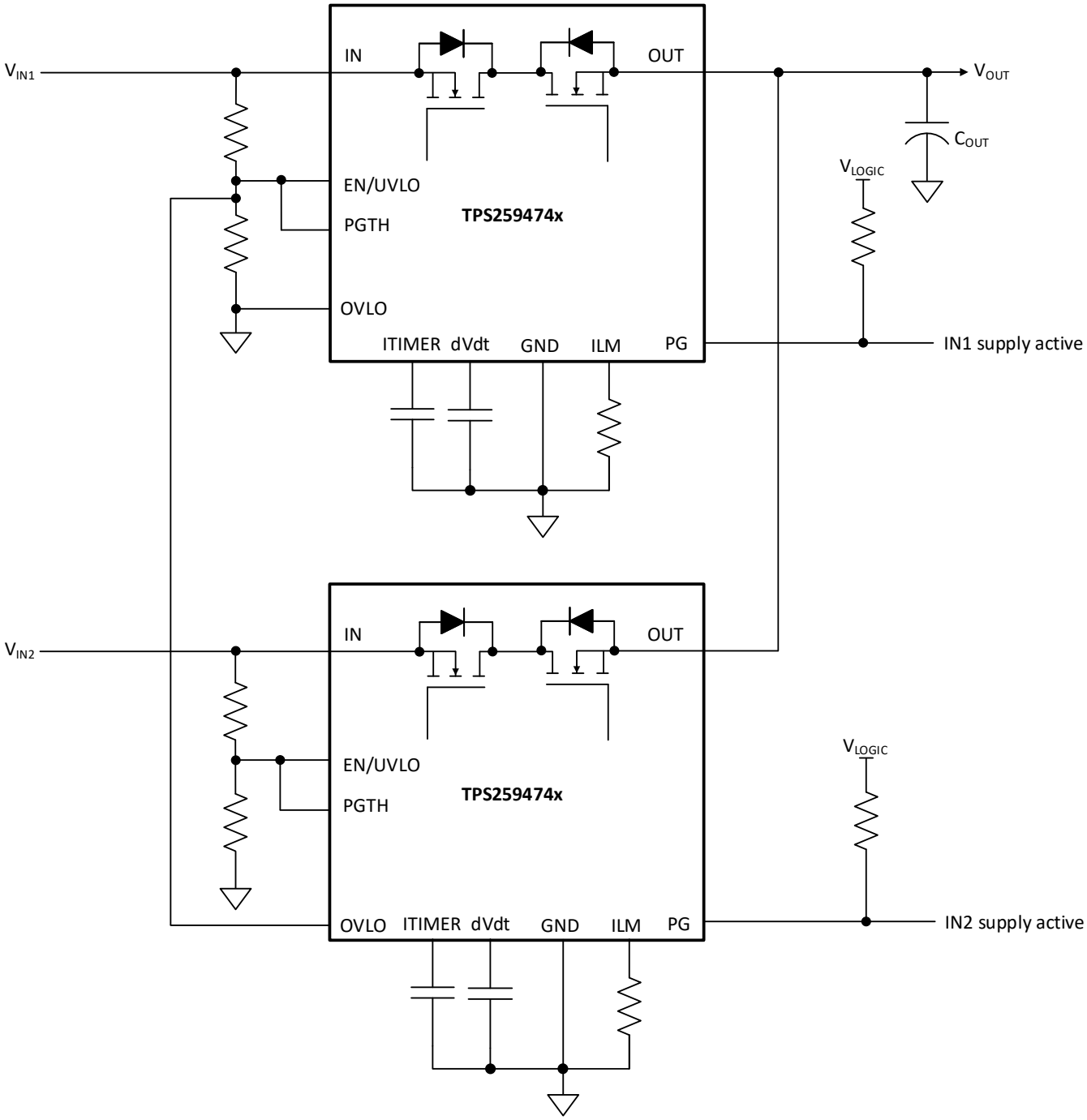


Figure 9-15. Priority power MUXing with 2 × TPS259474x

While switching from one supply rail to the other, the minimum bus voltage can be calculated using Equation 23. Here, the maximum switchover time (t_{SW}) is the time taken by the device to turn on and start delivering power to the load, which is equal to the device turn-on time (t_{ON}), which in turn includes the turn-on delay ($t_{D,ON}$) and rise time (t_R) determined by the dVdt capacitor (C_{dVdt}) and bus voltage.

$$V_{OUT(min)}(V) = \min\left(V_{IN1}, V_{IN2}\right) - \frac{t_{SW}(\mu s) \times I_{LOAD}(A)}{C_{OUT}(\mu F)} \quad (23)$$

Note

1. The TPS259472x (OVC variants) are not recommended for use in power MUXing or ORing applications. While the device is in clamping state, if the output is forced to a higher voltage by the other channel, the device can get damaged.
2. Power MUXing can be done either between two similar rails (such as 12-V Primary and 12-V Aux, 3.3-V Primary and 3.3-V Aux) or between dissimilar rails (such as 12-V Primary and 5-V Aux or vice versa).
3. For power MUXing cases with skewed voltage combinations, care must be taken to design circuit components on PGTH/EN/OVLO pins for the lower voltage channel devices such that the Absolute maximum ratings on those pins are not exceeded when higher voltage is present on the other channel. Also, the dVdt pin capacitor rating must be chosen based on the highest of the 2 supplies. Refer to Recommended Operating Conditions table for more details.

9.6 USB PD Port Protection

End equipments like PC, Notebooks, Docking Stations, Monitors etc.. have USB PD ports which can be configured as DFP (Source), UFP (Sink) or DRP (Source+Sink). TPS259470x can be used independently or in conjunction with LM73100 to handle the power path protection requirements of USB PD ports as shown in Figure 9-16 below.

TPS259470x provides Overcurrent and Short-Circuit protection in the source path, while blocking any reverse current from the port to the internal source power rail. The fast recovery (t_{SWRCB}) from reverse current blocking ensures minimum supply droop during Fast Role Swap (FRS) events. The PD controller can also use the OVLO pin as an active low enable signal to control the power path. Holding the OVLO pin high keeps the device in OFF state in sink mode and blocks current in both directions. After the PD controller determines the need to start sourcing power, it can pull the OVLO pin low to trigger a fast recovery from OFF to ON state within t_{SWOV}, meeting the FRS timing requirements.

The LM73100 provides overvoltage protection on the sink path, while blocking reverse current from internal sink rail to the port.

The linear ORing mechanism in TPS259470x and LM73100 ensures that there's no reverse current flowing from one power source to the other during fast or slow ramp of either supply.

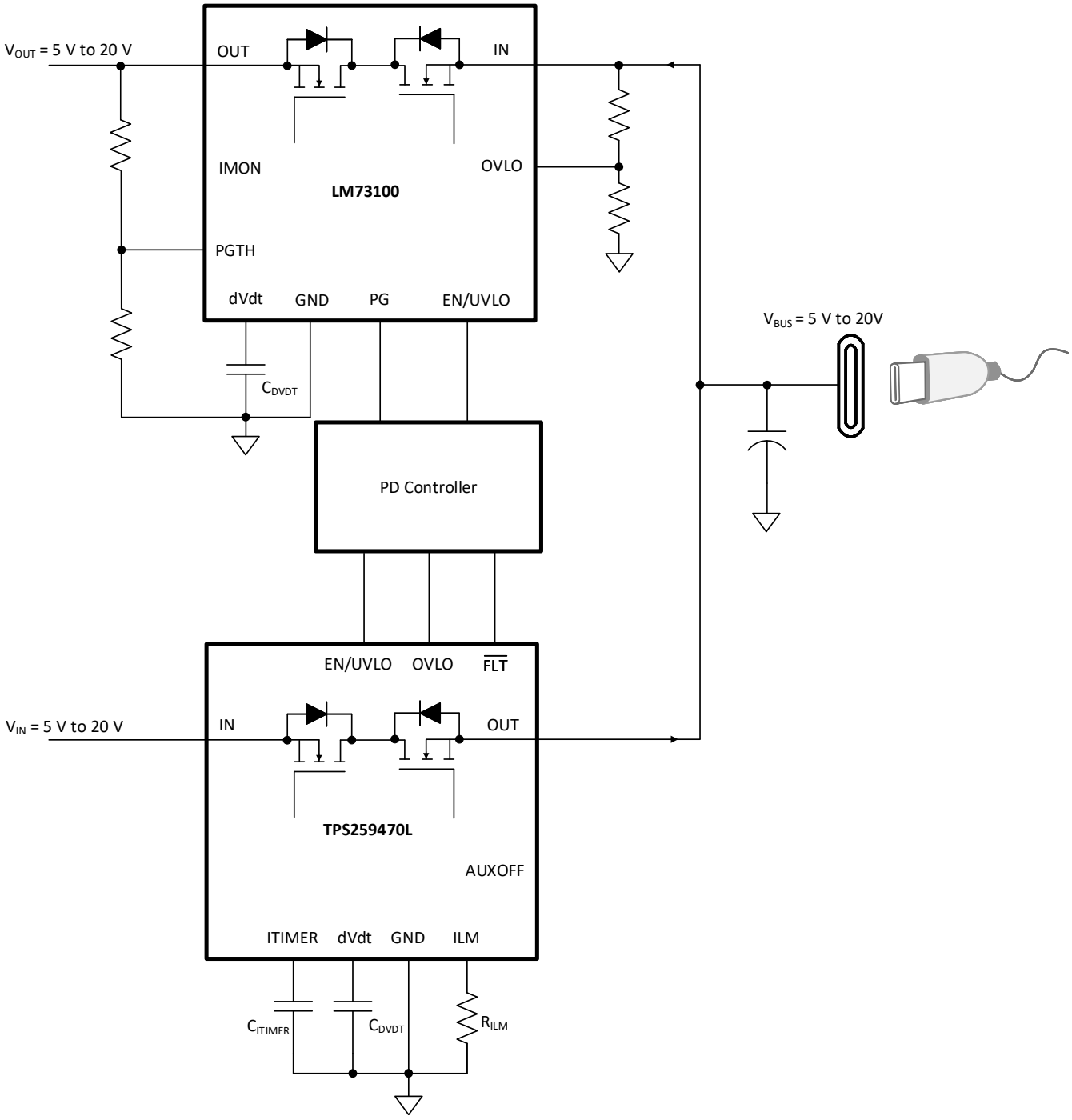
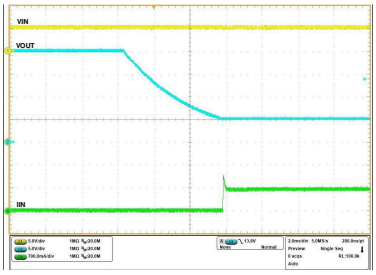


Figure 9-16. USB PD Port Protection

The waveform below shows the TPS259470x behavior when a 20-V source connected at the USB bus is suddenly disconnected. The TPS259470x is initially in reverse current blocking condition. As the bus voltage starts drooping, the TPS259470x exits the condition and performs a fast charge to restore the bus voltage above vSafe5V(min) within t_{SWRCB}, thereby meeting the USB FRS (Fast Role Swap) requirements.



V_{IN} = 5 V, C_{OUT} = 10 µF, R_{OUT} = 8 Ω, V_{OUT} = 20 V initially and then disconnected

Figure 9-17. TPS259470x 5-V Source Path - USB Fast Role Swap Response

9.7 Parallel Operation

Applications which need higher steady current can use 2 TPS25947xx devices connected in parallel as shown in Figure 9-18 below. In this configuration, the first device turns on initially to provide the inrush current limiting. The second device is held in an OFF state by driving its EN/UVLO pin low using the AUXOFF/PG signal of the first device. After the inrush sequence is complete, the first device asserts its AUXOFF/PG pin high and turns on the second device. The second device asserts its AUXOFF/PG signal to indicate when it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady state current.

After in steady state, both devices share current nearly equally. There can be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

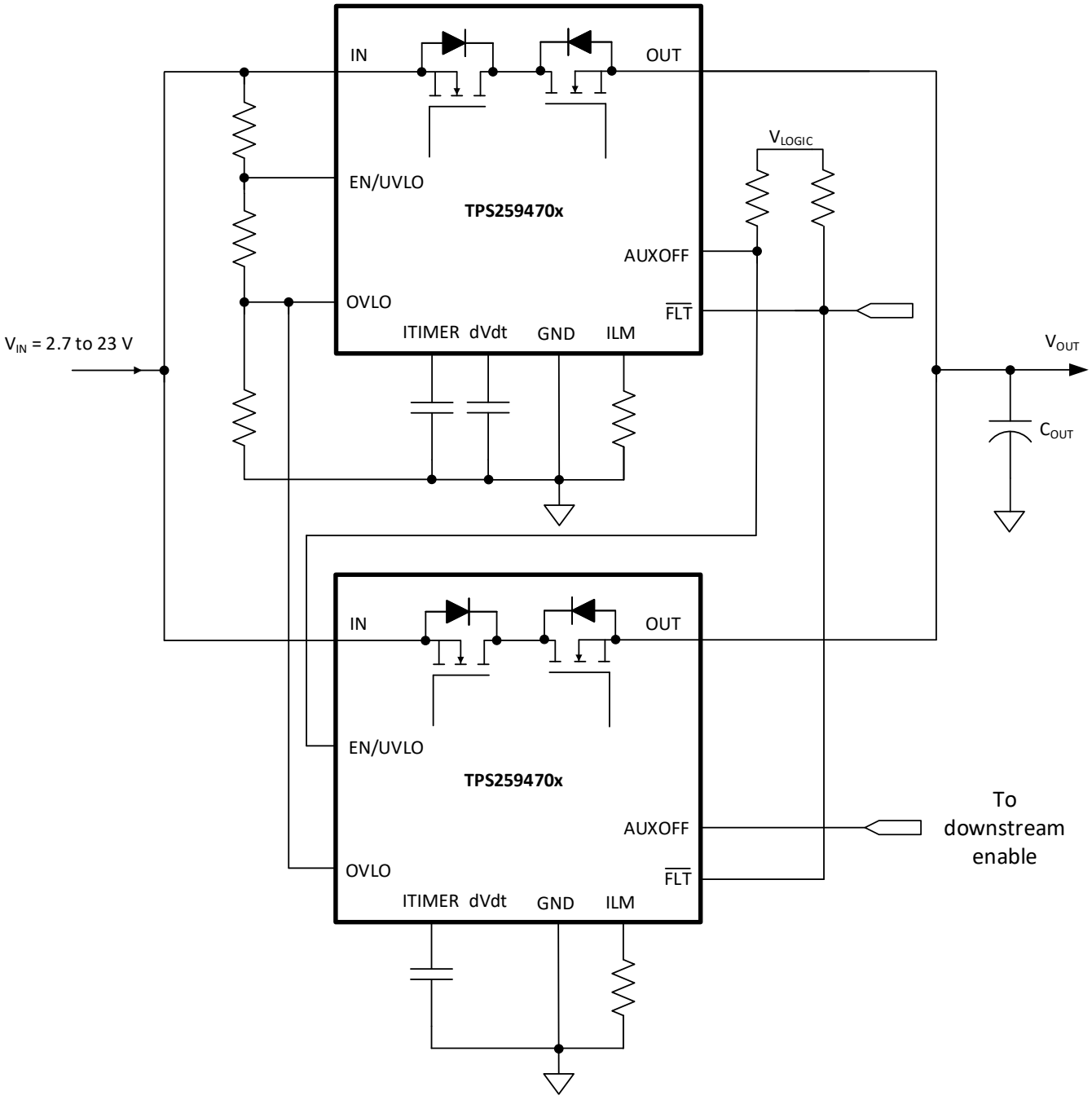


Figure 9-18. Two Devices Connected in Parallel for Higher Steady State Current Capability

The waveforms below illustrate the behavior of the parallel configuration during start-up as well as during steady state.

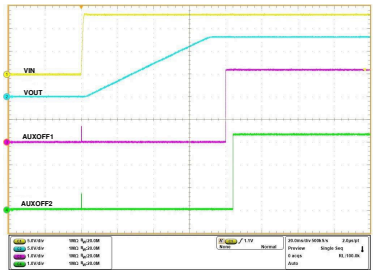


Figure 9-19. Parallel Devices Sequencing During Start-Up

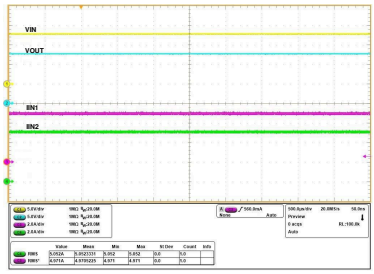


Figure 9-20. Parallel Devices Load Current During Steady State

10 Power Supply Recommendations

The TPS25947xx devices are designed for a supply voltage range of 2.7 V ≤ V_{IN} ≤ 23 V. TI recommends an input ceramic bypass capacitor higher than 0.1 µF if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

The lowest negative voltage the device can handle at the input is limited to –15 V or V_{OUT} –21 V, whichever is higher. Any low voltage signals (for example. EN/UVLO, OVLO, PGTH) derived from the input supply must have a sufficiently large pull-up resistor to limit the current through those pins to < 10 µA during reverse polarity conditions. Please refer to *Absolute Maximum Ratings* table for more details.

10.1 Transient Protection

In the case of a short-circuit and overload current limit when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating must be atleast twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

  The approximate value of input capacitance can be estimated with Equation 24:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \tag{24}$$

  where

  – V_{IN} is the nominal supply voltage.
  – • I_{LOAD} is the load current.
  – L_{IN} equals the effective inductance seen looking into the source.
  – C_{IN} is the capacitance present at the input.
- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

  Note

  If there is a likelihood of input reverse polarity in the system, TI recommends to use a bi-directional TVS, or a reverse blocking diode in series with the TVS.
- For applications such as USB-C ports where a powered cable can be plugged to the output of the device, there can be excess voltage stress from OUT to IN which exceeds the absolute maximum rating of the device. TI recommends to add a TVS diode from OUT to IN to clamp the voltage to a safe level.

The circuit implementation with optional protection components is shown in Figure 10-1.

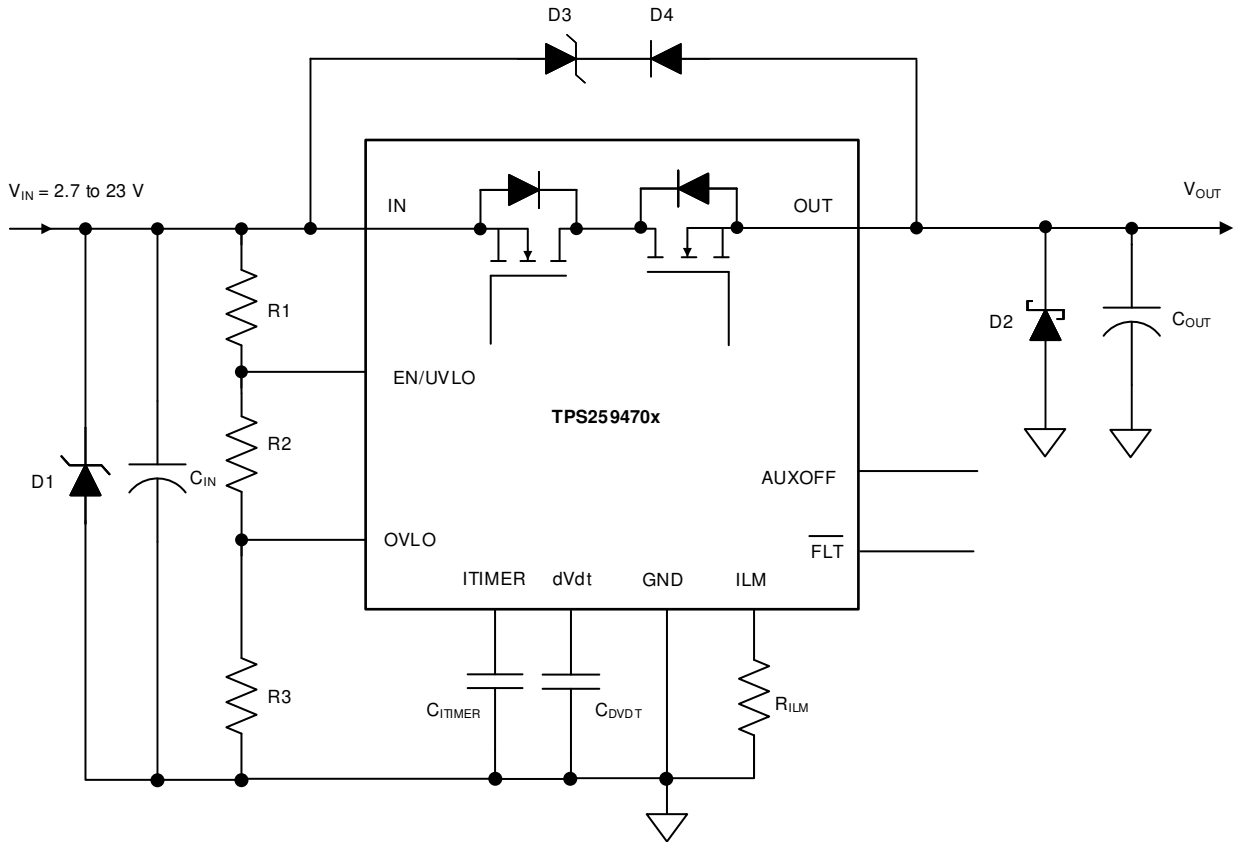


Figure 10-1. Circuit Implementation with Optional Protection Components

10.2 Output Short-Circuit Measurements

It is difficult to obtain repeatable and similar short-circuit testing results. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

11 Layout

11.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane doesn't carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane must be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient accross the IN and OUT pads and distribute current unformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{ILM}
  - C_{dVdT}
  - C_{ITIMER}
  - Resistors for the EN/UVLO, OVLO/OVCSEL and PGTH pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{ILM}, C_{ITIMER} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current limit , overcurrent blanking interval and soft start timing. TI recommends to keep parasitic capacitance on ILM pin below 50 pF to ensure stable operation. These traces must not have any coupling to switching signals on the board.
- Because the bias current on ILM pin directly controls the overcurrent protection behavior of the device, the PCB routing of this node must be kept away from any noisy (switching) signals.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads. TI recommends to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND terminal of the IC.

11.2 Layout Example

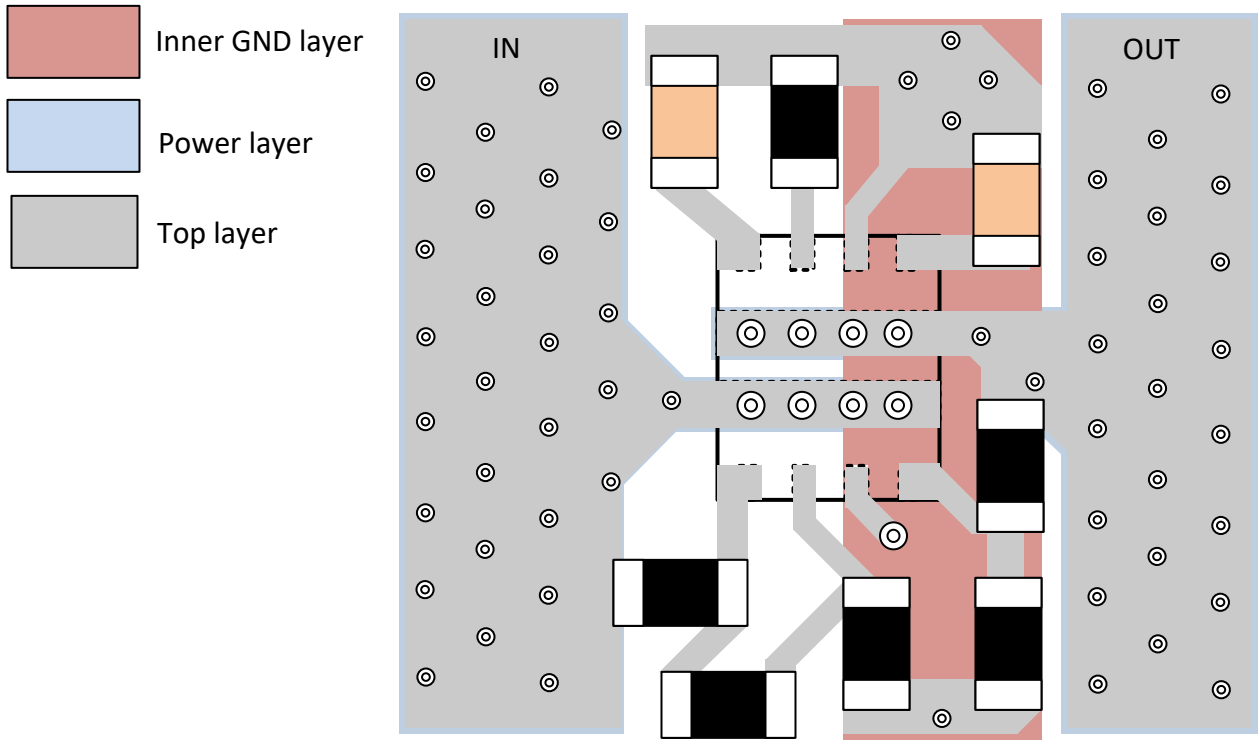


Figure 11-1. Layout Example - Single TPS259474x with PGTH Referred to OUT

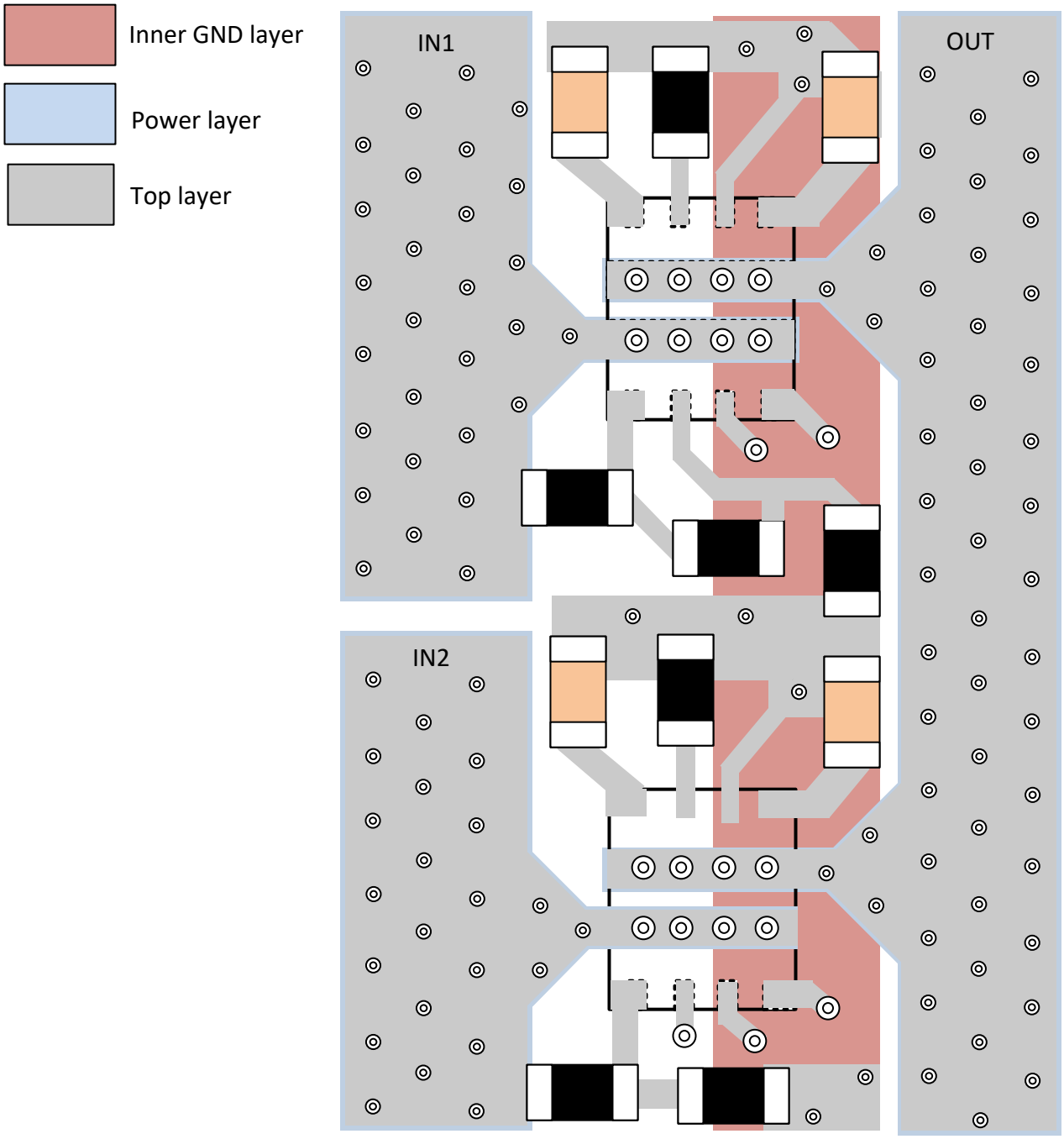


Figure 11-2. Layout Example - 2 × TPS259470x in PowerMUX Configuration

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS25947EVM eFuse Evaluation Board* user's guide
- Texas Instruments, *TPS25947xx Design Calculator*
- Texas Instruments, *Fast Role Swap, Linear ORing with TPS25947 and LM73100 in USB Type-C Systems* application brief
- Texas Instruments, *eFuses in Smart Electricity Meters* application brief

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS259470ARPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2A9H	Samples
TPS259470LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2A8H	Samples
TPS259472ARPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2ABH	Samples
TPS259472LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2AAH	Samples
TPS259474ARPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2ADH	Samples
TPS259474LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	2ACH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

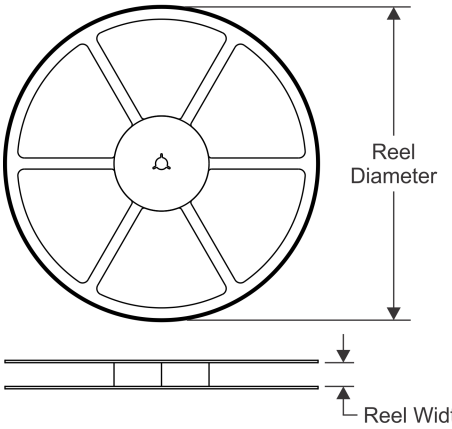
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

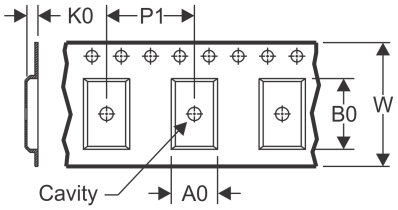
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

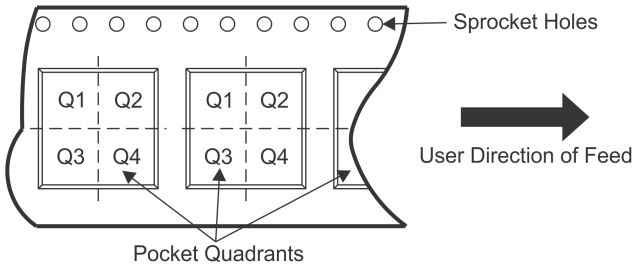


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

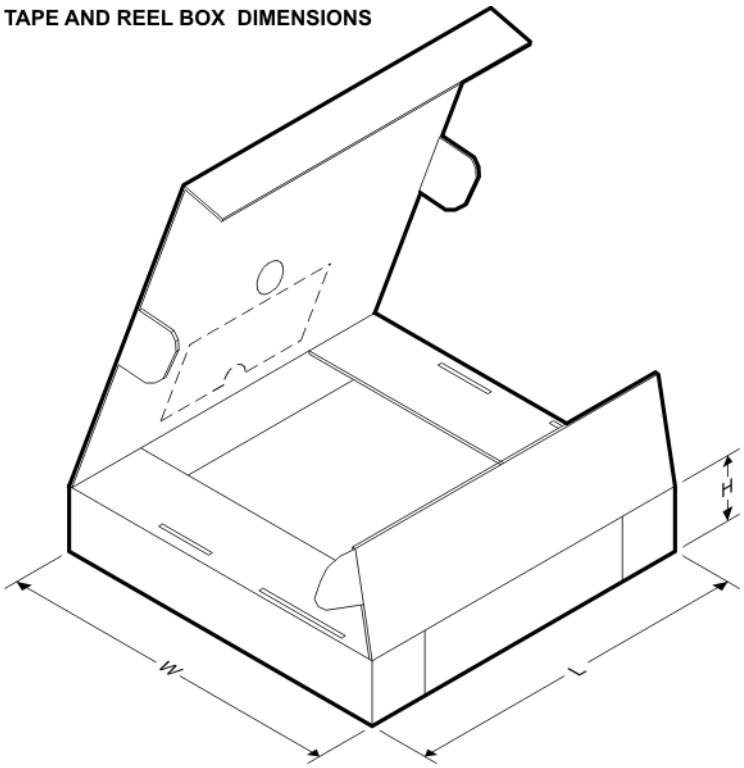
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS259470ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259470LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259472ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259472LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259474ARPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS259474LRPWR	VQFN-HR	RPW	10	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

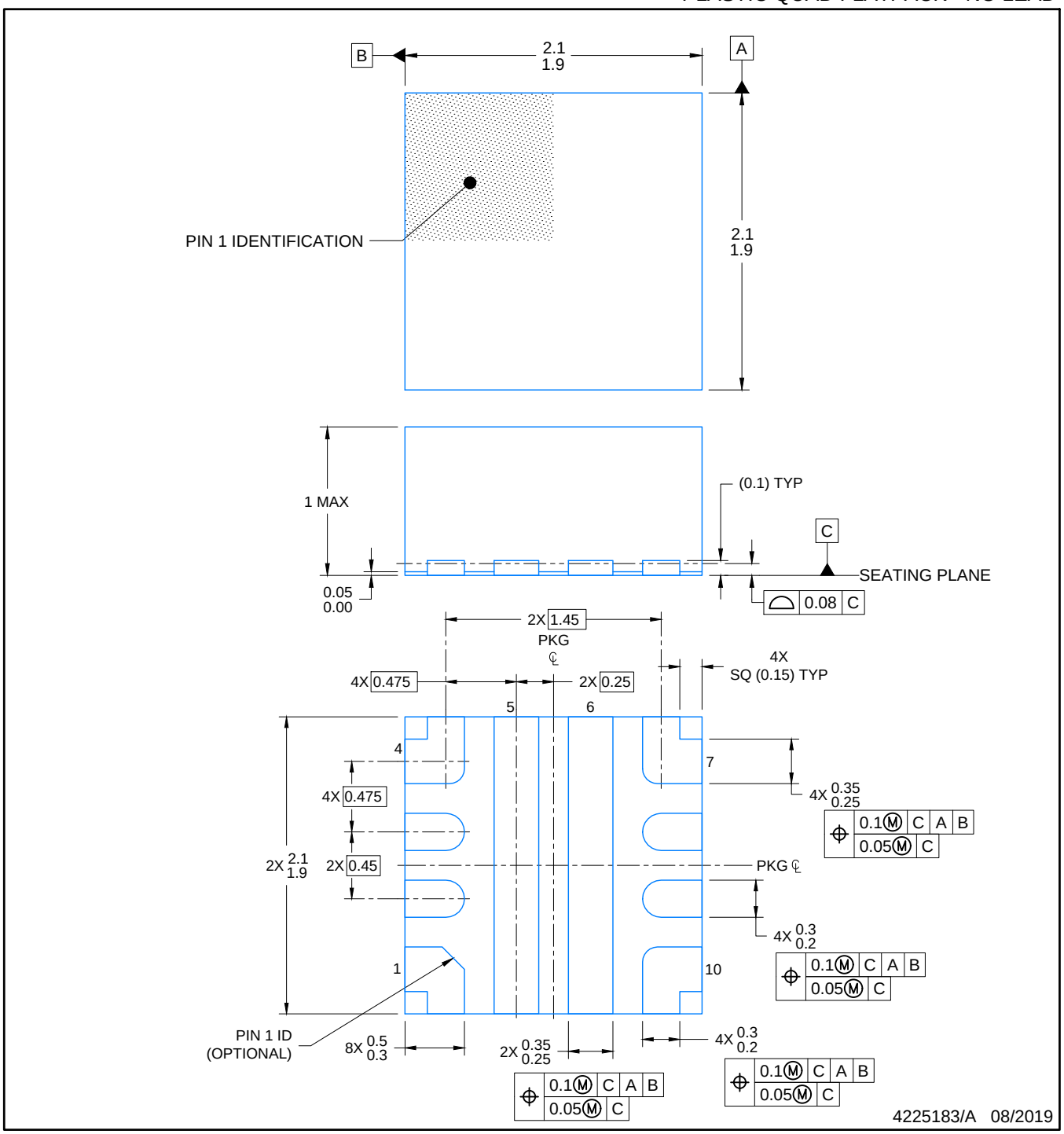
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS259470ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259470LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259472ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259472LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259474ARPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0
TPS259474LRPWR	VQFN-HR	RPW	10	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPW0010A

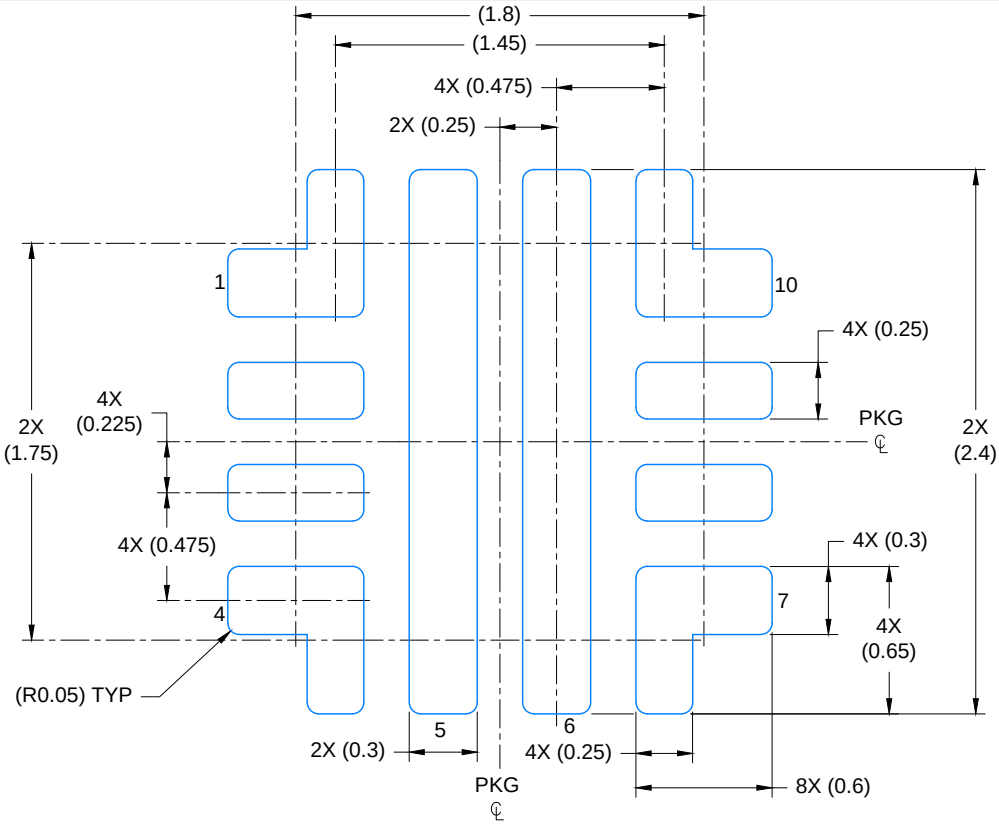
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



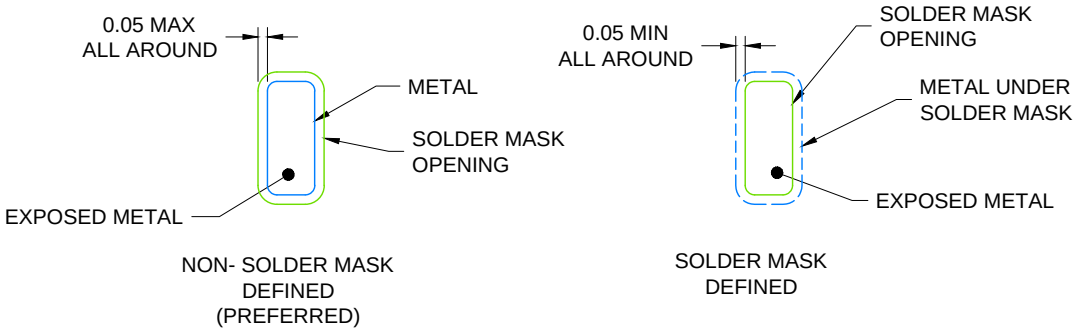
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



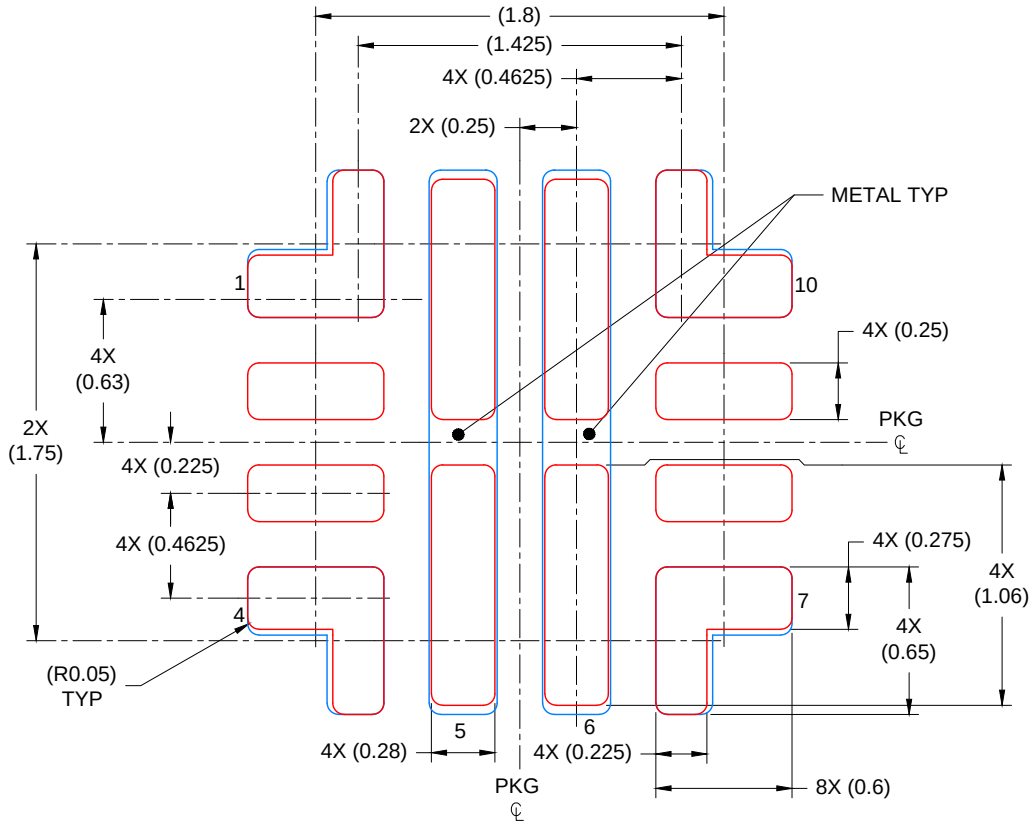
SOLDER MASK DETAILS

NOT TO SCALE

4225183/A 08/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

4225183/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265