

User's Guide

Power Stage Designer



ABSTRACT

Power Stage Designer™ software tool is a Java® based tool that helps engineers speed up their power supply designs by calculating voltages and currents for 21 topologies according to the user's inputs. Additionally, Power Stage Designer contains a Bode plotting tool and a helpful toolbox with various functions for power supply design. This document describes how the different features of Power Stage Designer can be used and also explains the calculations behind these functions.

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1 Topologies Window

To start a power supply design with Power Stage Designer, first select a topology from the Topology menu. The window changes and displays the schematic of the selected topology with a set of input fields and various output values. After entering the parameters of the power supply specification, Power Stage Designer suggests a value for the output inductance to stay below the entered current ripple requirement. For isolated topologies, the tool also displays a recommendation for the transformer turns ratio (TTR) based on the selected maximum duty cycle and suggests a value for the magnetizing inductance. Users can enter values of their choice and evaluate their impact on voltage and current waveforms and other parameters like on-time, off-time, and duty cycle.

Figure 1-1 shows the main window of Power Stage Designer displaying supported topologies.



Figure 1-1. Main Window of Power Stage Designer Displaying Supported Topologies

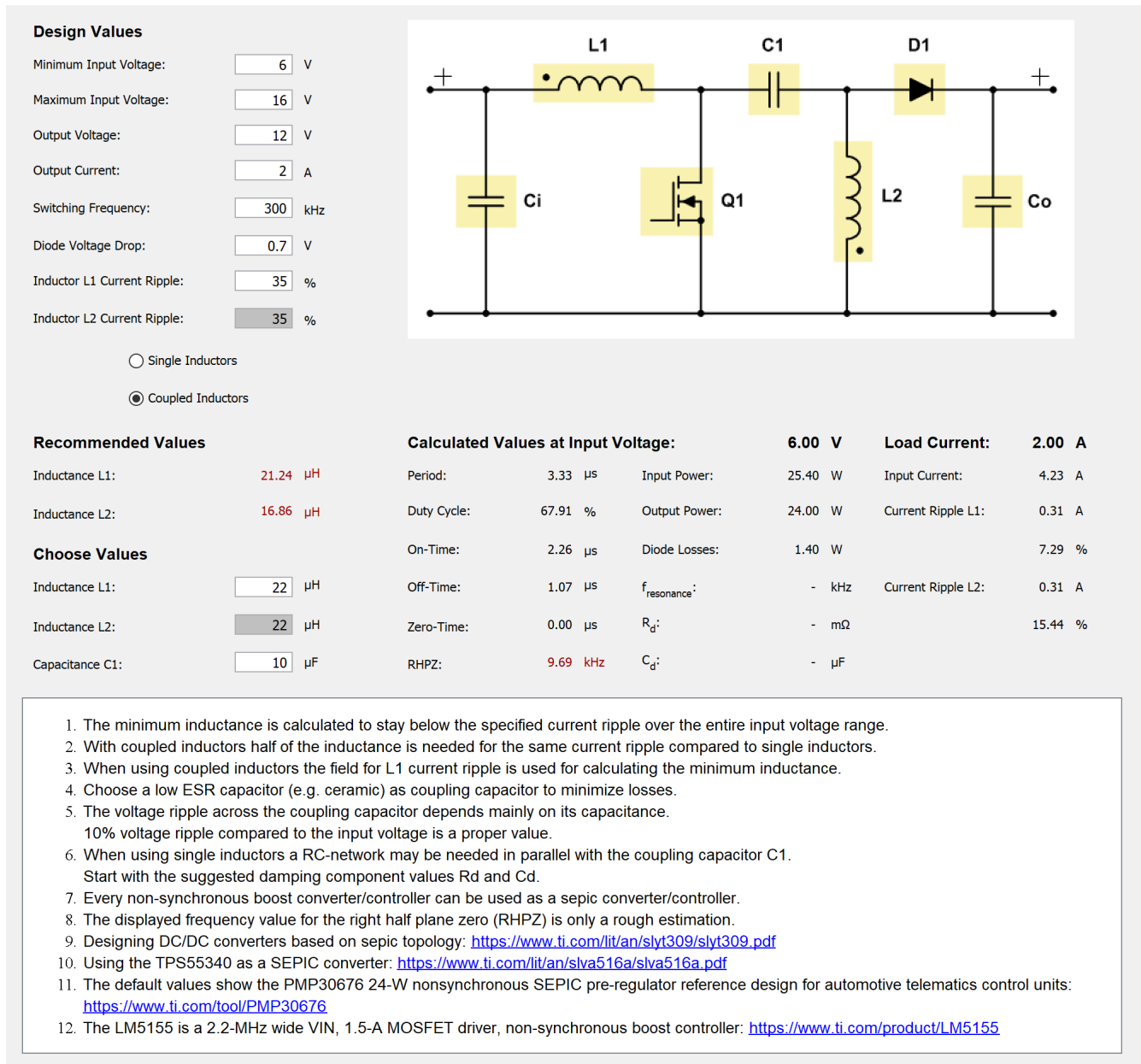


Figure 1-2. Topology Window for SEPIC

After clicking on one of the yellow highlighted components in the schematic (see Figure 1-2), a new window displays the voltage and current waveforms for this specific component (see Figure 1-3). Additional information like the minimum and maximum voltage, minimum and maximum current, as well as root mean square (RMS), average, and AC values for the current is also provided in this window. The input voltage can be changed across the entire input voltage range with a slider. For most topologies the load current can be altered in the range of 1% to 100% of the entered output current with a second slider. Some topology models do not support such a wide load current range, thus the load current slider can be changed only in the range of 50% and 100%. The Quasi-resonant Flyback model uses a fixed output power as base for all calculations. That is why the load current slider is not available for this specific topology.

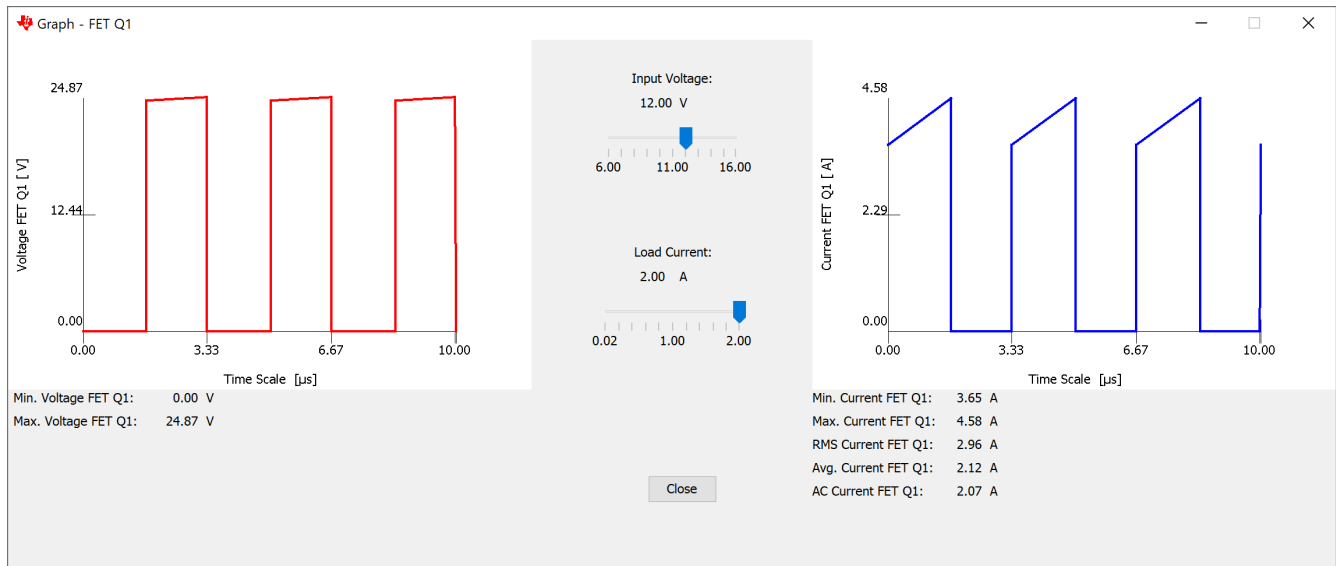


Figure 1-3. Graph Window for FET Q1 of a SEPIC Operating in CCM

Note

All equations used for calculations are ideal, with the only exception that the forward voltage of rectifier and freewheeling diodes is considered. For a collection of the equations behind certain topologies, see the [Power Topologies Handbook](#).

2 FET Losses Calculator

The FET Losses Calculator lets the user either compare two different FETs or calculate losses for the main FET and a synchronous rectifier in a hard-switching power stage. Figure 2-1 shows the FET Losses Calculator window.

Note

The Quasi-resonant Flyback, LLC-Half-Bridge, LLC-Full-Bridge, and Phase-Shifted Full-Bridge are resonant topologies. Manual inputs can provide more accurate results.

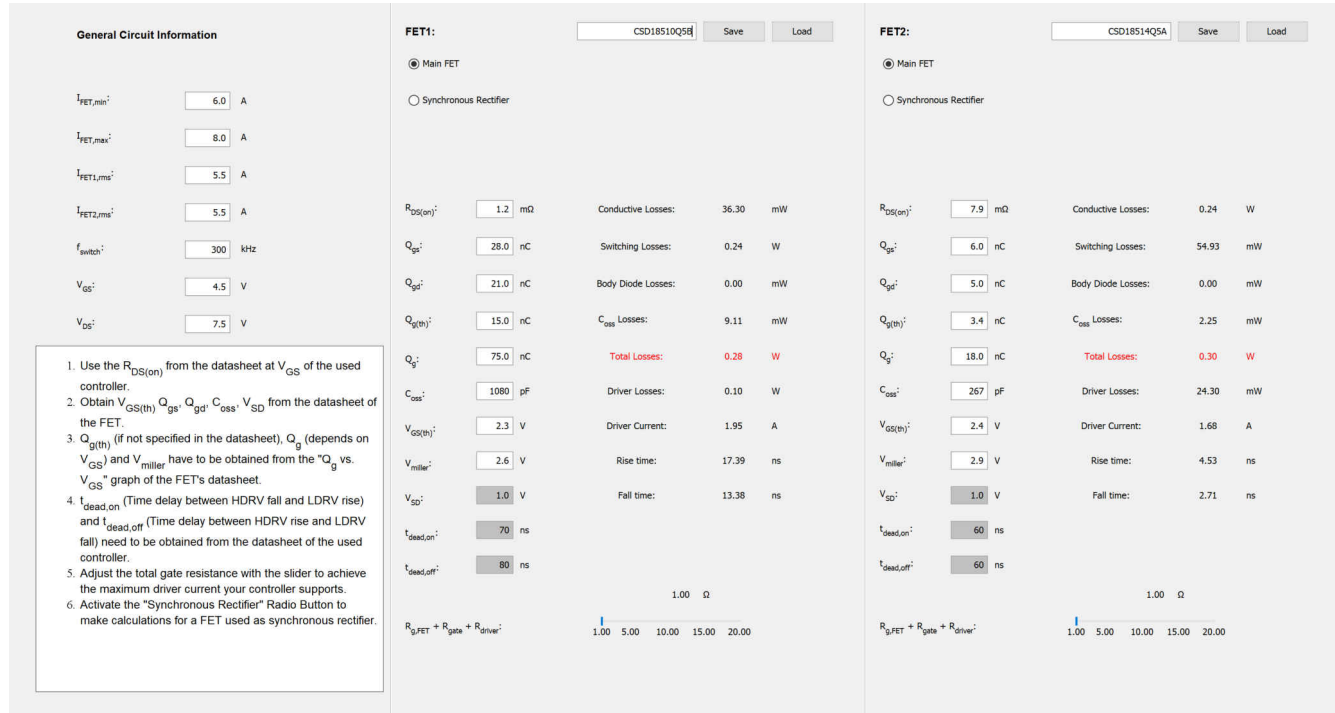


Figure 2-1. FET Losses Calculator Window

To attain the most accurate results, it is important to determine the gate drive voltage (V_{GS}) of the power management controller since the values for Q_g (which is relevant for driver losses) and $R_{DS(on)}$ are dependent on this voltage and must be obtained from graphs in the data sheet of the FET.

The different losses which can be seen in the FET of a power supply are conducted losses, switching losses, C_{oss} losses, and body diode losses. Reverse recovery losses are neglected, but can become significant at high switching frequencies.

Conductive losses:

$$P_{cond} = I_{FET,rms}^2 \times R_{DS(on)} \quad (1)$$

Switching losses:

$$t_{\text{rise}} = \frac{(Q_{\text{gs}} - Q_{\text{g(th)}}) \times R_{\text{g, total}}}{V_{\text{GS}} - \frac{V_{\text{miller}}}{2} - \frac{V_{\text{GS(th)}}}{2}} + \frac{Q_{\text{gd}} \times R_{\text{g, total}}}{V_{\text{GS}} - V_{\text{miller}}}$$

$$t_{\text{fall}} = \frac{Q_{\text{gd}} \times R_{\text{g, total}}}{V_{\text{miller}}} + \frac{(Q_{\text{gs}} - Q_{\text{g(th)}}) \times R_{\text{g, total}}}{\frac{V_{\text{miller}}}{2} + \frac{V_{\text{GS(th)}}}{2}}$$

$$P_{\text{switching}} = V_{\text{DS}} \times \frac{f_{\text{switch}}}{2} \times (t_{\text{rise}} \times I_{\text{FET, min}} + t_{\text{fall}} \times I_{\text{FET, max}}) \quad (2)$$

C_{oss} losses:

$$P_{\text{Coss}} = C_{\text{oss}} \times V_{\text{DS}}^2 \times \frac{f_{\text{switch}}}{2} \quad (3)$$

Body Diode losses:

$$P_{\text{body}} = V_{\text{SD}} \times f_{\text{switch}} \times (t_{\text{dead, on}} \times I_{\text{FET, min}} + t_{\text{dead, off}} \times I_{\text{FET, max}}) \quad (4)$$

The total losses for the main FET can be calculated as indicated in [Equation 5](#)

$$P_{\text{total}} = P_{\text{cond}} + P_{\text{switching}} + P_{\text{Coss}} \quad (5)$$

For synchronous rectifiers, the switching losses equal zero due to soft switching, but during the dead time the body diode is conducting. So the total losses result as indicated in [Equation 6](#):

$$P_{\text{total}} = P_{\text{cond}} + P_{\text{body}} + P_{\text{Coss}} \quad (6)$$

Additionally, driver losses occur in the power management controller, which can be calculated as shown in [Equation 7](#):

$$P_{\text{driver}} = Q_{\text{g}} \times V_{\text{GS}} \times f_{\text{switch}} \quad (7)$$

Power management controllers typically have a limited amount of gate drive current they can source and sink. Therefore, it is important to adjust the total resistance in the gate drive path so the resulting gate drive current is equal to or smaller than the limit in the data sheet.

3 Load Step Calculator

The *Load Step Calculator* enables the user to estimate the minimum required output capacitance to meet certain load transient requirement for power supplies that use current mode control or voltage mode control schemes.

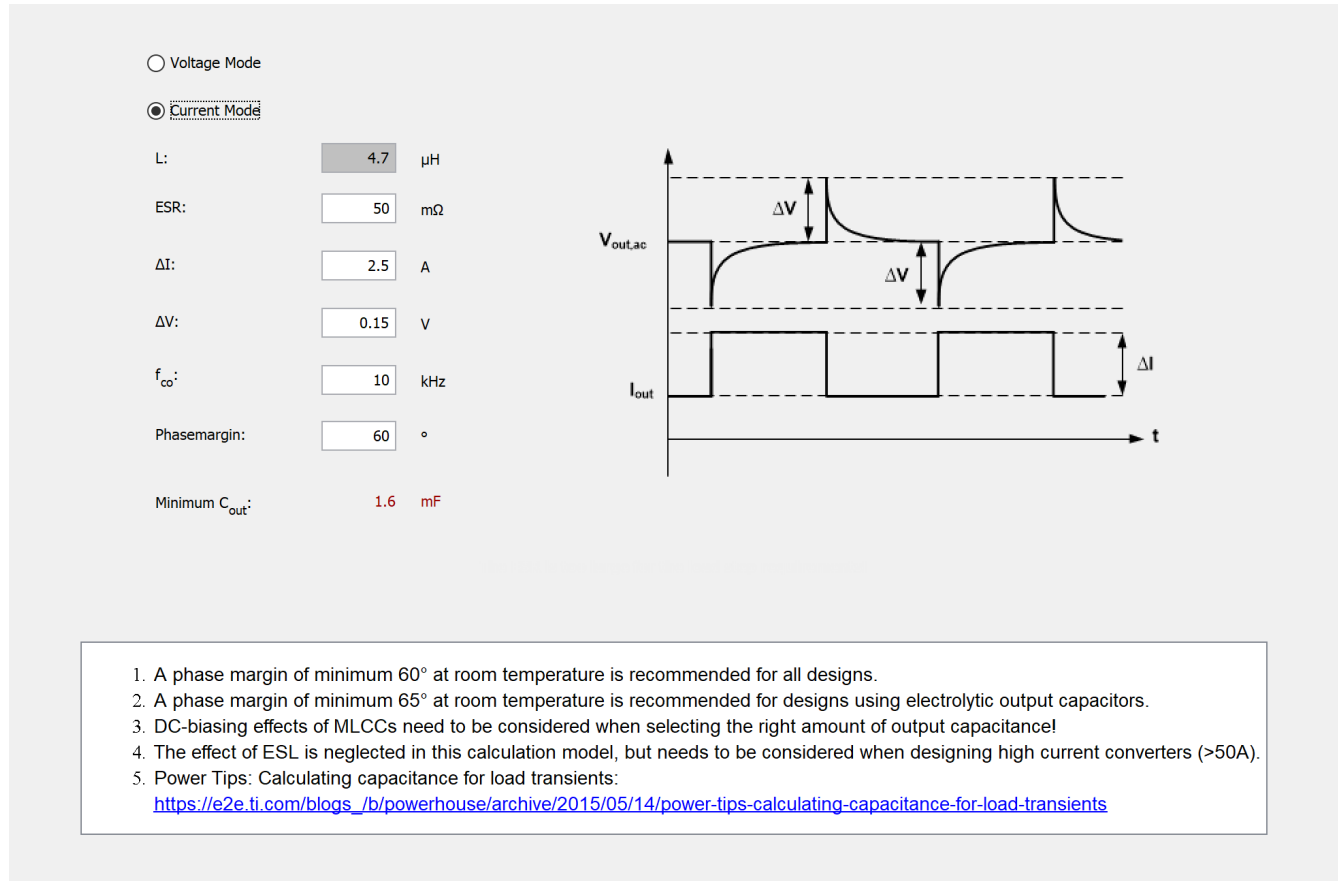


Figure 3-1. Load Step Calculator Window

Current Mode Control (CMC):

$$C_{out} = \frac{1}{2 \times \pi \times f_{co} \times \left(\frac{\Delta V_{out}}{\Delta I_{tran}} - ESR \right) \times \sqrt{2 - 2 \times \cos\left(\frac{PM \times \pi}{180^\circ}\right)}} \quad (8)$$

Voltage Mode Control (VMC):

$$C_{out} = \frac{1}{2 \times \pi \times f_{co} \times \left(\frac{\frac{1}{\frac{\Delta I_{tran}}{\Delta V_{out}} - \frac{1}{2 \times \pi \times f_{co} \times L}}}{\Delta V_{out}} - ESR \right) \times \sqrt{2 - 2 \times \cos\left(\frac{PM \times \pi}{180^\circ}\right)}} \quad (9)$$

4 Capacitor Current Sharing Calculator

When connecting different kinds of capacitors in parallel at the input or output of a power supply, the RMS current going through each capacitor is different as it depends on the impedance of the capacitors across the entire frequency range. For exact results for the RMS current per capacitor, impedances and currents must be calculated for all harmonics of the switching frequency. The RMS current for each harmonic must be derived with a Fast Fourier Transformation (FFT) of the total current signal based on the ratio between total impedance and single-capacitor impedance at that harmonic frequency.

Figure 4-1 shows the Capacitor Current Sharing Calculator.

Note

In Power Stage Designer, the impedances and the RMS currents are only calculated at the switching frequency. Thus, the resulting RMS currents are rough estimations.

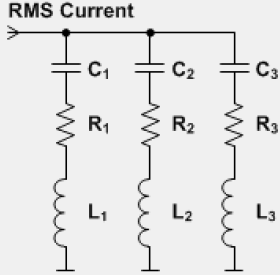
| | | | | | | | | |
|------------------------------|----------------------------------|-----|--|---------------------------------|----|----------------------|--------------------------------|----|
| Capacitance C ₁ : | <input type="text" value="0.1"/> | μF | ESR C ₁ : | <input type="text" value="4"/> | mΩ | ESL C ₁ : | <input type="text" value="4"/> | nH |
| Capacitance C ₂ : | <input type="text" value="1"/> | μF | ESR C ₂ : | <input type="text" value="4"/> | mΩ | ESL C ₂ : | <input type="text" value="4"/> | nH |
| Capacitance C ₃ : | <input type="text" value="100"/> | μF | ESR C ₃ : | <input type="text" value="40"/> | mΩ | ESL C ₃ : | <input type="text" value="4"/> | nH |
| RMS Current: | <input type="text" value="2.5"/> | A |  | | | | | |
| f _{switch} : | <input type="text" value="300"/> | kHz | | | | | | |
| RMS Current C ₁ : | 0.02 | A | | | | | | |
| RMS Current C ₂ : | 0.19 | A | <div style="border: 1px solid black; padding: 5px;"> <ol style="list-style-type: none"> The RMS current of each capacitor is calculated <u>only</u> at the entered switching frequency based on the impedance of each capacitor. Thus the displayed result is a rough estimation as impedances might be different at higher harmonics, but contribute to the overall rms current. Typical capacitor ESL values are between 1nH and 7nH. </div> | | | | | |
| RMS Current C ₃ : | 2.50 | A | | | | | | |

Figure 4-1. Capacitor Current Sharing Calculator

The impedance for one capacitor at the switching frequency (n can be 1, 2, or 3 and refers to the capacitor index) can be calculated as indicated in Equation 10:

$$Z_{cap,n} = ESR C_n + i \times \left(2 \times \pi \times f_{switch} \times ESL C_n - \frac{1}{2 \times \pi \times f_{switch} \times C_n} \right) \quad (10)$$

Typical ESL values for capacitors are from 1 nH to 7 nH. By assuming 6 nH/cm as parasitic inductance for a conductor, the inductance for a ceramic capacitor can be estimated by multiplying this value with the capacitor length. PCB traces and vias can increase this value slightly (see [1]).

The total impedance of three parallel capacitors at the switching frequency results as seen in [Equation 11](#):

$$Z_{\text{total}} = \frac{1}{\frac{1}{Z_{\text{cap},1}} + \frac{1}{Z_{\text{cap},2}} + \frac{1}{Z_{\text{cap},3}}} \quad (11)$$

The RMS current of one capacitor, while neglecting all other harmonics besides the switching frequency, can be calculated as seen in [Equation 12](#):

$$I_{\text{rms, cap},n} = I_{\text{rms, total}} \times \frac{|Z_{\text{total}}|}{|Z_{\text{cap},n}|} \quad (12)$$

5 AC/DC Bulk Capacitor Calculator

AC/DC power supplies typically require a bulk capacitor behind the input rectifier that provides a quasi-constant input voltage for the converter stage (see [Figure 5-1](#)). Power Stage Designer can calculate the minimum capacitance based on the desired minimum bulk voltage $V_{\text{bulk,min}}$, the maximum acceptable voltage ripple ΔV in percent, the input power P_{in} and the minimum line frequency $f_{\text{line,min}}$ (see [Equation 13](#)).

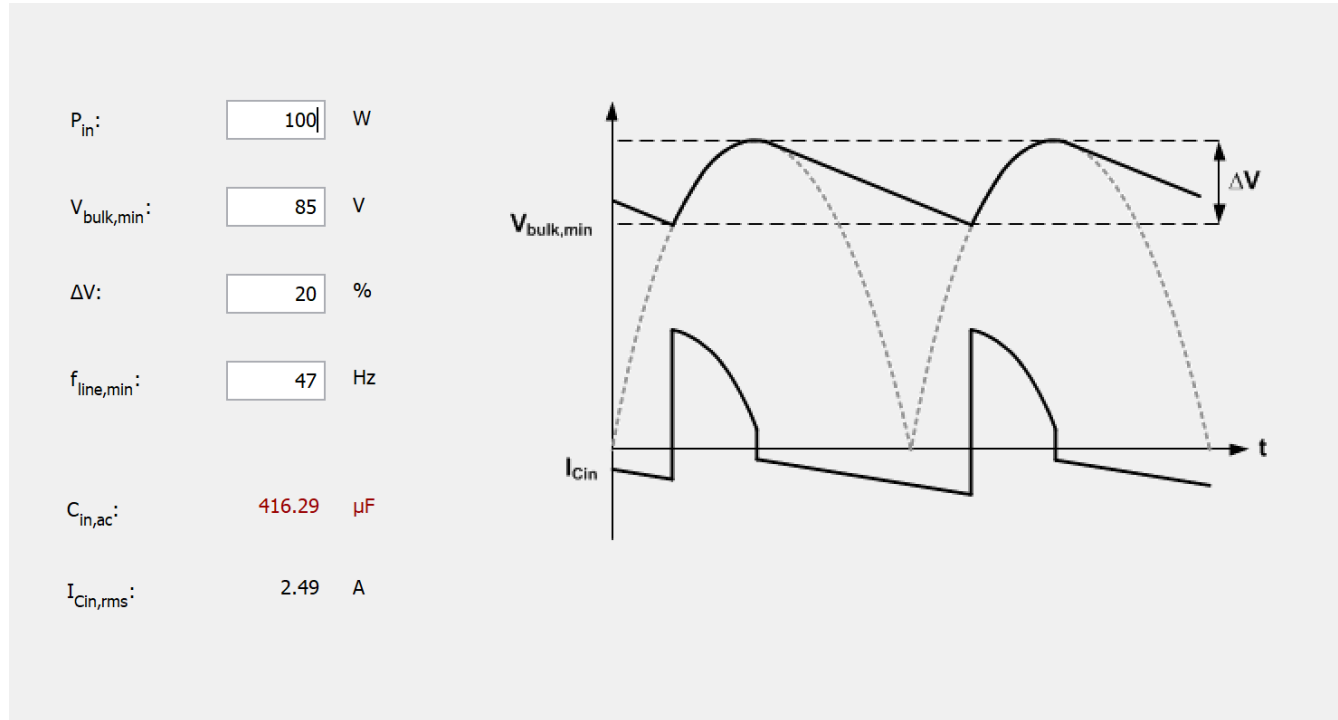


Figure 5-1. Bulk Capacitor Calculator for AC/DC Power Supplies Window

$$V_{\text{AC,min}} = \frac{V_{\text{bulk,min}}}{(1 - \Delta V) \times \sqrt{2}}$$

$$t_{\text{discharge}} = \frac{1}{4 \times f_{\text{line,min}}} + \frac{1}{2 \times \pi \times f_{\text{line,min}}} \times \sin^{-1}(1 - \Delta V)$$

$$t_{\text{charge}} = \frac{1}{4 \times f_{\text{line,min}}} - \frac{1}{2 \times \pi \times f_{\text{line,min}}} \times \sin^{-1}(1 - \Delta V)$$

$$C_{\text{bulk}} = \frac{2 \times P_{\text{in}} \times t_{\text{discharge}}}{V_{\text{bulk,min}}^2 \times \left(\left(\frac{1}{1 - \Delta V} \right)^2 - 1 \right)}$$

$$I_{\text{bulk,rms}} = \sqrt{\left(\frac{C_{\text{bulk}} \times V_{\text{bulk,min}} \times \left(\frac{1}{1 - \Delta V} - 1 \right)}{t_{\text{charge}} \times \sqrt{3}} \right)^2 + \left(\frac{P_{\text{in}}}{V_{\text{bulk,min}}} \right)^2} \quad (13)$$

6 RCD-Snubber Calculator for Flyback Converters

In Flyback converters the output voltage is reflected from the secondary to the primary side. Additionally, parasitics caused by the layout and the Flyback transformer leakage inductance can cause a voltage spike followed by ringing when the MOSFET is turning off. The voltage spike and the ringing can be limited by implementing an RCD-snubber circuit in parallel to the primary winding. The energy of the high-frequency ringing is dissipated in the RCD-network. The RCD-Snubber Calculator for Flyback converters in Power Stage Designer helps the designer choose the starting values for snubber resistor and capacitor based on the user's inputs, which follow:

- Sum of output voltage and rectifier voltage
- Flyback transformer turns ratio
- Leakage inductance
- Maximum primary current
- Switching frequency
- Permitted voltage overshoot as a factor
- Snubber capacitor voltage ripple in percent

Figure 6-1 shows the RCD-Snubber Calculator for Flyback Converters window.

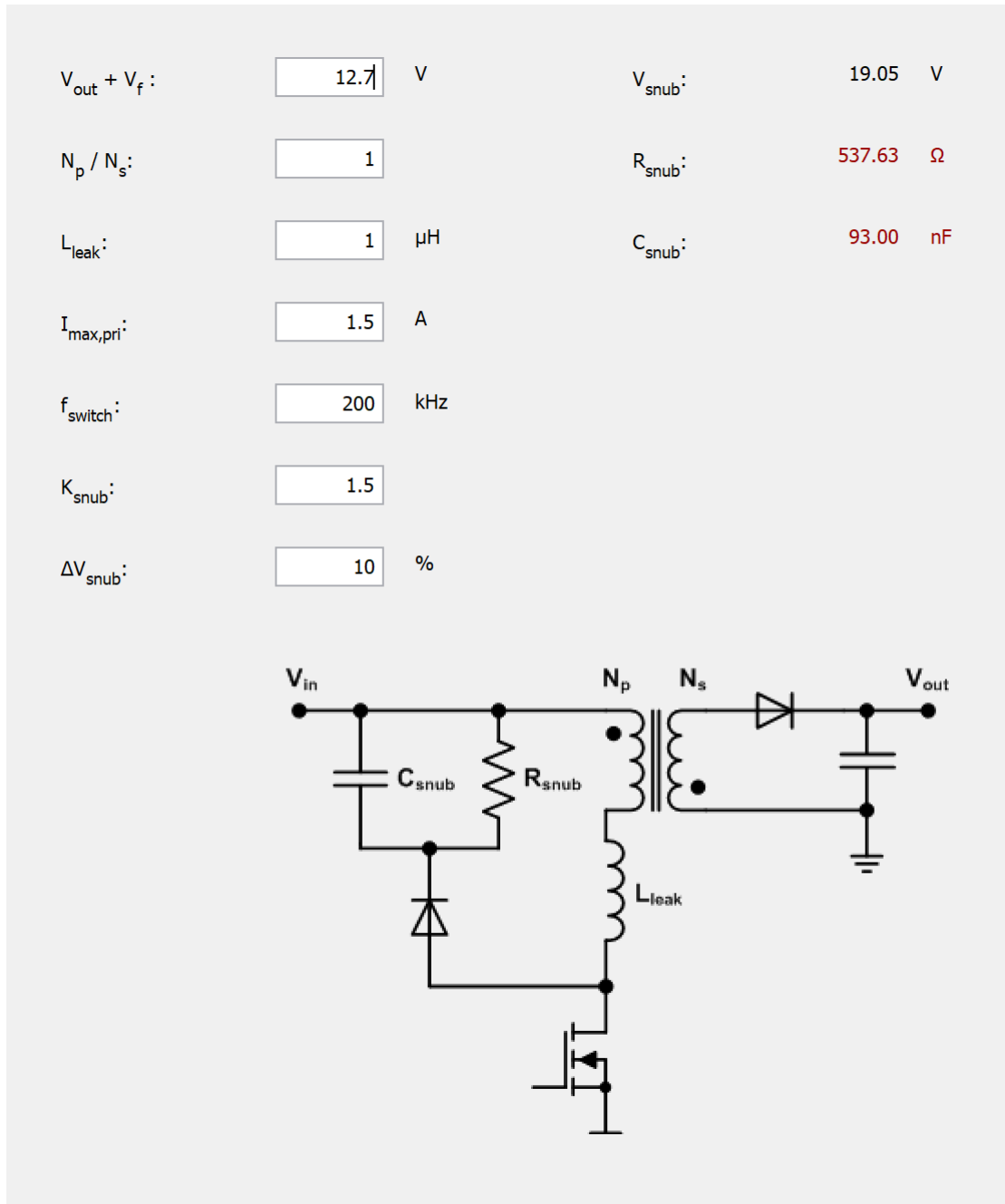


Figure 6-1. RCD-Snubber Calculator for Flyback Converters Window

V_{snub} is the reflected output voltage plus the permitted overshoot caused by transformer leakage inductance and switching node parasitics. Thus K_{snub} has a value greater than 1. TI recommends a value of 1.5 for most applications, permitting 50% overshoot (see [1]). See Equation 14.

$$V_{snub} = K_{snub} \times \frac{N_p}{N_s} \times (V_{out} + V_f) \quad (14)$$

Starting Snubber resistance:

$$R_{snub} = \frac{V_{snub}^2}{\frac{1}{2} \times L_{leak} \times I_{max, pri}^2 \times \frac{V_{snub}}{V_{snub} - \frac{N_p}{N_s} \times (V_{out} + V_f)} \times f_{switch}} \quad (15)$$

Starting Snubber capacitance:

$$C_{snub} = \frac{V_{snub}}{\Delta V_{snub} \times V_{snub} \times R_{snub} \times f_{switch}} \quad (16)$$

7 RC-Snubber Calculator

An RC-Snubber circuit is one option to reduce ringing in a switch mode power supply. Alternatives are the use of MOSFET gate resistors or a resistor in series with the bootstrap capacitor to slow down rise and/or fall times. With the RC-Snubber Calculator, Power Stage Designer helps the designer determine starting values for the snubber resistor and capacitor.

Figure 7-1 shows the RC-Snubber Calculator window.

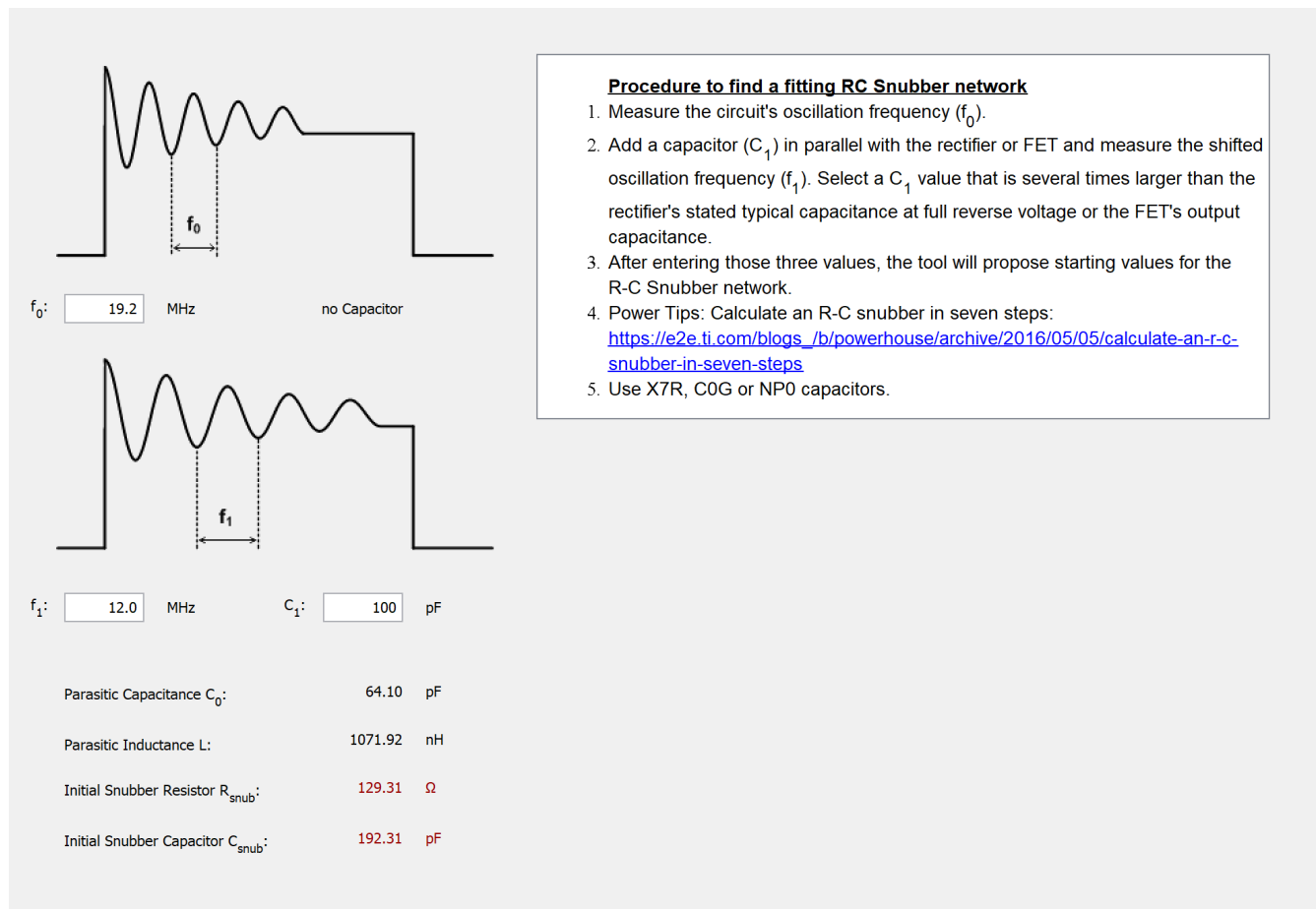


Figure 7-1. RC-Snubber Calculator Window

- Measure the oscillation frequency f_0 of the circuit without a snubber network.
- Add a capacitor C_1 in parallel with the rectifier or FET and measure the shifted oscillation frequency f_1 . Select a C_1 value that is several times larger than the stated typical capacitance of the rectifier at full reverse voltage or the output capacitance of the FET.
- After entering these three values, the tool will propose starting values for the R-C Snubber network.

Frequency shift ratio:

$$m = \frac{f_0}{f_1} \quad (17)$$

Parasitic capacitance:

$$C_0 = \frac{C_1}{m^2 - 1} \quad (18)$$

Parasitic inductance:

$$L = \frac{m^2 - 1}{(2 \times \pi \times f_0)^2 \times C_1} \quad (19)$$

Initial Snubber capacitance:

$$C_{\text{snub}} = 3 \times C_0 \quad (20)$$

Initial Snubber resistance:

$$R_{\text{snub}} = \sqrt{\frac{L}{C_0}} \quad (21)$$

8 Output Voltage Resistor Divider

The Output Voltage Resistor Divider Tool calculates the closest resistor values of the chosen E-Series to match the specified output voltage based on the entered reference voltage, reference voltage tolerance, and desired resistance value. The resistance value can be entered for the high-side (HS) or the low-side (LS) resistor. It is also possible to parallel two resistors to get more precise results. The following equations calculate the resulting output voltage while respecting resistor tolerances and reference voltage tolerances. However, because effects caused by the bias current are not considered for the calculations, these values are estimates.

Figure 8-1 shows the Output Voltage Resistor Divider Calculator window.

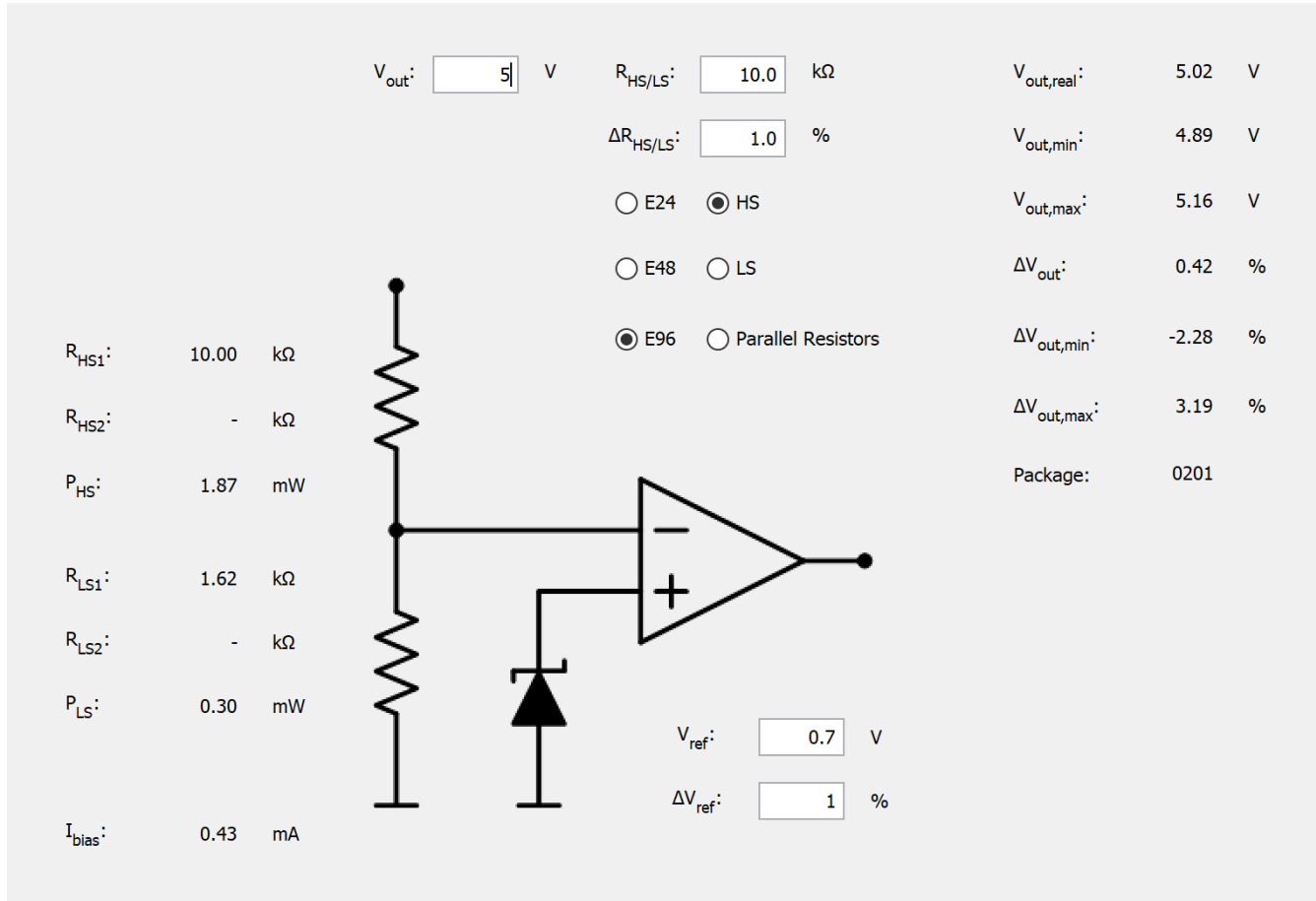


Figure 8-1. Output Voltage Resistor Divider Calculator Window

Effective output voltage with chosen resistance values (see Equation 22):

$$V_{\text{out,real}} = V_{\text{ref}} \times \frac{R_{\text{HS}} + R_{\text{LS}}}{R_{\text{LS}}}$$

$$\Delta V_{\text{out}} = \frac{V_{\text{out,real}} - V_{\text{out}}}{V_{\text{out}}} \quad (22)$$

Bias current:

$$I_{\text{bias}} = \frac{V_{\text{out,real}}}{R_{\text{HS}} + R_{\text{LS}}} \quad (23)$$

Worst-case minimum output voltage:

$$V_{\text{out, min}} = V_{\text{ref, min}} \times \frac{R_{\text{HS, min}} + R_{\text{LS, max}}}{R_{\text{LS, max}}}$$
$$\Delta V_{\text{out, min}} = \frac{V_{\text{out, min}} - V_{\text{out}}}{V_{\text{out}}} \quad (24)$$

Worst-case maximum output voltage:

$$V_{\text{out, max}} = V_{\text{ref, max}} \times \frac{R_{\text{HS, max}} + R_{\text{LS, min}}}{R_{\text{LS, min}}}$$
$$\Delta V_{\text{out, max}} = \frac{V_{\text{out, max}} - V_{\text{out}}}{V_{\text{out}}} \quad (25)$$

9 Dynamic Analog Output Voltage Scaling

If the output voltage of a power supply must be adjustable, add a third resistor to the feedback resistor divider and apply an analog voltage to this resistor (for example, with the DAC of a microcontroller). The analog signal can also be provided by smoothing a PWM signal with a low-pass filter. After entering the minimum output voltage, maximum output voltage, reference voltage, maximum adjusting voltage signal, and the desired value for the top feedback resistor, Power Stage Designer calculates the required bottom feedback resistance and the adjusting voltage signal series resistance, as well as the minimum bias current going through the top feedback resistor.

Figure 9-1 shows the Dynamic Output Voltage Scaling Calculator window.

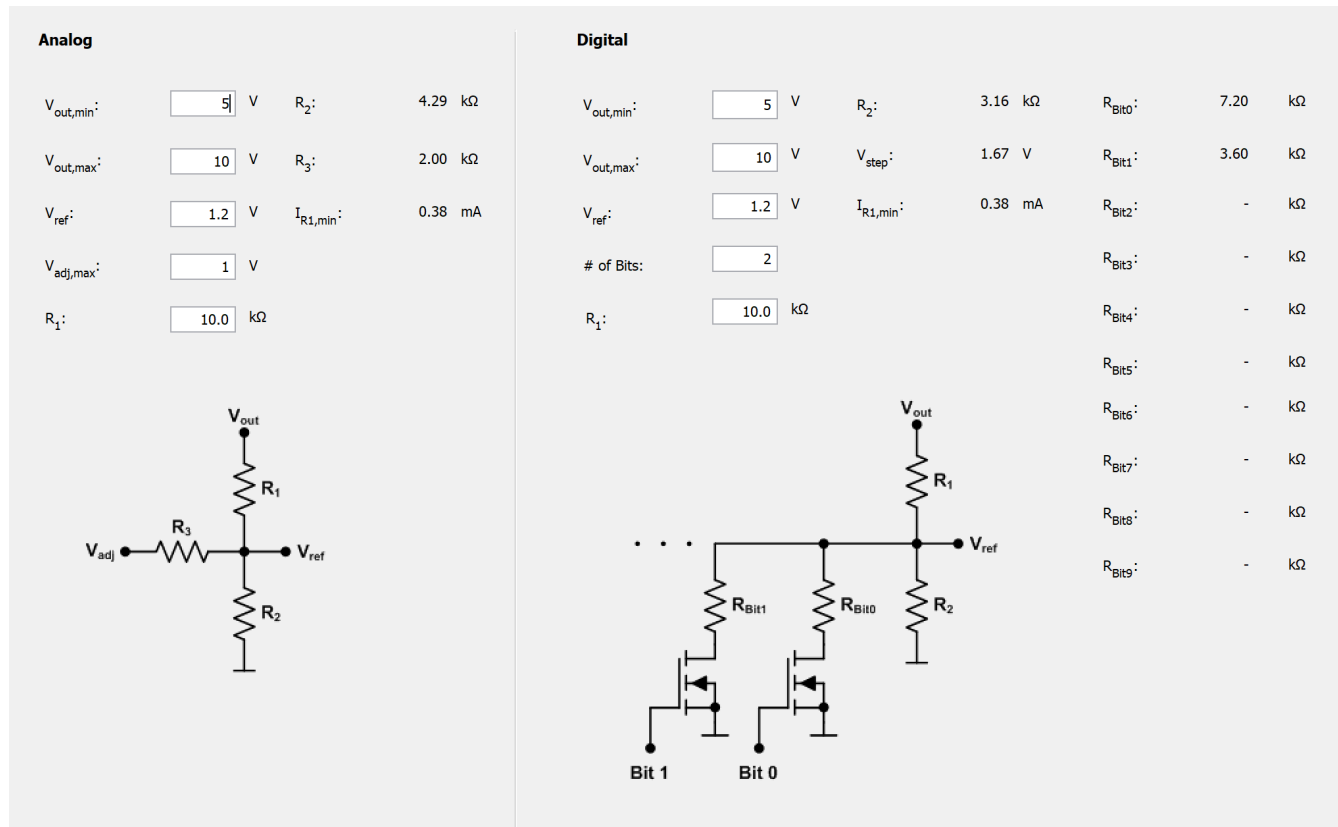


Figure 9-1. Dynamic Output Voltage Scaling Calculator Window

$$I_{R1, \min} = \frac{V_{\text{out, min}} - V_{\text{ref}}}{R_1}$$

$$R_3 = \frac{R_1 \times V_{\text{adj, max}}}{V_{\text{out, max}} - V_{\text{ref}} - R_1 \times I_{R1, \min}}$$

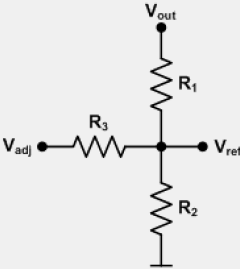
$$R_2 = \frac{R_1 \times R_3 \times V_{\text{ref}}}{R_3 \times V_{\text{out, max}} - R_3 \times V_{\text{ref}} - R_1 \times V_{\text{ref}}} \quad (26)$$

10 Dynamic Digital Output Voltage Scaling

Dynamic output voltage adjustment can also be achieved by applying GPIO signals to an array of resistors and signal FET combinations in parallel with the low-side resistor of the feedback divider. For most cases, a microcontroller output in open-drain configuration can be used instead of an external signal FET because it is already part of the system. Power Stage Designer calculates the low-side feedback resistor, the voltage per step, the bias current, and the series resistance for each bit based on the output voltage range, the reference voltage, the number of bits, and the value of the high-side feedback resistor.

Figure 10-1 shows the Dynamic Output Voltage Scaling Calculator window.

| Analog | | | | Digital | | | | | |
|-----------------|--|----------------|-----------------|-----------------|--|----------------|-----------------|--------------|-----------------|
| $V_{out,min}$: | <input type="text" value="5"/> V | R_2 : | 4.29 k Ω | $V_{out,min}$: | <input type="text" value="5"/> V | R_2 : | 3.16 k Ω | R_{Bit0} : | 7.20 k Ω |
| $V_{out,max}$: | <input type="text" value="10"/> V | R_3 : | 2.00 k Ω | $V_{out,max}$: | <input type="text" value="10"/> V | V_{step} : | 1.67 V | R_{Bit1} : | 3.60 k Ω |
| V_{ref} : | <input type="text" value="1.2"/> V | $I_{R1,min}$: | 0.38 mA | V_{ref} : | <input type="text" value="1.2"/> V | $I_{R1,min}$: | 0.38 mA | R_{Bit2} : | - k Ω |
| $V_{adj,max}$: | <input type="text" value="1"/> V | | | # of Bits: | <input type="text" value="2"/> | | | R_{Bit3} : | - k Ω |
| R_1 : | <input type="text" value="10.0"/> k Ω | | | R_1 : | <input type="text" value="10.0"/> k Ω | | | R_{Bit4} : | - k Ω |
| | | | | | | | | R_{Bit5} : | - k Ω |
| | | | | | | | | R_{Bit6} : | - k Ω |
| | | | | | | | | R_{Bit7} : | - k Ω |
| | | | | | | | | R_{Bit8} : | - k Ω |
| | | | | | | | | R_{Bit9} : | - k Ω |



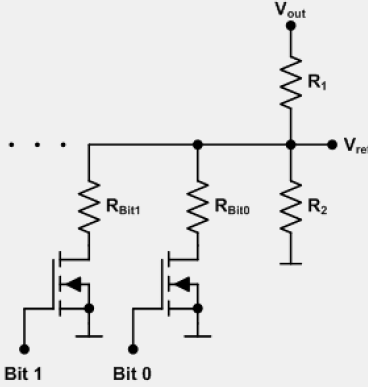


Figure 10-1. Dynamic Output Voltage Scaling Calculator Window

$$I_{R1,min} = \frac{V_{out,min} - V_{ref}}{R_1}$$

$$R_2 = \frac{R_1 \times V_{ref}}{V_{out,min} - V_{ref}}$$

$$V_{step} = \frac{V_{out,max} - V_{out,min}}{2^{Bits} - 1}$$

$$R_{Bit n} = \frac{1}{\frac{V_{out,min} + 2^{Bit} \times V_{step} - V_{ref}}{R_1 \times V_{ref}} - \frac{1}{R_2}} \quad (27)$$

The LM10011 is a device that has this feature integrated for 4/6-Bit VID.

11 Unit Converter

The Unit Converter can help power supply designers convert typical parameters related to power supplies. These parameters are magnetic flux, gain, length, weight, airstream, PCB copper thickness, and temperature. Figure 11-1 shows the Unit Converter window.

| | | | |
|-------------|-----------------------------------|--|--------|
| Flux | <input type="text" value="1000"/> | G to mT | 100.0 |
| Gain | <input type="text" value="10"/> | factor to Voltage dB | 20.0 |
| Length | <input type="text" value="100"/> | mil to mm | 2.54 |
| Weight | <input type="text" value="1"/> | oz to g | 28.349 |
| Airstream | <input type="text" value="100"/> | lfm to m/s | 0.508 |
| PCB Copper | <input type="text" value="1"/> | oz to μm | 35.0 |
| Temperature | <input type="text" value="20"/> | $^{\circ}\text{C}$ to $^{\circ}\text{F}$ | 68.0 |
| Power | <input type="text" value="200"/> | kW to hp | 272 |
| Torque | <input type="text" value="1000"/> | Nm to lb-ft | 737.56 |
| Speed | <input type="text" value="250"/> | km/h to mph | 155.34 |

Figure 11-1. Unit Converter Window

12 Loop Calculator

The Loop Calculator can help power supply designers with the compensation network for voltage mode controlled (VMC) buck converters or current mode controlled (CMC) buck, boost, inverting buck-boost, forward, and flyback converters operating in continuous conduction mode (CCM). The transfer functions have been simplified, thus the results give a first-order approximation of how the Bode plot of the power supply will appear. Figure 12-1 shows the Loop Calculator window.

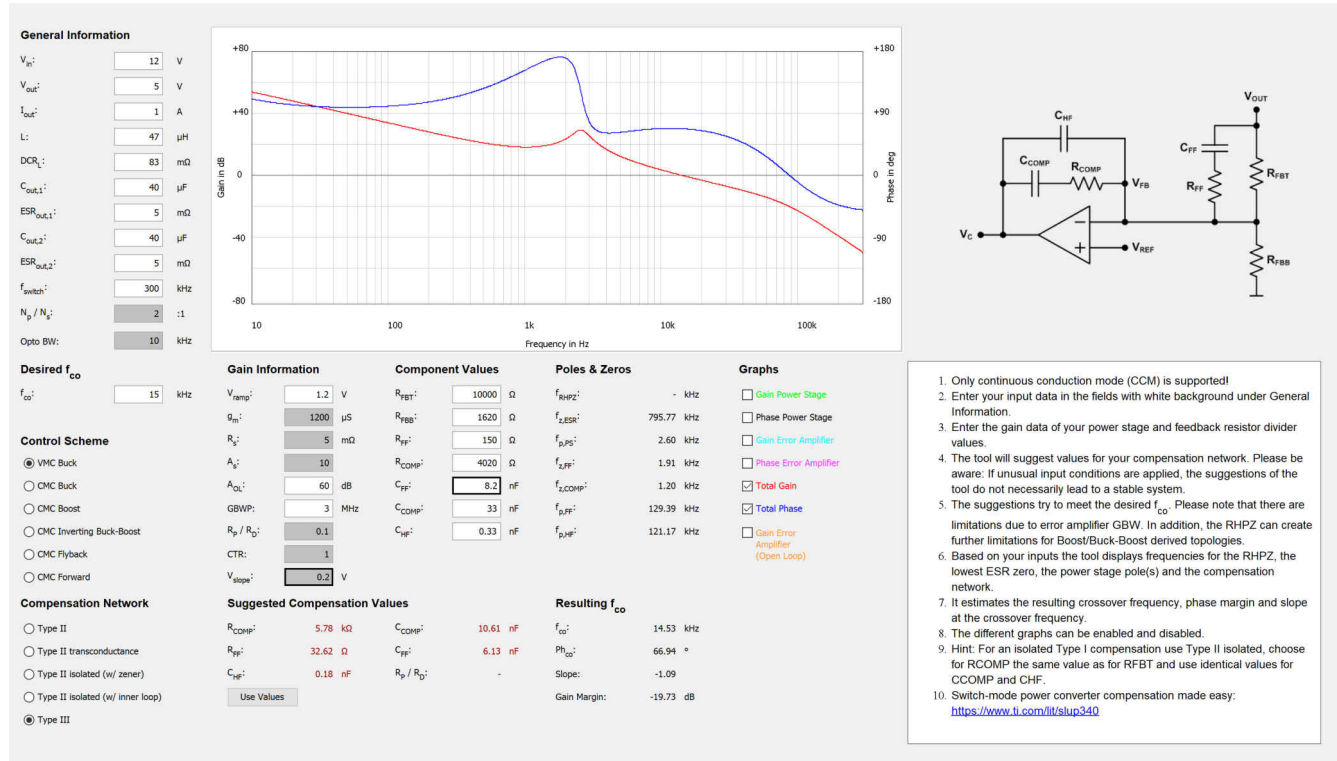


Figure 12-1. Loop Calculator Window

The following steps apply when using the Loop Calculator.

1. Select the topology/control scheme and the type of compensation for the design with the radio buttons in the bottom-left corner. Typically, only the VMC buck needs a Type III Compensation. For all CMC topologies, a Type II Compensation is usually sufficient.
2. Fill in all input fields with white background. If the Loop Calculator is started from one of the supported topologies, applicable values from the topologies window will directly transfer to the Loop Calculator window.
3. Under General Information (from the schematic) sum the capacitance of the same output capacitor types and calculate their effective ESR. The DC-biasing effect for ceramic capacitors must be considered because it can have a major impact on the accuracy of the gain and phase plot of the power stage.
4. Enter the Gain Information (from the schematic and the data sheet for the controller).
5. Fill in the values for RFBT and RFBB. With this information the Loop Calculator can suggest values for the compensation network of the entered power supply design.

The compensation network suggestions are calculated as follows:

CAUTION

If unusual input conditions are applied, the suggestions of the tool do not necessarily lead to a stable system.

- Compensation zeroes are placed on the pole of the transfer function of the power stage (L and C_{out} double pole for VMC, R_{out} and C_{out} single pole for CMC).
- Compensation poles are placed on the lower of either half of the switching frequency or the ESR zero for Buck derived topologies.
- Compensation poles are placed on the lower of either the right half plane zero (RHPZ) frequency or the ESR zero frequency for Boost/Buck-Boost derived topologies.
- The maximum achievable crossover frequency is approximately two decades below the GBWP (gain bandwidth product) of the error amplifier. The gain of the compensation network should never go above the open loop gain of the error amplifier. Otherwise, the error amplifier will be clipping.
- For Boost/Buck-Boost derived topologies the desired crossover frequency is automatically set to 1/5 of the RHPZ frequency.

12.1 Inputs

Table 12-1 lists general information.

Table 12-1. General Information

| | |
|--------------------------------|--|
| V _{in} | Input voltage |
| V _{out} | Output voltage |
| I _{out} | Load current |
| L | Inductance / Flyback primary inductance |
| DCR _L | Inductor DC resistance |
| C _{out,1} | Capacitance output capacitor 1 For ceramic capacitors use the capacitance at the DC bias voltage. |
| ESR _{out,1} | Equivalent series resistance output capacitor 1 |
| C _{out,2} | Capacitance output capacitor 2 For ceramic capacitors use the capacitance at the DC bias voltage. |
| ESR _{out,2} | Equivalent series resistance output capacitor 2 |
| f _{switch} | Switching frequency |
| N _p /N _s | Transformer turns ratio |
| Opto BW | Optocoupler bandwidth |

Table 12-2 lists gain information.

Table 12-2. Gain Information

| | |
|--------------------------------|--|
| V _{ramp} | PWM ramp voltage |
| G _m | Error amplifier transconductance |
| A _s | Current-sense amplifier gain |
| R _s | Current-sense resistance |
| A _{OL} | Error amplifier open-loop gain |
| GBWP | Error amplifier gain bandwidth product |
| R _p /R _D | Optocoupler transfer ratio |
| CTR | Current Transfer Ratio |
| V _{slope} | Slope compensation voltage |
| SLM | Slope compensation multiplier |

Current-sense gain A_s and current-sense resistance R_s :

For converters with integrated current-sensing circuits, sometimes there are no specific values for A_s and R_s in the data sheet. Instead, a value for $G_{m,ps}$ (can also appear as “COMP to switch current transconductance”) is typically displayed. Equation 28 shows the relationship between these values.

$$G_{m,ps} = \frac{1}{A_s \times R_s} \quad (28)$$

In this case, values for A_s and R_s must be chosen to have the stated $G_{m,ps}$ as a result. (For example, use the $R_{DS(on)}$ of the internal FET for R_s and calculate A_s from Equation 28.)

The input field for V_{slope} offers the user the option to use either V_{slope} or a slope compensation multiplier (SLM), in case the value for V_{slope} cannot be calculated by the designer (for example, because of internal slope compensation). Switching between these two variables can be done by right-clicking on the V_{slope} /SLM input field.

V_{slope} :

- Calculate the value for V_{slope} with the equations from the data sheet. If the device has internal slope compensation, a value for V_{slope} is typically given in the Electrical Characteristics section.

SLM:

- SLM is a variable to simulate the slope compensation under certain circumstances. How it affects calculations can be found in the subsections for each topology.
- Ideal slope compensation will be calculated with a value of 1.
- Values greater than 1 show how the converter will drift to VMC with increasing values of SLM, as the information of the original current signal will be lost at a certain point. A Type III compensation network would then be necessary to compensate the converter.
- Values in the range from 0 to 1 simulate conditions when not enough slope compensation is present, and a resonance will become visible at half the switching frequency caused by the quality factor of the double pole of the inductance.

Table 12-3 lists component values.

Table 12-3. Component Values

| | |
|------------|---|
| R_{FBT} | Top feedback resistance |
| R_{FBB} | Bottom feedback resistance |
| R_{FF} | Compensation feed-forward resistance |
| R_{COMP} | Compensation resistance |
| C_{FF} | Compensation feed-forward capacitance |
| C_{COMP} | Compensation capacitance |
| C_{HF} | Compensation high-frequency capacitance |

For Type II and Type II transconductance compensation networks, the Loop Calculator offers an option to use an additional Feed-Forward Capacitor in parallel with R_{FBT} . This option can be enabled by right-clicking on the C_{FF} input field and choosing *Use*.

At start-up the Loop Calculator displays only the resulting Bode plot for the Total Gain and Total Phase. The graphs for the Gain of the Power Stage, Phase of the Power Stage, Gain of the Error Amplifier, Phase of the Error Amplifier and the Error Amplifier Open Loop Gain can be switched on by selecting the respective checkbox.

12.2 Transfer Functions

12.2.1 Output Impedance Transfer Function

For two parallel capacitors the transfer function can be written as shown in [Equation 29](#):

$$Z_{out} = \frac{R_{out} \times (s \times C_1 \times ESR_1 + 1) \times (s \times C_2 \times ESR_2 + 1)}{(s \times C_1 \times ESR_1 + 1) \times (s \times C_2 \times ESR_2 + 1) + R_{out} \times [s \times C_2 \times (s \times C_1 \times ESR_1 + 1) + s \times C_1 \times (s \times C_2 \times ESR_2 + 1)]} \quad (29)$$

12.2.2 Transfer Function VMC Buck Power Stage

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{K_m \times Z_{out}}{Z_L + Z_{out}} \quad (30)$$

DC-Gain:

$$K_m = \frac{V_{in}}{V_{ramp}} \quad (31)$$

Filter-Inductor Impedance:

$$Z_L = s \times L + DCR_L \quad (32)$$

12.2.3 Transfer Function CMC Buck Power Stage

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{K_m \times Z_{out}}{Z_L + Z_{out} + K_m \times R_i \times H(s)} \quad (33)$$

Duty cycle:

$$D = \frac{V_{out}}{V_{in}} \quad (34)$$

DC-Gain:

$$K_m = \frac{1}{(0.5 - D) \times R_S \times A_S \times \frac{1}{f_{switch} \times L} + \frac{V_{slope}}{V_{in}}} \quad (35)$$

Sampling Gain Pole:

$$\omega_L = \pi \times f_{switch} \quad (36)$$

$$R_i = A_S \times R_S \quad (37)$$

$$H(s) = 1 + \frac{s}{Q_L \times \omega_L} + \frac{s^2}{\omega_L^2} \quad (38)$$

With V_{slope} :

$$s_e = V_{slope} \times f_{switch} \quad (39)$$

With SLM:

$$s_e = \frac{SLM \times V_{out} \times A_S \times R_S}{L}$$

$$s_n = \frac{(V_{in} - V_{out}) \times A_S \times R_S}{L}$$

$$Q_L = \frac{1}{\pi \times \left[\left(1 + \frac{s_e}{s_n} \right) \times (1 - D) - 0.5 \right]} \quad (40)$$

12.2.4 Transfer Function CMC Boost Power Stage

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{K_m \times (1 - D) \times \left(1 - \frac{Z_L}{(1 - D)^2 \times R_{out}} \right)}{(1 - D)^2 + \frac{Z_L}{Z_{out}} + K_m \times R_i \times H(s) \times \left(\frac{1}{R_{out}} + \frac{1}{Z_{out}} \right) + K \times K_m \times (1 - D) \times \left(1 - \frac{Z_L}{(1 - D)^2 \times R_{out}} \right)} \quad (41)$$

Duty cycle:

$$D = \frac{V_{out} - V_{in}}{V_{out}} \quad (42)$$

DC-Gain:

$$K_m = \frac{1}{(0.5 - D) \times R_S \times A_S \times \frac{1}{f_{switch} \times L} + \frac{V_{slope}}{V_{in}}} \quad (43)$$

$$K = 0.5 \times R_S \times A_S \times \frac{1}{f_{switch} \times L} \times D \times (1 - D) \quad (44)$$

Sampling Gain Pole:

$$\omega_L = \pi \times f_{switch} \quad (45)$$

$$R_i = A_S \times R_S \quad (46)$$

$$H(s) = 1 + \frac{s}{Q_L \times \omega_L} + \frac{s^2}{\omega_L^2} \quad (47)$$

With V_{slope} :

$$s_e = V_{slope} \times f_{switch} \quad (48)$$

With SLM:

$$s_e = \frac{SLM \times V_{out} \times A_S \times R_S}{L}$$

$$s_n = \frac{V_{in} \times A_S \times R_S}{L}$$

$$Q_L = \frac{1}{\pi \times \left[\left(1 + \frac{s_e}{s_n} \right) \times (1 - D) - 0.5 \right]} \quad (49)$$

12.2.5 Transfer Function CMC Inverting Buck-Boost Power Stage

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{K_m \times (1 - D) \times \left(1 - \frac{D \times Z_L}{(1 - D)^2 \times R_{out}} \right)}{(1 - D)^2 + \frac{Z_L}{Z_{out}} + K_m \times R_i \times H(s) \times \left(\frac{D}{R_{out}} + \frac{1}{Z_{out}} \right) + K \times K_m \times (1 - D) \times \left(1 - \frac{D \times Z_L}{(1 - D)^2 \times R_{out}} \right)} \quad (50)$$

Duty cycle:

$$D = \frac{-V_{out}}{-V_{out} + V_{in}} \quad (51)$$

Sampling Gain Pole:

$$\omega_L = \pi \times f_{switch} \quad (52)$$

$$R_i = A_S \times R_S \quad (53)$$

$$H(s) = 1 + \frac{s}{Q_L \times \omega_L} + \frac{s^2}{\omega_L^2} \quad (54)$$

$$K_m = \frac{1}{(0.5 - D) \times R_S \times A_S \times \frac{1}{f_{switch} \times L} + \frac{V_{slope}}{V_{in} - V_{out}}} \quad (55)$$

$$K = 0.5 \times R_S \times A_S \times \frac{1}{f_{switch} \times L} \times D \times (1 - D) \quad (56)$$

With V_{slope} :

$$s_e = V_{slope} \times f_{switch} \quad (57)$$

With SLM:

$$s_e = \frac{SLM \times (-V_{out}) \times A_s \times R_s}{L}$$

$$s_n = \frac{V_{in} \times A_s \times R_s}{L}$$

$$Q_L = \frac{1}{\pi \times \left[\left(1 + \frac{s_e}{s_n} \right) \times (1 - D) - 0.5 \right]} \quad (58)$$

12.2.6 Transfer Function CMC Forward Power Stage

For interleaved topologies like Push-Pull, Half-Bridge, or Full-Bridge, twice as much FET switching frequency must be used for calculations because the output inductor "sees" twice the FET switching frequency.

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{K_m \times Z_{out} \times \frac{N_s}{N_p}}{Z_L + Z_{out} + K_m \times R_i \times \frac{N_s}{N_p}} \quad (59)$$

Duty cycle:

$$D = \frac{V_{out} \times \frac{N_p}{N_s}}{V_{in}} \quad (60)$$

DC-Gain:

$$K_m = \frac{1}{(0.5 - D) \times R_s \times A_s \times \frac{1}{f_{sw} \times L} + \frac{V_{slope}}{V_{in}}} \quad (61)$$

Sampling Gain Pole:

$$\omega_L = \pi \times f_{switch} \quad (62)$$

$$R_i = A_s \times R_s \quad (63)$$

$$A_s = \frac{1}{N'} \quad (64)$$

N' is the turns ratio between auxiliary and primary winding.

$$H(s) = 1 + \frac{s}{Q_L \times \omega_L} + \frac{s^2}{\omega_L^2} \quad (65)$$

With V_{slope} :

$$s_e = V_{slope} \times f_{switch} \quad (66)$$

With SLM:

$$s_e = \frac{SLM \times V_{out} \times \frac{N_p}{N_s} \times A_s \times R_s}{L \times \left(\frac{N_p}{N_s}\right)^2}$$

$$s_n = \frac{\left(V_{in} \times \frac{N_s}{N_p} - V_{out}\right) \times A_s \times R_s}{L}$$

$$Q_L = \frac{1}{\pi \times \left[\left(1 + \frac{s_e}{s_n}\right) \times (1 - D) - 0.5\right]} \quad (67)$$

12.2.7 Transfer Function CMC Flyback Power Stage

$$\frac{\hat{v}_{out}}{\hat{v}_c} = \frac{K_m \times (1 - D) \times \left(1 - \frac{D \times Z_L}{(1 - D)^2 \times R_{out} \times \left(\frac{N_p}{N_s}\right)^2}\right)}{(1 - D)^2 + \frac{Z_L}{Z_{out} \times \left(\frac{N_p}{N_s}\right)^2} + K_m \times R_i \times H(s) \times \left(\frac{D}{R_{out}} + \frac{1}{Z_{out} \times \left(\frac{N_p}{N_s}\right)^2}\right) + K \times K_m \times (1 - D) \times \left(1 - \frac{D \times Z_L}{(1 - D)^2 \times R_{out} \times \left(\frac{N_p}{N_s}\right)^2}\right)} \quad (68)$$

Duty cycle:

$$D = \frac{V_{out} \times \frac{N_p}{N_s}}{V_{in} + V_{out} \times \frac{N_p}{N_s}} \quad (69)$$

DC-Gain:

$$K_m = \frac{1}{(0.5 - D) \times R_s \times A_s \times \frac{1}{f_{sw} \times L} + \frac{V_{slope}}{V_{in} + \left(\frac{N_p}{N_s}\right) \times V_{out}}} \quad (70)$$

$$K = 0.5 \times R_s \times A_s \times \frac{1}{f_{switch} \times L} \times D \times (1 - D) \quad (71)$$

Sampling Gain Pole:

$$\omega_L = \pi \times f_{switch} \quad (72)$$

$$R_i = A_s \times R_s \quad (73)$$

$$H(s) = 1 + \frac{s}{Q_L \times \omega_L} + \frac{s^2}{\omega_L^2} \quad (74)$$

With V_{slope} :

$$s_e = V_{slope} \times f_{switch} \quad (75)$$

With SLM:

$$s_e = \frac{SLM \times V_{out} \times \frac{N_p}{N_s} \times A_s \times R_s}{L}$$

$$s_n = \frac{V_{in} \times A_s \times R_s}{L}$$

$$Q_L = \frac{1}{\pi \times \left[\left(1 + \frac{s_e}{s_n} \right) \times (1 - D) - 0.5 \right]} \quad (76)$$

12.2.8 Transfer Function Closed Loop

Closed-loop error amplifier transfer function for non-isolated feedback:

$$\frac{\hat{v}_c}{\hat{v}_{out}} = -G_{EA}(s) \times \frac{1}{1 + \left(\frac{1}{A_{OL}} + \frac{s}{\omega_{BW}} \right) + (1 + G_{FB}(s))} \quad (77)$$

12.2.8.1 Transfer Function Type II Compensation Network

Figure 12-2 is a schematic of a Type II compensation network.

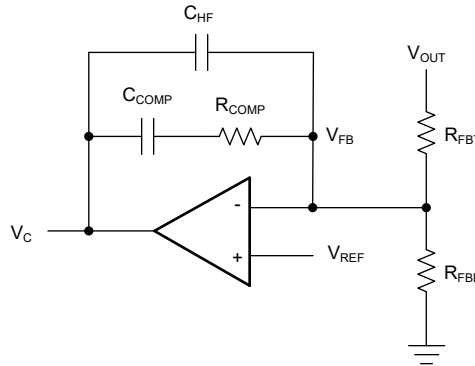


Figure 12-2. Schematic of a Type II Compensation Network

Type II with feed forward:

$$G_{EA}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}} \right) \times \left(1 + \frac{s}{\omega_{ZFF}} \right)}{\left(1 + \frac{C_{HF}}{C_{COMP}} \right) \times \left(1 + \frac{s}{\omega_{HF}} \right)} \quad (78)$$

$$G_{FB}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}} \right) \times \left(1 + \frac{s}{\omega_{ZFF}} \right)}{\frac{R_{FBB}}{R_{FBB} + R_{FBT}} \times \left(1 + \frac{C_{HF}}{C_{COMP}} \right) \times \left(1 + \frac{s}{\omega_{HF}} \right)} \quad (79)$$

Type II:

$$G_{EA}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}} \right)}{\left(1 + \frac{C_{HF}}{C_{COMP}} \right) \times \left(1 + \frac{s}{\omega_{HF}} \right)} \quad (80)$$

$$G_{FB}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}} \right)}{\frac{R_{FBB}}{R_{FBB} + R_{FBT}} \times \left(1 + \frac{C_{HF}}{C_{COMP}} \right) \times \left(1 + \frac{s}{\omega_{HF}} \right)} \quad (81)$$

Compensation zero:

$$\omega_{ZEA} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (82)$$

Compensation pole:

$$\omega_{HF} = \frac{1}{R_{COMP} \times C_{HF}} \quad (83)$$

With additional feed-forward capacitor in parallel with R_{FBT} :

$$\omega_{ZFF} = \frac{1}{R_{FBT} \times C_{FF}}$$

$$\omega_{PFF} = \frac{1}{\left(\frac{1}{R_{RFBB}} + \frac{1}{R_{RFBT}} \right)} \times C_{FF} \quad (84)$$

12.2.8.2 Transfer Function Type II Transconductance Compensation Network

Figure 12-3 is a schematic of a Type II transconductance compensation network.

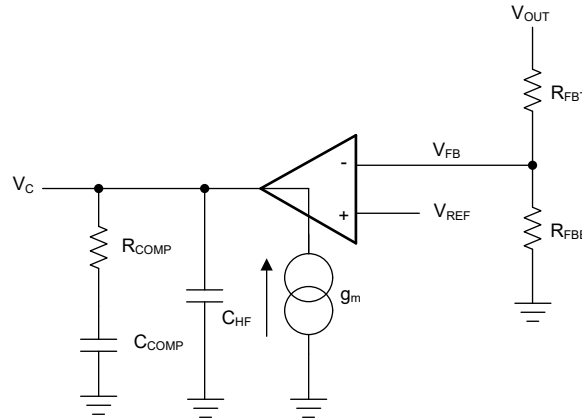


Figure 12-3. Schematic of a Type II Transconductance Compensation Network

Type II Transconductance with feed-forward:

$$G_{EA}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}}\right) \times \left(1 + \frac{s}{\omega_{ZFF}}\right)}{\left(1 + \frac{C_{HF}}{C_{COMP}}\right) \times \left(1 + \frac{s}{\omega_{PFF}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (85)$$

$$G_{FB}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}}\right) \times \left(1 + \frac{s}{\omega_{ZFF}}\right)}{\frac{R_{FBTT}}{R_{FBTT} + R_{FBTT}} \times \left(1 + \frac{C_{HF}}{C_{COMP}}\right) \times \left(1 + \frac{s}{\omega_{PFF}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (86)$$

Type II Transconductance:

$$G_{EA}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}}\right)}{\left(1 + \frac{C_{HF}}{C_{COMP}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (87)$$

$$G_{FB}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}}\right)}{\frac{R_{FBTT}}{R_{FBTT} + R_{FBTT}} \times \left(1 + \frac{C_{HF}}{C_{COMP}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (88)$$

DC-Gain:

$$A_{VM} = \frac{R_{FBTT}}{R_{FBTT} + R_{FBTT}} \times G_m \times R_{COMP} \quad (89)$$

Compensation zero:

$$\omega_{ZEA} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (90)$$

Compensation Pole:

$$\omega_{HF} = \frac{1}{R_{COMP} \times C_{HF}} \quad (91)$$

With additional feed-forward capacitor in parallel with R_{FBT} :

$$\omega_{ZFF} = \frac{1}{R_{FBT} \times C_{FF}}$$

$$\omega_{PPF} = \frac{1}{\frac{1}{\frac{1}{R_{FBT}} + \frac{1}{R_{FBB}}} \times C_{FF}} \quad (92)$$

12.2.8.3 Transfer Function Type III Compensation Network

Figure 12-4 is a schematic of a Type III compensation network.

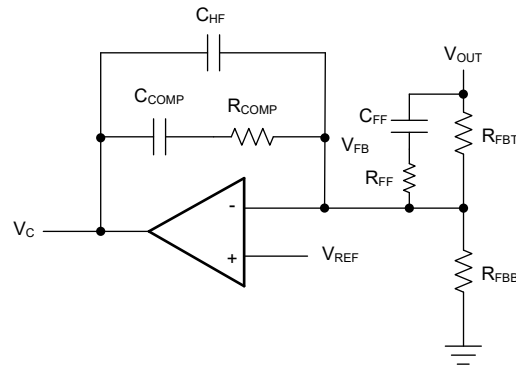


Figure 12-4. Schematic of a Type III Compensation Network

Type III:

$$G_{EA}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}}\right) \times \left(1 + \frac{s}{\omega_{ZFF}}\right)}{\left(1 + \frac{C_{HF}}{C_{COMP}}\right) \times \left(1 + \frac{s}{\omega_{PPF}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (93)$$

$$G_{FB}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}}\right) \times \left(1 + \frac{s}{\omega_{ZFF}}\right)}{\frac{R_{FBB}}{R_{FBB} + R_{FBT}} \times \left(1 + \frac{C_{HF}}{C_{COMP}}\right) \times \left(1 + \frac{s}{\omega_{PPF}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (94)$$

DC-Gain:

$$A_{VM} = \frac{R_{COMP}}{R_{FBT}} \quad (95)$$

Compensation zero 1:

$$\omega_{ZEA} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (96)$$

Compensation zero 2:

$$\omega_{ZFF} = \frac{1}{R_{FBT} \times C_{FF}} \quad (97)$$

Compensation pole 1:

$$\omega_{FP} = \frac{1}{R_{FF} \times C_{FF}} \quad (98)$$

Compensation pole 2:

$$\omega_{HF} = \frac{1}{R_{COMP} \times C_{HF}} \quad (99)$$

12.2.9 Transfer Function Isolated Type II Compensation Network With a Zener Clamp

Figure 12-5 is a schematic of an isolated Type II compensation network with a Zener clamp.

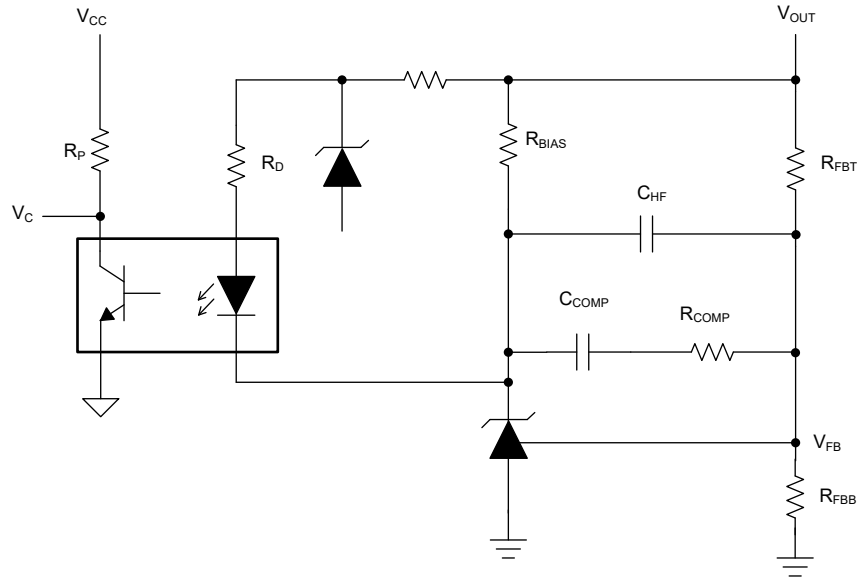


Figure 12-5. Schematic of an Isolated Type II Compensation Network With a Zener Clamp

Closed loop error amplifier transfer function for isolated feedback.

Type II Isolated with Zener Clamp:

$$\frac{\hat{v}_c}{\hat{v}_{out}} = -CTR(s) \times \frac{R_P}{R_D} \times G_{EA}(s) \times \frac{1}{1 + \left(\frac{1}{AOL} + \frac{s}{\omega_{BW}}\right) + (1 + G_{FB}(s))} \quad (100)$$

$$G_{EA}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}}\right)}{\left(1 + \frac{C_{HF}}{C_{COMP}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (101)$$

$$G_{FB}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}}\right)}{\frac{R_{FB_B}}{R_{FB_B} + R_{FB_T}} \times \left(1 + \frac{C_{HF}}{C_{COMP}}\right) \times \left(1 + \frac{s}{\omega_{HF}}\right)} \quad (102)$$

$$CTR(s) = \frac{CTR}{1 + \frac{s}{\omega_{OPTO}}} \quad (103)$$

DC-Gain:

$$A_{VM} = CTR \times \frac{R_P}{R_D} \quad (104)$$

Power Stage Designer uses a constant value of 1 for CTR.

Compensation zero:

$$\omega_{ZEA} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (105)$$

Compensation pole:

$$\omega_{HF} = \frac{1}{R_{COMP} \times C_{HF}} \quad (106)$$

12.2.10 Transfer Function Isolated Type II Compensation Network Without a Zener Clamp

Figure 12-6 is a schematic of an isolated Type II compensation network without a Zener clamp.

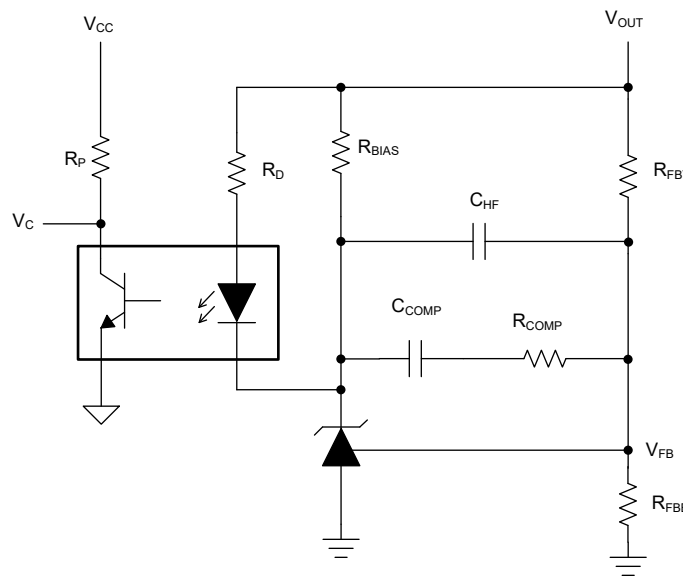


Figure 12-6. Schematic of an Isolated Type II Compensation Network Without a Zener Clamp

$$\frac{\hat{v}_c}{\hat{v}_{out}} = -CTR(s) \times \frac{R_P}{R_D} \times \left[1 + G_{EA}(s) \times \frac{1}{1 + \left(\frac{1}{A_{OL}} + \frac{s}{\omega_{BW}} \right) + (1 + G_{FB}(s))} \right] \quad (107)$$

$$G_{EA}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}} \right)}{\left(1 + \frac{C_{HF}}{C_{COMP}} \right) \times \left(1 + \frac{s}{\omega_{HF}} \right)} \quad (108)$$

$$G_{FB}(s) = \frac{A_{VM} \times \frac{\omega_{ZEA}}{s} \times \left(1 + \frac{s}{\omega_{ZEA}} \right)}{\frac{R_{FBB}}{R_{FBB} + R_{FBT}} \times \left(1 + \frac{C_{HF}}{C_{COMP}} \right) \times \left(1 + \frac{s}{\omega_{HF}} \right)} \quad (109)$$

$$CTR(s) = \frac{CTR}{1 + \frac{s}{\omega_{OPTO}}} \quad (110)$$

DC-Gain:

$$A_{VM} = CTR \times \frac{R_P}{R_D} \quad (111)$$

Compensation Zero:

$$\omega_{ZEA} = \frac{1}{R_{COMP} \times C_{COMP}} \quad (112)$$

Compensation pole:

$$\omega_{HF} = \frac{1}{R_{COMP} \times C_{HF}} \quad (113)$$

Note**Loop Calculator Tips**

A Type I compensation network can be simulated by choosing a Type II compensation (Type II, Type II isolated with a Zener clamp, Type II isolated with inner loop) and setting R_{COMP} equal to R_{FBT} . The crossover frequency depends on the value of C_{COMP} . Set C_{HF} equal to C_{COMP} .

13 Filter Designer

The Filter Designer enables the user to design a differential mode filter, such as the input filter for a power supply. The tool shows the Bode plot of the filter transfer function and the damping circuit and helps with finding a desirable damping circuit (see example in [Figure 13-1](#)). In addition, the filter impedance with and without the damping circuit is displayed to determine if the filter is stable or not.

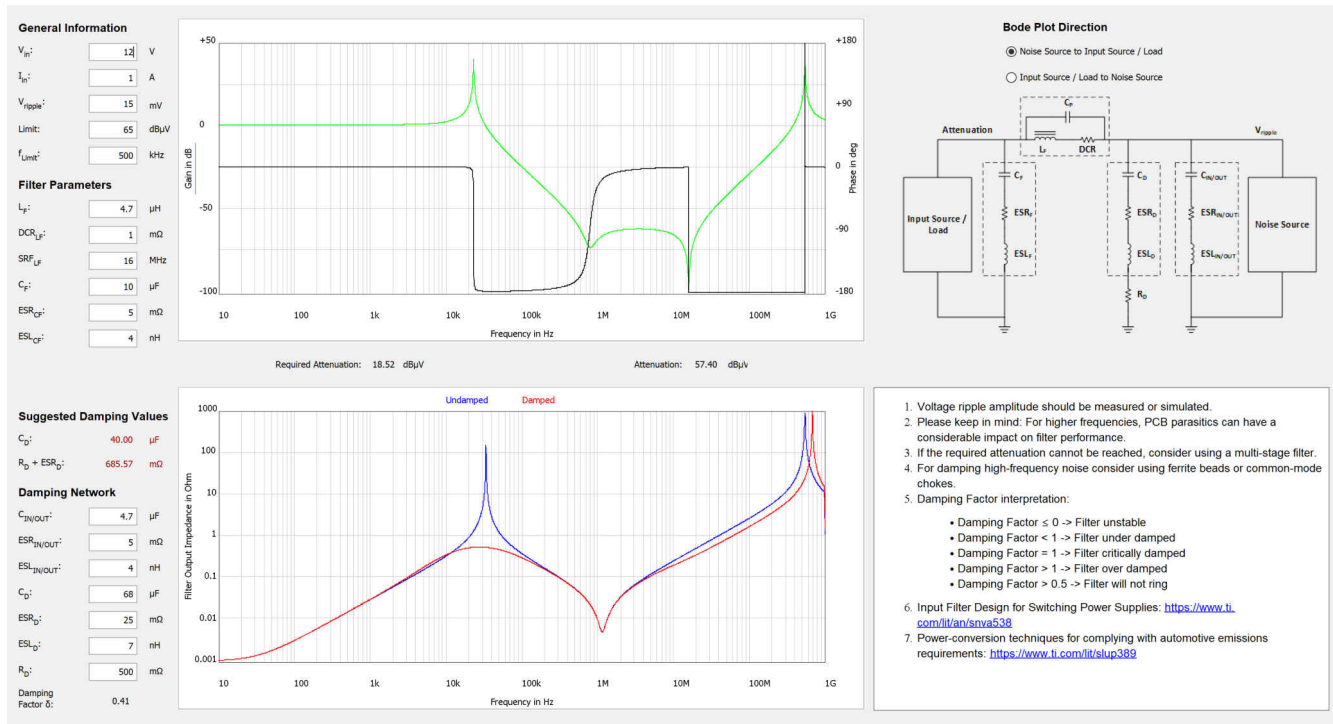


Figure 13-1. Filter Designer Window

13.1 Impedances

$$Z_{IN/OUT}(s) = ESR_{IN/OUT} + s \times ESL_{IN/OUT} + \frac{1}{s \times C_{IN/OUT}} \quad (114)$$

$$Z_D(s) = R_D + ESR_D + s \times ESL_D + \frac{1}{s \times C_D} \quad (115)$$

$$Z_F(s) = ESR_F + s \times ESL_F + \frac{1}{s \times C_F} \quad (116)$$

$$C_L = \frac{1}{L_F} \times \left(\frac{1}{2 \times \pi \times SRF} \right)^2 \quad (117)$$

$$Z_L(s) = \frac{DCR + s \times L}{s \times C_L \times (DCR + s \times L) + 1} \quad (118)$$

13.2 Transfer Functions

Noise source to input source, load:

$$G_F(s) = \frac{Z_F(s)}{Z_F(s) + Z_L(s)} \quad (119)$$

Input source, load to noise source:

$$G_D(s) = \frac{\frac{Z_D(s) \times Z_{IN/OUT}(s)}{Z_D(s) + Z_{IN/OUT}(s)}}{\frac{Z_D(s) \times Z_{IN/OUT}(s)}{Z_D(s) + Z_{IN/OUT}(s)} + Z_L(s)} \quad (120)$$

13.3 Filter Output Impedance

Undamped:

$$Z_{out, undamped}(s) = \left| \frac{Z_L(s) \times Z_{IN/OUT}(s)}{Z_L(s) + Z_{IN/OUT}(s)} \right| \quad (121)$$

Damped:

$$Z_{out, damped}(s) = \left| \frac{Z_L(s) \times \frac{Z_D(s) \times Z_{IN/OUT}(s)}{Z_D(s) + Z_{IN/OUT}(s)}}{Z_L(s) + \frac{Z_D(s) \times Z_{IN/OUT}(s)}{Z_D(s) + Z_{IN/OUT}(s)}} \right| \quad (122)$$

13.4 Damping Factor

f_{damp} is the filter frequency of the filter inductor and the parallel input/output capacitor and damping capacitor network.

$$X_{Cin/out} = \frac{1}{2 \times \pi \times f_{damp} \times C_{IN/OUT}} \quad (123)$$

$$X_{Cd} = \frac{1}{2 \times \pi \times f_{damp} \times C_D} \quad (124)$$

Effective impedance at f_{damp} .

$$Z_{eff} = \frac{\sqrt{ESR_{IN/OUT}^2 + X_{Cin/out}^2} \times \sqrt{(R_D + ESR_D)^2 + X_{Cd}^2}}{\sqrt{(R_D + ESR_D + ESR_{IN/OUT})^2 + (X_{Cd} + X_{Cin/out})^2}} \quad (125)$$

Effective phase angle at f_{damp} .

$$\varphi_{eff} = \tan^{-1}\left(\frac{X_{Cin/out}}{ESR_{IN/OUT}}\right) + \tan^{-1}\left(\frac{X_{Cd}}{R_D + ESR_D}\right) - \tan^{-1}\left(\frac{X_{Cin/out} + X_{Cd}}{ESR_{IN/OUT} + R_D + ESR_D}\right) \quad (126)$$

Effective capacitance:

$$C_{eff} = \frac{1}{2 \times \pi \times f_{damp} \times Z_{eff} \times \sin(\varphi_{eff})} \quad (127)$$

Effective ESR:

$$ESR_{eff} = Z_{eff} \times \cos(\varphi_{eff}) \quad (128)$$

Damping factor:

$$\delta = 0.5 \times \left(\frac{DCR + ESR_{eff}}{\sqrt{\frac{L_F}{C_{eff}}}} + \sqrt{\frac{L_F}{C_{eff}}} \frac{V_{in}}{I_{in}} \right) \quad (129)$$

14 Additional Information

The following list contains references to additional information for various topics in this user's guide.

1. Mammano, Robert A.; Kollmann, Robert; *Fundamentals of Power Supply Design, Chapter 13: Power-Supply Construction*, Texas Instruments, ISBN: 978-0-9985994-0-3 (see [Section 4](#))
2. Dinwoodie, L.; [Exposing the Inner Behavior of a Quasi-Resonant Flyback Converter](#), Texas Instruments Power Supply Design Seminar SEM2000, 2012/2013 (see [Section 5](#))
3. Keogh, Bernard; Cohen, Isaac; [Flyback transformer design considerations for efficiency and EMI](#), Texas Instruments Power Supply Design Seminar SEM2200, 2016/2017 (see [Section 6](#))
4. Dinwoodie, Lisa; [Design Review: Isolated 50-Watt Flyback Converter Using the UCC3809 Primary Side Controller and the UC3965 Precision Reference and Error Amplifier](#) (see [Section 6](#))
5. Dinwoodie, Lisa; [Application Report: UCC38C44 12-V Isolated Bias Supply](#) (see [Section 6](#))
6. Betten, John; [Power Tips: Calculate an R-C snubber in seven steps](#) (see [Section 7](#))
7. Sheehan, R.; Diana, L.; [Switch-mode power converter compensation made easy](#), Texas Instruments Power Supply Design Seminar SEM2200, 2016/2017 (see [Section 12.2](#))
8. Ridley, R.; [A More Accurate Current-Mode Control Model](#), Texas Instruments Power Supply Design Seminar SEM1400, 2000 (see [Section 12.2](#))

15 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision A (November 2017) to Revision B (February 2023) | Page |
|--|-------------|
| • Updated the numbering format for tables, figures, and cross-references throughout the document..... | 1 |
| • Replaced several figures to represent the new UI. Updated equations for Capacitor Current Sharing Calculator and Loop Calculator . Added new tools, the Load Step Calculator and Filter Designer | 1 |
| Changes from Revision * (November 2017) to Revision A (February 2018) | Page |
| • Changed fourth line of Equation 13 | 10 |

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