Section 5

High Speed PCB Layout Techniques

Scenario: You have spent several days, no maybe weeks, perfecting a design on paper and also using Spice to ensure the design exceeds all expectations. You hand the schematic to your layout person who puts all everything on a printed circuit board (PCB). The PCB comes back in a week or two and is finally populated and ready to test. But it doesn't work!!!!

Why not? On paper it works!! Spice said it works!! But it doesn't work!!

This scenario happens more often than not and the reason many circuits do not work as expected is due primarily to the PCB layout.
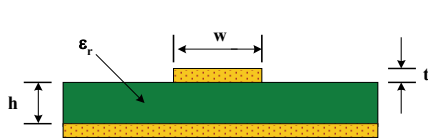
This section looks at some key fundamentals of high speed PCB layout techniques so that hopefully the above scenario will never happen to you.

PCB Components

Component: Copper Traces

Purpose: Interconnect two or more points

Problem: Inductance and Capacitance

x = length of trace (cm)
w = width of trace (cm)
h = height of trace (cm)
t = thickness of trace (cm)
e_r = PCB Permeability

$$L(nH) \approx 2x\ ln\left(\frac{5.98\ h}{0.8\ w + t}\right)$$

$$C(pF) \approx \frac{0.264x\ (\varepsilon_r + 1.41)}{ln\left(\frac{5.98\ h}{0.8\ w + t}\right)}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \qquad T_p(\ ps/cm\ ) = 31.6\sqrt{L(nH)C(pF)}$$

0.8mm (0.031") trace on 0.8mm (0.031") thick PCB (FR-4) has:

~ 4nH and 0.8pF per cm

~ 10nH and 2.0pF per inch

e_r = PCB material permeability (FR-4 ~ 4.5)

The PCB consists of layers of metal and insulator and can consist of several layers. Examining some common elements of a PCB will help the reader understand what many people believe is "Black Magic".
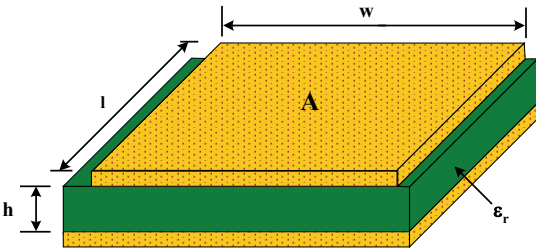
Copper traces are utilized to connect one element node to another node. The shape of these traces determine one very important aspect of a PCB – the characteristic inductance, capacitance, and ultimately the characteristic impedance. Resistance is generally ignored as most designs do not carry more than several mA of current and the results can often be negligible.

Characteristic impedance (Z_0) was covered previously, so this will not be discussed here. But what is important is the inductance and capacitance as determined by the trace dimensions and the PCB dielectric (ε_r). FR-4, probably the most common PCB material used by manufacturers today and has a permeability range normally from 4.0 to 5.0, but 4.5 is often used as a typical permeability. Check with the PCB manufacturer to determine what material they utilize and the associated permeability.

NOTE: Reference the book entitled "High-Speed Digital Design – A Handbook for Black Magic" written by Howard Johnson and Martin Graham, 1993, Prentice-Hall, ISBN 0-13-395724-1.

PCB Components

Component: Copper Planes
Purpose: Used For Ground Planes and Power Planes
Problem: Stray Capacitance on Signal Traces
Benefit: Large Bypass Capacitance & Minimal Inductance

$$C(pF) \approx \frac{0.0886 \; \varepsilon_r \; A}{h}$$

h = separation between planes (cm)
A = area of common planes = l*w (cm²)
e$_r$ = PCB Permeability

0.8mm (0.031") thick PCB (FR-4) has:
˜ 0.5pF per cm²
˜ 32.7pF per inch²

e$_r$ = PCB material permeability (FR-4 ˜ 4.5)

Copper planes are typically found when power planes and ground planes are utilized. Planes make an excellent high frequency capacitor and can often be utilized for high frequency bypassing in complement with traditional capacitors.

The use of a solid ground plane is generally preferred over a grid plane. A solid plane minimizes inductance to the absolute minimum which is a desirable trait for high speed signals – which includes both Analog and Digital signals. But, as will be discussed later, this plane can cause capacitance problems to sensitive nodes of the circuit. Be aware of all attributes of the circuit and do not blindly use planes everywhere.
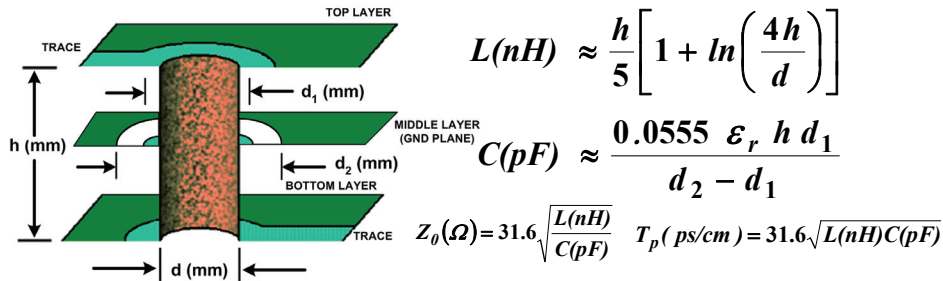
A side benefit of a solid plane is it becomes a very good thermal conductor and can act as a heat sink to keep thermal levels of all devices minimized. But on the flip side, temperature sensitive components may not want to have the ground plane nearby due to this heat spreading.

PCB Components

Component: Vias

Purpose: Interconnect traces on different layers

Problem: Inductance and Capacitance

TOP LAYER

TRACE

d_1 (mm)

h (mm)

MIDDLE LAYER
(GND PLANE)

d_2 (mm)

BOTTOM LAYER

TRACE

d (mm)

$$L(nH) \approx \frac{h}{5}\left[1 + ln\left(\frac{4h}{d}\right)\right]$$

$$C(pF) \approx \frac{0.0555 \ \varepsilon_r \ h \ d_1}{d_2 - d_1}$$

$$Z_0(\Omega) = 31.6\sqrt{\frac{L(nH)}{C(pF)}} \quad T_p(ps/cm) = 31.6\sqrt{L(nH)C(pF)}$$

0.4mm (0.0157") via with 1.6mm (0.063") thick PCB has ˜ 1.2nH

1.6mm (0.063") Clearance hole around 0.8mm (0.031") pad on FR-4 has ˜ 0.4pF

e_r = PCB material permeability (FR-4 ˜ 4.5)

Vias are utilized to simplify trace routing around other components or when there is a high density of interconnections to be made (i.e. BGA packages). Just as a PCB trace had inductance and capacitance, so to does a via. Generally these elements are ignored as the length of the vias are typically very small relative to the rest of the trace. But, this Can cause issues if the signals are very high frequency (>100MHz) or have energy / harmonics at high frequencies.

The easiest way to minimize problems of a via is to simply not use them with signal traces. At the very least it should be minimized. If vias must be used, there are other issues to worry about that will be discussed later.

Current Density

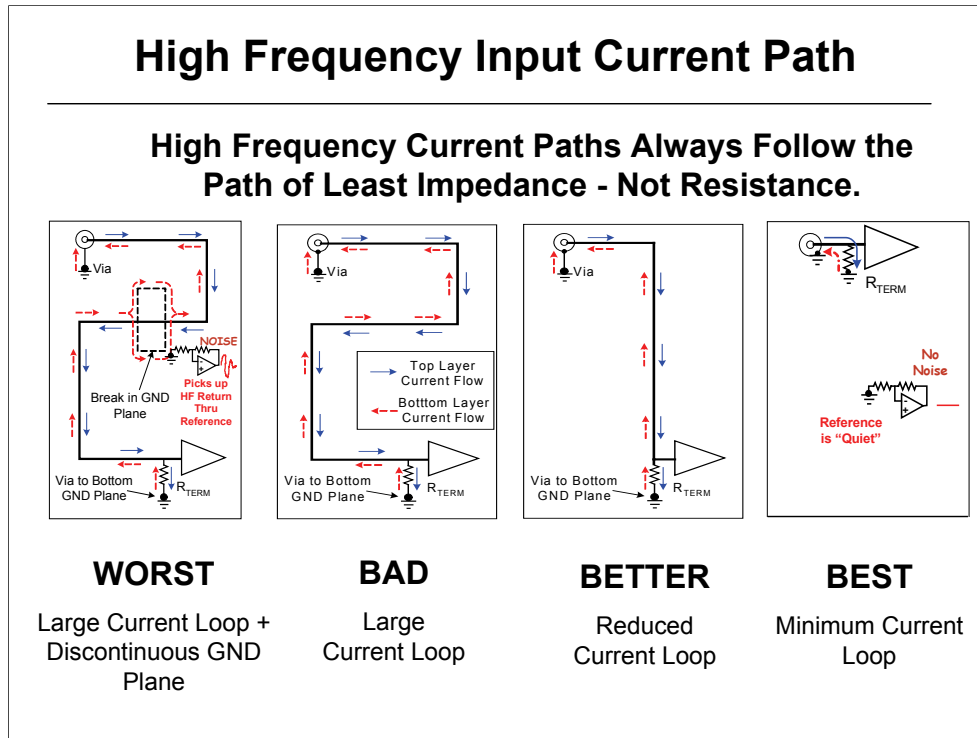$$i(A/cm) = \frac{I_O}{\pi \, h} \times \frac{1}{1 + \left(\dfrac{D}{h}\right)^2}$$

I_O = total signal current (A)
h = height of trace (cm)
D = distance from trace (cm)
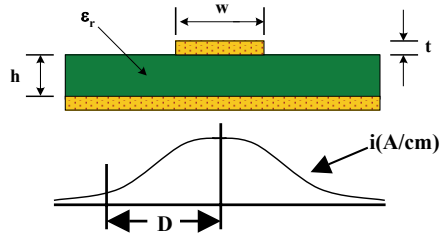
◆ Illustrates Return Current Flow is directly below the signal trace. The creates the path of least impedance.
◆ Must have Solid return path (i.e. Solid Ground Plane) under the signal trace to maintain homogeneous nature of current density.

Current density is the concentration of current flowing through a conductor. This is especially important when looking at return currents.

One thing that many people forget about is for a current to flow out to a point, there MUST be a return path or else current will Not flow. Since there is a current flow, then the return current flow will find a way back to its' source one way or another. Return current density is highest directly under (or over) the signal trace it was sourced from. Even if a solid ground plane is used, the concentration of current flow will still be adjacent to the signal source trace.

High Frequency Input Current Path

High Frequency Current Paths Always Follow the Path of Least Impedance - Not Resistance.

WORST
Large Current Loop + Discontinuous GND Plane

BAD
Large Current Loop

BETTER
Reduced Current Loop

BEST
Minimum Current Loop

As just discussed, the lowest impedance path of a high speed signal is directly under a PCB trace. This minimizes the current loop area substantially. The "worst" case scenario shows a long winding trace creates a large current loop area which is made even worse by the break in the ground plane. The obvious issue with this is the ground plane is often used as a reference point for other parts of the system. If the current flow density is high near one of these reference points, this can (and often does) cause noise to occur in the circuit and often propagates throughout the entire signal flow.

As the bad layout shows, also shows a long winding trace that does not follow the "shortest distance between two points is a straight line" method. The better layout minimizes the distance while reducing the current loop area. But, the best way to do the layout is to place the receiver part as close as possible to the input. This easily is the smallest loop area and delays in the signal path are drastically reduced. A key benefit of this method is the reference ground point for other circuits are kept "quiet" and should have no contribution from the undesirable current flow.

This also minimizes the need for adhering to strict strip-line techniques as the signal path acts as a lumped circuit and not a distributed circuit. A lumped circuit typically has rising edges much less than the delay time of the transmission line, thus minimizing issues. The construction of transmission lines naturally keeps the source and return currents close to each other. This helps minimize current loop area and drastically reduces noise along the path on the PCB and also EMI.

High Frequency Output Current Path

Problems:

◆ Long winding path causing large current loop area.

◆ HF bypass caps are placed too far away from amplifier and GND. Inductance eliminates benefit of bypass caps.

◆ GND of bypass caps are too far away from amplifier output.

◆ Series Resistor (RSOURCE) is too far away from the amplifier. Causes C-loading on amplifier and lack of a transmission line.

◆ Single GND point on connector
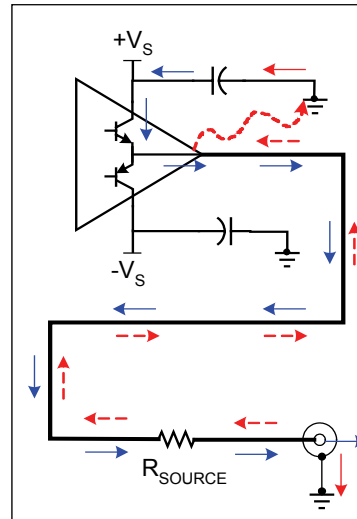
Looking at the Output current path shows the exact same phenomenon as the input current flow – the return current path will follow the signal trace path wherever it may go. One issue that is often overlooked is where does this return current flow once it reaches the output of the driver? As we all know, current must close the loop or else there is no current flow.

In the example above, the return current flows through the bypass capacitors and back into the power supply lines. Now we see that the bypass capacitors are part of the loop and will have impact on the performance of the system. Obviously it makes sense to place the capacitors as close as possible to the driver power supply pins and the actual output trace.

Another issue with the above system is the source resistance is very far away from the driver. As will be discussed later, this is a bad thing for the driver and may cause stability problems. Additionally, the transmission line typically starts at the load side of the resistor. This system may have a undefined characteristic impedance that may cause reflection concerns.

The last concern is the single ground connection point of the connector. This may cause a significant impedance mismatch in the return current flow.

High Frequency Output Current Path

Solutions:

◆ Amplifier is next to Connector minimizing loop area.

◆ HF bypass caps are now placed next to amplifier power supply pins and has short GND connection.

◆ GND of bypass caps near amplifier output – but not too close to cause C-loading issues.

◆ Source Resistance is next to amplifier output.

◆ Multiple GND points on connector.
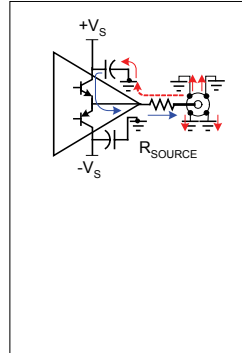
As seen before, the simple solution is to simply minimize the current flow area as much as possible. Easily solved by moving the connector and the driver next to each other. The bypass caps are now very close to the driver power supply pins and have very short trace lengths that are near the driver output pin. The series resistor that matches the transmission line characteristic impedance is placed very close to the driver. Additionally the connector has multiple ground connection points to minimize impedance issues.

High Frequency Output Current Path Differentially From 2 Amplifiers

- ◆ Minimize Loop Area on Driver Side.
- ◆ Utilize a single Capacitor between opposite amplifier supplies as this should be the main current flow. Adding this Capacitor can reduce 2nd-Order Distortion by 6 to 10dB!
- ◆ Use bypass caps to GND at a mid-point to handle stray-C return path currents but do not disrupt differential current flow.
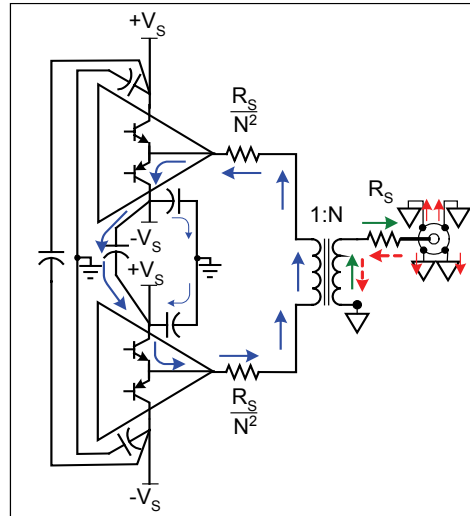

Using two individual amplifiers in a differential drive configuration, such as a ADSL line driver, also must follow the same concepts discussed previously. The use of a transformer helps isolate the driver-side current flow and the line side current flow. Since the drivers' outputs are differential, there must be a differential current flow from one driver to the other. The bypass capacitors allow this to occur and should follow the concepts previously discussed. The only difference here is we want to force the current to flow through a bypass capacitor connected from the positive supply of one driver to the negative supply of the other driver.

The use of bypass capacitors to the ground plane will still be required, as will be discussed later. To make sure the current does NOT flow into the ground, place these capacitors symmetrically to each other and connect the ground at the midpoint of the capacitors. The differential current flow should have no reason to go into the ground plane. Combined with the single capacitor across the supplies, this configuration can reduce even-order harmonics by 6 to 12dB.

Although not shown above, there will be interwinding capacitance across the transformer windings. There must be a way for high frequency current flowing through this capacitance to return back to the source, or else there can be issues.

High Frequency Output Current Path Differentially From Fully Diff. Amplifier

◆ Minimize Loop Area on Driver Side.
◆ Utilize a single Capacitor between opposite amplifier supplies as this should be the main current flow.
◆ Use bypass caps to GND at a mid-point to handle stray-C return path currents but do not disrupt differential current flow.
◆ Filter Cap should allow for small Loop Areas – including "kick-back" current flow.
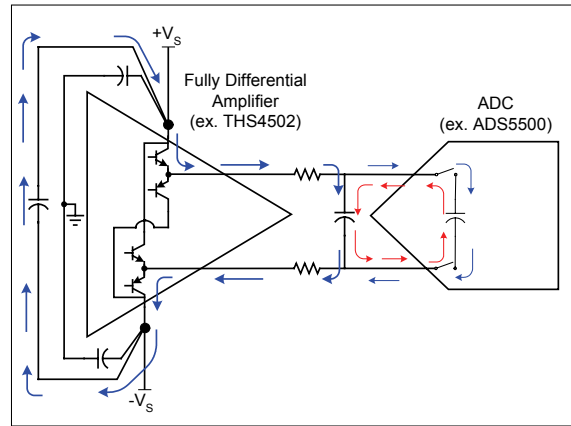
A fully differential amplifier follows essentially the same concepts as the single-ended differential driver. The only difference is the two outputs are in the same package. But, the bypass capacitors should follow the same principles as mentioned before – one capacitor form the positive supply to the negative supple, and the two bypass capacitors to ground should optimally be placed symmetrically to each other and connected to ground at the midpoint.

One of the most common uses for a fully differential amplifier is to drive an ADC. When doing this, pay attention to the current flows around the amplifier and the ADC (caused by the ADC's internal capacitor). Keep the paths as symmetrical as possible.

Why Add Bypass Capacitors to Ground?

- Allows Common-Mode Return Currents a path back to the source to complete the loop.

- Hopefully, does NOT disrupt Differential Current Flow – hence the mid-point grounding.

- Some of these currents will flow back into the opposite phased signal path through the stray capacitance.

+V_S

Fully Differential Amplifier (ex. THS4502)

ADC (ex. ADS5500)

Stray Capacitance

-V_S
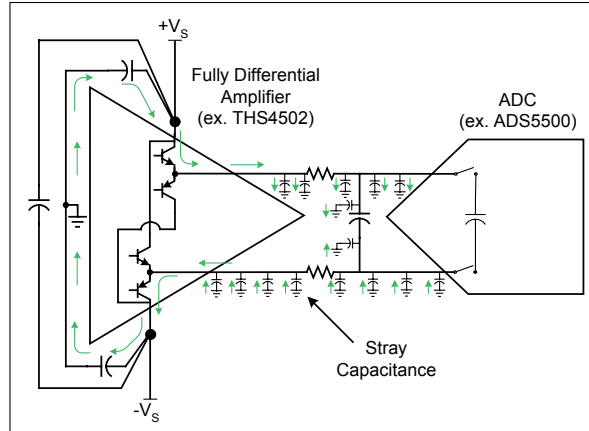
Remember: Minimize ALL Current Loops – Differential AND Common-Mode

Adding capacitors to ground, even in a fully differential system, needs to be done to account for the current flowing through the stray capacitance of the system. This stray capacitance can even occur inside the silicon of the driver and/or the ADC. As you know by now, the current will find a way back to its' source in-order to complete the loop. The bypass capacitors to ground allow this current flow to occur and will minimize the loop area.

Routing Differential Traces
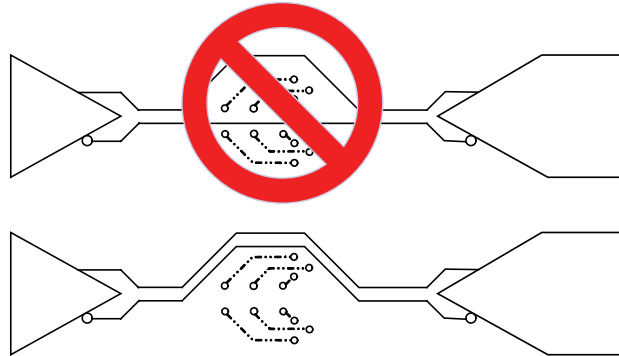
- ◆ Keep Differential Traces Close Together. Keeps noise injection as a Common-Mode Signal which is attenuated in the Differential System.
- ◆ Route Differential Traces Around Obstacles Together, Do Not Separate.
- ◆ Try to keep trace lengths the exact same length to keep delays equal.

When routing differential traces, they should always be routed together (side-by-side). This keeps any noise injection into the signal a true common-mode noise which gets rejected by the receiver. If noise only gets into one channel and not the other, the amount of rejection is minimal at best.

Additionally, the lengths of both traces should be kept the same length. Otherwise the signals can arrive at the receiver at different times and cause performance issues. This is especially true for very fast switching digital signals and very high analog signals (>1-GHz).

Differential Traces

MICROSTRIP
- ◆ Most Commonly Used
- ◆ Less Propagation Delay
- ◆ May Radiate more RF
- ◆ Only requires 2 Layers

STRIPLINE
- ◆ More Propagation Delay
- ◆ Better Noise Immunity/Radiation
- ◆ Requires at least 3 Layers
- ◆ May be harder to control Z0
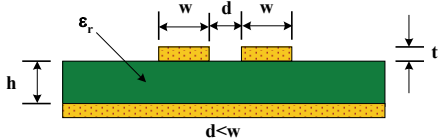
$$Z_{diff}(\Omega) \approx 2 * Z_0 \left(1 - 0.48e^{-\frac{0.96d}{h}} \right)$$
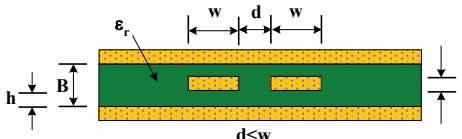
$$Z_{diff}(\Omega) \approx 2 * Z_0 \left(1 - 0.347e^{-\frac{2.9d}{B}} \right)$$

$$Z_0(\Omega) \approx \frac{60}{\sqrt{0.475\,\varepsilon_r + 0.67}} \ln\left(\frac{4\,h}{0.67(0.8w + t)} \right)$$

$$Z_0(\Omega) \approx \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4\,h}{0.67\pi(0.8w + 1)} \right)$$

Just like single traces, differential traces also can have a characteristic impedance dictated by the inductance and capacitance. Keeping the differential traces close together is highly desirable as it minimizes noise injection problems and minimizes the radiated electromagnetic field.

Differential Traces
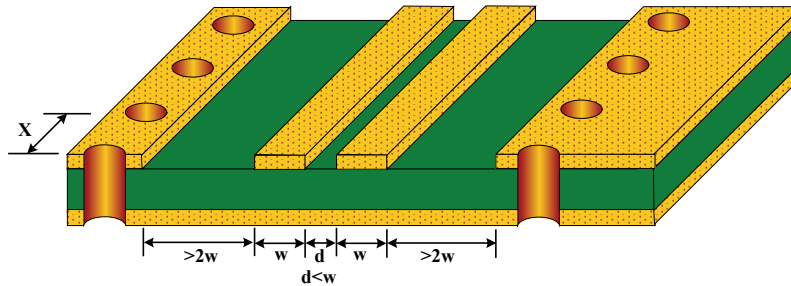
- ◆ Common to utilize GND plane on Top AND Plane Layers.
- ◆ GND plane on same layer should be $\geq$ 2 times the trace width. Reduces radiating magnetic field area and also susceptibility to extraneous signals.
- ◆ Ensure MULTIPLE Vias are utilized and placed near signal traces.
- ◆ Via distance apart (X) should be $\leq$ 0.25cm ($\leq$0.1").

It is common to use a ground plane on the signal layer. One benefit of this is it reduces the radiating magnetic field of the signal on the trace. If an adjacent ground plane is utilized, it is best to keep the distance between the trace and the ground plane equal to at least twice the trace width distance. This minimizes the capacitance of the plane which can alter the characteristic impedance of the trace.

Because there WILL be some capacitance between the trace and the same-layer ground area, there will be some current flow through this capacitance. To minimize the current flow loop area as much as possible, it is desirable to place vias connecting the two planes together. These vias should be spaced no more than 0.25cm (0.1") apart from each other for the entire length of the trace.

Taking a Look at Vias

◆ Must have Return Path Vias next to Signal Path Vias.

◆ Notice Large Current Density Area flow in return path.

◆ Will have a change in impedance with this configuration.
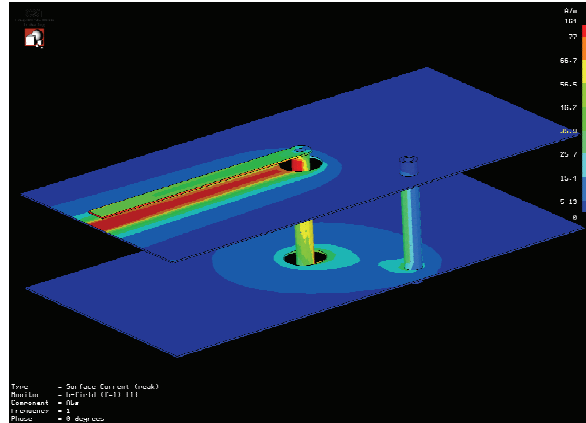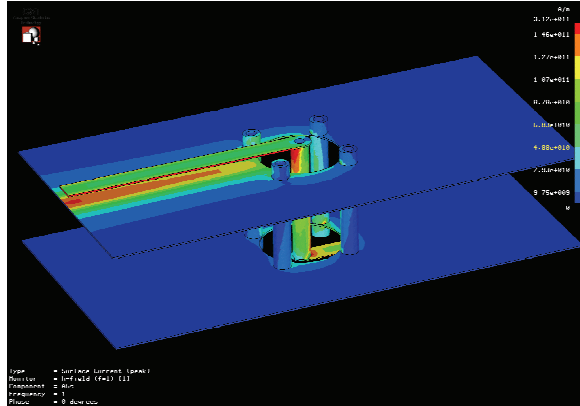

2-Layer PCB showing Current Density of PCB trace and Single Return Path Via.

Now let's take a look at vias once again. We know that the return current density follows the trace path directly under the signal trace. But what happens when the signal trace goes through a via? How will the return current flow form the bottom ground layer to the top ground layer? The current WILL find a way to do this, one way or another and you may not like the path it chooses.

To minimize this return current flow path problem, every time a via is utilized, a ground via should also be utilized next to the signal via. This allows the return current to flow near the signal current flow. But, the signal via flows through essentially a cylinder that wants to have the return current flow 360° around it. If a single ground via is used for the return current, the characteristic impedance of the trace will be altered slightly and may be an issue.

Controlled Impedance Vias

◆ Better Solution is to add Multiple Return Path Vias.

◆ Notice minimal Current Density Area Flow at vias.

◆ Improved impedance – reduces reflections.

2-Layer PCB showing Current Density of PCB trace and Multiple Return Path Vias.

The obvious solution to help maintain the characteristic impedance of the via is to use multiple ground vias around the signal via. Using 4-ground vias next to the signal via shows very good results and should be utilized if possible.

Controlled Impedance Vias
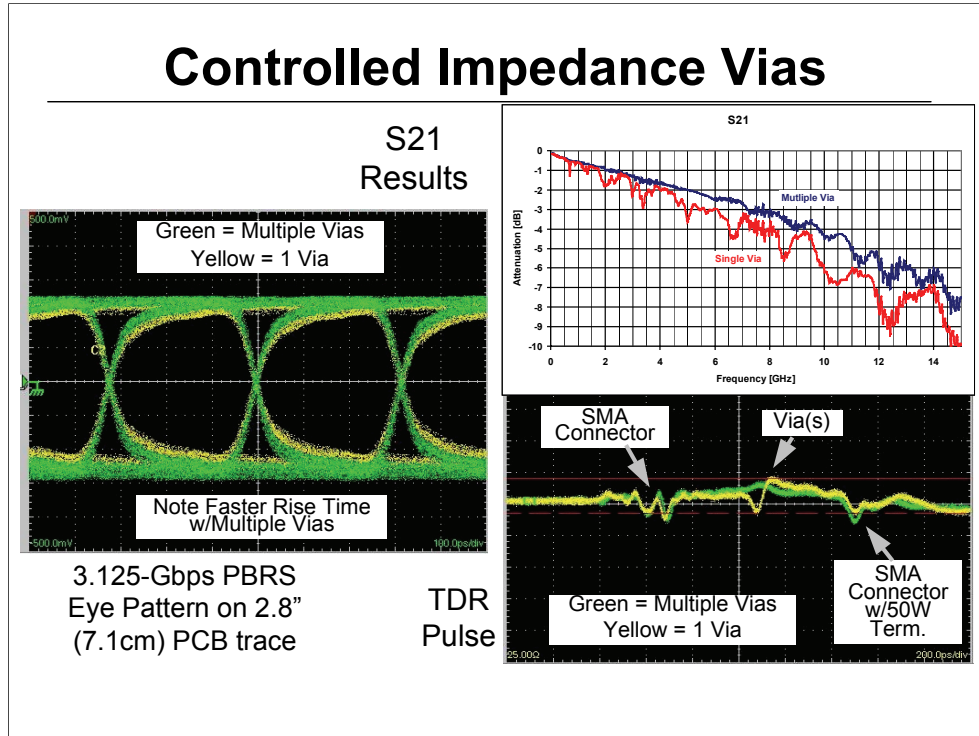
These graphs show the difference between a single ground via and the 4-ground via configuration. These tests are real results form a test PCB constructed to illustrate the differences between the two scenarios.

As these results show, using the 4-via configuration widens the PBRS (pseudorandom-bit-stream) eye pattern indicating a better high frequency system. It also improves the S21 (input reflection) considerably, and a TDR (time-domain-reflectometry) pulse shows improved impedance matching through the via.

For more information see the October 2, 2003 article in EDN magazine entitled "Designing Controlled-Impedance Vias" written by Thomas Neu, Texas Instruments.

Passive Component Models - Capacitors

Best Model

Ideal Model   Better Model

Impedance Vs. Frequency
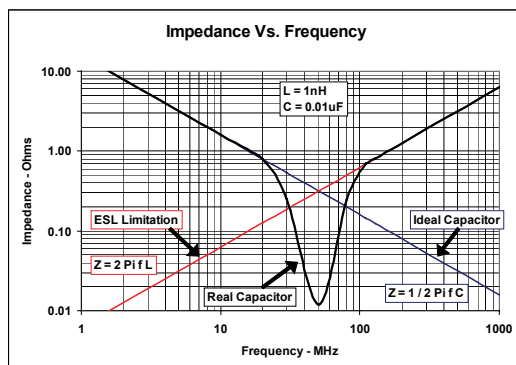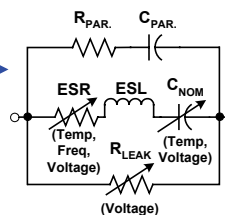
$$Z(\Omega)= \sqrt{(ESR)^2 + (X_{ESL} + X_C)^2}$$

$$X_{ESL}(\Omega)= 2\pi f L$$

$$X_C(\Omega)= \frac{1}{2\pi f C}$$

$$f_{RES} = \frac{1}{2\pi\sqrt{LC}}$$

Capacitors are utilized extensively within most systems. They are used for power-supply bypassing, AC-coupling, integrators, filtering, etc. But, capacitors are not perfect components. They have elements within them that limit their usefulness. The most pronounced elements are the true capacitance, the equivalent series resistance (ESR), and the equivalent series inductance (ESL). It is the ESL which causes the capacitor to stop behaving like a true capacitor at high frequencies as the impedance starts to increase rather than keep decreasing.

This ESL gets compounded when leaded capacitors are utilized rather than surface mount technology (SMT) capacitors. As the lead inductance increases, the high frequency impedance limitation also increases. This increase is directly proportional to the amount of lead inductance increase. For example, if the lead inductance of the example above increased from 1nH to 4nH by using a leaded ceramic capacitor, the impedance due to ESL increases by a factor of 4. The resonant frequency is also reduced by the square root of the increase, or by a factor of 2 for this example from 50MHz to 25MHz. It should be pretty clear that avoiding the use of any leaded device should be adhered to for high frequency designs.

It should also be noted that when multiple capacitors are placed in parallel, resonances can occur which cause a relatively high impedance to occur. If these resonances occur at the signal frequency or clock frequency, the effect of the capacitor is essentially nullified due to the high impedance at this resonant frequency. Sometimes adding a resistor in series should be done with one of the capacitors to dampen the resonance effect. Additionally, it has been found that sometimes simply removing one of the parallel capacitors actually can improve the system as the resonance is eliminated.

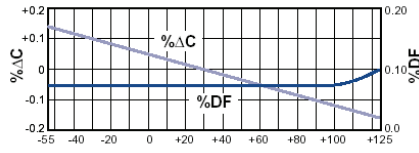**Passive Component Models - Capacitors**

EFFECT OF TEMPERATURE

Figure 3. Temperature °C
Capacitance & DF vs Temperature - C0G

Figure 4. Temperature °C
Capacitance & DF vs Temperature - X7R

Figure 5. Temperature °C
Capacitance & DF vs Temperature - Z5U

Ceramic Dielectric Materials and Common Tolerances:

COG (NPO) = ±30PPM (-55°C to +125°C)

X7R = ±15% (-55°C to +125°C)

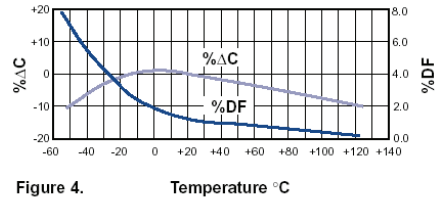Z5U = +22%, -56% (+10°C to +85°C)

Y5V = +22%, -82% (-30°C to +85°C)
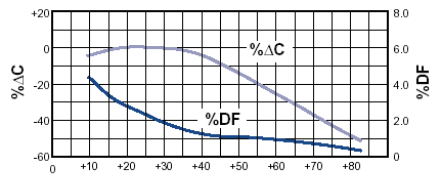
The material of the capacitor has a significant influence on the characteristics of the capacitor. The most widely used high frequency bypass capacitor is the ceramic capacitor. These typically come in the following grades rated from the best quality to the worst quality; COG (or NPO), X7R, Z5U, and Y5V grades. The problem with the grades is the capacitance value of each grade is limited in range. COG for example, is generally limited to less than 1000pF while the Y5V can be found in as high as 1µF values.

The COG grades are considered to have the best characteristics as their change in capacitance with temperature is the flattest of all with the lowest dissipation factor (DF). Dissipation Factor is the measure of losses in a capacitor under an AC signal. It is the ratio of the ESR to the capacitive reactance and is measured in percent. Where as the Y5V capacitance value can change between +22% to -82%. A 0.1µF Y5V capacitor could vary between 0.122µF to 0.018µF over temperature – which may cause some serious concerns.
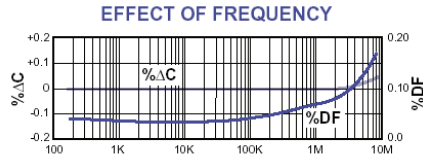
Passive Component Models - Capacitors

EFFECT OF FREQUENCY

Figure 8. Frequency - Hertz
Capacitance & DF vs Frequency - C0G
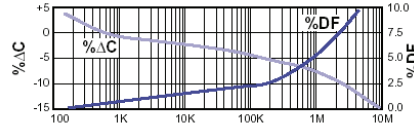
Figure 9. Frequency - Hertz
Capacitance & DF vs Frequency - X7R & Z5U
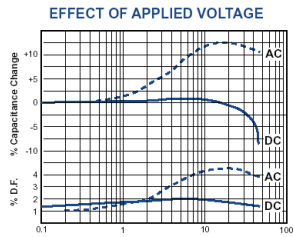
EFFECT OF APPLIED VOLTAGE

Figure 6. AC or DC Volts Applied
Typical Effects of 1000 Hz AC and DC Voltage Level on
Capacitance and Dissipation Factor - X7R
*Note: C0G Dielectric capacitance and dissipation factor are
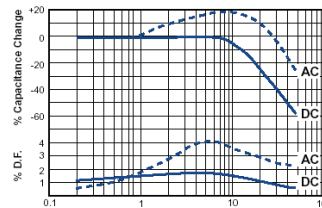stable with voltage.*

Figure 7. AC or DC Volts Applied
Typical Effects of 1000 Hz AC and DC Voltage Level on
Capacitance and Dissipation Factor - Z5U

Frequency also has an effect on capacitors. Again, COG (NPO) capacitors have the best characteristics varying less than 0.1% at 10MHz. A X7R and Z5U capacitor can vary as much as +5% to -15% from 100Hz to 10MHz.

Capacitors also vary with the voltage applied across them. The COG capacitor are considered to have negligible effects with voltage. But, the Z5U capacitor can vary by +20% to -30% with AC signals and 0% to -60% with DC.

This should show that if COG (NPO) capacitors are not used, make sure the capacitor that is chosen for the system meets the required capacitance value over temperature, frequency, and voltage.
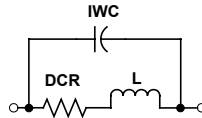
NOTE: typical plots shown are from Kemet Electronics Corporation SMT ceramic capacitor data sheets.
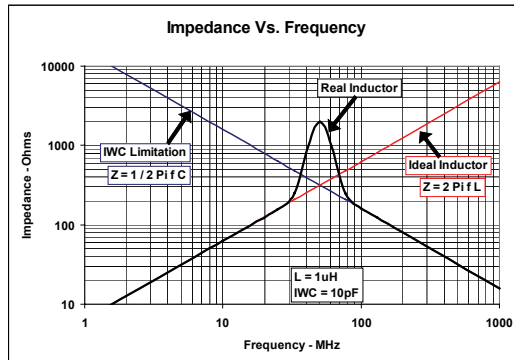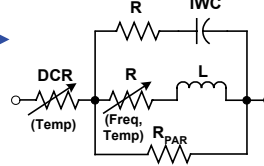
Passive Component Models - Inductors
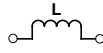
Ideal Model　　　　Better Model　　　　Best Model

$$Z(\Omega) = DCR + \frac{X_L\,X_{IWC}}{X_L + X_{IWC}}$$

$$X_L(\Omega) = 2\pi\,f\,L$$

$$X_{IWC}(\Omega) = \frac{1}{2\pi\,f\,C}$$

$$f_{RES} = \frac{1}{2\pi\sqrt{LC}}$$

Just as capacitors have other elements within them, inductors also have other elements. This includes the DC resistance (DCR) and the interwinding capacitance (IWC). Just as the capacitor stops behaving like a capacitor at high frequencies, an inductor stops behaving like an inductor at high frequencies. At the transition point the impedance will have a resonance causing a substantial rise in the impedance of the inductor. This resonance can cause issues in some situations and should not be ignored.

Passive Component Models - Resistors

Ideal Model   Better Model   Best Model
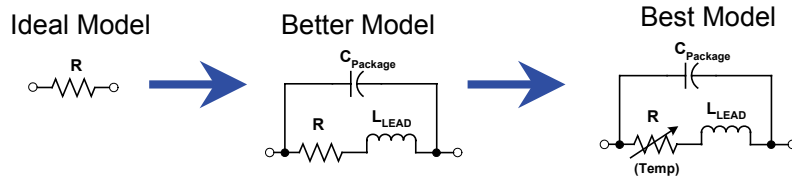
- Using SMT resistors minimizes lead inductance to the point that PCB traces are the limiting factor.

- SMT packages also minimize the capacitance between the leads such that this parasitic is usually insignificant.

- Note that resistor packs CAN have significant lead inductance and resistor-to-resistor capacitance, so choose wisely based on the application.

- Resistors will have temperature coefficients, 200PPM is common, but higher precision is available.

- AVOID Wire-wound resistors and leaded resistors for high speed applications due to their large inductance.

Resistors also have elements which make them have a frequency dependence characteristic. The capacitance is usually caused by the resistor package and the PCB mounting pads. The inductance is caused by the resistor leads and the PCB trace length.

In general, these extra elements can be ignored if the resistance value is relatively low – below 1k-ohm for example. But, they cannot be ignored if leaded resistors or wire wound resistors are utilized.

Bypass Capacitors

- ◆ DO NOT have vias between bypass caps and active device – Visualize the high frequency current flow !!!
- ◆ Ensure Bypass caps are on same layer as active component for best results.
- ◆ Route vias into the bypass caps and then into the active component.
- ◆ The more vias the better.
- ◆ The wider the traces the better.
- ◆ The closer the better (<0.5cm, <0.2")
- ◆ Length to Width should not exceed 3:1
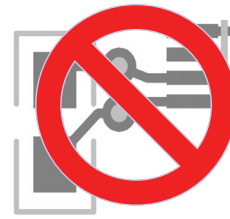
Poor Bypassing
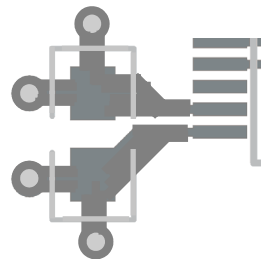
Good Bypassing

Now that the characteristics of a capacitor are known and the proper one has been selected, the next thing to do is place it on the PCB. For bypass capacitors this can be a concern if done without taking time to think about the high frequency implications of routing. The rule of thumb of placing capacitors as close as possible to the IC power input pins should be adhered to. Otherwise there can be too much inductance and a resonance effect can take place along with the straight forward impedance increase due to the inductance.

Typically the power and ground are on inner layers of the PCB and must be brought up to the IC level by vias. As we have learned, the more vias utilized, the lower the impedance. So using multiple vias is highly recommended for BOTH power supply voltage connection and Ground connection.

Additionally, the vias should run into the capacitor and then into the IC. This forces the current flow into the capacitor. Placing vias directly on the capacitor mounting pads can be an effective way to minimize routing area and still achieve the current flow routing.

Low Speed Techniques to Avoid

Low Speed Techniques are typically used for circuits with
Amplifiers and/or Data Converters with speeds ≤1MHz

Common Things to Avoid:
◆ Ground Planes
   ▪ Common to Pour Copper Planes Everywhere
   ▪ Instead, use with caution – Causes STRAY CAPACITANCE
◆ Guard Rings
   ▪ Typically used to minimize Leakage currents
   ▪ Just like Ground Planes, use with caution – Stray Capacitance
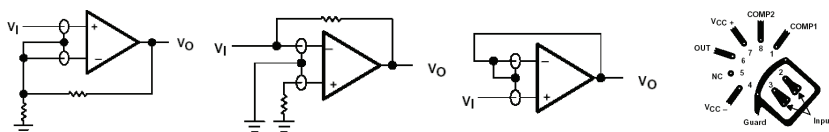
"Low Speed" techniques are considered things done that work acceptably
at frequencies below 1MHz. But would cause issues at frequencies above
10MHz.

Some of the most common mistakes are due to the capacitance issue.
Having ground planes everywhere can be a good thing as it reduces
inductance and creates a bypass capacitor. But, if placed in the wrong
spot, it can be disastrous to the system.

The use of guard rings for low leakage systems should generally e avoided
as this also causes capacitance to occur in sensitive areas of an amplifier
– most notably the inverting input node (aka summing node).

Another rule is to use low value resistors. Using anything above several k-
ohms is generally not recommended. This is because even a small stray
capacitance of 1-pF with a 10-kohm resistor can cause a pole (or worse
yet a zero) to occur at 16MHz, which is typically well within a high speed
amplifier's frequency of operation causing stability issues.

Lastly, minimize trace lengths to avoid trace inductance which can also
cause instability concerns if in the wrong spot.

Stray Capacitance

Stray Capacitance is Good and Bad

◆ Good because it helps form a characteristic impedance (Z0) when desired.

◆ Bad because it causes capacitance when a characteristic impedance is NOT desired. This can slow down a signal or cause an amplifier to ring or oscillate.

◆ Dominated by Layer-to-Layer Capacitance due to Surface Area. Trace Height (thickness) is very small (0.001" typ.), thus small area and capacitance.
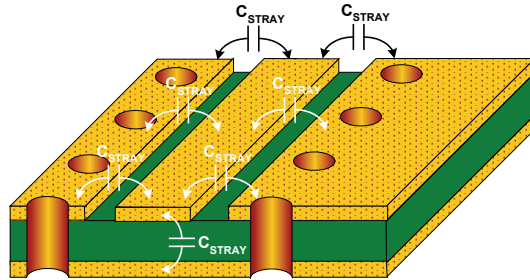

Having stray capacitance is a requirement to create a characteristic impedance for a transmission line. But, a transmission line is not always required – in fact it is often not required within the system but only for external interfacing.

If a transmission line is not required, then this capacitance can be detrimental to the system. It can slow the signals significantly down and also cause zeroes to occur in an amplifier which can lead to oscillations.
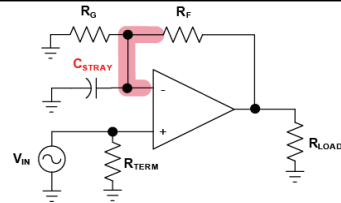
Stray Capacitance - Reducing

Possible Solutions

◆ If trace is NOT a characteristic impedance, reduce it's width. Not too much or else inductance can increase too much.

◆ Remove the GND plane under the trace. Connect the planes elsewhere.

◆ Increase distance between trace and same-Layer GND plane.
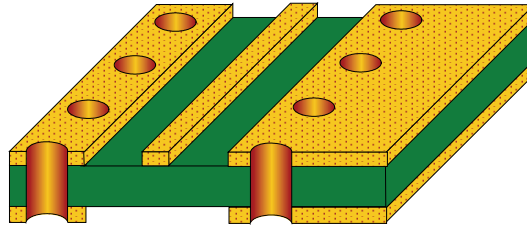
To minimize stray capacitance, it is as easy as separating the ground plane away from the signal trace. This can involve increasing th distance on the top layer, and/or removing the ground plane below the signal trace.

Remember, power planes are considered AC grounds and behave exactly the same as a ground plane. So removing the power planes is as important as removing the ground planes in sensitive areas. This is often referred to as moating.
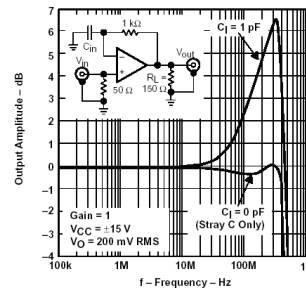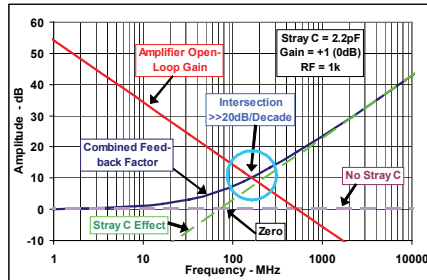
Stray Capacitance and Amplifiers

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(1 + 2\pi\, C_{STRAY}\, R_G\right)$$

$$f_{ZERO} = \frac{R_F + R_G}{2\pi\, C_{STRAY}\, R_F\, R_G}$$

◆Inverting Node (-) of Any Amplifier is Very Sensitive to Stray Capacitance

◆As Little as 1pF of Stray Capacitance can cause stability problems

◆Node includes Entire Trace up to the placement of RF, RG, and any other Component on (-) Node

As discussed, having stray capacitance at the wrong place can cause serious concerns. Having stray capacitance at the inverting node of an amplifier is one of those places. The stray capacitance causes a zero in the transfer function. If the zero intersects the amplifier's open-loop response at a 40-dB/decade rate of closure, this will cause the amplifier to be unstable and it will oscillate. Having as little as 1-pF can cause problems with the system.

Remember that the inverting input node includes everything connected to it up to the point there is some resistance or impedance of reasonable value (ie. >50-ohms).

Minimizing Stray C at (-) Input

Solutions:

◆ Eliminate Ground Planes and Power Planes near (-) input node.

◆ Shorten trace by moving components closer to (-) input pin.

◆ Reduce RF value

◆ Increase Gain of System

◆ Use Inverting Configuration which bootstraps voltage at (-) node minimizing the effects of Stray Capacitance

◆ Place Compensation Capacitor Across RF – Cancels Stray C

$$C_{COMP} = \frac{R_G}{R_F} C_{STRAY}$$

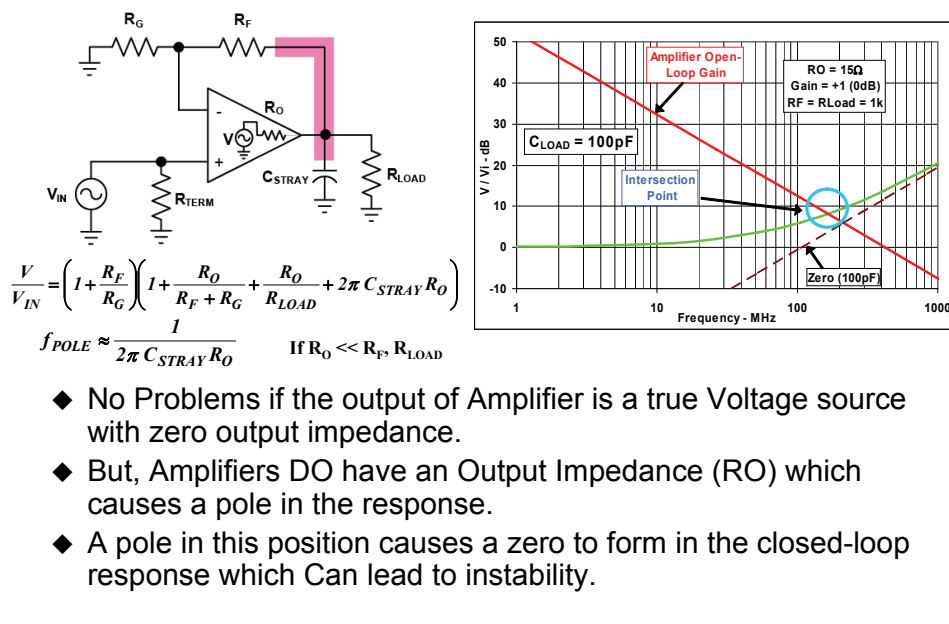**Compensation**
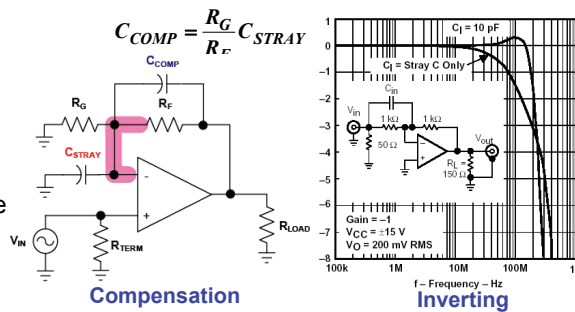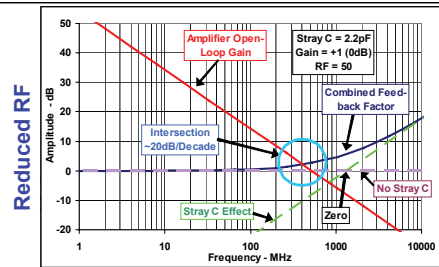
Inverting

There are several ways to minimize the effects of stray capacitance at the inverting input node of an amplifier. These are illustrated above.

The fundamental task at hand to make the amplifier stable once again is to reduce the intersection point of the noise gain and the open-loop response to as close to a 20-dB/decade rate of closure as possible. Even if this is close, this should be sufficient to create a stable system.

For more information on some of these techniques, refer to the TI Application Report entitled "Effect of Parasitic Capacitance in Op Amp Circuits", SLOA013.

Stray Capacitance and Amplifiers

$$\frac{V}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(1 + \frac{R_O}{R_F + R_G} + \frac{R_O}{R_{LOAD}} + 2\pi\, C_{STRAY} R_O\right)$$

$$f_{POLE} \approx \frac{1}{2\pi\, C_{STRAY} R_O} \qquad \text{If } R_O \ll R_F, R_{LOAD}$$

- ◆ No Problems if the output of Amplifier is a true Voltage source with zero output impedance.
- ◆ But, Amplifiers DO have an Output Impedance (RO) which causes a pole in the response.
- ◆ A pole in this position causes a zero to form in the closed-loop response which Can lead to instability.

Stray capacitance at the output of high speed amplifier can also cause the amplifier to become unstable. This is caused by the pole formed by the amplifier's internal resistance and the capacitive loading. This RC network causes a zero to occur in the feedback system of the amplifier.

Just like the stray capacitance at the inverting input node, stability is dictated by the noise gain of the amplifier intersecting the open-loop gain and should be as close as possible to the 20-dB/decade rate of closure as possible.
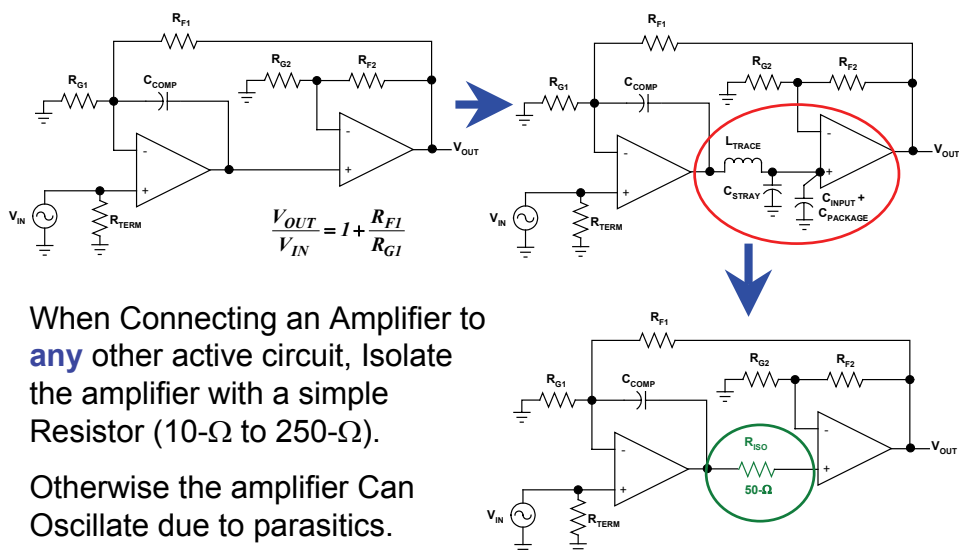
Minimizing Stray C at Output

Solutions:

- **Eliminate Ground Planes and Power Planes under output node.**
- **Shorten traces by moving components closer to output pin – especially Series Matching R.**
- **Increase Gain of System**
- **Increase Noise Gain of System**
- **Use Feedback Compensation.**

Adding Series R for Isolation   **Increasing Noise Gain Only**   **Feedback Compensation**
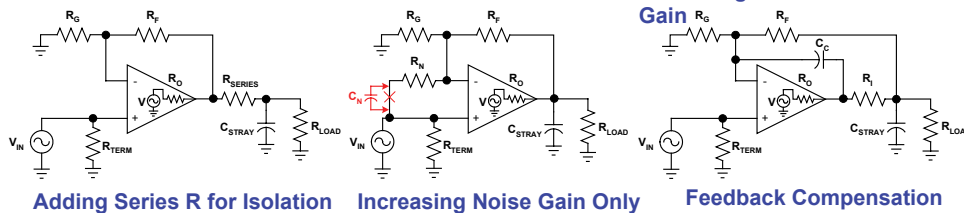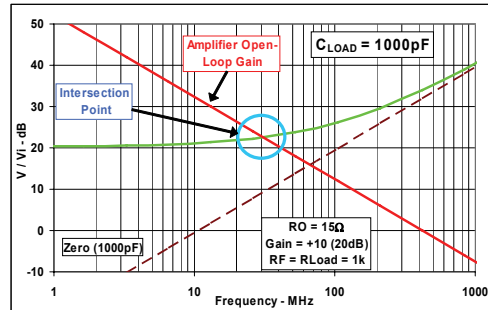
Solving the stability of the amplifier with a capacitive load can be relatively simple. Most common ways are to isolate the capacitive load by some real resistance. Another way to make the amplifier stable is to increase the gain of the amplifier, or increasing the noise gain of the amplifier, which both attempt to reduce the rate of closure to the 20-dB/decade goal for stability.

Connecting Amplifiers

When Connecting an Amplifier to **any** other active circuit, Isolate the amplifier with a simple Resistor (10-Ω to 250-Ω).

Otherwise the amplifier Can Oscillate due to parasitics.

$$\frac{V_{OUT}}{V_{IN}} = 1 + \frac{R_{F1}}{R_{G1}}$$

Sometimes high-speed amplifiers need a series input resistor, because package parasitics become more and more apparent at higher signal frequencies. Package parasitics are mainly due to the leadframe pins, bondwire and the IC die itself. The pins and bondwire can be modeled as high frequency inductors, with small capacitors between each. The die adds parasitic capacitance from the bondpad on the die to the die substrate.

All together, these parasitics can form resonant circuits, with high Q values and resonant frequencies in the hundreds of MHz. Most problems that are created by these parasitics occur at the high impedance input of the IC. Even if the overall bandwidth of the IC is much less than the resonant frequency, the transistors in the input stage can still be affected.

An indication of problems associated with the parasitics is higher than expected gain peaking of the amplifier. A series input resistor will help prevent excessive gain peaking problems or even oscillation by dampening the parasitic LC circuit. Typical values for this resistor are between 10Ω to 250Ω. The value can vary widely because of different PC-board parasitics that will add to this problem.

One rule, however, exists: the smaller the package the less its parasitics and the smaller the associated effects. Therefore, designers should choose SOIC (or smaller) packages over DIP packages whenever possible.
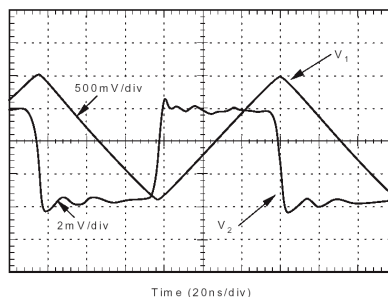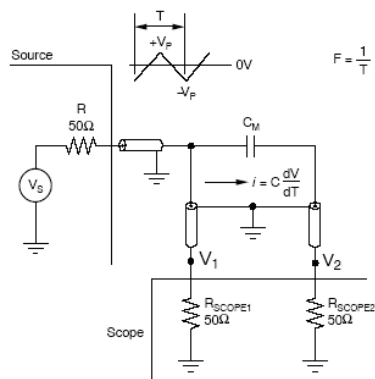
Measuring PCB Parasitic Capacitance

After building a PC boards one often is not sure the traces have the correct inductance or capacitance. It's even more difficult to measure those values without network analyzer or TDR.

A very easy way to measure trace's capacitance is to use a ramp generator and oscilloscope, with the hook-up shown here.

$$i = C\frac{dV}{dt} \rightarrow \frac{dV}{dt} = \frac{2 \cdot V_{1PP}}{\frac{T}{2}} = V_{1PP} \cdot F \cdot 4$$

$$V_{2PP} = (50\Omega)C\frac{dV}{dt} = (50\Omega)C \cdot V_{1PP} \cdot F \cdot 4$$

$$C_M = \frac{V_{2PP}}{V_{1PP}} \cdot \frac{1}{4(50\Omega)F}$$

See application note SB0A094 Measuring Board Parasitic in High Speed Design

In some cases, it is desirable to know how much parasitic (stray) capacitance is actually on a trace. This may help determine stability problems or to verify a characteristic impedance.

A relatively simple way to measure this is with the above test set-up. This set-up uses an HP8116A function generator (V_{gen}) to drive a tiangle wave through coaxial cable where one end is solder to the boards trace, ground plane, etc and two identical points are measured using an oscilloscope terminated in 50Ω.

This method can measure capacitance to an accuracy of 30f to 50f and includes fringing effects associated with high frequency fields.

See the TI Application Report entitled "Measuring Board Parasitics in High-Speed Analog Design", SBOA094
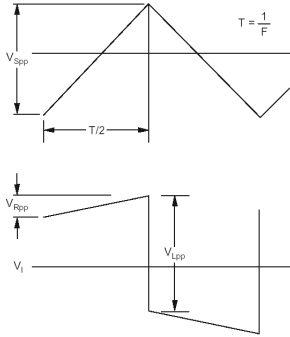
Measuring PCB Parasitic Inductance

A very easy way to measure trace's Inductance is to use a ramp generator and oscilloscope, with the hook-up shown here.
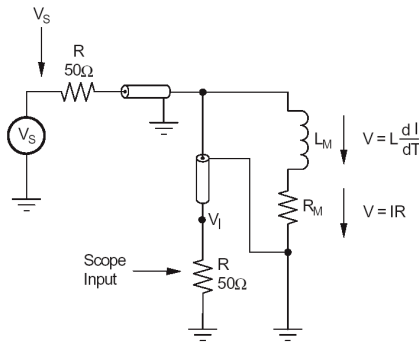
$$\frac{V_{S_{PP}}}{R} = I_{TEST}$$

$$V_{L_{PP}} = \frac{L_m \cdot 2 \cdot V_{S_{PP}}}{\frac{R \cdot T}{2}} = \frac{L_m \cdot 4 \cdot F \cdot V_{S_{PP}}}{R}$$

$$L_m = \frac{V_{L_{PP}} \cdot R}{4 \cdot F \cdot V_{S_{PP}}} \qquad R_M = R \frac{V_{R_{PP}}}{V_{S_{PP}}}$$

Very similar to measuring the capacitance of a PCB trace, this set-up shows how to accurately measure a PCB trace's inductance.

Example of High Speed PCB - Schematic

- ◆ Multiple Caps for Low Freq. and High Freq. Bypassing
- ◆ Look for ALL Current Paths and their Loops
- ◆ Pay attention to Sensitive Inverting Input Node
- ◆ Match Impedances
- ◆ Ferrite Chips Used to Isolate Power Supply Currents
- ◆ SMA Connectors
- ◆ Small (0603) Components to minimize Inductance
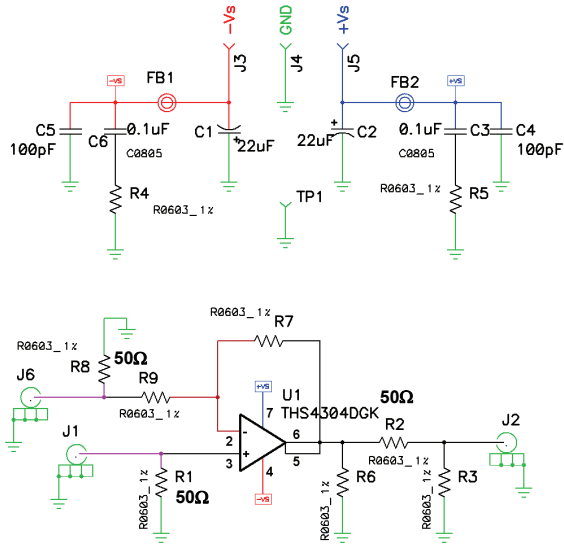
Let's see an example of a high speed PCB looks like. This is a schematic for the THS4303, a very high speed voltage feedback op-amp that has a bandwidth greater than 1.5-GHz. With such high bandwidth, the design must pay attention to all high speed constraints or else the amplifier will be unstable.

Example of High Speed PCB - Layout

TOP LAYER Attributes

- Signal In/Out traces are microstrip line with Z0 = 50Ω.
- Terminating Resistors next to Amplifier.
- Output Series Resistor next to Amp.
- 100pF (NPO HF) Bypass Caps next to Amp.
- Larger Bypass Caps Farther Away with Ferrite Chips for HF isolation of currents.
- MULTIPLE Vias Everywhere to Allows for Reduced Current Flow Area – Although not able to be seen here, Vias are also on Component solder pads (See other Layers).
- Short, Fat Traces to reduce inductance – even on Feedback Trace (THS4304 BW-3dB>1GHz).
- Large Solid Ground Plane – No Spokes
- Side Mount SMA connectors for Smooth Signal Flow
- Rounded Signal Traces, no 90° bends
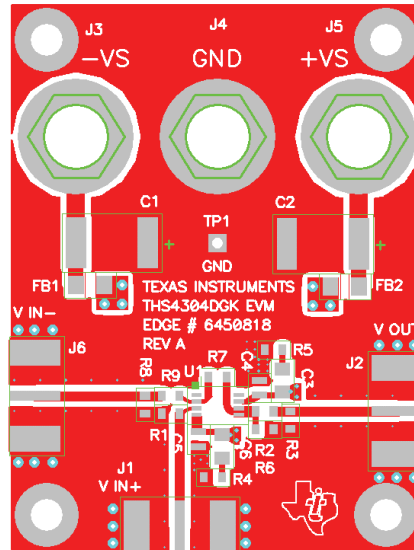
The top layer of the PCB is shown. Because this si a relatively simple system, all of the components are mounted on the top layer. This eliminates the signal trace via concerns to ensure the best situation possible.

Example of High Speed PCB - Layout
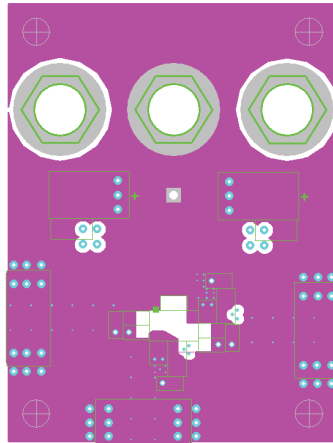
Layer 2: Signal GND Plane

GND Plane Next To Signal Plane for Continuity in Return Current Flows.
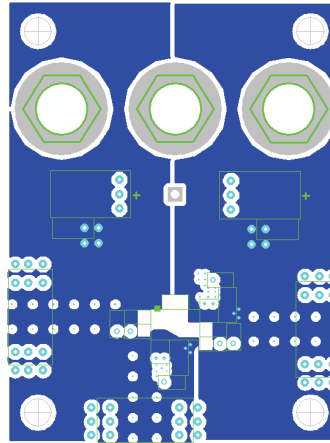
Layer 3: Power Plane

Notice Cut-Out in Sensitive areas near Amplifier on ALL planes.

Notice the Ground layer is directly below the signal layer. This is to allow for the return current signal flows to be as close a possible to the signal traces. The PCB material thickness also dictates the characteristic impedance input and output traces.

The power layer is below the ground layer, which helps form a good bypass capacitor by using the simple parallel plate capacitor method.

Notice the removal of ground plane and power plane around the sensitive areas of the amplifier. This includes the inverting input node, the feedback capacitor trace path, and the output node up to the series characteristic impedance matching resistor.

Also notice that multiple vias are placed on the component pads (SMA connectors and bypass capacitors for example).

Example of High Speed PCB - Layout

Bottom Layer – GND Plane
- Solid GND plane to minimize inductance.
- Layer-2 GND plane and Bottom Layer form excellent bypass capacitor with Power Plane.
- All Signals are on Top Layer to minimize the need for signals to flow through vias.
- Again, Multiple Vias Everywhere
- Cut-Out around Amplifier to reduce Stray Capacitance – except when turned into Microstrip Line
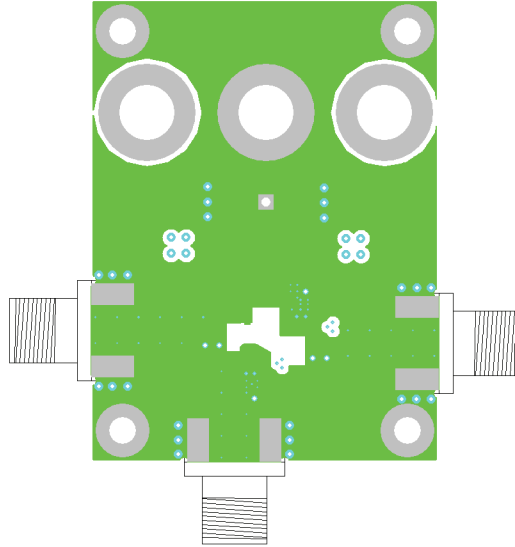

Notice the number of vias utilized between the top layer ground, second-layer ground, and the bottom layer ground. This ensures minimal current loop areas allowing the return currents to flow where they want to flow – directly under the signal trace.

Lastly, there are NO spoke connections to any ground point. This solid connection ensures minimal inductance and although not really required for this design, good thermal conductivity.

Thermal Issues – Silicon

- ◆ Junction Temperature should be kept below 125ºC
    - ▪ Process Limit = 150°C
    - ▪ Usable Electrical Limit = 125°C
- ◆ Amplifier performance degrades with high junction temperature
- ◆ True For ALL semiconductor amplifiers – not just TI
- ◆ Lower Junction Temperature Improves Long-Term Reliability
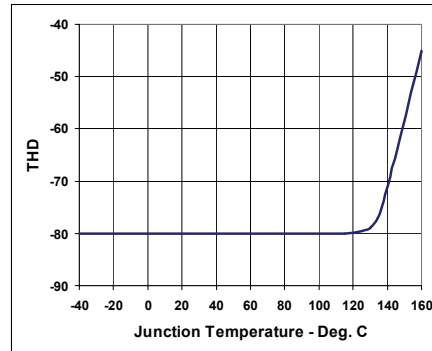
Thermal issues often arise in many systems. As far as the integrated circuit is concerned, the silicon temperature has a working area that is defined by the process of the silicon. Elevated junction temperatures can reduce long term reliability resulting in a part that ultimately fails.

Additionally, the performance of the part typically start to degrade at temperature extremes – both hot and cold. So it makes sense to pay attention to the thermal characteristics of the part, the power dissipation of the part, which package to use, and ultimately the PCB layout.

PowerPAD Package on 4-Layer PCB

PowerPAD™

Heat Transfer

Top Trace

V_{DD}

GND

Bottom Trace
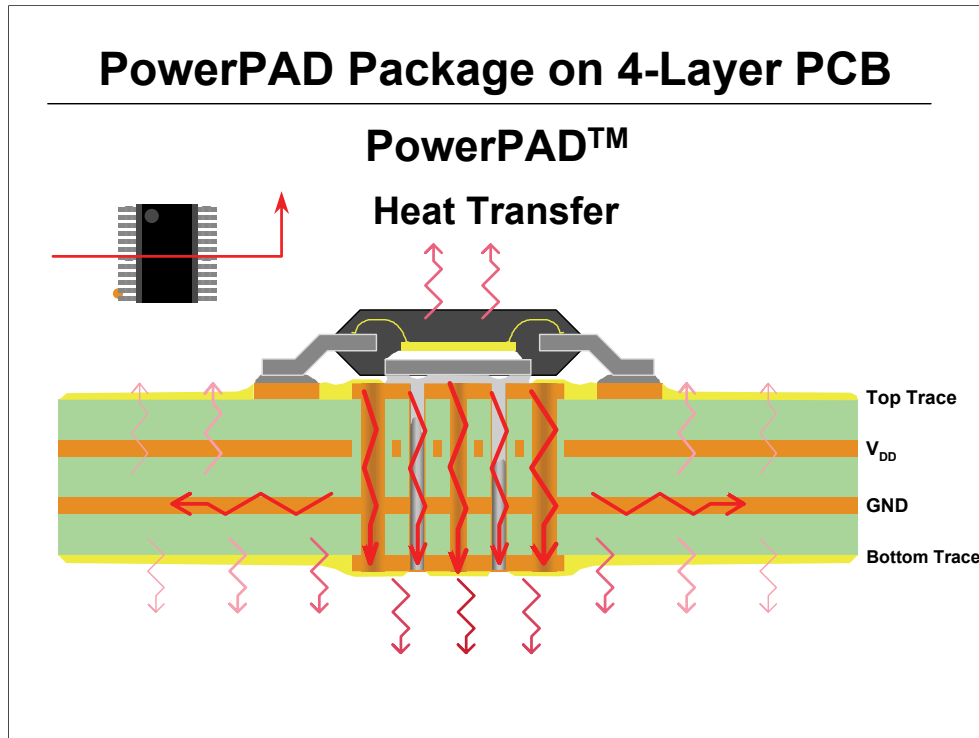
Utilizing the copper planes on the PCB for thermal conduction is an excellent way to remove the heat from an IC. The use of a PowerPAD can allow over 3X better heat dissipation that a traditional package without the thermal pad while still using the same footprint.

Thermal Management

◆ Must do thermal management at the device, the board, and the box levels

- Device: proper package heat sinking
  - Thermal vias to Cu planes
  - Unobstructed airflow
  - Soldering the device thermal pad to the PCB
- Board level
  - Heat flow out of the board
  - Air flow, PCB card guides, PCB with metal heat sinks
- Other Devices
  - Other Active parts generate Heat
  - Can cause localized hot-spots on PCB – effectively reducing thermal flow and increasing Silicon Temp.
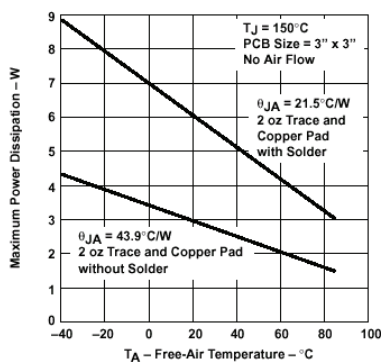
See Application note SPRA953 – IC Package Thermal Metrics for more information. The only thing that must be done is to lay out the PCB correctly for this pad and soldering the part to the pad. Failure to solder the pad to the PCB will result in an increase in thermal resistance and cause the junction temperature to rise which may hinder it's performance or reduce the long term reliability.

See Application note SLMA002 –"PowerPAD Thermally Enhanced Package" for more information.

Thermal Calculations

$$\Theta_{JA} = \Theta_{JC} + \Theta_{CA}$$

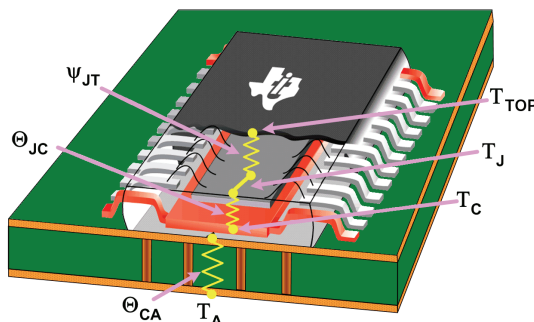$$Power = \frac{T_{JUNCTION} - T_{AMBIENT}}{\Theta_{JA}}$$

q_{JC} = Thermal Resistance from Junction to Case (°C/W)
q_{CA} = Thermal Resistance from Case to Ambient (°C/W)
q_{JA} = Thermal Resistance from Junction to Ambient (°C/W)

Remember θ_{CA} is dependant upon package, PCB design, and external environment.

Thus, θ_{JA} can fluctuate considerably from design to design!!!

$$T_{JUNCTION} = T_{TOP} + (\Psi_{JT} \cdot Power)$$

Ψ_{JT} is useful to calculate Junction Temperature

Ψ_{JT} is NOT a true Thermal Resistance – Only used as a Tool

Trying to figure out what the silicon junction temperature really is can be quite a daunting task. But using simple formulas can make things go quickly. The hardest part about doing thermal calculations is trying to figure out the PCB thermal impedance. Every PCB design is different which results in the Θ_{CA} value to be different. Add to the fact that other active devices, and some passive devices too, create heating of the PCB, the design can be difficult.

Once a PCB is built and populated, one way to measure the silicon junction temperature is by using the Ψ_{JT} formula. For PowerPAD packages, the dominant heat flow is through the PowerPAD itself. Very little heat flows through the package. But it is difficult to measure the case temperature as it is soldered onto the PCB.

Ψ_{JT} allows you to simply measure the top of the package, and quickly calculate the junction temperature. This is not a thermal resistance in the classical sense as there is essentially no heat flow through this point. But rather it is a measurement tool to simplify the measurement of the junction temperature.

See Application note SPRA953 – IC Package Thermal Metrics for more information.