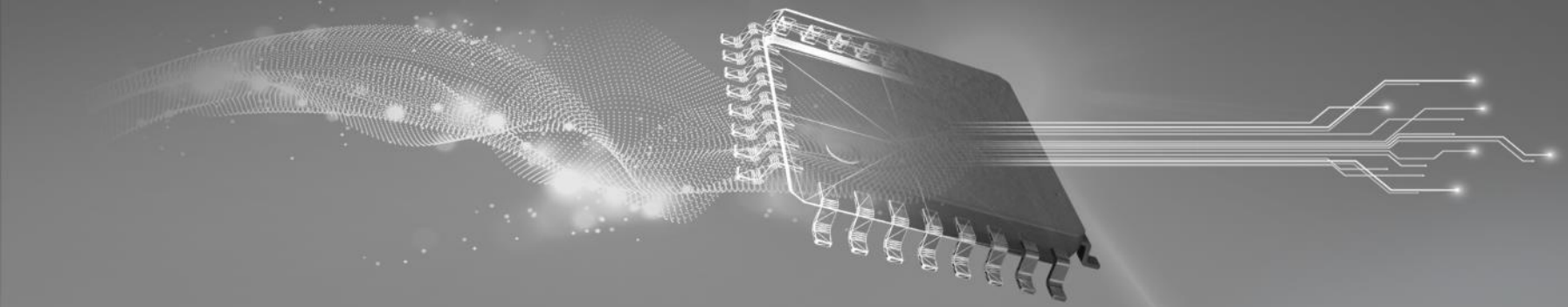
TI TECH DAYS



Power design with thermal reliability in mind

Presenter: Alejandro Iraheta and Jimmy Hua

Alejandro Iraheta

Analog Power - Applications Engineer

Career

- Electrical Engineering degree from Florida Atlantic University
- Joined TI through Application Rotation Program (Feb. 2018)
  - TI power modules group (2018)
  - Converters & modules, low-current (Aug. 2020)

Role

- Responsibilities as an Applications Engineer in the converter & modules team:
  - Customer and FAE support
  - Technical documentations: data sheets, application notes, user guides
  - New products development
  - Creating training presentations and field collateral

Jimmy Hua

Analog Power - Applications Engineer

Career

- Electrical Engineering degree from University of California, Davis
- Joined TI through Application Rotation Program (2016)
- Joined TI power modules group (2017)
- Controllers, converters & modules, high-current (Aug. 2020)

Role

- As an applications engineer in the power modules team I am responsible for customer and FAE support, writing data sheets and application notes, new product development, and creating training presentations and field collateral.

Agenda

1. **Thermal design primer**
   - Thermal design terminology and datasheet specifications.

2. **Package comparison**
   - Benefits of HotRod™ QFN package.
   - Comparing HotRod™ QFN and standard wirebond QFN package.

3. **Designing calculations for PCB thermal performance**
   - Calculating power dissipation and maximum junction-to-ambient thermal resistance.
   - Estimating the minimum board area for PCB thermal performance.

4. **Design examples and data**
   - Evaluating thermal performance between SOIC and HotRod package.
   - Evaluating Enhanced HotRod™ QFN package and HotRod™ QFN package.

5. **Thermal tools and PCB layout considerations**
   - Tools: thermal estimator excel and PCB online calculator tool, WEBENCH® Power Designer tool.
   - PCB layout considerations: copper area, copper thickness, vias, and copper planes.

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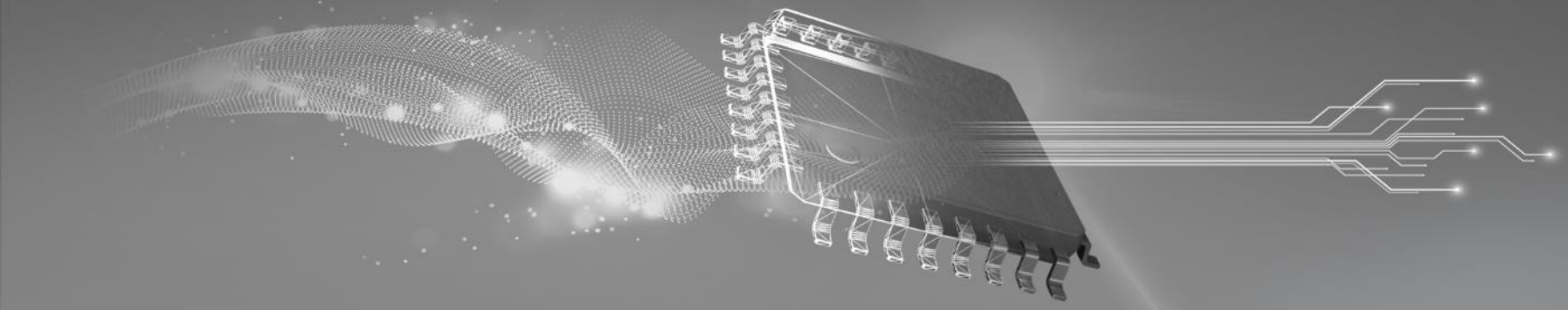


Thermal design primer

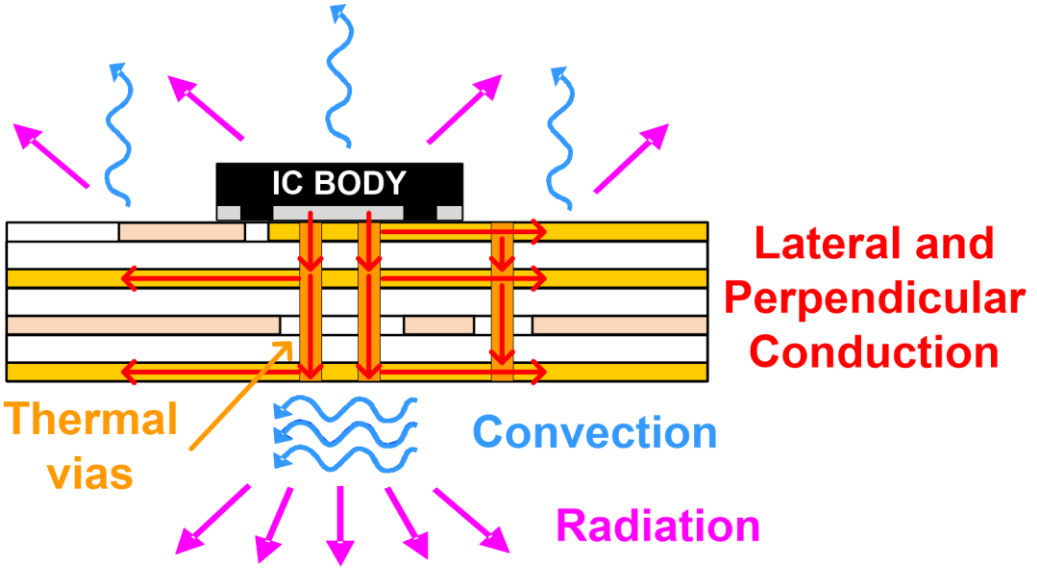
Heat transfer

IC Power Loss is Heat

- Conduction: The transfer of energy between objects that are in physical contact (primary path for heat leaving the IC package).
- Convection: The transfer of energy between an object and its environment (primary path for heat leaving the PCB).
- Radiation: The transfer of energy to or from a body by means of the emission or absorption of electromagnetic radiation.
  - The secondary path for heat leaving the PCB and the IC package.
  - Goal: provide minimum resistance path for heat flow.
    - » Minimum IC temp rise

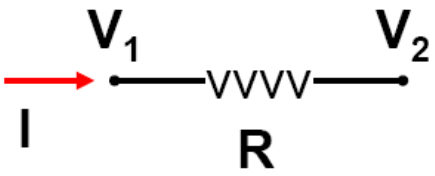
Heat transfer basic theory

- Conduction: $Q = \frac{k \times A \times \Delta T}{L}$
- Convection: $Q = h \times A \times \Delta T$
- Radiation: $Q = \varepsilon \times \sigma \times A \times \left(T_b^4 - T_a^4\right)$
- Where:
  - Q = heat
  - k = material conductivity
  - A = area
  - L = thickness (length)
  - h = convection coefficient
  - ΔT = temperature delta
  - ε = emissivity
  - σ = Stefan-Boltzmann constant



Thermal and electrical resistance

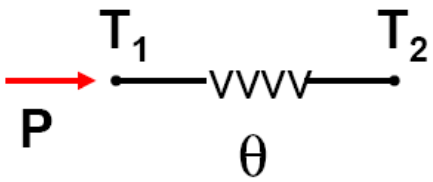
Electrical Resistor



$R = (V_1 - V_2) / I$

$$I \times t = Q$$

Thermal Resistor



$\theta = (T_1 - T_2) / P$

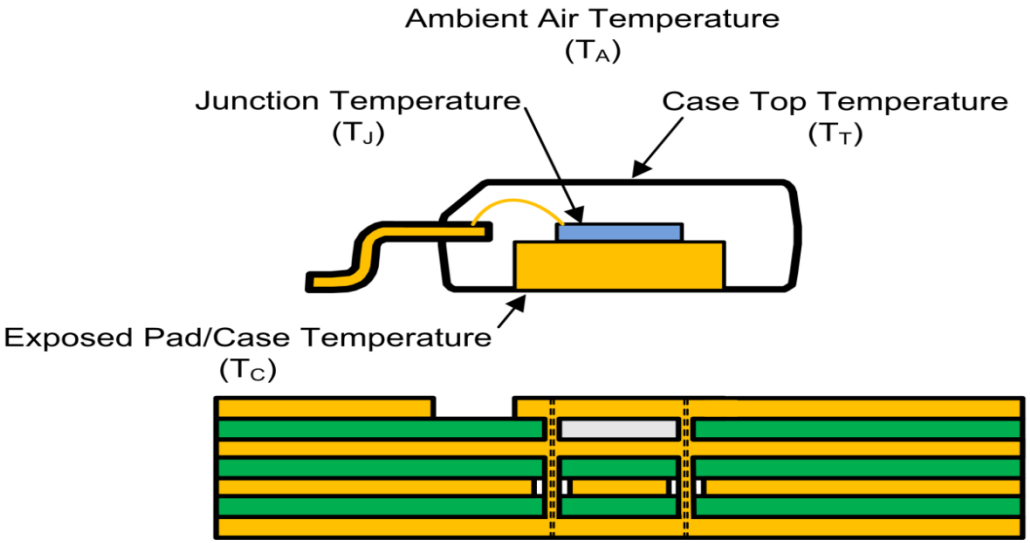
$$P \times t = Q$$

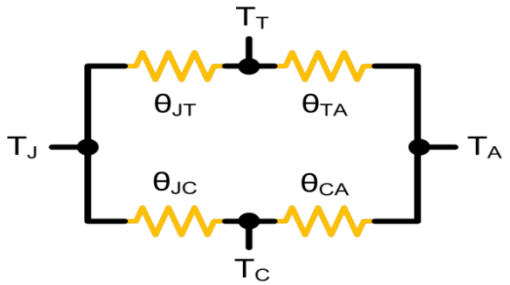
Temperature -> “Thermal potential”
Power -> “Thermal current”
Heat -> “Electrical charge”

Electrical => Q is charge

Thermal => Q is heat

Thermal design terminology





At each interface from the junction to the ambient air there is an associated thermal resistance.

Goal of thermal management

Maximum junction temperature.
Given in data sheet of converter; usually 125°C or 150°C

Power dissipation of converter.
Depends on required output power and converter efficiency

$$T_J = T_A + P_D \cdot \theta_{JA}$$

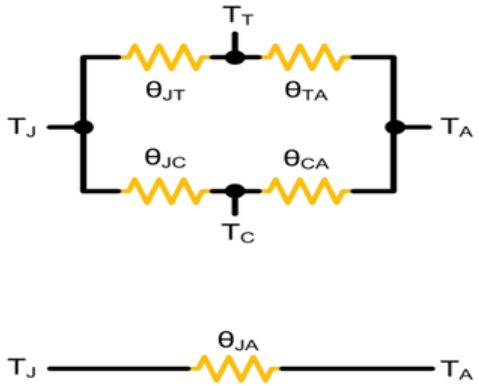
Maximum ambient temperature.
Specified by customer application

Thermal resistance from ambient to junction of converter.
Depends on everything; package, copper area, airflow, etc.

The goal is to keep T_J below the maximum specified in the data sheet.

Some basic terminology

- Thermal resistance; θ_{JA}
  - Total thermal resistance from the junction to the ambient environment.
    - Not too easy to estimate, in some cases.
    - Depends on many factors:
      - Package type
      - Copper heatsink area
      - Air flow
      - Number of copper planes
      - Weight of copper planes
      - Number of thermal vias
      - Adjacent components
      - Power dissipation



Some basic terminology

Difference between θ-type and Ψ-type parameters

θ-Type

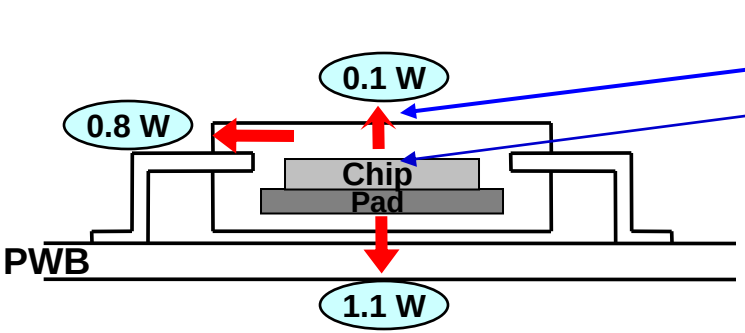
- All the heat flows from the junction to location X
  - Assumes isothermal conditions
- Location X serves as the external heat sink to the package
  - Assumes non-isothermal conditions

Ψ-Type

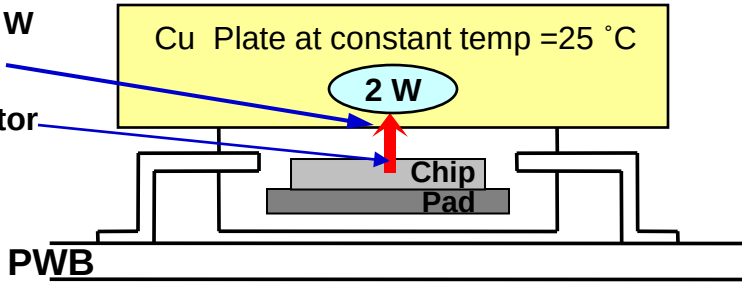
- Only a fraction of the heat flows from the junction to location X
  - Assumes non-isothermal conditions
- Temperature gradient exists in location X
  - Assumes non-isothermal conditions

THERMAL METRIC (1) (2)		DDA (HSOIC) 8 PINS	RNX (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9	72.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	23.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.8	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	N/A	°C/W

Difference between Ψ_{JT} vs θ_{JC}



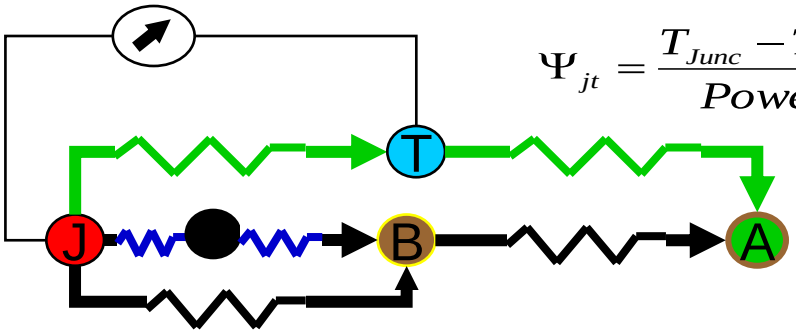
Power dissipation = 2 W
Case temp monitor
Junction temp monitor



Ψ_{JT}

Power is dissipated in all directions

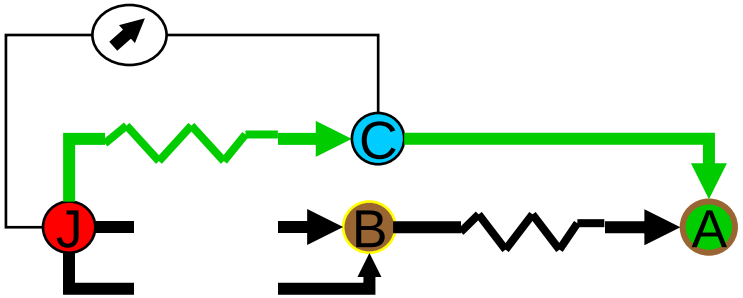
$$\Psi_{jt} = \frac{T_{Junc} - T_{case}}{Power}$$



$$\theta_{JC} = \frac{T_{Junc} - T_{Case}}{Power}$$

θ_{JC}

All the power is forced to be dissipated only in one direction {UPWARD}



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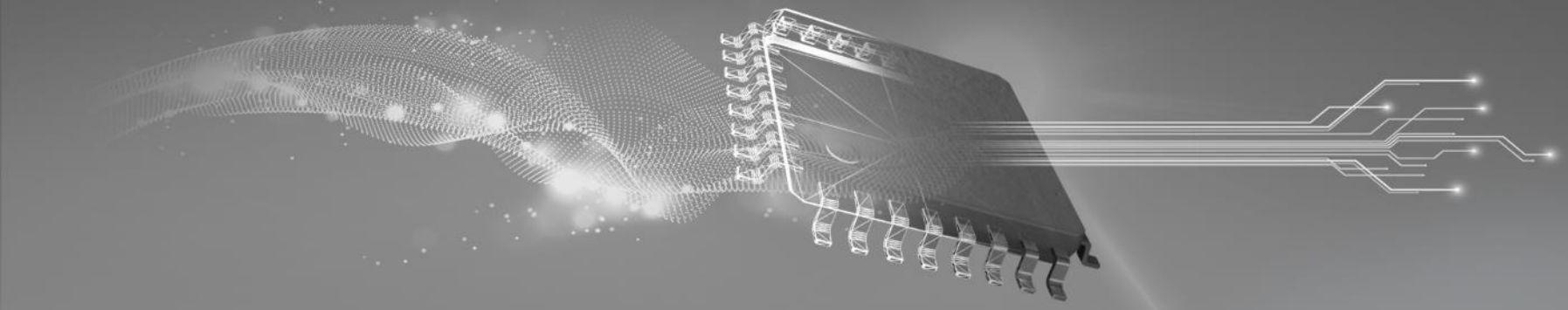
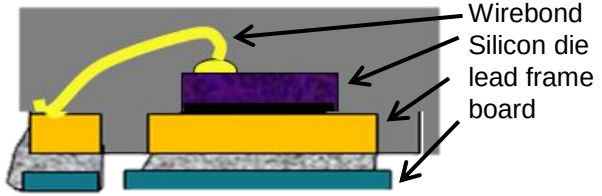


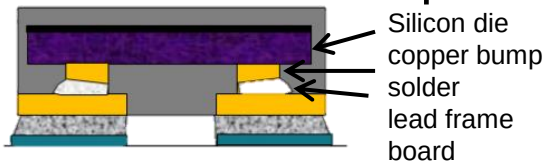
Package comparison

HotRod™ QFN vs wirebond QFN package

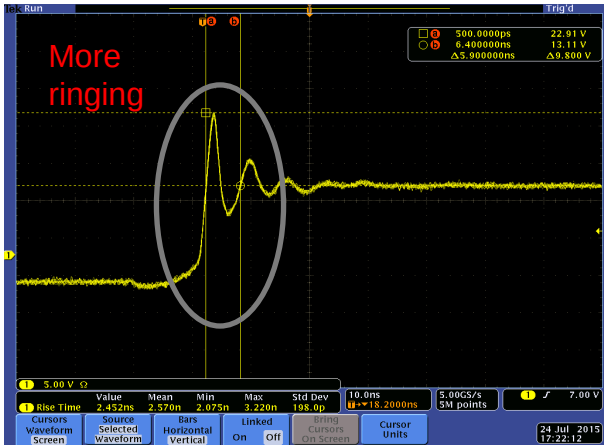
Standard wirebond QFN

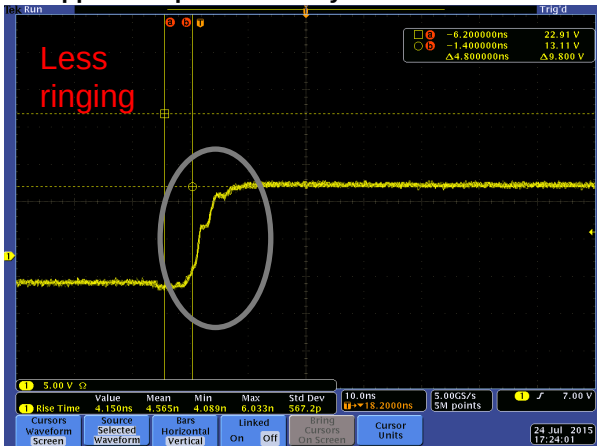


HotRod™ QFN package



Die is flipped and placed directly onto the lead frame





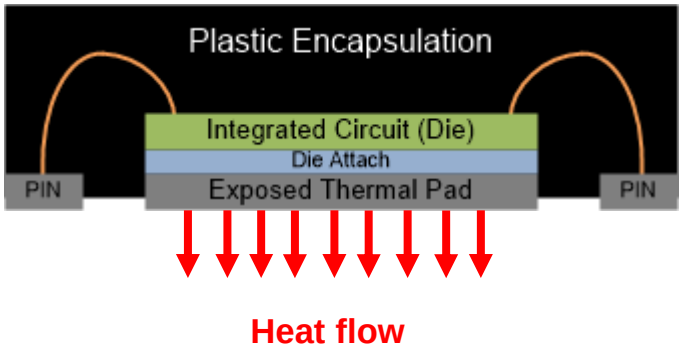
Minimize EMI through:

1. **No-wirebond VSON packaging**
2. Symmetric pinout

Package differences

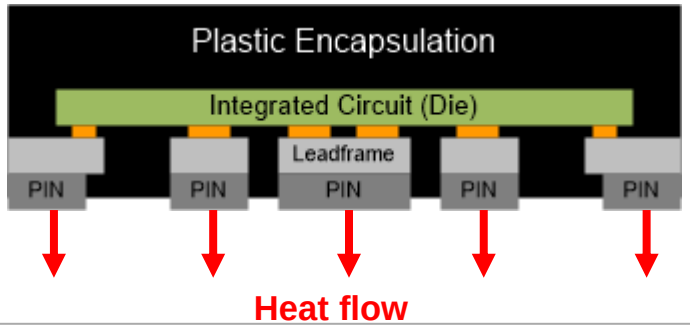
Standard wirebond QFN package

- Bondwires connect IC to pins
- Good thermal performance
- Higher parasitic resistance and inductance
- Larger than QFN



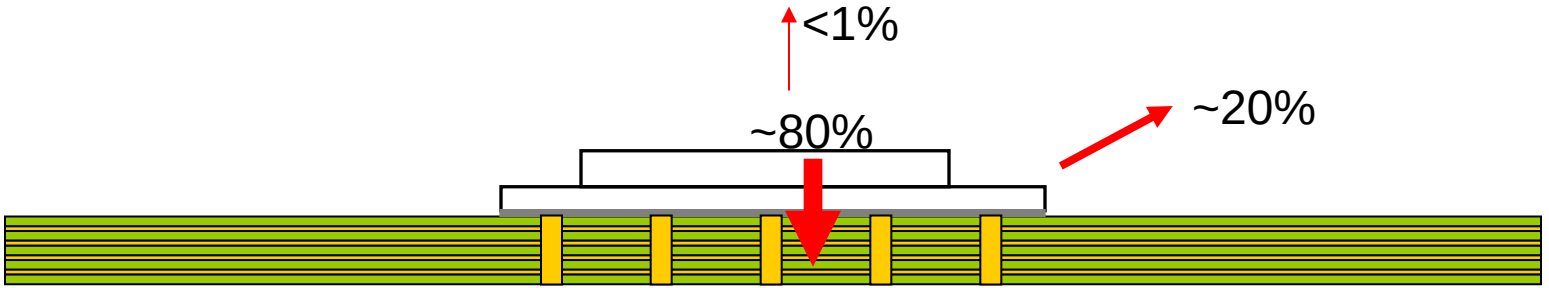
HotRod™ QFN package

- Copper pillars (bumps/posts) on IC soldered directly to the lead-frame
- Poor thermals compared to DAP
- Reduced parasitic resistance and inductance
- Smaller than SOIC



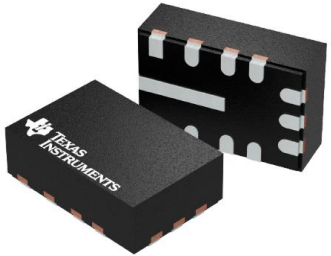
Thermal path for exposed pad packages

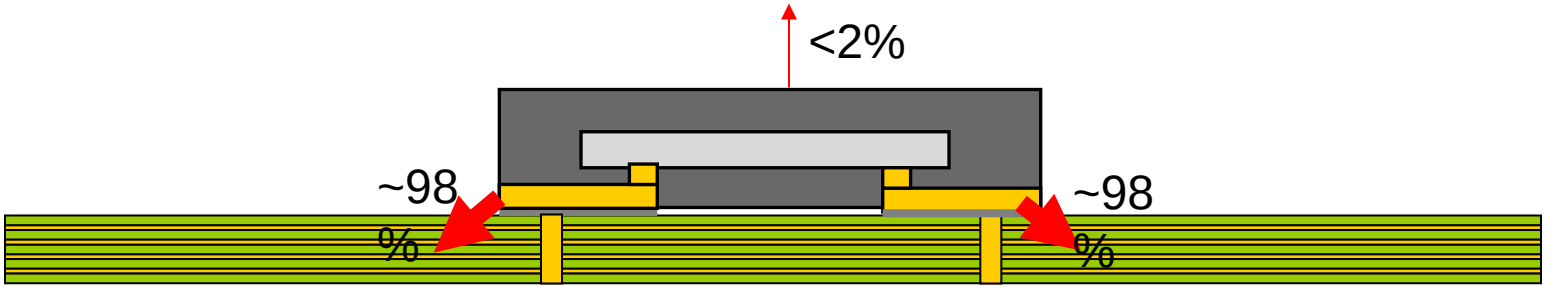
- PowerPad™ QFP/TSSOP, QFN
  - Typical power: 0.5-10 W
  - Thermal design for these packages:
    - Soldered to PCB thermal/GND plane
    - PCB has thermal pad and vias tied to ground plane
    - Most of the heat uses the exposed pad, because that is the lowest thermal impedance path



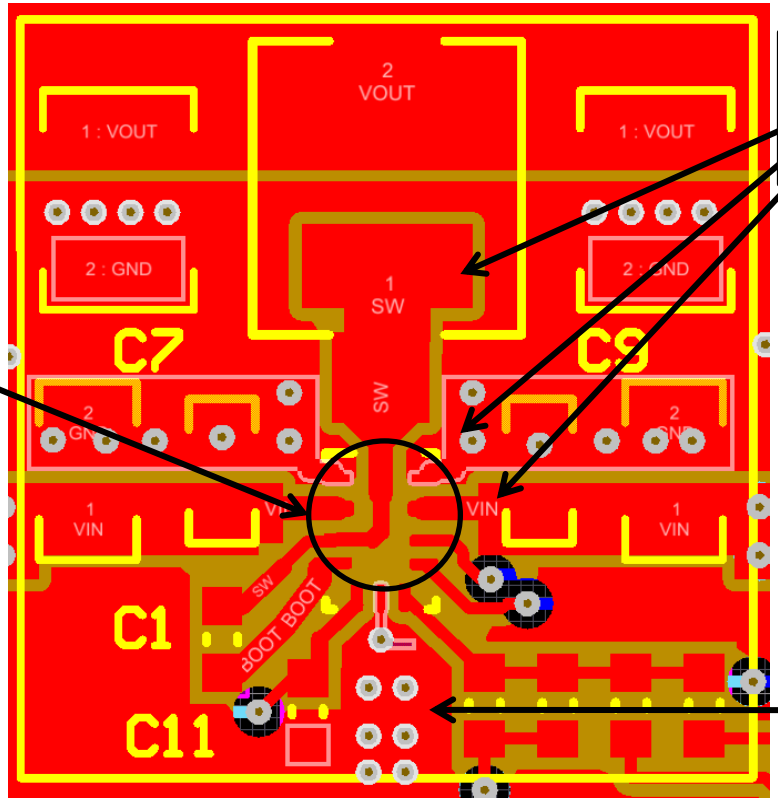
Thermal path for HotRod™ QFN package

- Flipped die on leadframe (HotRod™ QFN package)
  - Typical power: 0.5-3 W
  - Thermal design for these packages:
    - Large pads connected to power devices are essential to distribute heat
      - Most of heat is through large pads because of metal routing but pir heat
        - » PGND, GND, SW: most effective





Layout guidelines for HotRod™ QFN package



Fat and wide traces on V_{IN}, GND, SW

SW routed under the IC, no space for PGND trace and vias

Note: Tradeoff on SW Pin for EMI and thermal

Lots of GND vias

Data sheet thermal characteristics

- Values of θ_{JA} given in the table are NOT as beneficial for thermal design
  - They are useful for comparing packages within TI or with our competitors

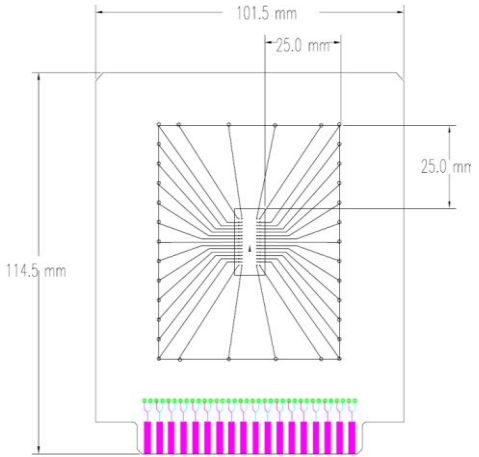
- The other values can be useful
  - θ_{JC} , Ψ_{JB} and Ψ_{JT} are the most useful

SOIC **HotRod™**

THERMAL METRIC (1) (2)		DDA (HSOIC) 8 PINS	RNX (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9	72.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	23.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	4.3	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	13.8	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	N/A	°C/W

Data sheet thermal characteristics

- The values given in the table are simulations
  - The traces on the JEDEC board are too small to provide adequate heat-sinking
    - For HotRod™ the heat is mostly dissipated from the pads
      - This makes the JEDEC board a bad estimate for thermals
- JEDEC uses the same standard for all packages
  - This makes the numbers good for comparing packages
- Need better methods for estimating θ_{JA}



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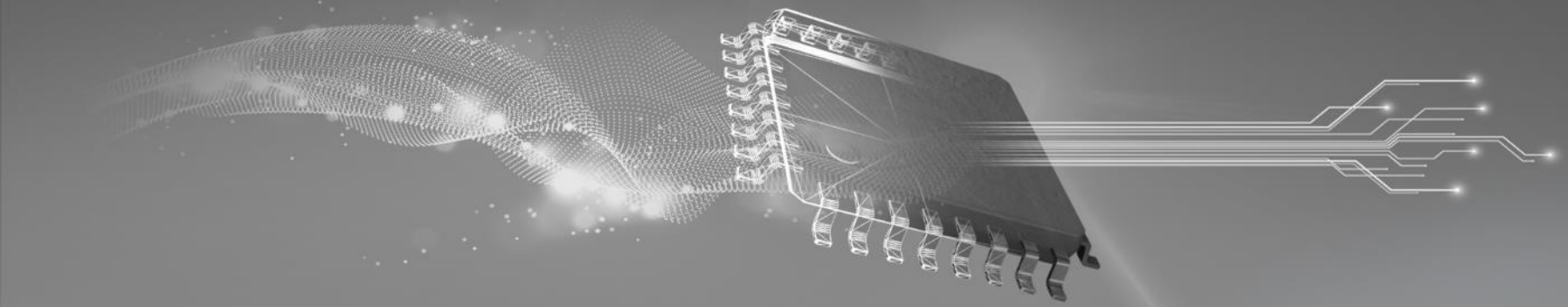


Design calculations for PCB thermal performance

Design strategy summary

- Calculate PD based on the efficiency and system inputs: T_A, V_{IN}, V_{OUT}, and I_{OUT}
  - Refer to typical power dissipation curve in datasheet for PD (if provided)
  - Example with LMR33630 and LM60440
- Calculate required θ_{JA}
- Determine required board size:
  - Datasheet guidelines
  - Online calculator
  - WEBENCH® Power Designer
- Follow layout guidelines for vias, and routing, etc.

Thermal design for LMR33630 (Step 1)

Example: **LMR33630 RNX (Hot Rod)** V_{IN} = 12 V, V_{OUT}, = 5 V, I_{OUT} = 3 A, 2.1 MHz

1a. We find an efficiency from the data sheet:

Approximate efficiency of **91%**

based on graph shown

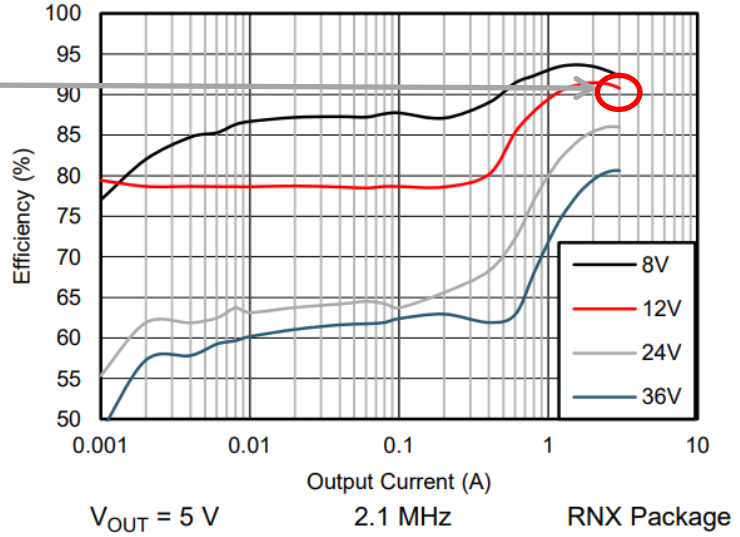


Figure 36. Efficiency

1b. P_{LOSS} = **1.48 W**

1c. P_D = **1.16 W** (R_L~35 mΩ from EVM user guide)

Thermal design for LMR33630 (Step 2)

- For this step we need the maximum ambient temperature from the application requirement and the maximum junction temperature from the data sheet.
- T_A = 85°C
- T_{Jmax} = 150°C

$$\theta_{JA} \leq \frac{T_{Jmax} - T_A}{P_D}$$

- We get $\theta_{JA} \leq 56°C/W$

- A quick start calculator is also available to help with “what-if” calculations:

Thermal design for LMR33630 (Step 3)

- This option is more accurate since it based on measured data.
- The curves for LMR33630 are shown.
- This curve indicates that a 4 layer board with an area of 4.0 cm x 5.0 cm (20 cm^2) will give $\theta_{JA} < 56°C/W$.

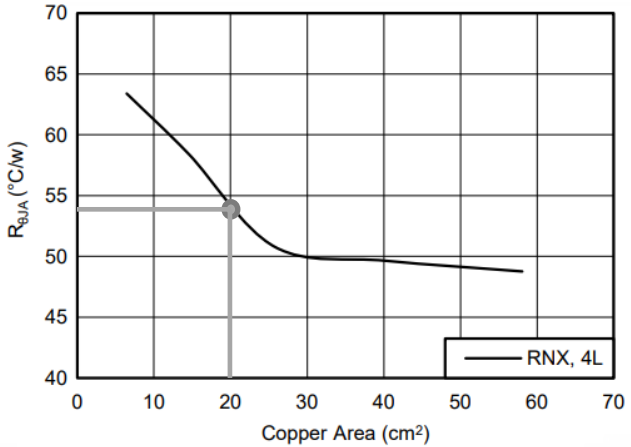
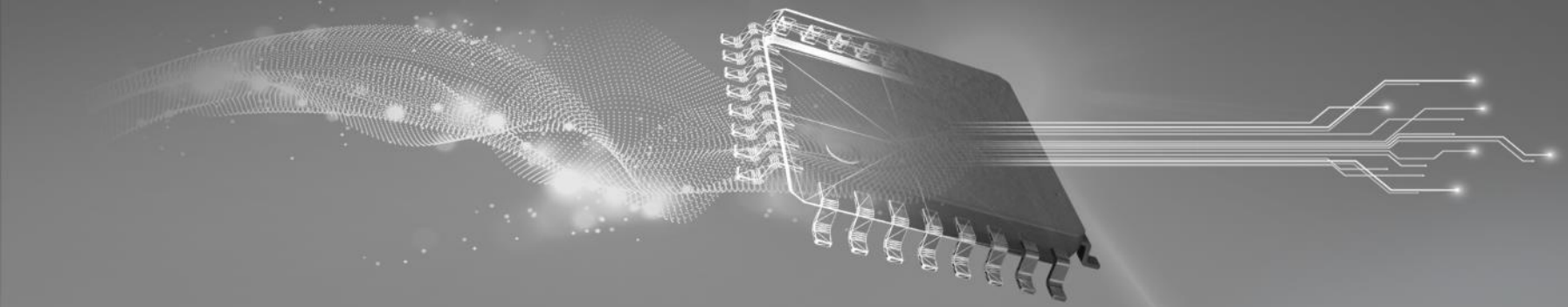


Figure 23. $R_{\theta JA}$ vs Copper Board Area for the VQFN (RNX) Package

TI TECH DAYS



Design examples and data

LMR33630 case study

Scenario:

I have a design with the following specifications:

V_{IN} = 6 V to 18 V with a typical value of 12 V

V_{OUT} = 3.3 V

I_{OUT} = 3 A

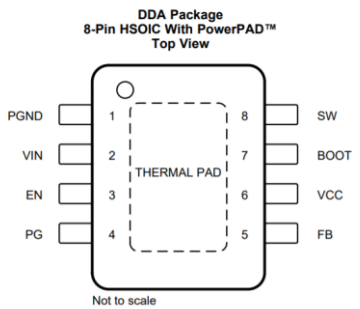
Operating Frequency = 2.1 MHz

How does the HotRod™ QFN package compare to the SOIC?

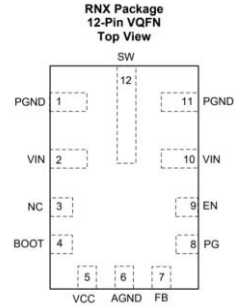
LMR33630 package comparison

Can the HotRod™ QFN package handle my thermal requirement?

Should I stick with SOIC with DAP Package?



OR



THERMAL METRIC(1) (2)		LMR336x0 DDA (HSOIC) 8 PINS	LMR336x0 RNX (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.9(2)	72.5(2)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54	35.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.6	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.3	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13.8	23.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.3	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For design information see *Maximum Ambient Temperature* section.

LMR33630 efficiency comparison

SOIC

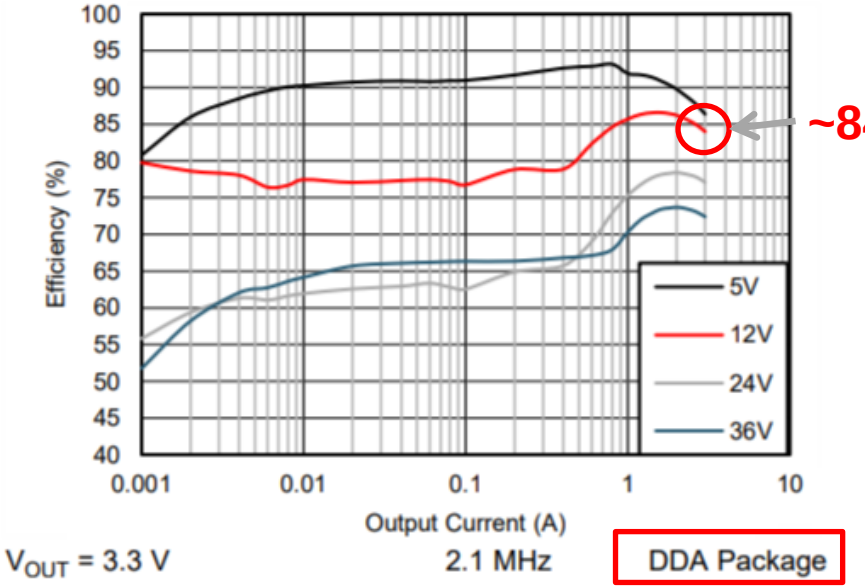


Figure 31. Efficiency

At 12 V input and 3 A (Efficiency ~ 84%)

HOTROD

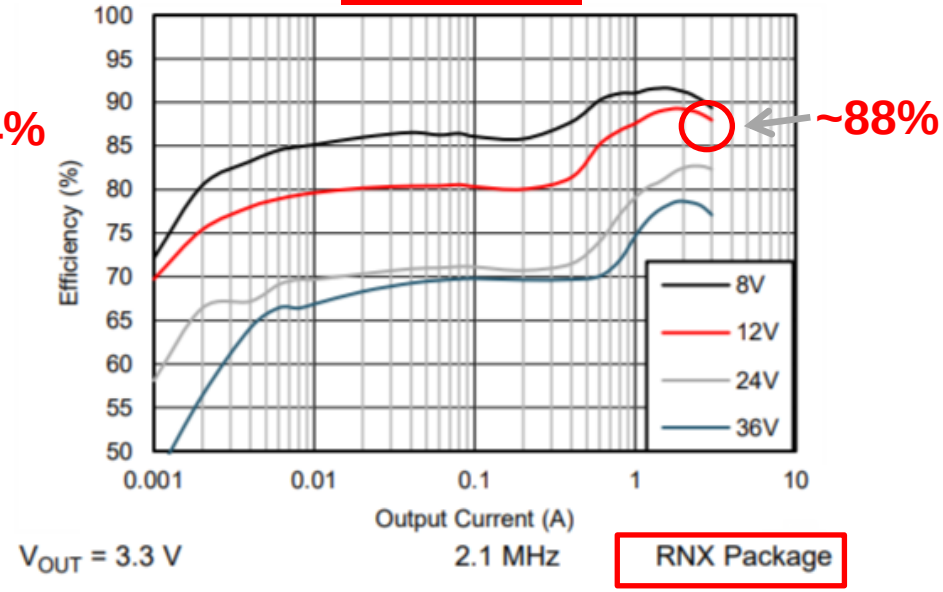


Figure 37. Efficiency

At 12 V input and 3 A (Efficiency ~ 88%)

LMR33630 power dissipation

PARAMETER	SOIC	HOT ROD
Efficiency	84%	88%
Total Power Loss (P_{LOSS})	1.88 W	1.35W
Inductor DCR (R_L) (from EVM)	25 mΩ	35mΩ
Power Dissipated DCR	0.225 W	0.315 W
Power Dissipated IC (P_D)	**1.655 W**	**1.035 W**

$$P_{LOSS} = V_{OUT} \cdot I_{OUT} \cdot \left(\frac{1-\eta}{\eta} \right)$$

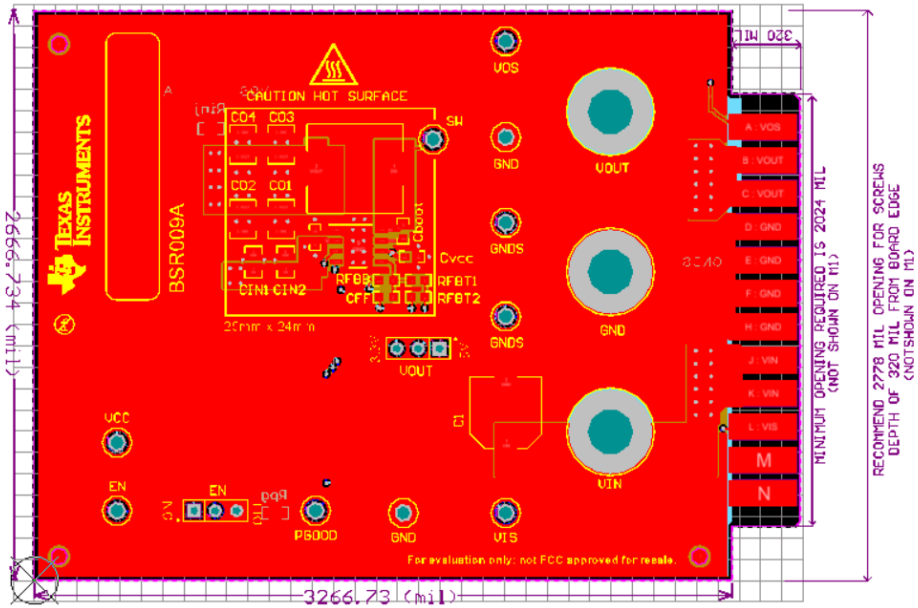
$$P_D = P_{LOSS} - I_{OUT}^2 \cdot R_L$$

$$\theta_{JA} \leq \frac{T_{Jmax} - T_A}{P_D}$$

The HotRod™ QFN device dissipate less power compared to the SOIC device

LMR33630EVM board size comparison

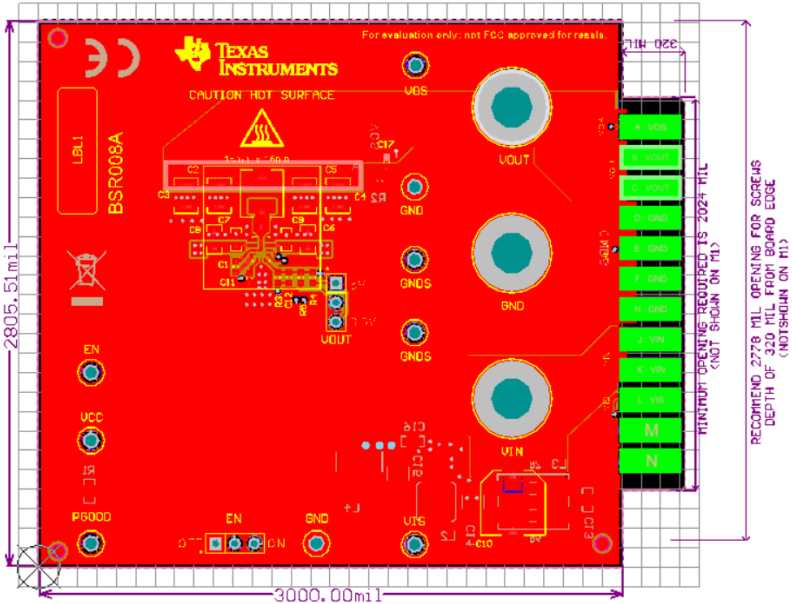
SOIC



Board area = 3.2 in x 2.6 in

= 8.32 in^2 = **53.6** cm^2

HOTROD



Board area = 3.0 in x 2.8 in

= 8.4 in^2 = **54.2** cm^2

LMR33630 θ_{JA} comparison

SOIC

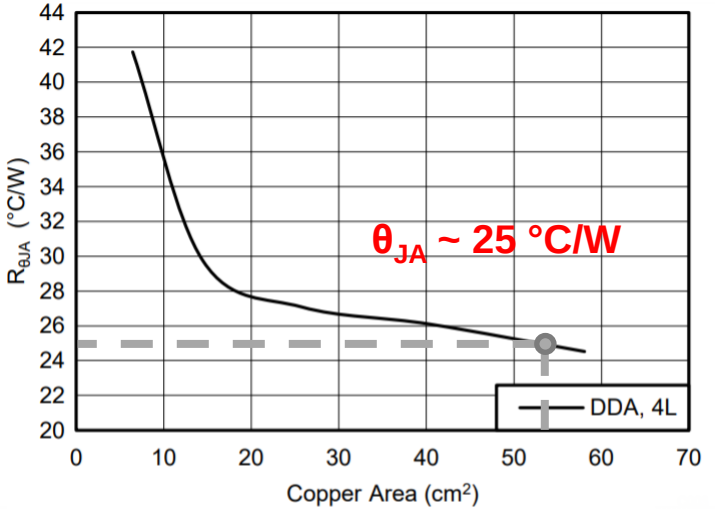


Figure 22. Typical $R_{\theta JA}$ vs Copper Area for a Four-Layer Board and the HSOIC (DDA) Package

Board area = **53.6** cm²

HOTROD

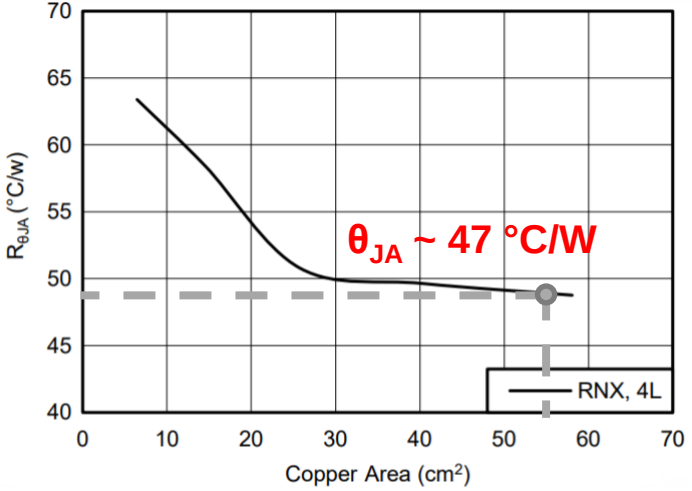


Figure 23. $R_{\theta JA}$ vs Copper Board Area for the VQFN (RNX) Package

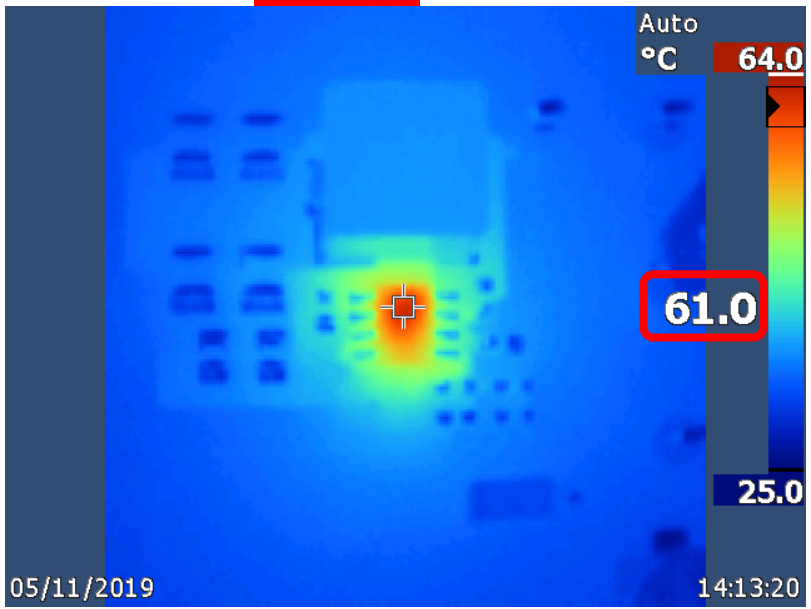
Board area = **54.2** cm²

LMR33630 expected temperature

PARAMETER	SOIC	HOTROD
Power Dissipated IC (P_D)	**1.655 W**	**1.03 W**
Junction to Ambient Thermal Resistance ($R_{\theta JA}$)	**~ 25 °C/W**	**~ 47 °C/W**
Temperature Rise	**1.655 W x 25°C/W = 41.3°C**	**1.03 W x 47°C/W = 48.4°C**
At 25°C Ambient (Tj)	~ 66°C	~ 73°C

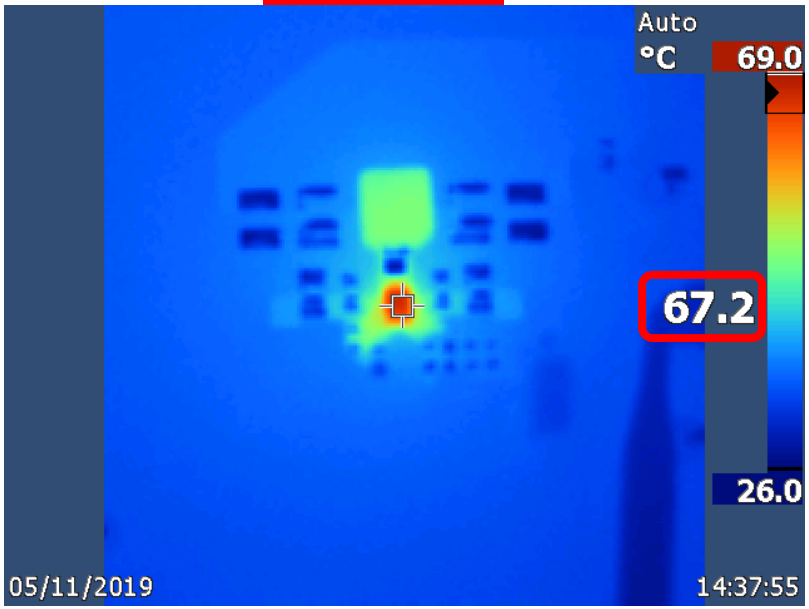
LMR33630EVM measurements

SOIC



Measured Case Temperature = 61°C
With Ψ_{JT} = 4.3°C/W
Junction Temperature ~ 68°C

HOTROD



Measured Case Temperature = 67°C
With Ψ_{JT} = 0.8°C/W
Junction Temperature ~ 68°C

Example summary

1) $R_{\theta JA}$ value given in the datasheet thermal table should not be used to measure thermal performance of the IC.

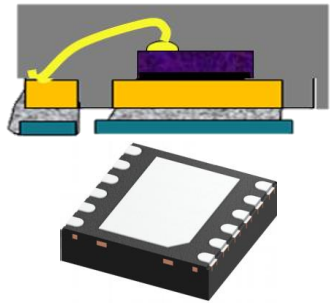
2) The value is only useful to compare packages within TI and our competitors.

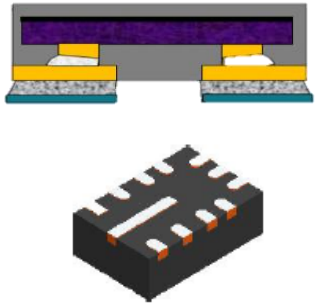
3) $R_{\theta JA}$ curves within the datasheet can be used to estimate the temperature of the IC for a given copper size area.

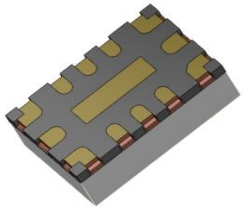
4) Some datasheet will also show derating curves for a specific $R_{\theta JA}$ value.

5) Ψ_{JT} number can be used to accurately estimate the IC junction temperature.

Enhanced HotRod™QFN and its benefits







Standard wirebond QFN package

- Ground DAP: optimized thermal performance
- Unleaded package: reduced package size
- Improved Power Density

- Un-optimized EMI performance because of the presence of wirebonds

HotRod (FCOL) package

- No wirebonds – Better EMI performance
- No wirebonds – Package size further reduced

- Wettable flanks – Optimized for manufacturing
  - Improvement BLR numbers

- Un-optimized thermal performance due to absence of ground DAP

Enhanced HotRod QFN package

Thermal design for LM60440

Step 1: Calculate the power dissipation

a. Total Power Loss:

$$P_{LOSS} = V_{OUT}.I_{OUT}.\frac{(1-\eta)}{\eta}$$

- η is the conversion efficiency

b. Subtract the loss in Inductor

$$P_D = P_{LOSS} - I_{OUT}^2.R_L$$

- R_L = Inductor DCR

c. LM60440 Calculations:

$$P_{LOSS} = 5.067x4.01 \times \frac{(1-0.904)}{0.904}$$

$$= 2.18W$$

$$P_D = 1.82W$$

Step 2: Calculate the required thermal resistance ($R_{\theta JA}$)

a. Maximum Ambient Temperature for Application (T_A)

b. Maximum Junction Temperature from Datasheet (T_{JMAX})

$$\theta_{JA} \leq \frac{T_{Jmax} - T_A}{P_D}$$

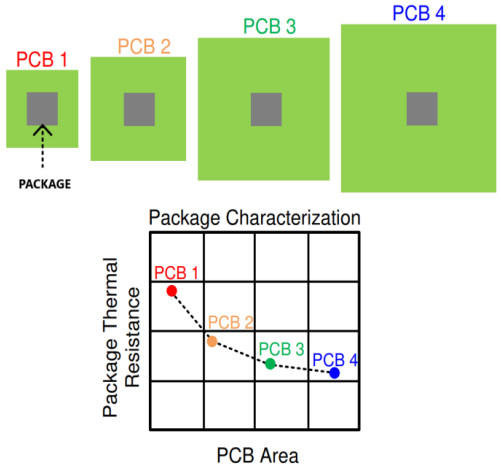
c. LM60440 Thermal Resistance:

$$\theta_{JA} < \frac{(150 - 85)}{1.82}$$

$$\boldsymbol{\theta}_{JA} < 35.71^oC/W$$

Step 3: Estimate the PCB copper area

- This curve indicates the required area of 4 layer board for a calculated $R_{\theta JA}$ from Step 2.

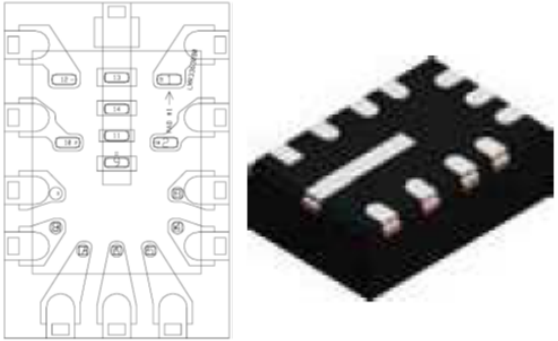


Thermal performance comparative analysis

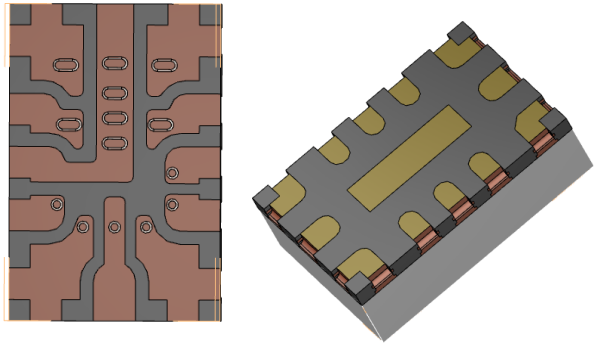
LM60440 in Enhanced HotRod™ QFN package and LMR33630 in HotRod™ QFN package were compared thermally:

- Nearly identical EVM designs used for comparison
  - EVMs were adjusted minimally to accommodate footprint differences

LM33630 HotRod™ QFN



LM60440 Enhanced HotRod ™ QFN



Application EVMs

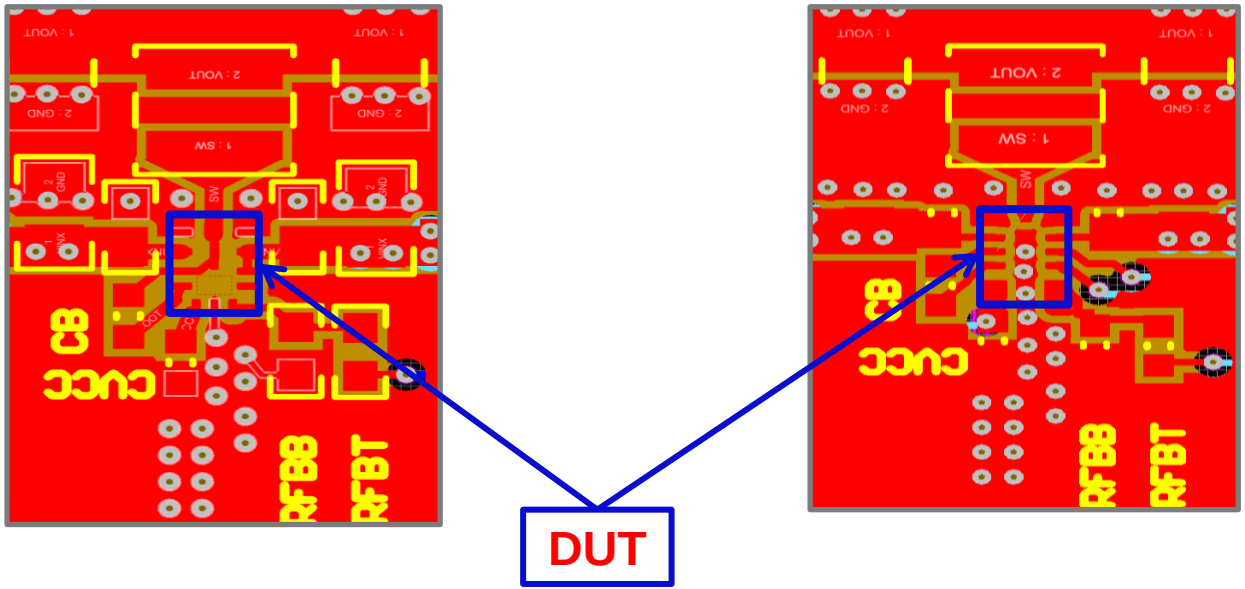
PGND thermal via pattern consistent between EVM layouts

LMR33630

No DAP under device

LM60440

3 vias from DAP to GND



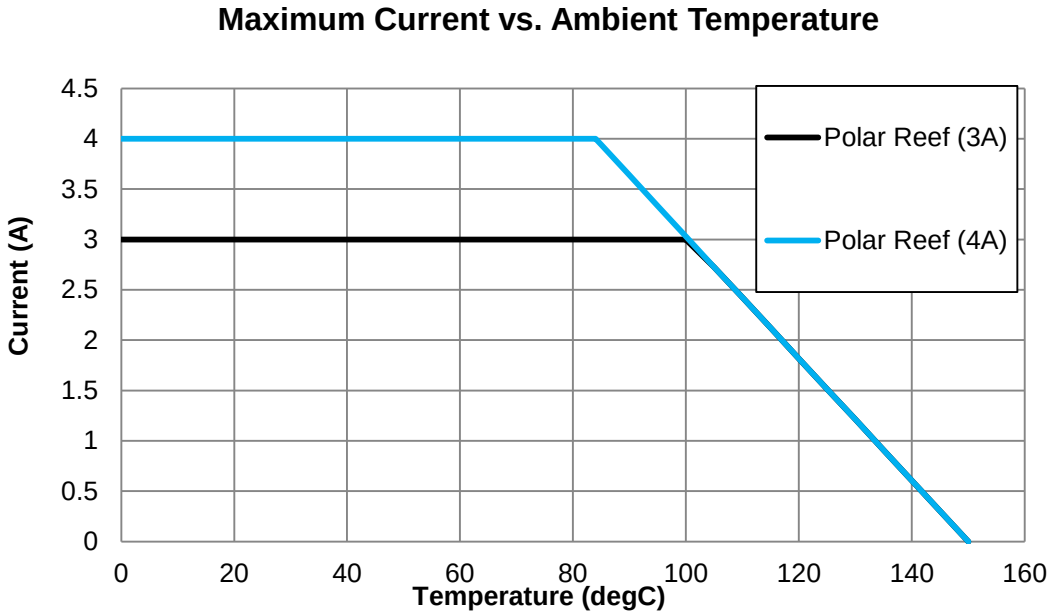
Summary table: V_{IN}= 12 V, I_{OUT}= 4 A; T_a= 25ºC

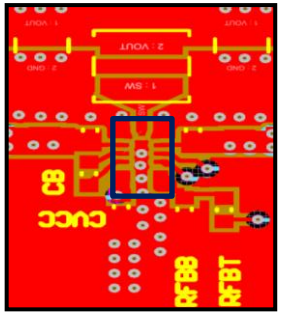
	V_{IN} (V)	I_{IN} (A)	V_{OUT} (V)	I_{OUT} (A)	Efficiency (%)	Total Power Dissipation (W)	IC Power Dissipation (W)	IC Temperature (°C)	Temp Rise (°C)	Theta Ja (°C/W)
LM60440 (Board 1)	12.042	1.866	5.067	4.01	90.42	2.186	1.82	**86.98**	61.98	**34.18**
LM60440 (Board 2)	12.005	1.8727	5.058	4.0126	90.27642	2.173	1.807	**87.62**	62.62	**34.65**
LMR33630 (4A Trim)	12.022	1.8503	5.023	4.0123	90.602	2.0905	1.7245	**91.57**	66.57	**38.60**

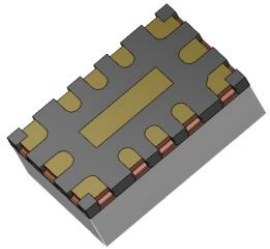
- Thermal performance of Enhanced HotRod™ QFN package technology is better in comparison to HotRod™ QFN package technology.

Note: The IC temperature is based on average measurement.

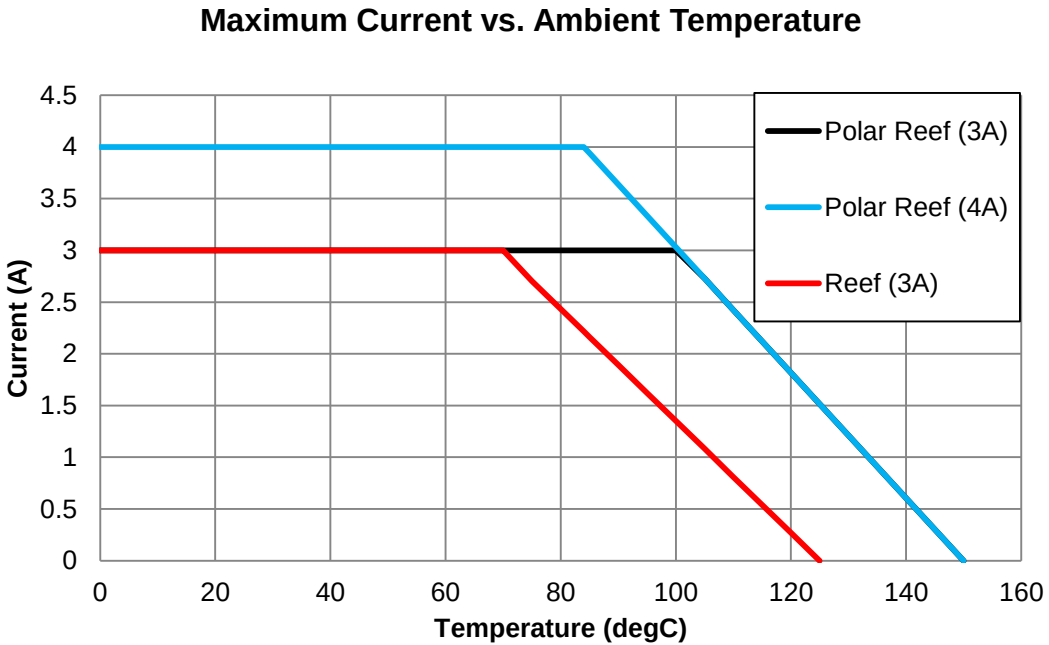
LM60440 (4 A) vs LM60430 (3 A)

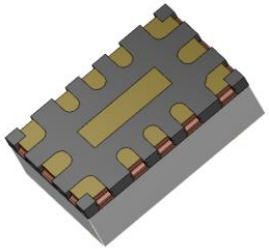


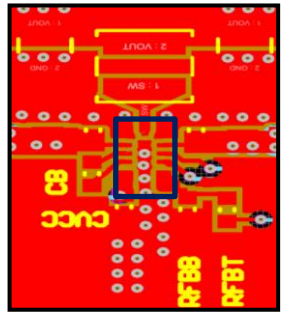


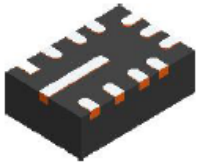


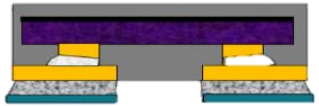
LM60430/LM60440 vs LMR33630







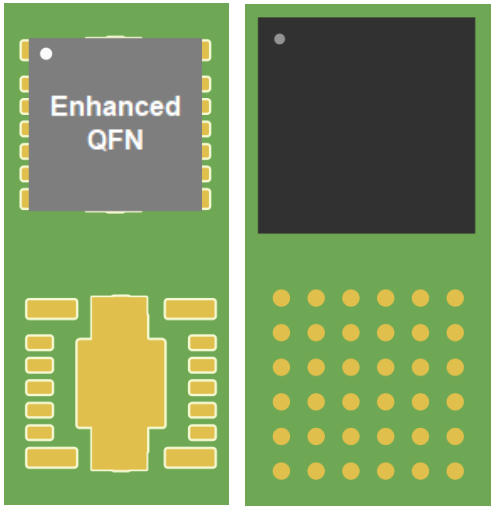




TI power module & competitor comparison

TPSM53604
3.8-36 V
4 A
5x5.5 mm
Enhanced QFN

Area = 27.5 mm²

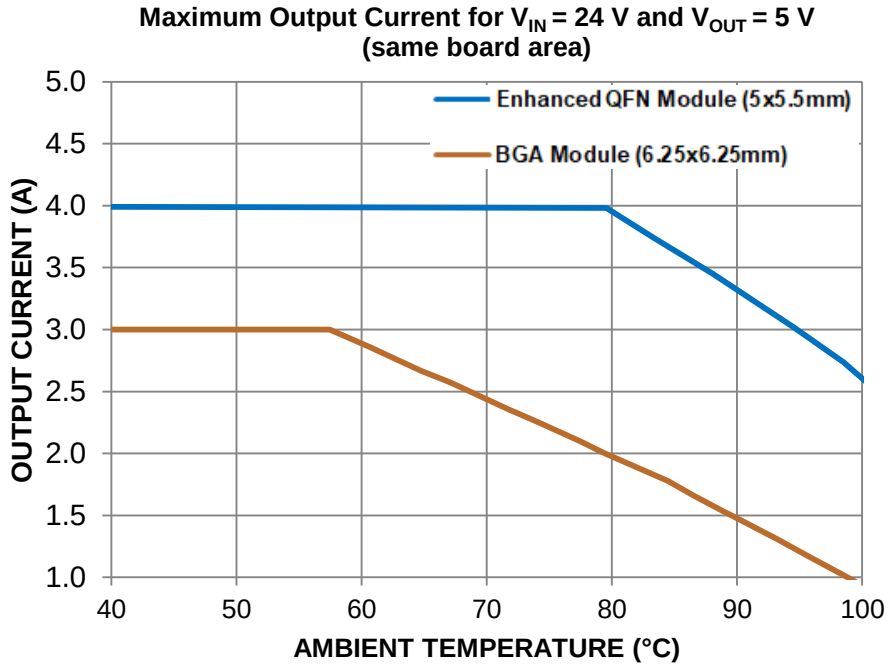


Thermal contact
42% of package area

Competitor
3.4-40 V
3.5 A “peak”
6.25x6.25 mm
BGA

Area = 39 mm²

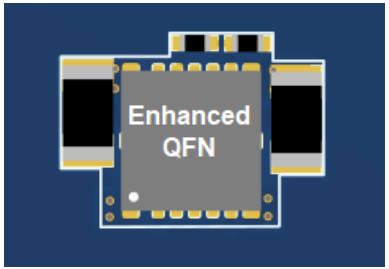
Thermal contact
18% of package area



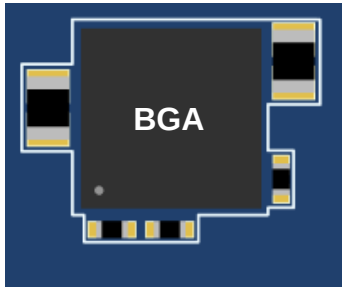
TI versus competitor efficiency

Solution size

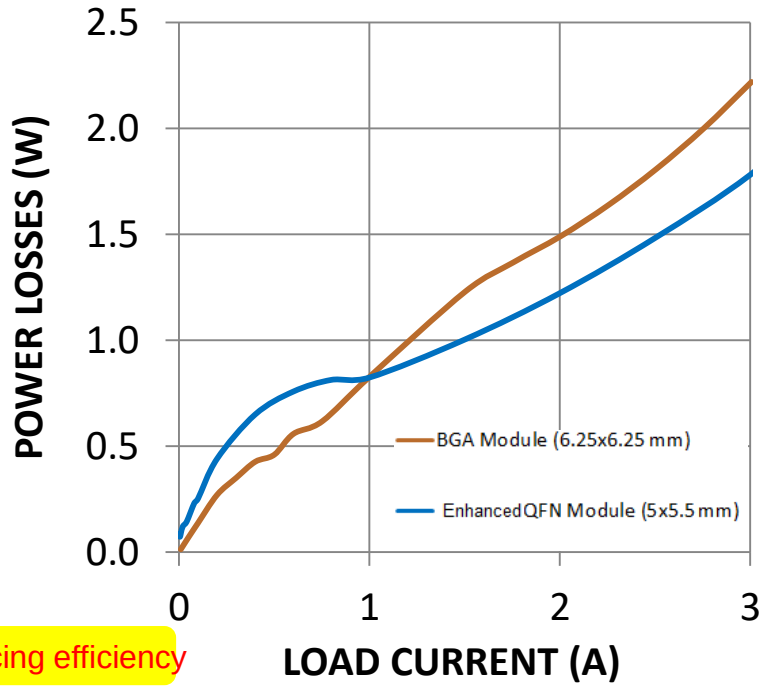
TPSM53604
3.8-36 V
4 A
Enhanced QFN



Competitor
3.4-40 V
3.5 A “peak”
BGA



Power dissipation
V_{IN} = 24 V V_{OUT} = 5.0 V

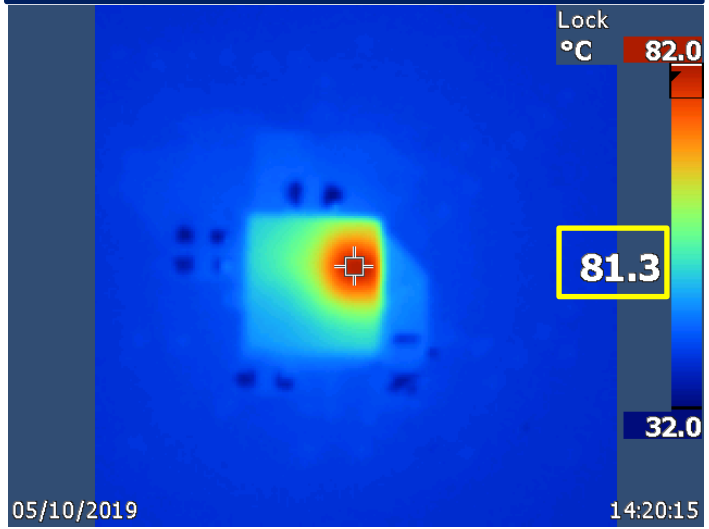


TI power module solution provides higher power density without sacrificing efficiency

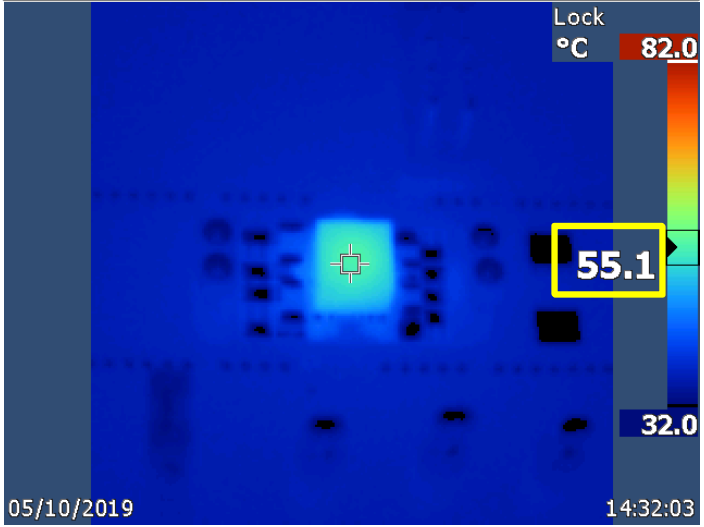
Thermal data analysis

Test Conditions:
Vin = 24 V ; Vout = 5 V , Iout = 2.5 A

Competitor Part

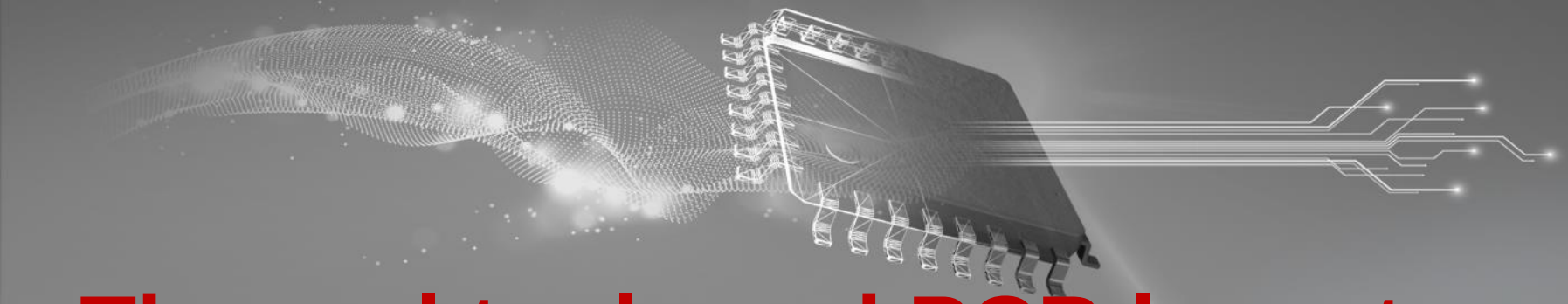


TPSM53603



TI product runs **significantly cooler** than competitor

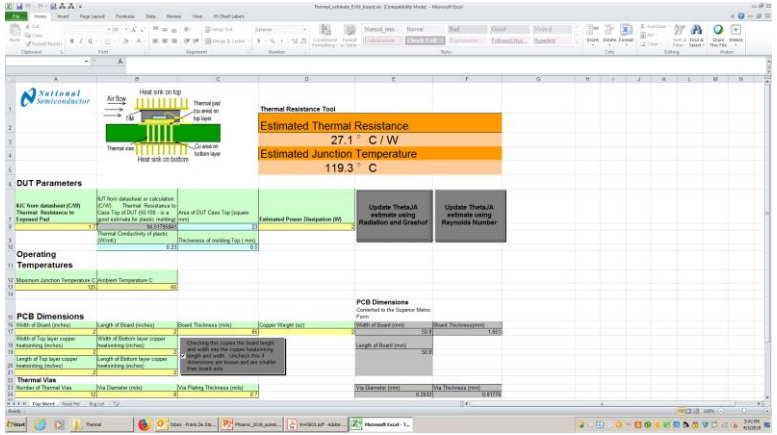
TI TECH DAYS



Thermal tools and PCB layout considerations

Tool (thermal estimator excel)

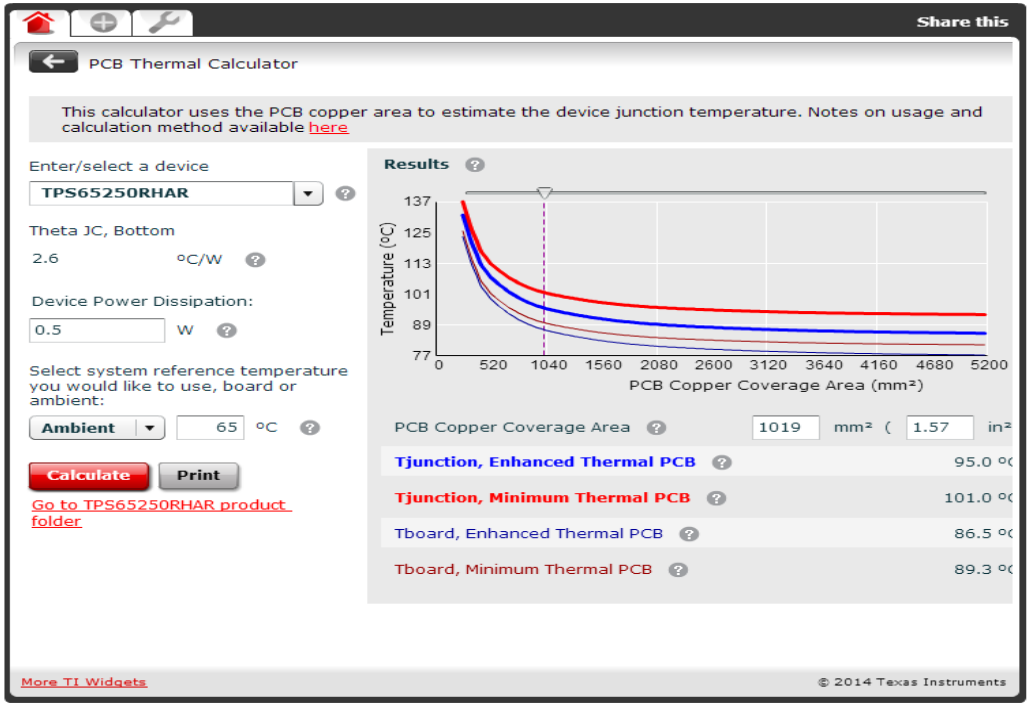
- **Application Note SNVA419C** and the associated spread-sheet can be used to estimate the required board size for a given set of conditions
  - Allows you to play “what-if” scenarios
  - Works well for packages with a DAP
    - Need to “adjust” values of θ_{JC} for other package types



Thermal_Estimate_Calculator

App Note: https://www.ti.com/lit/an/snva419c/snva419c.pdf

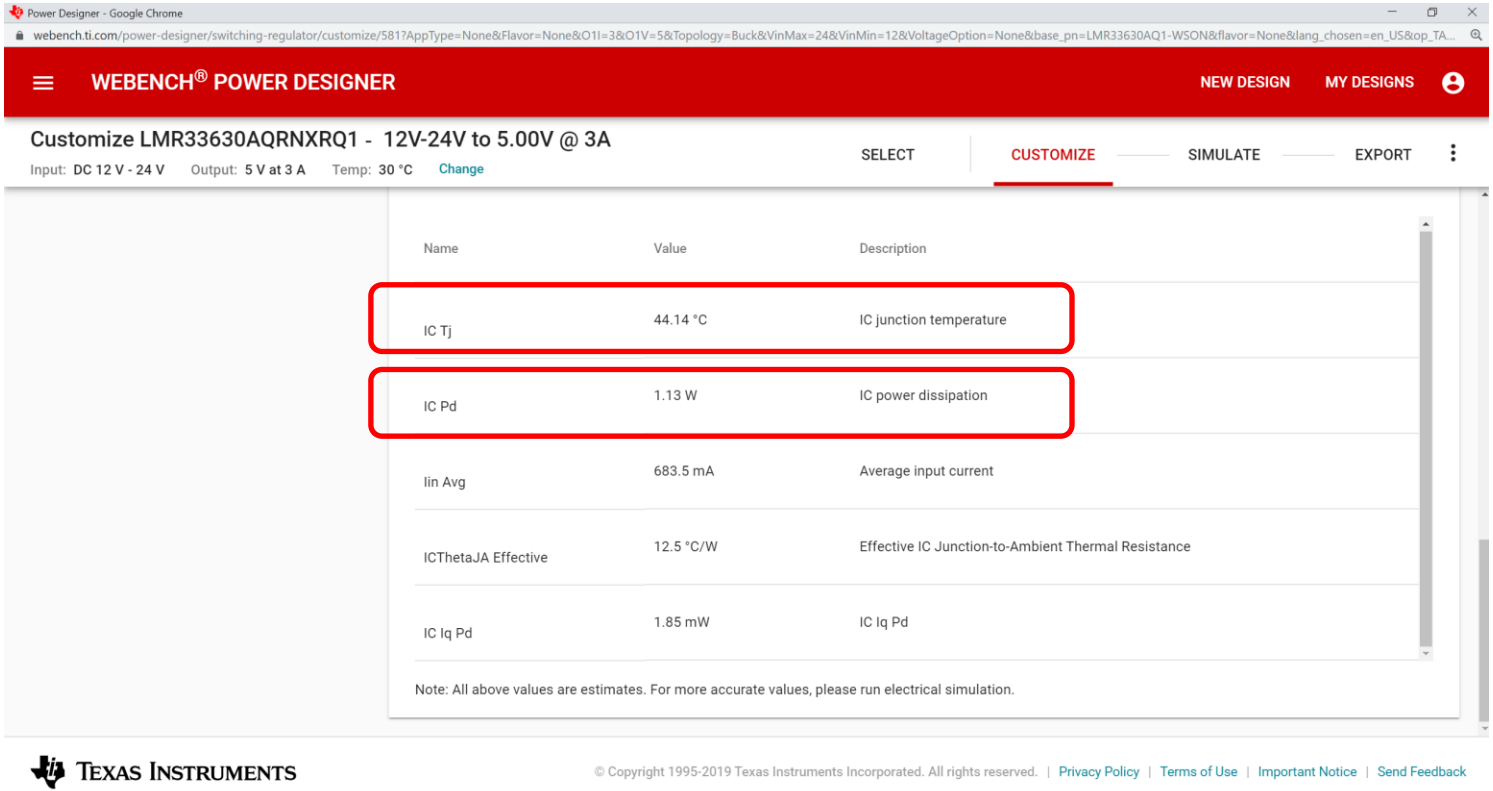
Tool (online PCB calculator)



Only available for some IC packages

http://www.ti.com/adc/docs/midlevel.tsp?contentId=76735

Tool (WEBENCH® Power Designer) cont.



Data sheet de-rate curves

- Many data sheets will have a “de-rating” curve
  - This shows the maximum load current for a given ambient temperature
  - Taken with one particular θJA
  - Uses the efficiency taken at an elevated temperature
    - 85°C or 125°C

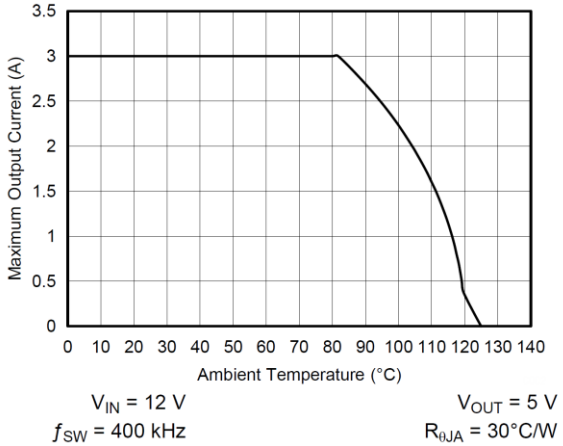


Figure 24. Maximum Output Current vs Ambient Temperature

Effects of copper area (TPS54824)

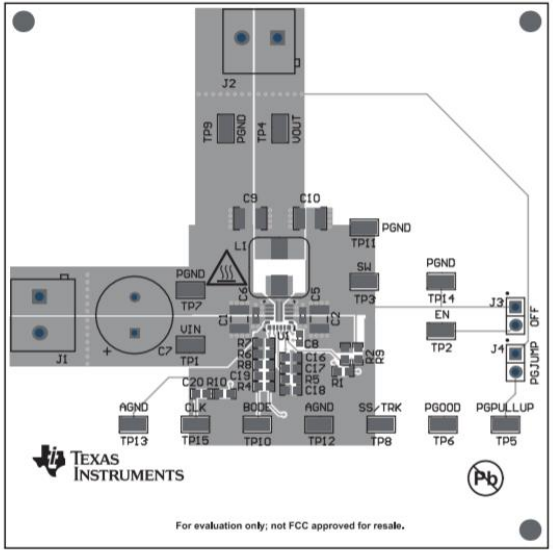


Figure 19. 1 in × 1 in Copper Area Top Layer

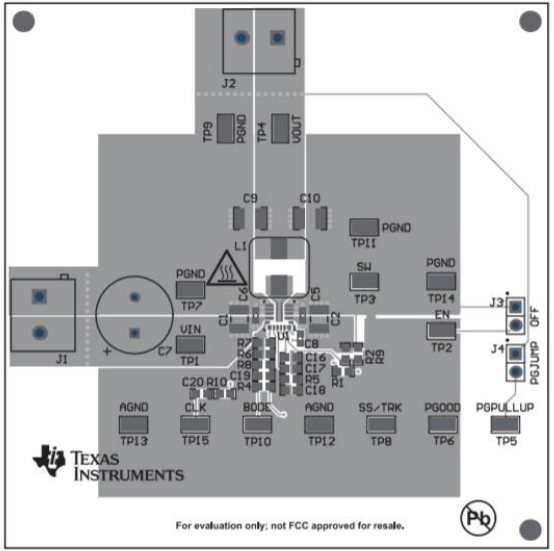
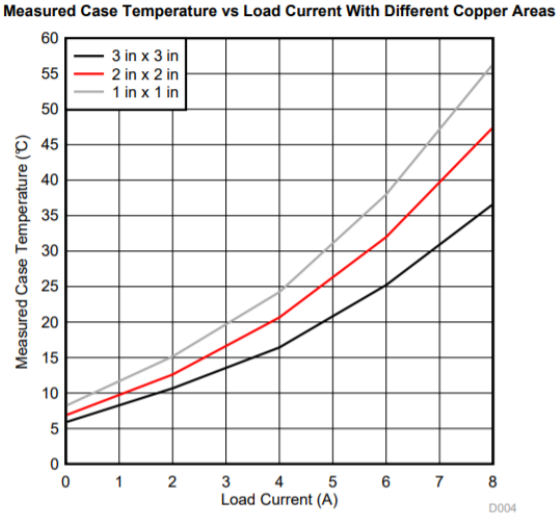


Figure 20. 2 in × 2 in Copper Area Top Layer



V_{IN} = 12 V
T_A = 23°C

V_{OUT} = 1.8 V
10-minute soak time

Comparing the 2 different copper area, at higher current of 8A, the improvement of case temperature ~ **10°C**

App Note: http://www.ti.com/lit/an/snva839/snva839.pdf

Layout guidelines – copper thickness

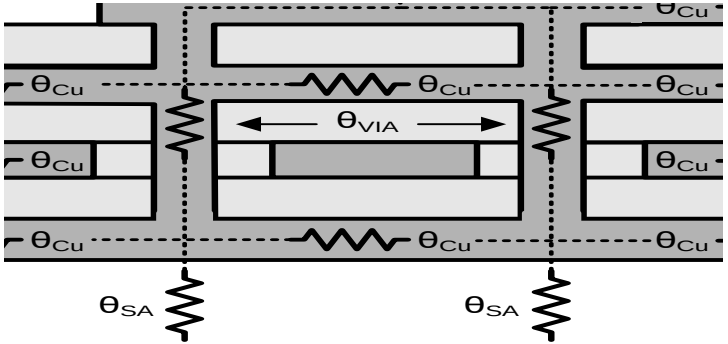
- Use appropriate copper thickness
- 1oz copper thickness is 35 µm and 2 oz copper thickness is 70 µm
- At least 1 oz copper is recommended for all DC-DC converter designs.
- 2 oz copper is recommended for designs that dissipate more than 3 Watts

$$\theta_{CU} = \frac{\frac{1}{\lambda_{CU}} \cdot \text{Length}}{\text{Width} \cdot \text{Thickness}}$$

Layout guidelines – vias

- Use lots of vias
  - Thermal resistances in parallel
  - The more you add, the lower the resistance is.
- Typical 0.3 mm (12 mil) thermal vias with 17.5 µm (0.5 oz) plating
- 1.56 mm (62 mil) PCB thickness

$$\theta_{vias} \cong \frac{251}{\text{no. of vias}}$$



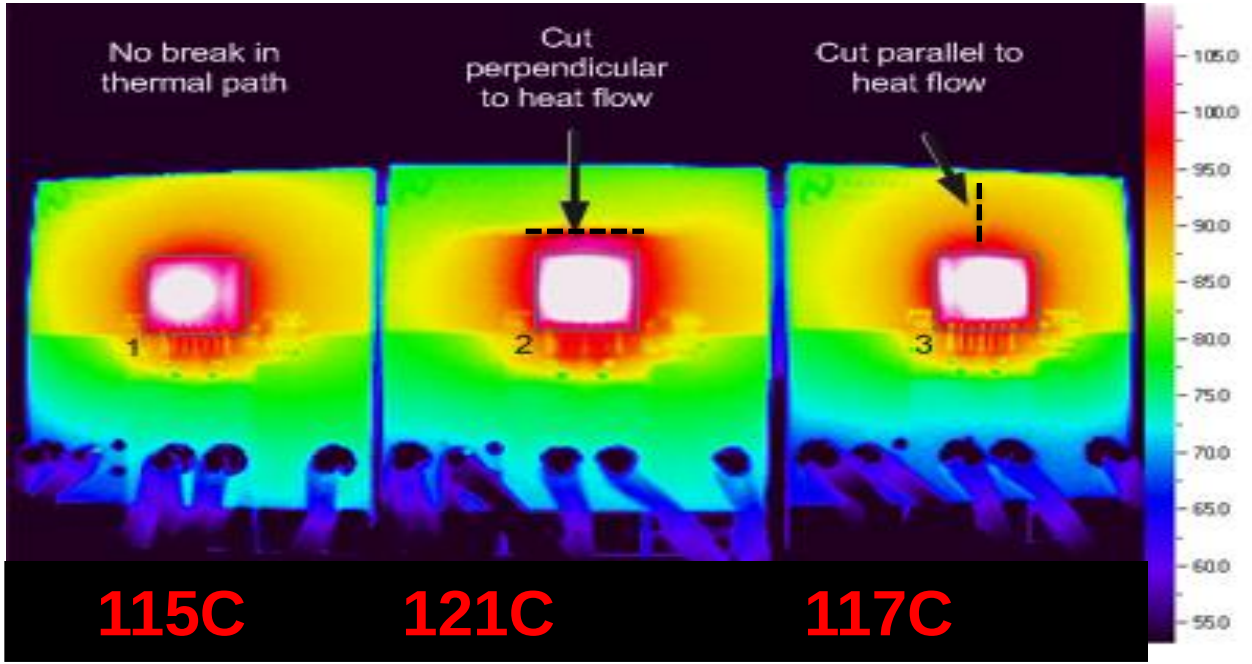
Via Array Thermal Resistance Calculations:

Microsoft Excel Worksheet

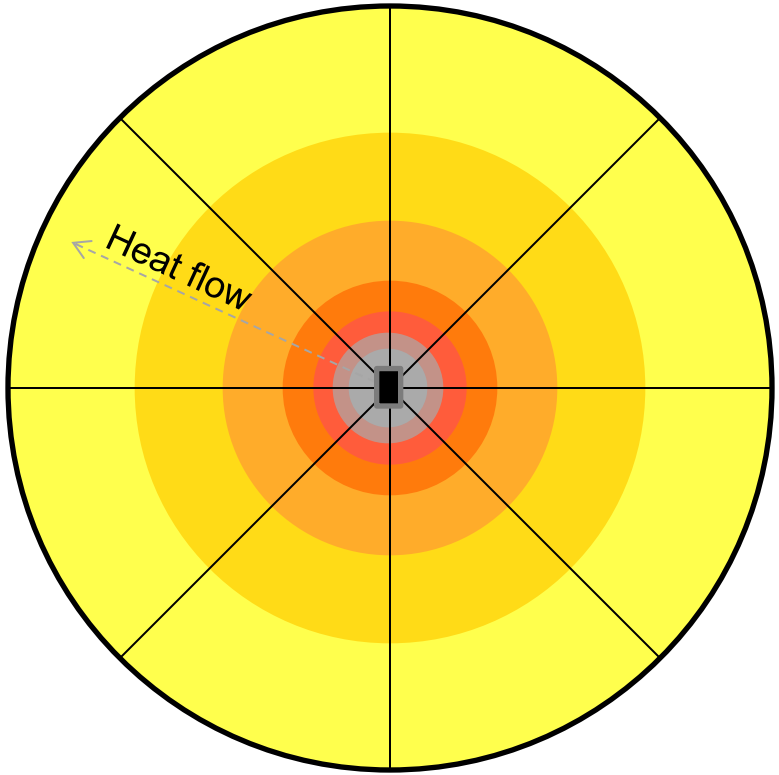
More thermal via guidelines in Application Notes SNVA419C and AN-1520

Layout guidelines – cuts in copper planes

– Cut copper plane parallel to heat flow



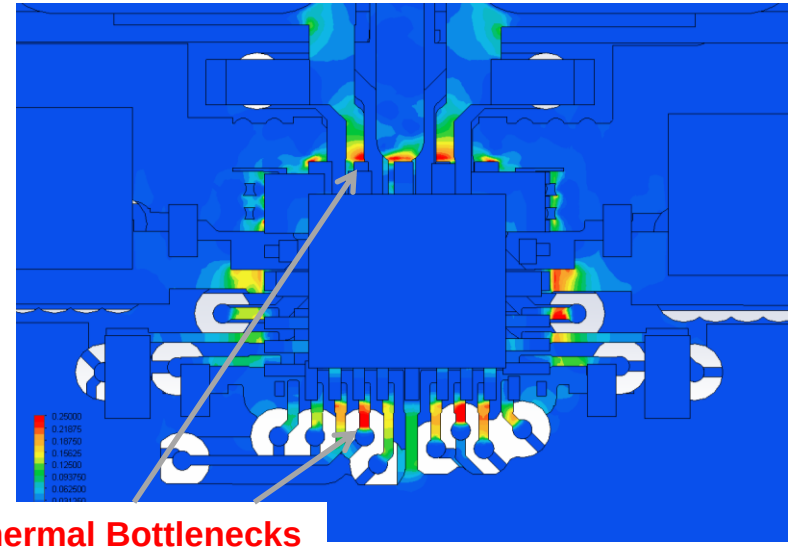
Layout guidelines – “Pizza slice”



1. IC is the heat source and “tiny” compared to PCB.
2. Maximize so that heat is radiating in all 360 degree directions of top and bottom copper plane.
3. Ideally, heat source is placed in center of a PCB.
4. If the tip of the “slice” is not touching the heat source properly then the whole “slice” can not efficiently contribute as heat sink.
5. Make thermal cuts only in heat flow directions.
6. Maximize total copper area, number of layers and Cu thickness on PCB.
7. Utilize the bottom copper side of PCB.
8. Use all available external components like Inductors, resistors and ceramic caps as potential heat conductors to bridge to colder areas / slices.
9. Use larger components like connectors and aluminum caps to improve heat sinking of slices.

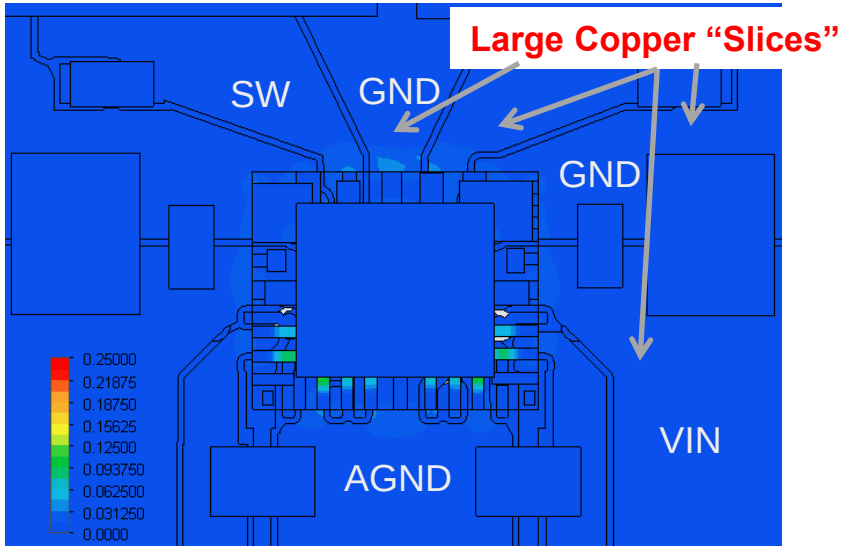
Layout guidelines – optimum cuts

- Non-optimized PCB design
- Die Temp = 124°C
- Θ_{JA} = 32°C/W



Thermally Optimized PCB

- Die Temp = 88.3°C
- Θ_{JA} = 20.4°C/W



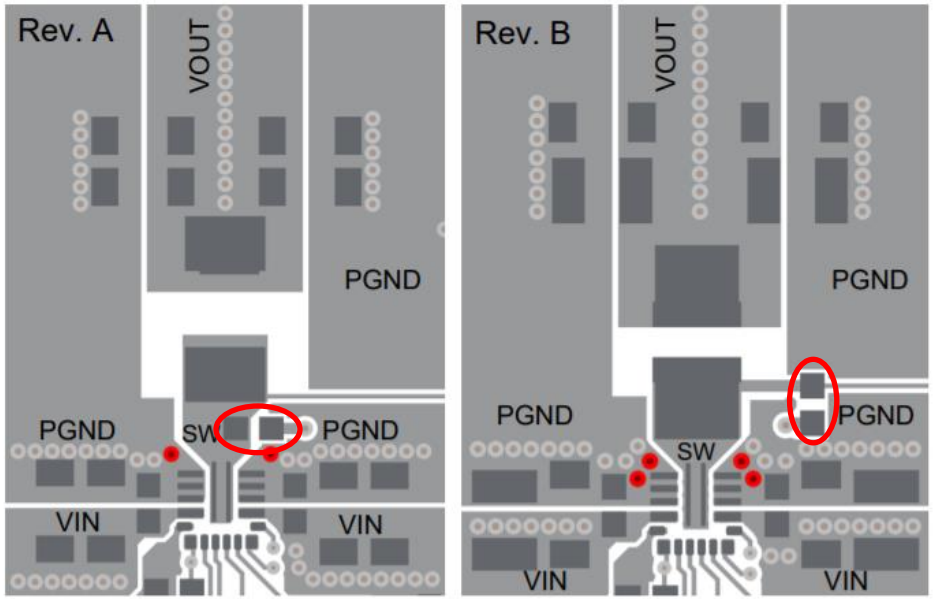
Layout guidelines – high current vias

- High Current Via Requirements:
  - 1A/via max <14 mil diameter
  - 2A/via max >14 mil diameter
  - 5A/via max >40 mil diameter
  - Don’t block high current paths with vias

Example of vias near the IC

V_{IN} = 12 V
T_A = 23 °C

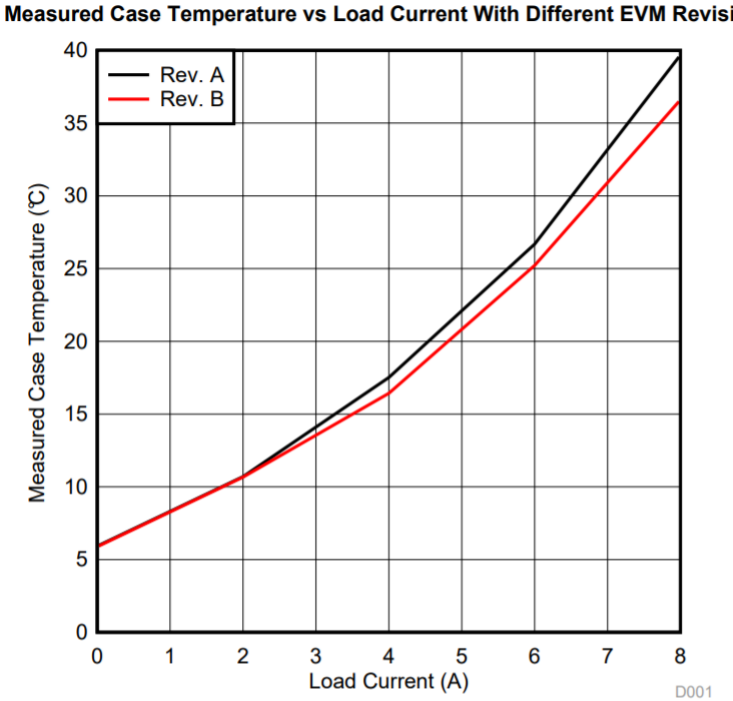
V_{OUT} = 1.8 V
10-minute soak time



REV A

REV B

Figure 8. TPS54824EVM-779 Rev. A vs Rev B. Top Layer Layout



App Note: http://www.ti.com/lit/an/snva839/snva839.pdf

Via density near the IC

V_{IN} = 12 V
T_A = 23°C

V_{OUT} = 1.8 V
10 minute soak time

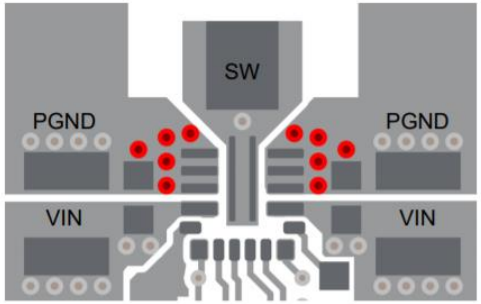


Figure 10. Medium Via Density

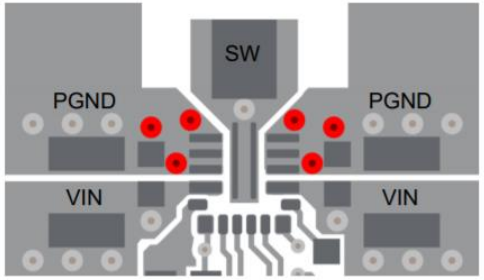


Figure 11. Lower Via Density

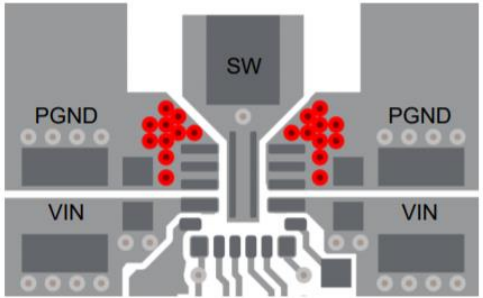


Figure 12. Higher Via Density

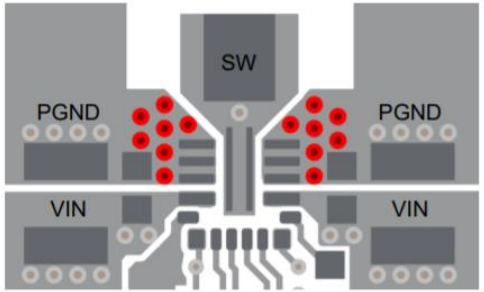
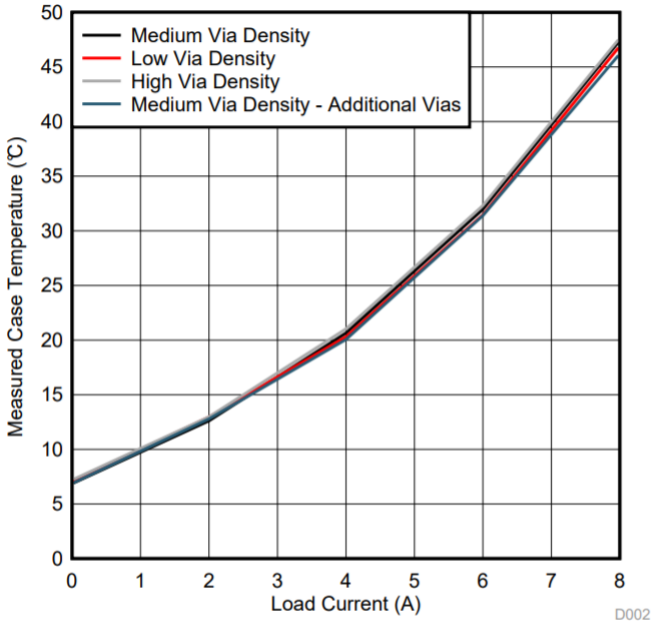


Figure 13. Medium Via Density - Additional Vias

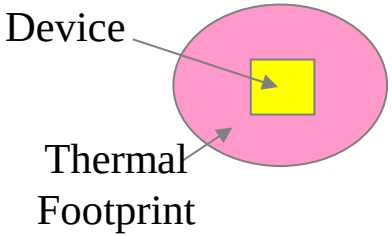
Measured Case Temperature vs Load Current With Different Via Design Rules

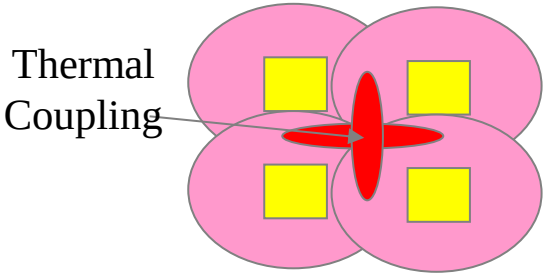


App Note: http://www.ti.com/lit/an/snva839/snva839.pdf

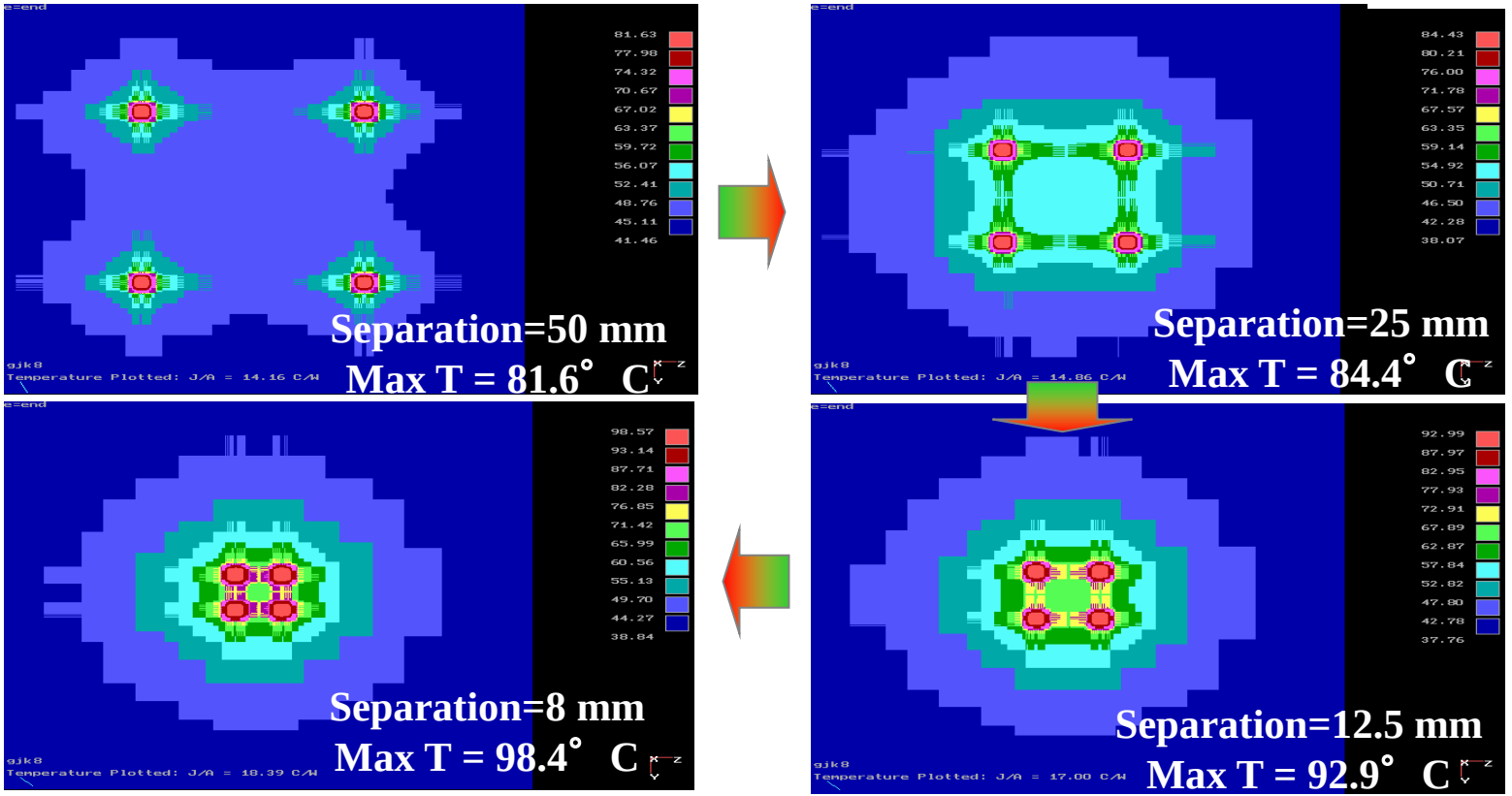
Thermal coupling and footprint

- Thermal Coupling
  - Devices in a system are always thermally coupled
  - Most significant when packages get closer than 2x the package dimension to each other
- Thermal Footprint
  - A thermal footprint is the area of the PCB that participates strongly in the convection and radiation from the package
  - This area is about 18x the package area as shown
    - Top of PCB and bottom of PCB count
- When thermal footprints overlap, changes in junction temperatures are dramatic

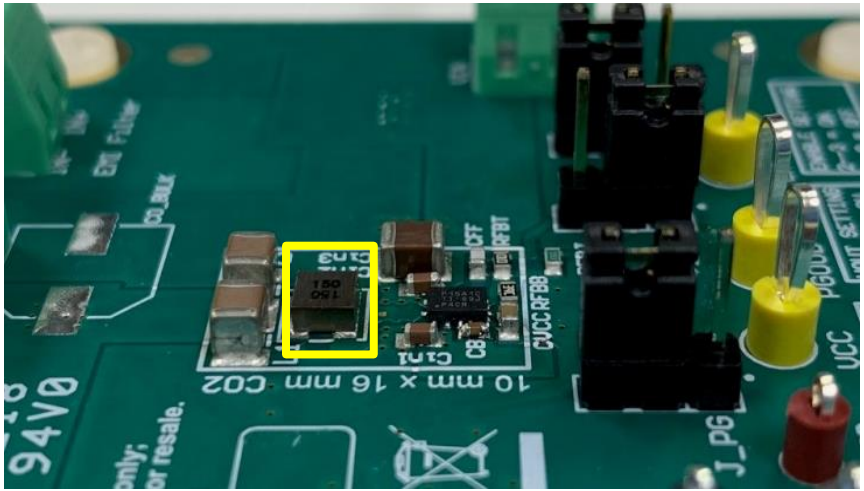




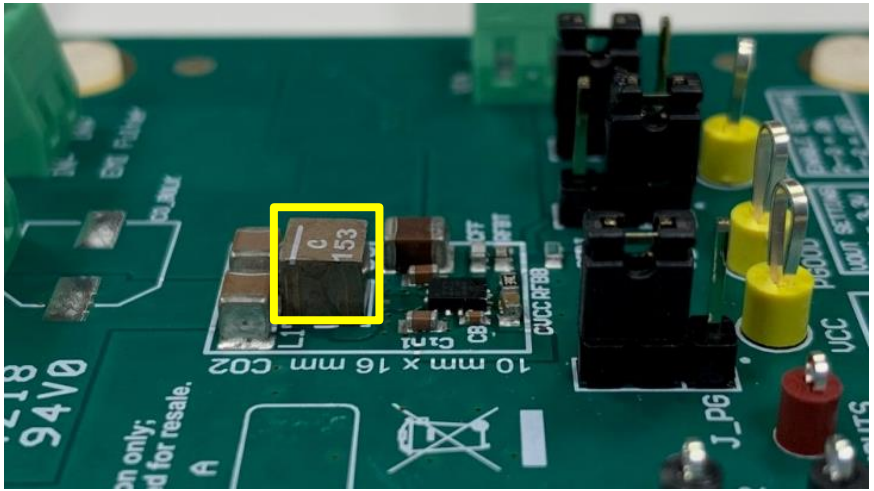
Thermal coupling example



Which design is better for thermals?

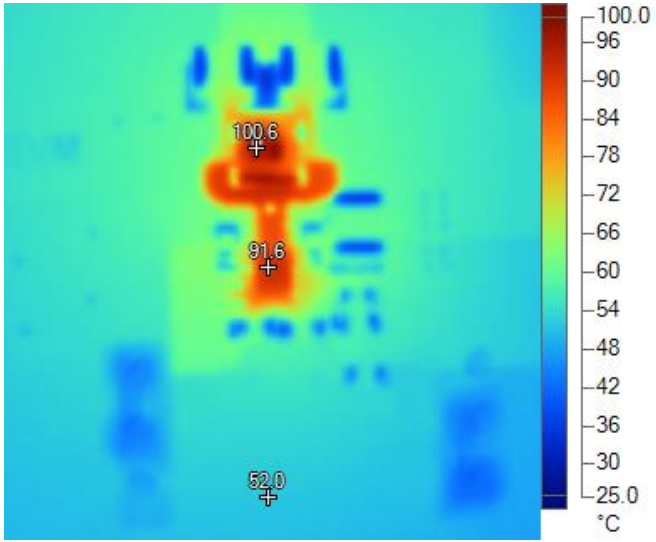


- Inductor 74438335150 (3 mm x 3 mm x 1.5 mm)
- 15 µH, 720 mΩ

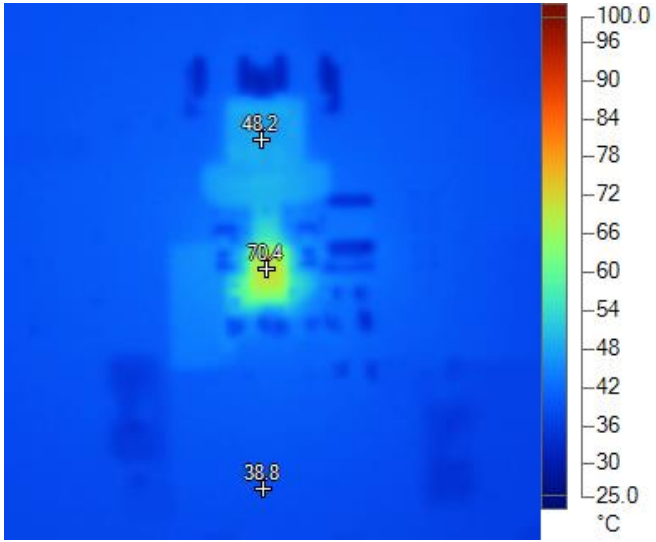


- Inductor XAL4040-153 (4 mm x 4 mm x 4 mm)
- 15 µH, 84 mΩ

Temperature comparison



- **IC Package Temperature ~ 92°C**



- **IC Package Temperature ~ 71°C**

Operating Conditions

- LMR36015
- VIN = 24 V
- VOUT = 5 V
- IOUT = 1.2 A
- Fsw = 2.1 MHz

Summary layout best practices

- Spread out hot devices on PCB
- Maximize GND layer in PCB
- No breaks in heat flow through planes
- Increase PCB layers or thickness
- Widen PCB traces near device
- Thermal vias under or near device
- Airflow (global and local)

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