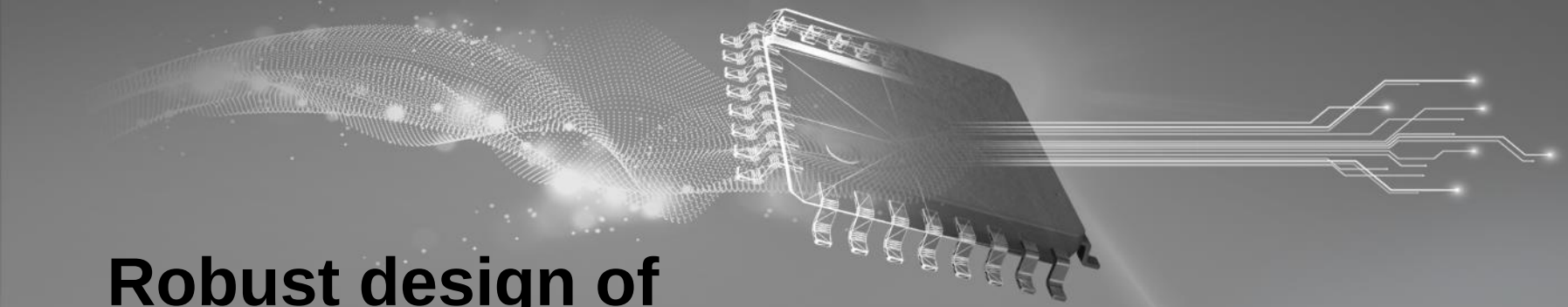
TI TECH DAYS



Robust design of delta-sigma ADC system inputs for EOS immunity – PLC analog input module

Dale Li

Applications, Data Converters – Precision ADC

Agenda

- **EOS and fault conditions**
  - EOS vs ESD
  - Fault conditions
- **Diode and ADC input structure**
  - Diode: Type and characteristic
  - ADC input protection structure
- **Protection topologies for RTD in PLC AI module**
  - Conventional TVS diode
  - TI flat-clamp TVS diode
- **IEC testing (IEC61000-4-x) – RTD in PLC AI module**

ESD vs. EOS – what's the difference?

ESD

- Electrostatic discharge
- Short duration event (1-100ns)
- High voltage (kV)
- Fast edges
- Both "in-circuit" and "out-of-circuit"

EOS

- Electrical overstress
- Longer duration event
  - Milliseconds or more
  - Can be continuous
- Lower voltage
  - May be just beyond absolute maximum ratings
- "In-circuit" event only

EOS from fault or overdriven

– **Fault conditions**

- ✓ Harsh electrical environment
- ✓ High voltage circuit in the system
- ✓ Improper power up sequencing
- ✓ Hot-swap connection and disconnection
- ✓ Loss of power supply but input signal is applied
- ✓ Apply bipolar signal to unipolar input ADC
- ✓ Miswiring
- ✓ Other conditions violating the absolute maximum specifications

– **Key conditions to result in an EOS to RTD application:**

- ✓ Miswiring power supply to RTD input
- ✓ Connect high voltage signal from voltage channel to RTD input

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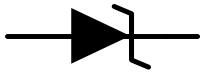
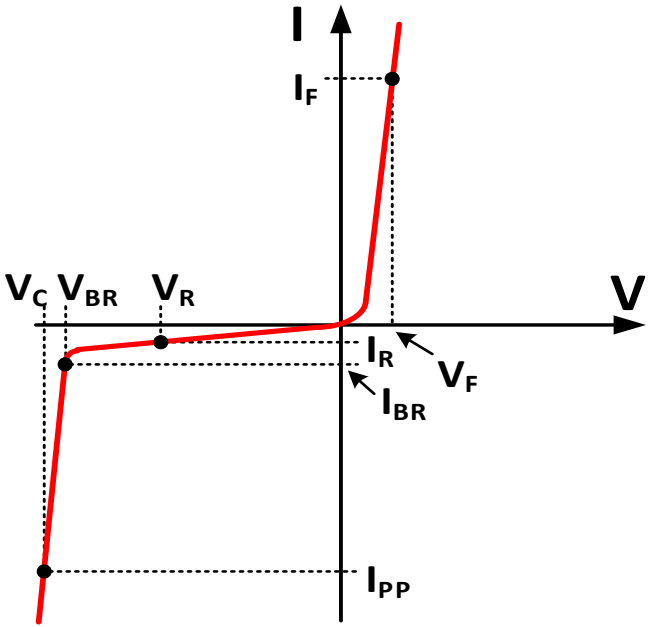
Unidirectional TVS Diode
(Transient voltage suppressor)

Symbol	Parameter
V_{BR}	Breakdown voltage
V_R	Stand-off voltage
V_C	Clamping voltage
V_F	Forward voltage drop
I_{BR}	Breakdown Current @ V_{BR}
I_R	Reverse Leakage @ V_R
I_F	Forward Current @ V_F
I_{PP}	Peak Pulse current @ V_C



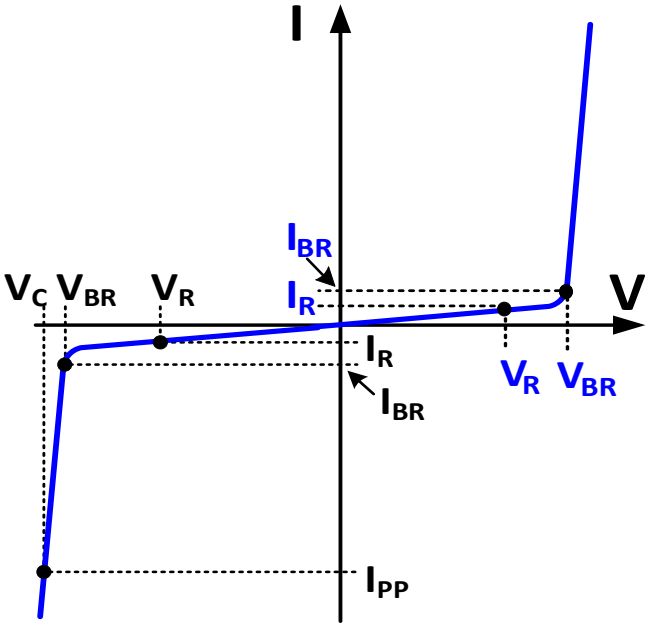
TVS_Uni



Bidirectional TVS diode
(Transient voltage suppressor)

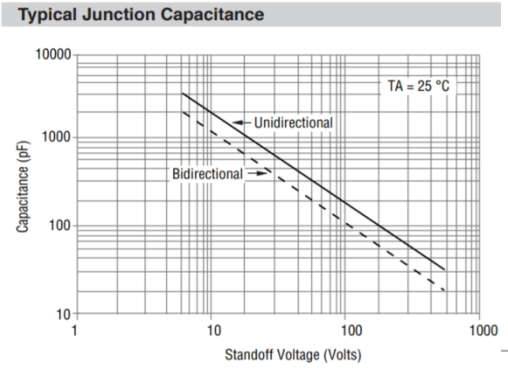
Symbol	Parameter
V_{BR}	Breakdown voltage
V_R	Stand-off voltage
V_C	Clamping voltage
V_F	Forward voltage drop
I_{BR}	Breakdown Current @ V_{BR}
I_R	Reverse Leakage @ V_R
I_F	Forward Current @ V_F
I_{PP}	Peak Pulse current @ V_C

TVS_Bi



Capacitance and leakage current on TVS diode

- **Capacitance**
  - Not constant, change with standoff voltage
  - Junction capacitance changes from hundreds pF up to 10-nF
  - Large power rating diode has higher capacitance and variation
  - Key impact to switch-capacitor input structure SAR ADC

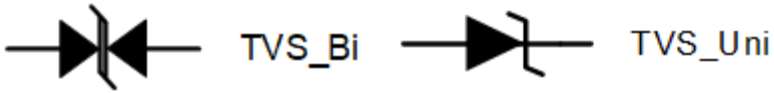


- **Leakage Current**
  - Data sheet from most manufacturers only shows max leakage at room temperature.
  - Same PN from different manufacturers may have different leakage spec.
  - Leakage variation with temperature.
  - Key impact to RTD measurement.

Manufacturers	PN	Leakage current(max at 25°C)
Bourns Inc.	SMBJ14CA	1uA
Littelfuse	SMBJ14CA	1uA
Vishay	SMBJ14CA	1uA
Diodes Inc.	SMBJ14CA	5uA
Taiwan Semi	SMBJ14CA	5uA

TVS vs. Zener

- **TVS Diode**
  - Solid state PN junction
  - Designed for operation in reverse-breakdown region only during over-voltage events
  - Junction area sized to conduct significant current and absorb significant power
  - Specifically designed for large transients such as ESD
  - Can react to overvoltage in pico-seconds

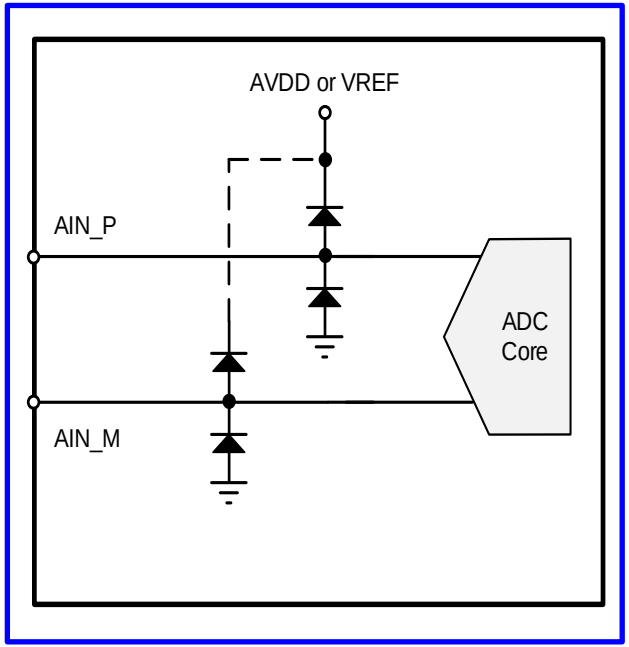


- **Zener**
  - Solid state PN junction
  - Designed for full-time operation in reverse-breakdown region
  - Ideal for voltage regulation
  - Slower reaction time
  - Lower current/power capability

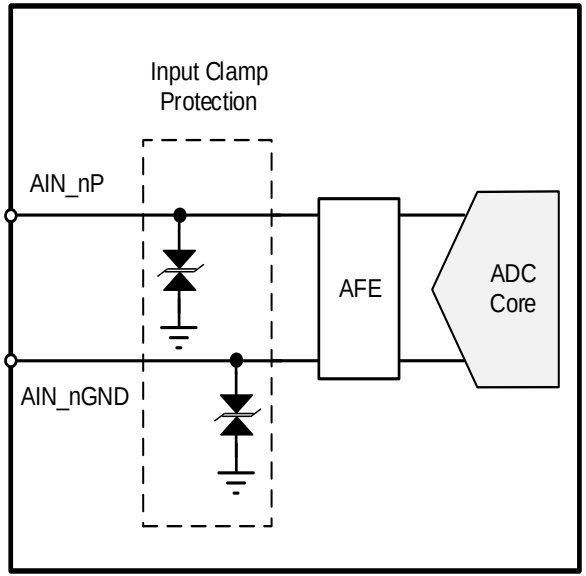
Zener diode

Internal clamp/protection on data converters

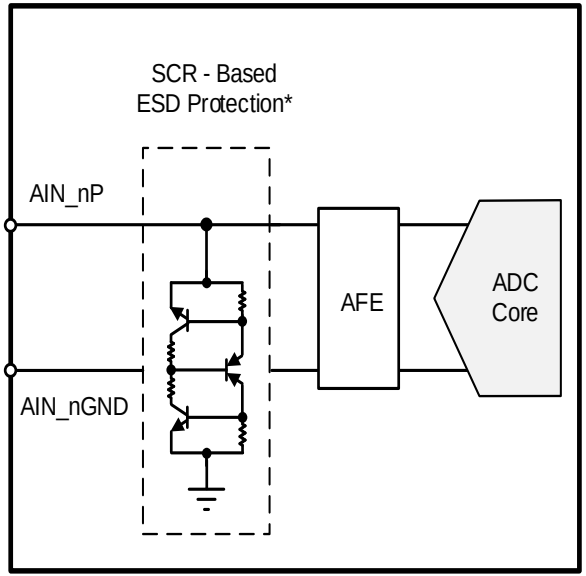
1. Input steering diodes:



2. Back-to-back Zener diode:



3. SCR-based input:



*Bi-directional SCR example

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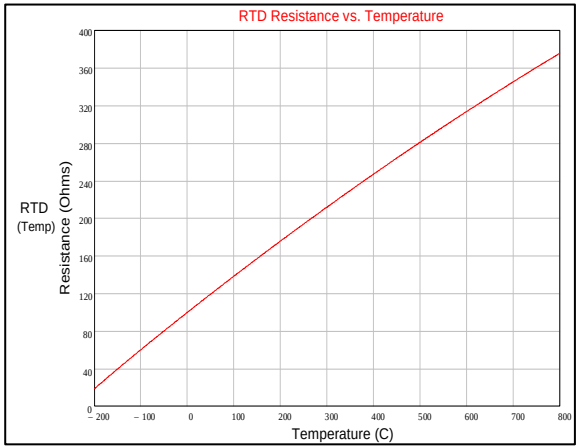
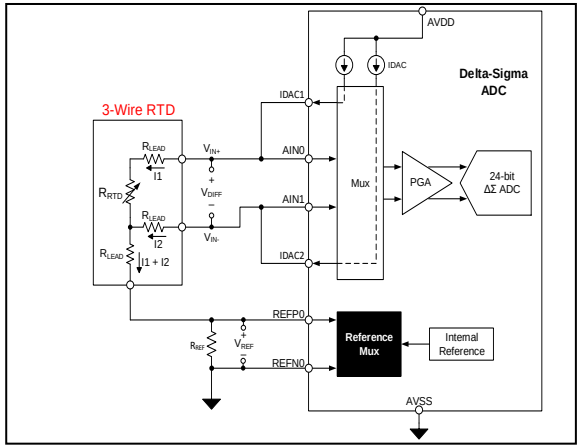
RTD (resistance temperature detector) sensor



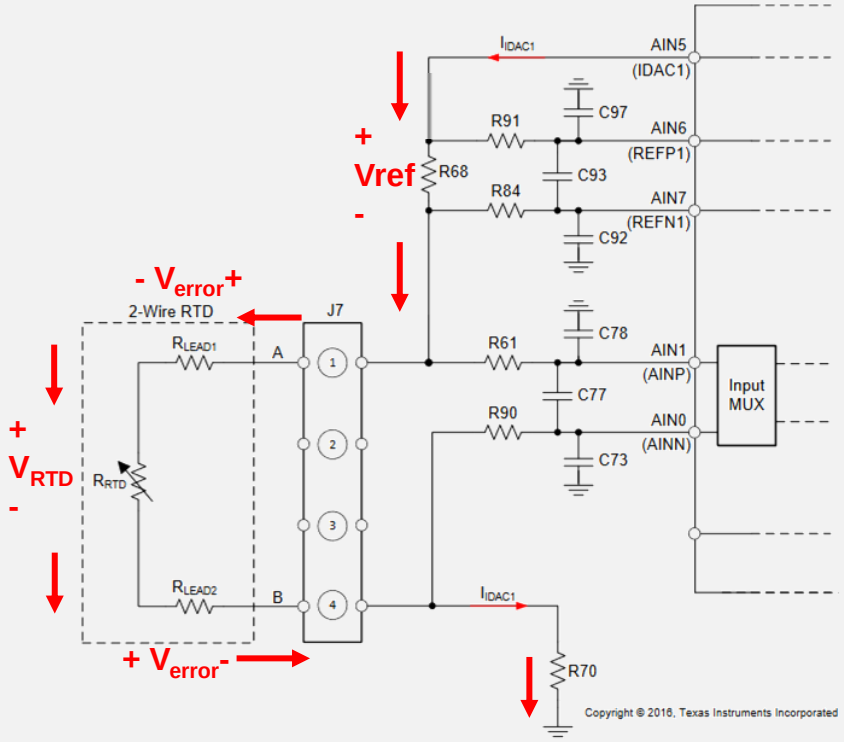


Application notes:
sbaa275.pdf
sbaa310.pdf
sbaa330a.pdf
sbaa334.pdf
sbaa336a.pdf
sbaa329a.pd
sbaa201.pdf

- **PT-100** exhibits 100Ω resistance at 0ºC and has wide temp range: **-200ºC to 850ºC**.
- R varies from **20Ω to 400Ω**, Currents are pumped into RTD and voltage is measured.
- Sensor with a predictable resistance vs. temperature.
- Measure the resistance and calculate temperature based on the resistance vs. temperature characteristics of the RTD material.
- Overstress (EOS) protection is an increasingly popular requirement from customers.

Typical block diagram: 2-wire RTD inputs

2-wire RTD block diagram



Circuit notes

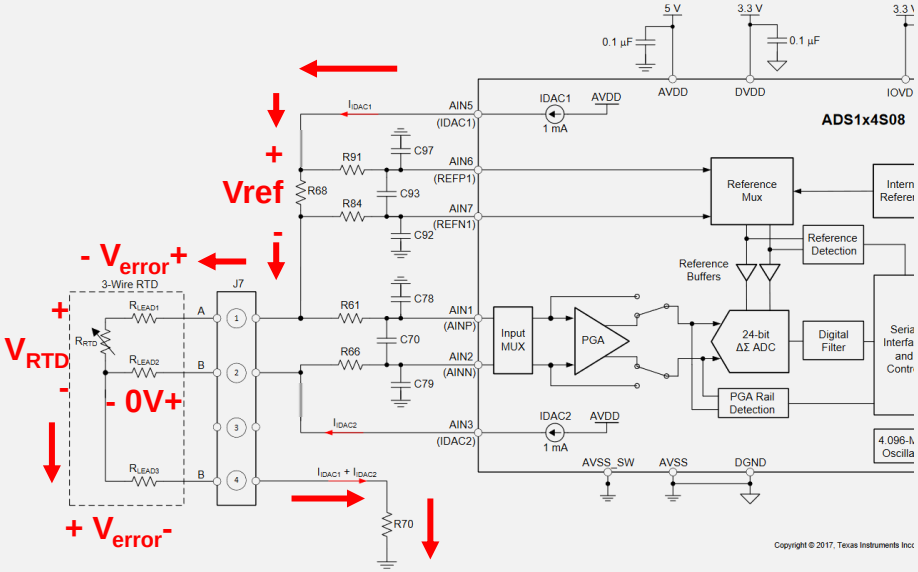
- 2 terminal input
- High-side reference (low-side is possible as well)
- One excitation current required
- No lead wire compensation
- R_{REF} is typically largest source of error

- Differential VREF inputs
- 1x current sources
- Low-noise
- Integrated gain stage

**From ADS124S08 EVM

Typical block diagram: 3-wire RTD inputs

3-wire RTD block diagram



Circuit notes

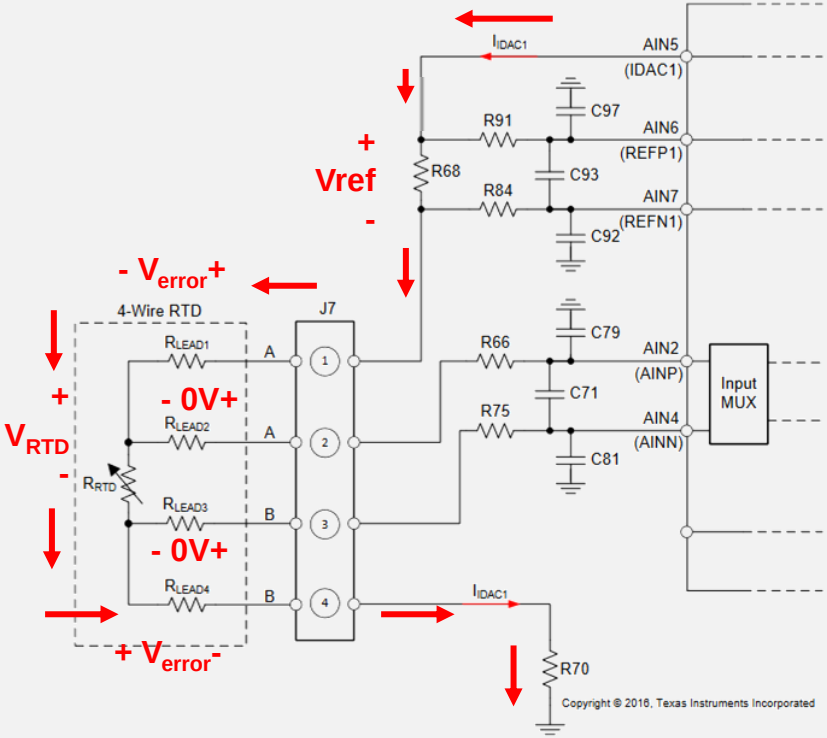
- 3 terminal input
- High-side reference (low-side is possible as well)
- Excitation via 1x or 2x current sources (1x IDAC requires 2x measurements)
- Lead wire compensation is possible
- R_{REF} is typically largest source of error

- Differential VREF inputs
- 2x or 1x current sources
- Low-noise
- Integrated gain stage

**From ADS124S08 EVM

Typical block diagram: 4-wire RTD Inputs

4-wire RTD block diagram



Circuit notes

- 4 terminal input
- High-side reference (low-side is possible as well)
- One excitation current required
- Inherent lead wire compensation
- R_{REF} is typically largest source of error

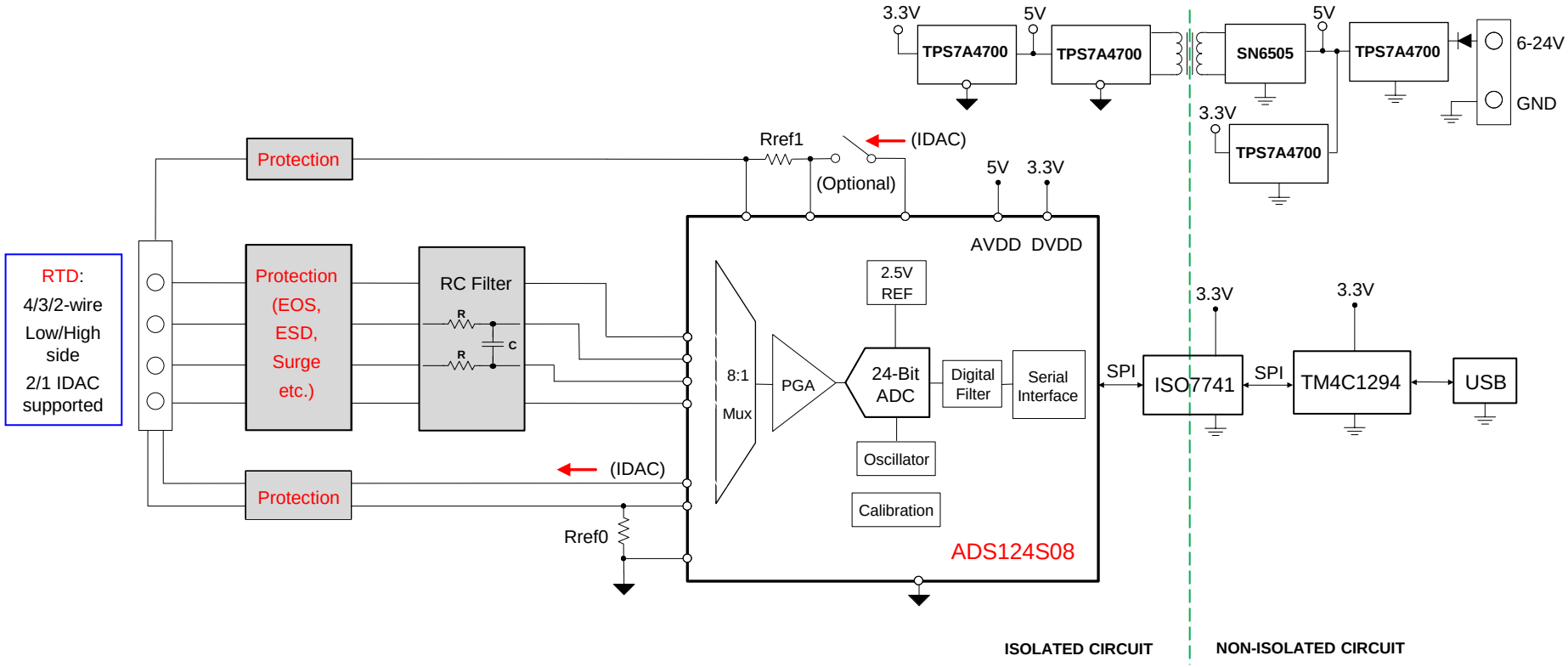
- Differential VREF inputs
- 1x current source
- Low-noise
- Integrated gain stage

**From ADS124S08 EVM

Design dequirements

Parameter	Value
Input sensor	RTD: PT100
Measurement range	-200ºC to 850ºC (20Ω to 400Ω)
EOS fault protection	±30V on RTD input
Resolution	ENOB: >20 bits Noise-free resolution: >17 bits
Accuracy (T_A = -40 to 85°C)	±0.1% at room, ±0.5% full temp range
IEC certifications	ESD: IEC61000-4-2 EFT: IEC61000-4-4 Surge: IEC61000-4-5

Design block diagram: RTD measurement (IEC Testing)



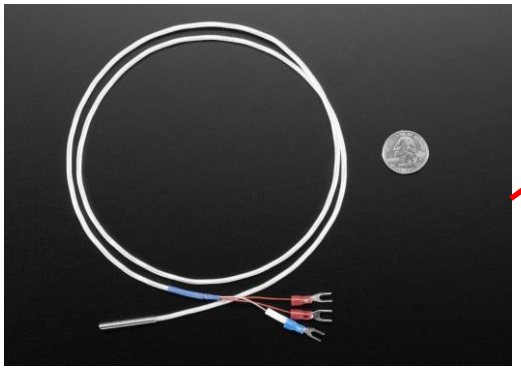
Note: ADS124S08's other channels are used for voltage and current measurement in this design.

Common 3-wire RTD measurement without protection

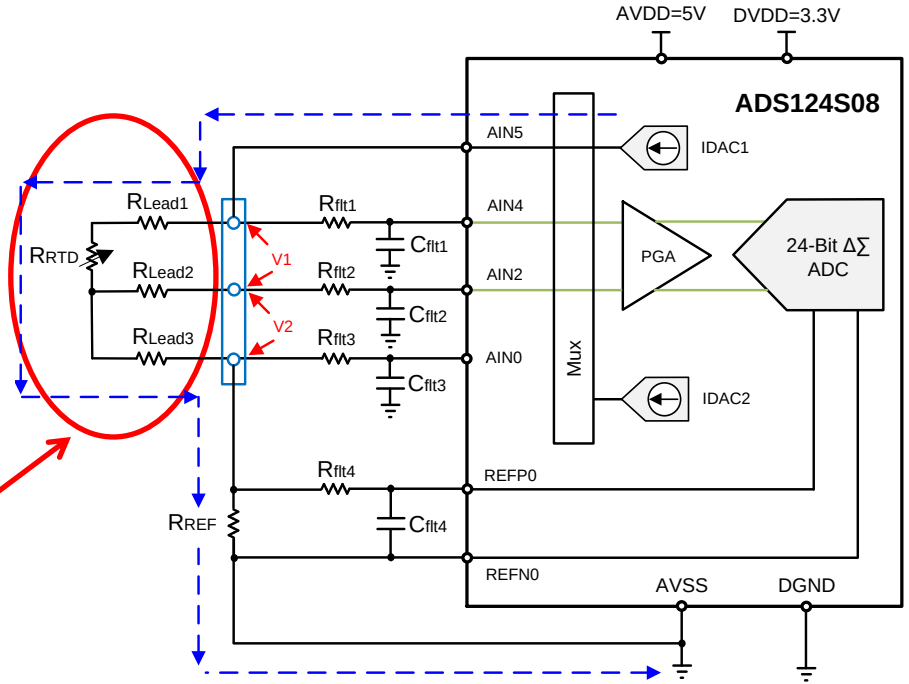
- **Ratiometric measurement**:

  IDAC noise and drift are cancelled.

- **Lead wire resistance cancellation**:
  - ✓ Lead resistance is related to length, material and cross-sectional-area of the conductor.
  - ✓ One IDAC needs two measurements.
- **Two IDACs need current chopping to minimize the effect of mismatched current sources**.



Note: 1-meter PT100 RTD sensor from Adafruit.

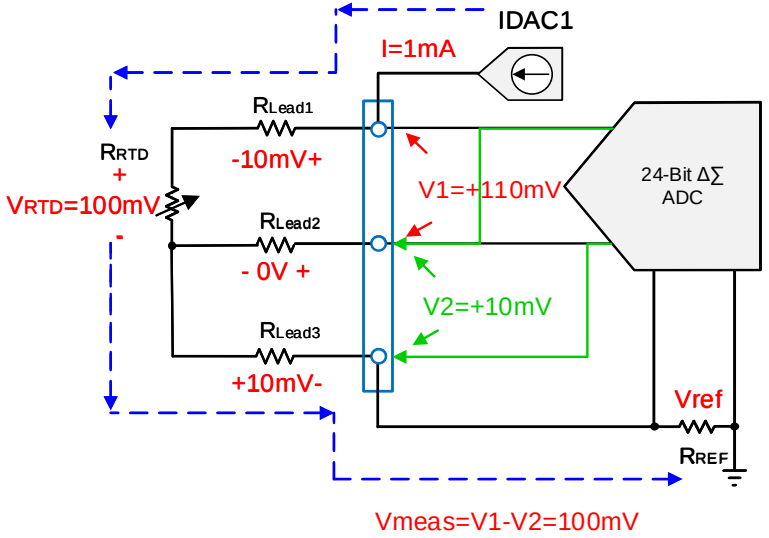


3-wire RTD, low-side reference measurement circuit with one IDAC current source (common-mode capacitor not shown)

Why do we need two measurements

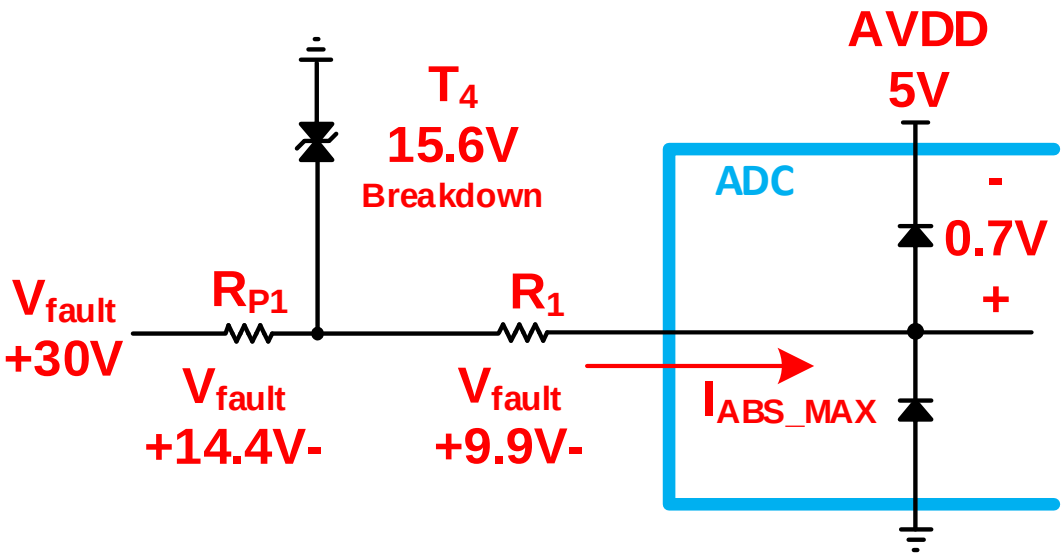
Two measurements by taking difference between V_1 and V_2:

- Cancel lead wire resistance.
- Cancel the offset of ADC.
- Low side reference requires two measurements.
- High side reference measurement only requires one measurement, however the resistor selections (R_{RTD}, R_{ref} and R_{bias}) and IDAC current are limited by compliance voltage.



Note: R_{RTD} =100Ω, R_{Lead1} = R_{Lead2} = R_{Lead3} = 10Ω

ESD / EOS Protection Design



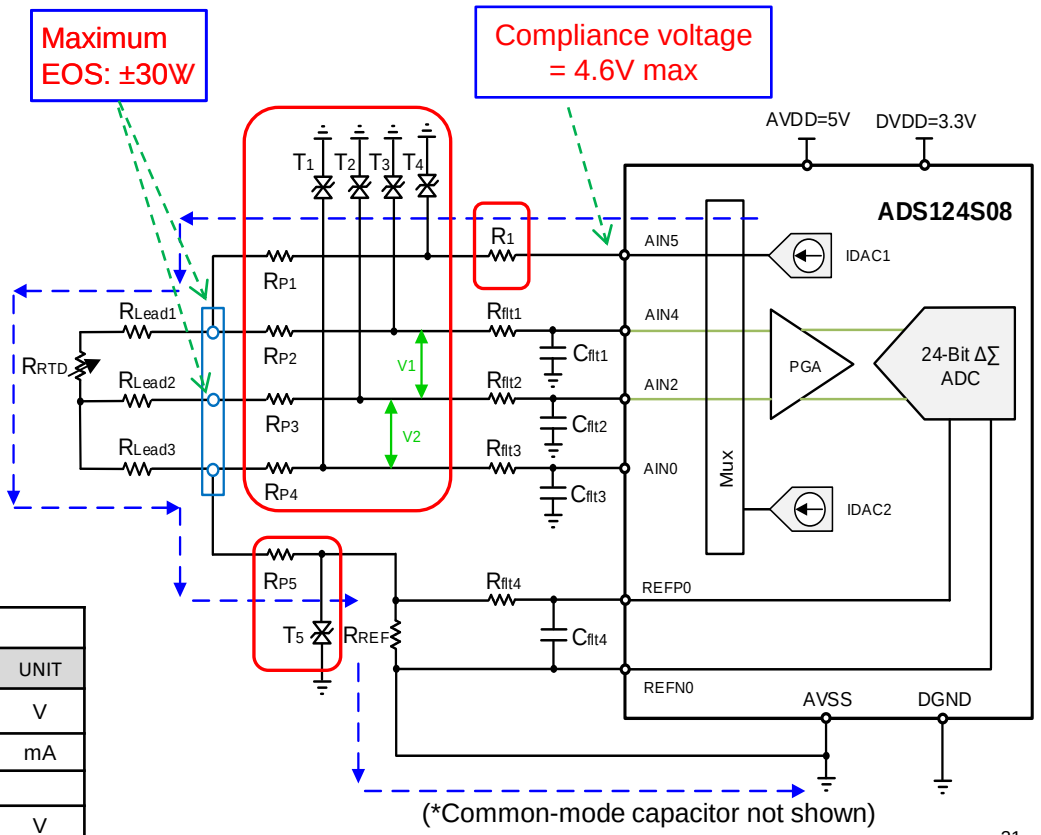
Design Goals

- Assume continuous fault
- Limit I_{ABS_MAX} < 10mA
- Minimize fault power dissipation in R_{P1}, R_1, and T_4
- Make sure normal operation of circuit is functional and has minimal error
  - Compliance limit
  - Leakage Errors

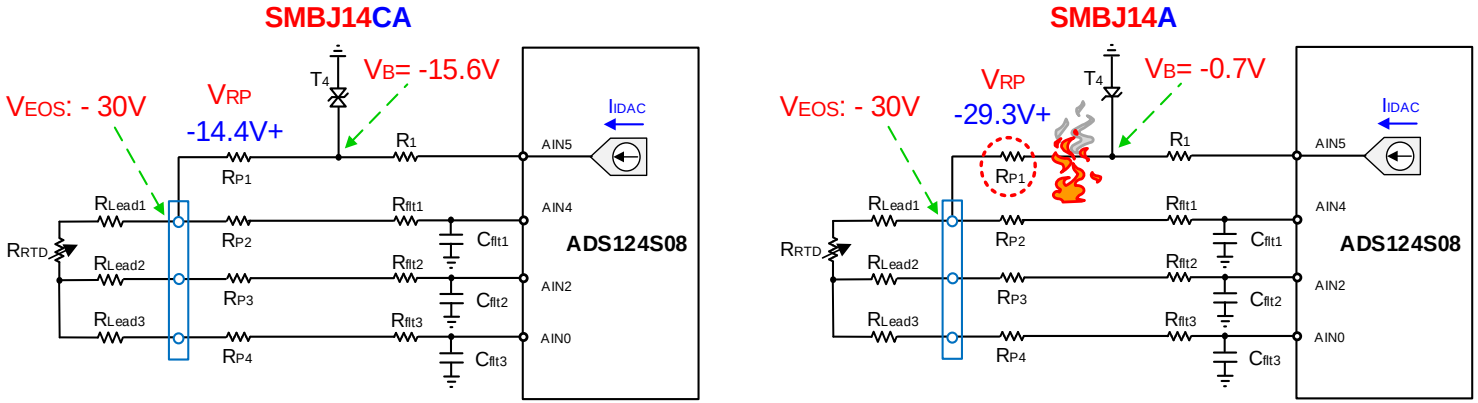
Protection: 3-wire RTD, low-side reference measurement

- **Current limiting resistors:**
  - $R_{P1}/R_{P2}/R_{P3}/R_{P4}$: limit current to TVS and ADC inputs
  - R_1 limits current to IDAC (no R_{flt} on AIN5).
  - Large value R_{P1} and R_1 limit current more:
    - Advantage: lower clamped voltage under fault condition.
    - Disadvantage: higher voltage under normal operation. (violate compliance voltage on IDAC).
  - Small value R_{P1} and R_1 limit less current, have higher power dissipation on R_{P1} and R_1.
  - Mismatching and drift affect accuracy.
- **TVS diode considerations:**
  - Proper standoff voltage(14V) -> tradeoff for R_{P1} and R_1.
  - Bidirectional TVS instead of unidirectional TVS.
  - Leakage current is a key error contribution to accuracy.
  - Temp drift of leakage current affects accuracy.

Absolute Maximum Ratings (Single 5V Power Supply)				
Parameter	MIN	TYP	MAX	UNIT
Analog input voltage (V_{in_Abs})	-0.3		+5.3	V
Analog input current (I_{in_Abs})	-10		+10	mA
Normal input signal				
AINx signal (V_{in})	0		+5	V



Why do we use bidirectional TVS diode?



- Voltage drop across Rp1 can not be acceptable and power dissipation on Rp1 can be a challenge.

Diodes Inc.	**SMBJ14CA** (Bidirectional)	**SMBJ14A** (Unidirectional)
V_B (Breakdown Voltage)	$-15.6V$	$-0.7V$
$V_{RP} = V_{EOS} - V_B$ (Volts on R_P)	$-14.4V$	$-29.3V$
$P_P = \frac{V_{RP}^2}{R_{P1}}$ (Power Dissipation on Rp)	$\frac{(-14.4V)^2}{590\Omega} = 0.351W$	$\frac{(-29.3V)^2}{590\Omega} = \mathbf{1.455W}$

Solution 1: Choose Rp_1 and R_1 with regular TVS diode

Part number	MFG	Reverse standoff voltage(V_R)	Breakdown voltage (V_{BR})		Clamping voltage max (V_C@I_{PP})	Reverse leakage max (I_R@V_R) 25°C	Breakdown current (I_{BR}@V_{BR})	Peak pulse current (I_{PP})	Peak power dissipation (P_{PP})	Steady state power dissipation(P_{PP})
			Min	Max						
SMBJ14CA	Bourns	14V	15.6	17.9	23.2V	1uA	1mA	25.9A	600W	5W

Positive EOS: (+30V)

1	$R_{P1} \geq \frac{V_{EOS\_max} - V_{BR\_min}}{I_{fault}} = \frac{30V - 15.6V}{25mA} = 576\Omega$ $(\boldsymbol{choose\ 590\Omega})$
2	$R_1 \geq \frac{V_{BR\_min} - V_{in\_max}}{I_{ADC}} = \frac{15.6V - 5.3V}{5mA} = 2.06k\Omega$ $(\boldsymbol{choose\ 2.2k\Omega}, 5mA < I_{Ain\_Abs})$

Negative EOS: (-30V)

1	$R_{P1} \geq \frac{V_{EOS\_max} - V_{BR\_min}}{I_{fault}} = \frac{-30V - (-15.6V)}{-25mA} = 576\Omega$ $(\boldsymbol{choose\ 590\Omega})$
2	$R_1 \geq \frac{V_{BR\_min} - V_{in\_min}}{I_{ADC}} = \frac{-15.6V - (-0.3V)}{-5mA} = 3.06k\Omega$ $(\boldsymbol{choose\ 3.4k\Omega}, 5mA < I_{Ain\_Abs})$
Power	$P_{RP1} = \frac{(V_{EOS\_max} - V_{BR\_min})^2}{R_{P1}} = \frac{(-30V - (-15.6V))^2}{590\Omega} = 351mW$ $(\boldsymbol{choose} \geq 0.5W\ for\ P_{RP1})$
Power	$P_{R1} = \frac{(V_{BR\_min} - V_{in\_min})^2}{R_1} = \frac{(-15.6V - (-0.3V))^2}{3.4k\Omega} = 68.85mW$
Power	$P_{TVSmax} = (\frac{V_{EOS\_max} - V_{BR\_min}}{R_{P1}} - \frac{V_{BR\_min} - V_{in\_max}}{R_1}) \cdot V_C = (\frac{-30V - (-15.6V)}{590\Omega} - \frac{-15.6V - (-0.3V)}{3.4k\Omega}) \cdot 23.2V = 461mW$

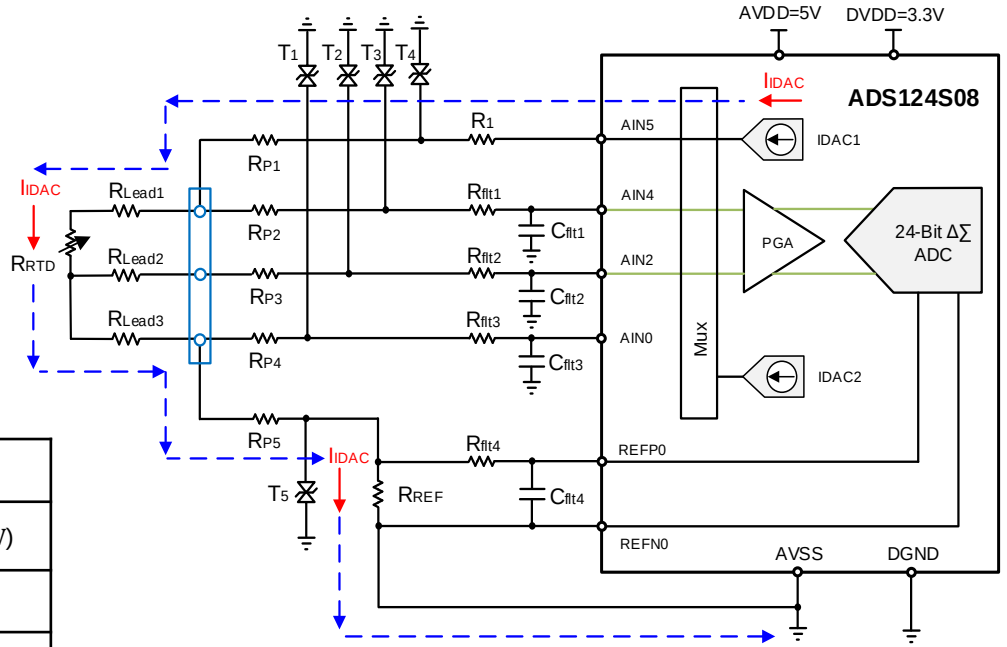
Select worst case!

Select reference resistor - R_{REF}

Parameters known:		
PT100	Min (-200°C)	Max (+850°C)
	20Ω	400Ω *
Lead resistance	Min	Max
	0Ω	10Ω
Components selected: $R_P = 590\Omega, R_1 = 3.4k\Omega$		

* Approximate value.

Select R_{REF} regarding maximum voltage across R_{RTD}:	
1	Use $I_{DAC} = 0.5mA$ (lower sensor self-heating: 0.093mW<0.1mW)
2	$V_{RTD\_max} = I_{IDAC} \cdot R_{RTD\_max} = 0.5mA \cdot 400\Omega = 0.2V$
3	Use Gain = 4, $V_{REF\_min} = V_{RTD\_max} \cdot Gain = 0.2V \cdot 4 = 0.8V$ => $V_{REF} = 1V$
4	$R_{REF} = V_{REF}/I_{IDAC} = 1V/0.5mA = 2k\Omega$



(*Common-mode capacitor not shown)

Compliance Voltage on Iref

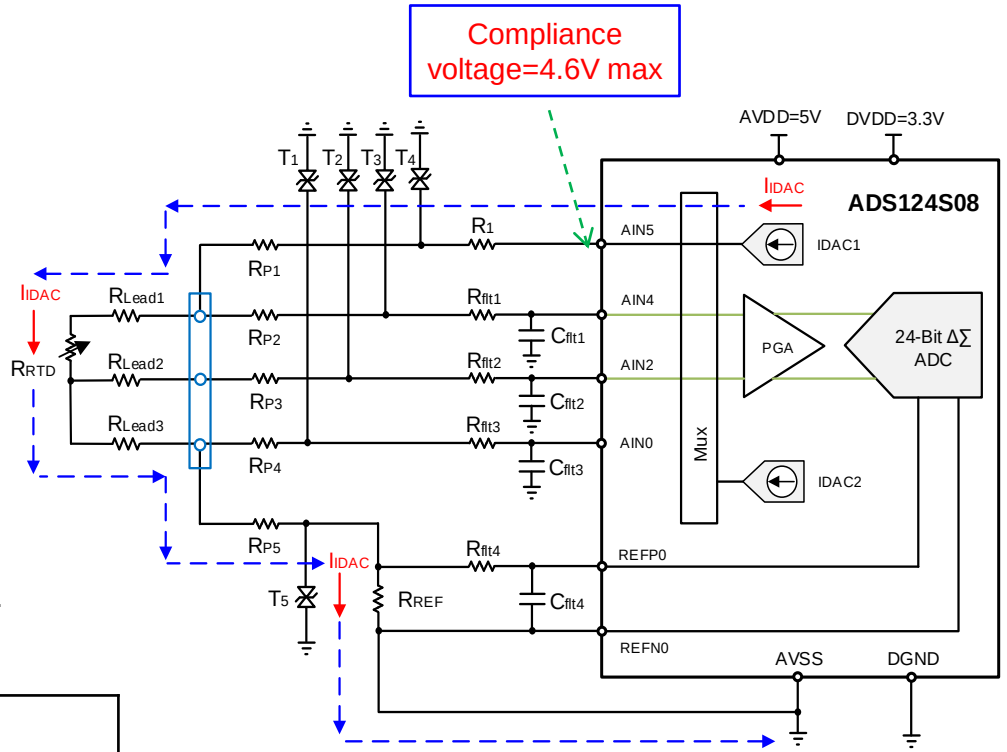
Accuracy		–1.5%		1.5%	
EXCITATION CURRENT SOURCES (IDACS)					
Current settings		10, 50, 100, 250, 500, 750, 1000, 1500, 2000			µA
Compliance voltage[4]	10 µA to 750 µA, 0.1% deviation	AVSS		AVDD – 0.4	V
	1 mA to 2 mA, 0.1% deviation	AVSS		AVDD – 0.6	
	T_A = 25°C, 10 µA to 100 µA	–5%	±0.7%	5%	

5V – 0.4V = 4.6V
Need to confirm that
IDAC input < 4.6V

Verify node voltage

Parameters Known:	
PT100 (max)	400Ω
Lead Resistance (max)	10Ω
Excitation Current (I_{DAC})	0.5mA
Compliance voltage (V_C)	0.4V< V_C< 4.6V *
$V_{(AINx)}$ (Gain=4)	0.45V< $V_{(AINx)}$<4.55V *
Components Selected: $R_P = 590\Omega,\ R_1 = 3.4k\Omega,\ R_{REF} = 2k\Omega$	

* Limit calculated under specified conditions(Gain=4, AVDD=5V).



(*Common-mode capacitor not shown)

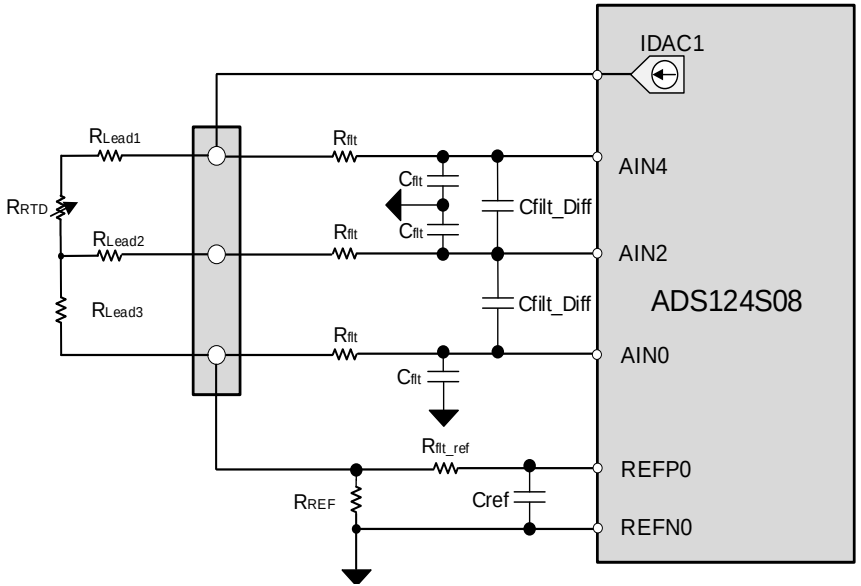
Verify Node Voltage under Normal Operation:

$V_{AIN5} = I_{IDAC} \cdot (R_1 + R_{P1} + R_{lead1} + R_{RTD} + R_{lead3} + R_{P5} + R_{REF}) =$
$0.5mA \cdot (3.4k\Omega + 590\Omega + 10\Omega + 400\Omega + 10\Omega + 590\Omega + 2k\Omega) = \mathbf{3.35V < 4.6V}$ *

Select R_{flt} and C_{flt} for differential and common-mode filter

- Keep bandwidth of differential filter ≥ 10×data rate.
- Keep differential capacitor ≥ 10× Common-mode capacitor.
- Keep input resistance < 10kΩ for proper input sampling.
- Higher resistance helps to limit current to ADC input.
- Keep resistance low on REFN0 since for single power supply.
- Set R_{flt} =R_{flt_ref} = $4.12k\Omega$, C_{flt}=C_{ref} = $470pF$, C_{flt_Diff} = $4.7nF$.

For ADC input filtering:	
1	$f_{in\_Diff} = 1/[2 \cdot \pi \cdot C_{in_{Diff}} \cdot (R_{RTD} + 2 \cdot R_{flt} + R_p)] = 3.67kHz$
2	$f_{in\_CM} = 1/[2 \cdot \pi \cdot C_{flt} \cdot (R_{RTD} + R_{flt})] = 74.9kHz$
For reference input filtering:	
1	$f_{Ref\_filter} = 1/(2 \cdot \pi \cdot C_{ref} \cdot R_{flt\_ref}) + R_{flt})] = 82kHz$



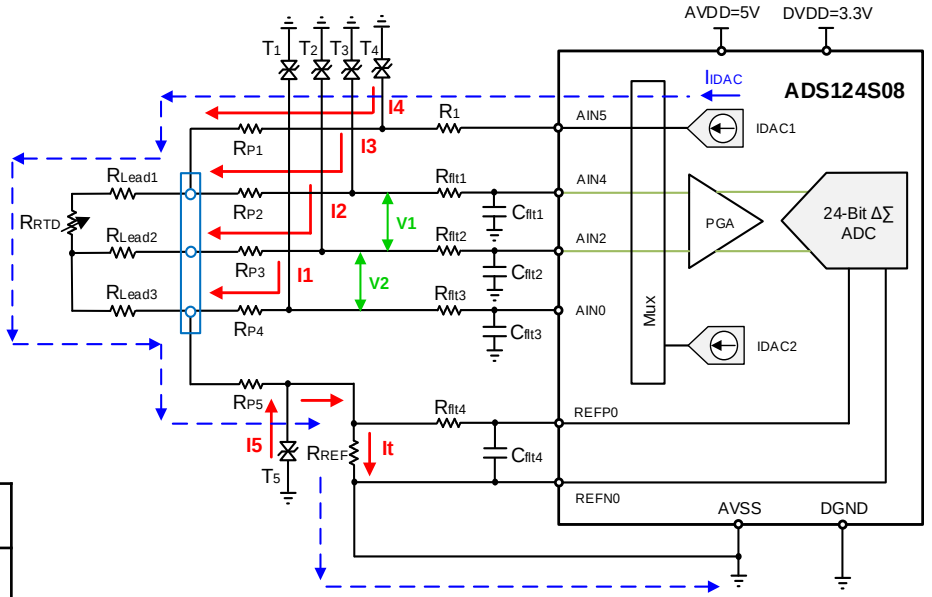
(*Protection circuitry not shown)

*see RTD Ratiometric Measurements and Filtering Using the ADS1148 and ADS1248.

Calculated and simulated error with SMBJ14CA diode

- **TVS leakage current are added:**
  - ➢ I3 and I4 through both R_{RTD} and R_{REF}.
  - ➢ I2 and I1 through R_{REF} only.
- **Leakage current on SMBJ14CA from Bourns**: **I_{leak} = 1uA**

  (maximum at room temp, no spec over temp)



(*Common-mode capacitor not shown)

Additional error (maximum) at room temperature:

$\text{Ratio}_{\text{Ideal}} = (I_{DAC} \cdot R_{RTD} \cdot \text{Gain})/(I_{DAC} \cdot R_{REF}) = 400\Omega \cdot 4/2k\Omega = 0.8$
$V_1 = (I_{DAC} + I_3 + I_4) \cdot (R_{RTD} + R_{lead1}) + I_3 \cdot R_{RP2} - I_2 \cdot (R_{P3} + R_{lead2})$
$V_2 = (I_{DAC} + I_2 + I_3 + I_4) \cdot R_{lead3} + I_2 \cdot (R_{RP3} + R_{lead2}) - I_1 \cdot R_{RP4}$
$\text{Ratio}_{\text{Actual}} = (V_{meas\_error} \cdot \text{Gain})/V_{REF} = ((V_1 - V_2) \cdot \text{Gain})/(R_{REF} \cdot (I_{DAC} + I_1 + I_2 + I_3 + I_4 + I_5))$ $= (((I_{DAC} + 2I) \cdot R_{RTD} - 3I \cdot R_{lead}) \cdot \text{Gain})/(R_{REF} \cdot (I_{DAC} + 5I)) = 0.795$ *
$\text{Error} = (\text{Ratio}_{\text{Actual}} - \text{Ratio}_{\text{Ideal}})/\text{Ratio}_{\text{Ideal}} \cdot 100\% = -0.625\%$

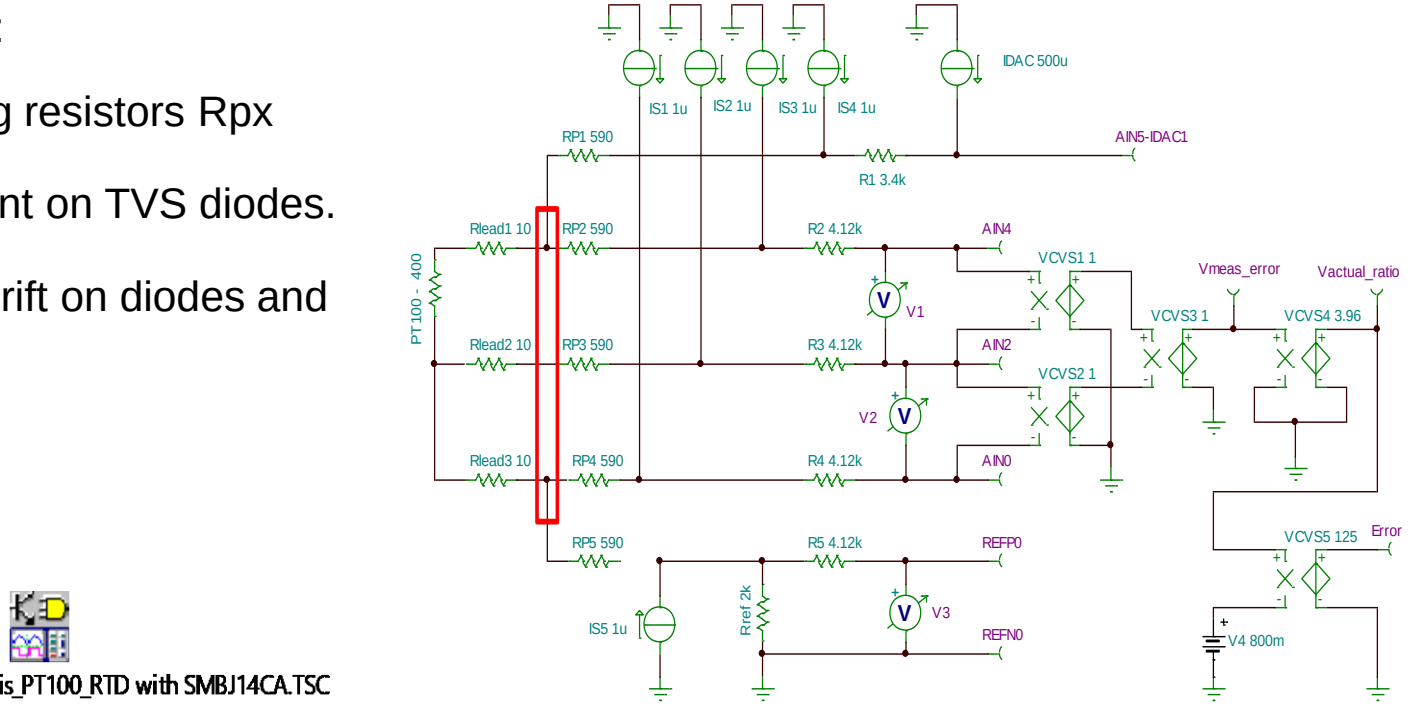
← **Accuracy desired: ±0.5%**

* *Note*: $I_1 = I_2 = I_3 = I_4 = I_5 = I$

Component mismatch - Monte Carlo simulation in TINA™-TI

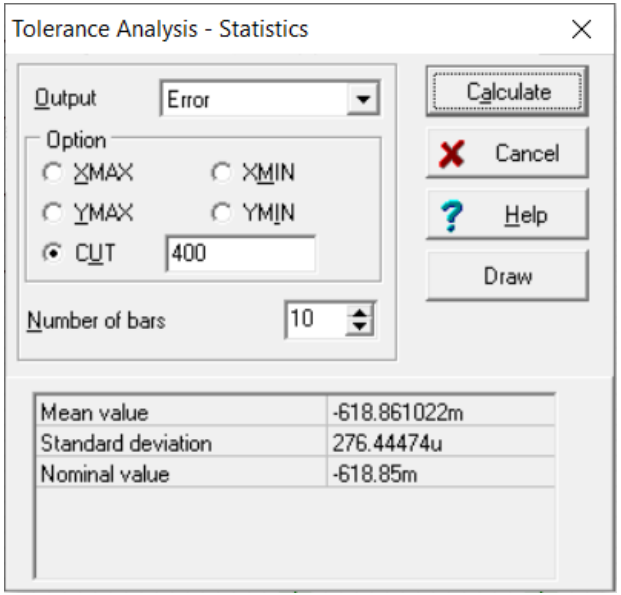
Mismatch from:

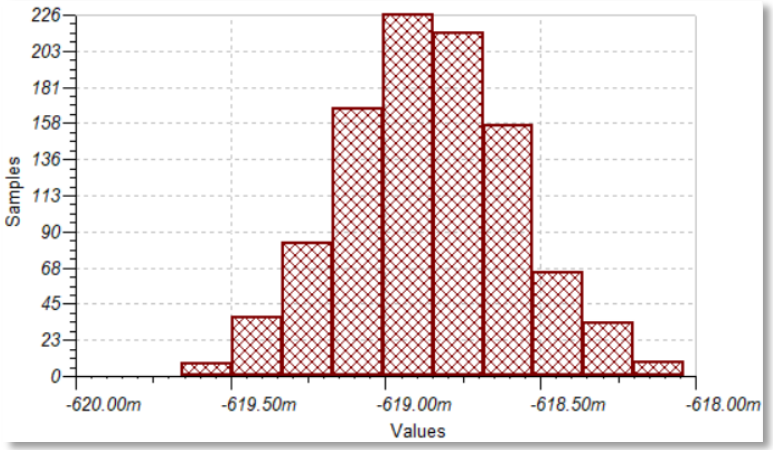
- Current limiting resistors Rpx
- Leakage current on TVS diodes.
- Temperature drift on diodes and resistors.



Monte Carlo_Error Analysis_PT100_RTD with SMBJ14CA.TSC

Component Mismatch - Monte Carlo Simulation - Cont'd





Press draw to get a graph of the histogram

$$TypError = \frac{standard\ deviation}{Mean} \cdot 100 = \left(\frac{276.44474u}{-618.861022m}\right) \cdot 100 = \pm 0.045\%$$ For 68.26% of the population

$$MaxEerror = 3 \cdot Typical = 3 \cdot (\pm 0.045\%) = \pm 0.135\%$$ For 99.73% of the population

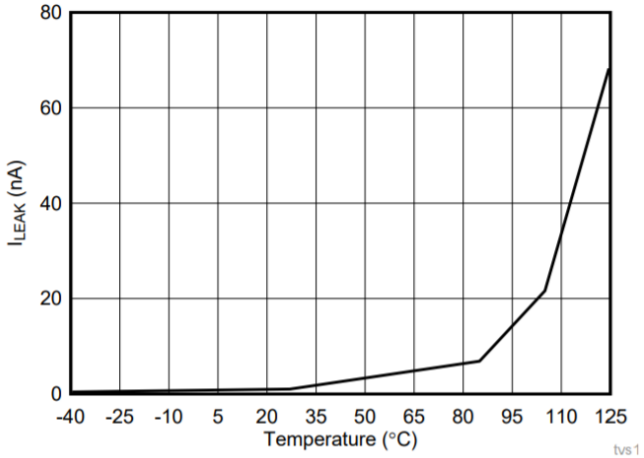
Error with low leakage current of TVS diode

Part number	MFG	Reverse standoff voltage (V_R)	Breakdown voltage (V_{BR})		Clamping voltage max (V_C@I_{PP})	Reverse leakage (I_R@V_R)			Peak power dissipation W (P_{PP})	
			Min	Typ		Typ at 27°C	**Max** at 27°C	**Max** at **85°C**	8/20us	1ms
TVS1401	TI	14V	17.1	17.6	22.2	1.1nA	30nA	**260nA**	600	120
SMBJ14CA	Bourns	14V	15.6	17.2	23.2		**1uA**			600

RTD system error calculated from leakage current:

PN	MFG	Error	Temperature
TVS1401	TI	**-0.16%**	**85°C**
SMBJ14CA	Bourns	**-0.625%**	**25°C**

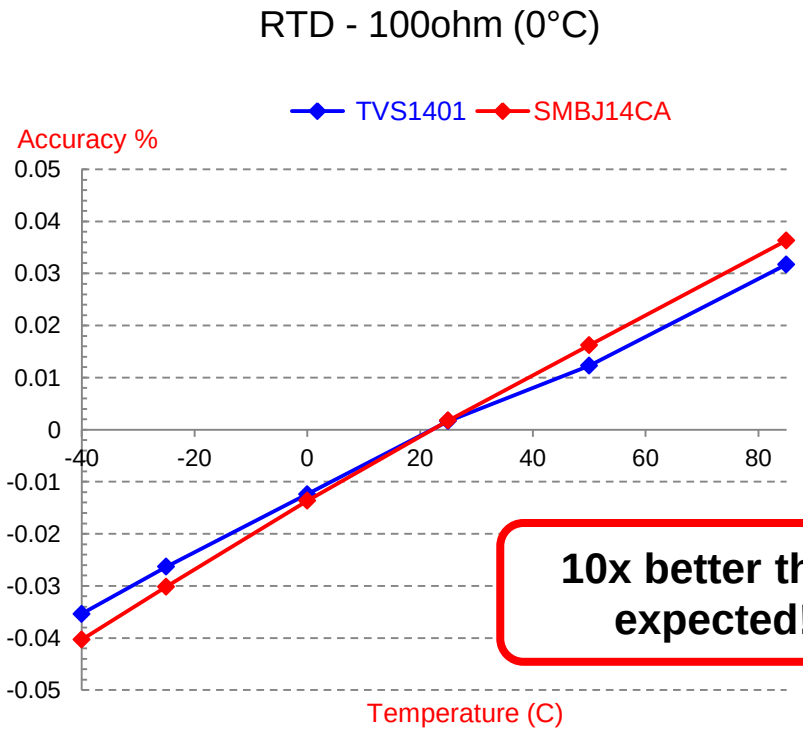
Accuracy desired: ±0.5%

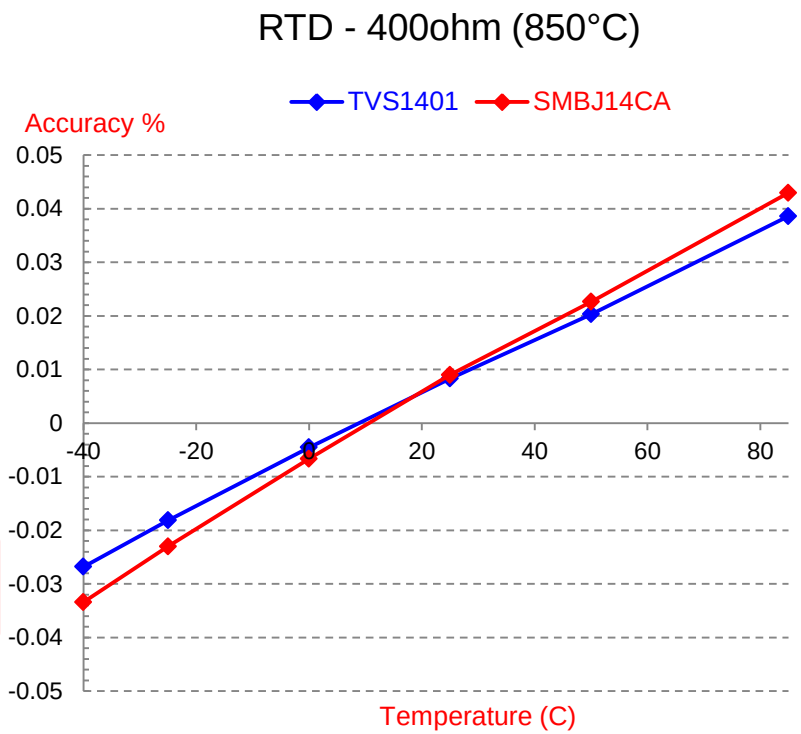


Leakage Current vs Temperature at ±14V on TVS1401.

Note: The error with TVS1401 at room temp is much smaller.

RTD measurement: accuracy vs. temperature

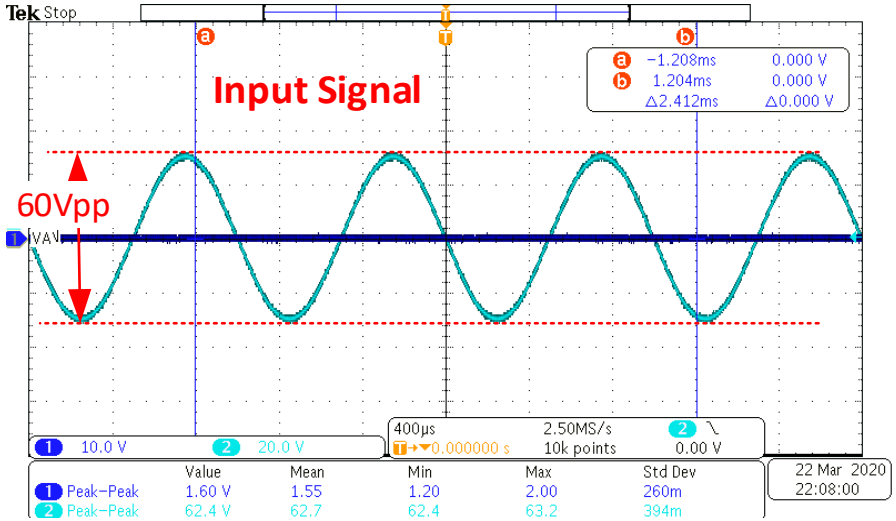


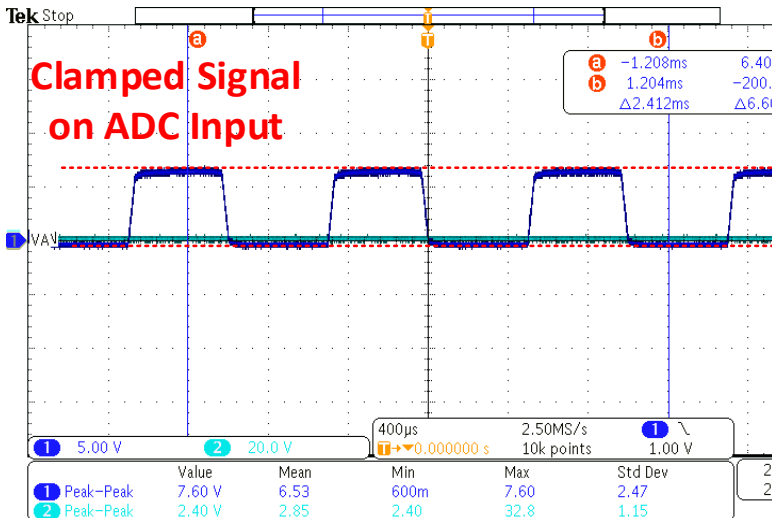


10x better than expected!

Conditions: 0.1% 10ppm/°C resistors for Rp and R1, 0.01%, 5ppm/°C resistor for Rref.

EOS protection verification on ADC input





Agenda

- **EOS and fault conditions**
  - EOS vs ESD
  - Fault conditions
- **Diode and ADC input structure**
  - Diode: Type and characteristic
  - ADC input protection structure
- **Protection topologies for RTD in PLC AI module**
  - Conventional TVS diode
  - TI flat-clamp TVS diode
- **IEC testing (IEC61000-4-x) – RTD in PLC AI module**

Electromagnetic compatibility (EMC) tests

IEC – International Electrotechnical Commission

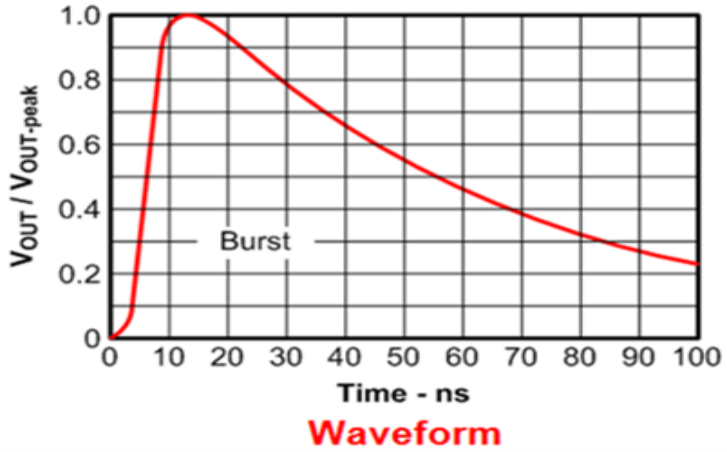
- Promotes international cooperation on standardization
- Created test standards for electronics
- IEC 61000-4 standard
  - IEC 61000-4-2: Electrostatic discharge (**ESD**)
  - IEC 61000-4-3: Radiated electromagnetic interference (EMI)
  - IEC 61000-4-4: Electrical fast transients (**EFT**)
  - IEC 61000-4-5: **Surge**
  - IEC 61000-4-6: Conducted electromagnetic interference (EMI)

* Precision Labs - Op Amps: Electrical Overstress

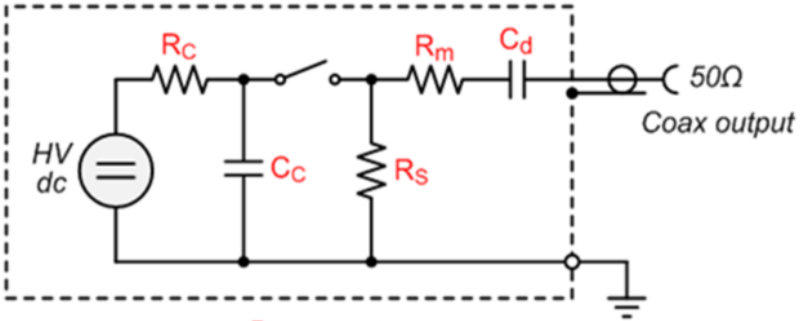
Electrical fast transient (EFT) immunity

IEC61000-4-4

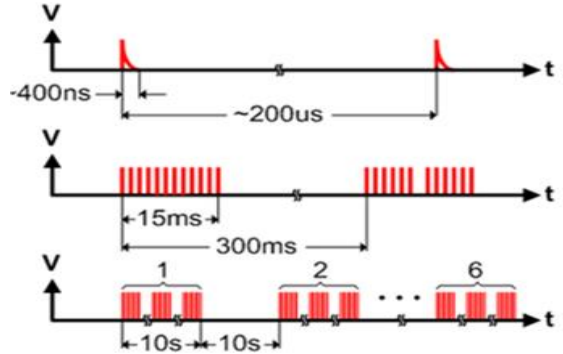
Simulates everyday switching transients caused by interruption of inductive loads, relay bounces, etc.



Waveform



Generator



Test pulses

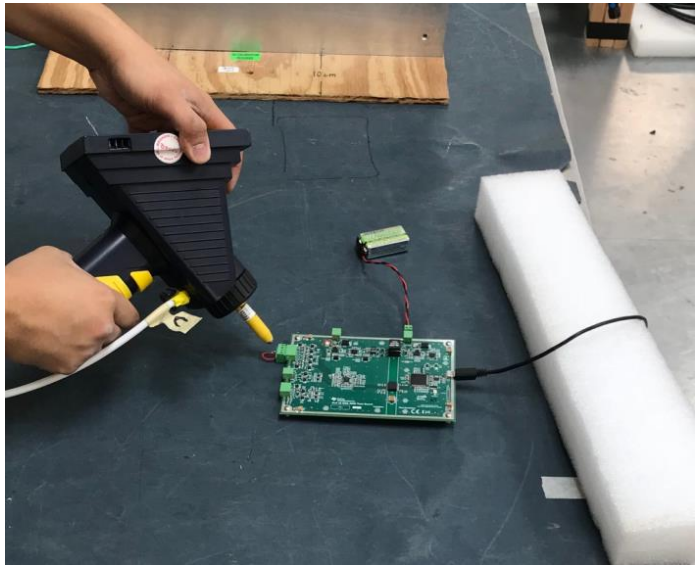
* Precision Labs - Op Amps: Electrical Overstress

IEC 61000-4-4 threat levels

	Power supply port		I/O, signal, data & control lines	
Level	**Open-circuit voltage (kV)**	**Short-circuit current (A)**	**Open-circuit voltage (kV)**	**Short-circuit current (A)**
1	0.5	10	0.25	5
2	1	20	0.5	10
3	2	40	1	20
4	4	80	2	40

* Precision Labs - Op Amps: Electrical Overstress

IEC 61000-4 test setup – RTD hardware



ESD

EFT

IEC61000-4 tested RTD module with TVS1401 EOS protection solution

Standard		Type	Level	Outcome	Grade
ESD Immunity	IEC 61000-4-2	Contact	±8kV	Passed	Class B
		Air	±15kV	Passed	Class B
EFT Immunity	IEC 61000-4-4	5kHz	±4kV	Passed	Class B
		100kHz	±4kV	Planning	
Surge Immunity	IEC 61000-4-5			Planning	

Thank you!

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from PADC team

TI Precision Labs – ADCs: Electrical Overstress on Data Converters

https://training.ti.com/eos-and-esd-adc?cu=1128375

TEXAS INSTRUMENTS

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