Texas Instruments

HIGH VOLTAGE SEMINAR

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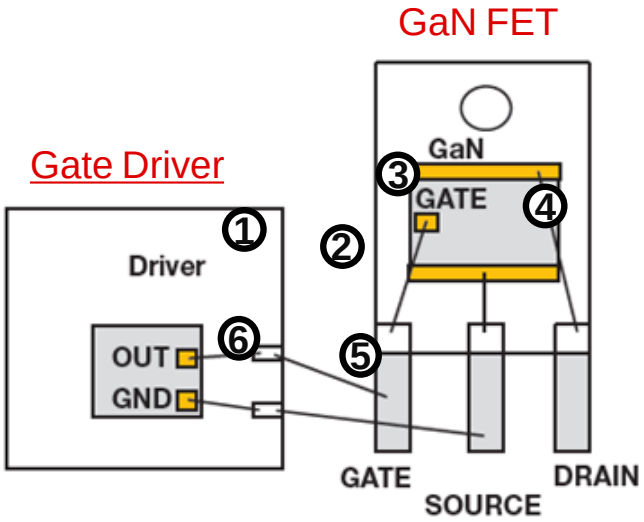
GaN FETS DEMYSTIFIED – YOUR FAQS

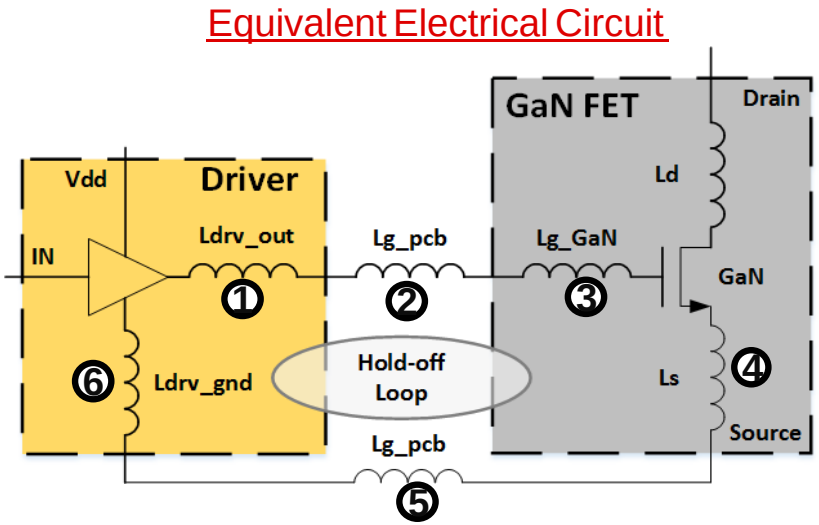
Agenda

- Why is an integrated driver necessary for high-frequency design?
- What's GaN direct-drive structure?
  - Direct drive vs. Cascode
- Does GaN have a body diode?
  - Third quadrant conduction
- How to minimize GaN's 3rd quadrant conduction losses?
- How can integrated smart features and protection in GaN simplify design and enhance robustness?
- What are GaN FET package variants and cooling strategies?
  - Bottom vs. top side cooled device
- How can GaN can reduce overall system cost?

Why is an integrated driver necessary for high-frequency design?

- Introduction to parasitic inductances

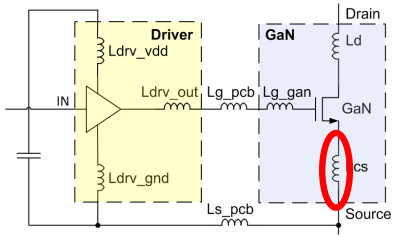


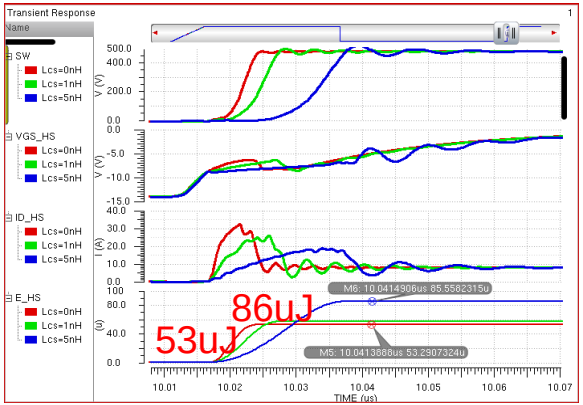


- Parasitic inductances cause switching loss, ringing and reliability issues, especially at higher frequencies

Why is an integrated driver necessary for high-frequency design?

- Common Source inductance reduces the di/dt during turn-on and turn-off.
  - Increases power dissipated during the di/dt ramp
- 5nH common source inductance increases turn-on loss by 60%

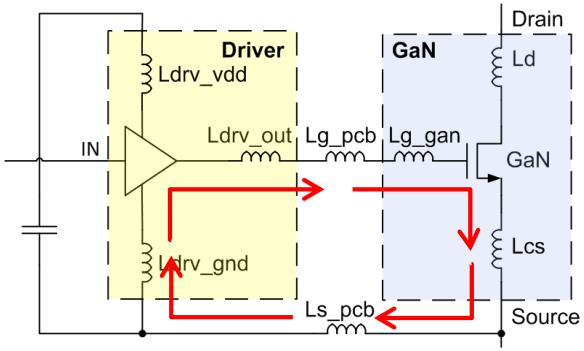


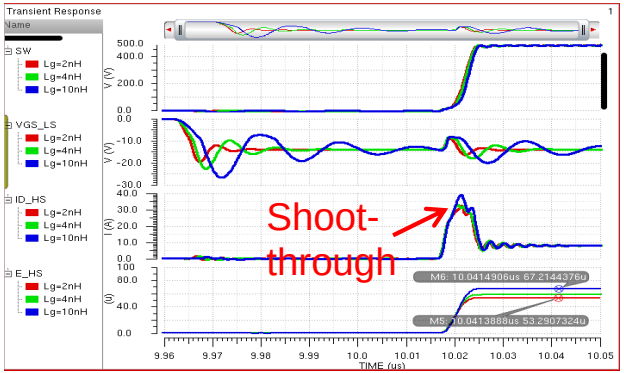


High-side turn on versus common-source inductance: red = 0 nH, green = 1 nH, blue = 5 nH

Why is an integrated driver necessary for high-frequency design?

- Gate loop inductance increases the impedance between the gate and the driver.
  - Limits the ability to hold off the GaN device during the Vds ramp
  - Shoot through increases the power dissipated in the high-side device and can cause it to fail due to SOA.
- Gate loop inductance increases ringing
  - Higher stress on gate
  - Ringing can cause the device to turn-on/off
  - Loop resistance is required to dampen ringing

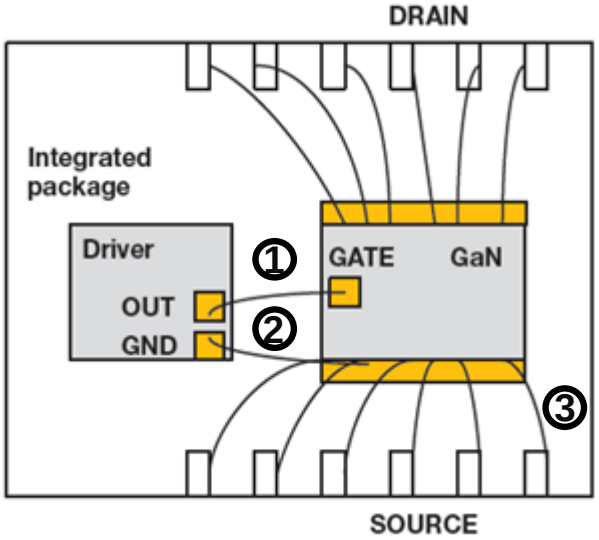




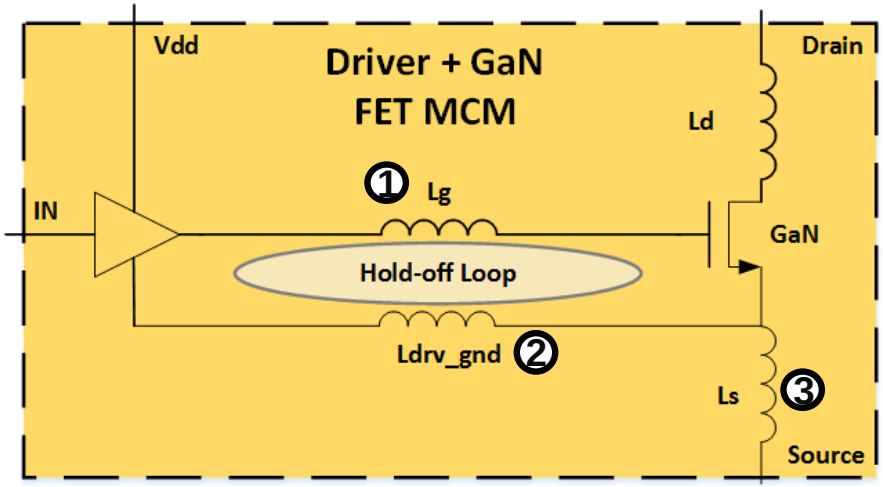
Low-side hold-off versus gate-loop inductance
red = 2 nH, green = 4 nH, blue = 10 nH

Integrated driver: lowest parasitic

GaN FET/Driver Integrated Package



Equivalent Electrical Circuit

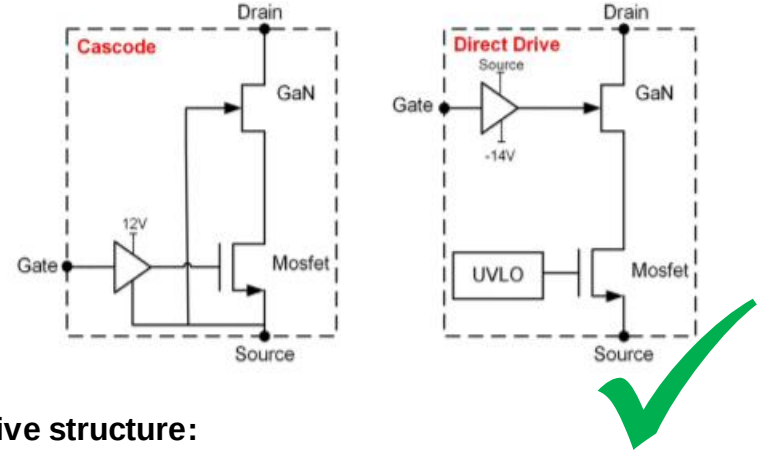


- Integrating the driver eliminates common-source inductance and significantly reduces the inductance the driver output and GaN FET

Application Note: Optimizing GaN performance with an integrated driver

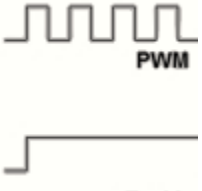
What's GaN direct-drive structure?

Cascode: Gate of GaN connected to Source of MOSFET; MOSFET Gate driven by gate driver



Direct Drive: Gate of GaN driven directly by gate driver; MOSFET is always On when VDD > UVLO

Direct Drive Approach



GaN FET is driven directly

Silicon FET is used as an "enable" switch

- **Advantages of direct-drive structure:**
- Zero reverse recovery (Qrr = 0 nC)
- Low gate charge of GaN
- No LV MOSFET switching loss
- Integrated gate driver can be engineered with programmable dv/dt (EMI vs efficiency)
- MOSFET is a current sensor, can be used for overcurrent protection

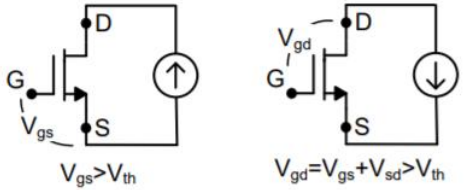
- **Application Note:** Direct-drive configuration for GaN devices (Rev. A)

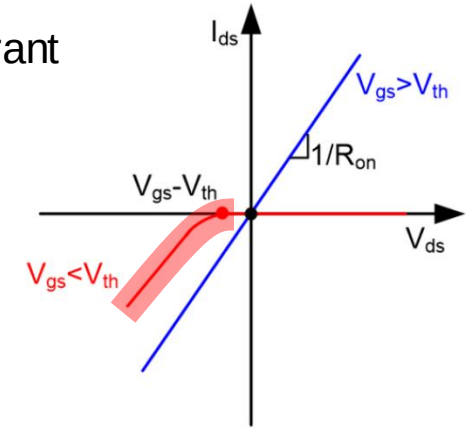
Does GaN have a body diode?

Understanding the third quadrant operation of GaN

- GaN FETs have **no body diode** yet capable of reverse conduction
- The symmetry of the device helps conduct in the third quadrant with diode-like behavior in OFF state
  - Unlike cascode, the silicon FET is always ON
  - No reverse recovery time and reverse recovery loss Qrr
- Reverse voltage drop starts ~5V with TI GaN

$$V_{sd} \approx (V_{th} - V_{gs}) + I_{sd}R_{on\_reverse}$$





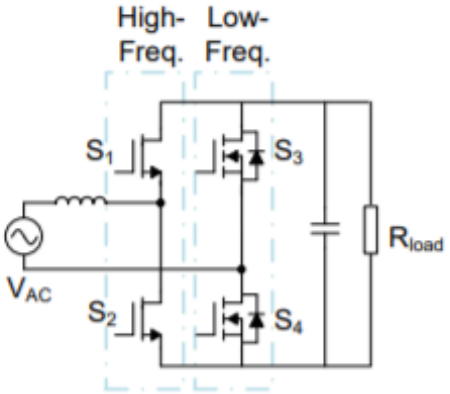
Simplified behavior of GaN in the first and third quadrants

Application Note: Does GaN Have a Body Diode? – Understanding the Third Quadrant Operation of GaN

Does GaN have a body diode?

Understanding the third quadrant operation of GaN

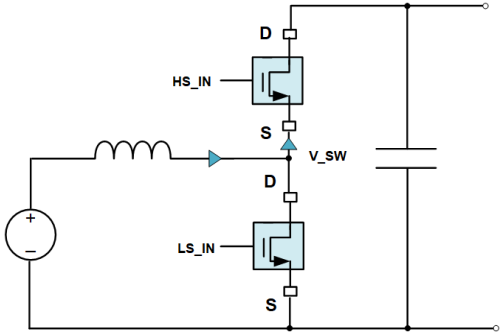
- It is recommended not to add an antiparallel diode with the GaN FET to conduct the reverse current
  - Adding an antiparallel diode adds output capacitance to the switch node and increases switching losses
- The third quadrant losses can be minimized by optimizing the dead time
  - Adaptive dead time by controller
  - Ideal Diode Mode with TI GaN



Totem-pole PFC with GaN for high-frequency FETs

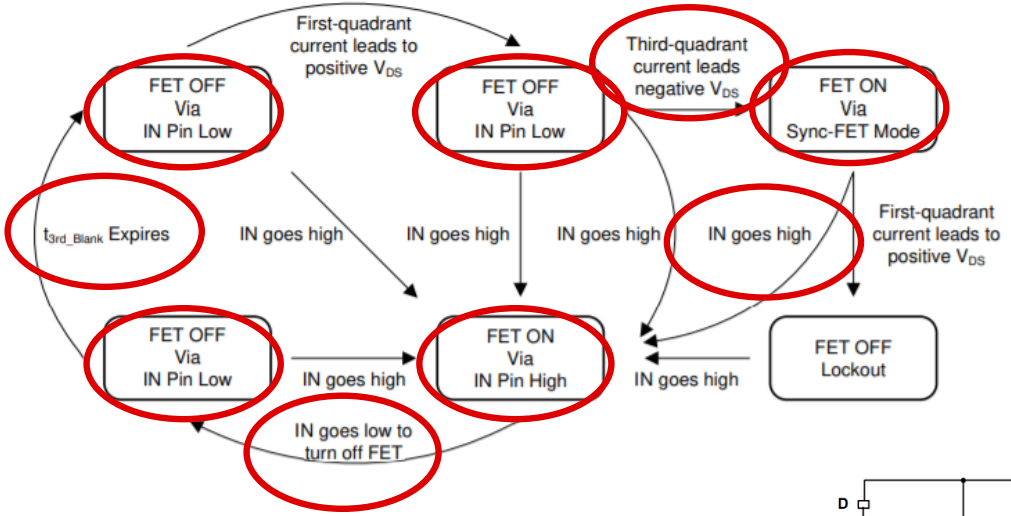
How to minimize GaN's 3rd quadrant conduction losses?

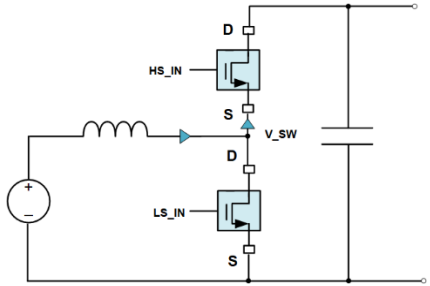
- **Ideal diode mode** is triggered by the detection of negative V_{DS} (±150mV) and when IN signal is low
- Once triggered the GaN FET is turned on within ~35ns
- A built-in blanking period is provided to prevent shoot-through
- Saves designer's effort to fine tune the dead time
- **Application Note:** Maximizing the Performance of GaN with Ideal Diode Mode



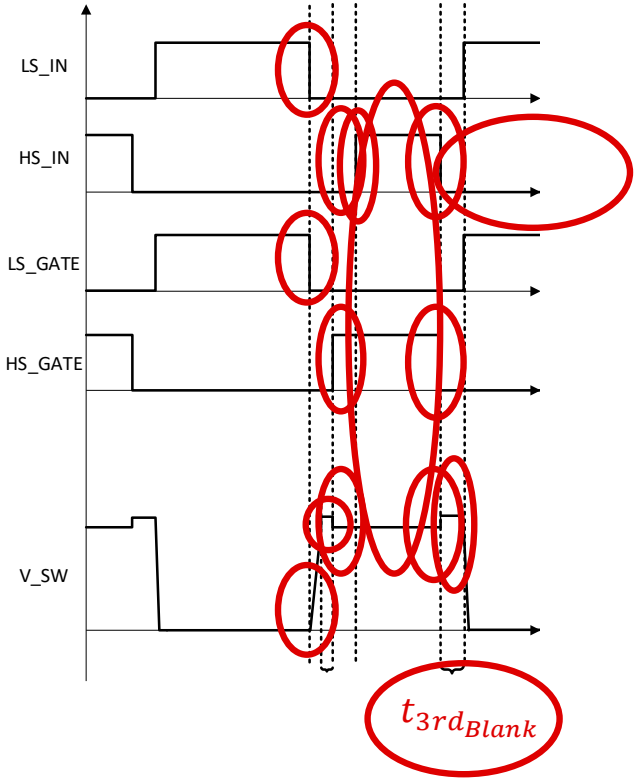
Boost Converter Example

How to minimize GaN's 3rd quadrant conduction losses?





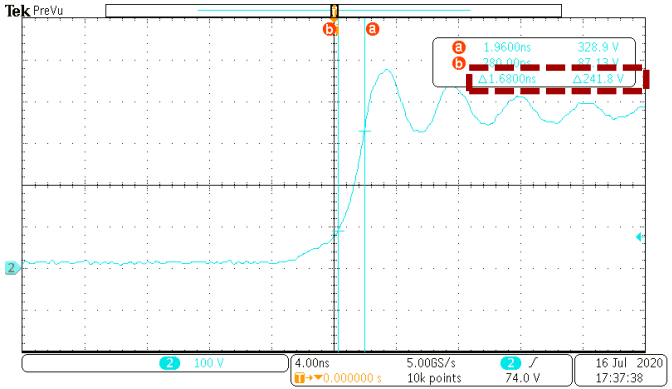
Boost Converter Example



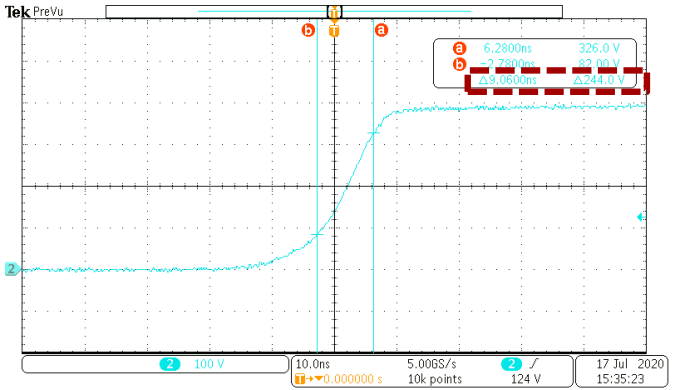
What are the integrated smart features for TI GaN?

- **Adjustable turn-on slew rate**
  - Helps to balance between the switching losses and ringing
  - Can be fine tuned for EMI

Buck converter switch node waveform:



150 V/ns



20 V/ns

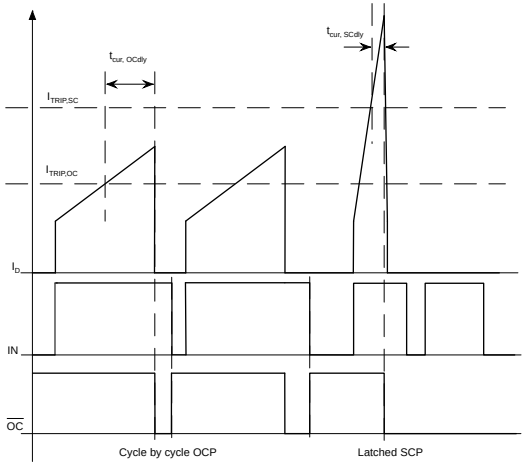
What are the integrated smart features for TI GaN?

- <100 ns **overcurrent protection** with zero external components
- Cycle-by-cycle feature allows system to ride through transients
- Abnormal short circuit conditions are latched off for system intervention
- dI/dt used to differentiate between CBC & SCP modes

	50 mΩ	30 mΩ	Action
Overcurrent Protection*	50A	70A	Cycle-by-cycle
Short-circuit Protection*	75A	95A	Latched-off

* Typical Values

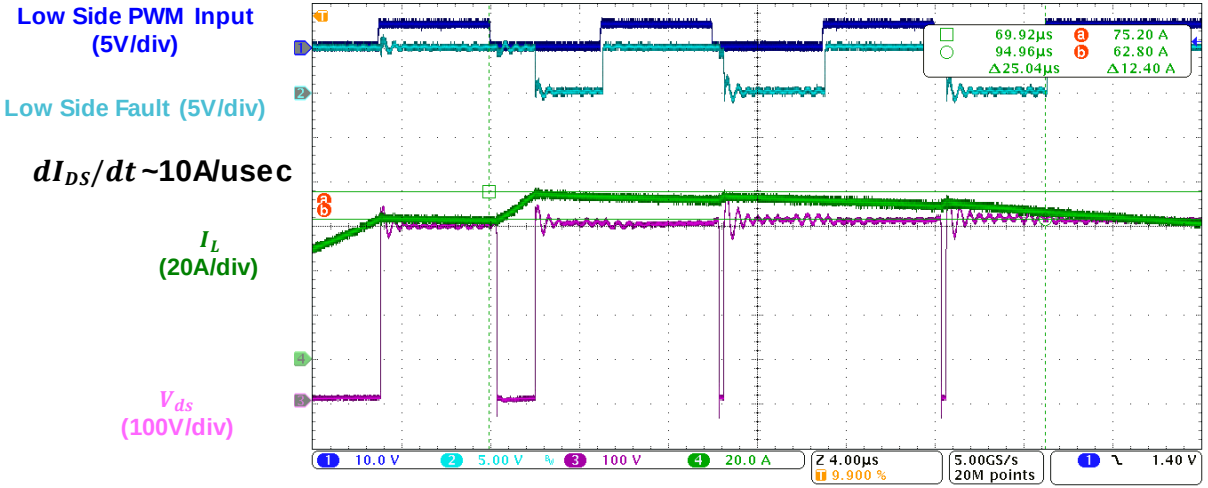
[schedule, specs, features & pinouts subject to change without prior notice.]



Overcurrent detection vs. Short-circuit detection

What are the integrated smart features for TI GaN?

- **Cycle-by-cycle overcurrent protection (OCP)**
- Boost converter configuration, and the current builds up when the low-side device in on
- When current builds up to ~75 A, a cycle-by-cycle OCP is triggered. The fault is reset in each switching cycle.



What are the integrated smart features for TI GaN?

- **Latched short-current protection (SCP)**
- The high-side device is shorted to the high voltage bus. A short circuit is induced when the low-side device is turned on, and the current increases quickly
- A short circuit event is detected at “cursor A”, and Soft turn-off action is taken within 78 ns (“cursor B”)

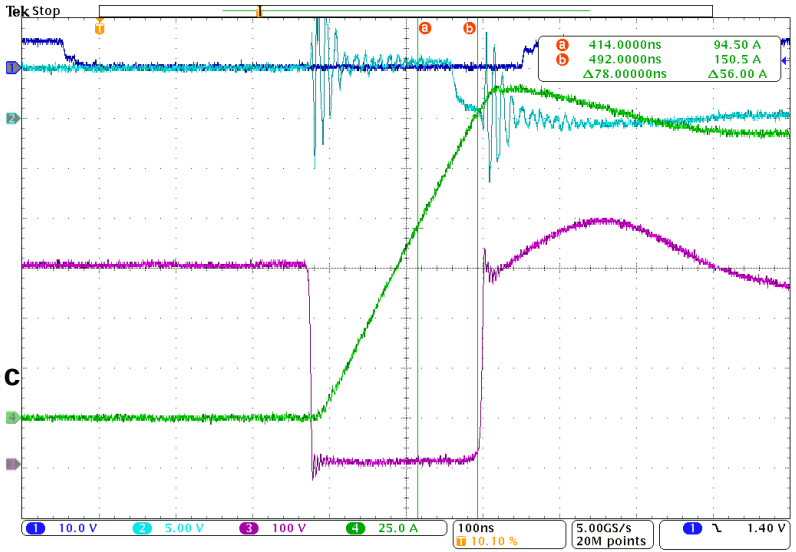
Inverse of Low Side PWM Input (5V/div)

Low Side Fault (5V/div)

dI_{DS}/dt ~718A/usec

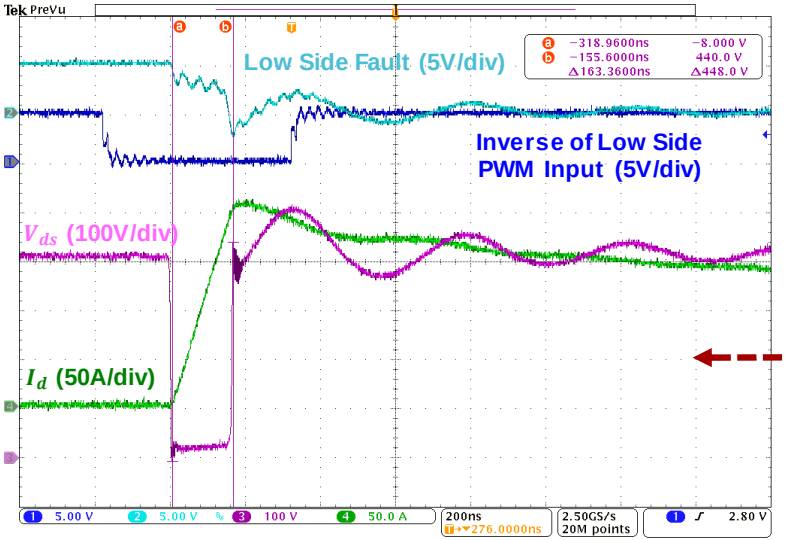
I_L (20A/div)

V_{ds} (100V/div)

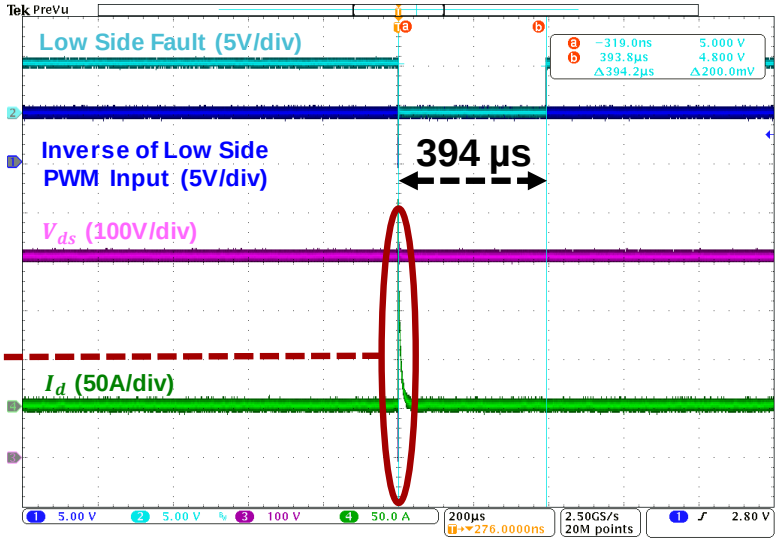


What are the integrated smart features for TI GaN?

- The latched fault can be reset by keeping the **IN pin low** for >350 µs.
- This multi-use of IN pin helps to save isolation channels, and two-channel (one input for IN and one output for Fault) isolators like ISO7721 can be used for cost reduction.



Zoom-in of short-circuit protection



Fault Reset

What are the integrated smart features for TI GaN?

- Digital TEMP feature eliminates the need for external temperature sensors and provides ±3ºC accuracy

- Digital fault outputs provide a simple interface to the host controller

	Normal operation	UVLO or Over-temperature	Overcurrent	Short-circuit
FAULT pin	High	Low	High	Low
OC pin	High	High	Low	Low

[schedule, specs, features & pinouts subject to change without prior notice.]

What are GaN FET package variants and cooling strategies?

Gen-I (LMLG341x)

50mΩ 2.1kW
LMG341xR050

70mΩ 1kW
LMG341xR070

150mΩ <1kW
LMG341xR150

8x8 mm

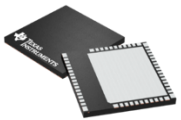
6 devices in mass production

2x the power

Gen-II (LMG342x, 600V)

30mΩ - 4kW
LMG342xR030

50mΩ- 3kW
LMG32xR050



12x12 mm bottom-side cooled

Samples: Available Now
https://www.ti.com/product/LMG3422R030

AECQ-100

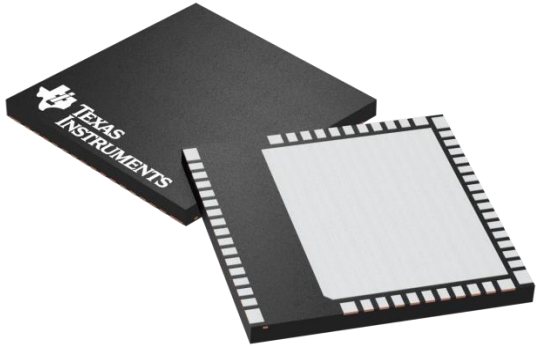
Gen-II Automotive (LMG352x, 650V)

30mΩ - 6kw
LMG352xR030-Q1

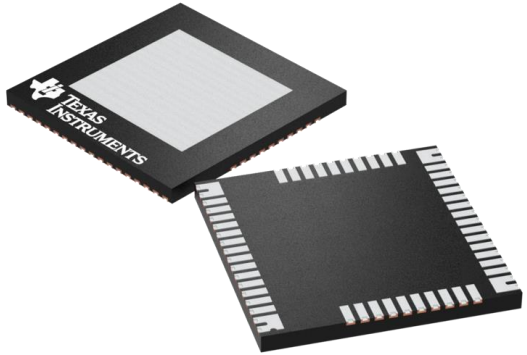
Samples: Available Now
https://www.ti.com/product/LMG3522R030-Q1

12x12 mm top-side cooled

Top vs. bottom-side cooled package

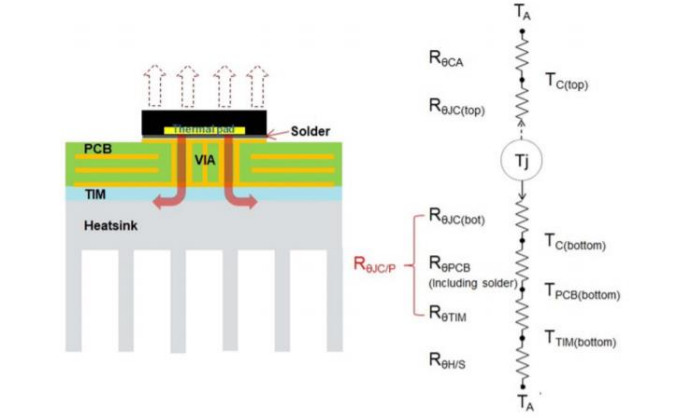


Package type	QFN
Package size (X/Y/Z)	12mm/12mm/0.9mm
Exposed thermal Pad	Bottom side (Connected to Source)
Exposed pad size (mm^2)	79
Minimum creepage (mm)	2.75

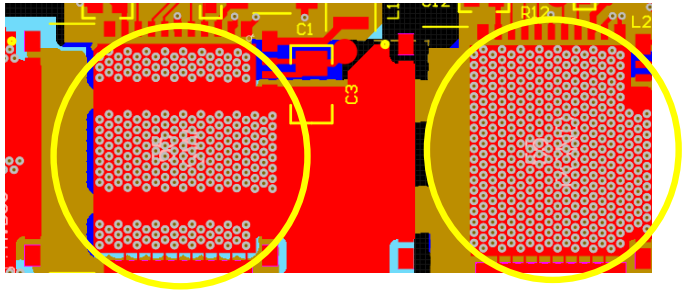


Package Type	QFN with wettable flanks
Package Size (X/Y/Z)	12mm/12mm/0.9mm
Exposed Pad Direction	Top side (Connected to Source)
Exposed Pad Size (mm^2)	63
Minimum Creepage (mm)	2.75mm (bottom)

Bottom-side cooled device



Bottom-side cooled device with heatsink

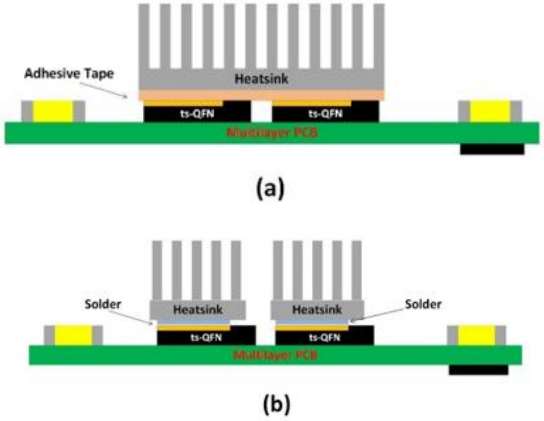


Thermal Vias for heat dissipation through PCB

- Thermal pad on the bottom of the device
- Heat dissipated through thermal vias on PCB
- Thermal interface material (TIM) example: GR80A
- Example calculation:
  - 55°C ambient
  - 125°C max junction temperature
  - 4°C/W junction to ambient thermal impedance (1.8°C/W for heatsink)
  - Allowed loss: $P = \frac{125-55}{4} = 17.5W$

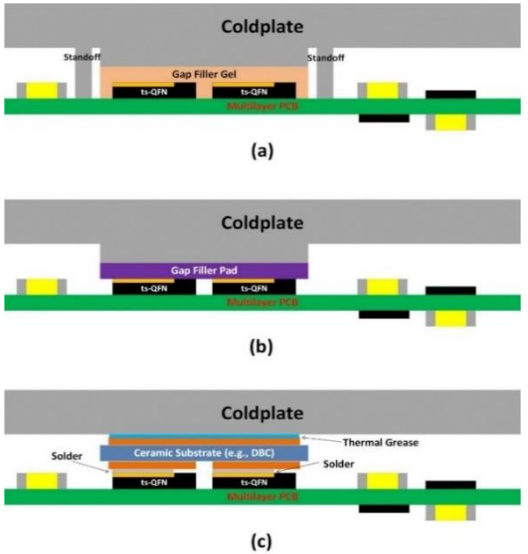
- **Application Note:** Thermal Performance of QFN12x12 Package for 600V, GaN Power Stage

Top-side cooled device



Top-side cooled device with heatsink

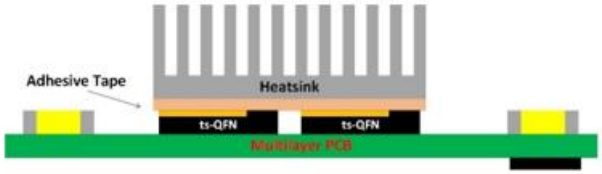
- Thermal pad on top side of the device
- For thermal design with **heatsink**
  - One heatsink cover multiple devices with TIM
  - Individual heatsink with solder

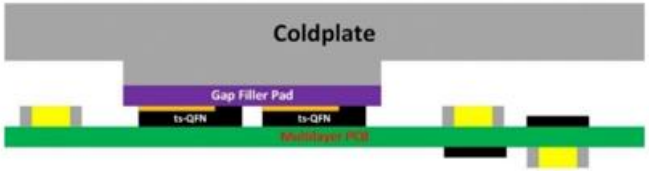


Top-side cooled device with coldplate

- For thermal design with **coldplate**
  - Gap filler gel
  - Gap filler pad
  - Ceramic substrate with thermal grease

Top-side cooled device





- Top-side cooling device with **heatsink**:
  - 55°C ambient
  - 125°C max junction temperature
  - 3.2°C/W junction to heatsink thermal impedance
  - Allowed loss: $P = \frac{125-55}{3.2} = 21.9W$

- Top-side cooling device with **coldplate**:
  - 55°C ambient
  - 125°C max junction temperature
  - 2°C/W junction to coldplate thermal impedance
  - Allowed loss: $P = \frac{125-55}{2} = 35W$

Examples of thermal interface materials (TIM)
Thermal pad TIM example: GR80A Link
Gel TIM example: TIA282GF Link

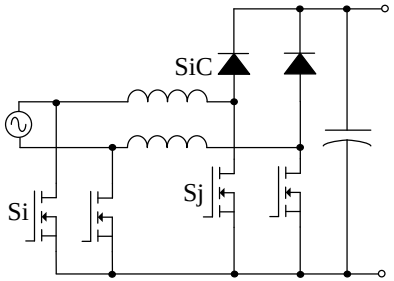
Thermal interface material for coldplate

	Advantage	Disadvantage
Gap filler gel	• Minimal normal stress applied on the package and solder joints • Excellent conformability and good tolerance in component height variance and surface planarity	• Need customized coldplate • Relative high thermal impedance
Gap filler pad	• Lower thermal impedance compared to gel	• Pressure applied on package/solder joints
Ceramic substrate with thermal grease	• The best thermal performance • Best isolation property	• Pressure applied on package/solder joints • Higher cost

How can GaN reduce overall system cost?

- GaN is a new topology enabler – totem-pole PFC

Dual-boost PFC



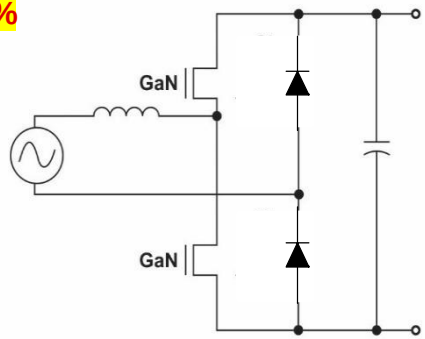
Components	Quantity
SJ MOSFETs IPW60R037P7	2
SiC Diodes C3D16060D	2
Diode Bridges GBJ25V08	2
Gate Drivers UCC27511DBV	2
Inductors	2

Efficiency

98.0% → 98.8%

Power stage cost parity with super junction MOSFET

Totem-pole PFC

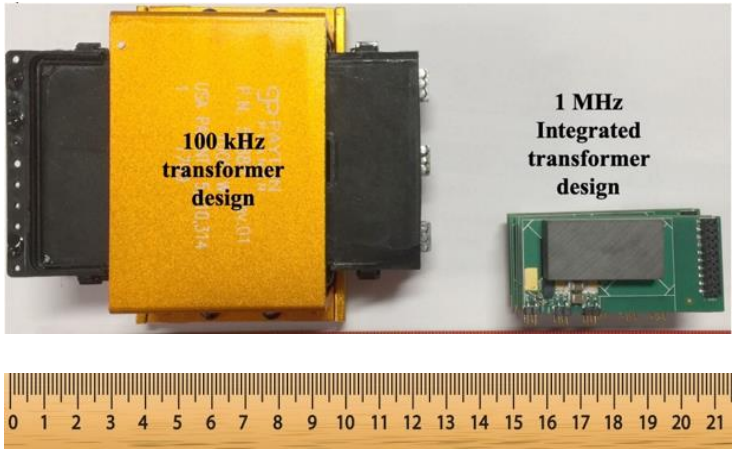


Components	Quantity Estimated Cost
GaN FETs LMG3422R030	2
Diode Bridges GBJ25V08	2
HS isolator ISO6721QDR	2
Inductor	1

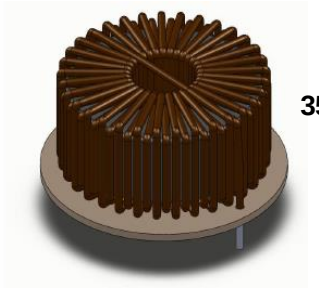
- SJ Mosfet has large reverse recovery loss
  - Shoot-through risk due to insufficient dead time
- GaN FET with 0 Qrr is ideal for totem-pole PFC

How can GaN reduce overall system cost?

- GaN reduces system-level cost by going to higher switching frequency
- Reduced size and cost of magnetics



40-kHz CCM PFC inductor (1000 W)



35mm

63mm

Inductor volume 138915mm^3

3.2x reduction in inductor volume

Reduced cost

100-kHz CCM PFC inductor (1000 W)

23.24mm

Inductor volume 43952mm^3

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