Enhancing Resolution and Reducing System Size in High-Speed Video Applications

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This white paper introduces you to a modern solution to these problems: V3Link™ SerDes pairs.

At a glance

1 **The current state of high-resolution imaging**

High-resolution imagers are more accessible than ever on the market. But can data bridges keep up with the issues that come with higher bandwidths?

2 **What are V3Link SerDes?**

V3Link SerDes provide a single-wire, two-chip solution for connecting imagers to processors. This section details how, and what that means for you.

3 **V3Link features**

V3Link SerDes include many added features that enable live data control, adaptive signal compensation, synchronized video, and more.

Increasing the resolution of an imager in a system increases the amount of data it generates -- data that must be transmitted, processed and stored. Many designers place imagers in remote locations that are physically separate from the main processing board. Unfortunately, connecting an imager over a small-diameter wire or cable adds signal interference and other issues that surpass the limits of the transmission channels of existing bridge technologies. You may be in this predicament now -- wanting to use a high-resolution camera (or multiple!) but realizing that implementation with chipsets such as USB and Ethernet would require using too many large chips and cables and too much design effort to maintain good signal integrity over the lifespan of the device. This white paper introduces you to a modern solution to these problems: V3Link™ SerDes pairs.

The current state of high-resolution imaging

To better understand the design challenges, the conversation to imagers needs to be narrowed, keeping in mind that the discussion is still relevant for other sensor types. Imagers are readily available in many sizes, resolutions and price points. To meet the demands for more and better vision in many technologies such as autonomous robotics, medical imaging, wearables and white goods, designers are taking advantage of the increased availability of higher-resolution imagers as they become more cost-effective and easier to find in standard interfaces such as Camera Serial Interface (CSI)-2. “Higher resolution” is very subjective, but for the purposes of this paper, let’s classify it as resolutions from 1 MP to over 8 MP, or 720p to over 4K.

For example, a 4-MP imager operating at 30 fps generates roughly 3.2 Gbps of video data that needs to move from a remote image module to a processor. To connect both ends, you need an integrated circuit (IC) pair to form a bridge that can carry the entire 3.2 Gbps of video data across the cable from the imager’s interface to the processor’s interface. In addition, the bridge may need to carry power, clock and peripheral control data in the opposite direction from processor to imager.

Cables introduce fundamental issues to the link, however; electromagnetic interference (EMI), loss and latency can compromise link integrity and lead to timing variances. This is where many bridge ICs reach their limits as resolutions increase. A bridge must transmit all of the video and peripheral data across the cable distance with high signal integrity, and without compromising system size and cost.

Before choosing a specific bridge IC, you need to consider whether you are going to need to send the data compressed or uncompressed, since the architecture is so different between the two.

Compression technologies generally use transmitter and receiver physical layers to transmit data across the line to the processing unit. Compression requires additional components within the imager module, including a processing element to perform the compression, a crystal oscillator for clocking, and an interface converter. These components produce delays in the data path that add latency to the link and can affect time-sensitive applications such as factory automation, machine vision or medical vision.

For that 4-MP imager running at 30 fps and generating about 3.2 Gbps of video data, a single Gigabit-based Ethernet link such as 1000BASE-T does not have sufficient bandwidth to carry this amount of high-resolution data without compression.

On the other hand, uncompressed interface technology such as a serializer/deserializer (SerDes) pair can transmit raw, uncompressed data directly between the imager interface and the processor interface, eliminating the need for algorithms to compress and decompress data.

A SerDes traditionally transfers video over short distances across a printed circuit board trace or flex cable. As seen in **Figure 1**, modern solutions such as the high-speed V3Link SerDesfrom Texas Instruments (TI) improve on basic SerDes technology while requiring fewer system components and overheads than compressed technologies. With good signal integrity and many other added features, V3Link pairs can bridge longer-distance connections from less than a meter to over 14m using a single wire or cable.

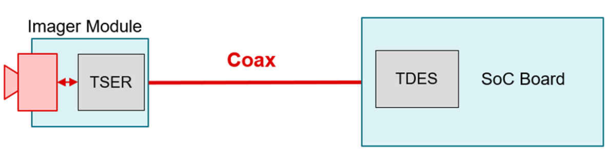

Figure 1. *Transporting video over fewer cables without compression using V3Link SerDes devices.*

What are V3Link SerDes?

V3Link SerDes are ultra-low-latency SerDes that aggregates video, clock, control and general-purpose input/output data into a single-wire bidirectional bridge between industry-standard interfaces. You can leverage V3Link bridge pairs to support increased resolution, reduce system size, extend cable reach and strengthen signal integrity.

There are two components to basic V3Link SerDes links: the serializer and the deserializer. The serializer takes in raw video and peripheral data, aggregates and serializes it, and sends it across to the deserializer at multigigabit-per-second speeds. The deserializer deserializes that data back into the original raw data and provides that raw data to the processor.

Simultaneously, the deserializer communicates data in the opposite direction across the same wire to the serializer. This results in a high-speed bidirectional bridge for systems needing to transmit data in real time, with minimal cabling between the remote module and the processor.

Figure 2 illustrates the high-level data flow between sensor and serializer, across the cable, and between deserializer and SoC.

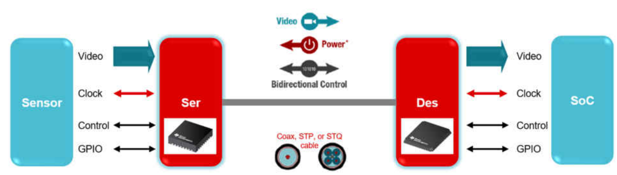

Figure 2. *Interfaces and data channels of V3Link devices.*

V3Link chipsets also support a range of cables and connectors, including coaxial, twisted pair and shielded twisted pair. In terms of imager support, they are compatible with interfaces such as CSI-2 that are common in various types of sensor modules and processors. The resolution and configuration of the imager are very flexible: V3Link only cares about the total video data rate, and as long as you stay within that rate, you are good to go.

To give an example in more detail, TI's TSER953 serializer (which comes in a small 5 mm x5 mm VQFN package) supports 3.3 Gbps of video data on the line. The following equation estimates the video data rate of an imager:

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Video data rate (bps) = resolution
(horizontal × vertical) × frame rate (fps)
× color depth (bpp)
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Just as a 4-MP imager running at 30 fps generates approximately 3.2 Gbps of video data, a 1-MP imager running at 120 fps generates approximately 2.36 Gbps of video data, and an 8-MP imager running at 30 fps generates approximately 3.11 Gbps of video data. These rates are all below 3.3 Gbps, so the TSER953 coupled with a compatible deserializer can support all three imagers (and more).

Imagers and cables are available in various sizes to help meet the space and cost considerations of space-constrained systems. However, small-sized solutions can introduce fundamental system challenges in areas such as heat dissipation. V3Link provides a thermal-friendly solution for small modules. The TSER953, which sits on the sensor side, has approximately 0.25 W power consumption and approximately 250 mW of power-dissipation capability, reducing the need for additional power and heat dissipation modules such as fans or coolers. Additionally, V3Link SerDes pairs aggregate video, clock, peripheral data and power over a single wire or cable, which helps minimize the number of chips and cables in the system.

V3Link features

The thinner a cable is, the more likely that cable loss and interference could be introduced to the data channel. V3Link SerDes provides signal conditioning, EMI reduction and an integrated feature called adaptive equalization to support high signal integrity across the cable. Adaptive equalization automatically compensates for any factors that would compromise signal integrity – different cable sizes, aging cables and connectors, and variances in voltage levels and temperatures across the line – by boosting the signal strength as needed. In total, adaptive equalization can compensate for losses of as much as 21 dB at 2.1 GHz, enabling the use of cables as small as 28 to 32 American Wire Gauge (AWG).

So what about managing more than one imager to get a wider field of view? In machine vision, autonomous robotics, and surveillance, synchronized multidimensional vision capture is important for asset tracking across multiple cameras. Increasing field of view and resolution comes with the trade-off of more complex system architectures, since each sensor added to a design generally requires an additional wire and connector to the main processing board. As seen in **Figure 3**, deserializer hubs such as TI's TDES960 counter extra design efforts by enabling multiple imager feeds to aggregate to a single deserializer chip, reducing the total number of chips required in the system.

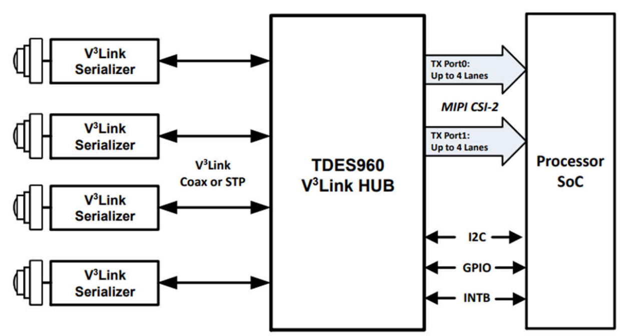

Figure 3. *Hub deserializers synchronize modular cameras without sacrificing board space.*

The incoming camera feeds need to synchronize in order for the processor to use the data immediately. Additionally, peripherals on the sensor module need to synchronize to the frame rate of the video capture. For example, if the sensor is using an LED for lighting, that LED needs to flash in time with the frame capture in order to avoid lighting errors in the video.

The embedded clock that V3Link transfers on the line is actually an embedded grandmaster synchronous clock supplied by the deserializer hub, meaning that the deserializer supplies the exact same synchronized clock to all connected serializers (and by extension, all connected sensor modules) with 600-ns accuracy. This synchronization enables video stitching, image blending and stereovision for 3D reconstruction and depth sensing without errors caused by timing variances. Additionally, reference clock extraction from the reverse channel eliminates synchronization errors caused by the relative drift of different oscillators clocking multiple imagers.

Conclusion

The key to a successful high-speed image sensor or display link is a resilient transmission channel that can transport the entire data bandwidth (including video, clock and peripheral control information) without taking up too much physical footprint on the board – and in a power-efficient manner. Video links leveraging V3Link SerDes help eliminate the many struggles that come with high-resolution imagers and displays. Consumers will be able to leverage the full resolution of video for smooth, seamless viewing or machine interpretation.

References

- Watch the TI video, **What are V3Link SerDes**?
- Watch the TI New Product Update, **TI New Product Update: V3Link Industrial SerDes**.
- Read the technical article, **How to Transfer High-Resolution Video Data Over a Single Wire in Machine-Vision Applications**.