

LMC555 CMOS Timer

1 Features

- Fast astable frequency of 3MHz
- Available in industry's smallest 8-bump DSBGA package (1.43mm × 1.41mm)
- Less than 1mW typical power dissipation at 5V supply
- 1.5V specified supply operating voltage
- output fully compatible with TTL and CMOS logic at 5V supply
- Tested to -10mA, 50mA output current levels
- Reduced supply current spikes during output transitions
- Extremely low reset, trigger, and threshold currents
- Excellent temperature stability
- Pin-for-pin compatible with 555 series of timers

2 Applications

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generators

3 Description

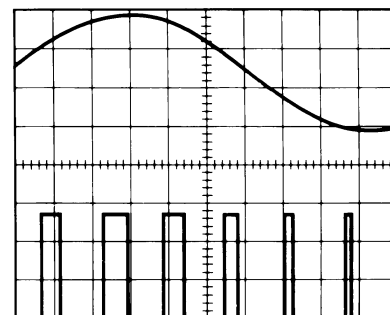
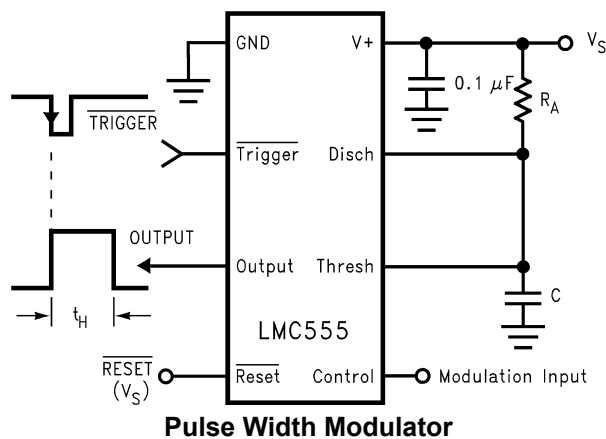
The LMC555 device is a CMOS version of the industry standard 555 series general-purpose timers. In addition to the standard SOIC, VSSOP, and PDIP packages, the LMC555 is also available in a chip-sized, 8-bump DSBGA package using TI's DSBGA package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555, but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In astable mode, the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. TI's LCMOS process extends both the frequency range and the low supply capability.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
LMC555	D (SOIC, 8)	4.9mm × 6mm
	DGK (VSSOP, 8)	3mm × 4.9mm
	P (PDIP, 8)	9.81mm × 9.43mm
	YBF (DSBGA, 8)	1.75mm × 1.75mm

(1) For more information, see [Section 11](#).

(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Pulse Width Modulator Waveform:
 Top Waveform—Modulation
 Bottom Waveform—Output Voltage



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4 Pin Configuration and Functions

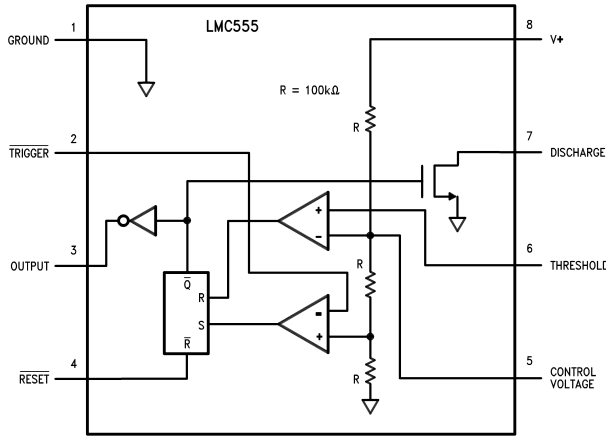


Figure 4-1. D Package, 8-Pin SOIC, DGK Package, 8-Pin VSSOP, and P Package, 8-Pin PDIP (Top View)

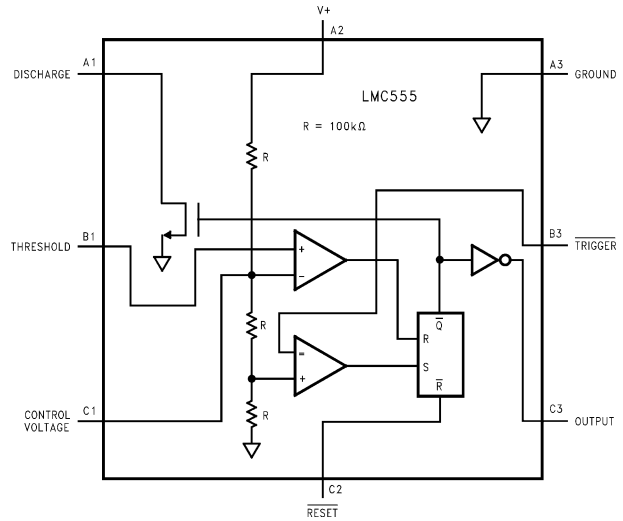


Figure 4-2. YPB Package, 8-Pin DSBGA (Top View)

Table 4-1. Pin Functions

NAME	PIN NO.		TYPE	DESCRIPTION
	D (SOIC), DGK (VSSOP), P (PDIP)	YPB (DSBGA)		
CONTROL VOLTAGE	5	C1	Input	Control voltage controls the threshold and trigger levels. This pin determines the pulse duration of the output waveform. An external voltage applied to this pin can also be used to modulate the output waveform.
DISCHARGE	7	A1	Input	Open collector output that discharges a capacitor between intervals (in phase with output). This pin toggles the output from high to low when voltage reaches 2/3 of the supply voltage (V+).
GROUND	1	A3	Power	Ground reference voltage
OUTPUT	3	C3	Output	Output driven waveform
RESET	4	C2	Input	Negative pulse applied to this pin to disable or reset the timer. When not used for reset purposes, connect this pin to V+ to avoid false triggering.
THRESHOLD	6	B1	Input	Compares the voltage applied to the pin with a reference voltage of 2/3 V+. The amplitude of voltage applied to this pin is responsible for the set state of the flip-flop.
TRIGGER	2	B3	Input	Responsible for transition of the flip-flop from set to reset. The output of the timer depends on the amplitude of the external trigger pulse applied to this pin.
V+	8	A2	Power	Supply voltage with respect to ground

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted.^{(1) (2) (3)}

		MIN	MAX	UNIT
Voltage	Supply		15	V
	Input	-0.3	(V+) + 0.3	
	Output		15	
Current	Output		100	mA
Storage temperature, T _{stg}		-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) See AN-1112 ([SNVA009](#)) for DSBGA considerations.
- (3) If military- or aerospace-specified devices are required, contact the TI Sales Office or Distributors for availability and specifications.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±1500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Temperature	LMC555IM	-40		125	°C
	LMC555CM, MM, N, TP	-40		85	
Maximum allowable power dissipation at 25°C	PDIP-8			1126	mW
	SOIC-8			740	
	VSSOP-8			555	
	8-bump DSBGA			568	

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMC555				UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	YPB (DSBGA)	
		8 PINS	8 PINS	8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	138.9	188.3	93.1	102.3	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	78.8	78.8	82.5	0.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	87.9	110.2	69.6	31.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	23.2	18.5	52.0	0.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	86.9	108.6	69.2	31.2	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	°C/W

- (1) For information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.5 Electrical Characteristics

Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted⁽¹⁾

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Supply current	$V_S = 1.5\text{ V}$		130	200	μA
		$V_S = 5\text{ V}$		180	250	
		$V_S = 12\text{ V}$		220	400	
V_{CTRL}	Control voltage	$V_S = 1.5\text{ V}$	0.8	1.0	1.2	V
		$V_S = 5\text{ V}$	2.9	3.3	3.8	
		$V_S = 12\text{ V}$	7.4	8.0	8.6	
V_{DIS}	Discharge saturation voltage	$V_S = 1.5\text{ V}, I_{\text{DIS}} = 1\text{ mA}$		75	150	mV
		$V_S = 5\text{ V}, I_{\text{DIS}} = 10\text{ mA}$		150	300	
V_{OL}	Output voltage (low)	$V_S = 1.5\text{ V}, I_O = 1\text{ mA}$		0.2	0.4	V
		$V_S = 5\text{ V}, I_O = 8\text{ mA}$		0.3	0.6	
		$V_S = 12\text{ V}, I_O = 50\text{ mA}$		1.0	2.0	
V_{OH}	Output voltage (high)	$V_S = 1.5\text{ V}, I_O = -0.25\text{ mA}$	1.0	1.25		V
		$V_S = 5\text{ V}, I_O = -2\text{ mA}$	4.4	4.7		
		$V_S = 12\text{ V}, I_O = -10\text{ mA}$	10.5	11.3		
V_{TRIG}	Trigger voltage	$V_S = 1.5\text{ V}$	0.4	0.5	0.6	V
		$V_S = 12\text{ V}$	3.7	4.0	4.3	
I_{TRIG}	Trigger current	$V_S = 5\text{ V}$		10		pA
V_{RES}	Reset voltage	$V_S = 1.5\text{ V}$ ⁽²⁾	0.4	0.7	1.0	V
		$V_S = 12\text{ V}$	0.4	0.75	1.1	
I_{RES}	Reset current	$V_S = 5\text{ V}, V_{\text{RES}} = V_S$		10		pA
		$V_S = 5\text{ V}, V_{\text{RES}} = 0\text{ V}$		5.9		μA
I_{THRESH}	Threshold current	$V_S = 5\text{ V}$		10		pA
I_{DIS}	Discharge leakage	$V_S = 12\text{ V}$		1.0	100	nA

- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) If the $\overline{\text{RESET}}$ pin is to be used at temperatures of -20°C and less, then ensure that V_S is 2.0 V or greater.

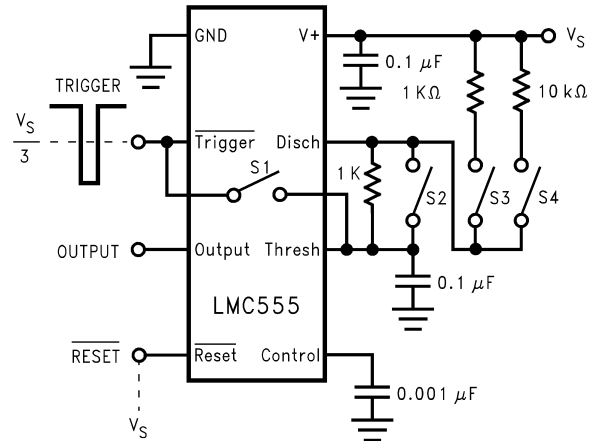
5.6 Switching Characteristics

Test Circuit, T = 25°C, all switches open, $\overline{\text{RESET}}$ to V_S unless otherwise noted.⁽¹⁾ Characteristic values are specified by design, characterization, or both.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t	Timing accuracy	SW 2, 4 closed	$V_S = 1.5\text{ V}$	0.9	1.1	1.25	ms
			$V_S = 5\text{ V}$	1.0	1.1	1.20	
			$V_S = 12\text{ V}$	1.0	1.1	1.25	
$\Delta t/\Delta V_S$	Timing shift with supply	$V_S = 5\text{ V} \pm 1\text{ V}$		0.3		%/V	
$\Delta t/\Delta T$	Timing shift with temperature	$V_S = 5\text{ V}$		75		ppm/ $^\circ\text{C}$	
f_A	Astable frequency	SW 1, 3 closed, $V_S = 12\text{ V}$	4.0	4.8	5.6	kHz	
f_{MAX}	Maximum frequency	Maximum frequency test circuit, $V_S = 5\text{ V}$		3.0		MHz	
t_R, t_F	Output rise and fall times	Maximum frequency test circuit $V_S = 5\text{ V}, C_L = 10\text{ pF}$		15		ns	
t_{PD}	Trigger propagation delay	$V_S = 5\text{ V}$, measure delay from trigger to output		100		ns	

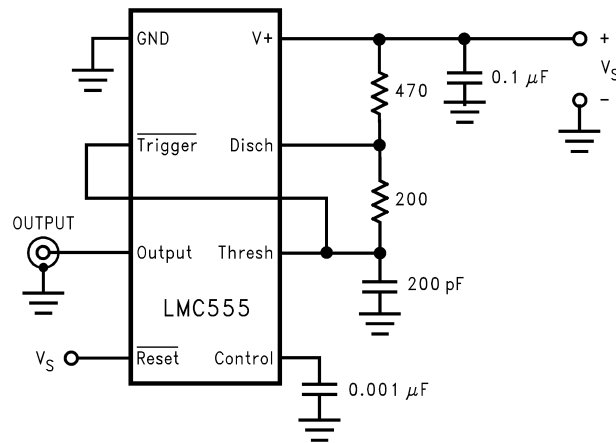
- (1) All voltages are measured with respect to the ground pin, unless otherwise specified.

6 Parameter Measurement Information



For device pinout, see [Section 4](#).

Figure 6-1. Test Circuit



For device pinout, see [Section 4](#).

Figure 6-2. Maximum Frequency Test Circuit

7 Detailed Description

7.1 Overview

The LMC555 is a CMOS version of the industry standard 555 series general-purpose timers. In addition to the standard SOIC, VSSOP, and PDIP packages, the LMC555 is also available in a chip-sized package (8-bump DSBGA) using TI's DSBGA package technology. The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation and supply current spikes. When operated as a one-shot, the time delay is precisely controlled by a single external resistor and capacitor. In the astable mode, the oscillation frequency and duty cycle are accurately set by two external resistors and one capacitor. The use of TI's LMC MOS process extends both the frequency range and the low supply capability.

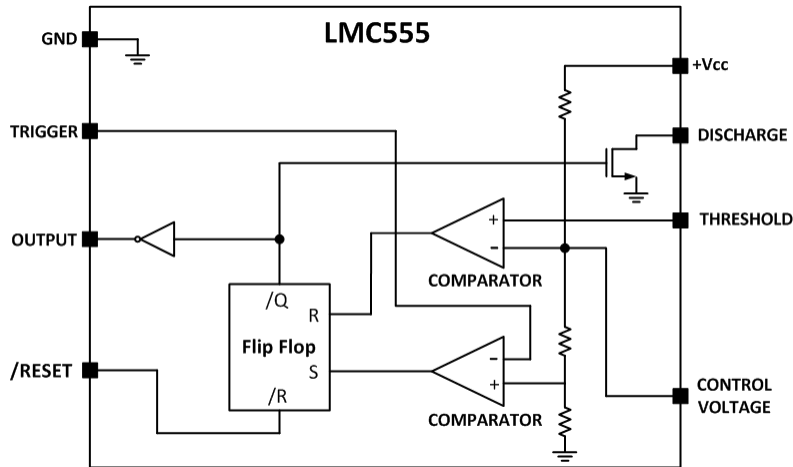
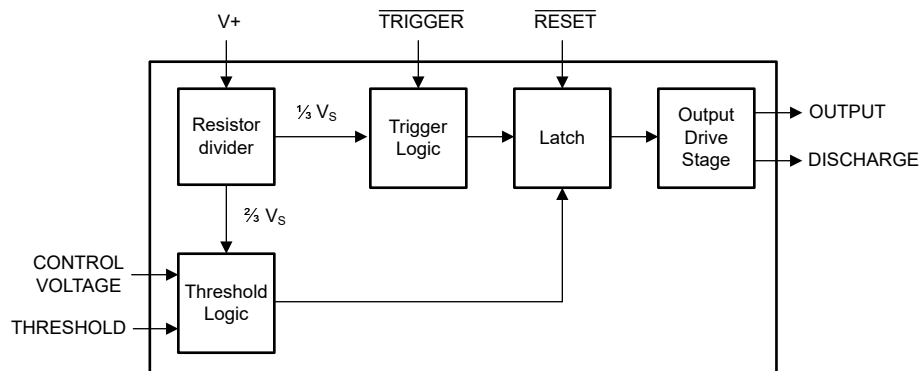


Figure 7-1. Simplified Schematic

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Low-Power Dissipation

The LMC555 offers the same capability of generating accurate time delays and frequencies as the LM555 but with much lower power dissipation. A power dissipation of less than 0.2 mW can be achieved with a 1.5-V operating supply voltage and less than 1 mW with a 5-V operating supply voltage. The use of TI's LCMOS process allows this low supply current and voltage capability. Reduced supply current spikes during output transitions and extremely low reset, trigger and threshold currents also provide low power dissipation advantages with the LMC555.

7.3.2 Various Packages and Compatibility

There are various packages available for use of the LMC555. In addition to the standard package (8-pin SOIC, VSSOP, and PDIP), the LMC555 is also available in a chip-sized package (8-bump DSBGA). The PDIP, SOIC, and VSSOP packages for the LMC555 are pin-for-pin compatible with the 555 series of timers (NE555/SE555/LM555) allowing flexibility in design and unnecessary modifications to PCB schematics and layouts.

7.3.3 Operates in Both Astable and Monostable Mode

The LMC555 can operate in both astable and monostable mode depending on the application requirements.

- Monostable mode: The LMC555 timer acts as a “one-shot” pulse generator. The pulse begins when the LMC555 timer receives a signal at the trigger input that falls below a 1/3 of the voltage supply. The width of the output pulse is determined by the time constant of an RC network. The output pulse ends when the voltage on the capacitor equals 2/3 of the supply voltage. The output pulse width can be extended or shortened depending on the application by adjusting the R and C values.
- Astable (free-running) mode: The LMC555 timer can operate as an oscillator and puts out a continuous stream of rectangular pulses having a specified frequency. The frequency of the pulse stream depends on the values of RA, RB, and C.

7.4 Device Functional Modes

7.4.1 Monostable Operation

In this mode of operation, the timer functions as a one-shot (Figure 7-2). The external capacitor is initially held discharged by internal circuitry. Upon application of a negative trigger pulse of less than $1/3 V_S$ to the $\overline{\text{TRIGGER}}$ pin, the flip-flop is set, which both releases the short circuit across the capacitor and drives the output high.

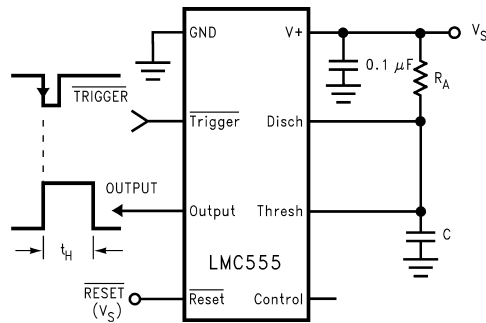
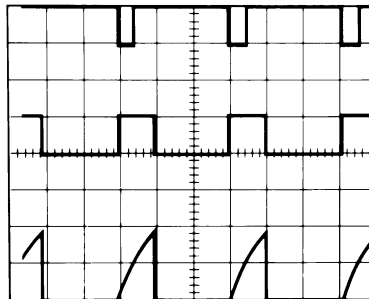


Figure 7-2. Monostable (One-Shot)

The voltage across the capacitor then increases exponentially for a period of $t_H = 1.1 R_A C$. This period is also the time that the output stays high, at the end of which time the voltage equals $2/3 V_S$. The comparator then resets the flip-flop, which in turn discharges the capacitor and drives the output to the low state. Figure 7-3 shows the waveforms generated in this mode of operation. Because the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing interval is independent of supply.



$V_S = 5 \text{ V}$

TIME = 0.1 ms/div

Top trace: Input 5 V/div

Middle trace: Output 5 V/div

Bottom trace: Capacitor voltage 2 V/div

$R_A = 9.1 \text{ k}\Omega$

$C = 0.01 \text{ }\mu\text{F}$

Figure 7-3. Monostable Waveforms

$\overline{\text{RESET}}$ overrides $\overline{\text{TRIGGER}}$, which can override $\overline{\text{THRESHOLD}}$. Therefore, ensure that the trigger pulse is shorter than the desired t_H . The minimum pulse duration for $\overline{\text{TRIGGER}}$ is 20 ns, and is 400 ns for $\overline{\text{RESET}}$. During the timing cycle when the output is high, the further application of a trigger pulse does not effect the circuit as long as the trigger input is returned high at least 10 μs before the end of the timing interval. However the circuit can be reset during this time by the application of a negative pulse to the $\overline{\text{RESET}}$ pin. The output remains in the low state until a trigger pulse is applied again.

When the reset function is not used, connect the $\overline{\text{RESET}}$ pin to V_+ to avoid any possibility of false triggering. Figure 7-4 is a nomograph for easy determination of RC values for various time delays.

Note

In monostable operation, drive the trigger high before the end of timing cycle.

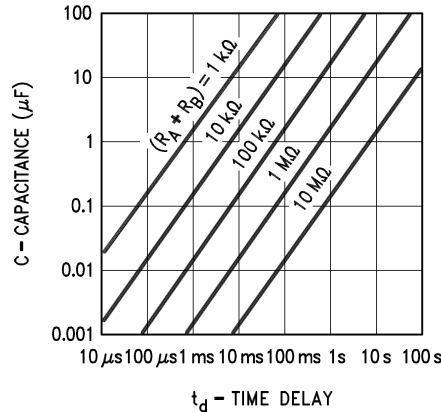


Figure 7-4. Time Delay

7.4.2 Astable Operation

If the circuit is connected as shown in Figure 7-5 ($\overline{\text{TRIGGER}}$ and $\overline{\text{THRESHOLD}}$ pins connected together), the circuit triggers and free runs as a multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B . Thus, the duty cycle can be precisely set by the ratio of these two resistors.

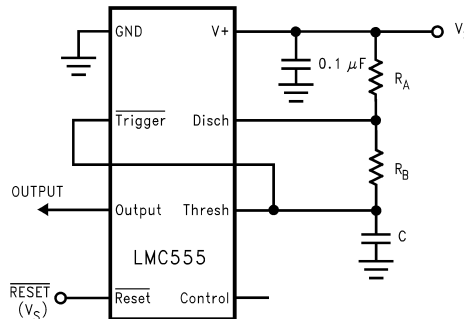
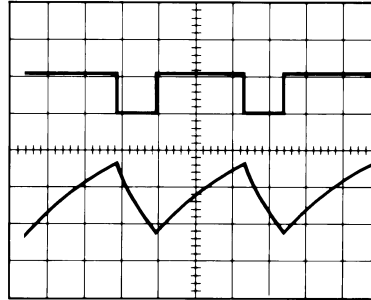


Figure 7-5. Astable (Variable Duty Cycle Oscillator)

In this mode of operation, the capacitor charges and discharges between $1/3 V_S$ and $2/3 V_S$. As in the triggered mode, the charge and discharge times, and therefore, the frequency are independent of the supply voltage.

Figure 7-6 shows the waveform generated in this mode of operation.



$$V_S = 5 \text{ V}$$

$$\text{TIME} = 20 \mu\text{s/div}$$

Top trace: Output 5 V/div

Bottom trace: Capacitor voltage 1 V/div

$$R_A = 1.78 \text{ k}\Omega$$

$$R_B = 4.12 \text{ k}\Omega$$

$$C = 0.01 \mu\text{F}$$

Figure 7-6. Astable Waveforms

The charge time (output high) is given by

$$t_1 = 0.693 (R_A + R_B)C \quad (1)$$

And the discharge time (output low) by:

$$t_2 = 0.693 (R_B)C \quad (2)$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693 (R_A + 2R_B)C \quad (3)$$

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)C} \quad (4)$$

Figure 7-7 can be used for quick determination of these RC Values. The duty cycle, as a fraction of total period that the output is low, is:

$$D = \frac{R_B}{R_A + 2R_B} \quad (5)$$

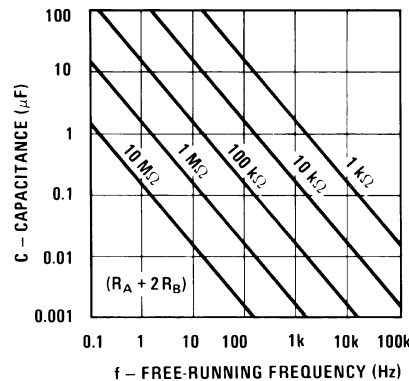


Figure 7-7. Free-Running Frequency

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The LMC555 timer can be used a various configurations, but the most commonly used configuration is in monostable mode. A typical application for the LMC555 timer in monostable mode is to turn on an LED for a specific time duration. A pushbutton is used as the trigger to output a high pulse when trigger pin is pulsed low. This simple application can be modified to fit any application requirement.

8.2 Typical Applications

8.2.1 Flash LED in Monostable Mode

Figure 8-1 shows the schematic of an LMC555 that flashes an LED in monostable mode.

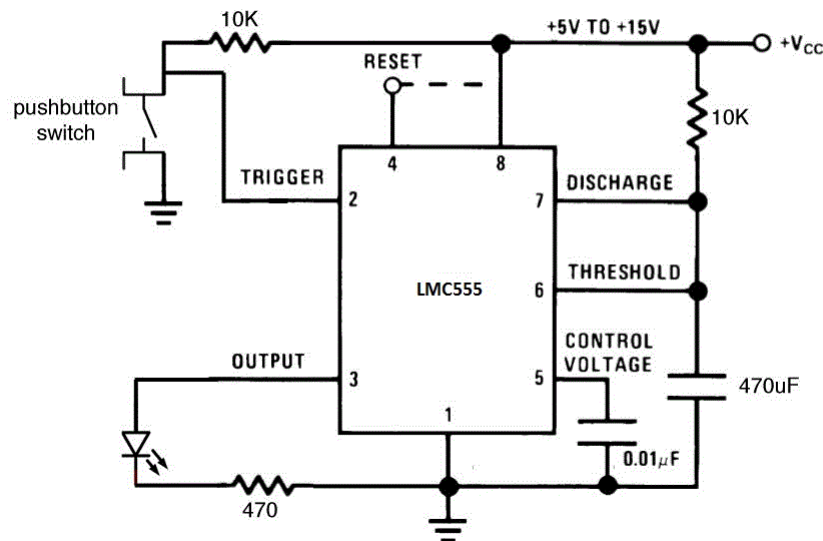


Figure 8-1. Schematic of Monostable Mode to Flash an LED

8.2.1.1 Design Requirements

The main design requirement for this application requires calculating the duration of time that the output stays high. The duration of time depends on the R and C values (shown in Figure 7-4) and is calculated by the following equation:

$$t = 1.1 \times R \times C \text{ seconds} \quad (6)$$

8.2.1.2 Detailed Design Procedure

To allow the LED to flash on for a noticeable amount of time, a 5-second time delay was chosen for this application. Using Equation 6, $R \times C$ equals 4.545.

If R is chosen as 100 k Ω , C = 45.4 μ F. The values of R = 100 k Ω and C = 47 μ F were chosen based on standard values of resistors and capacitors.

A momentary push button switch connected to ground is connected to the trigger input with a 10-k Ω current limiting resistor pull up to the supply voltage. When the push button is pressed, the $\overline{\text{TRIGGER}}$ pin goes to GND. An LED is connected to the OUTPUT pin with a current limiting resistor in series from the output of the LMC555 to GND. The $\overline{\text{RESET}}$ pin is not used and was connected to the supply voltage.

8.2.1.3 Application Curve

The data shown in Figure 8-2 were collected with the circuit used in the typical applications section. The LMC555 was configured in the monostable mode with a time delay of 5.17 s. The waveforms correspond to:

- Top Waveform (Blue) – Capacitor voltage
- Middle Waveform (Purple) – $\overline{\text{TRIGGER}}$
- Bottom Waveform (Green) – OUTPUT

As the $\overline{\text{TRIGGER}}$ pin pulses low, the capacitor voltage starts charging and the output goes high. The output goes low as soon as the capacitor voltage reaches 2/3 of the supply voltage, which is the time delay set by the R and C value. For this example, the time delay is 5.17 seconds.

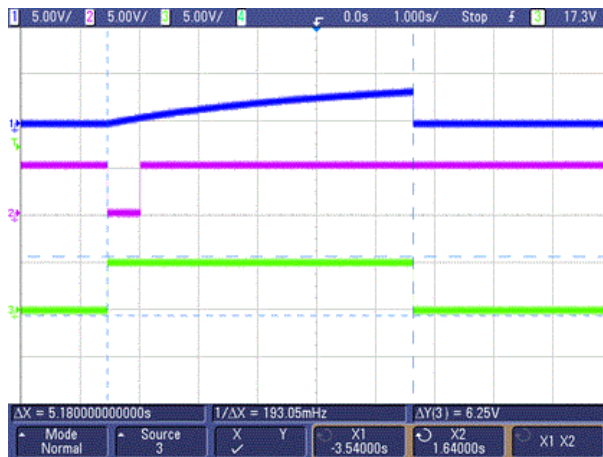


Figure 8-2. $\overline{\text{TRIGGER}}$, Capacitor Voltage, and OUTPUT Waveforms in Monostable Mode

8.2.2 Frequency Divider

The monostable circuit of Figure 8-3 can be used as a frequency divider by adjusting the length of the timing cycle. Figure 8-4 shows the waveforms generated in a divide by three circuit.

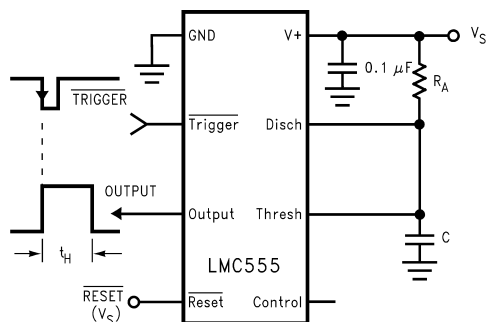


Figure 8-3. Monostable (One-Shot)

8.2.2.1 Design Requirements

Design a frequency divider by adjusting the length of the timing cycle.

8.2.2.2 Application Curve

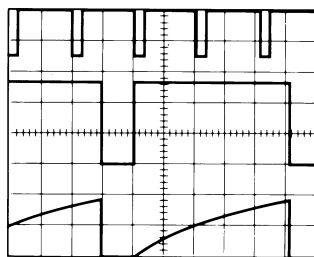


Figure 8-4. Frequency Divider Waveforms

8.2.3 Pulse Width Modulator

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to the control voltage terminal. Figure 8-5 shows the circuit, and in Figure 8-6 are some waveform examples.

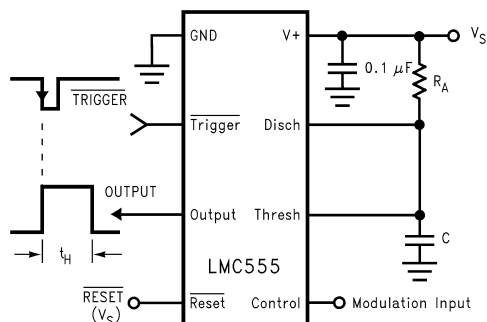


Figure 8-5. Pulse Width Modulator

8.2.3.1 Design Requirements

Modulator the output pulse width by the signal applied to the control voltage terminal.

8.2.3.2 Application Curve

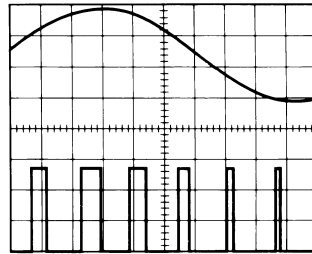


Figure 8-6. Pulse Width Modulator Waveforms

8.2.4 Pulse Position Modulator

This application uses the timer connected for astable operation, as in Figure 8-7, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 8-8 shows the waveforms generated for a triangle wave modulation signal.

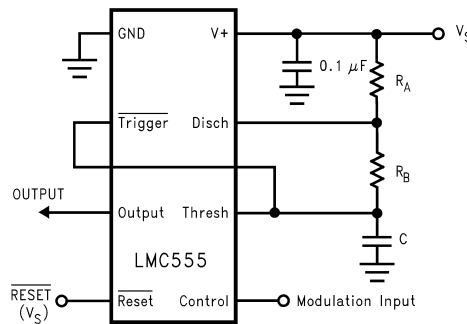


Figure 8-7. Pulse Position Modulator

8.2.4.1 Design Requirements

Using astable operation vary the pulse position with a modulating signal applied to the control voltage terminal.

8.2.4.2 Application Curve

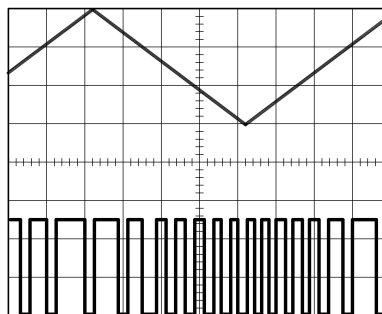


Figure 8-8. Pulse Position Modulator Waveforms

8.2.5 50% Duty Cycle Oscillator

The frequency of oscillation is:

$$f = 1/(1.4 R_C C)$$

(7)

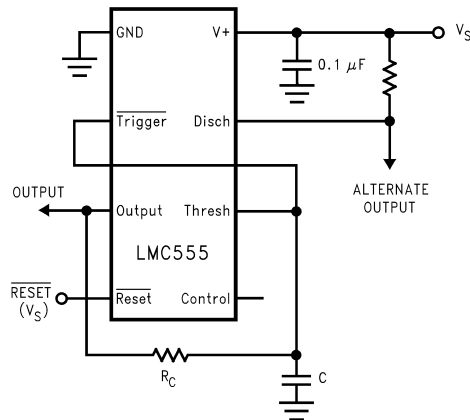


Figure 8-9. 50% Duty Cycle Oscillator

8.2.5.1 Design Requirements

An oscillator with a 50% duty cycle output.

8.3 Power Supply Recommendations

The LMC555 requires a voltage supply within 1.5 V to 15 V. Adequate power supply bypassing is necessary to protect associated circuitry; the minimum recommended is 0.1 μF in parallel with 1- μF electrolytic. Place the bypass capacitors as close as possible to the LMC555 and minimize the trace length.

8.4 Layout

8.4.1 Layout Guidelines

Standard PCB rules apply to routing the LMC555. Keep the 0.1 μF capacitor in parallel with a 1- μF electrolytic capacitor as close as possible to the LMC555. Place the capacitor used for the time delay as close as possible to the DISCHARGE pin. Use a ground plane on the bottom layer to provide better noise immunity and signal integrity.

8.4.2 Layout Example

The figure below is the basic layout for various applications.

- C1 – based on time delay calculations
- C2 – 0.01 μF bypass capacitor for control voltage pin
- C3 – 0.1 μF bypass ceramic capacitor
- C4 – 1- μF electrolytic bypass capacitor
- R1 – based on time delay calculations
- U1 – LMC555

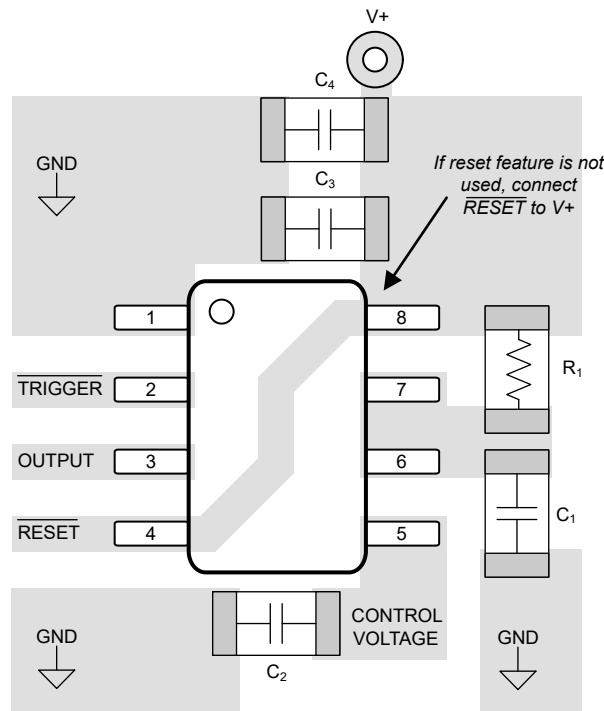


Figure 8-10. PCB Layout

9 Device and Documentation Support

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision M (July 2016) to Revision N (March 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Updated wording of <i>Features</i> bullets for clarity.....	1
• Updated GROUND and V+ pin types in <i>Pin Configuration and Functions</i>	3
• Changed V _{CC} to V+ in <i>Pin Configuration and Functions</i>	3
• Added (V+) to DISCHARGE description in <i>Pin Configuration and Functions</i>	3
• Updated R _{θJA} and added detailed thermal characteristics for all packages in <i>Thermal Information</i>	4
• Moved timing accuracy, timing shift with supply, timing shift with temperature, astable frequency, maximum frequency, output rise and fall times, and trigger propagation delay parameters from <i>Electrical Characteristics</i> to <i>Switching Characteristics</i>	5
• Changed supply current (I _S) typical values from 50 μA to 130 μA at V _S = 1.5 V; from 100 μA to 180 μA at V _S = 1.5 V; and from 150 μA to 220 μA at V _S = 12 V, in <i>Electrical Characteristics</i>	5
• Changed supply current (I _S) max value from 150 μA to 200 μA at V _S = 1.5 V in <i>Electrical Characteristics</i>	5
• Changed reset current (I _{RES}) test condition to V _{RES} = V _S in <i>Electrical Characteristics</i>	5
• Added new reset current (I _{RES}) typical value for test condition V _{RES} = 0 V to <i>Electrical Characteristics</i>	5
• Updated <i>Switching Characteristics</i> to clarify that values are specified by design, characterization, or both.....	5
• Changed units of timing shift with temperature from %V to %V (typo) in <i>Switching Characteristics</i>	5
• Changed functional block diagram to simplified schematic and moved to <i>Overview</i>	7
• Updated <i>Functional Block Diagram</i>	7
• Changed values of R _A from 3.9 kΩ to 1.78 kΩ, and R _B and 9 kΩ to 4.12 kΩ in Figure 7-6.....	10
• Changed "LM555" to "LMC555" (typo) in <i>Typical Applications</i>	12
• Updated figure in <i>Layout Example</i>	17

Changes from Revision L (February 2016) to Revision M (July 2016)	Page
• Changed order of <i>Features</i>	1
• Changed stable to astable (typo).....	1
• Changed stable to astable - typo.	7
• Changed beings to begins typo.....	8
• Changed typo LM555 to LMC555.	12
• Changed typo LM555 to LMC555.	12
• Added additional applications.	14

Changes from Revision K (January 2015) to Revision L (February 2016)	Page
• Changed typo - temp range from 185 to 85	4

Changes from Revision J (March 2013) to Revision K (October 2014)	Page
• Added <i>Pin Configuration and Functions, ESD Ratings, Feature Description, Device Functional Modes, Application and Implementation, Power Supply Recommendations, Layout, Device and Documentation Support, and Mechanical, Packaging, and Orderable Information</i> sections	1

Changes from Revision I (March 2013) to Revision J (March 2013)	Page
• Changed layout of National Semiconductor Data Sheet to TI format	17

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMC555CM/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	LMC555CM	
LMC555CMM/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	ZC5	Samples
LMC555CMMX/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	ZC5	Samples
LMC555CMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LMC555CM	Samples
LMC555CN/NOPB	ACTIVE	PDIP	P	8	40	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	(LMC, LMC555CN)555CN	Samples
LMC555CTP/NOPB	ACTIVE	DSBGA	YPB	8	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F02	Samples
LMC555CTPX/NOPB	ACTIVE	DSBGA	YPB	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	F02	Samples
LMC555IM/NOPB	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 125	LMC555IM	
LMC555IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(LM555I, LMC)555IM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMC555CMM/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LMC555CMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LMC555CTP/NOPB	DSBGA	YPB	8	250	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LMC555CTPX/NOPB	DSBGA	YPB	8	3000	178.0	8.4	1.5	1.5	0.66	4.0	8.0	Q1
LMC555IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMC555CMM/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LMC555CMMX/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0
LMC555CMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0
LMC555CTP/NOPB	DSBGA	YPB	8	250	208.0	191.0	35.0
LMC555CTPX/NOPB	DSBGA	YPB	8	3000	208.0	191.0	35.0
LMC555IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
LMC555CN/NOPB	P	PDIP	8	40	506	13.97	11230	4.32

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

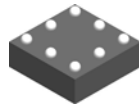
P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

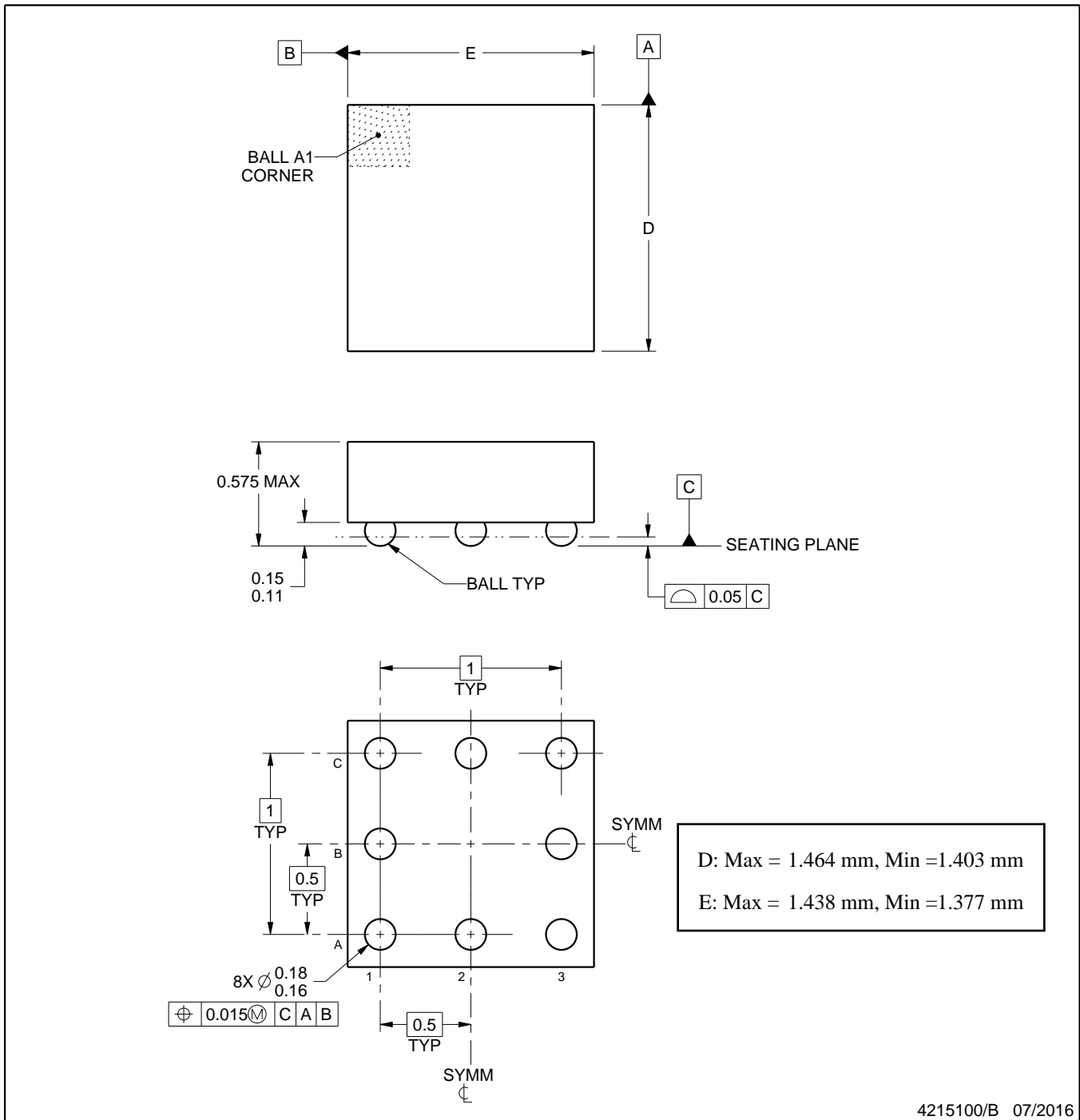
YPB0008



PACKAGE OUTLINE

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

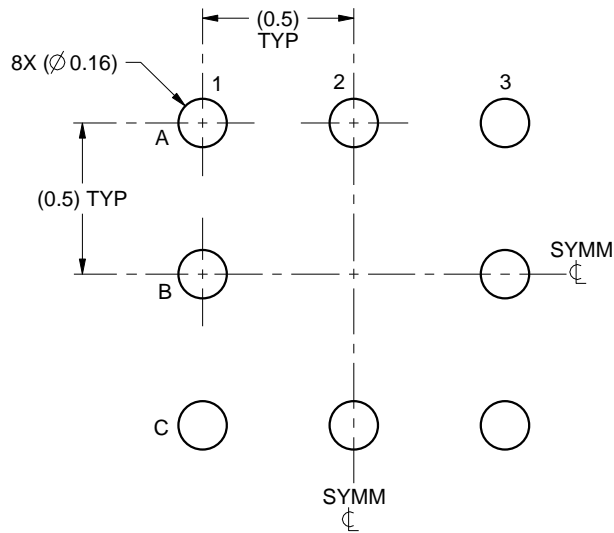
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

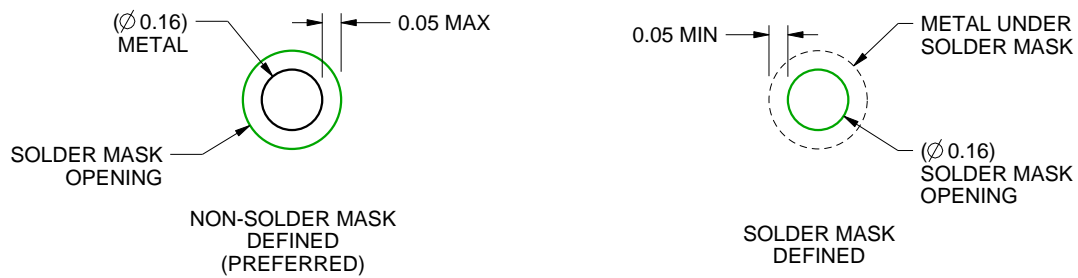
YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4215100/B 07/2016

NOTES: (continued)

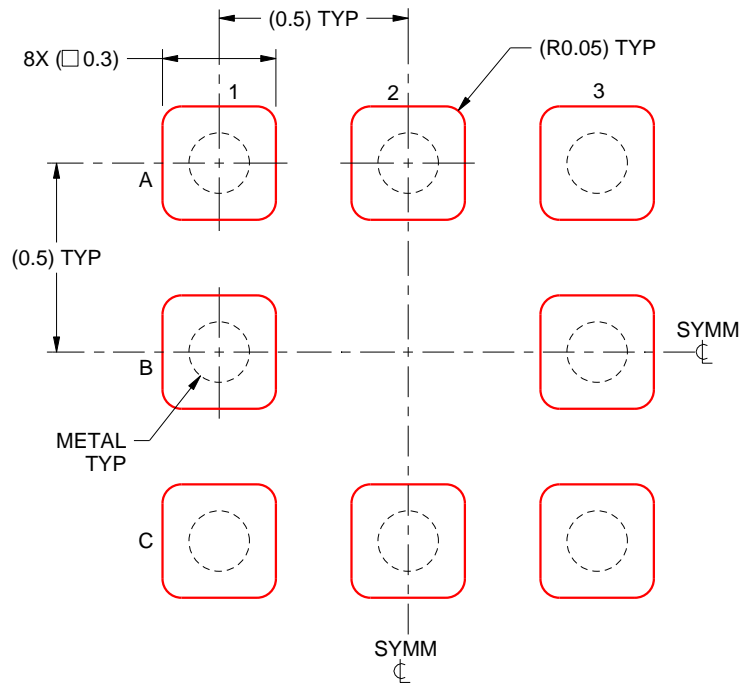
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. See Texas Instruments Literature No. SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YPB0008

DSBGA - 0.575 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.125mm THICK STENCIL
SCALE:50X

4215100/B 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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