Application Note 1111 An Introduction to IBIS (I/O Buffer Information Specification) Modeling

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An Introduction to IBIS (I/O Buffer Information Specification) Modeling

National Semiconductor
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INTRODUCTION

With time to market becoming shorter and shorter, system designers are struggling to release a product from concept to reality in a tightly budgeted time. The need to simulate before prototyping is very essential and the ability to simulate and simulate accurately has heightened even more. But in order to simulate a system level board, all components on the board need to be modeled. Unfortunately many device models are not readily available from vendors.

IBIS (I/O Buffer Information Specification) is a Behavioral Modeling Specification that is gaining world wide popularity as a standard format to generate device models. IBIS solves many of the problems that prevented system designers from obtaining semiconductor vendor's SPICE models.

This application note discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures and future trends.

ABOUT IBIS...

I/O Buffer Information Specification is a fast and accurate behavioral method of modeling input/output buffers based on V/I curve data derived from measurement or full circuit simulation. It uses a standardized software parsable format in the form of an ASCII file to store the Behavioral Information needed to model device characteristics of integrated circuits.

IBIS can be used by almost any Simulators/EDA tools in the industry. A wide range of Industry leaders support the IBIS open forum. Below is a partial list of vendors supporting the IBIS method of model generation.

AMP Incorporated www.amp.com (AMPredictor)
Applied Simulation Technology www.edac.org/Apsim (Apsim)
Avanti (Meta I/O)
Cadence Design System www.cadence.com (DFSigNoise)
HPEESof www.hp.com
HyperLynx www.hyperlynx.com (LineSimPRO)
INCASES www.pad.incases.com (INSIDE, EXLIN)
IntuSoft www.intusoft.com (IS_SPICE)
Mentor Graphics www.mentorg.com (IS)
Quantic EMC Inc www.quantic-emc.com (Greenfield)
Veribest www.veribest.com
Viewlogic Systems www.viewlogic.com (XTK/TLC)
Zuken-Redac

HISTORY OF IBIS

The originator of IBIS was Intel. Presently the standard is being driven by the IBIS forum with over 35 members consisting of EDA vendors, Computer manufacturers, Semiconductor vendors and Universities.

IBISv1.0 was released in April 1993. IBISv1.0 is capable of modeling standard TTL or CMOS type of I/O structure. In June 1993 at the DAC (Design Automation Conference) show in Dallas, IBISv1.1 was released. The major changes were the addition of more comments to the original specification.

IBISv2.0 was ratified in June 1994 at the DAC conference in San Diego. IBISv2.0 is a considerable improvement over IBISv1.1. Some of the added features are, Multiple rail support (ex. V+ and V− supply for RS-232), ECL, Terminator models, Open drain, Open collector, Differential I/O, Controlled slew rate and Definitions of complex package parameters to name a few.

IBISv2.1 added more comments to clarify v2.0 and has been ratified December 1994. Today IBIS is an approved standard within EIA (Electronic Industry Alliance) and is also known under ANSI/EIA-656.

IBISv3.0 has been ratified at DAC97. The committee is in the process of finalizing the development of the v3.0 parser. IBISv3.0 has various advanced features. Some of the added features are Driver selection, Diode stored charge, Package Model extension, Electrical board description, Multi-stage Drivers, Series elements and more. IBISv3.1 improves upon clarification issues with v3.0.

The EIG (Electronic Information Group) within EIA has been actively working towards making IBIS part of the IEC (European standard). IBIS has been accepted as IEC-62014-1 (Sep'97) at the Tokyo International Standards meeting.

The software parser (known as the *"Golden Parser"*) validates the IBIS model file. The *Golden Parser* checks the syntax of the IBIS model file to confirm that the data format meets the IBIS specification. The object code of the parser is available for free from the forum. Simulator vendors may also purchase the source code for a fee.

IBIS is backwards compatible. So all models created today using the present version of the specification are guaranteed to work with future versions of IBIS. The IBIS forum is continually defining new and improved ways of modeling complex and unique I/O structures.

ADVANTAGES OF IBIS

The IBIS model file protects proprietary information about the modeled circuit as no process or circuit design information is disclosed. A SPICE model on the other hand can disclose substantial information that Semiconductor vendors consider to be confidential such as circuit nodal connections and process parameters. IBIS models are accurate, as non-linear aspects of I/O structures as well as package parasitic and ESD structures are considered in the model parameters. Since IBIS is behavioral, the simulation time for an IBIS model can run 25x faster than a structural model (SPICE). IBIS does not have non-convergence issues like SPICE and can practically run on any Industry wide platforms as most EDA vendors support the IBIS specification. One of the most popular uses of IBIS is for Signal Integrity Analysis on system boards. The models are very easy to create as they can be made from bench measurements or from simulation data.

Following is a behavioral block diagram of IBIS (*Figure 1*) and the pieces needed to create an Input and an Output model.

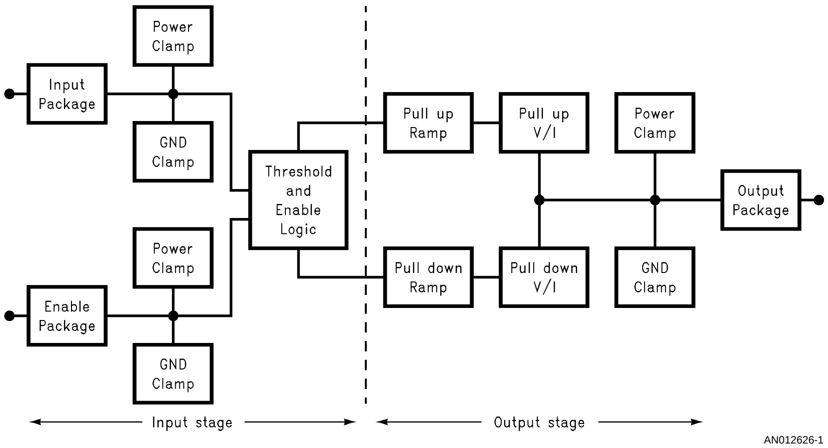

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FIGURE 1. Behavioral Diagram of IBIS

INPUT STRUCTURE MODEL

Information needed to model the Input Structure is shown in *Figure 2*. C__pkg, R__pkg and L__pkg are the package parameters. Power__Clamp and GND__Clamp defines the ESD structures on the Inputs. The V/I curve data defines these clamp structures. C__comp is the input capacitance of the input pin.

OUTPUT STRUCTURE MODEL

Information needed to model the output structure is shown in *Figure 3*. Pullup defines V_{OH}/I_{OH}, Pulldown defines the V_{OL}/I_{OL} and Ramp defines the dV/dT of the Rising and Falling waveforms.

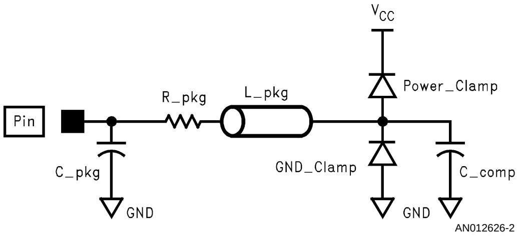

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FIGURE 2. Input/Enable Structure Model

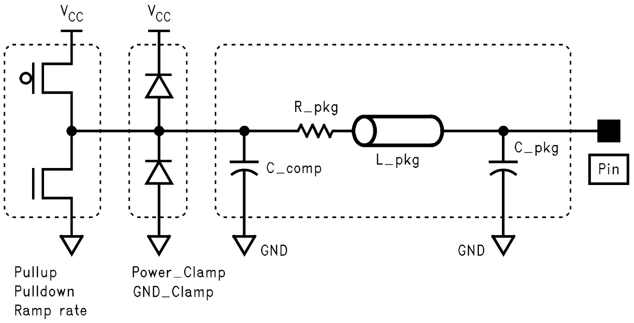

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FIGURE 3. Output Structure Model

The Pullup and Pulldown data are created from the V/I curves. The remaining parameters are similar to the Input structure except that they define the package parasitic of the output pin as well as the output capacitance of the output pin.

The Pullup and Power__Clamp data are "V_{CC} relative", meaning that the voltage values are referenced to V_{CC} and not ground. So the voltages in the tables are derived from the equation: $V_{table} = V_{CC} - V_{output}$. V_{CC} relative data is necessary for the simulator as the Pullup structure depends on the voltage between the output and V_{CC} and not the voltage between the output and ground pin.

An Interconnect engineer can create a slow and a fast model using IBIS. The slow model is useful to determine flight time and the fast model is useful to analyze overshoot, undershoot, crosstalk, etc. By combining min I_{OH}/I_{OL} with max ramp time and max package parameters, a slow model is generated. To create a fast model, the max I_{OH}/I_{OL}, min ramp and minimum package information is used.

MODEL GENERATION FLOW

The following steps are used in generating an IBIS model. All necessary V/I and other parameters need to be either measured on the bench, obtained from simulation or provided by the semiconductor vendor. (Step 1)

Measurements of package parameters can be made through TDR (Time Domain Reflectometry) techniques if they are not available from the semiconductor vendor. V/I data can be collected using a curve tracer or programmable supply with sinking and sourcing capabilities. Clamp curves can be generated by putting the device in TRI-STATE® and sweeping the I/O. For non TRI-STATE devices, the V/I curves are the summation of the Clamp and Pullup/Pulldown.

The required data is: R__pkg, L__pkg, C__pkg and C__comp for all Inputs and Outputs and Enables. Power__Clamp and GND__Clamp (ESD structures if present) for I/O. Pullup, Pulldown and Ramp rates for Outputs.

The Interconnect engineer then creates the IBIS ASCII file following the format defined in the IBIS standard (Step 2). This can be done on a UNIX or DOS text editor.

The ASCII model file is then checked by the *"Golden Parser"* for possible syntax errors (Step 3). If passed, the model is then imported into a simulator and validated for accuracy (Step 4). Now the model is ready for use. *Figure 4* shows this flow in a graphical form.

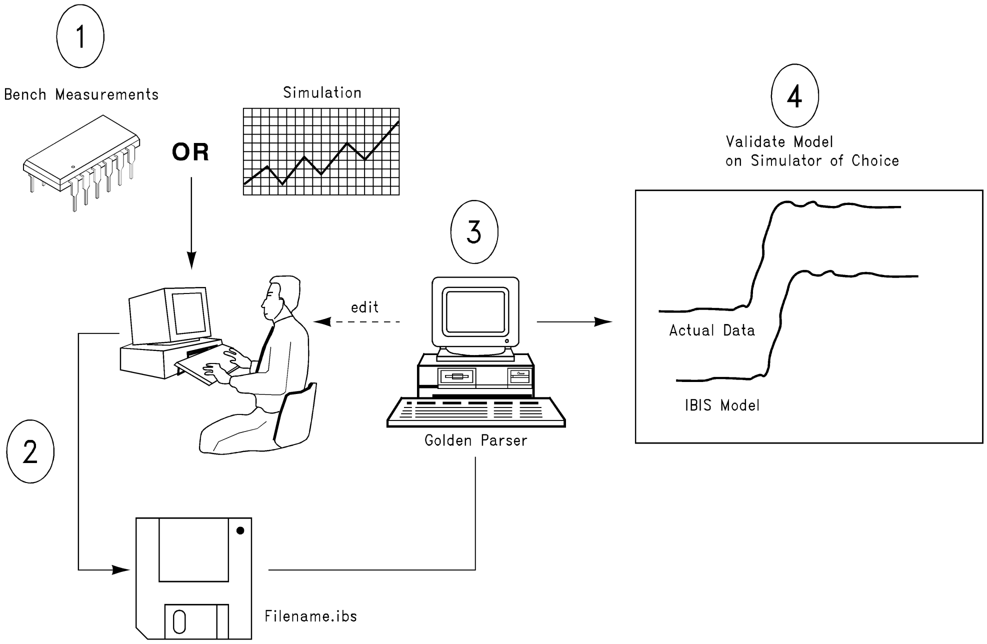

FIGURE 4. IBIS Model Generation Flow

MODEL VALIDATION ON SIMULATOR

Model validation is the final and critical step to IBIS modeling. Visual inspection, s2iplt checks, parser test, simulation of model under known loads, comparison of simulation data to bench/SPICE, edge rate and signal swing level verification are also done during this phase. National's Interface Products Group validates the IBIS models on two different IBIS complaint simulators.

IBIS models are primarily used for SI (Signal Integrity) Analysis. These are typically crosstalk, ringing, overshoot, undershoot, mismatched impedance, reflections, line termination analysis, topology scheme analysis, design rule generation and multi-board simulation.

IBIS is best suited for SI analysis on system boards requiring very little run time (25X faster than SPICE).

FUTURE TRENDS OF IBIS

Since its formation in 1993, IBIS has improved it's specification by many folds. More complex modeling features and possibly timing analysis may be added to future IBIS specifications. DIE (Die Information Exchange) forum which specifies DIE information for MCM applications references IBIS as the Signal Integrity Analysis specification. FMF (Free Model Forum), OMF (Open Model Forum), CFI (CAD Framework Initiative) are some of the other forums that references IBIS for behavioral modeling.

EIAJ III (I/O Interface model for Ics) is another organization working on generating an I/O spec based on IBIS but with added SPICE syntax's.

IEC 93/67/NP(IBIS and EMC simulation) is a task force assigned to investigate the use of IBIS models for EMC simulation.

IBIS is also working with the JC-16B committee to define SSTL and HSTL technology modeling using IBIS.

NATIONAL AND IBIS

National's various product lines are generating IBIS models today. Interface Applications actively participates in IBIS forum meetings and was very instrumental in adding the Differential I/O specification to IBISv2.1.

CONCLUSION

IBIS modeling is accurate, easy to create and compatible on a wide rage of Simulation platforms. It solves the *"NO MODELS AVAILABLE"* problem in the industry. IBIS has created a common Industry format for modeling using Behavioral information and does not disclose any propietary process parameters or circuit design details.

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