

AN-1126 BGA (Ball Grid Array)

ABSTRACT

Leaders in the consumer electronics industry will be determined by their ability to deliver increasingly miniaturized products at lower costs. The Ball Grid Array (BGA) package achieves these objectives by providing increased functionality for the same package size while being compatible with existing Surface Mount Technology (SMT) infrastructure.

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1 Introduction

Leaders in the consumer electronics industry will be determined by their ability to deliver increasingly miniaturized products at lower costs. The Ball Grid Array (BGA) package achieves these objectives by providing increased functionality for the same package size while being compatible with existing Surface Mount Technology (SMT) infrastructure.

Some of the other benefits of using BGA packages over similar lead count packages include:

1. Efficient use of board space.
2. Improved thermal and electrical performance. BGAs can offer power and ground planes for low inductances and controlled impedance traces for signals.
3. Improved surface mount yields compared to similar fine pitch leaded packages.
4. Reduced package thickness.
5. Potentially lower cost of ownership compared to leaded packages by virtue of their reworkability.

This application note provides general information about Plastic Ball Grid Array (PBGA) packages, and its variants - the TE-PBGA (Thermally Enhanced BGA), EBGA (Enhanced BGA) and TSBGA (Tape Super BGA). Information on FBGA (Fine Pitch BGA) and LBGA (Low Profile BGA) packages can be found in National Semiconductor's Laminate CSP application note (AN 1125). [Figure 1](#).

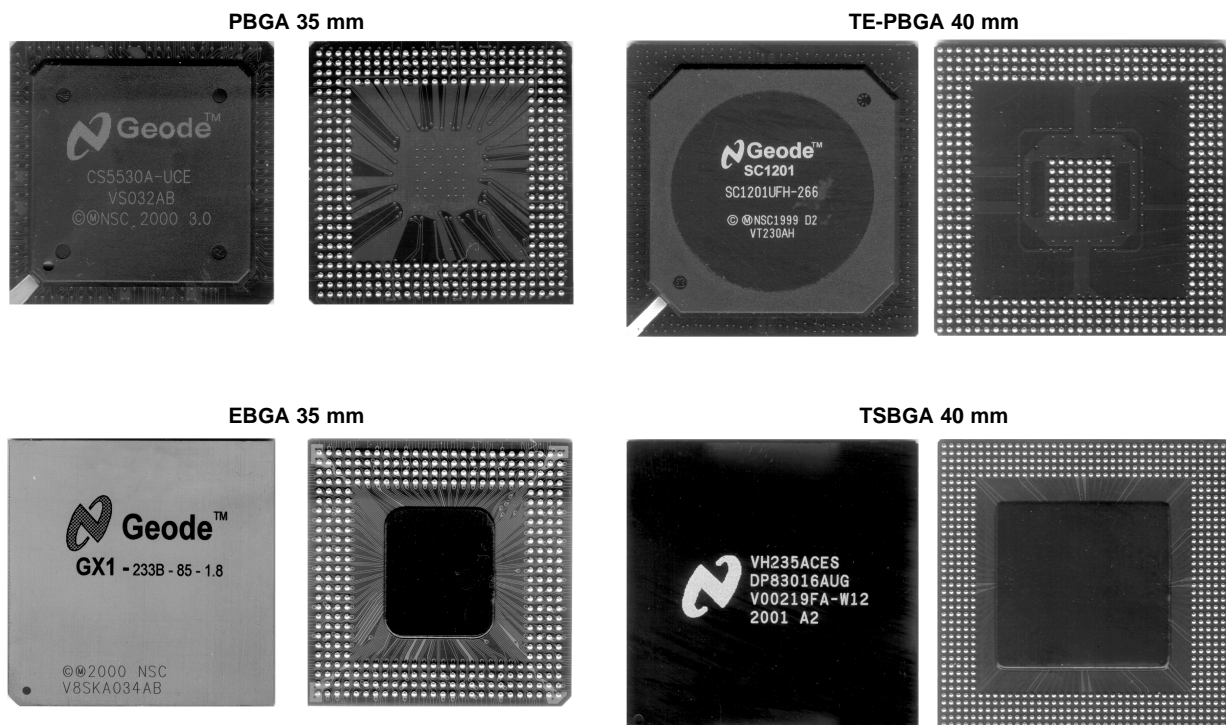


Figure 1. PBGA, TE-PBGA , EBGA and TSBGA

2 Package Overview

2.1 PBGA (PLASTIC BGA) CONSTRUCTION

The PBGA (Plastic Ball Grid Array) package is a cavity-up package based on a PCB substrate fabricated of Bismaleimide Triazine (BT) or FR5 epoxy/glass laminate; [Figure 2](#).

The BT / FR5 core is available in several thicknesses with rolled copper cladding on each side. The final plated copper thickness is typically 25-30 μm .

Solder mask is applied on both sides over the copper pattern to ensure that all the substrate vias are completely tented.

Four layer substrates are available for applications requiring power or ground planes (they also provide additional routing flexibility). For thermal applications, the inner layers can be clad with thicker (2 oz) copper (~ 70 μm).

The IC is attached on the top side of the substrate using die attach. The chip is then gold wire-bonded to bondfingers on the substrate. Traces from the bondfingers transfer the signals to vias that then carry them to the bottom of the substrate and finally to circular solder pads on the same side.

The bottom side solder pads are laid out in a square or rectangular grid format with a pitch recommended by JEDEC registration standards (MO-151) for PBGAs.

The part is then over-molded to completely encapsulate the chip, wires and substrate bondfingers. [Figure 6](#) shows the typical process flow for cavity up and cavity down assembly.

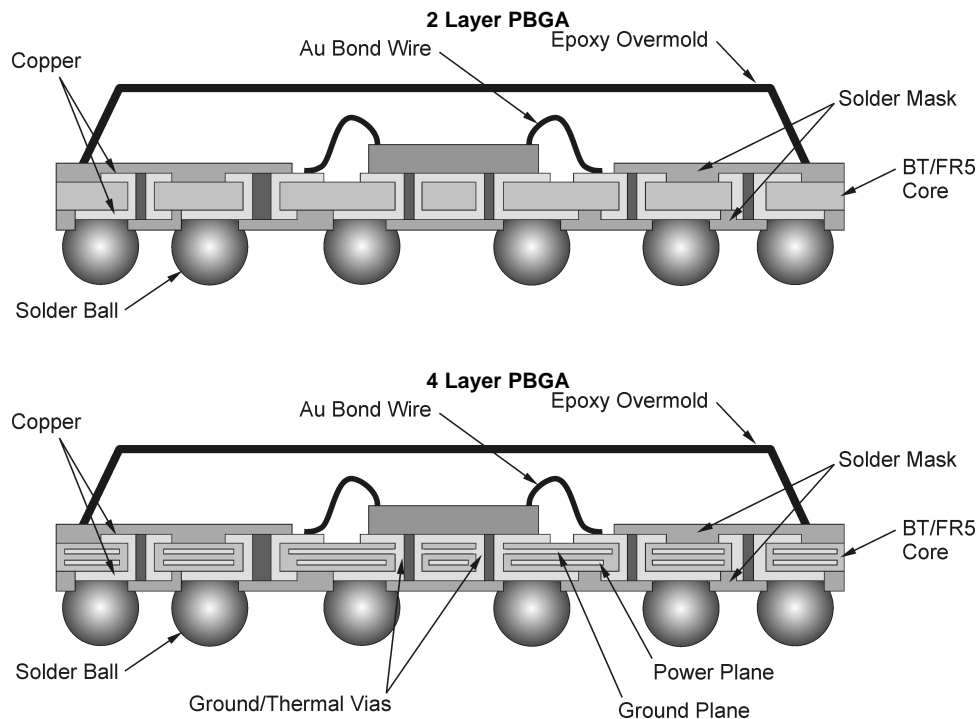


Figure 2. Cross-Sectional View of 2 and 4 Layer PBGA

2.2 TE-PBGA (THERMALLY ENHANCED BGA) CONSTRUCTION

The TE-PBGA (Thermally Enhanced Plastic Ball Grid Array) package is a variant of the PBGA package for enhanced thermal dissipation, [Figure 3](#). A drop-in heat slug is added to a 4 Layer PBGA with 2 oz (70 μm) copper on the inner layers. This provides a much better thermal path to the top surface of the package. The heat slug can be grounded to provide an EMI shield for the package. Thermal vias are provided under the die and are typically connected to the package ground plane thereby conducting the heat to the PCB ground plane.

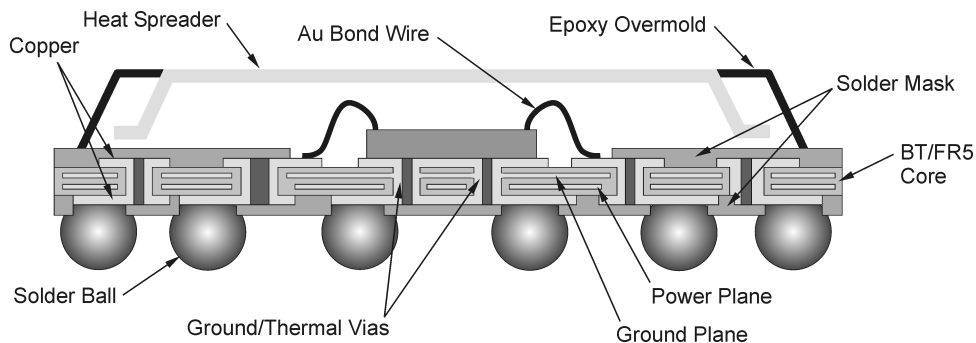


Figure 3. Cross-Sectional View of 4 Layer TE-PBGA

2.3 EBGA (ENHANCED BGA) CONSTRUCTION

The EBGA (Enhanced Ball Grid Array) package is a cavity down package configured to provide enhanced thermal and electrical performance; Figure 4. The thermal advantage of this package is realized by attaching the die to the bottom of a heat spreader or heat slug that also forms the top surface of this package. Since the heat spreader is on top of the package and is exposed to airflow the thermal resistance is very low.

The heat spreader or heat slug is laminated to a printed circuit board (PCB) substrate fabricated of BT or FR5 epoxy/glass laminate. The IC die is bonded to the heat spreader using a die attach adhesive. The die is then gold wire-bonded to bondfingers on the substrate. Traces from the bondfingers transfer the signals to solder pads. Unlike typical PBGAs, vias in an EBGA are primarily used to connect the solder pads to inner layers (typically the power and ground planes).

The solder pads are in a square or rectangular grid format with a pitch recommended by the JEDEC registration standard (MO-151) for the EBGAs.

The package is encapsulated to completely cover the chip, wires and substrate bondfingers.

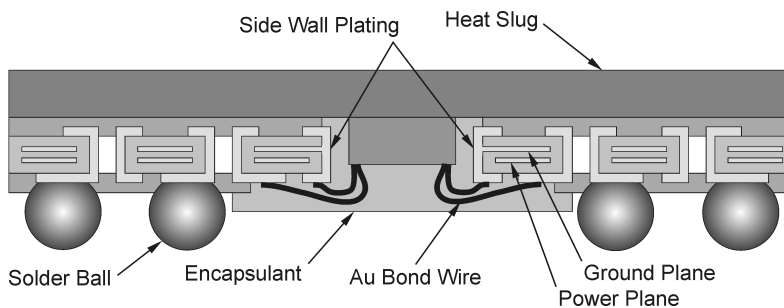


Figure 4. Cross-Sectional View of EBGA

2.4 TSBGA (TAPE SUPER BGA) CONSTRUCTION

The TSBGA (Tape Super Ball Grid Array) is similar to the EBGA package but uses a polyimide tape instead of the laminate substrate. The TSBGA is available in two versions: I-Metal and I-Metal-I-Plane structure packages.

The I-Metal tape has copper foil on one side and is laminated to the heat spreader on the other side, Figure 5. Solder mask is applied to the copper trace pattern to form the solder ball pads, bondfingers and rings. The die is attached directly to the heat spreader and then wire-bonded. Traces take the signals to the solder balls -there are no vias in the I-Metal package. The package assembly is similar to the EBGA.

In the I-Metal-I-Plane structure, the ground solder ball pads are formed by punching out vias in the tape, [Figure 5](#). The heat spreader is exposed on the punched openings. The punched vias are filled with solder, connecting the ground solder balls directly to the heat spreader. All ground bond pads on the die are bonded to a ring on the heat spreader. This provides a low inductance ground plane and a good return path for signal traces, with controlled impedances. Thus, the I-Metal-I-Plane package offers better electrical performance than a I-Metal package. Assembly process steps are identical to the I-Metal package, except for the two stage solder ball attach process.

For cavity down packages (TSBGA,EBGA) with ball pitch $\leq 1\text{mm}$, the PCB warpage must be carefully controlled and it is recommended that PCB warpage under the package is < 4 mils.

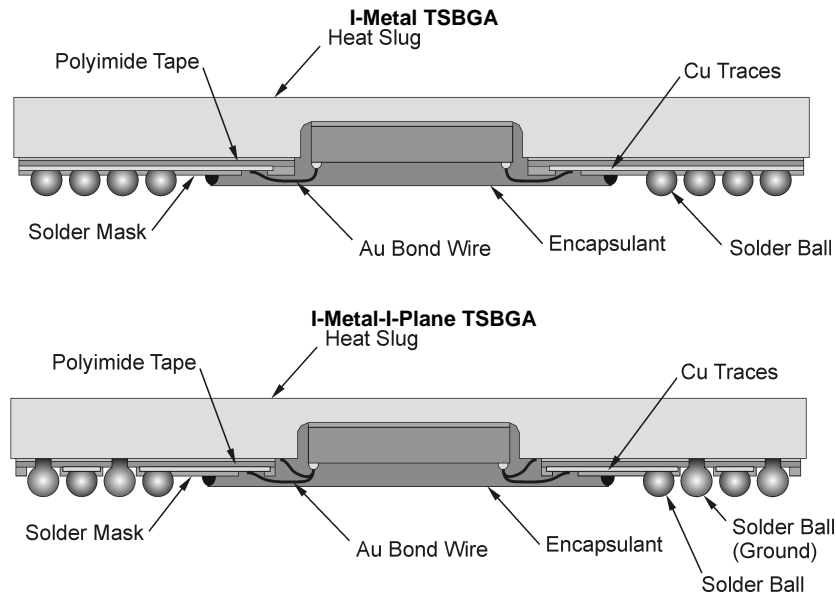


Figure 5. Cross-Sectional View of TSBGA Packages

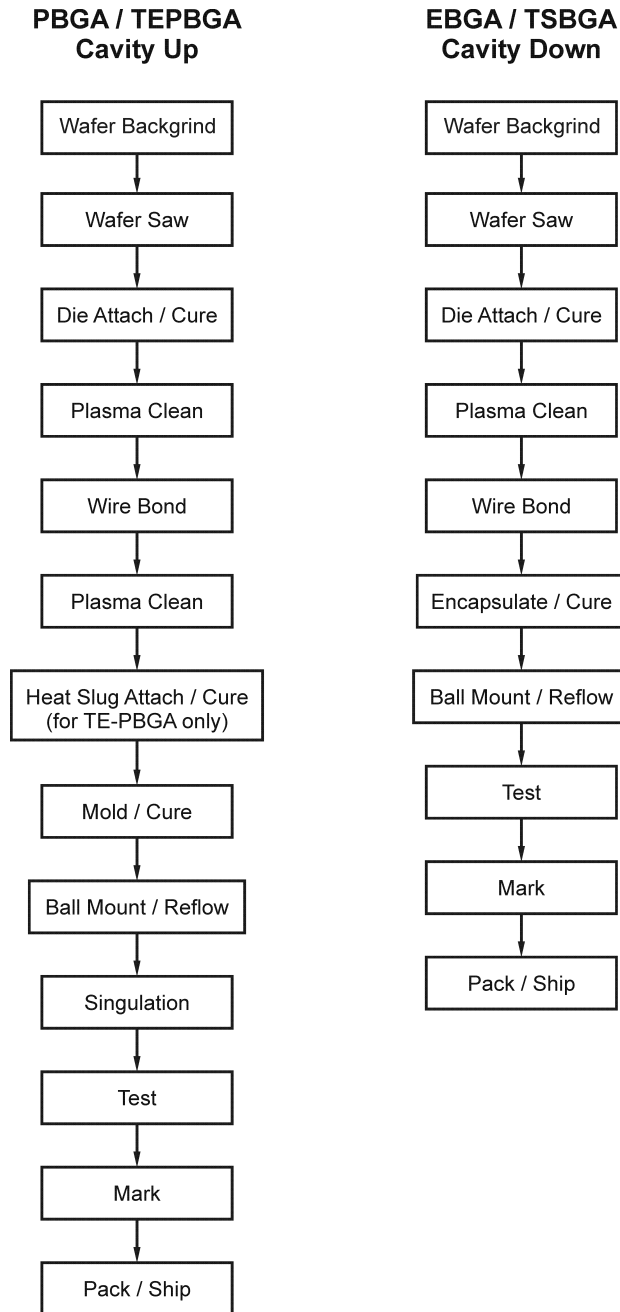


Figure 6. Typical Process Flow

2.5 PACKAGE ELECTRICAL PERFORMANCE

Electrical information about BGA packages is available in Application Note AN-1205. For electrical models of specific packages, contact your local National Semiconductor representative.

3 Component Reliability

All BGA packages are qualified to JEDEC MSL Level 3 at 220° C reflow conditions. All packaged devices pass 1000 hrs, THBT (85° C / 85%RH / Biased Testing) , 1500 TMCL (-40 to 125° C), 96 hrs ACLV (121° C / 100%RH), 1000 hrs HTSL (150° C) and 1000 hrs DOPL (125° C).

4 Package Handling/Shipping Media

The BGA packages are shipped in high temperature tolerant thin matrix trays. These trays comply with JEDEC standards and are easily stackable for storage and assembly.

5 Design Recommendations

5.1 SOLDER PAD GEOMETRY

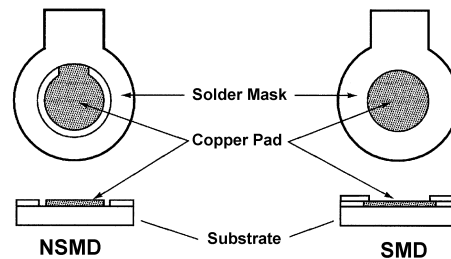


Figure 7. NSMD and SMD Pad Definition

5.2 NSMD vs. SMD LAND PATTERN

Two types of land patterns are used for surface mount packages: 1) Non-Solder Mask Defined pads (NSMD) and, 2) Solder Mask Defined pads (SMD). NSMD pads have a solder mask opening that is larger than the pad, whereas SMD pads have a solder mask opening that is smaller than the metal pad. Figure 7 illustrates the two different types of pad geometry.

NSMD is preferred because tighter control of the copper artwork registration is possible compared to the positional tolerance of the solder masking process. Moreover, SMD pad definition may introduce stress concentration points in the solder that may result in solder joint cracking under extreme fatigue conditions.

NSMD pads require a clearance (typically 3 mils) between the copper pad and solder mask, to avoid overlap between the solder joint and solder mask due to mask registration tolerances.

For optimal reliability, National Semiconductor recommends a 1:1 ratio between the package pad and the PCB pad on the BGA. The ratio may be reduced to 1:0.8 if trace routing constraints make it absolutely necessary. Figure 7 and Table 1.

Table 1. Guidelines for PCB Pad Design

	1.27 mm Pitch		1.0 mm Pitch	
	NSMD	SMD	NSMD	SMD
Solder Ball Diameter	0.75 mm	0.75 mm	0.63 mm	0.63 mm
PCB Pad Diameter	0.64 mm	0.78 mm	0.46 mm	0.60 mm
Solder Mask Opening Diameter	0.78 mm	0.64 mm	0.60 mm	0.46 mm

5.3 ESCAPE ROUTING GUIDELINES

A typical PBGA has four or five rows of solder balls around the periphery of the package. The number of lines routed (**N**) between the pads on the PCB is defined by the pad size and trace (width and spacing) fabrication capabilities of the PCB manufacturer. The following relationship is used to define **N**:

$$N = \frac{P - D - S}{L + S}$$

**Figure 8. P = Pad Pitch
D = Pad Diameter
L = Line Width
S = Line Space**

For NSMD pads, exposure of underlying copper traces is forbidden, so the diameter and tolerance of the solder mask opening define **D**.

The number of routing lines as a function of pad pitch for various PCB line space/width geometries is shown in [Table 2](#). Routing assumes a four-layer board (2 signal and 2 ground) with NSMD pads on the PCB.

Table 2. Recommended Number of Routing Lines Between Adjacent PCB Solder Pads

	Ball pitch 1.27 mm	Ball pitch 1.00 mm
L/S = 0.15 mm	1	N/A
L/S = 0.125 mm	1	1
L/S = 0.10 mm	2	1

Either a 1.0 or 1.27 mm pitch PBGA with four rows of solder balls can be routed to a four layer PCB ([Figure 9](#)) using a 0.15 mm (6 mils) or 0.125 (5 mils) line/space respectively. The first two ball rows can be routed to one signal layer while the third and fourth ball rows can be routed to a second signal layer.

Routing becomes more complicated for a four-layer board, if there are five rows of solder balls. For example, for a 1.27 mm ball pitch PBGA, a 0.125 mm (5 mil) PCB line/space design will be necessary for routing ([Figure 10](#)) with a 0.8:1 ratio of PCB pad to package pad. A 1.0 mm PBGA will require a 0.10 mm (4 mil) line/space with a 0.8: 1 PCB pad to package pad ratio, to successfully route 5 rows of solder balls to a four-layer PCB ([Figure 11](#)). For both packages, the first three ball rows are routed to one signal layer while the fourth and fifth ball rows are routed to the second signal layer.

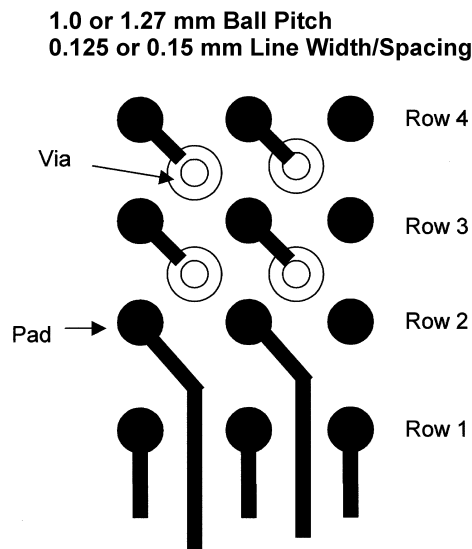


Figure 9. Routing for Four Rows of Solder Balls

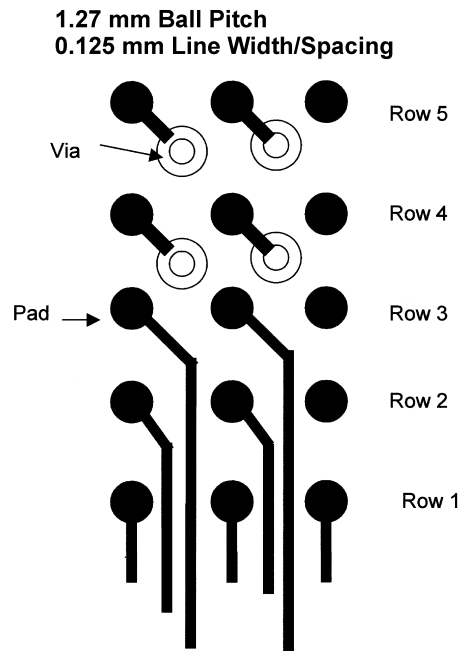


Figure 10. Routing for Five Rows of Solder Balls

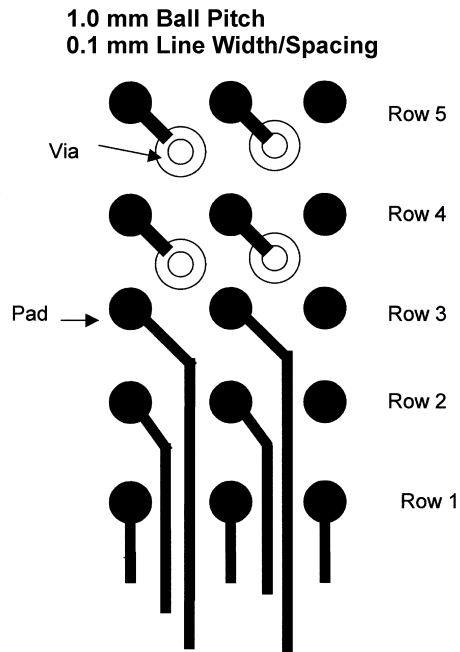


Figure 11. Routing for Five Rows of Solder Balls

6 Assembly Recommendations

6.1 PROCESS FLOW & SET-UP RECOMMENDATION

The BGA surface mount assembly process flow includes:

- PCB plating requirements

- Screen printing the solder paste on the PCB
- Monitoring the solder paste volume (uniformity)
- Package placement using standard SMT placement equipment
- X-ray inspection prior to reflow to check for placement accuracy and other defects such as solder paste bridging
- Reflow and flux residue cleaning (dependent upon the flux type)
- X-ray inspection after reflow to check for defects such as solder bridging & voids

6.2 PCB PLATING RECOMMENDATIONS

A uniform PCB plating thickness is key for high assembly yield.

- PCB with Organic Solderability Preservative coating (OSP) finish is recommended.
- For PCBs with electroless or immersion gold finish, the gold thickness recommendation is $0.15\ \mu\text{m} \pm 0.05\ \mu\text{m}$ to avoid solder joint embrittlement. For PCBs with Hot Air Solder Leveling (HASL), the surface flatness should be controlled within 28 μm .

6.3 SOLDER PASTE PRINTING

Solder paste deposition by the stencil-printing process involves the transfer of the solder paste through pre-defined apertures with the application of pressure. Stencil parameters such as aperture area ratio and the stencil fabrication method have a significant impact on paste deposition. Inspection of the stencil prior to placement of the BGA package is highly recommended to improve board assembly yields. Three typical stencil fabrication methods include:

- Chem-etch
- Laser cut
- Metal additive processes

Nickel-plated electro polished chem-etch or laser cut with tapered aperture walls (5° tapering) is recommended to facilitate paste release. The recommended aperture size is 0.1 mm larger than the pad size to allow a 0.05 mm overprinting on each side. Stencil thickness of 6 mils is recommended.

6.4 PASTE RECOMMENDATIONS

Type 3 water soluble, no clean paste or lead free solder pastes are acceptable.

6.5 COMPONENT PLACEMENT

BGA packages are placed using standard pick and place equipment with a placement accuracy of ± 0.10 mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system which physically performs the pick and place operation. Two commonly used types of vision systems are: (1) a vision system that locates a package silhouette and (2) a vision system that locates individual bumps on the interconnect pattern. Both methods are valid since the parts align due to self-centering feature of the BGA solder joint during solder reflow. The latter vision system while providing greater accuracy tends to be more expensive and time consuming.

BGAs have excellent self-alignment during solder reflow if a minimum of 50% of the ball is aligned with the pad. The 50% accuracy is in both the X and Y direction as determined by the following relation.

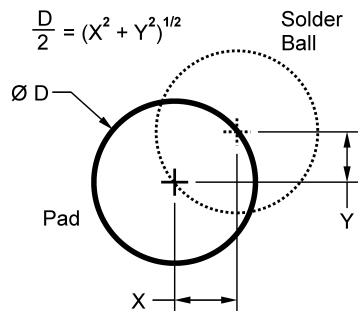


Figure 12. BGA self centering

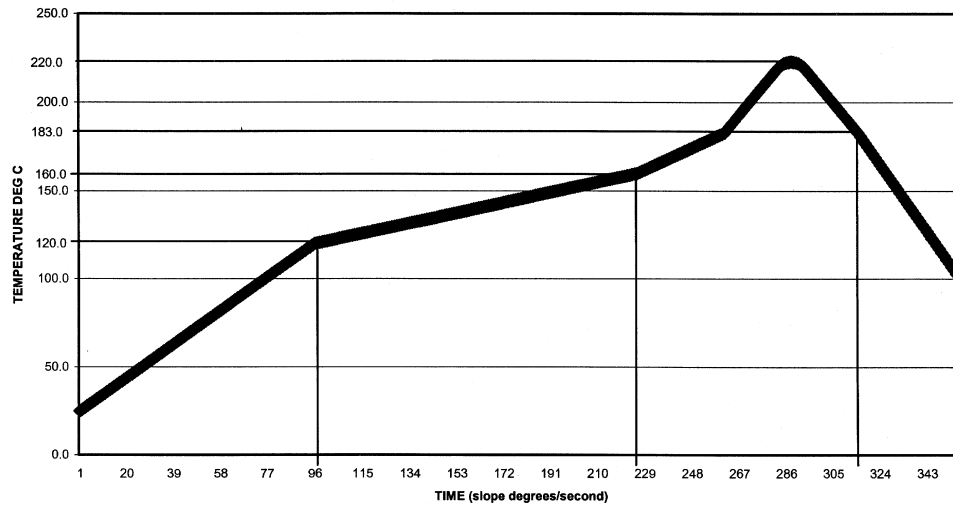
Standard pick and place equipment can place these components within the required degree of accuracy.

6.6 REFLOW

The BGA may be assembled using standard IR or IR convection SMT reflow processes. As with other packages, the thermal profile for specific board locations must be determined. The BGA is qualified for up to three reflow cycles at 225° C peak (J-STD-020). The actual temperature used in the reflow oven is a function of:

- Board density
- Board geometries
- Component location on the board
- Size of surrounding components
- Component mass
- Furnace loading
- Board finish
- Solder paste types

It is recommended that the temperature profile be validated at the ball location of the BGA as well as several other locations on the PCB surface.



		Convection / IR
Ramp Up °C/sec⁽¹⁾	Maximum	3 °C/sec
	Recommended	1 °C/sec⁽²⁾
	Minimum	⁽²⁾
Dwell Time 120° C to 160° C⁽¹⁾	Maximum	⁽²⁾
	Recommended	130 seconds
	Minimum	⁽²⁾
Dwell Time 160° C to 183° C⁽¹⁾	Maximum	⁽²⁾
	Recommended	35 seconds
	Minimum	⁽²⁾
Dwell Time ≥ 183° C⁽¹⁾	Maximum	85 seconds
	Recommended	50 seconds⁽²⁾
	Minimum	⁽²⁾
Peak Temperature⁽¹⁾	Maximum	225° C ⁽²⁾
	Recommended	220° C⁽²⁾
	Minimum	
Dwell Time Max. (within 5° C of peak temperature)	Maximum	10 seconds
	Recommended	5 seconds
	Minimum	1 second ⁽²⁾
Ramp Down °C/sec⁽¹⁾	Maximum	4 °C/sec
	Recommended	2 °C/sec
	Minimum	⁽²⁾

⁽¹⁾ Will vary depending on board density, geometry, package types, PCB finish, and solder paste types.

⁽²⁾ All Temperatures are measured on the solder joint.

Figure 13. General Reflow Profile Guidelines for PBGA & EBGA

6.7 SOLDER JOINT INSPECTION

After surface mount assembly, transmission X-ray should be used for sample monitoring of the solder attachment process. This identifies defects such as solder bridging, shorts, opens and voids.

Voids, up to 25% of the solder joint area, typically do not have an impact on solder joint reliability.

6.8 REPLACEMENT AND REWORK

Removing BGA packages involves heating the solder joints above the liquidus temperature of the solder and picking the part off the PCB when the solder melts. The quality of rework is controlled by directing thermal energy to solder without over-heating the adjacent components.

Heating should occur in an encapsulated, inert, gas-purged environment where the temperature gradients do not exceed $\pm 5^{\circ}$ C across the heating zone using a convective bottom side pre-heater to maximize temperature uniformity. If possible, the PCB area should be preheated through the bottom side of the board, to 100° C before heating the BGA to ensure a controlled process. Interchangeable nozzles designed with different geometries will accommodate different applications to direct the airflow path. Once the liquidus temperature is reached, the nozzle vacuum is automatically activated and the component is removed.

Complete rework systems are available from several suppliers like METCAL, Austin American Technology (AAT), Sierra Research and Technology (SRT), Manix Manufacturing, Semiconductor Equipment Corp. (SEC) and PACE.

6.9 SITE PREPARATION

Once the BGA is removed, the site must be cleaned in preparation for package attachment. The best results are achieved with a low-temperature, blade-style conductive tool matching the footprint area of the BGA in conjunction with a de-soldering braid. No-clean flux is needed throughout the entire rework process. Care must be taken to avoid burn, lift-off, or damage of the PCB attachment area.

6.10 COMPONENT PLACEMENT

Most BGA rework stations will have a pick and place feature for accurate placement and alignment. Manual pick and place, with only eyeball alignment, is not recommended. It is difficult to achieve consistent placement accuracy.

6.11 COMPONENT REFLOW

It is recommended that the reflow profile used to reflow the BGA be as close to the PCB mount profile as possible. Preheat from the bottom side of the board is recommended where possible. Once the liquidus temperature is reached, the solder will reflow and the BGA will self align.

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