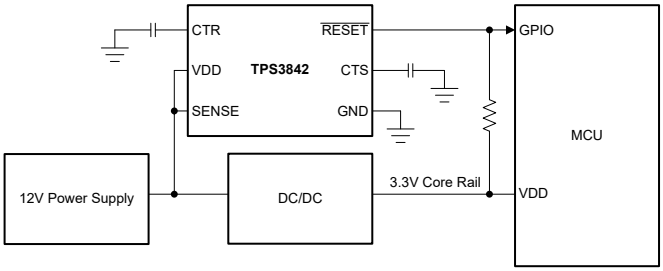
TPS3842 42V Small Size, 850nA Undervoltage Supervisor With Programmable Delay and De-Glitch

1 Features

- Wide supply voltage range: 1.9V to 42V
- VDD, SENSE, and $\overline{\text{RESET}}$ are rated to 42V
- Low quiescent current: 850nA (typical)
- High threshold accuracy: 0.5% (typical)
- Fixed internal threshold voltages: 2.7V to 9.5V
- Adjustable voltage variant: 0.7V
- Capacitor programmable adjustable delay time with CTR pin
- Capacitor programmable deglitch delay time with CTS pin
- Open-drain, active-low output
- Temperature range: –40°C to 125°C
- Small size: SOT563 (DRL)

2 Applications

- Factory Automation
- Motor Drives
- Power Devivery
- Enterprise Systems
- Grid Infrastructure



Typical Application Circuit

3 Description

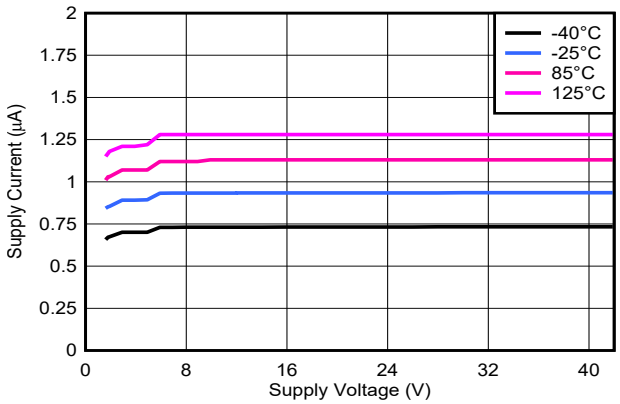
The TPS3842 is a 42V voltage supervisor with 850nA I_{DD} and 0.5% accuracy, and a fast detection time. This device can be connected directly to 12V / 24V voltage rail for continuous monitoring of undervoltage (UV) conditions. The TPS3842 comes in a small DRL package for size constraint applications. Built-in hysteresis on the SENSE pin prevents false reset signals when monitoring a supply voltage rail. 1%, 5%, and 10% hysteresis voltage options are available to offer design flexibility to support voltage transients.

SENSE is decoupled from VDD and can monitor higher and lower voltages than VDD. Fixed threshold variants provide accurate low-Iq voltage monitoring. Adjustable threshold variants offer flexible undervoltage threshold setting with external resistors. TPS3842 offers capacitor programable de-glitch on the SENSE with the CTS pin and capacitor programmable reset delay timing with the CTR pin.

Device Information

PART NUMBER	PACKAGE(1)	BODY SIZE (NOM) (2)
TPS3842	SOT563 (6)	1.20mm × 1.60mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Supply Voltage vs Supply Current

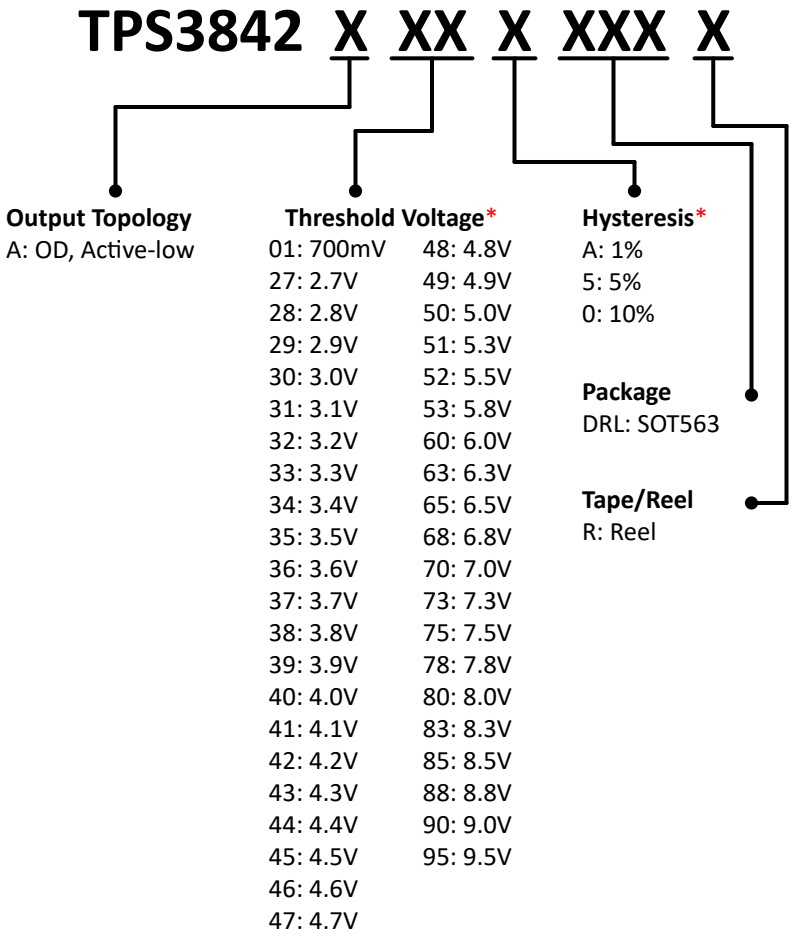
ADVANCE INFORMATION

ADVANCE INFORMATION

Table of Contents

4 Device Comparison

The following table shows the nominal rail to be monitored and the corresponding threshold voltage of the device.



OD – Open Drain output

* Refer 'Mechanical, Packaging and Orderable Information' section for list of released orderable. For any other orderable, contact local TI support.

1. Suffix 01 with V_{ITN} of 700mV corresponds to the adjustable variant, does not have internal voltage divider

ADVANCE INFORMATION

ADVANCE INFORMATION

5 Pin Configuration and Functions

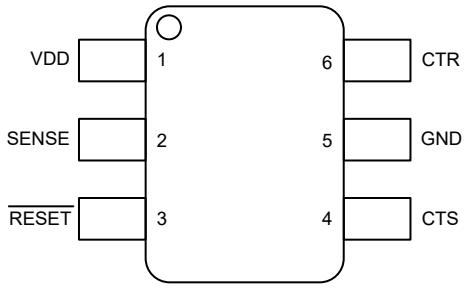


Figure 5-1. DRL Package
6-Pin SOT563
Top View

Table 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	SOT563		
V_{DD}	1	I	Supply voltage pin.
SENSE	2	I	Sense input. Monitors input voltage based on internal voltage threshold. See Section 8.3.1 for more details.
$\overline{\text{RESET}}$	3	O	Output reset signal. Connect $\overline{\text{RESET}}$ to pull up voltage using a pull up resistance.See Section 8.3.4 for more details.
CTS	4	I	Sense time delay: Capacitor programmable sense delay: CTS pin offers a user adjustable sense delay time when asserting a reset condition. See Section 8.3.2 for more details.
GND	5	—	Ground pin.
CTR	6	I	Reset output: User-programmable reset time delay for $\overline{\text{RESET}}$ pin. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section 8.3.3 for more details.

6 Specification

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	V_{DD}	–0.3	50	V
Voltage	V_{SENSE}	–0.3	50	V
Voltage	$V_{\overline{RESET}}$	–0.3	50	V
Voltage	V_{CTR}	–0.3	5.5	V
Voltage	V_{CTS}	–0.3	5.5	V
Current	$I_{\overline{RESET}}$		±40	mA
Temperature (2)	Operating junction temperature, T_J	-55	150	°C
	Operating free-air temperature, T_A	-55	150	°C
	Storage temperature, T_{stg}	-65	150	°C

(1) Stresses beyond values listed under Absolute Maximum Ratings can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
(2) As a result of the low dissipated power in this device, the operating temperature is assumed that $T_J = T_A$.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD}	Supply pin voltage	1.9		42	V
V_{SENSE}	Sense pin voltage	0		42	V
V_{CTR}	CTR pin voltage			5	V
V_{CTS}	CTS pin voltage			5	V
$V_{\overline{RESET}}$	Output pin voltage	0		42	V
$I_{\overline{RESET}}$	Output pin current	0		10	mA
T_J	Junction temperature (free-air temperature)	-40		125	℃

ADVANCE INFORMATION

6.4 Thermal Information

THERMAL METRIC[1]		TPS3842 DRL 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	153.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.9	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	41.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

6.5 Electrical Characteristics

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply Voltage		1.9		42	V
V_{POR}	Power on reset voltage(2)	V_{OL}(max) = 0.25V, I_{OUT} = 15µA			1.4	V
V_{ITN}	Negative-going threshold accuracy	Fixed internal threshold, V_{ITN} = 2.7V to 9.5V	-1.5	±0.5	1.5	%
V_{ITN}	Negative-going threshold accuracy	Adjustable internal threshold, V_{ITN} = 700mV	-1.5	±0.5	1.5	%
V_{HYS}	Hysteresis Voltage(1)	1% Variant	0.5	1	1.5	%
V_{HYS}	Hysteresis Voltage(1)	5% Variant	4.5	5	5.5	%
V_{HYS}	Hysteresis Voltage(1)	10% Variant	9.5	10	10.5	%
I_{DD}	Supply current	VDD = 12V, $\overline{RESET}$ = Not asserted		0.85	2.1	µA
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = V_{ITN}, Adjustable version	-25		25	nA
I_{SENSE}	Input current, SENSE pin	V_{SENSE} = 12V, Fixed versions		1.35	2.5	µA
V_{OL}	Low level output voltage	1.9V ≤ V_{DD} < 42V, I_{OUT} = 0.5mA			400	mV
I_{LKG}	Open drain output leakage current	V_{DD} = $V_{\overline{RESET}}$ = 12V			300	nA

(1) Hysteresis is with respect of the tripoint V_{ITN}.
(2) V_{POR} is the minimum V_{DD} voltage level for a controlled output state.

ADVANCE INFORMATION

ADVANCE INFORMATION

6.6 Timing Requirements

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

			MIN	NOM	MAX	UNIT
t_{PD}	Propagation detect delay(1) (2)	CTS = Open, ADJ V_{ITN}		10	20	µs
t_{PD}	Propagation detect delay(1) (2)	CTS = Open, Fixed V_{ITN}		10	20	µs
t_{CTS}	Sense time delay	CTR = 0.1uF		300		ms
$t_{GI\ (VITN)}$	Glitch Immunity undervoltage $V_{IT-(UV)}$, 20% Overdrive(1)	CTS = Open		5		µs

(1) 20% Overdrive from threshold. Overdrive % = [V_{SENSE} - V_{ITN}] / V_{ITN}
(2) t_{PD} measured from threhold trip point (V_{ITN}) to $\overline{RESET}$ V_{OL} voltage

6.7 Switching Characteristics

At 1.9V ≤ V_{DD} ≤ 42V, CTS = CTR = Open, $\overline{RESET}$ Voltage ($V_{\overline{RESET}}$) = 100kΩ to V_{DD}, $\overline{RESET}$ load = 50pF, and over the operating free-air temperature range of –40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C.

			MIN	NOM	MAX	UNIT
t_D	Reset time delay	CTR = Open		250		µs
t_{CTR}	Reset time delay	CTR = 0.1uF		300		ms
t_{CTR}	Reset time delay	CTR = 3.52uF		10		s
t_{SD}	Startup delay(1)			300		µs

(1) During the power-on sequence, V_{DD} must be at or above $V_{DD\ (MIN)}$ for at least t_{SD} + t_D + t_{CTR} before the output is in the correct state.

6.8 Timing Diagram

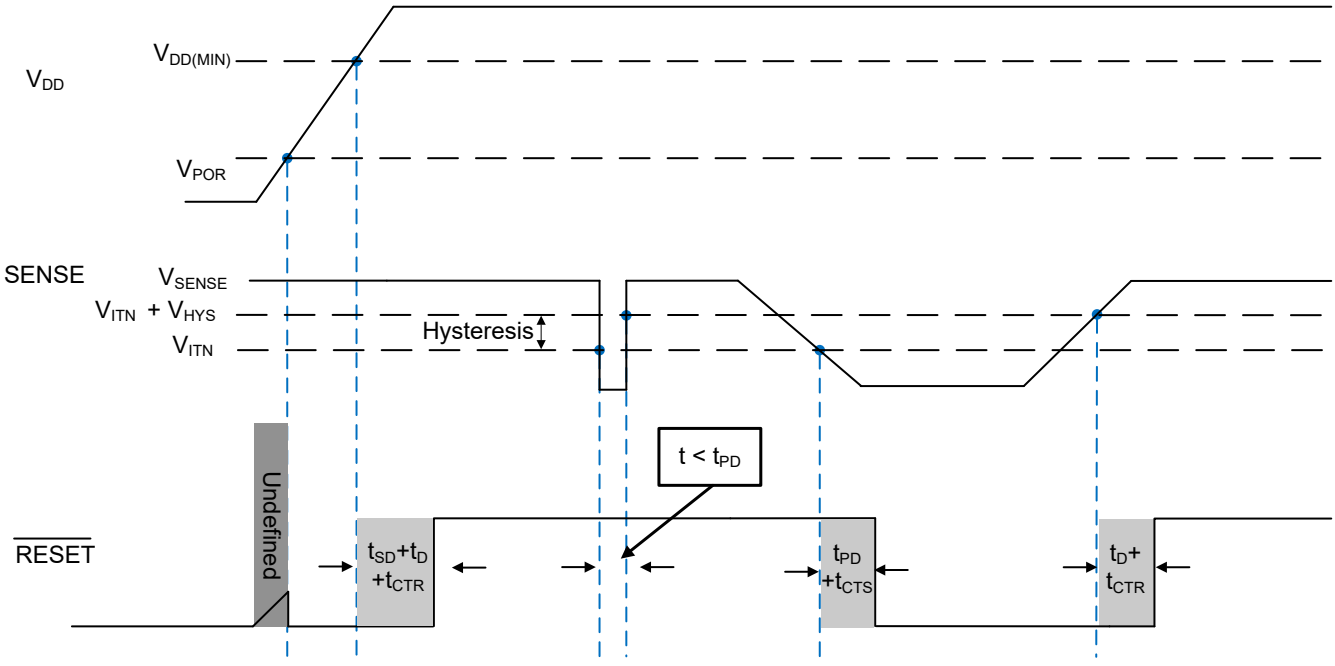


Figure 6-1. Timing Diagram

7 Typical Characteristics

At T_J = 25°C, V_{DD} = 3.3V, R_{LRESET} = 100kΩ, and C_{LRESET} = 50pF, unless otherwise noted.

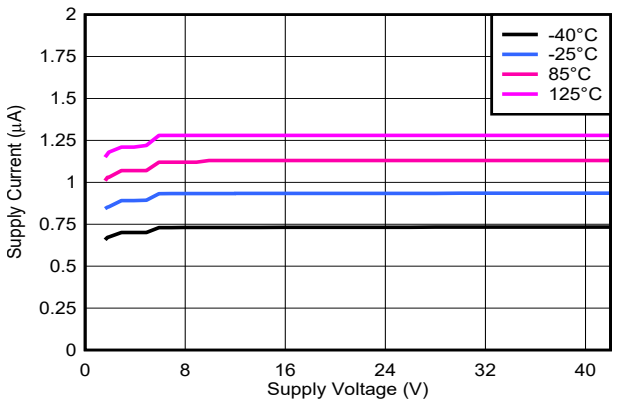


Figure 7-1. Supply Current vs Supply Voltage

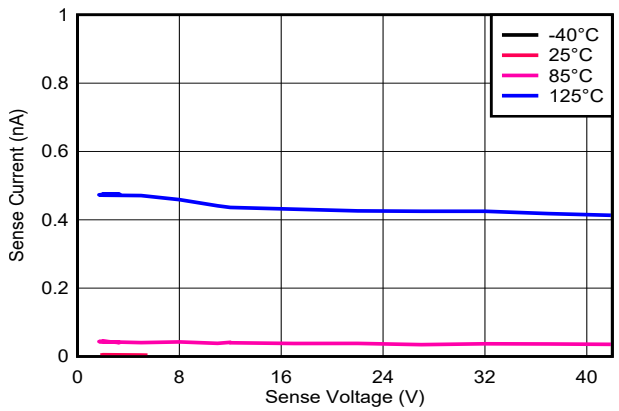


Figure 7-2. V_{SENSE} vs I_{SENSE} (V_{ITN} = 700mV)

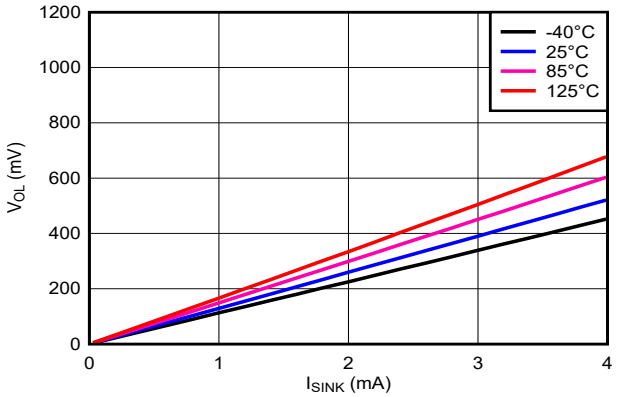


Figure 7-3. RESET Current vs V_{OL} (V_{DD} = 3.3V)

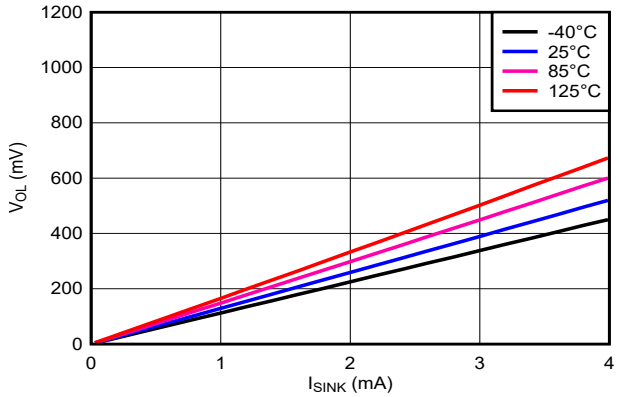


Figure 7-4. RESET Current vs V_{OL} (V_{DD} = 12V)

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TPS3842 high voltage supervisor product family is designed to assert a $\overline{\text{RESET}}$ signal when the SENSE pin voltage drops below V_{ITN} after a user-adjustable time. The $\overline{\text{RESET}}$ output remains asserted for a user-adjustable time after SENSE voltages returns above the respective threshold and hysteresis.

VDD, SENSE and $\overline{\text{RESET}}$ pins can support 42V continuous operation. Both VDD, SENSE, and $\overline{\text{RESET}}$ voltage levels can be independent of each other. The TPS3842-Q1 features capacitor programmable sense time delay (CTS) to set a minimum duration of a undervoltage event before $\overline{\text{RESET}}$ is asserted. CTS feature also functions as a programmable de-glitch to avoid false resets. The TPS3842-Q1 also features a capacitor programmable reset time delay (CTR) to set a minimum duration of $\overline{\text{RESET}}$ assertion after a undervoltage event.

8.2 Functional Block Diagrams

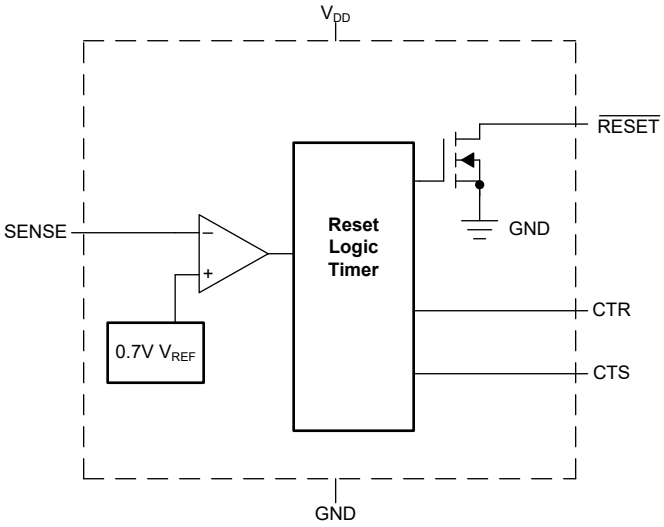


Figure 8-1. Adjustable-Voltage Version

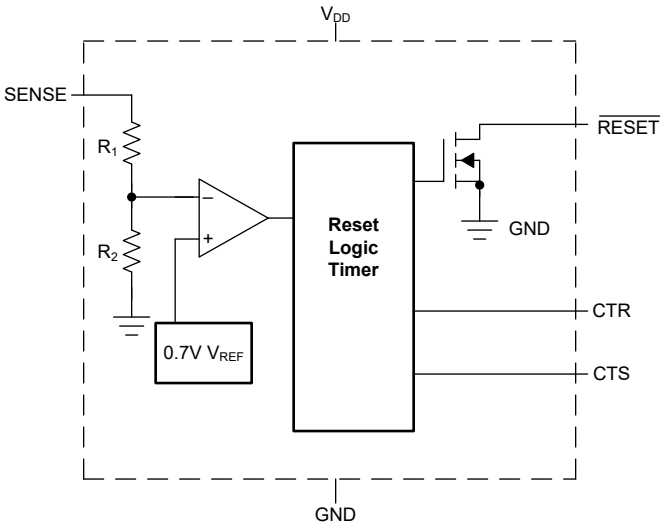


Figure 8-2. Fixed-Voltage Version

8.3 Feature Description

A broad range of voltage threshold and hysteresis options are available for the TPS3842, allowing this device to be used in a wide array of applications. Reset threshold voltages can be factory-set from adjustable 0.7V or fixed from 2.7V to 9.5V. The adjustable variant can be set to any voltage above 0.7V using an external resistor divider. Connecting a capacitor between C_{TR} and GND allows the designer to select any reset delay period up to 10s. Connecting a capacitor between CTS and GND allows the designer to select any sense delay period up to 10s.

8.3.1 SENSE Input

The SENSE input provides a pin at which any system voltage can be monitored. If the voltage on this pin drops below V_{ITN} for a T_{PD}+T_{CTS} time interval, then $\overline{RESET}$ is asserted. The comparator has a built-in hysteresis to suppress unintended $\overline{RESET}$ assertions and de-assertions. For noisy envirionments, good analog design practice is to put a 1nF bypass capacitor on the SENSE input to reduce sensitivity to transients and layout parasitics or leaverage the CTS feature to set a minimum fault time interval before $\overline{RESET}$ is asserted.

Figure 8-3 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 700mV threshold option when using an external resistor divider. The variant bypasses the internal resistor ladder for higher accuracy when using external resistors.

For example, consider a 12V rail, V_{MON}, being monitored for undervoltage (UV) using of the TPS3842A011DRLR variant, as shown in Figure 8-3. The monitored UV threshold, denoted as V_{MON-}, is the desired voltage where the device asserts the reset. For this example V_{MON-} = 5.8V. To assert an undervoltage reset the voltage at the sense pin, V_{SENSE}, needs to be equal to the input threshold negative, V_{ITN}. For this example variant V_{SENSE} = V_{ITN} = 0.7V. Using R_1 and R_2 the correlation between V_{MON-} and V_{SENSE} can be seen in Equation 1. Assuming R_2 = 100kΩ, and R_1 can be calculated as R_1 = 16kΩ.

$$V_{SENSE} = V_{MON-} \times (R_2 \div (R_1 + R_2)) \quad (1)$$

The TPS3842 hysteresis depends on the configuration selected. For the reset signal to become deasserted, V_{MON} must go above V_{ITN} + V_{HYS}. For this example variant a 1% voltage threshold hysteresis was selected. Therefore, V_{MON} equals 5.858V when the reset signal becomes deasserted. If a 10% hysteresis option was instead used, V_{MON} equals 6.38V when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that can affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance (R_{SENSE}) can be calculated by the SENSE voltage (V_{SENSE}) divided by the SENSE current (I_{SENSE}) as shown in Equation 3. V_{SENSE} can be calculated using Equation 1 depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using Equation 2.

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (2)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (3)$$

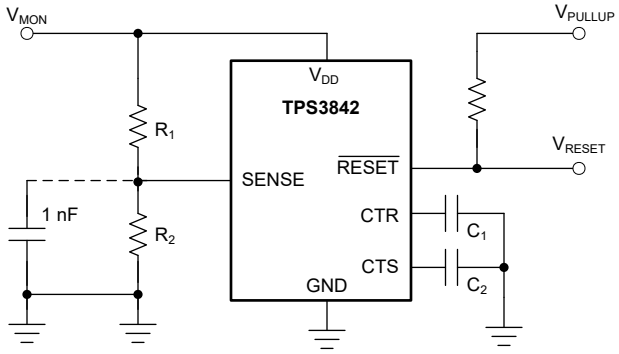


Figure 8-3. Using the TPS3842A011DRLR to Monitor a User-Defined Threshold Voltage

8.3.1.1 SENSE Hysteresis

TPS3842 device offers built-in hysteresis around the UV threshold to avoid erroneous $\overline{\text{RESET}}$ deassert. The hysteresis (V_{HYS}) is opposite to the threshold voltage for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

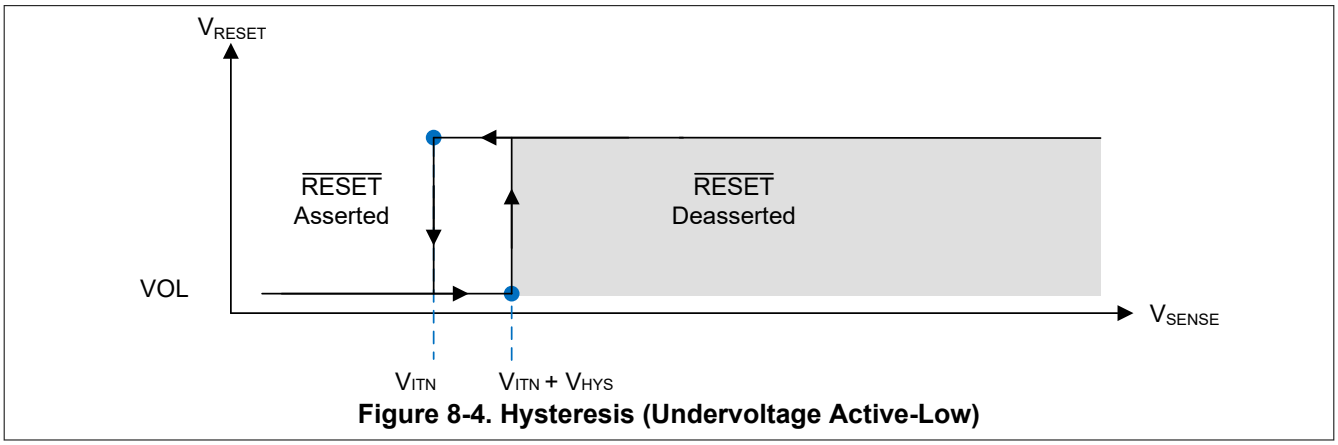


Figure 8-4. Hysteresis (Undervoltage Active-Low)

Table 8-1. Common Adjustable Hysteresis Lookup Table

Part Number	DEVICE HYSTERESIS OPTION
TPS3842Axx**1**DRLR	1%
TPS3842Axx**5**DRLR	5%
TPS3842Axx**0**DRLR	10%

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is (V_{ITN} + V_{HYS}). Hysteresis is dependent on the device V_{ITN} including V_{ITN} accuracy and deviations.

Undervoltage (UV)

V_{ITN} = 700mV

Voltage Hysteresis (V_{HYS}) = 1% = V_{ITN} x 1% = 7mV

Hysteresis Accuracy = +0.5% to +1.5% = 6.65mV to 7.105mV

Release Voltage = V_{ITN} + V_{HYS} = 706.65mV to 707.105mV

8.3.2 Selecting the SENSE Delay Time

TPS3842 has adjustable sense time delay with external capacitors.

- A capacitor on CTS programs the excursion detection on SENSE.
- No capacitor on this pin gives the fastest sense delay time indicated by t_{PD} in Section 6.6.
- Parasitic capacitance on the CTS pin counts as CTS capacitance and increases T_{CTS}.

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS\_EXT\ (typ)}$ and the time delay $t_{CTS\ (typ)}$ is given by Equation 4.

$$t_{CTS\ (typ)} = 2.858 \times C_{CTS\_EXT\ (typ)} \quad (4)$$

$C_{CTS\_EXT\ (typ)}$ = is given in microfarads (µF)

The sense delay varies according to the external capacitor (C_{CTS_EXT}). The minimum and maximum variance due to the constant is show in Equation 5 and Equation 6:

$$t_{CTS\ (max)} = 3.715 \times C_{CTS\_EXT\ (max)} \quad (5)$$

$$t_{CTS\ (min)} = 2 \times C_{CTS\_EXT\ (min)} \quad (6)$$

There is no limit to the capacitor on CTS pin. Make sure there is enough time for the capacitor to fully discharge when a voltage fault occurs to prevent the CTS capacitor from having charge before the next fault. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the internal circuit to trip earlier or later near the threshold.

* Leakages on the capacitor can effect accuracy of sense time delay.

ADVANCE INFORMATION

8.3.3 Selecting the RESET Delay Time

TPS3842 has adjustable reset release time delay with external capacitors.

- A capacitor on CTR programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time indicated by t_D in Section 6.7.
- Parasitic capacitance on the CTR pin counts as CTR capacitance and increases t_{CTR}.

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR pin and GND.

The relationship between external capacitor $C_{CTR\_EXT\ (typ)}$ and the time delay $t_{CTR\ (typ)}$ is given by Equation 7.

$$t_{CTR\ (typ)} = 2.858 \times C_{CTR\_EXT\ (typ)} \quad (7)$$

$C_{CTR\_EXT\ (typ)}$ = is given in microfarads (µF)

The reset delay varies according to the external capacitor (C_{CTR_EXT}). The minimum and maximum variance due to the constant is show in Equation 8 and Equation 9:

$$t_{CTR\ (max)} = 3.715 \times C_{CTR\_EXT\ (max)} \quad (8)$$

$$t_{CTR\ (min)} = 2 \times C_{CTR\_EXT\ (min)} \quad (9)$$

There is no limit to the capacitor on CTR pin. Having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold $\overline{\text{RESET}}$ active.

* Leakages on the capacitor can effect accuracy of reset time delay.

8.3.4 RESET Output

$\overline{\text{RESET}}$ (active low) denoted with a bar above the pin label. $\overline{\text{RESET}}$ remains high voltage (V_{OH}, deasserted) (open-drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation above the threshold boundary and VDD voltage is above VDD(min). If SENSE falls below V_{ITN} for a time period longer than t_{PD}+t_{CTS}, $\overline{\text{RESET}}$ is asserted, driving the $\overline{\text{RESET}}$ pin to a low impedance.

Once SENSE is above V_{ITN} + V_{HYS}, a delay circuit (CTR) is enabled that holds $\overline{\text{RESET}}$ low for a specified reset delay period. Once the reset delay has expired, the $\overline{\text{RESET}}$ pin goes to a high impedance state.

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels. $\overline{\text{RESET}}$ is supports pull-up voltages up to 42V and is independent of VDD and SENSE voltages.

To select the right pull-up resistor, consider system V_{OH} and the Open-Drain Leakage Current (I_{LKG}) provided in the electrical characteristics to set the maximum pull-up resistor value. Low pull-up resistor values increase the amount of current through the internal open-drain output. The current through the open-drain output must be lower than the $I_{\overline{\text{RESET}}}$ of the device.

ADVANCE INFORMATION

8.4 Device Functional Modes

Table 8-2. Truth Table

SENSE > V_{ITN}	$\overline{RESET}$	VDD
0	L	VDD > VDD(min)
1	H	VDD > VDD(min)
0	L	VDD(min) > VDD > V_{POR}
1	L	VDD(min) > VDD > V_{POR}

8.4.1 Normal Operation (V_{DD} > $V_{DD(min)}$)

When V_{DD} is greater than $V_{DD(min)}$, the $\overline{RESET}$ signal is determined by the voltage on the SENSE pin.

- The $\overline{RESET}$ signal corresponds to the voltage on SENSE relative to V_{ITN}.

8.4.2 Above Power-On Reset but Less Than $V_{DD(min)}$ (V_{POR} < V_{DD} < $V_{DD(min)}$)

When the voltage on V_{DD} is less than the device $V_{DD(min)}$ voltage, and greater than the power-on reset voltage (V_{POR}), the $\overline{RESET}$ signal is asserted and low impedance regardless of the voltage on the SENSE pin.

8.4.3 Below Power-On Reset (V_{DD} < V_{POR})

When the voltage on V_{DD} is lower than the required voltage (V_{POR}) needed to internally pull the asserted output to GND, $\overline{RESET}$ is undefined.

ADVANCE INFORMATION

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

9.2 Typical Application

A typical application of the TPS3842 used to monitor a 12V power rail is shown in Figure 9-1. The open-drain $\overline{\text{RESET}}$ output is typically connected to the $\overline{\text{RESET}}$ input of a microprocessor. A pullup resistor must be used to hold this line high when $\overline{\text{RESET}}$ is not asserted. The $\overline{\text{RESET}}$ output is undefined for voltage below V_{POR}, but this characteristic is normally not a problem because most microprocessors do not function below this voltage.

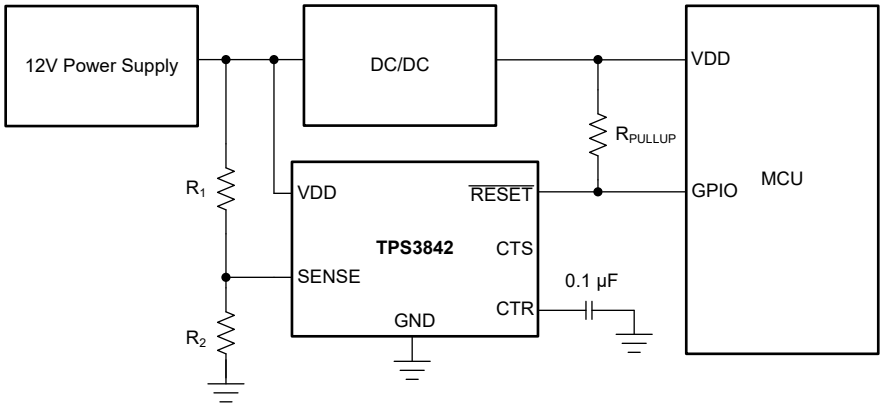


Figure 9-1. Typical Application of the TPS3842 Monitoring a 12V Power Supply

9.2.1 Design Requirements

Table 9-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Voltage Threshold	Typical UV voltage threshold 9.5V
Output logic	Open-Drain
SENSE delay	< 0.2ms
$\overline{\text{RESET}}$ delay	300ms

9.2.2 Detailed Design Procedure

The TPS3842 utilizes high-voltage SENSE and V_{DD} inputs to monitor a 12V power supply for undervoltage. In this design example TPS3842A011DRLR is used.

The negative-going threshold voltage, V_{ITN}, is set by the device variant. In this example, the nominal supply voltage from the power supply is 12V. Setting a undervoltage threshold of 9.5V (approximately 20% under 12V) makes sure that the device resets before supply voltage violates the allowed boundary. The adjustable voltage variant is chosen and R_1 and R_2 are adjusted to meet the threshold. Assuming R_2 equal to 10kΩ and R_1 is calculated as 125kΩ. For additional information on selecting resistor values see Section 8.3.1. TPS3842 also supports fixed voltage threshold variants. Threshold voltage decoding can be found in Device Decoder.

9.2.2.1 Meeting the Sense and Reset Delay

The TPS3842 features both reset assertion (sense) delay, t_{CTS}, and reset deassertion (reset) delay, t_{CTR}. Section 8.3.2 and Section 8.3.3 show how to set the timings for the capacitor-programmable delays. The application requires less than 0.2ms sense delay, thus no capacitor is used and CTS is left open. The application requires greater than 300ms reset delay, thus a 0.1µF capacitor is used.

9.2.3 Application Curve

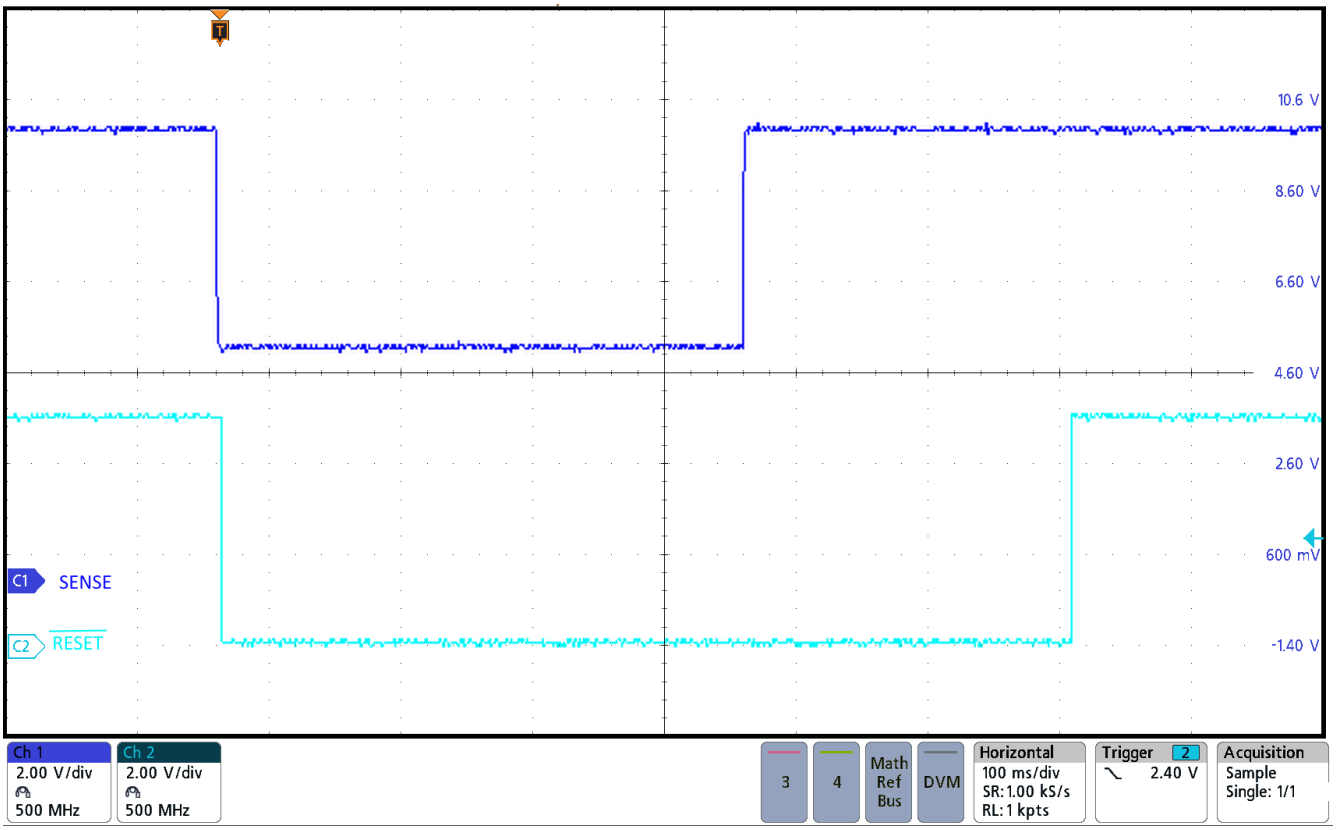


Figure 9-2. TPS3842 Detecting Undervoltage Fault and $\overline{\text{RESET}}$ Recovery

9.2.4 Power Supply Recommendations

TPS3842 is designed to operate from an input supply with a V_{DD} voltage between 1.9V (minimum operation) to 42V (maximum operation). Good analog design practice recommends placing a minimum 0.1µF ceramic capacitor as near as possible to the V_{DD} pin.

9.2.5 Layout

9.2.5.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1µF ceramic capacitor as near as possible to the VDD pin.
- For noisy envirionments and to improve noise immunity on the SENSE pins, an optional 1nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal. An alternative to improve noise immunity is to use the CTS feature.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance to not affect the T_{PD} or t_{CTR}.
- Place the pull-up resistors on $\overline{\text{RESET}}$ as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible.

ADVANCE INFORMATION

- Do not have high voltage metal pads or traces closer than 20mils (0.5mm) to the low voltage metal pads or traces.

9.2.5.2 Layout Example

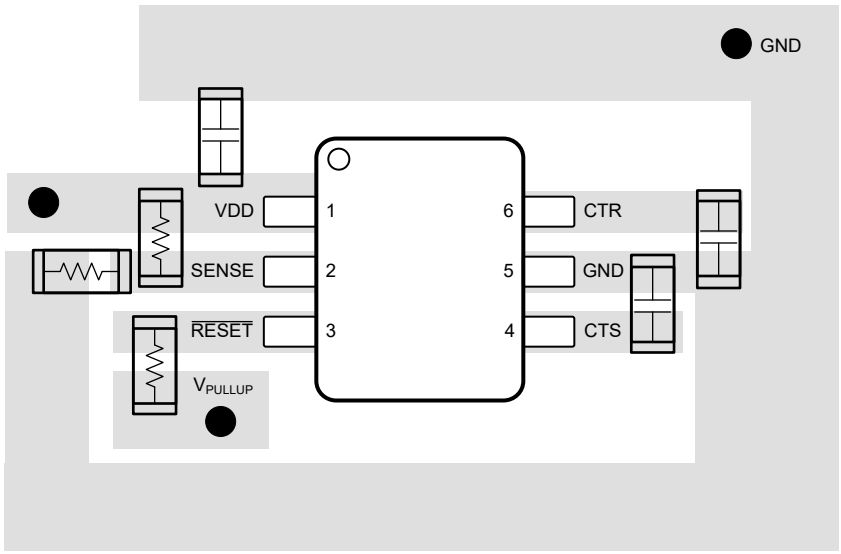


Figure 9-3. TPS3842 Reccomended Layout

ADVANCE INFORMATION

10 Device and Documentation Support

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

10.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTPS3842A011DRLR	ACTIVE	SOT-5X3	DRL	6	4000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

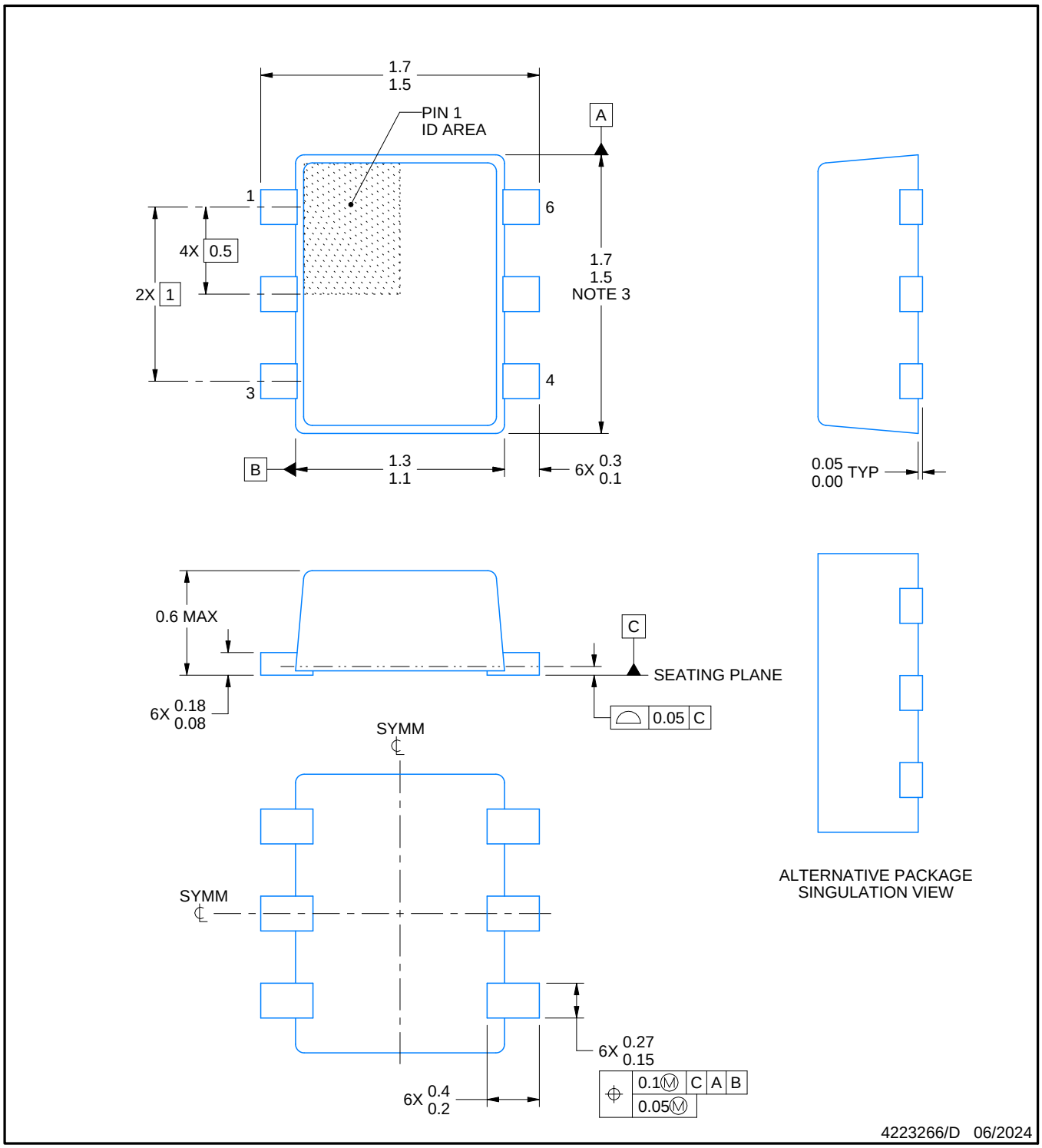
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS3842 :

- Automotive : TPS3842-Q1

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



NOTES:

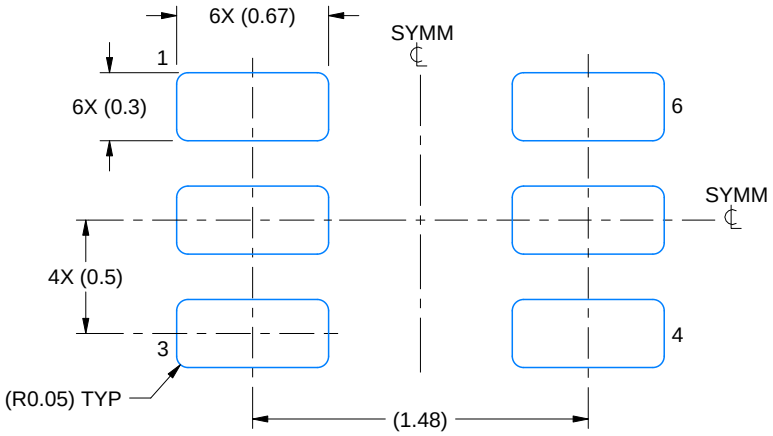
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

EXAMPLE BOARD LAYOUT

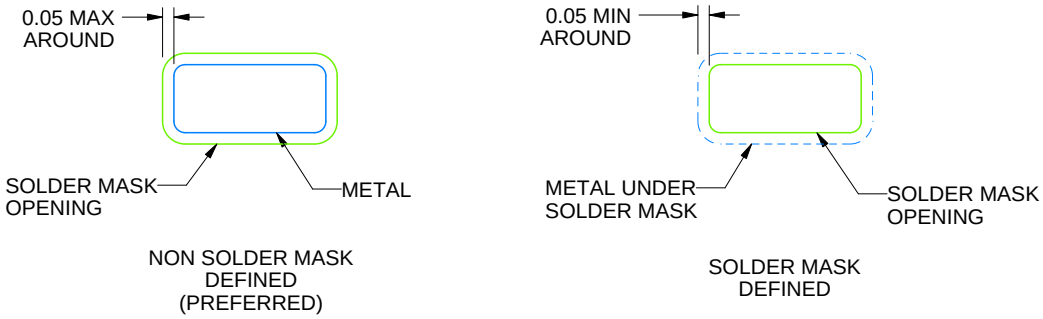
DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:30X



SOLDERMASK DETAILS

4223266/D 06/2024

NOTES: (continued)

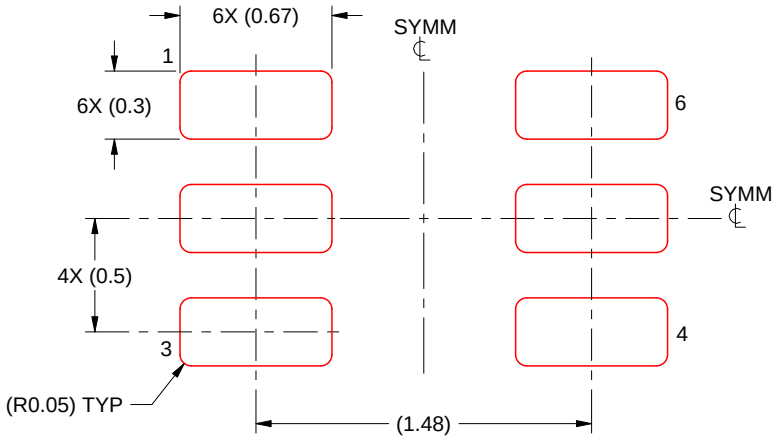
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4223266/D 06/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265