Application Report
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Hardware Design Guidelines for TMS320F28xx and TMS320F28xxx DSCs

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ABSTRACT

TMS320F28xx and F28xxx digital signal controllers (DSCs) include multiple complex peripherals running at fairly high-clock frequencies. They are commonly connected to low level analog signals using an onboard analog-to-digital converter (ADC). This application report is organized as a guide for system level hardware design, parts selection, and schematics design to board layout and helps in avoiding those hardware errors that become costly and time consuming when detected during the system level-debugging phase of the project, using the prototype of the custom board of the project. The issues related to clock generation, JTAG, power supply, interfacing of peripherals with special attention to analog inputs to ADC, general-purpose input/output (GPIO) connections, testing and debug, electromagnetic interference (EMI) and electromagnetic compatibility (EMC) considerations, and so forth are discussed. Each section explains signal routing and layout tips.

WARNING

This document only applies to the families F281x, F280x, F2801x, F28044, F2823x, and F2833x. It does not apply to the F2802x, F2803x, F2805x, F2806x, F28M3x, F2837x, or F2807x families of devices.

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1 Introduction

Digital signal processing (DSP) devices currently have higher central processing unit (CPU) performance (clock rates over 100 MHz) and integration of advanced high-speed peripherals. Great strides have been made in DSP power reduction through CMOS process technology. These advances have increased the complexity of the DSP board design, which provide more analog challenges than a simple digital design. Some of the examples of these challenges are: board traces can become transmission lines, floating unused device pins can consume unnecessary power, and different core and input/output (I/O) voltages need power management techniques.

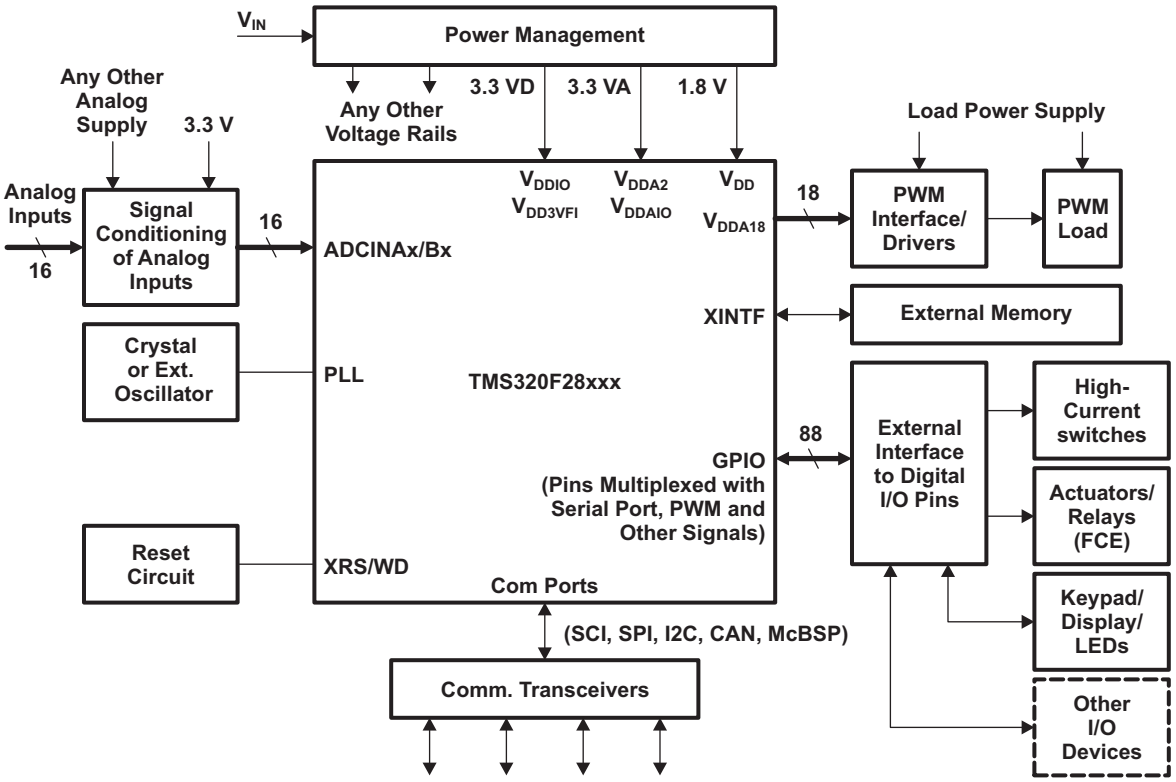
The TMS320F28xx and TMS320F28xxx are members of the C2000™ DSP generation used for embedded control applications. The current products run at a CPU frequency up to 150 MHz; future devices in the family may push this frequency upwards. The CPU frequencies of these devices fall in the radio frequency range. There is also a need to create a design that is *debug* friendly. How can designers access pins on the Ball Grid Array (BGA) packages? What can system designers do at the design stage to help isolate pieces of the board for debug? And even after the board design is completed, there is a need to have a methodical approach for system debug.

This application report discusses the topics starting from clock circuit, JTAG, interfacing with typical external devices, power supply and related requirements, thermal considerations, debugging, layout and EMI. The parts selection is also discussed as applicable. Various questions sent by TI's customers to the Central Support Team formed a good base for this document.

NOTE: The current revisions of all device-specific data manuals take precedence over the information/data in this report.

2 Typical System and Challenges

A typical C2000-based control or data acquisition system is shown in Figure 1. Normally, it is powered from the AC mains output; however, in some applications it is powered from a battery. Typically, the DSC is surrounded by power management circuits, reset/clock generator, signal conditioning circuits (for analog inputs using op-amps), driver circuits for control output with pulse width modulation (PWM), user interface, transceivers on serial communication ports, external memory, or other devices with parallel interface over XINTF or serial Flash over inter-integrated circuit (I2C), and other supporting circuitry.



A External interface (XINTF) is available on the F2812 and F2833x devices only

B The maximum number of signals for any interface is device dependent.

Figure 1. Typical TMS320F28xx/28xxx System

TMS320F28xx/F28xxx devices include various onboard peripheral blocks. Though these peripherals save adding external interface parts and make it flexible to meet the system level requirements for different applications, it is challenging to design the hardware to operate all these peripherals and the DSC to achieve the highest performance with optimum reliability. Therefore, designing a custom board, which should work as desired on the first attempt, is a real challenge.

With the CPU frequency up to 150 MHz, there are many internal functional blocks onboard operating at various frequencies. Any signal above 10 MHz can create a signal integrity issue if proper care is not taken during schematics and layout design. In addition, there are low-level analog signals on the same board. EMI/EMC and electrical noise issues should be considered before starting the board design. Overall design must be debug friendly.

NOTE: This report considers the families TMS320F281x, F280x, F280xx and F2833x which are active parts at the time of publication. Future revisions will include the data on newer parts.

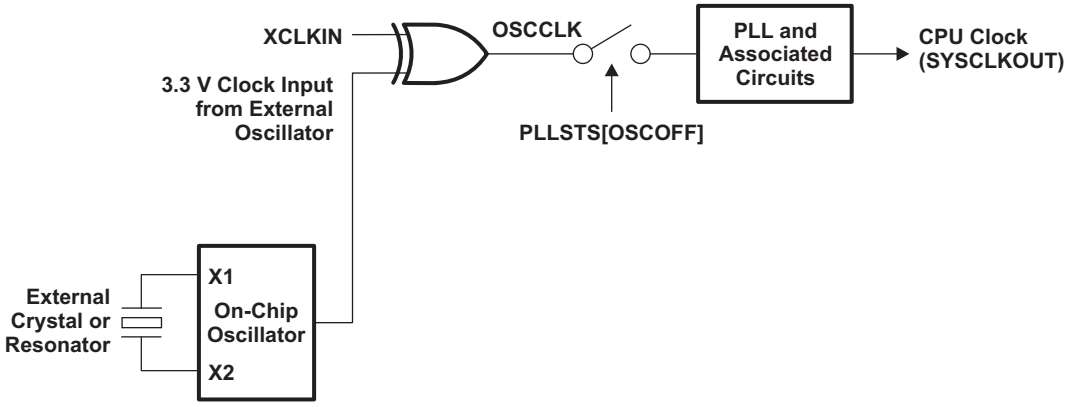
3 Handling of Different Hardware Building Blocks

The following sections discuss each building block of the entire design.

3.1 Clocking Circuit

The F28x devices offer two options for clock generation: using an onboard crystal oscillator or feeding the external clock to the XCLKIN pin. The frequency of this basic input clock, using an internal oscillator, is in the range of 20 MHz – 35 MHz. The on-chip phase-locked loop (PLL) can be set to multiply the input clock to provide a wide variety of system clock frequencies. Each time you write to the PLLCR register to configure the PLL multiplier, the PLL will take 131,072 cycles to lock. While the PLL is in the process of locking, the device frequency may experience a large swing at the start and end of the locking process. These two potentially abrupt frequency transitions may cause power rail fluctuations. Careful design of the power-supply is needed in order to prevent these transitions from impacting the device operation. Once the PLLCR register is written to, it is recommended that a tight loop be executed until the PLL relocks to the new frequency. Once the PLLCR is written to, writing to the PLLCR again, even with the same multiplier will cause these frequency swings and potential power supply swings. The frequency of the external clock fed to the CLKIN pin can be as high as the maximum frequency at which the CPU can operate (SYSCLKOUT). The CPU can operate within the wider range of that frequency. Further clock signals for all the peripherals are derived from the CPU clock.

In general, the highest possible frequency for the clock signal is selected to achieve maximum execution speed. However, the other aspect is power consumption because it increases linearly with the CPU clock frequency. For more information regarding the current/power consumption graphs, see the Electrical Specifications sections in the *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812, Digital Signal Processors Data Manual* (SPRS174), *TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2802, TMS320C2801, and TMS320F2801x DSPs Data Manual* (SPRS230), *TMS320F28044 Digital Signal Processor* (SPRS357), and the *TMS320F28335, TMS320F28334, TMS320F28332 Digital Signal Controllers (DSCs) Data Manual* (SPRS439).



A The F281x parts have a common pin for the X1 and XCLKIN signals.

Figure 2. Options for Clock Input

3.1.1 Internal (Crystal/Resonator) vs. External Oscillator

The first consideration for the clock generation circuit is whether to use the on-chip oscillator (crystal or resonator) or an external clock source, from an external oscillator or any other source in the system.

A primary concern of this choice is often cost; a crystal and its few associated components used with the internal oscillator are usually cheaper than an external oscillator. Therefore, using a crystal, along with the internal device oscillator circuit may be a good option, unless the same clock must be provided to other devices in the system. Since making any additional connections to the crystal circuit is not recommended, the only choice would be to use F28xx clock output (XCLKOUT) signal or to generate it using a PWM block to clock other devices in the system. However, the DSP is not usually run at the crystal frequency, so if other devices in the system require this same clock, using an external oscillator is simpler and generally the preferred approach.

3.1.1.1 Using Crystal/Resonator as Clock Source

The on-chip oscillator circuit of all the F28xx/F28xxx devices enables a crystal/resonator connected to the X1 and X2 pins. The X1 pin is referenced to the core digital power supply (V_{DD}). The X2 pin is the internal oscillator output. The crystal is connected across the X1 and X2 pins. If the X2 pin is not used, it must be left open. The F281x devices have a common pin for the X1 and XCLKIN signals.

Figure 3 shows the external circuitry and connections required for using the internal oscillator, along with the equation defining the relationship between the manufacturer's specified crystal load capacitance C_{LOAD}, formed by two external capacitors C1 and C2. The external clock mode control inputs specify whether the internal oscillator is enabled or disabled. When the internal oscillator is used, choose the clock-mode selection that enables the internal oscillator.

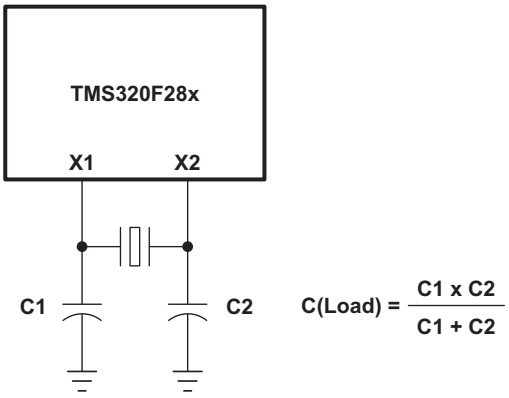


Figure 3. Typical Crystal Circuit

The effective load capacitance, C_{LOAD}, appears to the crystal circuit as the series combination of C1 and C2. Correct C_{LOAD} is important for proper operating frequency. Crystals are available with a variety of C_{LOAD} values. However, the internal DSC oscillator will not start and run reliably with too high or too low of a C_{LOAD} value. For more information, check the specifications from the crystal vendor's data sheets. It is recommended to select a fundamental mode parallel resonant type crystal having a C_{LOAD} of around 12 pF and ESR of 30 to 60 Ω.

The actual discrete values required for C1 and C2 are generally up to 5 pf below the calculated load capacitance due to PCB traces and the DSC input pin's stray capacitances; the board layout is quite important. If precise frequency control is required, the exact discrete capacitor values can be determined by varying the capacitor values and performing precision frequency measurements using a frequency counter.

NOTE: It is recommended that you have the resonator/crystal vendor characterize the operation of their device with the DSC chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise you regarding the proper tank component values for proper start-up and stability over the entire operating range.

3.1.1.2 Using External Oscillator

To select a proper external oscillator, consider the specifications such as frequency, stability, aging, voltage sensitivity, rise and fall time, duty cycle, and signal levels. Some designs may have to consider clock jitter. Note that only F280x and F28xxx devices can accept an external clock signal having an amplitude of V_{DD} (1.8 V/1.9 V) or 3.3 V. The clock signal for F281x parts should toggle between 0 and V_{DD}.

Connect the output of the external oscillator to the F280x and F28xxx parts as shown in Figure 4, based upon the level. It is important to connect X1 or XCLKIN to ground as shown. If they are left open, the frequency of CLKOUT will be incorrect and the DSC may not work properly.

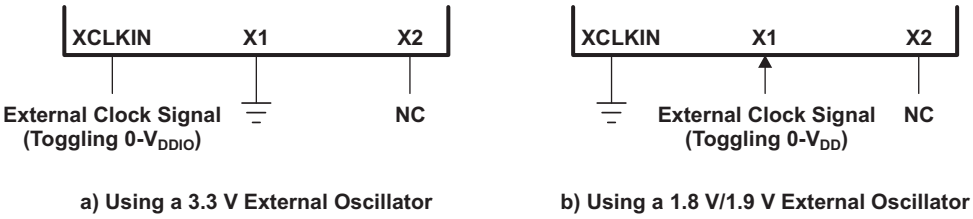


Figure 4. Connecting External Oscillator to F280x/F28xxx

The F281x devices select the external clock oscillator part that toggles between 0 - V_{DD} (0 – 1.8 V/1.9V).

NOTE: If you are using a 3.3 V external oscillator for an F281x system, use a 3.3 V to 1.8 V/1.9 V voltage translator device equivalent to TI's SN74LVC1G14 - *SN74LVC1G14 Single Schmitt-Trigger Inverter Data Sheet* (SCES218) .

3.1.2 Loss of Input Clock - Limp Mode

The PLL still issues a limp-mode clock if the input clock, OSCCLK, is removed or absent. The limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1 MHz - 5 MHz. Limp mode is not specified to work from power-up, but only after input clocks have been present. In PLL bypass mode, the limp mode clock from the PLL is automatically routed to the CPU if the input clock is removed or absent. The watchdog counter stops decrementing with the failure of the input clock and does not change with the limp-mode clock. These conditions could be used by the application firmware to detect the input clock failure and initiate a necessary shut-down procedure for the system.

NOTE: Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the DSC is held in reset should the input clocks ever fail. For example, an R-C circuit can be used to trigger the $\overline{XRS}$ pin of the DSC, should the capacitor ever get fully charged. An I/O pin can be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the Flash memory and the V_{DD3VFL} rail.

3.1.3 XCLKOUT

The output clock signal, derived from SYSCLKOUT, is available on XCLKOUT as a general-purpose clock source, which can be used for external wait-state generation. It also serves as a Test Point to check the CPU clock frequency and to ensure that the PLL is working properly. At reset, XCLKOUT = SYSCLKOUT/4; but it can be set the same as or ½ of SYSCLKOUT.

The XCLKOUT signal is active when reset is active. Since XCLKOUT should reflect SYSCLKOUT/4 when reset is low, you can monitor this signal to detect if the device is being properly clocked during debug. There is no internal pullup or pulldown on the XCLKOUT pin. The drive strength of this pin is 8 mA. If XCLKOUT is not being used, it can be turned off by setting the CLKOFF bit to 1 in the XINTF Configuration Register (XINTCNF2). This is an *output* pin of the CMOS device and should not be terminated to ground even if it is not used.

3.2 Reset and Watchdog

The $\overline{XRS}$ pin facilitates the device reset (in) and watchdog reset (out) signals. A warm reset pulse-width is specified as eight times the oscillator clock (OSCCLK) period; however, the power on reset's pulse-width has to be much longer to account for the time required for V_{DD} to reach 1.5 V (to enhance Flash reliability) and the oscillator start-up period of 10 mS (nominal). You may prefer to keep this duration in excess of 100 ms to overcome any other related delays.

During power down, the $\overline{XRS}$ pin must be pulled low at least 8 μs prior to V_{DD} reaching 1.5 V to enhance Flash reliability.

Whenever the 8-bit watchdog up counter has reached its maximum value, the watchdog module generates an output pulse 512 oscillator clocks wide. Note that the $\overline{WDRST}$ signal outputs the reset signal over the $\overline{XRS}$ pin. The output buffer of this pin is an open-drain with an internal pullup (100 uA, typical); it is recommended that the open-drain device drive this pin. Figure 5 illustrates a block diagram of the watchdog module.

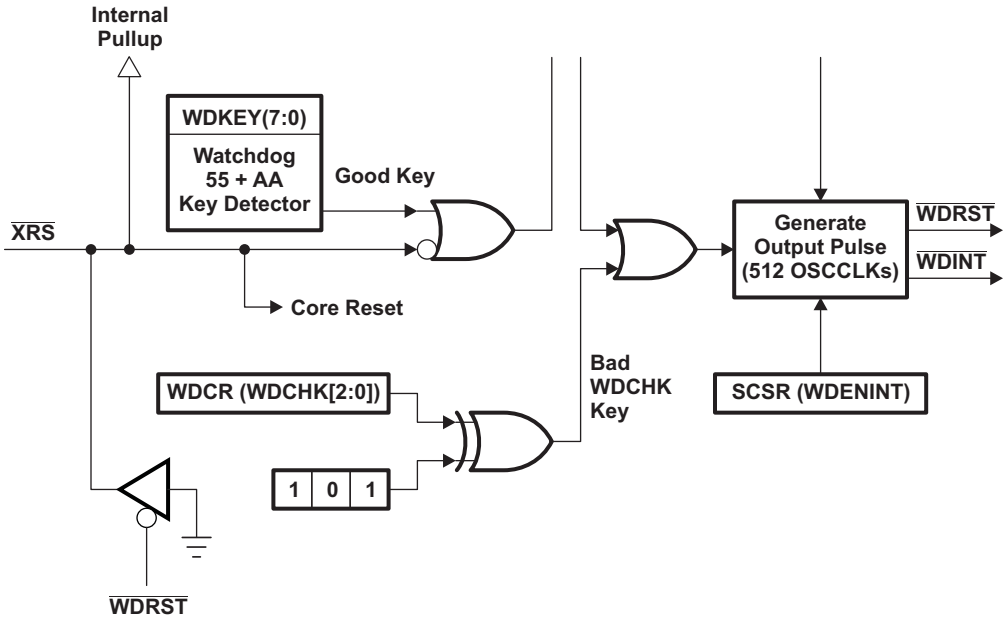


Figure 5. XRS Connection With Watchdog Module

For the $\overline{XRS}$ pin, simple R-C filters are often adequate. However, ESD protection diodes like CM1215 may offer better protection. For more information, see https://www.onsemi.com/pub/Collateral/CM1215-D.PDF.

3.3 Debug interface/JTAG and EMU Signals

For target-level debug interface, all F28xx/F28xxx devices use five of the standard IEEE Standard 1149.1–1990, IEEE Standard Test Access Port and Boundary-Scan Architecture (JTAG) signals ($\overline{\text{TRST}}$, TCK, TMS, TDI, and TDO) and two of the TI extensions (EMU0 and EMU1).

The pin assignment for the JTAG header is defined in Figure 6.

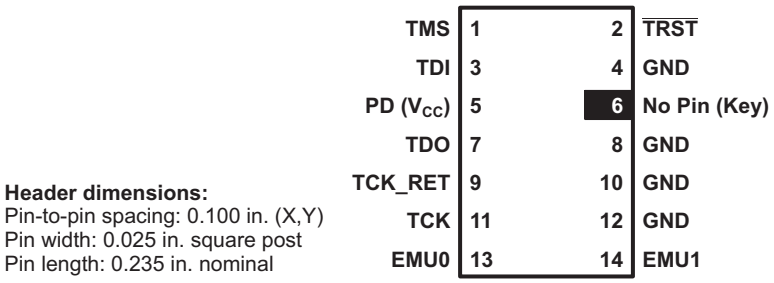


Figure 6. JTAG Header to Interface Target to a Scan Controller

As shown in Figure 6, the header requires more than the five JTAG signals and TI extensions. It also requires a test clock return signal (TCK_RET), target supply (V_{CC}), and ground (GND). TCK_RET is a test clock out of the scan controller and into the target system. The target system uses TCK_RET if it does not supply its own test clock, in which case TCK simply would not be used In many target systems. TCK_RET is connected to TCK and used as the test clock.

The drive strength of TDO, EMU0 and EMU1 pins is 8 mA.

The JTAG connector should be placed within 6 inches or less (preferably 2") from the corresponding pins on the DSC. If this is not possible, signal buffers should be added.

The pin descriptions are shown in Table 1.

Table 1. 14-Pin JTAG Header Signal Descriptions

Signal	Descriptions	Emulator State	Target State
EMU0	Emulation pin 0	I	I/O
EMU1	Emulation pin 1	I	I/O
GND	Ground		
PD (V_{CC})	Presence detect. This signal indicates that the emulation cable is connected and that the target is powered up. PD should be tied to V_{CC} in the target system.	I	O
TCK	Test clock. TCK is a clock source from the emulation cable pod. This signal can be used to drive the system test clock.	O	I
TCK_RET	Test clock return. Test clock input to the emulator. This signal can be a buffered or unbuffered version of TCK.	I	O
TDI	Test data input	O	I
TDO	Test data output	I	O
TMS	Test mode select	O	I
$\overline{\text{TRST}}$	Test reset	O	O

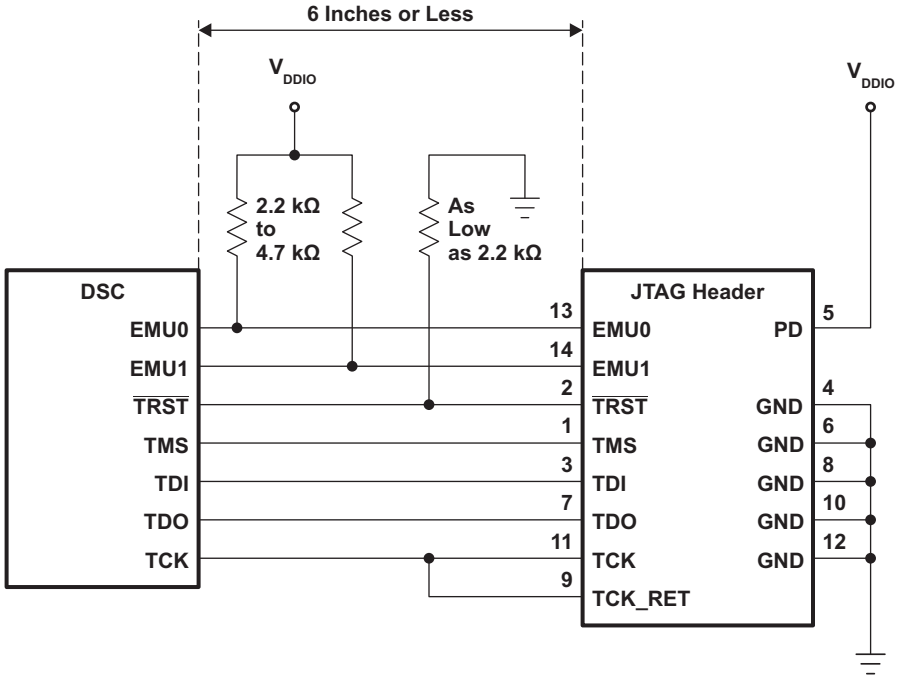


Figure 7. JTAG Pin Connections (for a single F28x based system)

3.3.1 Daisy Chaining With JTAG Ports of Other Devices on the Board

If your board contains more than one device with JTAG ports, a single JTAG connector can be shared between them.

While the connection to the JTAG header may be the same, the scan chains used for emulation purposes are different from those used for boundary scan. Various serial scan chains, through which the information can be scanned, are internal to the processor. The emulator card controls which scan chain is used and what information is contained in each scan chain. Traditionally referred to as the Scan Manager, this function assumes the task of controlling all information scanned into and out of the various processors in the scan chain. Furthermore, it directs this information to and from the various debugger windows.

A basic rule to remember is that all data must be scanned serially through all devices while connecting a common JTAG connector to multiple ports.

One method is shown in Figure 8.

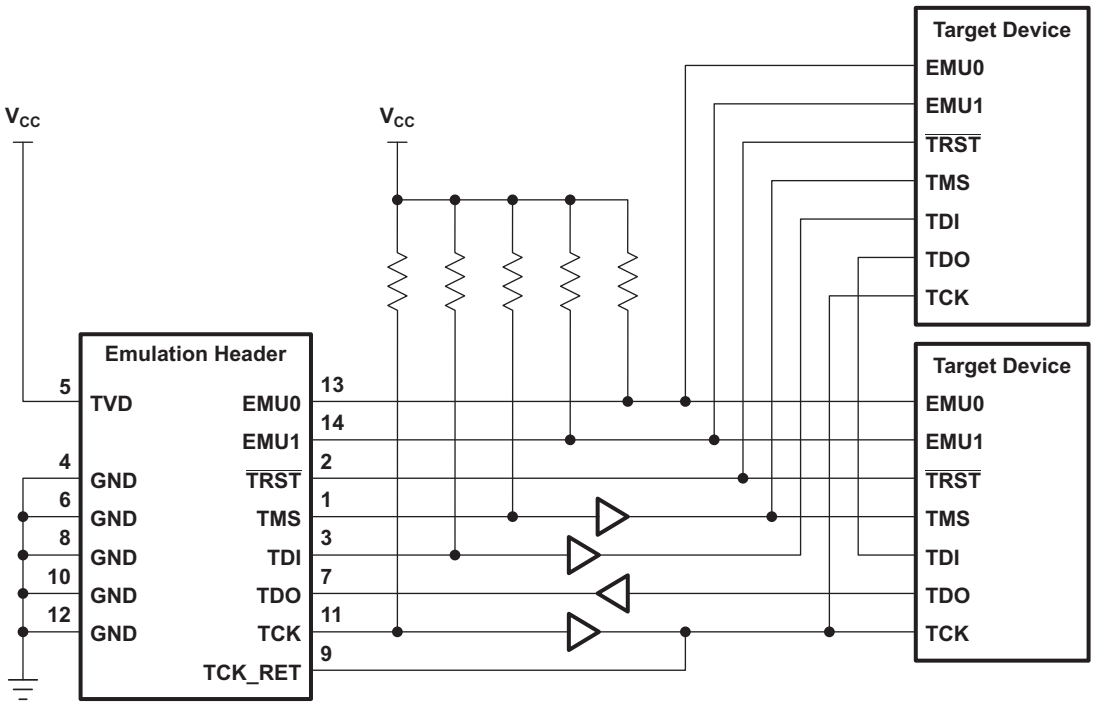
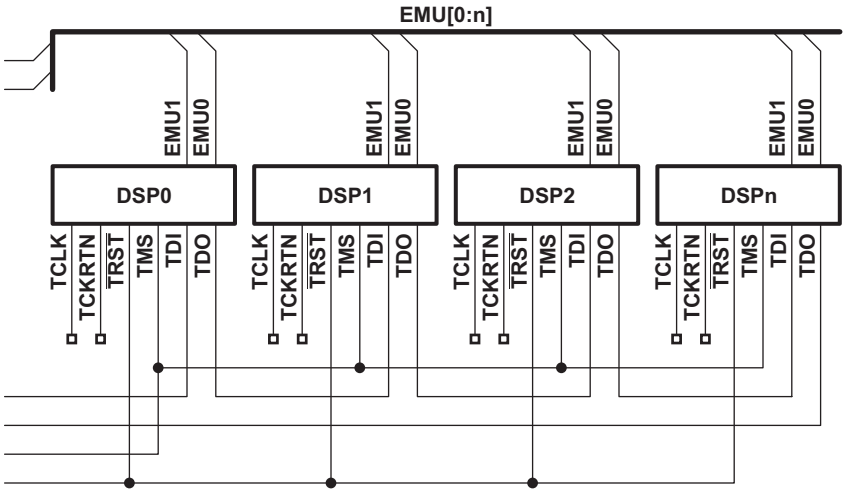


Figure 8. Emulator Connections for Multiprocessor System

Another configuration is to connect the ports in daisy-chain fashion, as shown in Figure 9.



A Target clock and target clock return connections not shown

Figure 9. Emulator Daisy-Chain Connections

When debugging systems that have more than one TI device defined, you are required to use the parallel debug manager (PDM), which provides a method of synchronous debugging of your multiprocessor application. If you have configured a multiprocessor system within CC_Setup, the PDM is automatically invoked when you start CC_App.

For additional information on the emulation features see *Emulation Fundamentals for TI's DSP Solutions* (SPRA439), the Emulation Features section in *TMS320C28x DSP CPU and Instruction Set Reference Guide* (SPRU430), and the Designer Considerations for Using the XDS510 Emulator section in the *TMS320F/C24x DSP Controllers CPU and Instruction Set Reference Guide* (SPRU160).

3.3.2 Important Careabout With JTAG and EMU Pins

Important issues are discussed in this section. The signal description section of every C2000 platform of data sheets describe the termination requirements on these pins. Whether you plan to use JTAG interface or not, you need to be sure that these signals will not interfere when the systems are running in the field. The first thing to note is the function of the $\overline{\text{TRST}}$ pin, which is a JTAG test reset pin.

NOTE: The $\overline{\text{TRST}}$ pin when driven high, gives control of the device operations to the scan system (emulator). This pin has an internal pulldown and should never be pulled high. The internal pulldown is not very strong so that it will not load the scan system. In a noisy environment, this pin can pick up a strong noise signal, putting the device in test mode. It is highly recommended to add an external pulldown resistor. The value of this resistor is based on the drive strength of the debugger pods used. A 2.2-kΩ resistor generally offers adequate protection.

Many simple looking designs have the presence of electrical noise. For example, driving a little larger load creates a voltage spike on supply rails. The I/O and core power supply can have a good amount of ripple and noise; otherwise, the board layout may not be *noise friendly*. Any spike picked up by the $\overline{\text{TRST}}$ pin will put the device in test mode and it will appear as if the DSC were suddenly hung while running the application code. To avoid this situation, terminate the $\overline{\text{TRST}}$ pin as mentioned in the note above.

Similar to the $\overline{\text{TRST}}$ pins, termination on EMU0 and EMU1 pins are important. The data sheets recommend pulling these pins high using a resistor between 2.2k to 4.7kΩs. You should make sure that the value you select will not load the debugger pod. If there is presence of higher noisy conditions, the value of the PD resistor on the $\overline{\text{TRST}}$ pin could be lowered further.

Add bypass caps (0.01 μF) to the critical JTAG signals, which are $\overline{\text{TRST}}$, EMU0, and EMU1. While GPIO pins without any PCB trace could generally be left to rely on the internal pull-up, critical pins like –XRS and -TRST should be designed with an external pull-up and pull-down, respectively.

3.4 Interrupts and GPIOs Pins and Onboard Peripherals

The following sections discuss the precautions required while interfacing GPIO/interrupt pins and onboard-peripherals.

3.4.1 GPIO Pins

The GPIO pins are multiplexed for two or more signals; each GPIO pin could be used to implement digital I/O or peripheral I/O. To help the routing of signals or if you need to use the pin for a different multiplexed option, some of the peripheral signals are multiplexed at two different sets of pins.

The drive strength (sink/source current) of the output buffer on GPIO pins is typically 4 mA (unless otherwise noted). The maximum toggling frequency of the GPIO pin is 20 MHz for the F281x devices and 25 MHz for the F280x/F28xxx devices.

Note that at reset, the GPIO pins are defined as input (default condition). A commonly asked question is what to do with unused GPIO pins? All of the F28x devices are built around CMOS technology. Therefore, the rules and care, as applied for CMOS input (high impedance) or output, are applicable. The options are either configured as outputs and left unconnected or define them as input with proper termination on the pin. A pullup or pulldown resistor (1 kΩ to 10 kΩ) to V_{CC} or GND puts them in defined state. Any input that is allowed to float can bias the input buffer in a linear mode in which excessive power supply current can be drawn; in most cases, this is undesirable. Theoretically, non-critical inputs could be defined as *output* and left floating in the interests of not wasting power; however, it is generally a good idea to keep them in default *input* mode and tie them off.

When tying off unused inputs, several different approaches can be used. If multiple inputs require being pulled up, this can be done (depending on input current) with a single resistor as long as the resistor value is low enough (do not forget Ohm's Law). This is also assuming none of these inputs ever get driven low. Note that if too many inputs are pulled high with a weak resistor, the result can be that a solid logic level is not maintained. If this level is not maintained, the device may interpret that one or more of the pins are in a logic low state. This has caused serious problems in many systems.

Any input that is normally pulled high but sometimes must be driven low, for a system test or other reasons, should be pulled up with its own resistor (unless you want to drive all these inputs low).

Ground any inputs required to be tied to logic zero unless the input needs to be forced high, for a system test or other reasons. Use a strong pulldown if the input is normally low but sometimes needs to be forced high. If you are sure that a particular GPIO pin will never be used, a good practice is to pull it to ground.

Also, note that some pins have internal pullups/pulldowns controlled by software, and may not be initialized to the desired state after reset. The register bits that control these functions should always be properly initialized in software, if necessary.

3.4.1.1 Driving High Value Load

Use the appropriate buffer devices if you need to drive the load on the GPIO pins in excess of their ± 4 mA capacity. Examples of this load are DC relay, LEDs and so forth. Consider the following TI parts:

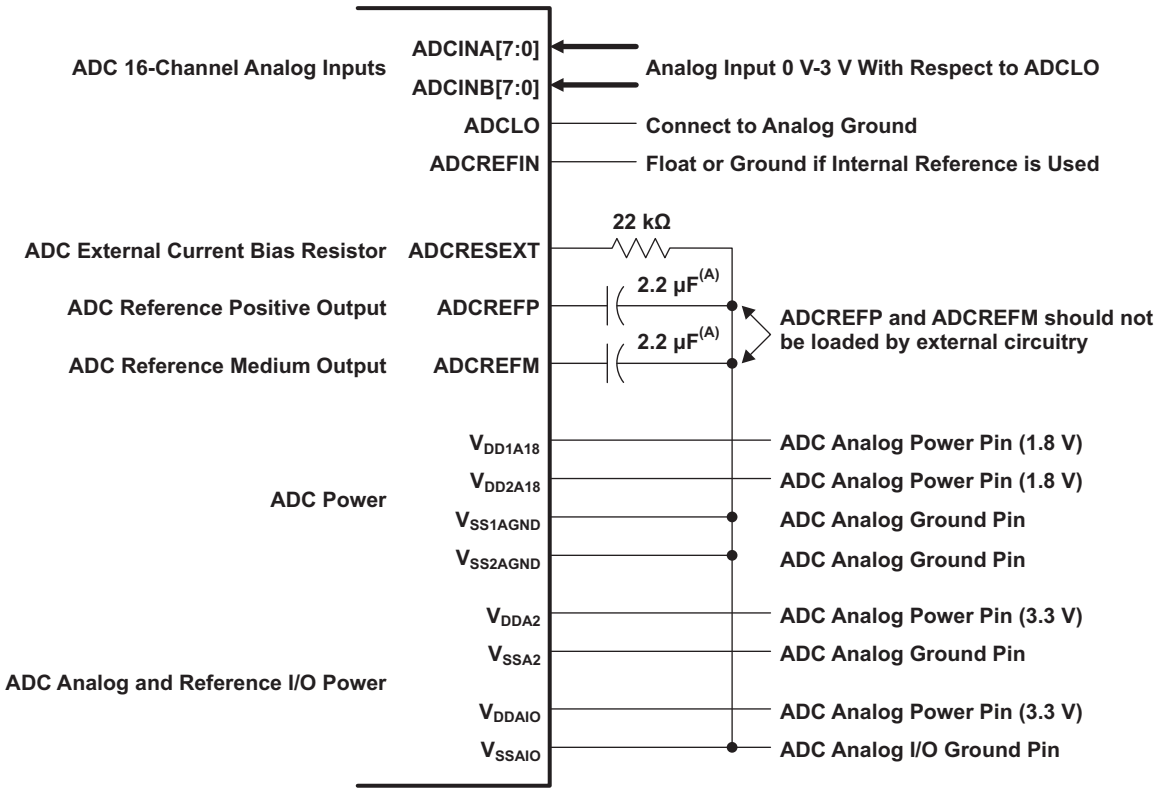
- ± 24 mA output drive: SN54AC241, SN74AC241

  SN54AC241, SN74AC241 Octal Buffers/Drivers With 3-State Output Data Sheet (SCAS513)
- High voltage, high-current load: ULN2xxx transistor arrays (50 V, 500 mA typical)

  ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A, High-Voltage High-Current Darlington Transistor Array Data Sheet (SLRS027)

3.4.2 Analog-to-Digital Converter (ADC)

The ADC peripheral requires few external components for biasing of internal band gap reference and filtering noise on reference voltage signals. The schematic in Figure 10 shows these parts and their connections.



A TAIYO YUDEN LMK212BJ225MG-T or equivalent

B External decoupling capacitors are recommended on all power pins.

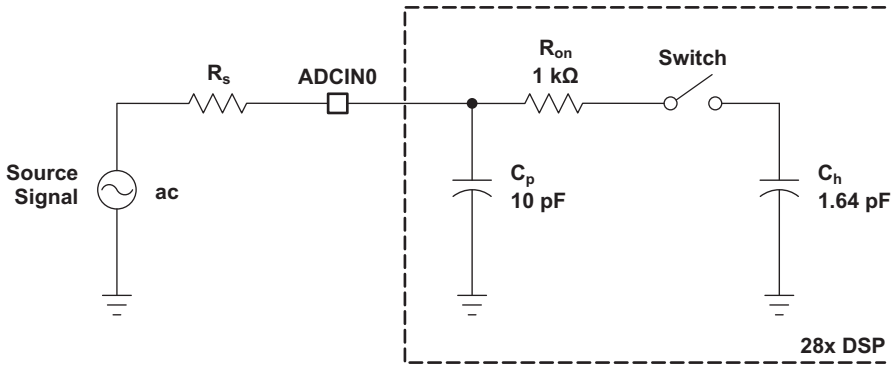
C Analog input pins must be driven from an operational amplifier that does not degrade the ADC performance.

Figure 10. ADC Pin Connections for TMS320F28xxx

Make sure that these components values are correct and that they are placed close to the respective pins.

3.4.2.1 Driving ADC Input Pins

The front end circuits of the ADC block is two sets of an 8-channel multiplexer followed by sample and hold circuits. Note that each input analog signal sees the load from the ADCIN pin as shown in Figure 11. C_h is the *sample* capacitor and R_{on} is the ON resistance of the multiplexer path. C_p is the parasitic capacitance associated with the ADCIN pin.



Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}):	1 kΩ
Sampling Capacitor (C_h):	1.64 pF
Parasitic Capacitance (C_p)	10 pF
Source Resistance (R_s)	50 Ω

Figure 11. Analog Input Impedance Model (F28xxx)

It is a good practice to use an op-amp driver circuit for signal conditioning of input analog signals and as a buffer. The op-amp isolates the ADC, acts as a low-impedance source to charge the sample capacitor, and can be configured as a unity gain buffer or level shifter. It provides low/stable output impedance and protects the ADC inputs. Figure 12 shows a commonly used ADC driver circuit configuration for DC and low-frequency signals.

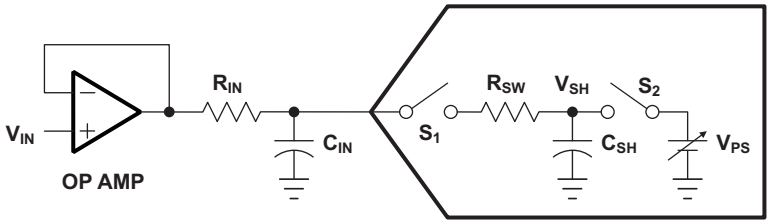


Figure 12. Typical Buffer/Driver Circuit for ADCIN

Though external R_{IN} and C_{IN} form a low-pass filter, they actually serve as a *flywheel* in the presence of the current pulses created by the ADC's input circuitry. R_{IN} isolates the ADC from the amplifier; however, during sampling, C_{IN} acts as a reservoir and helps in signal stability. The optimum capacitor value is 20 – 30 pF (CIN >= 10*CSH) and the resistor value is selected to meet the speed or bandwidth requirement; but it should not typically exceed 100 Ω.

V_{PS} is the residue from the previous sample. Ideally, it would be zero, but in reality if you are sampling back to back, it approaches the previously sampled value. R_{SW} is the on-resistance of MUX. During acquisition, S1 is closed - S2 is open. The sampling capacitor C_{SH} (1.64 pF) is charged through the switch resistor R_{SW} (1 KΩ) and R_{IN} for the period S1 is closed; this period is controlled by ACQ_PS (derived from ADC Clock) setting. This action of charging the capacitor is shown in the following equation:

$$Vc\ (t) = Vin \times (1 - e^{t})$$

For the internal RC circuit, formed by R_{SW} and C_{SH}, this settling time is 9 ns, much smaller than the minimum sampling window of 40 ns at 12.5 MSPS. However, this time period is much longer for the external RC circuit. Also consider the additional trace capacitance and pin's parasitic capacitance while calculating the time constant of RC circuit. It should be met by a higher value for ACQ_PS and/or a lower sampling frequency that meet the system requirements.

NOTE: It is necessary to maintain the analog input voltage applied to the ADCIN pins within 0 V – 3.0 V range. These analog signals pass through the multiplexer network first. Any voltage above V_{DDA} + 0.3 V or below V_{SS} – 0.3 V will bias the multiplexer in an undesired way, giving the wrong values for other channels. To achieve accurate values, the sample capacitor should be charged to within ½ LSB of the final value.

Here are a few suggestions for the low-noise/low-offset, single-supply op-amp to drive the ADC input circuit.

- OPA4376 - *OPA376, OPA2376, OPA4376 Precision, Low Noise, Low Quiescent Current, Operational Amplifier Data Sheet* (SBOS406)
- OPA4343 - *OPA343, OPA2343, OPA4343 Single-Supply, Rail-to-Rail Operational Amplifiers microAmplifiers Series* (SBOS090)
- TLV2474 - *TLV2470, TLV2471, TLV2472, TLV2473, TLV2474, TLV2475, TLV247xA Family of 600 μA/CH 2.8 MHz Rail-to-Rail Input/Output High-Drive Operational Amplifiers With Shutdown* (SLOS232)

For additional information on the ADC peripheral, see *An Overview of Designing Analog Interface With TMS320F28xx/28xxx DSCs* (SPRAAP6).

3.4.2.2 Reference Voltage – Internal vs. External

All the ADC blocks of the F28xx/F28xxx devices have internal bandgap reference voltage source. The only reason for going for external voltage source is the *temperature stability*. The temperature coefficient of the internal voltage source is 50 PPM/°C.

If your end product requires good ADC accuracy over a wider temperature variation, you need to select an external reference voltage source that requires lower value temperature coefficient. While doing so, it is important that you use a low output impedance op-amp buffer so that signal is stable during the conversions. Do not connect this node to any other input or load circuit on the design. It is important that noise on the reference input pins be less than 100 μV.

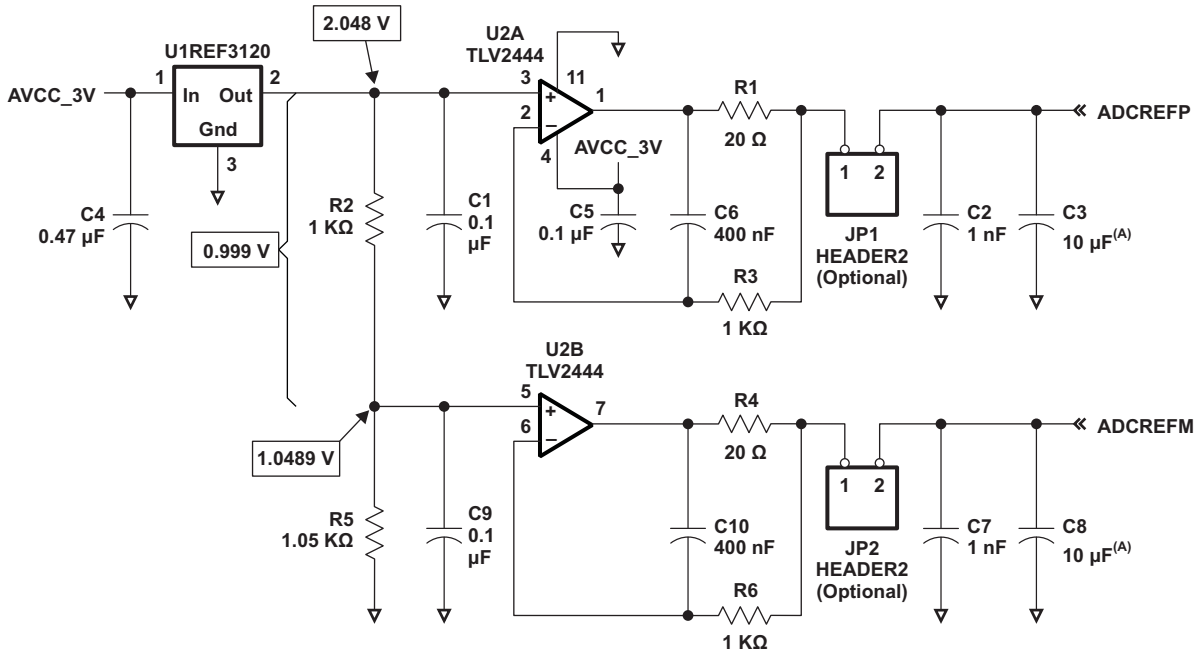
- Connecting an external voltage reference for the F280x, F280xx and F2833x devices: The ADC blocks of these parts require a single reference voltage input to be connected between the ADCREFIN and ADCLO pins. Based on customer application requirements, the ADC logic can be supplied by an external voltage reference. The F280x ADC accepts 2.048 V, 1.5 V, or 1.024 V on the ADCREFIN pin. You also need to set a two-bit field of the ADC Reference Select Register (ADCREFSEL) according to the voltage level of the external source to enable the external reference and determine the reference source selected.

  The voltage of 2.048 V was chosen to match the industry standard reference components; 1.5 V and 1.024 V are alternatives.

  NOTE: Selecting any of the three voltage levels (for external reference) does not change the analog input voltage range. It remains 0 V–3.0 V irrespective of the reference voltage level.

- Connecting an external voltage reference for F281x devices: The F281x family parts require two inputs for the ADC reference: ADCREFP and ADCREFM. The voltage difference ADCREFP – ADCREFM should be 1.00 ± 0.05 V.

Figure 13 shows a typical schematic for connecting the external reference voltages for F281x devices.



A Do not load ADCREFF and ADCREFM pins with any other circuitry. Connect the appropriate value, low ESR filter capacitors to these pins.

Figure 13. F281x ADC External Reference Schematics

The recommended Texas Instruments voltage reference parts are REF3120 (10 PPM typical, 20 PPM max) and REF5020 (3 PPM max).

REF3112, REF3120, REF3125, REF3130, REF3133, REF3140 15ppm/°C Max, 100 µA, SOT23-3 Series Voltage Reference Data Sheet (SBVS046)

REF5020, REF5025, REF5030, REF5040, REF5045, REF5050 Low-Noise, Very Low Drift, Precision Voltage Reference Data Sheet (SBOS410)

3.4.2.3 ADC Calibration

Like all ADCs, the inherent gain and offset errors are associated with the F28xx/F28xxx ADCs. Some applications may require corrections to improve the accuracy, i.e., improving ENOB.

The F281x ADC has a maximum offset error of ± 80 LSB and a maximum gain error of ± 200 LSB. The maximum values for both gain and offset error for F280x/F280xx parts are ± 60 LSB. The newer F2833x parts have improved these specifications to an offset error of ± 15 LSB and a gain error of ± 30 LSB. Furthermore, F280x/F280xx and F2833x parts include the ADC Offset Trim Register (ADCOFFTRIM), which is useful to correct the offset error. For the ADC on F2833x, this register also helps in getting the complete input voltage range of 0 V – 3 V, after offset correction. This family also includes the ADC_cal()routine programmed into the OTP memory by the factory. The Boot ROM automatically calls the ADC_cal() routine to initialize the ADCREFSEL and ADCOFFTRIM registers with device-specific calibration data.

For more information on calibration procedures, see *F2810, F2811, and F2812 ADC Calibration* (SPRA989) (for F281x) and *TMS320280x and TMS3202801x ADC Calibration* (SPRAAD8) (for F280xx). These application reports also include the schematics of additional circuitry and associated code.

3.4.2.4 Unused ADC Input Pins

Make sure that all unused ADC inputs are terminated to the analog ground ($V_{SS1AGND}$/$V_{SS2AGND}$); these pins are always defined as *input*. Having high-input impedance if left open, these pins can pick up noise signals and affect the performance of other inputs to the ADC through the multiplexer.

3.4.2.5 ADC Connections if the ADC is Not Used

It is recommended to keep the connections for the analog power pins - even if the ADC is not used. The following is a summary of how the ADC pins should be connected if the ADC is not used in an application:

- V_{DD1A18}/V_{DD2A18} – Connect to V_{DD}
- V_{DDA2}, V_{DDAIO} – Connect to V_{DDIO}
- $V_{SS1AGND}/V_{SS2AGND}$, V_{SSA2}, V_{SSAIO} – Connect to V_{SS}
- ADCLO – Connect to V_{SS}
- ADCREFIN – Connect to V_{SS}
- ADCREFP/ADCREFM – Connect a 100-nF cap to V_{SS}
- ADCRESEXT – Connect a 22-kΩ resistor (very loose tolerance) to V_{SS}
- ADCINAn, ADCINBn - Connect to V_{SS}

When the ADC is not being used, disable the clock to the ADC module to save power.

3.4.3 Control Peripherals - PWM, CAP, QEP and Event Manager

The event manager of the F281x devices and the ePWM, eCAP, and eQEP blocks of the F280xx/F28xxx devices account for generating and/or interfacing the PWM and pulse signals for various control applications. As mentioned previously, corresponding GPIO pins are set to select required interface via the GPIO MUX Register (GPxMUX). The current sink/source capacity of these pins is ± 4 mA for most F28x parts. You need to add an appropriate high-power circuit to enhance this capacity to drive the load and remember that at reset these GPIO pins are defined as input with the internal pullups enabled, except for the pins providing PWM output for which they are disabled. This condition remains for a short duration until the ports are initialized. Normally, there is no need for any external PU/PD resistor, unless it is mandatory for your schematic design.

The switching power circuits and other interface circuits for these peripherals are dependent on the goals of each design. This part of your circuit (and board) switches fairly high power, so pay close attention to the placement of these parts and the related board layout.

3.4.4 Serial Communication Ports (McBSP, I2C, SPI, SCI and CAN)

I2C and serial peripheral interface (SPI) are board-level interfaces that are connected to other devices on the board or system. These signals normally run directly. Pay close attention to the drive capability and trace length, which depends on the selected frequency of these signals. SCLA and SDAA pins of the I2C link are required to be pulled high using ~ 5 KΩ resistors.

However, serial communications interface (SCI) and controller area network (CAN) interfaces are used to connect to different systems running under another processor. These ports require specialized *transceiver* parts to transform the signal into the required electrical signaling (single-ended RS232 or differential for CAN and RS422/RS485), so that they can interface with the ports on the other devices per defined protocol. The CAN ports will not show any activity on the CANRX or CANTX pins during the transmission unless this port is connected to an active port on the other end through respective transceivers.

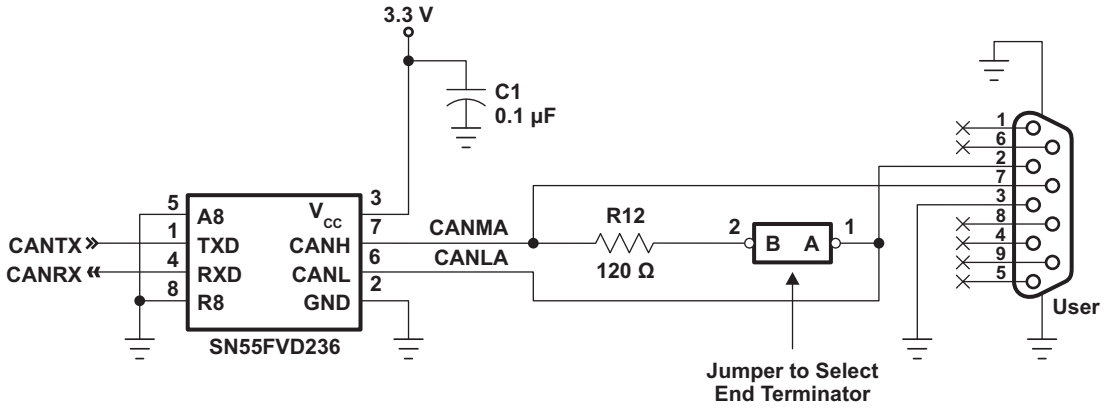


Figure 14. Typical CAN Transceiver Schematic

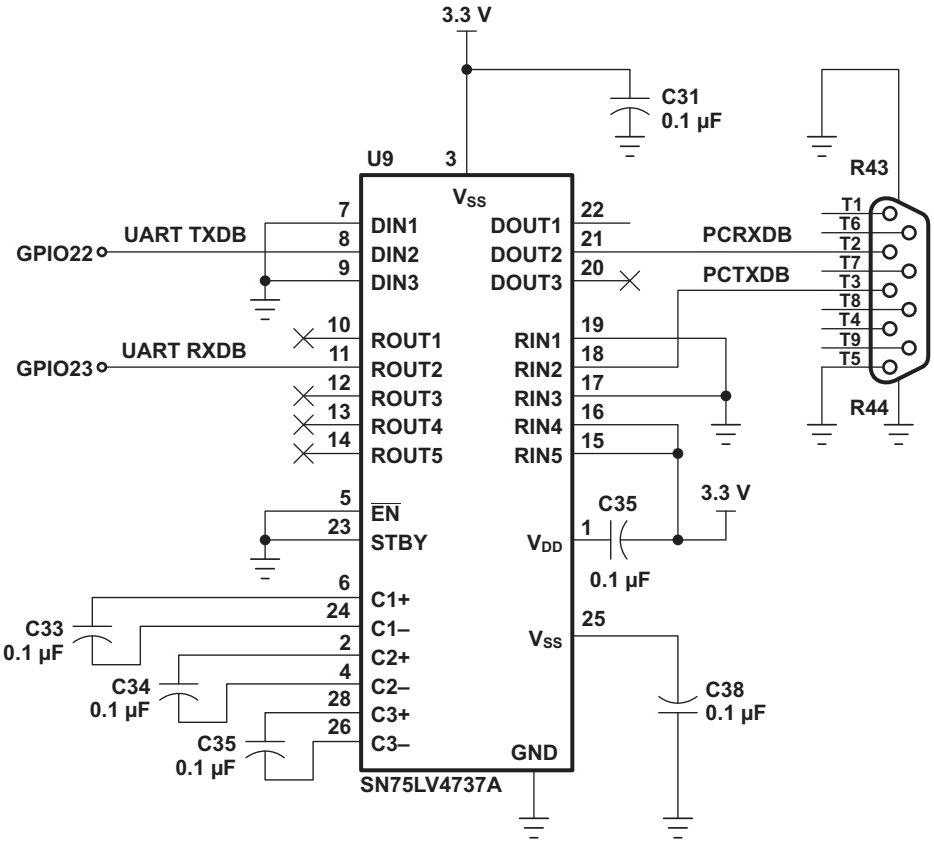


Figure 15. Typical RS-232 Transceiver Schematic

To select these parts for your design, go to the TI website: http://www.ti.com → Interface.

3.4.5 Interfacing the XINTF

F2812 and F2833x devices are supported with this non-multiplexed asynchronous bus to add an external parallel device. This interface is primarily used to expand system memory; generally RAM. These memories can be fast, running at or near the processor speed, or slow, many times slower than the processor speed, and can be asynchronous like SRAM, ROM, or Flash. When interfacing to memory, reference the device-specific data sheet to make note of the timing requirements from both a DC and an AC perspective and the loading conditions such as whether buffers will be required to ensure at speed access. Other devices that can be present on the parallel bus are first-in-first-out (FIFOs), digital logic and parallel A/D and D/As. If the parallel device is slower than the processor speed the software wait states may be generated, or in the case of a very slow memory or other parallel device, whether a hardware ready signal (XREADY) must be used to allow the slow memory to interface seamlessly to the fast processor.

Place the devices connected to the XINTF close to the DSC so that these bus signals run over short traces. Some designs may require connecting multiple memory devices to the XINTF. A good approach to evaluate the capacitive loading is to do IBIS model analysis for the 281x/2833x and memory devices. This analysis is the best way to evaluate the design.

The XINTF is designed with a high-performance buffer to support a 35pf load. For more information regarding the drive strength for all pins, see the device-specific data sheet. Make sure the address, data, and control signals are balanced with a minimum pf load. Consider faster memories or longer wait states to account for slew on the control signals.

3.5 Power Supply

The F28xx/F28xxx devices have multiple power supply pins. This includes:

- CPU core supply (V_{DD})
- I/O supply (V_{DDIO})
- ADC analog supply pins (V_{DDA2}, V_{DDAIO})
- ADC core supply (V_{DD1A18}, V_{DD2A18}) – for F280x/280xx
- Flash programming voltages (V_{DD3VFL})
- Supply ground (V_{SS}, V_{SSIO})
- ADC analog ground (VSSA2, VSSAIO)
- ADC analog/core ground ($V_{SS1AGND}$, $V_{DD2AGND}$)

All the power supply pins must be connected for proper operation. All these devices have multiple supply pins for the core, I/O, and ADC/analog supplies. All such pins must be connected to the proper supply voltage for proper operation. Do not leave any of the supply pins unconnected. The voltage level for I/O pins is 3.3 V; whereas, the core supply voltage is either 1.8 V or 1.9 V. For more information, see the Electrical Specifications section of the device-specific data manuals. They also have Flash programming supply pins. These pins have to be connected to 3.3 V rail, particularly for in-circuit flashing applications.

3.5.1 Digital I/O and Analog 3.3 V Supplies

For proper operation of the A/D converters, a noise-free analog supply is a must. Any noise on the analog supply voltage rail severely degrades the performance of the converter, leading to inaccurate and/or unstable converted counts. Digital circuits, especially CMOS circuits, draw more current while switching. When a node is switched from one logic level to the other, the capacitance associated with that node must be charged or discharged; current must be drawn from the supply to do this. On the other hand, static circuitry draws significantly smaller amounts of current. Therefore, for a complex digital circuit like any digital signal controller, the current drawn is highly irregular; this type of current draw leads to a lot of noise on the supply rail.

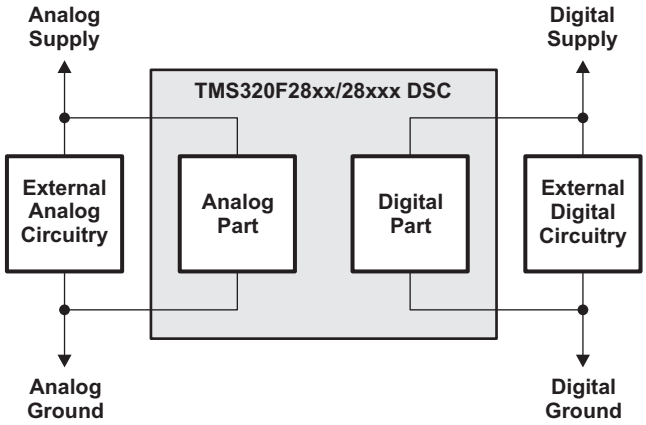


Figure 16. Separate Digital and Analog Supplies

If the analog circuitry is powered from a power supply like that mentioned above, there may be significant performance degradation. For example, the conversion results obtained from an analog-to-digital converter may bounce around, even though the voltage at the input of the ADC remains constant. To avoid ill-effects of noise that are usually present on the digital supply rail, it is necessary to power the ADC from a separate analog power supply (see Figure 16). This also applies to other analog circuits, normally using op-amps, comparators and so forth.

3.5.2 Generating Analog Supply From the Digital Supply

For most of the applications, the current drawn by the analog circuitry is small compared to the digital parts and it is okay to have a single voltage regulator capable to provide enough current for both type of parts. However, you need to isolate the analog supply from the noisy digital supply rail. The simplest form of circuit for generating an analog supply from the digital rail is to use passive components such as inductors to filter out the noise components. The inductors act as low pass filters, letting the DC power supply component through, but *choking* the noise, which is usually at a fairly high frequency. Using Ferrite beads is a better choice over a standard inductor. Ferrite beads have negligible parasitic capacitance; the electrical characteristics are similar to inductor. This part has a low DC resistance (DCR) (< 0.1 Ω) to keep the voltage drop at the lowest number. A suggestion for this part is Murata BLM21PG, which can be downloaded from the following URL:
http://search.murata.co.jp/Ceramy/CatalogAction.do?sHinnm=BLM21P221SG&sNHinnm=BLM21PG221SN1&sNhin_key=BLM21PG221SN1B&sLang=en&sParam=blm21.

In a noise-critical environment, another possibility is to use separate regulators to power the analog and digital circuitry. Close attention must be paid to the ground connection in this circumstance, since the ground connections can couple noise from the digital-to-analog circuits.

In both setups, pay attention to the regulator compensation specifications. Many regulators have sufficient compensation to ensure significant gain roll-off for the noise frequencies. However, it is always a good idea to ensure that the particular regulator you are using has internal compensation, or plan to add external compensation. This makes sure that the regulator does not oscillate.

3.5.3 Core Voltage Regulator

For more information regarding the correct values of the voltage and maximum current consumption, see the Electrical Specifications section of the device-specific data manual. Note that devices like F281x are specified at 1.9 V for CPU frequency of 150 MHz, but 1.8 V for up to 135 MHz.

3.5.4 Power Sequencing

For all F280x/F28xxx devices, no requirements are placed on the power up/down sequence of the various power pins to ensure the correct reset state for all the modules. However, if the 3.3 V transistors in the level shifting output buffers of the I/O pins are powered prior to the 1.8/1.9 V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} pins prior to or simultaneously with the V_{DDIO} pins, ensuring that the V_{DD} pins have reached 0.7 V before the V_{DDIO} pins reach 0.7.

NOTE: If you are planning to derive core supply (V_{DD}) from 3.3 V, you need to ensure that 3.3 V is not connected to DSC before V_{DD} as described above. You may have to use an FET switch to achieve this.

Additionally, it is recommended that no voltage larger than a diode drop (0.7 V) should be applied to any input pin prior to powering up the device. Voltages applied to pins of an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.

For F281x devices, if the 1.8 V (or 1.9 V) rail lags the 3.3 V rail, the GPIO pins are undefined until the 1.8 V rail reaches at least 1 V. The C281x devices do not require this sequencing. A simple way to achieve this is described below:

Enable power to all 3.3 V supply pins (V_{DDIO}, V_{DD3VFL}, V_{DDA1}/V_{DDA2}/V_{DDAIO}/AVDDREFBG) and then ramp 1.8 V (or 1.9 V) (V_{DD}/V_{DD1}) supply pins. 1.8 V or 1.9 V should not reach 0.3 V until V_{DDIO} has reached 2.5 V. This ensures the reset signal from the I/O pin has propagated through the I/O buffer to provide power-on reset to all the modules inside the device.

The F281x devices also need to follow the power-down sequencing as described below:

During power-down, the device reset should be asserted low (8 μs, minimum) before the V_{DD} supply reaches 1.5 V. This helps to keep on-chip Flash logic in reset prior to the V_{DDIO}/V_{DD} power supplies ramping down. It is recommended that you use the device reset control from *low-dropout (LDO)* regulators or voltage supervisors to meet this constraint. LDO regulators that facilitate power-sequencing, with the aid of additional external components, can be used to meet the power sequencing requirement. For F2812 eZdsp™ schematics and updates, see http://www.spectrumdigital.com.

3.5.5 Total Power Requirement and Selecting Voltage Regulators

While considering the current output capacity of the voltage regulators, allow for additional current required at the power-on as many capacitors are charged during this time. Also, some of the peripheral signals (e.g., PWM) draw excess current during switching. This dynamic current condition exists on both the voltage rails.

If your application uses in-circuit Flash programming, consider the extra current drawn (~ 200 mA) by the Flash circuits from 1.8 V rail during the program/erase cycles.

To determine the total current, add the maximum current values for different blocks specified in the data sheets. Consider all GPIO pins as output pins and calculate the total source current. Consider a 100% margin by multiplying this total by two for specifying the voltage regulator. Strictly avoid current starvation. Finally, determine if the heat-sinks are required.

The power supply noise should be quite low. Note that the ADC's step-size is 0.732 mV for the input range of 0 V - 3 V. A high value ripple on the ADC supply will result in bouncy ADC counts. The PLL jitter increases with power supply noise. Even the timing accuracy of the PWM is affected as the threshold of the transistors varies with high ripple/noise on the digital supply. Linear voltage regulators (LDO) have lower noise and high power supply rejection ratio (PSRR) compared to switching regulators (DC-DC converters). LDOs have faster response to load changes, typically 1 μs; however, LDOs have lower efficiency and they can become unstable if total decoupling capacitance exceeds higher limit.

Texas Instruments' power management portfolio offers various linear and switching regulators, reference designs/applications notes customized for F28x designs, and the power supply design support. You can find this information at the following URL: http://power.ti.com.

The F2808, F2812 and F28335 eZdsp boards use dual LDO part # TPS767D301 to generate 3.3 V and 1.8 V/1.9 V voltage rails. For more information regarding part # TPS767D301, see the *TPS767D3xx Dual-Output Low-Dropout Voltage Regulators Data Sheet* (SLVS209).

The *TMS320F2808 DSP Power Reference Design* (SLVA296) uses a dual DC-DC buck converter and a voltage supervisor part to generate a Reset signal, ensuring power sequencing requirement.

3.6 Boot-Mode and Flash Programming Options

All F28x devices come with a factory programmed Boot-ROM that contains bootloading software and standard tables, such as SIN/COS waveforms for use in math related algorithms. The first consideration is to tell the bootloader software which Boot mode to select at power on. Another point to consider is the Flash-programming mode at production level. Some applications require the facility for field updates of the application code and selected configurations need to be considered while going for the schematics design.

3.6.1 Boot-ROM and Boot-Mode selection

The reset vector in boot ROM redirects program execution to the InitBoot function. After performing device initialization, the bootloader checks the state of the GPIO pins to determine which boot mode you want to execute. Options include: jump to flash, jump to SARAM, jump to OTP, jump to XINTF, or call one of the on-chip boot loading routines from a serial port. At device Reset (power-on reset or warm-reset), after performing device initialization, the bootloader checks the state of these GPIO pins to determine which boot mode you want to execute.

Different F28x generations have their own Boot-mode criteria and use different GPIO pins. Table 2 through Table 4 provide these details.

Table 2. Boot-Mode Selection for TMS320F281x Devices

GPIOF4	GPIOF12	GPIOF3	GPIOF2	
(SCITXDA)	(MDXA)	(SPISTEA)	(SPICLK) [1]	
PU [2]	No PU [3]	No PU	No PU	Mode selected
1	X	X	X	Jump to Flash address 0x3F 7FF6 [4] You must have programmed a branch instruction here prior to reset to redirect code execution as desired.
0	1	X	X	Call SPI_Boot to load from an external serial SPI EEPROM
0	0	1	1	Call SCI_Boot to load from SCI-A
0	0	1	0	Jump to H0 SARAM address 0x3F 8000 [4]
0	0	0	1	Jump to OTP address 0x3D 7800 [4]
0	0	0	0	Call Parallel_Boot to load from GPIO port B

(1) You must take extra care due to any affect toggling SPICLK to select a boot mode may have on external logic.
(2) PU = Pin has an internal pullup
(3) No PU = Pin does not have an internal pullup
(4) If the boot mode selected is Flash, H0, or OTP, then no external code is loaded by the bootloader.

Table 3. Boot-Mode Selection for TMS320F280x/F280xx Devices

GPIO18 SPICLKA [1] SCITXDB	GPIO29 SCITXDA	GPIO34	Mode	Description
1	1	1	Boot to Flash [2]	Jump to Flash address 0x3F 7FF6. You must have programmed a branch instruction here prior to redirect code execution as desired.
1	1	0	SCI-A Boot	Load a data stream from SCI-A
1	0	1	SPI-A Boot	Load from an external serial SPI EEPROM on SPI-A
1	0	0	I2C Boot	Load data from an external EEPROM at address 0x50 on the I2C bus
0	1	1	eCAN-A Boot [3]	Call CAN_Boot to load from eCAN-A mailbox 1
0	1	0	Boot to M0 SARAM [4]	Jump to M0 SARAM address 0x00 0000
0	0	1	Boot to OTP [4]	Jump to OTP address 0x3D 7800
0	0	0	Parallel I/O Boot	Load data from GPIO0 - GPIO15

(1) You must take extra care due to any affect toggling SPICLKA to select a boot mode may have on external logic.
(2) When booting directly to Flash, it is assumed that you have previously programmed a branch statement at 0x3F 7FF6 to redirect the program flow as desired.
(3) On devices that do not have an eCAN-A module, this configuration is reserved. If it is selected, then the eCAN-A bootloader will run and loop forever while waiting for an incoming message.
(4) When booting directly to OTP or M0 SARAM, it is assumed that you have previously programmed or loaded code starting at the entry point location.

Table 4. Boot-Mode Selection for TMS320F2823x and TMS320F2833x Devices

MODE	GPIO87/XA15	GPIO86/XA14	GPIO85/XA13	GPIO84/XA12	MODE [1]
F	1	1	1	1	Jump to Flash
E	1	1	1	0	SCI-A boot
D	1	1	0	1	SPI-A boot
C	1	1	0	0	I2C-A boot
B	1	0	1	1	eCAN-A boot
A	1	0	1	0	McBSP-A boot
9	1	0	0	1	Jump to XINTF x16
8	1	0	0	0	Jump to XINTF x32
7	0	1	1	1	Jump to OTP
6	0	1	1	0	Parallel GPIO I/O boot
5	0	1	0	1	Parallel XINTF boot
4	0	1	0	0	Jump to SARAM
3	0	0	1	1	Branch to check boot mode
2	0	0	1	0	Branch to Flash, skip ADC calibration
1	0	0	0	1	Branch to SARAM, skip ADC calibration
0	0	0	0	0	Branch to SCI, skip ADC calibration

(1) All four GPIO pins have an internal pullup.

If the design always boots from one of the modes, respective GPIO pins need to be terminated to the required levels. Applications that require switching between different boot modes (e.g., in-circuit flash programming via SCI) have to use jumpers to change the mode as and when required.

3.6.2 Flash Programming Options

The application firmware, for all F28x devices, can reside in the onboard Flash memory. You can use either JTAG port or the SCI port for in-house programming of the Flash memory. Applications requiring field updates of the firmware must use the SCI port to work with a Host.

Programming via JTAG is typically done during the development phase as it requires a Code Composer Studio™ IDE to communicate with the CPU. Once you have the final code ready and the product assembled in the final enclosure, the Flash can be programmed using the serial Flash utility (using .out file) by connecting the SCI port to the computer. You need to add the RS232 transceiver to this port. Some applications may use RS-485 signaling protocol here.

For details on the actual Flash programming process and software utilities, see the respective product folder that covers application notes, reference guides, and the software tools.

4 Schematics and Board Layout Design

In Section 3, information relevant to each peripheral that affects the schematic designs was discussed. It was determined that they need external circuitry for their proper functioning. Analog signal conditioning and power supply topics were also covered. The other important parts on the schematics are bypass capacitors and connectors.

Component placement and layout design are quite challenging tasks. Many online documents and text books discuss the theory behind high frequency signal propagation and high-speed digital design. Apart from *frequency* the other key parameters/terms on this subject are rise/fall time, propagation delay, characteristic impedance, reflections, termination, resulting crosstalk and so on. You are encouraged to read more details and theory in the articles from the reference sections.

These discussions are limited to the F28x board layout issues. There are many parasitic elements on a PCB. These parasitic inductors, capacitors, and resistors dominate circuit behavior at high frequencies (typically above 10 MHz) destroying the frequency response of the signals. The complex F28x DSCs have several onboard peripherals operating at various frequencies. A well laid out board will avoid further iterations/spins from pushing the project schedule and increasing the cost. Also, with a good layout, many EMI problems can be minimized in order to meet required specifications.

NOTE: A schematic of a typical TMS320F2833x reference design including the OrCad files is available from the following URL: http://focus.ti.com/docs/toolsw/folders/print/sprc541.html or see the *TMS320F2833x Reference Design Reference Guide* (SPRC541).

4.1 Bypass Capacitors

Like most of the TI DSPs, C2000 parts are fabricated using advanced CMOS technology, which gives good high-speed performance consuming little power. The CMOS circuits draw large currents at every transition, producing current spikes on the supply rails. These rising and falling glitches have to be filtered before they traverse into the sensitive circuit area. The *bypass* or *decoupling* capacitors placed across supply-positive pins and ground are used for such filtering; F28x DSCs have several supply-positive pins. You need to use one capacitor on each supply-positive pin and should place this capacitor as close to the pin as possible, without using any via. Typically small (10 nF to 100 nF), low-ESR ceramic capacitors are used for this purpose.

For a sensitive design, you can calculate precise value considering noise frequency, surge current, and maximum ripple voltage of the power supply from the following formula:

$$C_{BYPASS} = I_{SURGE}/(2 \times \pi \times f_{NOISE} \times V_{RIPPLE})$$

Adding bypass capacitors to the analog supply pins helps reduce power-supply noise entering the analog circuits.

4.2 Location of Power Supply

Ideally, the voltage regulators should be placed in such a way that the supply traces do not run too long. Since the main DSC occupies center place because it needs to be connected to different interfaces, a better location for the power circuits is between the DSC and the center of one edge of the board. Also, the thermal management is a point to be considered. If your design uses the low-drop-out type of linear voltage regulators (LDO), they get heated, depending upon the power dissipated across them.

4.3 Power/Ground Routing and Number of Layers

Grounding is an important parameter to be considered for a good layout to achieve a high level of signal integrity, low interference, low noise and so forth. Remember for each digital signal there is a return signal via the ground trace. This criteria is important when deciding if your design requires a separate *ground plane*, which is an additional copper layer for the board. The basic rule is that the *signal* and its *return* trace should run together and be of equal length; on a two-layer board, the tendency is to have fewer *ground* traces. Also, if you have analog circuitry on the board and you are using ADC, there are going to be separate analog ground traces on the board.

Similar to ground plane, a separate power plane is recommended for complex systems. With many voltage rails, it is not possible to provide a separate layer for each rail. You will have to carefully split the power plane. This enables the board designer to supply power to circuits while keeping noise and ground bounce under control and simplifies the problem of powering high-power circuits, keeping the voltage drops to the supply pins at a minimum.

4.4 Clock Generation Circuits

For the external oscillator, see Section 3.1.1.1, to select the values of the load capacitors. Crystal/resonator and associated load capacitors should be placed close to the respective pins. If the external oscillator is used, place it close to the X1 or the XCLKIN pin with a short ground path to avoid radiation.

4.4.1 Suggestion for Oscillator Layout

Figure 17 shows the typical parts placement and routing for the oscillator layout; you must modify this appropriately for your F28x part. You can use a crystal or resonator from any vendor. This is a simple two-pin component added to the DSP circuit. If you want to add other components (capacitors) with standard values, you should select these additional parts by referring to the schematics, Rs/Cs values and layout in the vendor's data sheets.

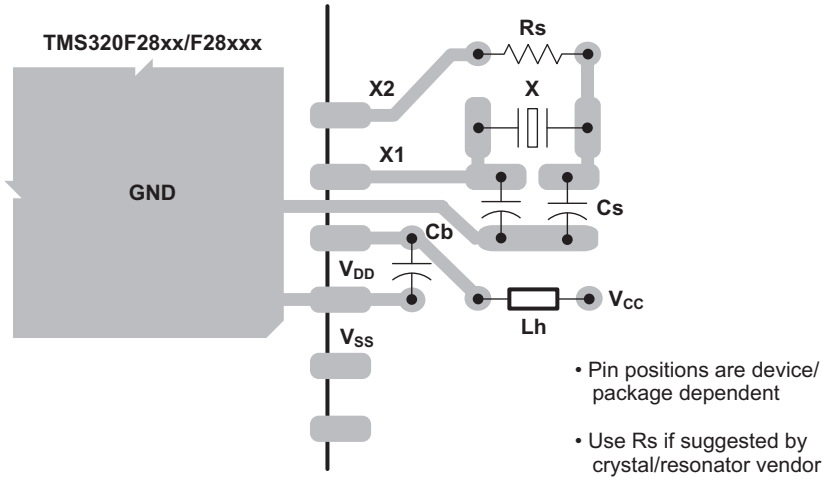


Figure 17. Suggested Crystal Oscillator Layout

All the traces should be direct, without using any via.

4.5 Debug/Test considerations

Most of the designers use a JTAG port for debugging/emulation purpose. The JTAG connector must be placed at a convenient location, but within the trace length of 6" from the DSC pins, Figure 7 shows the schematic. Even if you use any other method and interface for debugging, add the pullup and pulldown resistors to the EMUx and $\overline{\text{TRST}}$ pins of the JTAG port so that the system does not enter test mode due to the noise picked up by these pins.

Providing the test points for the following signals will help in troubleshooting and debugging:

- XCLKOUT – This test point should be very close to the device pin
- DGND – Digital ground is useful for connecting to the oscilloscope
- AGND – Analog ground
- 3.3 V – Output of the main 3.3 V voltage regulator
- 1.8 V/1.9V – Core supply
- ADCREFP and ADCREFM

Add jumpers or zero Ω resistors for signals that you want to connect or disconnect when debugging the system.

4.6 General Board Layout Guidelines

A good board layout is all about reducing the coupling of electrical noise generated by different circuit elements. The actions to target *low noise* starts much earlier during schematics design, part selection, and deciding certain design parameters, e.g., switching frequency of DC-DC converters.

4.6.1 Component Placement

A typical F28x design includes low-level analog circuitry among noise producing high-speed digital and very noisy circuits like relays, high-current switches like MOSFETs and BJT. The noise subsystems and sensitive circuitry should have good separation to limit the electromagnetic coupling. While placing the components, consider routing of the signals like clocks, external bus, serial port interface, and crystal circuits and so forth. As discussed earlier, each of these signals has a return path through ground trace or ground plane. Figure 18 suggests a broader way to separate different circuits.

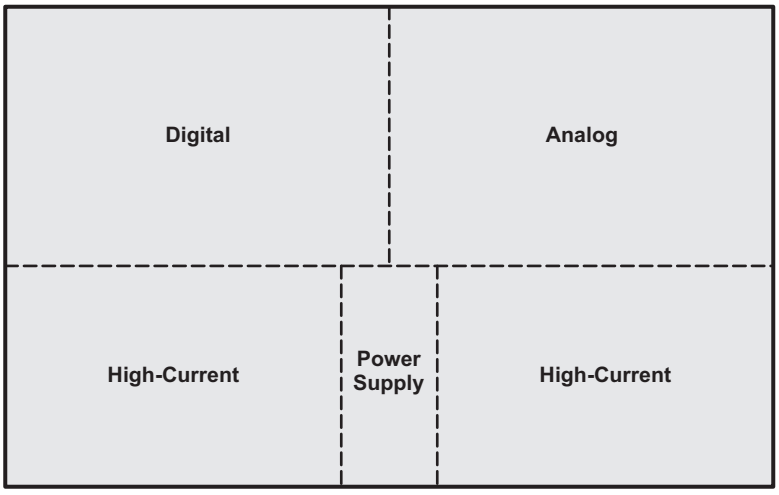


Figure 18. Suggestions for Circuit Separation

4.6.2 Considerations for Ground Layout

System ground is the most critical area and foundation related to noise and EMI problems on the board. The most practical way to minimize these problems is to have a separate ground plane.

What is Ground Noise?

As mentioned earlier, each signal originating from a circuit (say Driver) has a return current flow to its source via ground path. As the frequency increases, or even for simple but high-current switching like relays, there is a voltage drop due to line impedance generating interference in the grounding scheme. The return path is always via the least resistance. For DC signals, that will be a lowest resistive path and for high frequency signals it will be a lowest impedance path. This explains how a ground plane simplifies the issue and is the key to ensuring signal integrity.

4.6.3 Splitting Ground Plane

In Section 3.5.1, isolating digital and analog supplies was discussed. It is not recommended that the digital return signals propagate inside the analog return (ground) area; therefore, you have to split the ground plane to keep all the digital signal return loops within its ground area. This splitting should be done carefully. Many designs use a single (common) voltage regulator to generate a digital and analog supply of the same voltage level, e.g., 3.3 V. You need to isolate the analog rail and digital supply rails and their respective grounds from each other. Be careful while isolating ground, both grounds have to be *shorted* somewhere. Figure 19 suggests one method to achieve this.

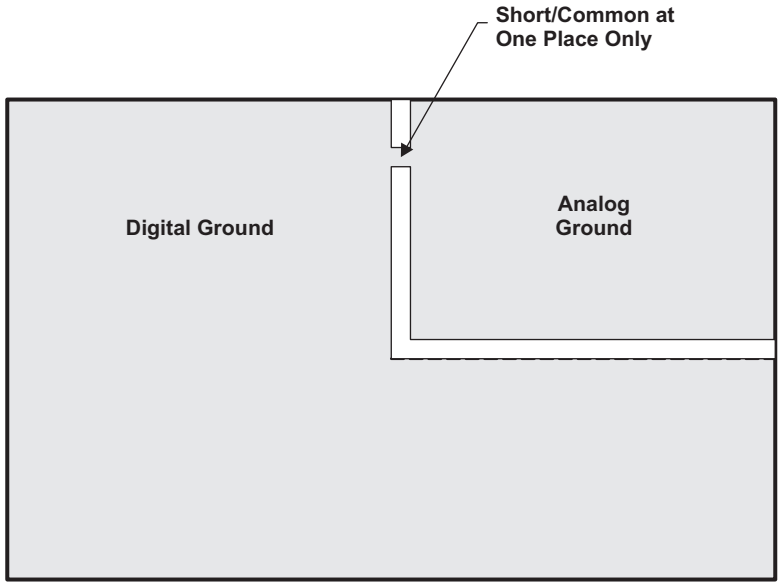


Figure 19. Digital and Analog Grounds and Common Area

Figure 19 shows how possible return paths for digital signals are not allowed to form a loop passing through the analog ground. On each design you need to decide the common point considering the component placements and so forth. Do not add any inductors (ferrite bead) or resistors (not even zero Ω) in the series with any ground trace. The impedance increases due to associated inductance at a high frequency, causing a voltage differential.

Do not route a signal referenced to digital ground over analog ground and vice versa. The return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise due to crosstalk into the analog ground plane, which can result in unstable ADC readings.

If your board has different layers for *digital* and *analog* ground, do not overlap the analog to digital planes.

4.6.4 Dealing With Two-Layer Board

If your project does not afford the cost of four-layer board, then for a two-layer board you need to use Star-ground. That is, have single point grounding at least for a group of sensitive signals. Do this by carefully laying down the ground traces; probably using manual routing. You need to make every effort to reduce coupled noise. Provide as much ground area as possible, instead of running several traces; use shorter and wider traces. As the (return) current always flows back to source, avoid large loops. They are quick to couple noise from the electromagnetic radiations.

Separate high-speed signals (e.g., clock signals) from low-speed signals and digital from analog signals; placement is important.

4.6.5 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner and the characteristic impedance changes. This impedance change causes reflections. Avoid right-angle bends in a trace and try to route them with at least two 45° corners. To minimize any impedance change, the best routing would be a round bend, as shown in Figure 20.

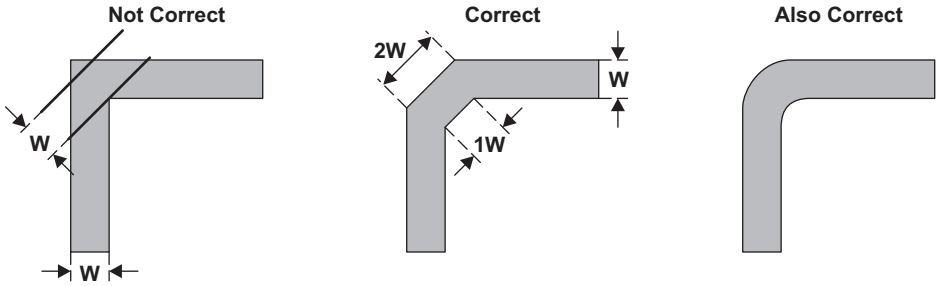


Figure 20. Poor and Correct Way of Bending Traces in Right Angle

To minimize crosstalk, not only between two signals on one layer but also between adjacent layers, route them 90° to each other.

The complex boards need to use vias while routing; you have to be careful when using them. They add additional inductance and capacitance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length. While using differential signals, use vias in both traces or compensate the delay in the other trace also.

5 EMI/EMC and ESD Considerations

These considerations are important for all system and board designs. Though the theory behind this is well explained, each board and system experiences this in its own way. There are many PCB and component related variables involved.

5.1 EMI/EMC

This application report does not go into the electromagnetic theory or explain the *whys* of different techniques used to combat the effects, but considers the effects and solutions as applied to CMOS circuits.

EMI is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby.

Studying EMC for your system allows testing the ability of your system to operate successfully counteracting the effects of unplanned electromagnetic disturbances coming from the devices and systems around it.

The electromagnetic noise or disturbances travels via two media: conduction and radiation.

The design considerations narrow down to:

- The radiated EMI from your board should be lower than that allowed by the standards you are following.
- The conducted EMI from your board should be lower than that allowed by the standards you are following.
- The ability of your board to operate successfully counteracting the *radiated* electromagnetic energy (EMC) from other systems around it.
- The ability of your board to operate successfully counteracting the *conducted* electromagnetic energy (EMC) from other systems around it.

The EMI sources for this system consists of several components such as PCB, connectors, cables and so forth. The PCB plays a major role in radiating the high frequency noise. At higher frequencies and fast-switching currents and voltages, the PCB traces become effective antennas radiating electromagnetic energy; e.g., a large loop of signal and corresponding ground. The five main sources of radiation are: digital signals propagating on traces, current return loop areas, inadequate power supply filtering or decoupling, transmission line effects, and lack of power and ground planes. Fast switching clocks, external buses, PWM signals are used as control outputs and in switching power supplies. The power supply is another major contributor to EMI. RF signals can propagate from one section of the board to another building up EMI. Switching power supplies radiate the energy which can fail the EMI test.

This is a huge subject and there are many books, articles and white papers detailing the theory behind it and the design criteria to combat its effects.

5.1.1 EMI Reduction Guidelines

Every board or system is different as far as EMI/EMC issues are concerned, requiring its own solution. However, the common guidelines to reduce an unwanted generation of electromagnetic energy are as shown below:

- Use multiple decoupling capacitors with different values and appropriate power supply decoupling techniques. Be aware that every capacitor has a self-resonant frequency.
- Provide adequate filter capacitors on the power supply source. These capacitors and decoupling capacitors should have low equivalent series inductance (ESL). Murata claims their three-terminal capacitors (NFM series) provide lower impedance at the frequencies above 20 MHz, than other types.
- Create ground planes if there are spaces available on the routing layers. Connect these ground areas to the ground plane with vias; creating a quarter-inch via grid is ideal.
- The high frequency signals (lower address lines, clock signals, serial ports and so forth) are usually terminated by a CMOS input, which is a load of > 100 K parallel with typically 10 pF. Charging/discharging of such a load results in high current peak. A possible fix is to add a series termination resistors (about 50Ω) and fine tune the resistors for optimal signal integrity. As per the transmission line theory, if the total output resistance (internal + external) is less than the line impedance (typically 70Ω–120Ω), it has no negative influence on speed. In general, reduce the rise-time of the signal if timing is not critical by adding a series termination resistor. Substantial benefits can be achieved with this approach at a low cost.
- Typically PWM signals driving a 3-phase H-bridge switch on and off cause current spikes. Symmetrical PWM reduces EMI related to dU/dt and di/dt by approximately 66% compared to asymmetrical PWM. The space vector PWM is symmetrical with respect to the PWM period, too. However, since only two transistors are switched during one PWM period, the switching losses as well as the EMI radiation are reduced by 30% compared to the symmetric PWM.
- Keep the current loops as small as possible. Add as many decoupling capacitors as possible. Always apply current return rules to reduce loop areas.
- Keep high-speed signals away from other signals and especially away from input and output ports or connectors.
- Apply current return rules to connect the grounds together while isolating the ground plane for the analog portion. If the project does not use ADC and there are no analog circuits do not isolate grounds.
- Avoid connecting the ground splits with a ferrite bead. At high frequencies, a ferrite bead has high impedance and creates a large ground potential difference between the planes.

- For PC board stackup, add as many power and ground planes as possible. Keep the power and ground planes next to each other to ensure low-impedance stackup or large natural capacitance stackup.
- Add an EMI pi filter on all the signals exiting the box or entering the box.
- If the system fails EMI tests, find the source by tracing the failed frequencies to their source. For example, assume the design fails at 300 MHz but there is nothing on the board running at that frequency. The source is likely to be a third harmonic of a 100 HMz signal.
- Determine if the failed frequencies are common mode or differential mode. Remove all the cables connected to the box. If the radiation changes, it is common mode. If not, then it is differential mode. Then, go to the source and use termination or decoupling techniques to reduce the radiation. If it is common mode, add pi filters to the inputs and outputs. Adding a common choke onto the cable is an effective solution but an expensive method for EMI reduction.

5.2 ESD

The TMS320F28x devices comply with TI standard ESD specifications and are tested for ESD compliance, including the peripherals and the port pins. TI tests the F28x devices with standard ESD tests (Human Body Model = 2.0 KV and Charged Device Model = 500 V).

Note that F28x and C28x parts are tested the same but they are electrically different. Since the ROM part lacks the Flash pump, they will have different EMI/ESD profiles. Before ramping production with C281x devices, evaluate performance of the hardware design with both devices.

A supply voltage glitch or ESD will put the device in an unknown state. Therefore, it is important to have a good PCB layout for optimum noise and ESD performance.

The similar ESD protection diodes can be utilized for JTAG pins as well. Keep the loop area of critical traces (in this case, it would be JTAG, $\overline{\text{XRS}}$, X1,X2) as small as possible.

If your design needs to bring any pin like GPIO to a connector (for external connectivity) you need to take special ESD care by adding ESD protection parts.

Some systems may require mechanical fixes like metallic shielding, rerouting of cabling and so forth.

For additional information and guidelines for the PCB design for reduction of EMI/EMC issues, see the *PCB Design Guidelines For Reduced EMI* (SZZA009) and *Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility* (SDYA011).

6 Conclusion

The following topics were covered in this document:

- While using an external oscillator, pay close attention to the load capacitors values. If you are using an internal or external oscillator, place all parts close to pins with short traces.
- JTAG: Use <10 k pullup resistors on EMU0/EMU1 pins and ~ 2.2 k pulldown on a $\overline{\text{TRST}}$ pin. Place the JTAG connector within 6” of trace length from the DSC pins. Additional 0.1 μF filter capacitors on these pins will combat the noise.
- ADC: Use appropriate drivers providing low source impedance to connect analog signals. Add the correct value filter capacitors and bias resistor to ADCREF pins. Terminate all unused ADCIN pins. If the system needs to work in a wider temperature range, use an external voltage reference.
- Power Supply: Select the V_{DD} (3.3 V) and V_{CORE} voltage regulators that have a current capacity of ~ x2 total peak current and low noise/ripple. For the F281x design, pay close attention to power sequencing. For other DSCs, V_{CORE} should not come before V_{DD}. If ADC is used, isolate digital and analog supplies (using L-C filter) and the analog and digital grounds.
- Use bypass-capacitors on every power pin and place them directly below the pins.
- While placing the components, divide the circuitry so that the analog circuits are away from the high-current switching circuits.
- Provide the shortest ground return paths for all the high-frequency signals. It is highly recommended to use a separate ground plane (layer).
- Consider the EMI/EMC guidelines while designing your schematics and layout.

7 References

- *TMS320F2810, TMS320F2811, TMS320F2812, TMS320C2810, TMS320C2811, TMS320C2812, Digital Signal Processors Data Manual* (SPRS174)
- *TMS320F2809, TMS320F2808, TMS320F2806, TMS320F2802, TMS320F2801, TMS320C2802, TMS320C2801, and TMS320F2801x DSPs Data Manual* (SPRS230)
- *SN74LVC1G14 Single Schmitt-Trigger Inverter Data Sheet* (SCES218)
- *TMS320F28044 Digital Signal Processor Data Manual* (SPRS357)
- *TMS320F28335, TMS320F28334, TMS320F28332, Digital Signal Controllers (DSCs) Data Manual* (SPRS439)
- *TMS320F/C24x DSP Controllers CPU and Instruction Set Reference Guide* (SPRU160)
- *TMS320C28x DSP CPU and Instruction Set Reference Guide* (SPRU430)
- *Emulation Fundamentals for TI's DSP Solutions* (SPRA439)
- *High-Speed DSP Systems Design Reference Guide* (SPRU889)
- *An Overview of Designing Analog Interface With TMS320F28xx/28xxx DSCs* (SPRAAP6)
- *Implications of Slow or Floating CMOS Inputs* (SCBA004)
- *Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility* (SDYA011)
- *Circuit Board Layout Techniques* (SLOA089)
- *Latch-Up, ESD, and Other Phenomena* (SLYA014)
- *High-Speed Layout Guidelines* (SCAA082)
- *F2810, F2811, and F2812 ADC Calibration* (SPRA989)
- *TMS320280x and TMS3202801x ADC Calibration* (SPRAAD8)
- *Choosing and Using Bypass Capacitors*, Article, http://www.embedded.com/
- *PCB Design Guidelines For Reduced EMI* (SZZA009)
- *Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility* (SDYA011)
- *Reduced Electromagnetic Interference (EMI) With the TMS320C24x DSP* (SPRA501)
- *TPS767D3xx Dual-Output Low-Dropout Voltage Regulators Data Sheet* (SLVS209)
- *TMS320F2808 DSP Power Reference Design* (SLVA296)
- *SN54AC241, SN74AC241 Octal Buffers/Drivers With 3-State Output* (SCAS513)
- *ULN2001A, ULN2002A, ULN2003A, ULN2004A, ULQ2003A, ULQ2004A, High-Voltage High-Current Darlington Transistor Array* (SLRS027)
- *OPA376, OPA2376, OPA4376 Precision, Low Noise, Low Quiescent Current, Operational Amplifier Data Sheet* (SBOS406)
- *OPA343, OPA2343, OPA4343 Single-Supply, Rail-to-Rail Operational Amplifiers microAmplifiers Series* (SBOS090)
- *TLV2470, TLV2471, TLV2472, TLV2473, TLV2474, TLV2475, TLV247xA Family of 600 μA/CH 2.8 MHz Rail-to-Rail Input/Outpu High-Drive Operational Amplifiers With Shutdown* (SLOS232)
- *REF5020, REF5025, REF5030, REF5040, REF5045, REF5050 Low-Noise, Very Low Drift, Precision Voltage Reference Data Sheet* (SBOS410)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from C Revision (June 2015) to D Revision	Page
• Update was made in Section 3.2.	7
• Update was made in Section 3.4.1.	12

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