Application Report

Derating and Lifetime Calculations for Flip Chip On Lead Packages HotRod and FC-SOT

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ABSTRACT

The reliability of electronic packages plays an important role in the overall lifetime of a system. Failure mechanisms for Flip Chip On Lead (FCOL) packages such as HotRod or Flip Chip Small Outline Transistor (FC-SOT) are detailed and investigated experimentally. Texas Instruments (TI) has carried out an electromigration test for HotRod package at certain temperatures with given densities of electric current. Parameters of a kinetic model, Black's Equation, are determined from the test data. With those parameters, a derating curve is generated for customers to estimate the lifetime of a FCOL device under their use conditions. Higher junction temperatures lead to a reduced lifetime so improving cooling through PCB design is critical to meet application requirements.

Table of Contents

List of Figures

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1 Introduction

HotRod is a plastic QFN (Quad Flat No Leads) package with a flip chip inside. The power device or die is directly attached to the leadframe, as shown in Figure 1-1. Connection between die and leadframe is through the flip chip solder joints between Cu post and leadframe (see Figure 1-2). This construction results in an innovative package that has improved electrical and thermal performance over traditional leaded packages. For more details of the package structure, see *HotRod QFN Package PCB Attachment*.

FC-SOT is another type of flip chip package on leadframe. Its internal connection has the same structure as in HotRod (see Figure 1-2), but its external structure is different. Unlike HotRod packages in which the leads are molded with their bottom and end exposed, the leads of FC-SOT packages are not molded (see Figure 1-3).

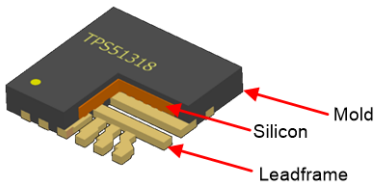

Figure 1-1. HotRod Structure and Die Attachment

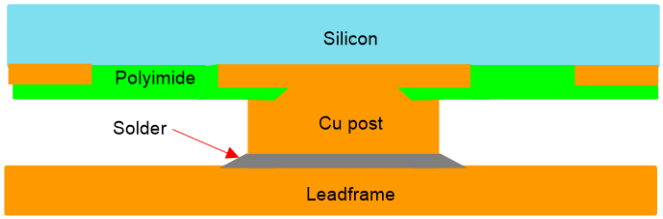

Figure 1-2. Cross Sectional Illustration of a Flip Chip Joint Inside HotRod and FC-SOT

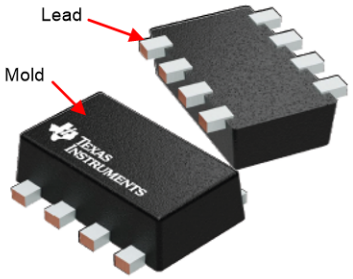

Figure 1-3. External Appearance of FC-SOT

As the industry has driven to smaller Flip Chip On Lead (FCOL) packages, like HotRod and FC-SOT, the size of interconnects has been greatly reduced. Thus, the density of electric current in the interconnects has been increased so much that Joule heating and electromigration could be major contributing factors for the failure of electronic packages.

This application report discusses the different failure mechanisms for FCOL packages. The experimental results of HotRod will then be used to model internal flip-chip joint reliability, thus providing a basis for derating curves that can help designers equate given qualification standards to their application-specific use cases.

Being aware of potential failure modes for FCOL packages and understanding the impact of high junction temperature and high current density on package lifetime is beneficial for system designers so that they can ensure that their design will meet system requirements in their application-specific use conditions.

2 Limiting Wear-Out Mechanism

- **HotRod packages**

  HotRod packages are molded and mechanically singulated from a matrix of leadframes. During surface mounting on the customer's printed circuit board (PCB), the leads are soldered on pads. Areas that could cause failure over time include:
  - Package molding compound
  - Internal and external solder joints as shown in Figure 2-1:
    - Flip chip joints between silicon die and leadframe inside package
    - Lead-to-pad joints between package and board

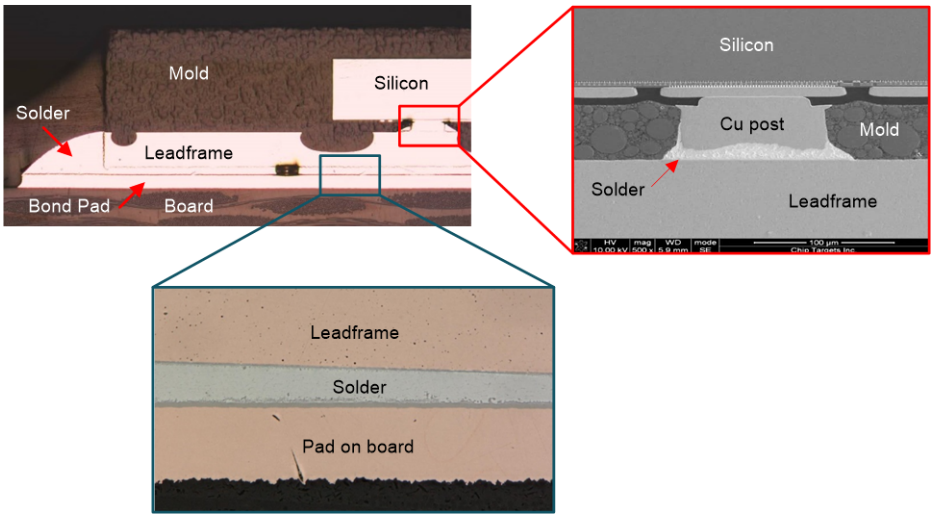

Figure 2-1. Cross Section of HotRod Mounted on Board

First, the integrity of the molding compound in HotRod packages after stressing has been investigated. No mold crack or delamination was found and molding compound lifetime was evaluated at 50k hours at 150°C. Therefore, wear out of molding compound is ruled out as a potential failure mechanism of HotRod packages.

Next, an experimental study of HotRod lead-to-pad joints found that the microstructure of solder joints was very different after stressing at 170°C compared with 150°C. After stressing with 2 amperes at 170°C for 800 hours, high level of voiding was observed in the joints. The Ni plating on the leadframe was completely consumed by solder reaction, forming Ni-Sn intermetallic compound (IMC) crystals. Sn atoms diffused through the channels among the IMC crystals to the Cu post, generating large voids in the bulk of solder. After stressing with 1 ampere at 150°C for 3500 hours, the Ni plating was still continuous and uniform in thickness. There was no void in either the bulk of solder or the interfacial region because diffusion of Sn was blocked by Ni plating. Though the electric current in the samples stressed at 170°C was twice of that in the samples stressed at 150°C, detailed analysis of the microstructure did not find any sign of electromigration in the solder joints, an indication that the high level of voiding in the solder joints from package to PCB after stressing at 170°C for 800 hours was a result of thermal exposure alone. As a result, there is a temperature boundary between 150°C and 170°C beyond which the solder joints from package to PCB will fail, though the exact temperature of this boundary was not yet determined. To be safe, the junction temperature in HotRod packages should not exceed 150°C to avoid external lead-to-pad solder joint failure.

Based on these results, the wear-out of the internal flip chip solder joints is the limiting failure mechanism for reliability of HotRod packages on board at temperatures below 150°C. This mechanism is discussed in Section 3.

- **FC-SOT packages**

  FC-SOT packages use the same set of packaging materials as HotRod packages. Since their leads are not molded, during reflow of PCB assembly, the molten solder not only wets the bottom and end of the leads, but also their top surface and side walls. After reflow, the leads are located inside the bulk of solder, as shown in Figure 2-2. Because of this, the external solder joints of FC-SOT to board are stronger than those of HotRod. They can tolerate higher level of voiding and withstand higher stress. Therefore, the wear out of the flip chip solder joints is the limiting mechanism for reliability of FC-SOT packages on board, similarly to HotRod packages.

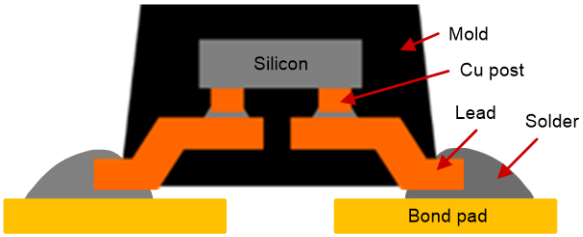

Figure 2-2. Cross Sectional Illustration of FC-SOT Structure and Solder Joints of Leads on Board

3 Influential Factors for Flip Chip Solder Joint Reliability

- **Effects of high temperature**

  When exposed to high temperature either due to ambient or Joule heating or both, diffusion of atoms is accelerated in the internal solder joints, causing fast growth of intermetallic compounds and formation of voids in the interface of the solder joints, which will eventually lead to package failure. The classic Arrhenius Equation can be used to describe the influence of temperature on package lifetime [1]:

$$MTTF = A \exp\left(\frac{E_a}{kT}\right) \quad (1)$$

  where,
  - MTTF: mean time to failure
  - A: empirical constant
  - T: temperature in Kelvin (°C+273.15)
  - E_a: activation energy in eV
  - k: Boltzman constant (8.616 X 10^5 eV/K)

- **Effect of current density**

  In addition to temperature, the flow of electric current can also affect the diffusion of atoms in the interconnects, a phenomenon known as electromigration. The driving force for electromigration is the momentum transfer from electrons to thermally activated atoms. The direction of atomic mass transport in electromigration is the same as the electron flow. Electromigration can cause depletion of metals and formation of voids at cathode and extrusion or hillock formation at anode, where mass flux divergence exists.

  In the industry, Black's Equation is widely accepted to model the performance of a package in electromigration testing. It is similar to the Arrhenius Equation, but with an additional factor describing the effect of electric current density on package reliability [2]:

$$MTTF = Aj^{-n} \exp\left(\frac{E_a}{kT}\right) \quad (2)$$

  where, j is the current density and n is the exponent for current density.

4 Determination of Model Parameters

Reliability of HotRod under the condition of high temperature and high current density has been characterized by electromigration testing. The test vehicle had Sn-Ag solder cap on bare Cu post and selective Ni/Pd/Au plating on leadframe. The stressing conditions: current density 11-12.5A (400-460 mA/μm^2); temperature on chip 144, 152, and 160°C.

During stressing, samples were put in an oil bath to effectively remove Joule heating and maintain uniformity and stability of temperature. The temperature of the Cu post joints to leadframe during testing was monitored using the on-chip temperature sensor, and the ambient temperature was adjusted to bring the Cu post temperature to the target temperature. The temperature difference between the sample and oil bath was controlled to be <10°C.

By fitting the experimental data of MTTF to Equation 2, the model parameters are determined: current density exponent n = 2.78 and activation energy Ea = 1.25 eV.

5 Derating With Temperature

- **Approach**

  Once the parameters in Equation 2 are determined from experimental data, the acceleration factor (AF) due to thermal effect alone can be calculated:

$$AF = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_{Use}} - \frac{1}{T_{Ref}}\right)\right] \quad (3)$$

  where, T_{Use} is the use temperature and T_{Ref} is the temperature at which a reference data point of package reliability was obtained; both temperatures are in Kelvin (°C+273.15); the electric current density is assumed the same under both conditions.

  The lifetime of the package under use condition can be calculated, or derating curves can be generated for different junction temperatures:

$$H_{Use} = AF \times H_{Ref} \quad (4)$$

  where, H_{Ref} is a reference data point and H_{Use} is the lifetime at use temperature. It should be noted that the type of the calculated lifetime from Equation 4 depends on the type of the reference data. For example, if a package has passed a certain amount of hours (H_{Ref}) at T_{Ref} in the high temperature storage test without failure, the number of hours HUse calculated from Equation 4 is the time the package is expected to pass at T_{Use} without failure.

- **Derating curve**

  TI's semiconductor technologies are developed with a minimum goal of fewer than 50 Failures in Time (FITs) at 100k Power-On-Hours (POH) and 105°C junction temperature, as stated in the Texas Instruments General Quality Guidelines. This means that, with the power constantly on (24 hours / 7 days per week), TI's semiconductor devices are typically expected to reach the normal or useful lifetime of 100k hours at 105°C with the maximum failure rate below 0.5%. Beyond that, the mechanisms of the end life of the silicon devices start to occur and failure rate increases. For the definition of normal life and FIT, see TI's reliability terminology page.

  Taking this 100k POH at 105°C as a reference data point and using the activation energy as determined in Section 4, a derating curve is generated from Equation 3 and Equation 4 for HotRod and FC-SOT packages, as shown in Figure 5-1. Since as pointed out above the type of the calculated lifetime by Equation 4 depends on the type of the reference data, the lifetime in Figure 5-1 is the guaranteed normal or useful life of the packages with the maximum failure rate less than 0.5%.

  As expected from the theory of atomic diffusion and its effect on solder joint reliability, a strong dependence of the package/solder joint lifetime on the junction temperature is clearly demonstrated in Figure 5-1. For example, if the junction temperature is 110°C, the lifetime of HotRod and FC-SOT packages will be about 7 years. If the junction temperature is increased to 115°C, their lifetime will be reduced to about 4 years.

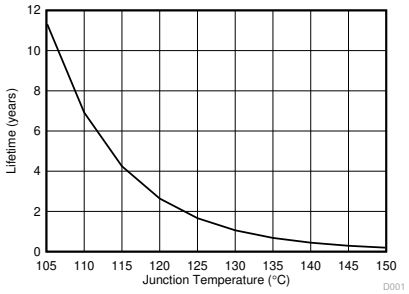

Figure 5-1. Derating Curve of HotRod and FC-SOT Packages (lifetime in years in the temperature of 105°C - 150°C)

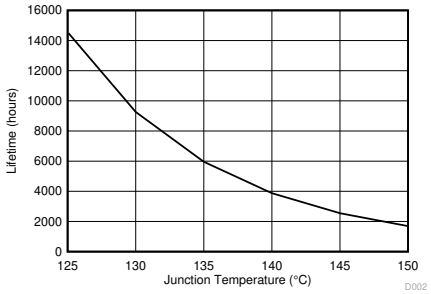

Figure 5-2. Derating Curve of HotRod and FC-SOT Packages (lifetime in hours in the temperature range of 125°C - 150°C)

6 PCB Design to Improve Cooling

Since the junction temperature has a great impact on package lifetime and board-level reliability, it is important to keep the junction temperature as low as possible. This can be realized by improving cooling through the PCB. There are several key variables that can be optimized to enable the best thermal performance of PCB:

The first key variable is the amount of copper connected to the device. Since HotRod and FC-SOT packages do not have a single thermal pad, connecting the high current pins to as large as possible areas of copper is the best approach. The optimal pins vary by device, but typically connecting the GND and VIN pins to large areas of copper is the easiest and provides the most benefits.

In applications where the board area may be limited, other methods to reduce the junction temperature are to increase the thickness of the copper layers or to use a multi-layer PCB with thermal vias pulling the heat into internal planes. For many applications, use of 2 oz copper can provide a significant reduction in temperatures compared to thinner copper.

Placing thermal vias as close to the device pins as possible can also help to draw the heat away from the device. Thermal vias are most commonly placed near the device's GND pin, as the vias can conduct the heat into large ground planes in the PCB.

Other system-level factors, such as any enclosure surrounding the board assembly, attachment of the board to an external body, and any forced airflow, can also aid in cooling the device. For more guidelines for PCB design for HotRod packages, see *HotRod QFN Package PCB Attachment*.

7 Summary

In summary, FCOL packages are susceptible to various failure mechanisms that are exacerbated at high temperatures. This means that the junction temperature in the application-specific use case has a large impact on package lifetime and board-level reliability.

For junction temperatures below 150°C, the internal solder joints between die and leadframe are the limiting factor and parameters in Black's Equation were experimentally determined to correlate the junction temperature and current density to the mean time to failure for FCOL packages. This model was used to estimate the lifetime at temperatures below 150°C based on known reference data from qualification results or industry standards. Junction temperatures above 150°C should be ruled out to avoid external lead-to-pad solder joint failures.

Overall, reducing the junction temperature at which FCOL packages such as HotRod or FC-SOT operate will help to extend the normal life of the device. Optimizing the thermal performance of the PCB layout is a step that systems designers can take to improve the lifetime of their design and meet requirements for their application.

8 References

1. JEDEC standard JEP122C, “Failure Mechanisms and Models for Semiconductor Devices”, March 2006. https://www.jedec.org/standards-documents/docs/jep-122e
2. S. Brandenburg and S. Yeh, “Electromigration study of flip chip bump solder joints”, Proc. Surface Mount Inter. Conf., San Jose, CA, August 1998, pp. 337–344.

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