

TMS320F28P55x Real-Time Microcontrollers

1 Features

- Real-time processing:
 - 150MHz C28x 32-bit DSP CPU
 - Equivalent to 300MHz Arm® Cortex®-M7 based device on real-time signal chain performance (see the [Real-time Benchmarks Showcasing C2000™ Control MCU's Optimized Signal Chain](#) Application Note)
 - IEEE 754 single-precision Floating-Point Unit (FPU32)
 - Trigonometric Math Unit (TMU)
 - Support for Nonlinear Proportional Integral Derivative (NLPID) control
 - Neural-Network Processing Unit (NNPU)
 - CRC Engine and Instructions (VCRC)
- Programmable Control Law Accelerator (CLA)
 - 150MHz
 - Equivalent to 200MHz Arm® Cortex®-M7 based device on real-time signal chain performance (see the [Real-time Benchmarks Showcasing C2000™ Control MCU's Optimized Signal Chain](#) Application Note)
 - IEEE 754 single-precision floating-point instructions
 - Executes code independently of main CPU
- On-chip memory
 - 1088KB of flash (ECC-protected) across five independent banks
 - Four 256KB banks
 - One 64KB bank, ideal of LFU/Bootloaders/ data
 - 8KB of OTP (One Time Programmable flash memory)
 - 133KB of RAM (ECC/Parity protected)
- Security
 - Secure Boot
 - JTAG Lock
 - Advanced Encryption Standard (AES) accelerator
 - Unique Identification (UID) number
- Clock and system control
 - Two internal 10MHz oscillators
 - Crystal oscillator or external clock input
 - Windowed watchdog timer module
 - Missing clock detection circuitry
 - Dual-clock Comparator (DCC)
- 3.3V I/O design
 - Internal VREG generation allows for single-supply design
 - Brownout reset (BOR) circuit
- 5V failsafe and tolerant capability on 4 GPIOs for PMBUS/I2C support
- Configurable 1.35V V_{IH} on 4 GPIOs
- System peripherals
 - 6-channel Direct Memory Access (DMA) controller
 - 91 individually programmable multiplexed General-Purpose Input/Output (GPIO) pins (22 shared with Analog)
 - 17 digital inputs on analog pins
 - Enhanced Peripheral Interrupt Expansion (ePIE)
 - Multiple low-power mode (LPM) support
- Communications peripherals
 - One Power-Management Bus (PMBus) interface
 - Fast Plus Mode Support - 1MHz SCL
 - 5V/3.3V/1.35V V_{IH} support on select pins
 - Two Inter-integrated Circuit (I2C) interfaces
 - Two Controller Area Network with Flexible Data-Rate (CAN FD/MCAN) bus port
 - 4KB message RAM per MCAN module, independent of system memory
 - Ability to re-use RAM for CPU data variables if MCAN is not used
 - One Universal Serial Bus (USB 2.0 MAC + PHY)
 - Two Serial Peripheral Interface (SPI) ports
 - Three UART-compatible Serial Communication Interface (SCI)
 - One UART-compatible Local Interconnect Network (LIN) interface
- Analog system
 - Five 3.9MSPS, 12-bit Analog-to-Digital Converters (ADCs)
 - Up to 39 external channels (includes one gpdac output)
 - Four integrated Post-Processing Blocks (PPB) per ADC
 - Four windowed comparators (CMPSS) with 12-bit reference Digital-to-Analog Converters (DACs)
 - Digital glitch filters
 - Low DAC output to pin capability on CMPSS1
 - One 12-bit buffered DAC output
 - Three Programmable Gain Amplifiers (PGAs)
 - Unity gain support
 - Inverting and non-inverting gain mode support
 - Programmable output filtering



- Enhanced control peripherals
 - 24 ePWM channels with 16 channels that have high-resolution capability (150ps resolution)
 - Integrated dead-band support
 - Integrated hardware trip zones (TZs)
 - Two Enhanced Capture (eCAP) modules
 - Three Enhanced Quadrature Encoder Pulse (eQEP) modules with support for CW/CCW operation modes
 - Embedded Pattern Generator (EPG)
 - Configurable Logic Block (CLB)
 - 2 tiles
 - Augments existing peripheral capability
 - Supports position manager solutions
 - Live Firmware Update (LFU)
 - Diagnostic features
 - Memory Power-On Self-Test (MPOST)
 - **Functional Safety-Compliant targeted**
 - Developed for functional safety applications
 - Documentation available to aid ISO 26262 and IEC 61508 system design
 - Systematic capability up to ASIL D and SIL 3 targeted
 - Hardware integrity up to ASIL B targeted
 - Safety-related certification
 - ISO 26262 certification up to ASIL B by TÜV SÜD planned
 - Package options:
 - 128-pin Thin Quad Flatpack (TQFP) [PDT suffix]
 - 100-pin Low-profile Quad Flatpack (LQFP) [PZ suffix]
 - 80-pin TQFP [PNA suffix]
 - 64-pin LQFP [PM suffix]
 - 56-pin Very Thin Quad Flatpack No-Lead (VQFN) [RSH suffix]
 - Temperature options:
 - Junction (T_J): –40°C to 150°C
- ## 2 Applications
- Appliances
 - [Air conditioner outdoor unit](#)
 - Building automation
 - [Door operator drive control](#)
 - Industrial machine & machine tools
 - [Automated sorting equipment](#)
 - [Textile machine](#)
 - AC inverter & VF drives
 - [AC drive control module](#)
 - [AC drive position feedback](#)
 - [AC drive power stage module](#)
 - Linear motor transport systems
 - [Linear motor power stage](#)
 - Single & multi axis servo drives
 - [Servo drive position feedback](#)
 - [Servo drive power stage module](#)
 - Speed controlled BLDC drives
 - [AC-input BLDC motor drive](#)
 - [DC-input BLDC motor drive](#)
 - Factory automation
 - [Robot servo drive](#)
 - [Mobile robot motor control](#)
 - [Position sensor](#)
 - Industrial power
 - [Industrial AC-DC](#)
 - UPS
 - [Three-phase UPS](#)
 - [Single-phase online UPS](#)
 - Telecom & server power
 - [Merchant DC/DC](#)
 - [Merchant network & server PSU](#)
 - [Merchant telecom rectifiers](#)
 - Hybrids, electric & powertrain systems
 - [DC/DC converter](#)
 - [Inverter & motor control](#)
 - [On-board \(OBC\) & wireless charger](#)
 - [Virtual engine sound system \(VESS\)](#)
 - [Engine fan](#)
 - [eTurbo/charger](#)
 - [Pump](#)
 - [Electric power steering \(EPS\)](#)
 - Infotainment and cluster
 - [Head-up display](#)
 - [Automotive head unit](#)
 - [Automotive external amplifier](#)
 - Body electronics & lighting
 - [Automotive HVAC compressor module](#)
 - [DC/AC inverter](#)
 - [Headlight](#)
 - ADAS
 - [Mechanically scanning LIDAR](#)
 - EV charging infrastructure
 - [AC charging \(pile\) station](#)
 - [DC charging \(pile\) station](#)
 - [EV charging station power module](#)
 - [Wireless EV charging station](#)
 - Renewable energy storage
 - [Energy storage power conversion system \(PCS\)](#)
 - [Portable Power Station](#)

- Solar energy
 - Central inverter
 - Micro inverter
 - Solar power optimizer
- Solar arc protection
- Rapid shutdown
- String inverter

3 Description

The TMS320F28P55x (F28P55x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such [applications](#) as:

- [Motor drives](#)
- [Appliances](#)
- [Hybrid, electric & powertrain systems](#)
- [Solar & EV charging](#)
- [Digital power](#)
- [Body electronics & lighting](#)
- [Test & measurement](#)

The [real-time control subsystem](#) is based on TI's 32-bit C28x DSP core, which provides 150MHz of signal-processing performance for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the [Floating-Point Unit \(FPU\)](#), [Trigonometric Math Unit \(TMU\)](#), and [VCRC \(Cyclical Redundancy Check\) extended instruction sets](#), speeding up common algorithms key to real-time control systems.

The CLA allows significant offloading of common tasks from the main C28x CPU. The CLA is an independent 32-bit floating-point math accelerator that executes in parallel with the CPU. Additionally, the CLA has its own dedicated memory resources and it can directly access the key peripherals that are required in a typical control system. Support of a subset of ANSI C is standard, as are key features like hardware breakpoints and hardware task-switching.

The F28P55x supports up to 1088KB of flash memory divided into four 256KB banks plus one 64KB bank, which enable programming one bank and execution in another bank in parallel. Up to 133KB of on-chip SRAM is also available to supplement the flash memory.

The Live Firmware Update hardware enhancements on F28P55x allow fast context switching from the old firmware to the new firmware to minimize application downtime when updating the device firmware.

High-performance analog blocks are integrated on the F28P55x real-time microcontroller (MCU) and are closely coupled with the processing and PWM units to provide optimal real-time signal chain performance. Twenty-four PWM channels, all supporting frequency-independent resolution modes, enable control of various power stages from a 3-phase inverter to power factor correction and advanced multilevel power topologies.

The inclusion of the Configurable Logic Block (CLB) allows the user to add [custom logic](#) and potentially [integrate FPGA-like functions](#) into the C2000 real-time MCU.

Interfacing is supported through various industry-standard communication ports (such as SPI, SCI, I2C, PMBus, LIN, and CAN FD) and offers [multiple pin-muxing options](#) for optimal signal placement.

Want to learn more about features that make C2000 Real-Time MCUs the right choice for your real-time control system? Check out [The Essential Guide for Developing With C2000™ Real-Time Microcontrollers](#) and visit the [C2000™ real-time control MCUs](#) page.

The [Getting Started With C2000™ Real-Time Control Microcontrollers \(MCUs\) Getting Started Guide](#) covers all aspects of development with C2000 devices from hardware to support resources. In addition to key reference documents, each section provides relevant links and resources to further expand on the information covered.

Ready to get started? Check out the [TMDSCNCD28P55X](#) evaluation board or the [LAUNCHXL-F28P55X](#) development kit, and download [C2000Ware](#).

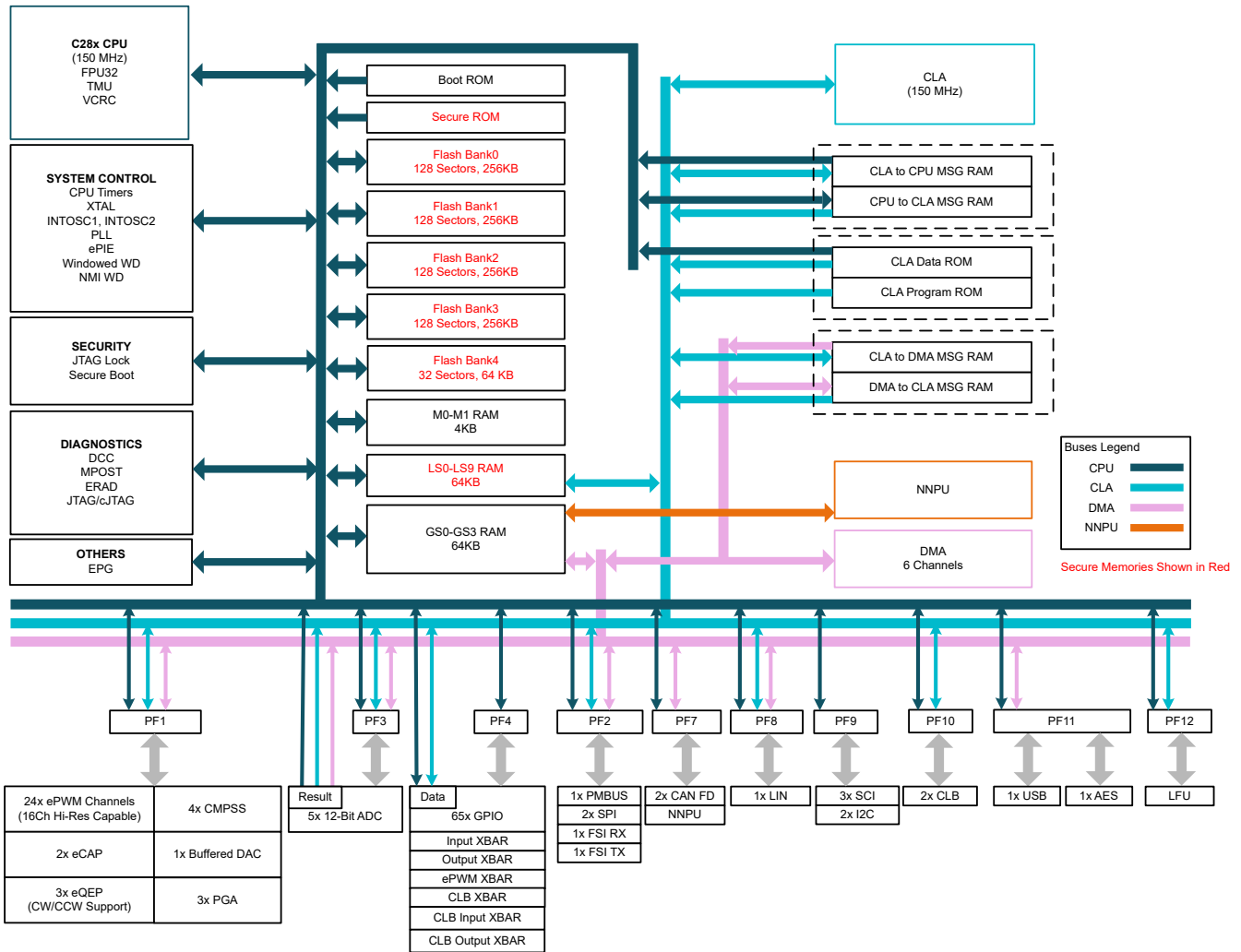
Package Information

| PART NUMBER ⁽¹⁾ | PACKAGE ⁽²⁾ | PACKAGE SIZE ⁽³⁾ |
|----------------------------|------------------------|-----------------------------|
| TMS320F28P559SJ-Q1 | PDT (QFP, 128) | 16mm x 16mm |
| | PZ (QFP, 100) | 16mm x 16mm |
| | PNA (QFP, 80) | 12mm x 12mm |
| | PM (QFP, 64) | 12mm x 12mm |
| TMS320F28P550SJ | PDT (QFP, 128) | 16mm x 16mm |
| | PZ (QFP, 100) | 16mm x 16mm |
| | PNA (QFP, 80) | 12mm x 12mm |
| | PM (QFP, 64) | 12mm x 12mm |
| | RSH (VQFN, 56) | 7mm x 7mm |
| TMS320F28P559SG-Q1 | PDT (QFP, 128) | 16mm x 16mm |
| | PZ (QFP, 100) | 16mm x 16mm |
| | PNA (QFP, 80) | 12mm x 12mm |
| | PM (QFP, 64) | 12mm x 12mm |
| TMS320F28P550SG | PDT (QFP, 128) | 16mm x 16mm |
| | PZ (QFP, 100) | 16mm x 16mm |
| | PNA (QFP, 80) | 12mm x 12mm |
| | PM (QFP, 64) | 12mm x 12mm |
| | RSH (VQFN, 56) | 7mm x 7mm |
| TMS320F28P550SD | PZ (QFP, 100) | 16mm x 16mm |
| | PNA (QFP, 80) | 12mm x 12mm |
| | PM (QFP, 64) | 12mm x 12mm |
| | RSH (VQFN, 56) | 7mm x 7mm |

- (1) For more information on these devices, see the *Device Comparison* table.
- (2) For more information, see the *Mechanical, Packaging and Orderable Information* section.
- (3) Package size (length x width) is a nominal value and includes pins, where applicable

ADVANCE INFORMATION

3.1 Functional Block Diagram



ADVANCE INFORMATION

- A. The internal DAC from one of the CMPSS modules can be configured as an output DAC.
- B. The LIN module can also be used as a SCI module.

Figure 3-1. Functional Block Diagram

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4 Device Comparison

Table 4-1. Device Comparison

| FEATURE ^{(1) (4)} | | F28P559SJ-Q1 ⁽³⁾ | F28P550SJ | F28P559SG-Q1 ⁽³⁾ | F28P550SG | F28P550SD |
|--|----------------------------------|--|-----------|---|-----------|-------------------------|
| C28x Subsystem | | | | | | |
| Frequency (MHz) | | 150 | | | | |
| C28x | 32-bit Floating-Point Unit (FPU) | Yes | | | | |
| | VCRC | Yes | | | | |
| | TMU - Type 1 | Yes - Type 1 - NLPID Instruction Supported | | | | |
| CLA - Type 2 | Number | 1: F28P559SJ9-Q1, F28P559SJ6-Q1 0: F28P559SJ2-Q1 | 1 | 1: F28P559SG9-Q1, F28P559SG8-Q1 0: F28P559SG2-Q1 | 1 | |
| | Frequency (MHz) | 150 | | | | |
| 6-Channel DMA - Type 0 | | 1 | | | | |
| External Interrupts | | 5 | | | | |
| MIPS | | 300 (CPU + CLA) | | | | |
| Memory | | | | | | |
| Flash | Main Array | 1MB (4 x 256KB Banks) | | 512KB (2 x 256KB Banks) | | 256KB (2 x 128KB Banks) |
| | 64KB Bank | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ6-Q1, F28P550SJ6, F28P559SG9-Q1, F28P550SG9 | | | | - |
| | User OTP | 8KB | | 2KB | | |
| RAM | Dedicated | 4KB | | | | |
| | Local Shared RAM | 64KB | | | | 32KB |
| | Message | 1KB | | | | |
| | Global Shared RAM | 64KB | | 32KB | | |
| | Total RAM | 133KB | | 101KB | | 69KB |
| Message RAM Types | C28x CPUs and CLAs | 512 bytes (256 bytes per direction) | | | | |
| | DMAs and CLAs | 512 bytes (256 bytes per direction) | | | | |
| ECC | | FLASH, Mx RAM | | | | |
| Parity | | ROM, CAN RAM, Message RAM, LSx RAM, GSx RAM | | | | |
| System | | | | | | |
| Configurable Logic Block (CLB) | | 2 tiles - F28P559SJ9-Q1, F28P559SJ6-Q1, F28P550SJ9, F28P550SJ6, F28P559SG9-Q1, F28P550SG9, F28P559SG8-Q1, F28P550SG8, F28P550SD7 | | | | |
| Neural-Network Processing Unit (NNPU) | | 1 - F28P559SJ9-Q1, F28P550SJ9, F28P559SG9-Q1, F28P550SG9 | | | | - |
| Embedded Pattern Generator (EPG) | | 1 | | | | |
| 32-bit CPU Timers | | 3 | | | | |
| Advanced Encryption Standard (AES) Accelerator | | 1 | | | | |
| Live Firmware Update (LFU) Support | | Yes, with enhancements and flash bank erase time improvements | | | | |
| Security for on-chip flash and RAM | | Yes | | | | |
| Zero-pin Boot | | Yes | | | | |
| Secure Boot | | Yes | | | | |
| JTAG Lock | | Yes | | | | |
| MPOST | | Yes | | | | |
| Embedded Real-time Analysis and Diagnostic (ERAD) - Type 2 | | 1 | | | | |
| Non-maskable Interrupt Watchdog (NMIWD) timers | | 1 | | | | |
| Watchdog (WD) timers | | 1 | | | | |
| Crystal oscillator/External clock input | | 1 | | | | |
| Internal Oscillator (Optional External Precision Resistor) | | 2 | | | | |

ADVANCE INFORMATION

Table 4-1. Device Comparison (continued)

| FEATURE ^{(1) (4)} | | F28P559SJ-Q1 ⁽³⁾ | F28P550SJ | F28P559SG-Q1 ⁽³⁾ | F28P550SG | F28P550SD | |
|--|--|---|-----------|---|-----------|-----------|---|
| Digital and Analog Pin Counts | | | | | | | |
| GPIO | 128-pin PDT | 65 | | 65 - F28P559SG9-Q1, F28P550SG9 | | - | |
| | 100-pin PZ | 43 | | | | | |
| | 80-pin PNA | 32 | | | | | |
| | 64-pin PM | 17 | | | | | |
| | 56-pin RSH | - | 15 | - | 15 | | |
| | Additional GPIO | 4 (2 from cJTAG and 2 from X1/X2) | | | | | |
| AIO (analog with digital inputs) | 128-pin PDT | 17 | | 17 - F28P559SG9-Q1, F28P550SG9 | | - | |
| | 100-pin PZ | 16 | | | | | |
| | 80-pin PNA | 12 | | | | | |
| | 64-pin PM | 12 | | | | | |
| | 56-pin RSH | - | 12 | - | 12 | | |
| AGPIO (analog with digital inputs and outputs) | 128-pin PDT | 22 | | 22 - F28P559SG9-Q1, F28P550SG9 | | - | |
| | 100-pin PZ | 19 | | | | | |
| | 80-pin PNA | 16 | | | | | |
| | 64-pin PM | 16 | | | | | |
| | 56-pin RSH | - | 14 | - | 14 | | |
| C28x Analog Peripherals⁽⁵⁾ | | | | | | | |
| Analog-to-Digital Converter (ADC) (12-bit) - Type 6 | Number of ADCs | 5 | | | | | |
| | MSPS | 3.9 | | | | | |
| | Conversion Time (ns) ⁽²⁾ | 187 | | | | | |
| ADC Input channels (single-ended) (includes the two DAC outputs) | 128-pin PDT | 39 | | 39 - F28P559SG9-Q1, F28P550SG9 | | - | |
| | 100-pin PZ | 35 | | | | | |
| | 80-pin PNA | 28 | | | | | |
| | 64-pin PM | 28 | | | | | |
| | 56-pin RSH | - | 26 | - | 26 | | |
| PGA - Type 2 | | | | | | 3 | |
| Temperature Sensor | | | | | | 1 | |
| Comparator subsystem (CMPSS) (each CMPSS has two comparators and two internal DACs) - Type 6 | | | | | | 4 | |
| Buffered Digital-to-Analog Converter (DAC) - Type 2 | | | | | | 1 | |
| DAC Out from CMPSS | | | | | | 1 | |
| C28x Control Peripherals⁽⁵⁾ | | | | | | | |
| eCAP - Type 2 | Total inputs | 2 | | | | | |
| ePWM/HRPWM - Type 4 | Total channels | 24 - F28P559SJ9-Q1, F28P559SJ6-Q1 16 - F28P559J2-Q1 | 24 | 24 - F28P559SG9-Q1, F28P559SG8-Q1 16 - F28P559SG2 | 24 | | |
| | Channels with high-resolution capability | 12- F28P559SJ9-Q1, F28P559SJ6-Q1 8 - F28P559SJ2-Q1 | 12 | 12 - F28P559SG9-Q1, F28P559SG8-Q1 8 - F28P559SG2 | 12 | | |
| eQEP modules - Type 2 | | | | | | 3 | |
| C28x Communications Peripherals⁽⁵⁾ | | | | | | | |
| CAN with Flexible Data-Rate (CAN-FD) - Type 2 | | | | | | | 2 |
| Fast Serial Interface (FSI) RX - Type 2 | | | | | | | 1 |
| Fast Serial Interface (FSI) TX - Type 2 | | | | | | | 1 |
| Inter-Integrated Circuit (I2C) - Type 2 | | | | | | | 2 |
| Local Interconnect Network (LIN) - Type 1 | | | | | | | 1 |
| Power Management Bus (PMBus) - Type 1 | | | | | | | 1 |
| Serial Communications Interface (SCI) - Type 0 (UART-compatible) | | | | | | | 3 |
| Serial Peripheral Interface (SPI) - Type 2 | | | | | | | 2 |
| Universal Serial Bus (USB) - Type 0 | | 1 - F28P559SJ9-Q1, F28P550SJ9, F28P559SJ6-Q1, F28P550SJ6 | | 1 - F28P559SG9-Q1, F28P550SG9 | | - | |

ADVANCE INFORMATION

Table 4-1. Device Comparison (continued)

| FEATURE ^{(1) (4)} | | F28P559SJ-Q1 ⁽³⁾ | F28P550SJ | F28P559SG-Q1 ⁽³⁾ | F28P550SG | F28P550SD |
|--|-------------|--|------------------------------------|-----------------------------|------------------------------------|-----------|
| Temperature and Qualification | | | | | | |
| Junction temperature (T _J) | | -40°C to 150°C | | | | |
| Free-Air temperature (T _A) | | -40°C to 125°C | | | | |
| Package Options | 128-pin PDT | F28P559SJ9-Q1, F28P559SJ6-Q1, F28P559SJ2-Q1, F28P550SJ9, F28P550SJ6, F28P559SG9-Q1, F28P550SG9 | | | | - |
| | 100-pin PZ | F28P559SJ9-Q1, F28P559SJ6-Q1, F28P559SJ2-Q1, F28P550SJ9, F28P550SJ6, F28P559SG9-Q1, F28P559SG8-Q1, F28P559SG2-Q1, F28P550SG9, F28P550SG8, F28P550SD7 | | | | |
| | 80-pin PNA | F28P559SJ9-Q1, F28P559SJ6-Q1, F28P559SJ2-Q1, F28P550SJ9, F28P550SJ6, F28P559SG9-Q1, F28P559SG8-Q1, F28P559SG2-Q1, F28P550SG9, F28P550SG8, F28P550SD7 | | | | |
| | 64-pin PM | F28P559SJ9-Q1, F28P559SJ6-Q1, F28P559SJ2-Q1, F28P550SJ9, F28P550SJ6, F28P559SG9-Q1, F28P559SG8-Q1, F28P559SG2-Q1, F28P550SG9, F28P550SG8, F28P550SD7 | | | | |
| | 56-pin RSH | - | F28P550SJ9, F28P550SJ6, F28P550SG9 | - | F28P550SG9, F28P550SG8, F28P550SD7 | |

- (1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. For more information, see the [C2000 Real-Time Control Peripherals Reference Guide](#).
- (2) Time between start of sample-and-hold window to start of sample-and-hold window of the next conversion.
- (3) The suffix -Q1 refers to AEC Q100 qualification for automotive applications.
- (4) "-" on the feature entry indicates that the corresponding package type is not available.
- (5) For devices that are available in more than one package, the peripheral count listed in the smaller package is reduced because the smaller package has less device pins available. The number of peripherals internally present on the device is not reduced compared to the largest package offered within a part number.

4.1 Related Products

[TMS320F280013x Real-Time Microcontrollers](#)

The F280013x has common pinouts with the F28P55x series of devices. The F28P55x series adds CLA and DMA support, in addition to faster CPU clock speed and increased memory size. Additionally the F28P55x has Programmable Gain Amplifiers(PGA), USB, CLB and supports live FW update.

[TMS320F28015x Real-Time Microcontrollers](#)

The F280015x has common pinouts with the F28P55x series of devices. The F28P55x series adds CLA and DMA support, in addition to faster CPU clock speed and increased memory size. Additionally the F28P55x has Programmable Gain Amplifiers(PGA), USB, CLB and supports live FW update. The F280015x series has lockstep C28x CPUs for safety related systems.

[TMS320F28003x Real-Time Microcontrollers](#)

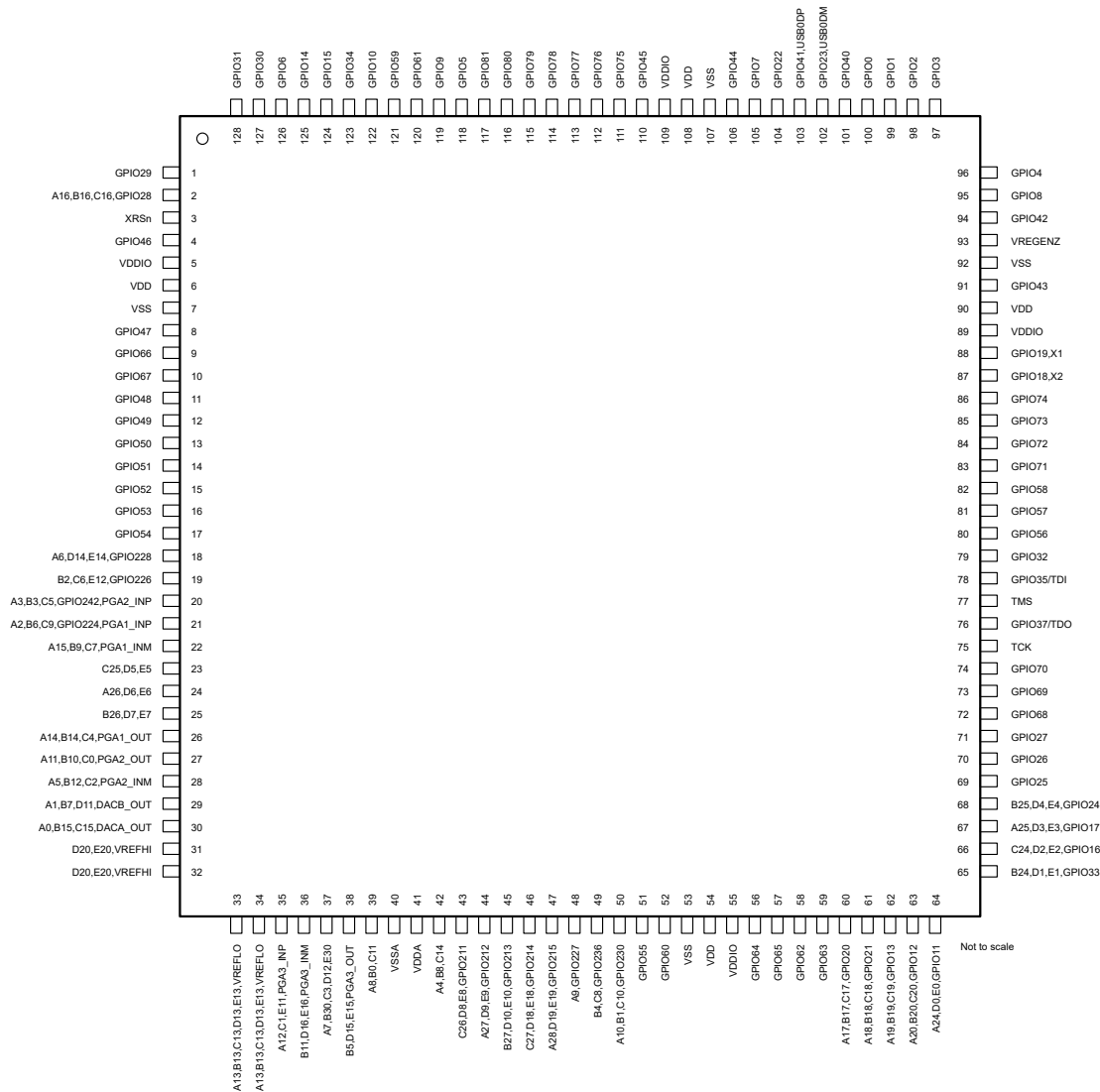
The F28003x has common pinouts with the F28P55x series of devices. The F28P55x series has a faster overall CPU clock and increased memory options in addition to Programmable Gain Amplifiers(PGA) and USB support. The F28003x series offers SDFM support, along with BGCRC and HWBIST.

5 Pin Configuration and Functions

5.1 Pin Diagrams

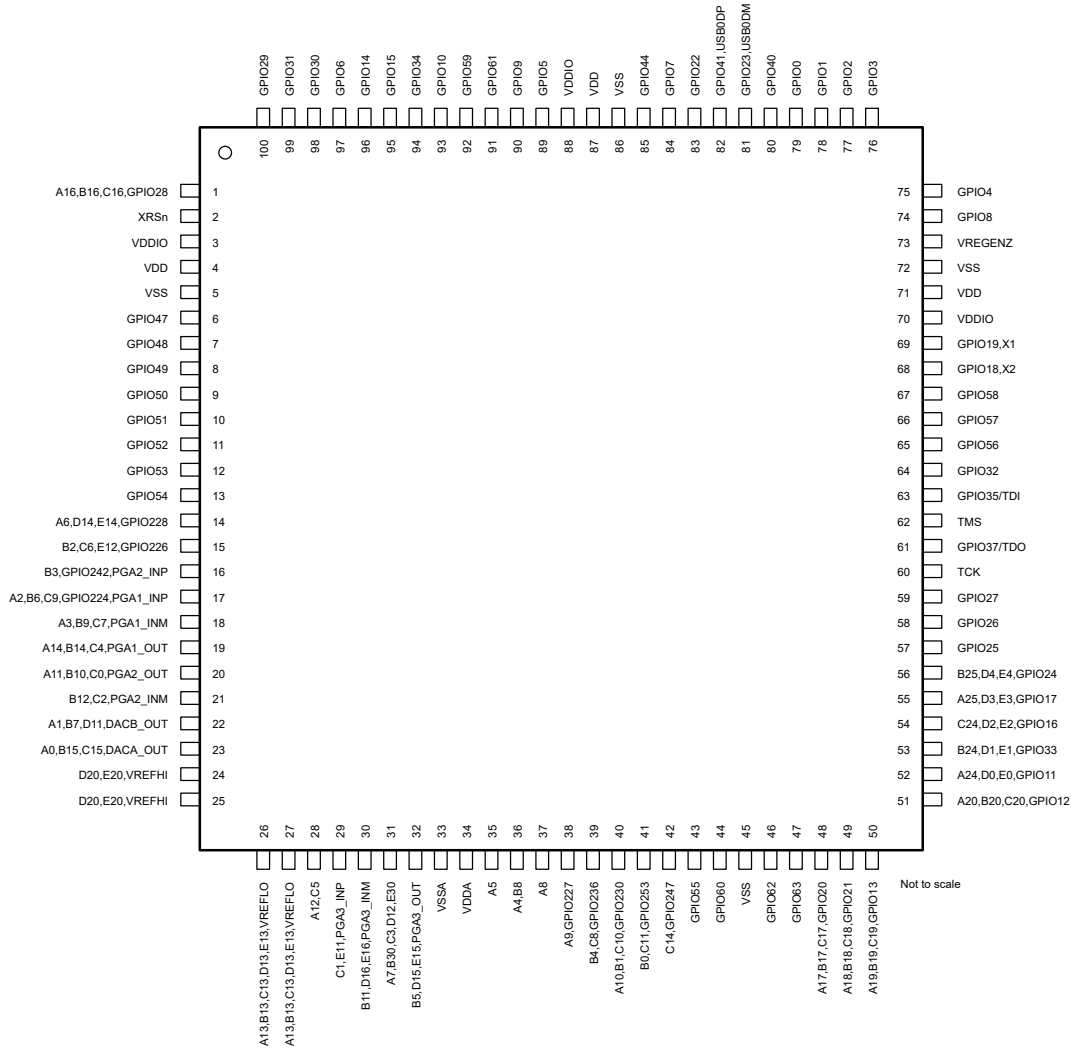
Figure 5-1 shows the pin assignments on the 128-pin PDT thin quad flatpack. Figure 5-2 shows the pin assignments on the 100-pin PZ low-profile quad flatpack. Figure 5-3 shows the pin assignments on the 80-pin PNA thin quad flatpack. Figure 5-4 shows the pin assignments on the 64-pin PM low-profile quad flatpack. Figure 5-5 shows the pin assignments on the 56-pin RSH very thin quad flatpack no-lead.

ADVANCE INFORMATION



A. Only the GPIO function is shown on GPIO pins. See the *Pin Attributes* table for the complete, muxed signal name.

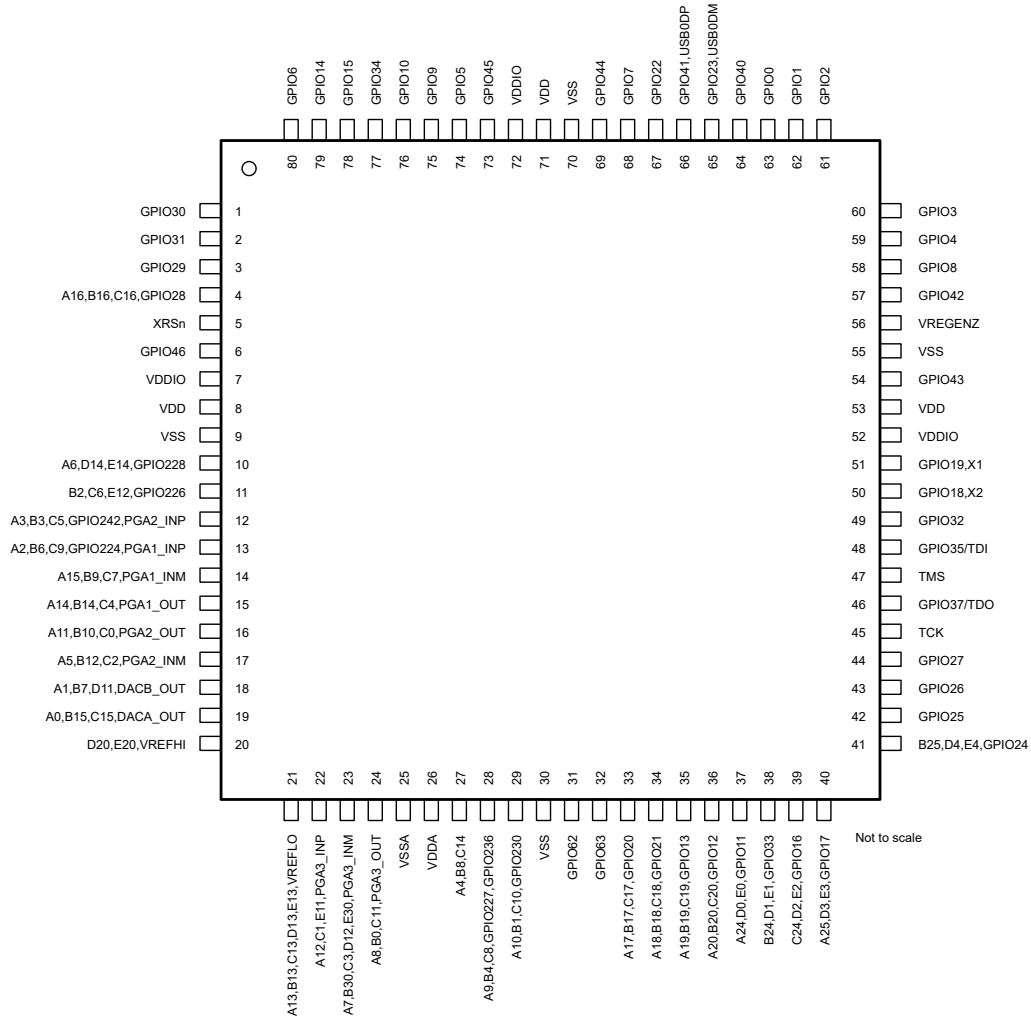
Figure 5-1. 128-pin PDT Thin Quad Flatpack (Top View)



ADVANCE INFORMATION

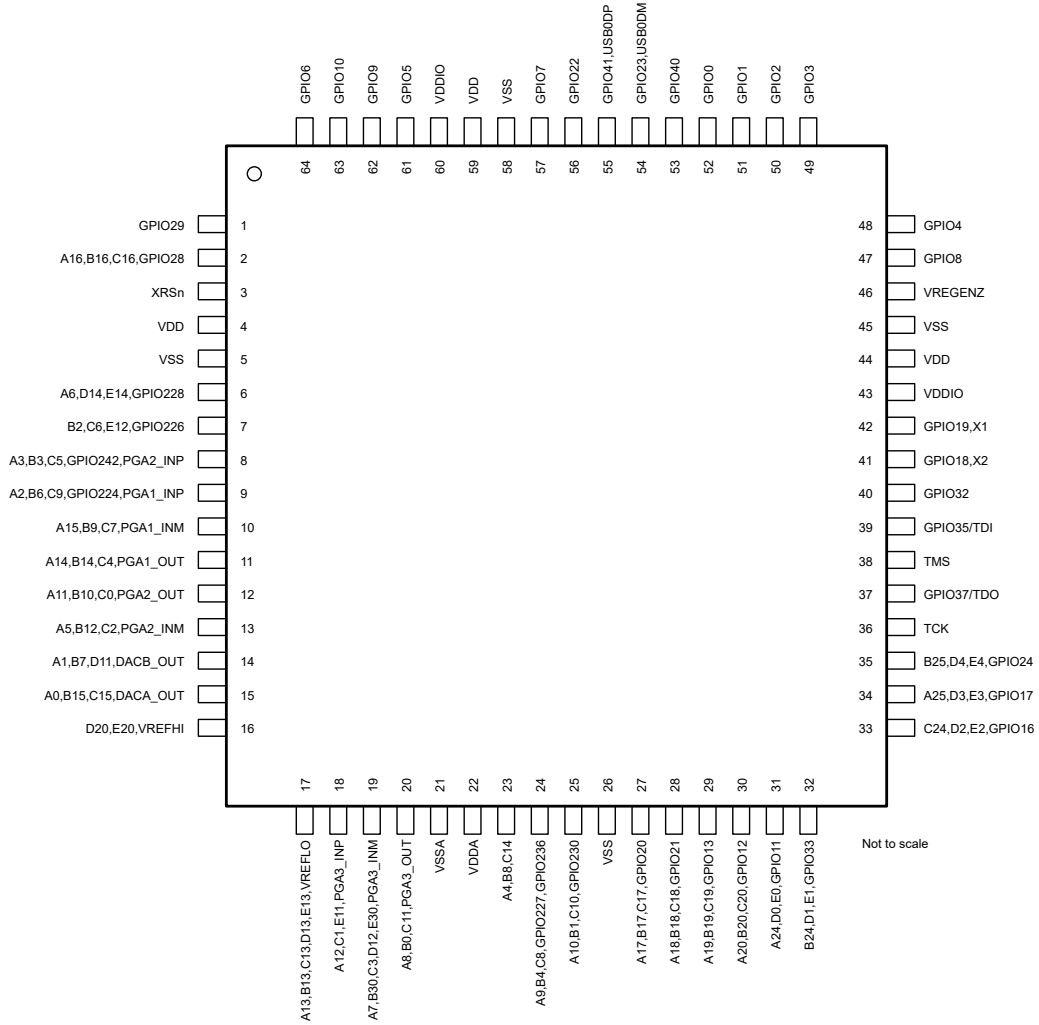
A. Only the GPIO function is shown on GPIO pins. See the *Pin Attributes* table for the complete, muxed signal name.

Figure 5-2. 100-Pin PZ Low-Profile Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO pins. See the *Pin Attributes* table for the complete, muxed signal name.

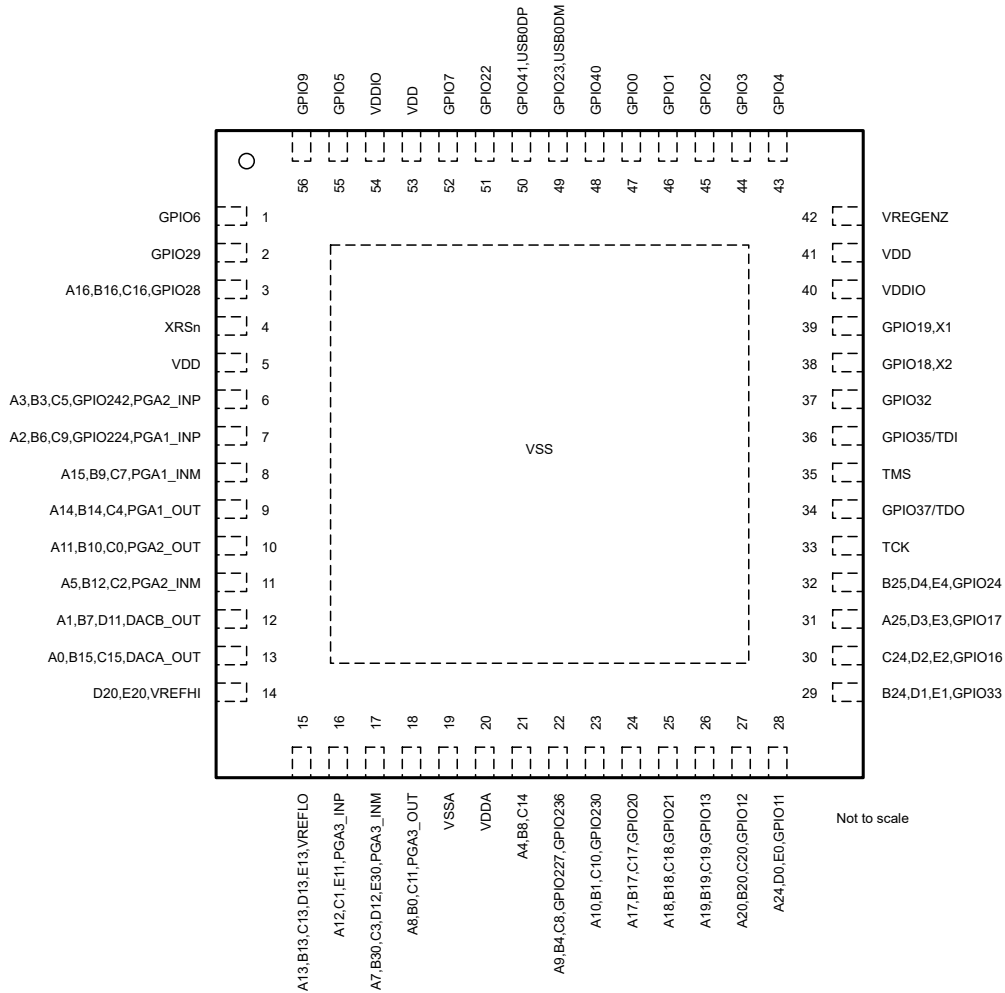
Figure 5-3. 80-Pin PNA Thin Quad Flatpack (Top View)



ADVANCE INFORMATION

A. Only the GPIO function is shown on GPIO pins. See the *Pin Attributes* table for the complete, muxed signal name.

Figure 5-4. 64-Pin PM Low-Profile Quad Flatpack (Top View)



A. Only the GPIO function is shown on GPIO pins. See the *Pin Attributes* table for the complete, muxed signal name.

Figure 5-5. 56-Pin RSH Very Thin Quad Flatpack No-Lead (Top View)

5.2 Pin Attributes

Table 5-1. Pin Attributes

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---------------|--------------|------------|-----------|--------|----------|--------|-------------|---|
| ANALOG | | | | | | | | |
| A0 | | | | | | | I | ADC-A Input 0 |
| B15 | | | | | | | I | ADC-B Input 15 |
| C15 | | | | | | | I | ADC-C Input 15 |
| CMP3_HP2 | | 30 | 23 | 19 | 15 | 13 | I | CMPSS-3 High Comparator Positive Input 2 |
| CMP3_LP2 | | | | | | | I | CMPSS-3 Low Comparator Positive Input 2 |
| DACA_OUT | | | | | | | O | Buffered DAC-A Output. |
| AIO231 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 231 |
| A1 | | | | | | | I | ADC-A Input 1 |
| B7 | | | | | | | I | ADC-B Input 7 |
| CMP1_HP4 | | 29 | 22 | 18 | 14 | 12 | I | CMPSS-1 High Comparator Positive Input 4 |
| CMP1_LP4 | | | | | | | I | CMPSS-1 Low Comparator Positive Input 4 |
| D11 | | | | | | | I | ADC-D Input 11 |
| DACB_OUT | | | | | | | O | Buffered DAC-B Output. |
| AIO232 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 232 |
| A2 | | | | | | | I | ADC-A Input 2 |
| B6 | | | | | | | I | ADC-B Input 6 |
| C9 | | | | | | | I | ADC-C Input 9 |
| CMP1_HP0 | | 21 | 17 | 13 | 9 | 7 | I | CMPSS-1 High Comparator Positive Input 0 |
| CMP1_LP0 | | | | | | | I | CMPSS-1 Low Comparator Positive Input 0 |
| GPIO224 | | | | | | | I/O | General-Purpose Input Output 224 This pin also has digital mux functions which are described in the GPIO section of this table. |
| PGA1_INP | | | | | | | I | PGA-1 Plus |
| A3 | | | | | | | I | ADC-A Input 3 |
| CMP3_HP5 | | | 18 | | | | I | CMPSS-3 High Comparator Positive Input 5 |
| CMP3_LP5 | | | | | | | I | CMPSS-3 Low Comparator Positive Input 5 |
| AIO229 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 229 |
| A3 | | 20 | | 12 | 8 | 6 | I | ADC-A Input 3 |
| CMP3_HP5 | | | | | | | I | CMPSS-3 High Comparator Positive Input 5 |
| CMP3_LP5 | | | | | | | I | CMPSS-3 Low Comparator Positive Input 5 |
| A4 | | | | | | | I | ADC-A Input 4 |
| B8 | | | | | | | I | ADC-B Input 8 |
| CMP2_HP0 | | 42 | 36 | 27 | 23 | 21 | I | CMPSS-2 High Comparator Positive Input 0 |
| CMP2_LP0 | | | | | | | I | CMPSS-2 Low Comparator Positive Input 0 |
| AIO225 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 225 |
| A5 | | | | | | | I | ADC-A Input 5 |
| CMP2_HP5 | | | 35 | | | | I | CMPSS-2 High Comparator Positive Input 5 |
| CMP2_LP5 | | | | | | | I | CMPSS-2 Low Comparator Positive Input 5 |
| AIO249 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 249 |
| A5 | | | | | | | I | ADC-A Input 5 |
| CMP2_HP5 | | 28 | | 17 | 13 | 11 | I | CMPSS-2 High Comparator Positive Input 5 |
| CMP2_LP5 | | | | | | | I | CMPSS-2 Low Comparator Positive Input 5 |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|--------------|------------|-----------|-----------|----------|-----------|--|--|
| A6 CMP1_HP2 CMP1_LP2 D14 E14 GPIO228 | | 18 | 14 | 10 | 6 | | I I I I I I/O | ADC-A Input 6 CMPSS-1 High Comparator Positive Input 2 CMPSS-1 Low Comparator Positive Input 2 ADC-D Input 14 ADC-E Input 14 General-Purpose Input Output 228 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A7 B30 C3 CMP4_HN1 CMP4_HP1 CMP4_LN1 CMP4_LP1 D12 E30 AIO245 | 0, 4, 8, 12 | 37 | 31 | 23 | 19 | 17 | I I I I I I I I I I | ADC-A Input 7 ADC-B Input 30 ADC-C Input 3 CMPSS-4 High Comparator Negative Input 1 CMPSS-4 High Comparator Positive Input 1 CMPSS-4 Low Comparator Negative Input 1 CMPSS-4 Low Comparator Positive Input 1 ADC-D Input 12 ADC-E Input 30 Analog Pin Used For Digital Input 245 |
| A8 CMP4_HP4 CMP4_LP4 AIO240 | 0, 4, 8, 12 | | 37 | | | | I I I I | ADC-A Input 8 CMPSS-4 High Comparator Positive Input 4 CMPSS-4 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 240 |
| A8 B0 C11 CMP4_HP4 CMP4_LP4 AIO241 | 0, 4, 8, 12 | 39 | | 24 | 20 | 18 | I I I I I I | ADC-A Input 8 ADC-B Input 0 ADC-C Input 11 CMPSS-4 High Comparator Positive Input 4 CMPSS-4 Low Comparator Positive Input 4 Analog Pin Used For Digital Input 241 |
| A9 CMP2_HP2 CMP2_LP2 GPIO227 | | 48 | 38 | 28 | 24 | 22 | I I I I/O | ADC-A Input 9 CMPSS-2 High Comparator Positive Input 2 CMPSS-2 Low Comparator Positive Input 2 General-Purpose Input Output 227 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A10 B1 C10 CMP2_HN0 CMP2_HP3 CMP2_LN0 CMP2_LP3 GPIO230 | | 50 | 40 | 29 | 25 | 23 | I I I I I I I I/O | ADC-A Input 10 ADC-B Input 1 ADC-C Input 10 CMPSS-2 High Comparator Negative Input 0 CMPSS-2 High Comparator Positive Input 3 CMPSS-2 Low Comparator Negative Input 0 CMPSS-2 Low Comparator Positive Input 3 General-Purpose Input Output 230 This pin also has digital mux functions which are described in the GPIO section of this table. |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|--|--------------|------------|-----------|--------|----------|--------|---|--|
| A11 B10 C0 CMP1_HN1 CMP1_HP1 CMP1_LN1 CMP1_LP1 PGA2_OUT AIO237 | 0, 4, 8, 12 | 27 | 20 | 16 | 12 | 10 | I I I I I I I O I | ADC-A Input 11 ADC-B Input 10 ADC-C Input 0 CMPSS-1 High Comparator Negative Input 1 CMPSS-1 High Comparator Positive Input 1 CMPSS-1 Low Comparator Negative Input 1 CMPSS-1 Low Comparator Positive Input 1 PGA-2 Output Analog Pin Used For Digital Input 237 |
| A12 CMP2_HN1 CMP2_HP1 CMP2_LN1 CMP2_LP1 AIO238 | 0, 4, 8, 12 | 35 | 28 | 22 | 18 | 16 | I I I I I I | ADC-A Input 12 CMPSS-2 High Comparator Negative Input 1 CMPSS-2 High Comparator Positive Input 1 CMPSS-2 Low Comparator Negative Input 1 CMPSS-2 Low Comparator Positive Input 1 Analog Pin Used For Digital Input 238 |
| A13 B13 C13 D13 E13 VREFLO AIO235 | 0, 4, 8, 12 | 34 | 26 | 21 | 17 | 15 | I I I I I I I | ADC-A Input 13 ADC-B Input 13 ADC-C Input 13 ADC-D Input 13 ADC-E Input 13 ADC Low Reference Analog Pin Used For Digital Input 235 |
| A13 B13 C13 D13 E13 VREFLO AIO235 | ALT | 33, 34 | 26, 27 | 21 | 17 | 15 | I I I I I I I | ADC-A Input 13 ADC-B Input 13 ADC-C Input 13 ADC-D Input 13 ADC-E Input 13 ADC Low Reference Analog Pin Used For Digital Input 235 |
| A14 B14 C4 CMP3_HP4 CMP3_LP4 PGA1_OUT AIO239 | 0, 4, 8, 12 | 26 | 19 | 15 | 11 | 9 | I I I I I O I | ADC-A Input 14 ADC-B Input 14 ADC-C Input 4 CMPSS-3 High Comparator Positive Input 4 CMPSS-3 Low Comparator Positive Input 4 PGA-1 Output Analog Pin Used For Digital Input 239 |
| A15 CMP1_HN0 CMP1_HP3 CMP1_LN0 CMP1_LP3 AIO233 | 0, 4, 8, 12 | 22 | | 14 | 10 | 8 | I I I I I | ADC-A Input 15 CMPSS-1 High Comparator Negative Input 0 CMPSS-1 High Comparator Positive Input 3 CMPSS-1 Low Comparator Negative Input 0 CMPSS-1 Low Comparator Positive Input 3 Analog Pin Used For Digital Input 233 |
| A16 B16 C16 GPIO28 | | 2 | 1 | 4 | 2 | 3 | I I I I/O | ADC-A Input 16 ADC-B Input 16 ADC-C Input 16 General-Purpose Input Output 28 This pin also has digital mux functions which are described in the GPIO section of this table. |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------------------------|--------------|---------|--------|--------|-------|--------|------------------|---|
| A17 B17 C17 | | 60 | 48 | 33 | 27 | 24 | I I I | ADC-A Input 17 ADC-B Input 17 ADC-C Input 17 |
| GPIO20 | | | | | | | I/O | General-Purpose Input Output 20 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A18 B18 C18 | | 61 | 49 | 34 | 28 | 25 | I I I | ADC-A Input 18 ADC-B Input 18 ADC-C Input 18 |
| GPIO21 | | | | | | | I/O | General-Purpose Input Output 21 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A19 B19 C19 | | 62 | 50 | 35 | 29 | 26 | I I I | ADC-A Input 19 ADC-B Input 19 ADC-C Input 19 |
| GPIO13 | | | | | | | I/O | General-Purpose Input Output 13 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A20 B20 C20 | | 63 | 51 | 36 | 30 | 27 | I I I | ADC-A Input 20 ADC-B Input 20 ADC-C Input 20 |
| GPIO12 | | | | | | | I/O | General-Purpose Input Output 12 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A24 D0 E0 | | 64 | 52 | 37 | 31 | 28 | I I I | ADC-A Input 24 ADC-D Input 0 ADC-E Input 0 |
| GPIO11 | | | | | | | I/O | General-Purpose Input Output 11 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A25 D3 E3 | | 67 | 55 | 40 | 34 | 31 | I I I | ADC-A Input 25 ADC-D Input 3 ADC-E Input 3 |
| GPIO17 | | | | | | | I/O | General-Purpose Input Output 17 This pin also has digital mux functions which are described in the GPIO section of this table. |
| A26 D6 E6 | | 24 | | | | | I I I | ADC-A Input 26 ADC-D Input 6 ADC-E Input 6 |
| AIO209 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 209 |
| A27 AIO227 D9 E9 | | 44 | | | | | I I I I | ADC-A Input 27 Analog Pin Used For Digital Input 227 ADC-D Input 9 ADC-E Input 9 |
| A28 AIO243 D19 E19 | | 47 | | | | | I I I I | ADC-A Input 28 Analog Pin Used For Digital Input 243 ADC-D Input 19 ADC-E Input 19 |
| B0 C11 CMP2_HP3 CMP2_LP3 | | | 41 | | | | I I I I | ADC-B Input 0 ADC-C Input 11 CMPSS-2 High Comparator Positive Input 3 CMPSS-2 Low Comparator Positive Input 3 |
| GPIO231 | | | | | | | I/O | General-Purpose Input Output 231 This pin also has digital mux functions which are described in the GPIO section of this table. |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|---|--------------|---------|--------|--------|-------|--------|--------------------------------------|--|
| B2 C6 CMP3_HP0 CMP3_LP0 E12 GPIO226 | | 19 | 15 | 11 | 7 | | I I I I I I/O | ADC-B Input 2 ADC-C Input 6 CMPSS-3 High Comparator Positive Input 0 CMPSS-3 Low Comparator Positive Input 0 ADC-E Input 12 General-Purpose Input Output 226 This pin also has digital mux functions which are described in the GPIO section of this table. |
| B3 CMP3_HN0 CMP3_HP3 CMP3_LN0 CMP3_LP3 GPIO242 PGA2_INP | | 20 | 16 | 12 | 8 | 6 | I I I I I I/O I | ADC-B Input 3 CMPSS-3 High Comparator Negative Input 0 CMPSS-3 High Comparator Positive Input 3 CMPSS-3 Low Comparator Negative Input 0 CMPSS-3 Low Comparator Positive Input 3 General-Purpose Input Output 242 This pin also has digital mux functions which are described in the GPIO section of this table. PGA-2 Plus |
| B4 C8 CMP4_HP0 CMP4_LP0 GPIO236 | 0, 4, 8, 12 | 49 | 39 | 28 | 24 | 22 | I I I I I/O | ADC-B Input 4 ADC-C Input 8 CMPSS-4 High Comparator Positive Input 0 CMPSS-4 Low Comparator Positive Input 0 General-Purpose Input Output 236 This pin also has digital mux functions which are described in the GPIO section of this table. |
| B5 CMP1_HP5 CMP1_LP5 D15 E15 AIO252 | 0, 4, 8, 12 | 38 | 32 | | | | I I I I I I | ADC-B Input 5 CMPSS-1 High Comparator Positive Input 5 CMPSS-1 Low Comparator Positive Input 5 ADC-D Input 15 ADC-E Input 15 Analog Pin Used For Digital Input 252 |
| B9 C7 PGA1_INM | | 22 | 18 | 14 | 10 | 8 | I I I | ADC-B Input 9 ADC-C Input 7 PGA-1 Minus |
| B11 CMP4_HP5 CMP4_LP5 D16 E16 AIO251 | 0, 4, 8, 12 | 36 | 30 | | | | I I I I I I | ADC-B Input 11 CMPSS-4 High Comparator Positive Input 5 CMPSS-4 Low Comparator Positive Input 5 ADC-D Input 16 ADC-E Input 16 Analog Pin Used For Digital Input 251 |
| B12 C2 CMP3_HN1 CMP3_HP1 CMP3_LN1 CMP3_LP1 PGA2_INM AIO244 | 0, 4, 8, 12 | 28 | 21 | 17 | 13 | 11 | I I I I I I I I | ADC-B Input 12 ADC-C Input 2 CMPSS-3 High Comparator Negative Input 1 CMPSS-3 High Comparator Positive Input 1 CMPSS-3 Low Comparator Negative Input 1 CMPSS-3 Low Comparator Positive Input 1 PGA-2 Minus Analog Pin Used For Digital Input 244 |
| B24 D1 E1 GPIO33 | | 65 | 53 | 38 | 32 | 29 | I I I I/O | ADC-B Input 24 ADC-D Input 1 ADC-E Input 1 General-Purpose Input Output 33 This pin also has digital mux functions which are described in the GPIO section of this table. |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-------------|--------------|---------|--------|--------|-------|--------|----------|---|
| B25 | | | | | | | I | ADC-B Input 25 |
| D4 | | | | | | | I | ADC-D Input 4 |
| E4 | | 68 | 56 | 41 | 35 | 32 | I | ADC-E Input 4 |
| GPIO24 | | | | | | | I/O | General-Purpose Input Output 24 This pin also has digital mux functions which are described in the GPIO section of this table. |
| B26 | | | | | | | I | ADC-B Input 26 |
| D7 | | 25 | | | | | I | ADC-D Input 7 |
| E7 | | | | | | | I | ADC-E Input 7 |
| AIO210 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 210 |
| AIO228 | | | | | | | I | Analog Pin Used For Digital Input 228 |
| B27 | | 45 | | | | | I | ADC-B Input 27 |
| D10 | | | | | | | I | ADC-D Input 10 |
| E10 | | | | | | | I | ADC-E Input 10 |
| C1 | | | | | | | I | ADC-C Input 1 |
| CMP4_HP2 | | | | | | | I | CMPSS-4 High Comparator Positive Input 2 |
| CMP4_LP2 | | 35 | 29 | 22 | 18 | 16 | I | CMPSS-4 Low Comparator Positive Input 2 |
| E11 | | | | | | | I | ADC-E Input 11 |
| PGA3_INP | | | | | | | I | PGA-3 Plus |
| AIO248 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 248 |
| C5 | | 20 | 28 | 12 | 8 | 6 | I | ADC-C Input 5 |
| C14 | | | | | | | I | ADC-C Input 14 |
| CMP4_HN0 | | | | | | | I | CMPSS-4 High Comparator Negative Input 0 |
| CMP4_HP3 | | | | | | | I | CMPSS-4 High Comparator Positive Input 3 |
| CMP4_LN0 | | | 42 | | | | I | CMPSS-4 Low Comparator Negative Input 0 |
| CMP4_LP3 | | | | | | | I | CMPSS-4 Low Comparator Positive Input 3 |
| GPIO247 | | | | | | | I/O | General-Purpose Input Output 247 This pin also has digital mux functions which are described in the GPIO section of this table. |
| C14 | | | | | | | I | ADC-C Input 14 |
| CMP4_HN0 | | 42 | | 27 | 23 | 21 | I | CMPSS-4 High Comparator Negative Input 0 |
| CMP4_HP3 | | | | | | | I | CMPSS-4 High Comparator Positive Input 3 |
| CMP4_LN0 | | | | | | | I | CMPSS-4 Low Comparator Negative Input 0 |
| CMP4_LP3 | | | | | | | I | CMPSS-4 Low Comparator Positive Input 3 |
| C24 | | | | | | | I | ADC-C Input 24 |
| D2 | | | | | | | I | ADC-D Input 2 |
| E2 | | 66 | 54 | 39 | 33 | 30 | I | ADC-E Input 2 |
| GPIO16 | | | | | | | I/O | General-Purpose Input Output 16 This pin also has digital mux functions which are described in the GPIO section of this table. |
| AIO253 | | | | | | | I | Analog Pin Used For Digital Input 253 |
| C25 | | | | | | | I | ADC-C Input 25 |
| D5 | | 23 | | | | | I | ADC-D Input 5 |
| E5 | | | | | | | I | ADC-E Input 5 |
| AIO208 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 208 |
| AIO226 | | | | | | | I | Analog Pin Used For Digital Input 226 |
| C26 | | 43 | | | | | I | ADC-C Input 26 |
| D8 | | | | | | | I | ADC-D Input 8 |
| E8 | | | | | | | I | ADC-E Input 8 |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|---------|--------|--------|-------|--------|----------|---|
| AIO242 | | | | | | | I | Analog Pin Used For Digital Input 242 |
| C27 | | 46 | | | | | I | ADC-C Input 27 |
| D18 | | | | | | | I | ADC-D Input 18 |
| E18 | | | | | | | I | ADC-E Input 18 |
| D20 | | | | | | | I | ADC-D Input 20 |
| E20 | | | | | | | I | ADC-E Input 20 |
| VREFHI | | 31 | 24 | 20 | 16 | 14 | I | ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2- μ F capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. |
| AIO234 | 0, 4, 8, 12 | | | | | | I | Analog Pin Used For Digital Input 234 |
| D20 | | | | | | | I | ADC-D Input 20 |
| E20 | | | | | | | I | ADC-E Input 20 |
| VREFHI | | 32 | 25 | 20 | 16 | 14 | I | ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2- μ F capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. |
| AIO234 | ALT | | | | | | I | Analog Pin Used For Digital Input 234 |
| PGA3_INM | | 36 | 30 | 23 | 19 | 17 | I | PGA-3 Minus |
| PGA3_OUT | | 38 | 32 | 24 | 20 | 18 | O | PGA-3 Output |
| GPIO | | | | | | | | |
| GPIO236 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 236 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM7_A | 1 | 49 | 39 | 28 | 24 | 22 | O | ePWM-7 Output A |
| EQEP1_INDEX | 5 | | | | | | I/O | eQEP-1 Index |
| EPWM12_A | 9 | | | | | | O | ePWM-12 Output A |
| GPIO0 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 0 |
| EPWM1_A | 1 | | | | | | O | ePWM-1 Output A |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| SCIA_RX | 5 | | | | | | I | SCI-A Receive Data |
| I2CA_SDA | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SPIA_PTE | 7 | 100 | 79 | 63 | 52 | 47 | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| MCANA_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| CLB_OUTPUTXBAR8 | 11 | | | | | | O | CLB Output X-BAR Output 8 |
| EQEP1_INDEX | 13 | | | | | | I/O | eQEP-1 Index |
| EPWM3_A | 15 | | | | | | O | ePWM-3 Output A |
| GPIO1 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 1 |
| EPWM1_B | 1 | | | | | | O | ePWM-1 Output B |
| SCIA_TX | 5 | | | | | | O | SCI-A Transmit Data |
| I2CA_SCL | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SPIA_POCI | 7 | 99 | 78 | 62 | 51 | 46 | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| EQEP1_STROBE | 9 | | | | | | I/O | eQEP-1 Strobe |
| MCANA_TX | 10 | | | | | | O | CAN/CAN FD Transmit |
| CLB_OUTPUTXBAR7 | 11 | | | | | | O | CLB Output X-BAR Output 7 |
| EPWM10_B | 13 | | | | | | O | ePWM-10 Output B |
| EPWM3_B | 15 | | | | | | O | ePWM-3 Output B |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|--------|----------|--------|-------------|--|
| GPIO2 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 2 |
| EPWM2_A | 1 | | | | | | O | ePWM-2 Output A |
| OUTPUTXBAR1 | 5 | | | | | | O | Output X-BAR Output 1 |
| PMBUSA_SDA | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SPIA_PICO | 7 | | | | | | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| SCIA_TX | 9 | 98 | 77 | 61 | 50 | 45 | O | SCI-A Transmit Data |
| FSIRXA_D1 | 10 | | | | | | I | FSIRX-A Optional Additional Data Input |
| I2CB_SDA | 11 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| EPWM10_A | 13 | | | | | | O | ePWM-10 Output A |
| MCANB_TX | 14 | | | | | | O | CAN/CAN FD Transmit |
| EPWM4_A | 15 | | | | | | O | ePWM-4 Output A |
| GPIO3 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 3 |
| EPWM2_B | 1 | | | | | | O | ePWM-2 Output B |
| OUTPUTXBAR2 | 2, 5 | | | | | | O | Output X-BAR Output 2 |
| PMBUSA_SCL | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SPIA_CLK | 7 | | | | | | I/O | SPI-A Clock |
| SCIA_RX | 9 | 97 | 76 | 60 | 49 | 44 | I | SCI-A Receive Data |
| FSIRXA_D0 | 10 | | | | | | I | FSIRX-A Primary Data Input |
| I2CB_SCL | 11 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| MCANB_RX | 14 | | | | | | I | CAN/CAN FD Receive |
| EPWM4_B | 15 | | | | | | O | ePWM-4 Output B |
| GPIO4 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 4 |
| EPWM3_A | 1 | | | | | | O | ePWM-3 Output A |
| I2CA_SCL | 2 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| MCANA_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| OUTPUTXBAR3 | 5 | | | | | | O | Output X-BAR Output 3 |
| SPIB_CLK | 7 | | | | | | I/O | SPI-B Clock |
| EQEP2_STROBE | 9 | 96 | 75 | 59 | 48 | 43 | I/O | eQEP-2 Strobe |
| FSIRXA_CLK | 10 | | | | | | I | FSIRX-A Input Clock |
| CLB_OUTPUTXBAR6 | 11 | | | | | | O | CLB Output X-BAR Output 6 |
| EPWM11_B | 13 | | | | | | O | ePWM-11 Output B |
| SPIA_POCI | 14 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| EPWM1_A | 15 | | | | | | O | ePWM-1 Output A |
| GPIO5 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 5 |
| EPWM3_B | 1 | | | | | | O | ePWM-3 Output B |
| I2CA_SDA | 2 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| OUTPUTXBAR3 | 3 | | | | | | O | Output X-BAR Output 3 |
| MCANA_RX | 5 | | | | | | I | CAN/CAN FD Receive |
| SPIA_PTE | 7 | 118 | 89 | 74 | 61 | 55 | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| FSITXA_D1 | 9 | | | | | | O | FSITX-A Optional Additional Data Output |
| CLB_OUTPUTXBAR5 | 10 | | | | | | O | CLB Output X-BAR Output 5 |
| SCIA_RX | 11 | | | | | | I | SCI-A Receive Data |
| EPWM1_B | 15 | | | | | | O | ePWM-1 Output B |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|-----------|----------|-----------|-------------|--|
| GPIO6 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 6 |
| EPWM4_A | 1 | | | | | | O | ePWM-4 Output A |
| OUTPUTXBAR4 | 2 | | | | | | O | Output X-BAR Output 4 |
| SYNCOUT | 3 | | | | | | O | External ePWM Synchronization Pulse |
| EQEP1_A | 5 | 126 | 97 | 80 | 64 | 1 | I | eQEP-1 Input A |
| SPIB_POCI | 7 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| FSITXA_D0 | 9 | | | | | | O | FSITX-A Primary Data Output |
| FSITXA_D1 | 11 | | | | | | O | FSITX-A Optional Additional Data Output |
| CLB_OUTPUTXBAR8 | 14 | | | | | | O | CLB Output X-BAR Output 8 |
| EPWM2_A | 15 | | | | | | O | ePWM-2 Output A |
| GPIO7 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 7 |
| EPWM4_B | 1 | | | | | | O | ePWM-4 Output B |
| EPWM2_A | 2 | | | | | | O | ePWM-2 Output A |
| OUTPUTXBAR5 | 3 | | | | | | O | Output X-BAR Output 5 |
| EQEP1_B | 5 | | | | | | I | eQEP-1 Input B |
| SPIB_PICO | 7 | 105 | 84 | 68 | 57 | 52 | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| FSITXA_CLK | 9 | | | | | | O | FSITX-A Output Clock |
| CLB_OUTPUTXBAR2 | 10 | | | | | | O | CLB Output X-BAR Output 2 |
| SCIA_TX | 11 | | | | | | O | SCI-A Transmit Data |
| MCANA_TX | 14 | | | | | | O | CAN/CAN FD Transmit |
| EPWM2_B | 15 | | | | | | O | ePWM-2 Output B |
| GPIO8 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 8 |
| EPWM5_A | 1 | | | | | | O | ePWM-5 Output A |
| ADCSOAO | 3 | | | | | | O | ADC Start of Conversion A for External ADC |
| EQEP1_STROBE | 5 | | | | | | I/O | eQEP-1 Strobe |
| SCIA_TX | 6 | 95 | 74 | 58 | 47 | | O | SCI-A Transmit Data |
| SPIA_PICO | 7 | | | | | | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| I2CA_SCL | 9 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| FSITXA_D1 | 10 | | | | | | O | FSITX-A Optional Additional Data Output |
| CLB_OUTPUTXBAR5 | 11 | | | | | | O | CLB Output X-BAR Output 5 |
| EPWM11_A | 13 | | | | | | O | ePWM-11 Output A |
| GPIO9 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 9 |
| EPWM5_B | 1 | | | | | | O | ePWM-5 Output B |
| SCIB_TX | 2 | | | | | | O | SCI-B Transmit Data |
| OUTPUTXBAR6 | 3 | | | | | | O | Output X-BAR Output 6 |
| EQEP1_INDEX | 5 | | | | | | I/O | eQEP-1 Index |
| SCIA_RX | 6 | | | | | | I | SCI-A Receive Data |
| SPIA_CLK | 7 | 119 | 90 | 75 | 62 | 56 | I/O | SPI-A Clock |
| I2CA_SCL | 9 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| FSITXA_D0 | 10 | | | | | | O | FSITX-A Primary Data Output |
| LINA_RX | 11 | | | | | | I | LIN-A Receive |
| PMBUSA_SCL | 13 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| I2CB_SCL | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| EQEP3_B | 15 | | | | | | I | eQEP-3 Input B |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|-----------|----------|-----------|-------------|---|
| GPIO10 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 10 |
| EPWM6_A | 1 | | | | | | O | ePWM-6 Output A |
| ADCSOCBO | 3 | | | | | | O | ADC Start of Conversion B for External ADC |
| EQEP1_A | 5 | | | | | | I | eQEP-1 Input A |
| SCIB_TX | 6 | | | | | | O | SCI-B Transmit Data |
| SPIA_POCI | 7 | 122 | 93 | 76 | 63 | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| I2CA_SDA | 9 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| FSITXA_CLK | 10 | | | | | | O | FSITX-A Output Clock |
| LINA_TX | 11 | | | | | | O | LIN-A Transmit |
| EQEP3_STROBE | 13 | | | | | | I/O | eQEP-3 Strobe |
| CLB_OUTPUTXBAR4 | 15 | | | | | | O | CLB Output X-BAR Output 4 |
| GPIO11 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 11 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM6_B | 1 | | | | | | O | ePWM-6 Output B |
| MCANA_RX | 2 | | | | | | I | CAN/CAN FD Receive |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| EQEP1_B | 5 | | | | | | I | eQEP-1 Input B |
| SCIB_RX | 6 | 64 | 52 | 37 | 31 | 28 | I | SCI-B Receive Data |
| SPIA_PTE | 7 | | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| FSIRXA_D1 | 9 | | | | | | I | FSIRX-A Optional Additional Data Input |
| LINA_RX | 10 | | | | | | I | LIN-A Receive |
| EQEP2_A | 11 | | | | | | I | eQEP-2 Input A |
| SPIA_PICO | 13 | | | | | | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| EQEP3_INDEX | 15 | | | | | | I/O | eQEP-3 Index |
| GPIO12 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 12 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM7_A | 1 | | | | | | O | ePWM-7 Output A |
| MCANA_RX | 3 | | | | | | I | CAN/CAN FD Receive |
| EQEP1_STROBE | 5 | | | | | | I/O | eQEP-1 Strobe |
| SCIB_TX | 6 | 63 | 51 | 36 | 30 | 27 | O | SCI-B Transmit Data |
| PMBUSA_CTL | 7 | | | | | | I/O | PMBus-A Control Signal - Target Input/Controller Output |
| FSIRXA_D0 | 9 | | | | | | I | FSIRX-A Primary Data Input |
| LINA_TX | 10 | | | | | | O | LIN-A Transmit |
| SPIA_CLK | 11 | | | | | | I/O | SPI-A Clock |
| GPIO13 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 13 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM7_B | 1 | | | | | | O | ePWM-7 Output B |
| MCANA_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| EQEP1_INDEX | 5 | | | | | | I/O | eQEP-1 Index |
| SCIB_RX | 6 | 62 | 50 | 35 | 29 | 26 | I | SCI-B Receive Data |
| PMBUSA_ALERT | 7 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| LINA_RX | 10 | | | | | | I | LIN-A Receive |
| SPIA_POCI | 11 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|-----------|----------|-----------|-------------|---|
| GPIO14 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 14 |
| EPWM8_A | 1 | | | | | | O | ePWM-8 Output A |
| SCIB_TX | 2 | | | | | | O | SCI-B Transmit Data |
| I2CB_SDA | 5 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| OUTPUTXBAR3 | 6 | | | | | | O | Output X-BAR Output 3 |
| PMBUSA_SDA | 7 | 125 | 96 | 79 | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SPIB_CLK | 9 | | | | | | I/O | SPI-B Clock |
| EQEP2_A | 10 | | | | | | I | eQEP-2 Input A |
| LINA_TX | 11 | | | | | | O | LIN-A Transmit |
| EPWM3_A | 13 | | | | | | O | ePWM-3 Output A |
| CLB_OUTPUTXBAR7 | 14 | | | | | | O | CLB Output X-BAR Output 7 |
| GPIO15 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 15 |
| EPWM8_B | 1 | | | | | | O | ePWM-8 Output B |
| SCIB_RX | 2 | | | | | | I | SCI-B Receive Data |
| I2CB_SCL | 5 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| OUTPUTXBAR4 | 6 | | | | | | O | Output X-BAR Output 4 |
| PMBUSA_SCL | 7 | 124 | 95 | 78 | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SPIB_PTE | 9 | | | | | | I/O | SPI-B Peripheral Transmit Enable (PTE) |
| EQEP2_B | 10 | | | | | | I | eQEP-2 Input B |
| LINA_RX | 11 | | | | | | I | LIN-A Receive |
| EPWM3_B | 13 | | | | | | O | ePWM-3 Output B |
| CLB_OUTPUTXBAR6 | 14 | | | | | | O | CLB Output X-BAR Output 6 |
| GPIO16 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 16 This pin also has analog functions which are described in the ANALOG section of this table. |
| SPIA_PICO | 1 | | | | | | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| EPWM9_A | 5 | | | | | | O | ePWM-9 Output A |
| SCIA_TX | 6 | | | | | | O | SCI-A Transmit Data |
| EQEP1_STROBE | 9 | 66 | 54 | 39 | 33 | 30 | I/O | eQEP-1 Strobe |
| PMBUSA_SCL | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| XCLKOUT | 11 | | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| EQEP2_B | 13 | | | | | | I | eQEP-2 Input B |
| SPIB_POCI | 14 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| EQEP3_STROBE | 15 | | | | | | I/O | eQEP-3 Strobe |
| GPIO17 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 17 This pin also has analog functions which are described in the ANALOG section of this table. |
| SPIA_POCI | 1 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| OUTPUTXBAR8 | 3 | | | | | | O | Output X-BAR Output 8 |
| EPWM9_B | 5 | | | | | | O | ePWM-9 Output B |
| SCIA_RX | 6 | | | | | | I | SCI-A Receive Data |
| EQEP1_INDEX | 9 | | | | | | I/O | eQEP-1 Index |
| PMBUSA_SDA | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| MCANA_TX | 11 | | | | | | O | CAN/CAN FD Transmit |
| EPWM6_A | 14 | | | | | | O | ePWM-6 Output A |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|-----------|----------|-----------|-------------|---|
| GPIO18 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 18 |
| SPIA_CLK | 1 | | | | | | I/O | SPI-A Clock |
| SCIB_TX | 2 | | | | | | O | SCI-B Transmit Data |
| MCANB_RX | 3 | | | | | | I | CAN/CAN FD Receive |
| EPWM6_A | 5 | | | | | | O | ePWM-6 Output A |
| I2CA_SCL | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| EQEP2_A | 9 | 87 | 68 | 50 | 41 | 38 | I | eQEP-2 Input A |
| PMBUSA_CTL | 10 | | | | | | I/O | PMBus-A Control Signal - Target Input/Controller Output |
| XCLKOUT | 11 | | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| LINA_TX | 13 | | | | | | O | LIN-A Transmit |
| EQEP3_INDEX | 15 | | | | | | I/O | eQEP-3 Index |
| X2 | ALT | | | | | | I/O | Crystal oscillator output. |
| GPIO19 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 19 |
| SPIA_PTE | 1 | | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| SCIB_RX | 2 | | | | | | I | SCI-B Receive Data |
| MCANB_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| EPWM6_B | 5 | | | | | | O | ePWM-6 Output B |
| I2CA_SDA | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| EQEP2_B | 9 | | | | | | I | eQEP-2 Input B |
| PMBUSA_ALERT | 10 | 88 | 69 | 51 | 42 | 39 | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| CLB_OUTPUTXBAR1 | 11 | | | | | | O | CLB Output X-BAR Output 1 |
| LINA_RX | 13 | | | | | | I | LIN-A Receive |
| X1 | ALT | | | | | | I/O | Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. |
| GPIO20 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 20 This pin also has analog functions which are described in the ANALOG section of this table. |
| EQEP1_A | 1 | | | | | | I | eQEP-1 Input A |
| EPWM12_A | 5 | | | | | | O | ePWM-12 Output A |
| SPIB_PICO | 6 | 60 | 48 | 33 | 27 | 24 | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| MCANA_TX | 9 | | | | | | O | CAN/CAN FD Transmit |
| ADCE_EXTMUXSEL0 | 10 | | | | | | O | ADCE external mux selection pin for position 0 |
| I2CA_SCL | 11 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SCIC_TX | 15 | | | | | | O | SCI-C Transmit Data |
| GPIO21 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 21 This pin also has analog functions which are described in the ANALOG section of this table. |
| EQEP1_B | 1 | | | | | | I | eQEP-1 Input B |
| EPWM12_B | 5 | | | | | | O | ePWM-12 Output B |
| SPIB_POCI | 6 | 61 | 49 | 34 | 28 | 25 | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| MCANA_RX | 9 | | | | | | I | CAN/CAN FD Receive |
| ADCE_EXTMUXSEL1 | 10 | | | | | | O | ADCE external mux selection pin for position 1 |
| I2CA_SDA | 11 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SCIC_RX | 15 | | | | | | I | SCI-C Receive Data |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|---------|--------|--------|-------|--------|----------|---|
| GPIO22 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 22 |
| EQEP1_STROBE | 1 | | | | | | I/O | eQEP-1 Strobe |
| SCIB_TX | 3 | | | | | | O | SCI-B Transmit Data |
| SPIB_CLK | 6 | 104 | 83 | 67 | 56 | 51 | I/O | SPI-B Clock |
| LINA_TX | 9, 11 | | | | | | O | LIN-A Transmit |
| CLB_OUTPUTXBAR1 | 10 | | | | | | O | CLB Output X-BAR Output 1 |
| EPWM4_A | 14 | | | | | | O | ePWM-4 Output A |
| EQEP3_A | 15 | | | | | | I | eQEP-3 Input A |
| GPIO23 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 23 |
| EQEP1_INDEX | 1 | | | | | | I/O | eQEP-1 Index |
| SCIB_RX | 3 | | | | | | I | SCI-B Receive Data |
| SPIB_PTE | 6 | | | | | | I/O | SPI-B Peripheral Transmit Enable (PTE) |
| LINA_RX | 9, 11 | 102 | 81 | 65 | 54 | 49 | I | LIN-A Receive |
| CLB_OUTPUTXBAR3 | 10 | | | | | | O | CLB Output X-BAR Output 3 |
| EPWM12_A | 13 | | | | | | O | ePWM-12 Output A |
| EPWM4_B | 14 | | | | | | O | ePWM-4 Output B |
| USB0DM | ALT | | | | | | O | USB-0 PHY differential data |
| GPIO24 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 24 This pin also has analog functions which are described in the ANALOG section of this table. |
| OUTPUTXBAR1 | 1 | | | | | | O | Output X-BAR Output 1 |
| EQEP2_A | 2 | | | | | | I | eQEP-2 Input A |
| SPIA_PTE | 3 | | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| EPWM8_A | 5 | | | | | | O | ePWM-8 Output A |
| SPIB_PICO | 6 | 68 | 56 | 41 | 35 | 32 | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| LINA_TX | 9 | | | | | | O | LIN-A Transmit |
| PMBUSA_SCL | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SCIA_TX | 11 | | | | | | O | SCI-A Transmit Data |
| ERRORSTS | 13 | | | | | | O | Error Status Output. This signal requires an external pull-down. |
| EPWM9_A | 14 | | | | | | O | ePWM-9 Output A |
| GPIO25 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 25 |
| OUTPUTXBAR2 | 1 | | | | | | O | Output X-BAR Output 2 |
| EQEP2_B | 2 | | | | | | I | eQEP-2 Input B |
| EQEP1_A | 5 | | | | | | I | eQEP-1 Input A |
| SPIB_POCI | 6 | 69 | 57 | 42 | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| FSITXA_D1 | 9 | | | | | | O | FSITX-A Optional Additional Data Output |
| PMBUSA_SDA | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| SCIA_RX | 11 | | | | | | I | SCI-A Receive Data |
| EQEP3_A | 13 | | | | | | I | eQEP-3 Input A |
| GPIO26 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 26 |
| OUTPUTXBAR3 | 1, 5 | | | | | | O | Output X-BAR Output 3 |
| EQEP2_INDEX | 2 | | | | | | I/O | eQEP-2 Index |
| SPIB_CLK | 6 | | | | | | I/O | SPI-B Clock |
| FSITXA_D0 | 9 | 70 | 58 | 43 | | | O | FSITX-A Primary Data Output |
| PMBUSA_CTL | 10 | | | | | | I/O | PMBus-A Control Signal - Target Input/Controller Output |
| I2CA_SDA | 11 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| EQEP3_B | 13 | | | | | | I | eQEP-3 Input B |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|--------------|--------------|---------|--------|--------|-------|--------|----------|---|
| GPIO27 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 27 |
| OUTPUTXBAR4 | 1, 5 | | | | | | O | Output X-BAR Output 4 |
| EQEP2_STROBE | 2 | | | | | | I/O | eQEP-2 Strobe |
| SPIB_PTE | 6 | 71 | 59 | 44 | | | I/O | SPI-B Peripheral Transmit Enable (PTE) |
| FSITXA_CLK | 9 | | | | | | O | FSITX-A Output Clock |
| PMBUSA_ALERT | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| I2CA_SCL | 11 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| EQEP3_STROBE | 13 | | | | | | I/O | eQEP-3 Strobe |
| GPIO28 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 28 This pin also has analog functions which are described in the ANALOG section of this table. |
| SCIA_RX | 1 | | | | | | I | SCI-A Receive Data |
| EPWM7_A | 3 | | | | | | O | ePWM-7 Output A |
| OUTPUTXBAR5 | 5 | | | | | | O | Output X-BAR Output 5 |
| EQEP1_A | 6 | 2 | 1 | 4 | 2 | 3 | I | eQEP-1 Input A |
| EQEP2_STROBE | 9 | | | | | | I/O | eQEP-2 Strobe |
| LINA_TX | 10 | | | | | | O | LIN-A Transmit |
| SPIB_CLK | 11 | | | | | | I/O | SPI-B Clock |
| ERRORSTS | 13 | | | | | | O | Error Status Output. This signal requires an external pulldown. |
| I2CB_SDA | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| GPIO29 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 29 |
| SCIA_TX | 1 | | | | | | O | SCI-A Transmit Data |
| EPWM7_B | 3 | | | | | | O | ePWM-7 Output B |
| OUTPUTXBAR6 | 5 | | | | | | O | Output X-BAR Output 6 |
| EQEP1_B | 6 | | | | | | I | eQEP-1 Input B |
| EQEP2_INDEX | 9 | 1 | 100 | 3 | 1 | 2 | I/O | eQEP-2 Index |
| LINA_RX | 10 | | | | | | I | LIN-A Receive |
| SPIB_PTE | 11 | | | | | | I/O | SPI-B Peripheral Transmit Enable (PTE) |
| ERRORSTS | 13 | | | | | | O | Error Status Output. This signal requires an external pulldown. |
| I2CB_SCL | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| AUXCLKIN | ALT | | | | | | I | Auxiliary Clock Input |
| GPIO30 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 30 |
| SPIB_PICO | 3 | | | | | | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| OUTPUTXBAR7 | 5 | | | | | | O | Output X-BAR Output 7 |
| EQEP1_STROBE | 6 | 127 | 98 | 1 | | | I/O | eQEP-1 Strobe |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| MCANA_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| EPWM1_A | 11 | | | | | | O | ePWM-1 Output A |
| EQEP3_INDEX | 13 | | | | | | I/O | eQEP-3 Index |
| GPIO31 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 31 |
| SPIB_POCI | 3 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| OUTPUTXBAR8 | 5 | | | | | | O | Output X-BAR Output 8 |
| EQEP1_INDEX | 6 | 128 | 99 | 2 | | | I/O | eQEP-1 Index |
| FSIRXA_D1 | 9 | | | | | | I | FSIRX-A Optional Additional Data Input |
| MCANA_TX | 10 | | | | | | O | CAN/CAN FD Transmit |
| EPWM1_B | 11 | | | | | | O | ePWM-1 Output B |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-------------|--------------|------------|-----------|-----------|----------|-----------|-------------|--|
| GPIO32 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 32 |
| I2CA_SDA | 1 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| EQEP1_INDEX | 2 | | | | | | I/O | eQEP-1 Index |
| SPIB_CLK | 3 | | | | | | I/O | SPI-B Clock |
| EPWM8_B | 5 | 79 | 64 | 49 | 40 | 37 | O | ePWM-8 Output B |
| LINA_TX | 6 | | | | | | O | LIN-A Transmit |
| FSIRXA_D0 | 9 | | | | | | I | FSIRX-A Primary Data Input |
| MCANB_TX | 10 | | | | | | O | CAN/CAN FD Transmit |
| PMBUSA_SDA | 11 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| ADCSOCBO | 13 | | | | | | O | ADC Start of Conversion B for External ADC |
| GPIO33 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 33 This pin also has analog functions which are described in the ANALOG section of this table. |
| I2CA_SCL | 1 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SPIB_PTE | 3 | | | | | | I/O | SPI-B Peripheral Transmit Enable (PTE) |
| OUTPUTXBAR4 | 5 | | | | | | O | Output X-BAR Output 4 |
| LINA_RX | 6 | 65 | 53 | 38 | 32 | 29 | I | LIN-A Receive |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| MCANB_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| EQEP2_B | 11 | | | | | | I | eQEP-2 Input B |
| ADCSOCAO | 13 | | | | | | O | ADC Start of Conversion A for External ADC |
| SCIC_RX | 15 | | | | | | I | SCI-C Receive Data |
| GPIO34 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 34 |
| OUTPUTXBAR1 | 1 | 123 | 94 | 77 | | | O | Output X-BAR Output 1 |
| PMBUSA_SDA | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| I2CB_SDA | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| GPIO35 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 35 |
| SCIA_RX | 1 | | | | | | I | SCI-A Receive Data |
| SPIA_POCI | 2 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| I2CA_SDA | 3 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| MCANB_RX | 5 | | | | | | I | CAN/CAN FD Receive |
| PMBUSA_SCL | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| LINA_RX | 7 | | | | | | I | LIN-A Receive |
| EQEP1_A | 9 | 78 | 63 | 48 | 39 | 36 | I | eQEP-1 Input A |
| PMBUSA_CTL | 10 | | | | | | I/O | PMBus-A Control Signal - Target Input/Controller Output |
| EPWM5_B | 11 | | | | | | O | ePWM-5 Output B |
| TDI | 15 | | | | | | I | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|-----------|----------|-----------|-------------|---|
| GPIO37 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 37 |
| OUTPUTXBAR2 | 1 | | | | | | O | Output X-BAR Output 2 |
| SPIA_PTE | 2 | | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| I2CA_SCL | 3 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SCIA_TX | 5 | | | | | | O | SCI-A Transmit Data |
| MCANB_TX | 6 | | | | | | O | CAN/CAN FD Transmit |
| LINA_TX | 7 | | | | | | O | LIN-A Transmit |
| EQEP1_B | 9 | 76 | 61 | 46 | 37 | 34 | I | eQEP-1 Input B |
| PMBUSA_ALERT | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| EPWM5_A | 11 | | | | | | O | ePWM-5 Output A |
| TDO | 15 | | | | | | O | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. |
| GPIO40 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 40 |
| SPIB_PICO | 1 | | | | | | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| EPWM2_B | 5 | | | | | | O | ePWM-2 Output B |
| PMBUSA_SDA | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| FSIRXA_D0 | 7 | 101 | 80 | 64 | 53 | 48 | I | FSIRX-A Primary Data Input |
| SCIB_TX | 9 | | | | | | O | SCI-B Transmit Data |
| EQEP1_A | 10 | | | | | | I | eQEP-1 Input A |
| LINA_TX | 11 | | | | | | O | LIN-A Transmit |
| CLB_OUTPUTXBAR4 | 14 | | | | | | O | CLB Output X-BAR Output 4 |
| EQEP3_STROBE | 15 | | | | | | I/O | eQEP-3 Strobe |
| GPIO41 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 41 |
| EPWM7_A | 1 | | | | | | O | ePWM-7 Output A |
| EPWM2_A | 5 | | | | | | O | ePWM-2 Output A |
| PMBUSA_SCL | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| FSIRXA_D1 | 7 | | | | | | I | FSIRX-A Optional Additional Data Input |
| SCIB_RX | 9 | 103 | 82 | 66 | 55 | 50 | I | SCI-B Receive Data |
| EQEP1_B | 10 | | | | | | I | eQEP-1 Input B |
| LINA_RX | 11 | | | | | | I | LIN-A Receive |
| EPWM12_B | 13 | | | | | | O | ePWM-12 Output B |
| SPIB_POCI | 14 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| USB0DP | ALT | | | | | | O | USB-0 PHY differential data |
| GPIO42 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 42 |
| LINA_RX | 2 | | | | | | I | LIN-A Receive |
| OUTPUTXBAR5 | 3 | | | | | | O | Output X-BAR Output 5 |
| PMBUSA_CTL | 5 | 94 | | 57 | | | I/O | PMBus-A Control Signal - Target Input/Controller Output |
| I2CA_SDA | 6 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| SCIC_RX | 7 | | | | | | I | SCI-C Receive Data |
| EQEP1_STROBE | 10 | | | | | | I/O | eQEP-1 Strobe |
| CLB_OUTPUTXBAR3 | 11 | | | | | | O | CLB Output X-BAR Output 3 |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|---------|--------|--------|-------|--------|----------|---|
| GPIO43 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 43 |
| OUTPUTXBAR6 | 3 | | | | | | O | Output X-BAR Output 6 |
| PMBUSA_ALERT | 5, 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| I2CA_SCL | 6 | 91 | | 54 | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SCIC_TX | 7 | | | | | | O | SCI-C Transmit Data |
| EQEP1_INDEX | 10 | | | | | | I/O | eQEP-1 Index |
| CLB_OUTPUTXBAR4 | 11 | | | | | | O | CLB Output X-BAR Output 4 |
| GPIO44 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 44 |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| EQEP1_A | 5 | | | | | | I | eQEP-1 Input A |
| PMBUSA_SDA | 6 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| FSITXA_CLK | 7 | 106 | 85 | 69 | | | O | FSITX-A Output Clock |
| PMBUSA_CTL | 9 | | | | | | I/O | PMBus-A Control Signal - Target Input/Controller Output |
| CLB_OUTPUTXBAR3 | 10 | | | | | | O | CLB Output X-BAR Output 3 |
| FSIRXA_D0 | 11 | | | | | | I | FSIRX-A Primary Data Input |
| LINA_TX | 14 | | | | | | O | LIN-A Transmit |
| GPIO45 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 45 |
| OUTPUTXBAR8 | 3 | | | | | | O | Output X-BAR Output 8 |
| FSITXA_D0 | 7 | 110 | | 73 | | | O | FSITX-A Primary Data Output |
| PMBUSA_ALERT | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| CLB_OUTPUTXBAR4 | 10 | | | | | | O | CLB Output X-BAR Output 4 |
| GPIO46 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 46 |
| LINA_TX | 3 | | | | | | O | LIN-A Transmit |
| MCANA_TX | 5 | 4 | | 6 | | | O | CAN/CAN FD Transmit |
| FSITXA_D1 | 7 | | | | | | O | FSITX-A Optional Additional Data Output |
| PMBUSA_SDA | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| GPIO47 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 47 |
| LINA_RX | 3 | | | | | | I | LIN-A Receive |
| MCANA_RX | 5 | 8 | 6 | | | | I | CAN/CAN FD Receive |
| CLB_OUTPUTXBAR2 | 7 | | | | | | O | CLB Output X-BAR Output 2 |
| PMBUSA_SCL | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| GPIO48 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 48 |
| OUTPUTXBAR3 | 1 | | | | | | O | Output X-BAR Output 3 |
| MCANA_TX | 5 | 11 | 7 | | | | O | CAN/CAN FD Transmit |
| SCIA_TX | 6 | | | | | | O | SCI-A Transmit Data |
| PMBUSA_SDA | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| GPIO49 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 49 |
| OUTPUTXBAR4 | 1 | | | | | | O | Output X-BAR Output 4 |
| MCANA_RX | 5 | | | | | | I | CAN/CAN FD Receive |
| SCIA_RX | 6 | 12 | 8 | | | | I | SCI-A Receive Data |
| LINA_RX | 9 | | | | | | I | LIN-A Receive |
| FSITXA_D0 | 14 | | | | | | O | FSITX-A Primary Data Output |
| GPIO50 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 50 |
| EQEP1_A | 1 | | | | | | I | eQEP-1 Input A |
| MCANA_TX | 5 | | | | | | O | CAN/CAN FD Transmit |
| SPIB_PICO | 6 | 13 | 9 | | | | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| I2CB_SDA | 9 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| FSITXA_D1 | 14 | | | | | | O | FSITX-A Optional Additional Data Output |

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Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|--------|----------|--------|-------------|---|
| GPIO51 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 51 |
| EQEP1_B | 1 | | | | | | I | eQEP-1 Input B |
| MCANA_RX | 5 | 14 | 10 | | | | I | CAN/CAN FD Receive |
| SPIB_POCI | 6 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| I2CB_SCL | 9 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| FSITXA_CLK | 14 | | | | | | O | FSITX-A Output Clock |
| GPIO52 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 52 |
| EQEP1_STROBE | 1 | | | | | | I/O | eQEP-1 Strobe |
| CLB_OUTPUTXBAR5 | 5 | 15 | 11 | | | | O | CLB Output X-BAR Output 5 |
| SPIB_CLK | 6 | | | | | | I/O | SPI-B Clock |
| SYNCOUT | 9 | | | | | | O | External ePWM Synchronization Pulse |
| FSIRXA_D0 | 14 | | | | | | I | FSIRX-A Primary Data Input |
| GPIO53 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 53 |
| EQEP1_INDEX | 1 | | | | | | I/O | eQEP-1 Index |
| CLB_OUTPUTXBAR6 | 5 | | | | | | O | CLB Output X-BAR Output 6 |
| SPIB_PTE | 6 | 16 | 12 | | | | I/O | SPI-B Peripheral Transmit Enable (PTE) |
| ADCSOCAO | 9 | | | | | | O | ADC Start of Conversion A for External ADC |
| MCANB_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| FSIRXA_D1 | 14 | | | | | | I | FSIRX-A Optional Additional Data Input |
| GPIO54 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 54 |
| SPIA_PICO | 1 | | | | | | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| EQEP2_A | 5 | | | | | | I | eQEP-2 Input A |
| OUTPUTXBAR2 | 6 | 17 | 13 | | | | O | Output X-BAR Output 2 |
| ADCSOCBO | 9 | | | | | | O | ADC Start of Conversion B for External ADC |
| LINA_TX | 10 | | | | | | O | LIN-A Transmit |
| FSIRXA_CLK | 14 | | | | | | I | FSIRX-A Input Clock |
| GPIO55 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 55 |
| SPIA_POCI | 1 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| EQEP2_B | 5 | | | | | | I | eQEP-2 Input B |
| OUTPUTXBAR3 | 6 | 51 | 43 | | | | O | Output X-BAR Output 3 |
| ERRORSTS | 9 | | | | | | O | Error Status Output. This signal requires an external pulldown. |
| LINA_RX | 10 | | | | | | I | LIN-A Receive |
| GPIO56 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 56 |
| SPIA_CLK | 1 | | | | | | I/O | SPI-A Clock |
| CLB_OUTPUTXBAR7 | 2 | | | | | | O | CLB Output X-BAR Output 7 |
| MCANA_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| EQEP2_STROBE | 5 | 80 | 65 | | | | I/O | eQEP-2 Strobe |
| SCIB_TX | 6 | | | | | | O | SCI-B Transmit Data |
| SPIB_PICO | 9 | | | | | | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| I2CA_SDA | 10 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| EQEP1_A | 11 | | | | | | I | eQEP-1 Input A |
| FSIRXA_D1 | 14 | | | | | | I | FSIRX-A Optional Additional Data Input |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|---------|--------|--------|-------|--------|----------|--|
| GPIO57 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 57 |
| SPIA_PTE | 1 | | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| CLB_OUTPUTXBAR8 | 2 | | | | | | O | CLB Output X-BAR Output 8 |
| MCANA_RX | 3 | | | | | | I | CAN/CAN FD Receive |
| EQEP2_INDEX | 5 | 81 | 66 | | | | I/O | eQEP-2 Index |
| SCIB_RX | 6 | | | | | | I | SCI-B Receive Data |
| SPIB_POCI | 9 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| I2CA_SCL | 10 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| EQEP1_B | 11 | | | | | | I | eQEP-1 Input B |
| FSIRXA_CLK | 14 | | | | | | I | FSIRX-A Input Clock |
| GPIO58 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 58 |
| OUTPUTXBAR1 | 5 | | | | | | O | Output X-BAR Output 1 |
| SPIB_CLK | 6 | | | | | | I/O | SPI-B Clock |
| LINA_TX | 9 | 82 | 67 | | | | O | LIN-A Transmit |
| MCANB_TX | 10 | | | | | | O | CAN/CAN FD Transmit |
| EQEP1_STROBE | 11 | | | | | | I/O | eQEP-1 Strobe |
| FSIRXA_D0 | 14 | | | | | | I | FSIRX-A Primary Data Input |
| GPIO59 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 59 |
| OUTPUTXBAR2 | 5 | | | | | | O | Output X-BAR Output 2 |
| SPIB_PTE | 6 | 121 | 92 | | | | I/O | SPI-B Peripheral Transmit Enable (PTE) |
| LINA_RX | 9 | | | | | | I | LIN-A Receive |
| MCANB_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| EQEP1_INDEX | 11 | | | | | | I/O | eQEP-1 Index |
| GPIO60 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 60 |
| EPWM12_B | 1 | | | | | | O | ePWM-12 Output B |
| MCANA_TX | 3 | 52 | 44 | | | | O | CAN/CAN FD Transmit |
| OUTPUTXBAR3 | 5 | | | | | | O | Output X-BAR Output 3 |
| SPIB_PICO | 6 | | | | | | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| GPIO61 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 61 |
| MCANA_RX | 3 | | | | | | I | CAN/CAN FD Receive |
| OUTPUTXBAR4 | 5 | 120 | 91 | | | | O | Output X-BAR Output 4 |
| SPIB_POCI | 6 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| MCANB_RX | 14 | | | | | | I | CAN/CAN FD Receive |
| GPIO62 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 62 |
| EPWM10_A | 1 | | | | | | O | ePWM-10 Output A |
| OUTPUTXBAR3 | 2 | | | | | | O | Output X-BAR Output 3 |
| MCANA_TX | 5 | 58 | 46 | 31 | | | O | CAN/CAN FD Transmit |
| SCIA_TX | 6 | | | | | | O | SCI-A Transmit Data |
| PMBUSA_SDA | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| GPIO63 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 63 |
| EPWM10_B | 1 | | | | | | O | ePWM-10 Output B |
| OUTPUTXBAR4 | 2 | | | | | | O | Output X-BAR Output 4 |
| MCANA_RX | 5 | 59 | 47 | 32 | | | I | CAN/CAN FD Receive |
| SCIA_RX | 6 | | | | | | I | SCI-A Receive Data |
| LINA_RX | 9 | | | | | | I | LIN-A Receive |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|--------------|--------------|---------|--------|--------|-------|--------|----------|---|
| GPIO64 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 64 |
| SCIA_RX | 1 | | | | | | I | SCI-A Receive Data |
| EPWM11_A | 2 | | | | | | O | ePWM-11 Output A |
| EPWM7_A | 3 | | | | | | O | ePWM-7 Output A |
| OUTPUTXBAR5 | 5 | | | | | | O | Output X-BAR Output 5 |
| EQEP1_A | 6 | 56 | | | | | I | eQEP-1 Input A |
| EQEP2_STROBE | 9 | | | | | | I/O | eQEP-2 Strobe |
| LINA_TX | 10 | | | | | | O | LIN-A Transmit |
| SPIB_CLK | 11 | | | | | | I/O | SPI-B Clock |
| ERRORSTS | 13 | | | | | | O | Error Status Output. This signal requires an external pulldown. |
| I2CB_SDA | 14 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| GPIO65 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 65 |
| EQEP1_A | 1 | | | | | | I | eQEP-1 Input A |
| EPWM11_B | 2 | 57 | | | | | O | ePWM-11 Output B |
| SPIB_PICO | 6 | | | | | | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| MCANA_TX | 9 | | | | | | O | CAN/CAN FD Transmit |
| I2CA_SCL | 11 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| GPIO66 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 66 |
| EQEP1_B | 1 | | | | | | I | eQEP-1 Input B |
| EPWM12_A | 2 | 9 | | | | | O | ePWM-12 Output A |
| SPIB_POCI | 6 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| MCANA_RX | 9 | | | | | | I | CAN/CAN FD Receive |
| I2CA_SDA | 11 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| GPIO67 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 67 |
| EPWM7_B | 1 | | | | | | O | ePWM-7 Output B |
| EPWM12_B | 2 | | | | | | O | ePWM-12 Output B |
| MCANA_TX | 3 | | | | | | O | CAN/CAN FD Transmit |
| EQEP1_INDEX | 5 | | | | | | I/O | eQEP-1 Index |
| SCIB_RX | 6 | 10 | | | | | I | SCI-B Receive Data |
| PMBUSA_ALERT | 7 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| LINA_RX | 10 | | | | | | I | LIN-A Receive |
| SPIA_POCI | 11 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| SCIC_RX | 15 | | | | | | I | SCI-C Receive Data |
| GPIO68 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 68 |
| EPWM7_A | 1 | | | | | | O | ePWM-7 Output A |
| EPWM3_A | 2 | | | | | | O | ePWM-3 Output A |
| MCANA_RX | 3 | | | | | | I | CAN/CAN FD Receive |
| EQEP1_STROBE | 5 | | | | | | I/O | eQEP-1 Strobe |
| SCIB_TX | 6 | 72 | | | | | O | SCI-B Transmit Data |
| PMBUSA_CTL | 7 | | | | | | I/O | PMBus-A Control Signal - Target Input/Controller Output |
| FSIRXA_D0 | 9 | | | | | | I | FSIRX-A Primary Data Input |
| LINA_TX | 10 | | | | | | O | LIN-A Transmit |
| SPIA_CLK | 11 | | | | | | I/O | SPI-A Clock |
| SCIC_TX | 15 | | | | | | O | SCI-C Transmit Data |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|--------------|--------------|---------|--------|--------|-------|--------|----------|---|
| GPIO69 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 69 |
| EPWM6_B | 1 | | | | | | O | ePWM-6 Output B |
| EPWM3_B | 2 | | | | | | O | ePWM-3 Output B |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| EQEP1_B | 5 | | | | | | I | eQEP-1 Input B |
| SCIB_RX | 6 | 73 | | | | | I | SCI-B Receive Data |
| SPIA_PTE | 7 | | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| FSIRXA_D1 | 9 | | | | | | I | FSIRX-A Optional Additional Data Input |
| LINA_RX | 10 | | | | | | I | LIN-A Receive |
| EQEP2_A | 11 | | | | | | I | eQEP-2 Input A |
| SPIA_PICO | 13 | | | | | | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| EQEP3_INDEX | 15 | | | | | | I/O | eQEP-3 Index |
| GPIO70 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 70 |
| I2CA_SCL | 1 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Clock |
| SPIB_PTE | 3 | | | | | | I/O | SPI-B Peripheral Transmit Enable (PTE) |
| OUTPUTXBAR4 | 5 | | | | | | O | Output X-BAR Output 4 |
| LINA_RX | 6 | 74 | | | | | I | LIN-A Receive |
| FSIRXA_CLK | 9 | | | | | | I | FSIRX-A Input Clock |
| MCANA_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| EQEP2_B | 11 | | | | | | I | eQEP-2 Input B |
| ADCSOAO | 13 | | | | | | O | ADC Start of Conversion A for External ADC |
| EQEP3_A | 15 | | | | | | I | eQEP-3 Input A |
| GPIO71 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 71 |
| SPIA_PICO | 1 | | | | | | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| EPWM4_B | 2 | | | | | | O | ePWM-4 Output B |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| EPWM9_A | 5 | | | | | | O | ePWM-9 Output A |
| SCIA_TX | 6 | | | | | | O | SCI-A Transmit Data |
| EQEP1_STROBE | 9 | 83 | | | | | I/O | eQEP-1 Strobe |
| PMBUSA_SCL | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| XCLKOUT | 11 | | | | | | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. |
| EQEP2_INDEX | 13 | | | | | | I/O | eQEP-2 Index |
| SPIB_POCI | 14 | | | | | | I/O | SPI-B Peripheral Out, Controller In (POCI) |
| EQEP3_STROBE | 15 | | | | | | I/O | eQEP-3 Strobe |
| GPIO72 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 72 |
| SPIA_POCI | 1 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| EPWM5_A | 2 | | | | | | O | ePWM-5 Output A |
| OUTPUTXBAR8 | 3 | | | | | | O | Output X-BAR Output 8 |
| EPWM9_B | 5 | | | | | | O | ePWM-9 Output B |
| SCIA_RX | 6 | 84 | | | | | I | SCI-A Receive Data |
| EQEP1_INDEX | 9 | | | | | | I/O | eQEP-1 Index |
| PMBUSA_SDA | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Data |
| MCANA_TX | 11 | | | | | | O | CAN/CAN FD Transmit |
| EPWM6_A | 14 | | | | | | O | ePWM-6 Output A |
| EQEP3_B | 15 | | | | | | I | eQEP-3 Input B |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|--------------|--------------|------------|-----------|-----------|----------|-----------|-------------|---|
| GPIO73 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 73 |
| OUTPUTXBAR1 | 1 | | | | | | O | Output X-BAR Output 1 |
| EPWM5_B | 2 | | | | | | O | ePWM-5 Output B |
| SPIA_PTE | 3 | | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| EPWM8_A | 5 | | | | | | O | ePWM-8 Output A |
| SPIB_PICO | 6 | 85 | | | | | I/O | SPI-B Peripheral In, Controller Out (PICO) |
| LINA_TX | 9 | | | | | | O | LIN-A Transmit |
| PMBUSA_SCL | 10 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| SCIA_TX | 11 | | | | | | O | SCI-A Transmit Data |
| ERRORSTS | 13 | | | | | | O | Error Status Output. This signal requires an external pulldown. |
| EPWM9_A | 14 | | | | | | O | ePWM-9 Output A |
| GPIO74 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 74 |
| EPWM2_B | 1 | | | | | | O | ePWM-2 Output B |
| ADCSOAO | 3 | 86 | | | | | O | ADC Start of Conversion A for External ADC |
| MCANA_TX | 5 | | | | | | O | CAN/CAN FD Transmit |
| SPIA_POCI | 6 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| EQEP1_B | 11 | | | | | | I | eQEP-1 Input B |
| GPIO75 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 75 |
| EPWM1_B | 1 | | | | | | O | ePWM-1 Output B |
| LINA_RX | 3 | | | | | | I | LIN-A Receive |
| EPWM6_A | 5 | 111 | | | | | O | ePWM-6 Output A |
| SPIA_CLK | 6 | | | | | | I/O | SPI-A Clock |
| EQEP1_STROBE | 11 | | | | | | I/O | eQEP-1 Strobe |
| SCIC_RX | 14 | | | | | | I | SCI-C Receive Data |
| GPIO76 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 76 |
| EPWM4_A | 1 | | | | | | O | ePWM-4 Output A |
| OUTPUTXBAR2 | 5 | 112 | | | | | O | Output X-BAR Output 2 |
| SPIA_PTE | 6 | | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| MCANA_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| EQEP1_INDEX | 11 | | | | | | I/O | eQEP-1 Index |
| GPIO77 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 77 |
| EPWM1_A | 1 | | | | | | O | ePWM-1 Output A |
| OUTPUTXBAR3 | 5 | | | | | | O | Output X-BAR Output 3 |
| SPIA_PICO | 6 | 113 | | | | | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| MCANA_TX | 10 | | | | | | O | CAN/CAN FD Transmit |
| EQEP1_A | 11 | | | | | | I | eQEP-1 Input A |
| SCIC_TX | 14 | | | | | | O | SCI-C Transmit Data |
| GPIO78 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 78 |
| EPWM8_A | 2 | | | | | | O | ePWM-8 Output A |
| EPWM3_A | 3 | 114 | | | | | O | ePWM-3 Output A |
| OUTPUTXBAR1 | 5 | | | | | | O | Output X-BAR Output 1 |
| EPWM2_B | 6 | | | | | | O | ePWM-2 Output B |
| FSITXA_CLK | 9 | | | | | | O | FSITX-A Output Clock |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|--------|----------|--------|-------------|---|
| GPIO79 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 79 |
| EPWM8_B | 2 | | | | | | O | ePWM-8 Output B |
| EPWM3_B | 3 | | | | | | O | ePWM-3 Output B |
| MCANA_RX | 5 | 115 | | | | | I | CAN/CAN FD Receive |
| EPWM2_A | 6 | | | | | | O | ePWM-2 Output A |
| I2CA_SDA | 7 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| PMBUSA_SCL | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |
| GPIO80 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 80 |
| EPWM1_A | 1 | | | | | | O | ePWM-1 Output A |
| OUTPUTXBAR7 | 3 | | | | | | O | Output X-BAR Output 7 |
| SCIA_RX | 5 | | | | | | I | SCI-A Receive Data |
| I2CB_SDA | 6 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| SPIA_PTE | 7 | 116 | | | | | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| FSITXA_D0 | 9 | | | | | | O | FSITX-A Primary Data Output |
| MCANA_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| CLB_OUTPUTXBAR8 | 11 | | | | | | O | CLB Output X-BAR Output 8 |
| EQEP1_INDEX | 13 | | | | | | I/O | eQEP-1 Index |
| EPWM3_A | 15 | | | | | | O | ePWM-3 Output A |
| GPIO81 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 81 |
| EPWM1_B | 1 | | | | | | O | ePWM-1 Output B |
| OUTPUTXBAR6 | 2 | | | | | | O | Output X-BAR Output 6 |
| SCIC_RX | 3 | | | | | | I | SCI-C Receive Data |
| SPIB_CLK | 5 | 117 | | | | | I/O | SPI-B Clock |
| I2CB_SCL | 6 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Clock |
| FSITXA_D1 | 9 | | | | | | O | FSITX-A Optional Additional Data Output |
| MCANA_TX | 10 | | | | | | O | CAN/CAN FD Transmit |
| EQEP3_INDEX | 11 | | | | | | I/O | eQEP-3 Index |
| GPIO211 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 211 |
| EPWM10_A | 1 | 43 | | | | | O | ePWM-10 Output A |
| EQEP3_A | 5 | | | | | | I | eQEP-3 Input A |
| GPIO212 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 212 |
| EPWM10_B | 1 | 44 | | | | | O | ePWM-10 Output B |
| EQEP3_B | 5 | | | | | | I | eQEP-3 Input B |
| GPIO213 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 213 |
| EPWM11_A | 1 | 45 | | | | | O | ePWM-11 Output A |
| EQEP3_STROBE | 5 | | | | | | I/O | eQEP-3 Strobe |
| GPIO214 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 214 |
| EPWM11_B | 1 | 46 | | | | | O | ePWM-11 Output B |
| EQEP3_INDEX | 5 | | | | | | I/O | eQEP-3 Index |
| GPIO215 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 215 |
| EPWM7_B | 1 | 47 | | | | | O | ePWM-7 Output B |
| EQEP2_A | 5 | | | | | | I | eQEP-2 Input A |

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|-----------------|--------------|------------|-----------|-----------|----------|-----------|-------------|--|
| GPIO224 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 224 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM11_B | 1 | | | | | | O | ePWM-11 Output B |
| OUTPUTXBAR3 | 5 | | | | | | O | Output X-BAR Output 3 |
| SPIA_PICO | 6 | 21 | 17 | 13 | 9 | 7 | I/O | SPI-A Peripheral In, Controller Out (PICO) |
| EPWM1_A | 9 | | | | | | O | ePWM-1 Output A |
| MCANA_TX | 10 | | | | | | O | CAN/CAN FD Transmit |
| EQEP1_A | 11 | | | | | | I | eQEP-1 Input A |
| ADCE_EXTMUXSEL3 | 13 | | | | | | O | ADCE external mux selection pin for position 3 |
| SCIC_TX | 14 | | | | | | O | SCI-C Transmit Data |
| GPIO226 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 226 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM10_B | 1 | | | | | | O | ePWM-10 Output B |
| LINA_RX | 3 | | | | | | I | LIN-A Receive |
| EPWM6_A | 5 | 19 | 15 | 11 | 7 | | O | ePWM-6 Output A |
| SPIA_CLK | 6 | | | | | | I/O | SPI-A Clock |
| EPWM1_B | 9 | | | | | | O | ePWM-1 Output B |
| EQEP1_STROBE | 11 | | | | | | I/O | eQEP-1 Strobe |
| ADCE_EXTMUXSEL1 | 13 | | | | | | O | ADCE external mux selection pin for position 1 |
| SCIC_RX | 14 | | | | | | I | SCI-C Receive Data |
| GPIO227 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 227 This pin also has analog functions which are described in the ANALOG section of this table. |
| I2CB_SCL | 1 | 48 | 38 | 28 | 24 | 22 | I/OD | I2C-B Open-Drain Bidirectional Clock |
| EPWM3_A | 3 | | | | | | O | ePWM-3 Output A |
| OUTPUTXBAR1 | 5 | | | | | | O | Output X-BAR Output 1 |
| EPWM2_B | 6 | | | | | | O | ePWM-2 Output B |
| GPIO228 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 228 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM10_A | 1 | | | | | | O | ePWM-10 Output A |
| ADCSOAO | 3 | | | | | | O | ADC Start of Conversion A for External ADC |
| MCANA_TX | 5 | 18 | 14 | 10 | 6 | | O | CAN/CAN FD Transmit |
| SPIA_POCI | 6 | | | | | | I/O | SPI-A Peripheral Out, Controller In (POCI) |
| EPWM2_B | 9 | | | | | | O | ePWM-2 Output B |
| EQEP1_B | 11 | | | | | | I | eQEP-1 Input B |
| ADCE_EXTMUXSEL0 | 13 | | | | | | O | ADCE external mux selection pin for position 0 |
| GPIO230 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 230 This pin also has analog functions which are described in the ANALOG section of this table. |
| I2CB_SDA | 1 | | | | | | I/OD | I2C-B Open-Drain Bidirectional Data |
| EPWM3_B | 3 | 50 | 40 | 29 | 25 | 23 | O | ePWM-3 Output B |
| MCANA_RX | 5 | | | | | | I | CAN/CAN FD Receive |
| EPWM2_A | 6 | | | | | | O | ePWM-2 Output A |
| I2CA_SDA | 7 | | | | | | I/OD | I2C-A Open-Drain Bidirectional Data |
| PMBUSA_SCL | 9 | | | | | | I/OD | PMBus-A Open-Drain Bidirectional Clock |

ADVANCE INFORMATION

Table 5-1. Pin Attributes (continued)

| SIGNAL NAME | MUX POSITION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH | PIN TYPE | DESCRIPTION |
|------------------------------|--------------|----------------|---------------|---------------|---------------|-----------|----------|---|
| GPIO242 | 0, 4, 8, 12 | | | | | | I/O | General-Purpose Input Output 242 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM11_A | 1 | | | | | | O | ePWM-11 Output A |
| OUTPUTXBAR2 | 5 | | | | | | O | Output X-BAR Output 2 |
| SPIA_PTE | 6 | 20 | 16 | 12 | 8 | 6 | I/O | SPI-A Peripheral Transmit Enable (PTE) |
| EPWM4_A | 9 | | | | | | O | ePWM-4 Output A |
| MCANA_RX | 10 | | | | | | I | CAN/CAN FD Receive |
| EQEP1_INDEX | 11 | | | | | | I/O | eQEP-1 Index |
| ADCE_EXTMUXSEL2 | 13 | | | | | | O | ADCE external mux selection pin for position 2 |
| GPIO247 | 0, 4, 8, 12 | | 42 | | | | I/O | General-Purpose Input Output 247 This pin also has analog functions which are described in the ANALOG section of this table. |
| EPWM12_B | 1 | | | | | | O | ePWM-12 Output B |
| GPIO253 | 0, 4, 8, 12 | | 41 | | | | I/O | General-Purpose Input Output 253 |
| EPWM12_A | 1 | | | | | | O | ePWM-12 Output A |
| TEST, JTAG, AND RESET | | | | | | | | |
| TCK | | 75 | 60 | 45 | 36 | 33 | I | JTAG test clock with internal pullup. |
| TMS | | 77 | 62 | 47 | 38 | 35 | I/O | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 kΩ) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation. |
| XRSn | | 3 | 2 | 5 | 3 | 4 | I/OD | Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 kΩ and 10 kΩ should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device. |
| POWER AND GROUND | | | | | | | | |
| VDD | | 6, 54, 90, 108 | 4, 71, 87 | 8, 53, 71 | 4, 44, 59 | 5, 41, 53 | | 1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 10 μF. It is also recommended that all VDD pins be externally connected to each other when internal VREG is used. |
| VDDA | | 41 | 34 | 26 | 22 | 20 | | 3.3-V Analog Power Pins. Place a minimum 2.2-μF decoupling capacitor on each pin. |
| VDDIO | | 5, 55, 89, 109 | 3, 70, 88 | 7, 52, 72 | 43, 60 | 40, 54 | | 3.3-V Digital I/O Power Pins. Place a minimum 0.1-μF decoupling capacitor on each pin. |
| VREGENZ | | 93 | 73 | 56 | 46 | 42 | I | Internal voltage regulator enable with internal pulldown. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply. |
| VSS | | 7, 53, 92, 107 | 5, 45, 72, 86 | 9, 30, 55, 70 | 5, 26, 45, 58 | PAD | | Digital Ground |
| VSSA | | 40 | 33 | 25 | 21 | 19 | | Analog Ground |

5.3 Signal Descriptions

5.3.1 Analog Signals

Table 5-2. Analog Signals

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|---------------------------------------|---------|--------|--------|-------|--------|
| A0 | I | ADC-A Input 0 | 30 | 23 | 19 | 15 | 13 |
| A1 | I | ADC-A Input 1 | 29 | 22 | 18 | 14 | 12 |
| A2 | I | ADC-A Input 2 | 21 | 17 | 13 | 9 | 7 |
| A3 | I | ADC-A Input 3 | 20 | 18 | 12 | 8 | 6 |
| A4 | I | ADC-A Input 4 | 42 | 36 | 27 | 23 | 21 |
| A5 | I | ADC-A Input 5 | 28 | 35 | 17 | 13 | 11 |
| A6 | I | ADC-A Input 6 | 18 | 14 | 10 | 6 | |
| A7 | I | ADC-A Input 7 | 37 | 31 | 23 | 19 | 17 |
| A8 | I | ADC-A Input 8 | 39 | 37 | 24 | 20 | 18 |
| A9 | I | ADC-A Input 9 | 48 | 38 | 28 | 24 | 22 |
| A10 | I | ADC-A Input 10 | 50 | 40 | 29 | 25 | 23 |
| A11 | I | ADC-A Input 11 | 27 | 20 | 16 | 12 | 10 |
| A12 | I | ADC-A Input 12 | 35 | 28 | 22 | 18 | 16 |
| A13 | I | ADC-A Input 13 | 33, 34 | 26, 27 | 21 | 17 | 15 |
| A14 | I | ADC-A Input 14 | 26 | 19 | 15 | 11 | 9 |
| A15 | I | ADC-A Input 15 | 22 | | 14 | 10 | 8 |
| A16 | I | ADC-A Input 16 | 2 | 1 | 4 | 2 | 3 |
| A17 | I | ADC-A Input 17 | 60 | 48 | 33 | 27 | 24 |
| A18 | I | ADC-A Input 18 | 61 | 49 | 34 | 28 | 25 |
| A19 | I | ADC-A Input 19 | 62 | 50 | 35 | 29 | 26 |
| A20 | I | ADC-A Input 20 | 63 | 51 | 36 | 30 | 27 |
| A24 | I | ADC-A Input 24 | 64 | 52 | 37 | 31 | 28 |
| A25 | I | ADC-A Input 25 | 67 | 55 | 40 | 34 | 31 |
| A26 | I | ADC-A Input 26 | 24 | | | | |
| A27 | I | ADC-A Input 27 | 44 | | | | |
| A28 | I | ADC-A Input 28 | 47 | | | | |
| AIO208 | I | Analog Pin Used For Digital Input 208 | 23 | | | | |
| AIO209 | I | Analog Pin Used For Digital Input 209 | 24 | | | | |
| AIO210 | I | Analog Pin Used For Digital Input 210 | 25 | | | | |
| AIO225 | I | Analog Pin Used For Digital Input 225 | 42 | 36 | 27 | 23 | 21 |
| AIO226 | I | Analog Pin Used For Digital Input 226 | 43 | | | | |
| AIO227 | I | Analog Pin Used For Digital Input 227 | 44 | | | | |
| AIO228 | I | Analog Pin Used For Digital Input 228 | 45 | | | | |
| AIO229 | I | Analog Pin Used For Digital Input 229 | | 18 | | | |
| AIO231 | I | Analog Pin Used For Digital Input 231 | 30 | 23 | 19 | 15 | 13 |
| AIO232 | I | Analog Pin Used For Digital Input 232 | 29 | 22 | 18 | 14 | 12 |
| AIO233 | I | Analog Pin Used For Digital Input 233 | 22 | | 14 | 10 | 8 |
| AIO234 | I | Analog Pin Used For Digital Input 234 | 31, 32 | 24, 25 | 20 | 16 | 14 |
| AIO235 | I | Analog Pin Used For Digital Input 235 | 33, 34 | 26, 27 | 21 | 17 | 15 |
| AIO237 | I | Analog Pin Used For Digital Input 237 | 27 | 20 | 16 | 12 | 10 |
| AIO238 | I | Analog Pin Used For Digital Input 238 | 35 | 28 | 22 | 18 | 16 |
| AIO239 | I | Analog Pin Used For Digital Input 239 | 26 | 19 | 15 | 11 | 9 |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|---------------------------------------|---------|--------|--------|-------|--------|
| AIO240 | I | Analog Pin Used For Digital Input 240 | | 37 | | | |
| AIO241 | I | Analog Pin Used For Digital Input 241 | 39 | | 24 | 20 | 18 |
| AIO242 | I | Analog Pin Used For Digital Input 242 | 46 | | | | |
| AIO243 | I | Analog Pin Used For Digital Input 243 | 47 | | | | |
| AIO244 | I | Analog Pin Used For Digital Input 244 | 28 | 21 | 17 | 13 | 11 |
| AIO245 | I | Analog Pin Used For Digital Input 245 | 37 | 31 | 23 | 19 | 17 |
| AIO248 | I | Analog Pin Used For Digital Input 248 | 35 | 29 | 22 | 18 | 16 |
| AIO249 | I | Analog Pin Used For Digital Input 249 | | 35 | | | |
| AIO251 | I | Analog Pin Used For Digital Input 251 | 36 | 30 | | | |
| AIO252 | I | Analog Pin Used For Digital Input 252 | 38 | 32 | | | |
| AIO253 | I | Analog Pin Used For Digital Input 253 | 23 | | | | |
| B0 | I | ADC-B Input 0 | 39 | 41 | 24 | 20 | 18 |
| B1 | I | ADC-B Input 1 | 50 | 40 | 29 | 25 | 23 |
| B2 | I | ADC-B Input 2 | 19 | 15 | 11 | 7 | |
| B3 | I | ADC-B Input 3 | 20 | 16 | 12 | 8 | 6 |
| B4 | I | ADC-B Input 4 | 49 | 39 | 28 | 24 | 22 |
| B5 | I | ADC-B Input 5 | 38 | 32 | | | |
| B6 | I | ADC-B Input 6 | 21 | 17 | 13 | 9 | 7 |
| B7 | I | ADC-B Input 7 | 29 | 22 | 18 | 14 | 12 |
| B8 | I | ADC-B Input 8 | 42 | 36 | 27 | 23 | 21 |
| B9 | I | ADC-B Input 9 | 22 | 18 | 14 | 10 | 8 |
| B10 | I | ADC-B Input 10 | 27 | 20 | 16 | 12 | 10 |
| B11 | I | ADC-B Input 11 | 36 | 30 | | | |
| B12 | I | ADC-B Input 12 | 28 | 21 | 17 | 13 | 11 |
| B13 | I | ADC-B Input 13 | 33, 34 | 26, 27 | 21 | 17 | 15 |
| B14 | I | ADC-B Input 14 | 26 | 19 | 15 | 11 | 9 |
| B15 | I | ADC-B Input 15 | 30 | 23 | 19 | 15 | 13 |
| B16 | I | ADC-B Input 16 | 2 | 1 | 4 | 2 | 3 |
| B17 | I | ADC-B Input 17 | 60 | 48 | 33 | 27 | 24 |
| B18 | I | ADC-B Input 18 | 61 | 49 | 34 | 28 | 25 |
| B19 | I | ADC-B Input 19 | 62 | 50 | 35 | 29 | 26 |
| B20 | I | ADC-B Input 20 | 63 | 51 | 36 | 30 | 27 |
| B24 | I | ADC-B Input 24 | 65 | 53 | 38 | 32 | 29 |
| B25 | I | ADC-B Input 25 | 68 | 56 | 41 | 35 | 32 |
| B26 | I | ADC-B Input 26 | 25 | | | | |
| B27 | I | ADC-B Input 27 | 45 | | | | |
| B30 | I | ADC-B Input 30 | 37 | 31 | 23 | 19 | 17 |
| C0 | I | ADC-C Input 0 | 27 | 20 | 16 | 12 | 10 |
| C1 | I | ADC-C Input 1 | 35 | 29 | 22 | 18 | 16 |
| C2 | I | ADC-C Input 2 | 28 | 21 | 17 | 13 | 11 |
| C3 | I | ADC-C Input 3 | 37 | 31 | 23 | 19 | 17 |
| C4 | I | ADC-C Input 4 | 26 | 19 | 15 | 11 | 9 |
| C5 | I | ADC-C Input 5 | 20 | 28 | 12 | 8 | 6 |
| C6 | I | ADC-C Input 6 | 19 | 15 | 11 | 7 | |

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|--|---------|--------|--------|-------|--------|
| C7 | I | ADC-C Input 7 | 22 | 18 | 14 | 10 | 8 |
| C8 | I | ADC-C Input 8 | 49 | 39 | 28 | 24 | 22 |
| C9 | I | ADC-C Input 9 | 21 | 17 | 13 | 9 | 7 |
| C10 | I | ADC-C Input 10 | 50 | 40 | 29 | 25 | 23 |
| C11 | I | ADC-C Input 11 | 39 | 41 | 24 | 20 | 18 |
| C13 | I | ADC-C Input 13 | 33, 34 | 26, 27 | 21 | 17 | 15 |
| C14 | I | ADC-C Input 14 | 42 | 42 | 27 | 23 | 21 |
| C15 | I | ADC-C Input 15 | 30 | 23 | 19 | 15 | 13 |
| C16 | I | ADC-C Input 16 | 2 | 1 | 4 | 2 | 3 |
| C17 | I | ADC-C Input 17 | 60 | 48 | 33 | 27 | 24 |
| C18 | I | ADC-C Input 18 | 61 | 49 | 34 | 28 | 25 |
| C19 | I | ADC-C Input 19 | 62 | 50 | 35 | 29 | 26 |
| C20 | I | ADC-C Input 20 | 63 | 51 | 36 | 30 | 27 |
| C24 | I | ADC-C Input 24 | 66 | 54 | 39 | 33 | 30 |
| C25 | I | ADC-C Input 25 | 23 | | | | |
| C26 | I | ADC-C Input 26 | 43 | | | | |
| C27 | I | ADC-C Input 27 | 46 | | | | |
| CMP1_HN0 | I | CMPSS-1 High Comparator Negative Input 0 | 22 | | 14 | 10 | 8 |
| CMP1_HN1 | I | CMPSS-1 High Comparator Negative Input 1 | 27 | 20 | 16 | 12 | 10 |
| CMP1_HP0 | I | CMPSS-1 High Comparator Positive Input 0 | 21 | 17 | 13 | 9 | 7 |
| CMP1_HP1 | I | CMPSS-1 High Comparator Positive Input 1 | 27 | 20 | 16 | 12 | 10 |
| CMP1_HP2 | I | CMPSS-1 High Comparator Positive Input 2 | 18 | 14 | 10 | 6 | |
| CMP1_HP3 | I | CMPSS-1 High Comparator Positive Input 3 | 22 | | 14 | 10 | 8 |
| CMP1_HP4 | I | CMPSS-1 High Comparator Positive Input 4 | 29 | 22 | 18 | 14 | 12 |
| CMP1_HP5 | I | CMPSS-1 High Comparator Positive Input 5 | 38 | 32 | | | |
| CMP1_LN0 | I | CMPSS-1 Low Comparator Negative Input 0 | 22 | | 14 | 10 | 8 |
| CMP1_LN1 | I | CMPSS-1 Low Comparator Negative Input 1 | 27 | 20 | 16 | 12 | 10 |
| CMP1_LP0 | I | CMPSS-1 Low Comparator Positive Input 0 | 21 | 17 | 13 | 9 | 7 |
| CMP1_LP1 | I | CMPSS-1 Low Comparator Positive Input 1 | 27 | 20 | 16 | 12 | 10 |
| CMP1_LP2 | I | CMPSS-1 Low Comparator Positive Input 2 | 18 | 14 | 10 | 6 | |
| CMP1_LP3 | I | CMPSS-1 Low Comparator Positive Input 3 | 22 | | 14 | 10 | 8 |
| CMP1_LP4 | I | CMPSS-1 Low Comparator Positive Input 4 | 29 | 22 | 18 | 14 | 12 |
| CMP1_LP5 | I | CMPSS-1 Low Comparator Positive Input 5 | 38 | 32 | | | |
| CMP2_HN0 | I | CMPSS-2 High Comparator Negative Input 0 | 50 | 40 | 29 | 25 | 23 |
| CMP2_HN1 | I | CMPSS-2 High Comparator Negative Input 1 | 35 | 28 | 22 | 18 | 16 |
| CMP2_HP0 | I | CMPSS-2 High Comparator Positive Input 0 | 42 | 36 | 27 | 23 | 21 |
| CMP2_HP1 | I | CMPSS-2 High Comparator Positive Input 1 | 35 | 28 | 22 | 18 | 16 |
| CMP2_HP2 | I | CMPSS-2 High Comparator Positive Input 2 | 48 | 38 | 28 | 24 | 22 |
| CMP2_HP3 | I | CMPSS-2 High Comparator Positive Input 3 | 50 | 40, 41 | 29 | 25 | 23 |
| CMP2_HP5 | I | CMPSS-2 High Comparator Positive Input 5 | 28 | 35 | 17 | 13 | 11 |
| CMP2_LN0 | I | CMPSS-2 Low Comparator Negative Input 0 | 50 | 40 | 29 | 25 | 23 |
| CMP2_LN1 | I | CMPSS-2 Low Comparator Negative Input 1 | 35 | 28 | 22 | 18 | 16 |
| CMP2_LP0 | I | CMPSS-2 Low Comparator Positive Input 0 | 42 | 36 | 27 | 23 | 21 |
| CMP2_LP1 | I | CMPSS-2 Low Comparator Positive Input 1 | 35 | 28 | 22 | 18 | 16 |

ADVANCE INFORMATION

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|--|---------|--------|--------|-------|--------|
| CMP2_LP2 | I | CMPSS-2 Low Comparator Positive Input 2 | 48 | 38 | 28 | 24 | 22 |
| CMP2_LP3 | I | CMPSS-2 Low Comparator Positive Input 3 | 50 | 40, 41 | 29 | 25 | 23 |
| CMP2_LP5 | I | CMPSS-2 Low Comparator Positive Input 5 | 28 | 35 | 17 | 13 | 11 |
| CMP3_HN0 | I | CMPSS-3 High Comparator Negative Input 0 | 20 | 16 | 12 | 8 | 6 |
| CMP3_HN1 | I | CMPSS-3 High Comparator Negative Input 1 | 28 | 21 | 17 | 13 | 11 |
| CMP3_HP0 | I | CMPSS-3 High Comparator Positive Input 0 | 19 | 15 | 11 | 7 | |
| CMP3_HP1 | I | CMPSS-3 High Comparator Positive Input 1 | 28 | 21 | 17 | 13 | 11 |
| CMP3_HP2 | I | CMPSS-3 High Comparator Positive Input 2 | 30 | 23 | 19 | 15 | 13 |
| CMP3_HP3 | I | CMPSS-3 High Comparator Positive Input 3 | 20 | 16 | 12 | 8 | 6 |
| CMP3_HP4 | I | CMPSS-3 High Comparator Positive Input 4 | 26 | 19 | 15 | 11 | 9 |
| CMP3_HP5 | I | CMPSS-3 High Comparator Positive Input 5 | 20 | 18 | 12 | 8 | 6 |
| CMP3_LN0 | I | CMPSS-3 Low Comparator Negative Input 0 | 20 | 16 | 12 | 8 | 6 |
| CMP3_LN1 | I | CMPSS-3 Low Comparator Negative Input 1 | 28 | 21 | 17 | 13 | 11 |
| CMP3_LP0 | I | CMPSS-3 Low Comparator Positive Input 0 | 19 | 15 | 11 | 7 | |
| CMP3_LP1 | I | CMPSS-3 Low Comparator Positive Input 1 | 28 | 21 | 17 | 13 | 11 |
| CMP3_LP2 | I | CMPSS-3 Low Comparator Positive Input 2 | 30 | 23 | 19 | 15 | 13 |
| CMP3_LP3 | I | CMPSS-3 Low Comparator Positive Input 3 | 20 | 16 | 12 | 8 | 6 |
| CMP3_LP4 | I | CMPSS-3 Low Comparator Positive Input 4 | 26 | 19 | 15 | 11 | 9 |
| CMP3_LP5 | I | CMPSS-3 Low Comparator Positive Input 5 | 20 | 18 | 12 | 8 | 6 |
| CMP4_HN0 | I | CMPSS-4 High Comparator Negative Input 0 | 42 | 42 | 27 | 23 | 21 |
| CMP4_HN1 | I | CMPSS-4 High Comparator Negative Input 1 | 37 | 31 | 23 | 19 | 17 |
| CMP4_HP0 | I | CMPSS-4 High Comparator Positive Input 0 | 49 | 39 | 28 | 24 | 22 |
| CMP4_HP1 | I | CMPSS-4 High Comparator Positive Input 1 | 37 | 31 | 23 | 19 | 17 |
| CMP4_HP2 | I | CMPSS-4 High Comparator Positive Input 2 | 35 | 29 | 22 | 18 | 16 |
| CMP4_HP3 | I | CMPSS-4 High Comparator Positive Input 3 | 42 | 42 | 27 | 23 | 21 |
| CMP4_HP4 | I | CMPSS-4 High Comparator Positive Input 4 | 39 | 37 | 24 | 20 | 18 |
| CMP4_HP5 | I | CMPSS-4 High Comparator Positive Input 5 | 36 | 30 | | | |
| CMP4_LN0 | I | CMPSS-4 Low Comparator Negative Input 0 | 42 | 42 | 27 | 23 | 21 |
| CMP4_LN1 | I | CMPSS-4 Low Comparator Negative Input 1 | 37 | 31 | 23 | 19 | 17 |
| CMP4_LP0 | I | CMPSS-4 Low Comparator Positive Input 0 | 49 | 39 | 28 | 24 | 22 |
| CMP4_LP1 | I | CMPSS-4 Low Comparator Positive Input 1 | 37 | 31 | 23 | 19 | 17 |
| CMP4_LP2 | I | CMPSS-4 Low Comparator Positive Input 2 | 35 | 29 | 22 | 18 | 16 |
| CMP4_LP3 | I | CMPSS-4 Low Comparator Positive Input 3 | 42 | 42 | 27 | 23 | 21 |
| CMP4_LP4 | I | CMPSS-4 Low Comparator Positive Input 4 | 39 | 37 | 24 | 20 | 18 |
| CMP4_LP5 | I | CMPSS-4 Low Comparator Positive Input 5 | 36 | 30 | | | |
| D0 | I | ADC-D Input 0 | 64 | 52 | 37 | 31 | 28 |
| D1 | I | ADC-D Input 1 | 65 | 53 | 38 | 32 | 29 |
| D2 | I | ADC-D Input 2 | 66 | 54 | 39 | 33 | 30 |
| D3 | I | ADC-D Input 3 | 67 | 55 | 40 | 34 | 31 |
| D4 | I | ADC-D Input 4 | 68 | 56 | 41 | 35 | 32 |
| D5 | I | ADC-D Input 5 | 23 | | | | |
| D6 | I | ADC-D Input 6 | 24 | | | | |
| D7 | I | ADC-D Input 7 | 25 | | | | |
| D8 | I | ADC-D Input 8 | 43 | | | | |

ADVANCE INFORMATION

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|------------------------|---------|--------|--------|-------|--------|
| D9 | I | ADC-D Input 9 | 44 | | | | |
| D10 | I | ADC-D Input 10 | 45 | | | | |
| D11 | I | ADC-D Input 11 | 29 | 22 | 18 | 14 | 12 |
| D12 | I | ADC-D Input 12 | 37 | 31 | 23 | 19 | 17 |
| D13 | I | ADC-D Input 13 | 33, 34 | 26, 27 | 21 | 17 | 15 |
| D14 | I | ADC-D Input 14 | 18 | 14 | 10 | 6 | |
| D15 | I | ADC-D Input 15 | 38 | 32 | | | |
| D16 | I | ADC-D Input 16 | 36 | 30 | | | |
| D18 | I | ADC-D Input 18 | 46 | | | | |
| D19 | I | ADC-D Input 19 | 47 | | | | |
| D20 | I | ADC-D Input 20 | 31, 32 | 24, 25 | 20 | 16 | 14 |
| DACA_OUT | O | Buffered DAC-A Output. | 30 | 23 | 19 | 15 | 13 |
| DACB_OUT | O | Buffered DAC-B Output. | 29 | 22 | 18 | 14 | 12 |
| E0 | I | ADC-E Input 0 | 64 | 52 | 37 | 31 | 28 |
| E1 | I | ADC-E Input 1 | 65 | 53 | 38 | 32 | 29 |
| E2 | I | ADC-E Input 2 | 66 | 54 | 39 | 33 | 30 |
| E3 | I | ADC-E Input 3 | 67 | 55 | 40 | 34 | 31 |
| E4 | I | ADC-E Input 4 | 68 | 56 | 41 | 35 | 32 |
| E5 | I | ADC-E Input 5 | 23 | | | | |
| E6 | I | ADC-E Input 6 | 24 | | | | |
| E7 | I | ADC-E Input 7 | 25 | | | | |
| E8 | I | ADC-E Input 8 | 43 | | | | |
| E9 | I | ADC-E Input 9 | 44 | | | | |
| E10 | I | ADC-E Input 10 | 45 | | | | |
| E11 | I | ADC-E Input 11 | 35 | 29 | 22 | 18 | 16 |
| E12 | I | ADC-E Input 12 | 19 | 15 | 11 | 7 | |
| E13 | I | ADC-E Input 13 | 33, 34 | 26, 27 | 21 | 17 | 15 |
| E14 | I | ADC-E Input 14 | 18 | 14 | 10 | 6 | |
| E15 | I | ADC-E Input 15 | 38 | 32 | | | |
| E16 | I | ADC-E Input 16 | 36 | 30 | | | |
| E18 | I | ADC-E Input 18 | 46 | | | | |
| E19 | I | ADC-E Input 19 | 47 | | | | |
| E20 | I | ADC-E Input 20 | 31, 32 | 24, 25 | 20 | 16 | 14 |
| E30 | I | ADC-E Input 30 | 37 | 31 | 23 | 19 | 17 |
| PGA1_INM | I | PGA-1 Minus | 22 | 18 | 14 | 10 | 8 |
| PGA1_INP | I | PGA-1 Plus | 21 | 17 | 13 | 9 | 7 |
| PGA1_OUT | O | PGA-1 Output | 26 | 19 | 15 | 11 | 9 |
| PGA2_INM | I | PGA-2 Minus | 28 | 21 | 17 | 13 | 11 |
| PGA2_INP | I | PGA-2 Plus | 20 | 16 | 12 | 8 | 6 |
| PGA2_OUT | O | PGA-2 Output | 27 | 20 | 16 | 12 | 10 |
| PGA3_INM | I | PGA-3 Minus | 36 | 30 | 23 | 19 | 17 |
| PGA3_INP | I | PGA-3 Plus | 35 | 29 | 22 | 18 | 16 |
| PGA3_OUT | O | PGA-3 Output | 38 | 32 | 24 | 20 | 18 |

ADVANCE INFORMATION

Table 5-2. Analog Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|---|---------|--------|--------|-------|--------|
| VREFHI | I | ADC High Reference. In external reference mode, externally drive the high reference voltage onto this pin. In internal reference mode, a voltage is driven onto this pin by the device. In either mode, place at least a 2.2- μ F capacitor on this pin. This capacitor should be placed as close to the device as possible between the VREFHI and VREFLO pins. | 31, 32 | 24, 25 | 20 | 16 | 14 |
| VREFLO | I | ADC Low Reference | 33, 34 | 26, 27 | 21 | 17 | 15 |

5.3.2 Digital Signals

Table 5-3. Digital Signals

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-----------------|----------|--|--|--|--|-----------------------------------|--------------------------|-----------------------|
| ADCE_EXTMUXSEL0 | O | ADCE external mux selection pin for position 0 | 20, 228 | 18, 60 | 14, 48 | 10, 33 | 6, 27 | 24 |
| ADCE_EXTMUXSEL1 | O | ADCE external mux selection pin for position 1 | 21, 226 | 19, 61 | 15, 49 | 11, 34 | 7, 28 | 25 |
| ADCE_EXTMUXSEL2 | O | ADCE external mux selection pin for position 2 | 242 | 20 | 16 | 12 | 8 | 6 |
| ADCE_EXTMUXSEL3 | O | ADCE external mux selection pin for position 3 | 224 | 21 | 17 | 13 | 9 | 7 |
| ADCSOCAO | O | ADC Start of Conversion A for External ADC | 8, 33, 53, 70, 74, 228 | 16, 18, 65, 74, 86, 95 | 12, 14, 53, 74 | 10, 38, 58 | 6, 32, 47 | 29 |
| ADCSOCBO | O | ADC Start of Conversion B for External ADC | 10, 32, 54 | 17, 79, 122 | 13, 64, 93 | 49, 76 | 40, 63 | 37 |
| AUXCLKIN | I | Auxiliary Clock Input | 29 | 1 | 100 | 3 | 1 | 2 |
| CLB_OUTPUTXBAR1 | O | CLB Output X-BAR Output 1 | 19, 22 | 88, 104 | 69, 83 | 51, 67 | 42, 56 | 39, 51 |
| CLB_OUTPUTXBAR2 | O | CLB Output X-BAR Output 2 | 7, 47 | 8, 105 | 6, 84 | 68 | 57 | 52 |
| CLB_OUTPUTXBAR3 | O | CLB Output X-BAR Output 3 | 23, 42, 44 | 94, 102, 106 | 81, 85 | 57, 65, 69 | 54 | 49 |
| CLB_OUTPUTXBAR4 | O | CLB Output X-BAR Output 4 | 10, 40, 43, 45 | 91, 101, 110, 122 | 80, 93 | 54, 64, 73, 76 | 53, 63 | 48 |
| CLB_OUTPUTXBAR5 | O | CLB Output X-BAR Output 5 | 5, 8, 52 | 15, 95, 118 | 11, 74, 89 | 58, 74 | 47, 61 | 55 |
| CLB_OUTPUTXBAR6 | O | CLB Output X-BAR Output 6 | 4, 15, 53 | 16, 96, 124 | 12, 75, 95 | 59, 78 | 48 | 43 |
| CLB_OUTPUTXBAR7 | O | CLB Output X-BAR Output 7 | 1, 14, 56 | 80, 99, 125 | 65, 78, 96 | 62, 79 | 51 | 46 |
| CLB_OUTPUTXBAR8 | O | CLB Output X-BAR Output 8 | 0, 6, 57, 80 | 81, 100, 116, 126 | 66, 79, 97 | 63, 80 | 52, 64 | 1, 47 |
| EPWM1_A | O | ePWM-1 Output A | 0, 4, 30, 77, 80, 224 | 21, 96, 100, 113, 116, 127 | 17, 75, 79, 98 | 1, 13, 59, 63 | 9, 48, 52 | 7, 43, 47 |
| EPWM1_B | O | ePWM-1 Output B | 1, 5, 31, 75, 81, 226 | 19, 99, 111, 117, 118, 128 | 15, 78, 89, 99 | 2, 11, 62, 74 | 7, 51, 61 | 46, 55 |
| EPWM2_A | O | ePWM-2 Output A | 2, 6, 7, 41, 79, 230 | 50, 98, 103, 105, 115, 126 | 40, 77, 82, 84, 97 | 29, 61, 66, 68, 80 | 25, 50, 55, 57, 64 | 1, 23, 45, 50, 52 |
| EPWM2_B | O | ePWM-2 Output B | 3, 7, 40, 74, 78, 227, 228 | 18, 48, 86, 97, 101, 105, 114 | 14, 38, 76, 80, 84 | 10, 28, 60, 64, 68 | 6, 24, 49, 53, 57 | 22, 44, 48, 52 |
| EPWM3_A | O | ePWM-3 Output A | 0, 4, 14, 68, 78, 80, 227 | 48, 72, 96, 100, 114, 116, 125 | 38, 75, 79, 96 | 28, 59, 63, 79 | 24, 48, 52 | 22, 43, 47 |
| EPWM3_B | O | ePWM-3 Output B | 1, 5, 15, 69, 79, 230 | 50, 73, 99, 115, 118, 124 | 40, 78, 89, 95 | 29, 62, 74, 78 | 25, 51, 61 | 23, 46, 55 |
| EPWM4_A | O | ePWM-4 Output A | 2, 6, 22, 76, 242 | 20, 98, 104, 112, 126 | 16, 77, 83, 97 | 12, 61, 67, 80 | 8, 50, 56, 64 | 1, 6, 45, 51 |
| EPWM4_B | O | ePWM-4 Output B | 3, 7, 23, 71 | 83, 97, 102, 105 | 76, 81, 84 | 60, 65, 68 | 49, 54, 57 | 44, 49, 52 |
| EPWM5_A | O | ePWM-5 Output A | 8, 37, 72 | 76, 84, 95 | 61, 74 | 46, 58 | 37, 47 | 34 |
| EPWM5_B | O | ePWM-5 Output B | 9, 35, 73 | 78, 85, 119 | 63, 90 | 48, 75 | 39, 62 | 36, 56 |
| EPWM6_A | O | ePWM-6 Output A | 10, 17, 18, 72, 75, 226 | 19, 67, 84, 87, 111, 122 | 15, 55, 68, 93 | 11, 40, 50, 76 | 7, 34, 41, 63 | 31, 38 |
| EPWM6_B | O | ePWM-6 Output B | 11, 19, 69 | 64, 73, 88 | 52, 69 | 37, 51 | 31, 42 | 28, 39 |
| EPWM7_A | O | ePWM-7 Output A | 12, 28, 41, 64, 68, 236 | 2, 49, 56, 63, 72, 103 | 1, 39, 51, 82 | 4, 28, 36, 66 | 2, 24, 30, 55 | 3, 22, 27, 50 |
| EPWM7_B | O | ePWM-7 Output B | 13, 29, 67, 215 | 1, 10, 47, 62 | 50, 100 | 3, 35 | 1, 29 | 2, 26 |
| EPWM8_A | O | ePWM-8 Output A | 14, 24, 73, 78 | 68, 85, 114, 125 | 56, 96 | 41, 79 | 35 | 32 |
| EPWM8_B | O | ePWM-8 Output B | 15, 32, 79 | 79, 115, 124 | 64, 95 | 49, 78 | 40 | 37 |
| EPWM9_A | O | ePWM-9 Output A | 16, 24, 71, 73 | 66, 68, 83, 85 | 54, 56 | 39, 41 | 33, 35 | 30, 32 |
| EPWM9_B | O | ePWM-9 Output B | 17, 72 | 67, 84 | 55 | 40 | 34 | 31 |
| EPWM10_A | O | ePWM-10 Output A | 2, 62, 211, 228 | 18, 43, 58, 98 | 14, 46, 77 | 10, 31, 61 | 6, 50 | 45 |
| EPWM10_B | O | ePWM-10 Output B | 1, 63, 212, 226 | 19, 44, 59, 99 | 15, 47, 78 | 11, 32, 62 | 7, 51 | 46 |
| EPWM11_A | O | ePWM-11 Output A | 8, 64, 213, 242 | 20, 45, 56, 95 | 16, 74 | 12, 58 | 8, 47 | 6 |
| EPWM11_B | O | ePWM-11 Output B | 4, 65, 214, 224 | 21, 46, 57, 96 | 17, 75 | 13, 59 | 9, 48 | 7, 43 |
| EPWM12_A | O | ePWM-12 Output A | 20, 23, 66, 236, 253 | 9, 49, 60, 102 | 39, 41, 48, 81 | 28, 33, 65 | 24, 27, 54 | 22, 24, 49 |
| EPWM12_B | O | ePWM-12 Output B | 21, 41, 60, 67, 247 | 10, 52, 61, 103 | 42, 44, 49, 82 | 34, 66 | 28, 55 | 25, 50 |
| EQEP1_A | I | eQEP-1 Input A | 6, 10, 20, 25, 28, 35, 40, 44, 50, 56, 64, 65, 77, 224 | 2, 13, 21, 56, 57, 60, 69, 78, 80, 101, 106, 113, 122, 126 | 1, 9, 17, 48, 57, 63, 65, 80, 85, 93, 97 | 4, 13, 33, 42, 48, 64, 69, 76, 80 | 2, 9, 27, 39, 53, 63, 64 | 1, 3, 7, 24, 36, 48 |
| EQEP1_B | I | eQEP-1 Input B | 7, 11, 21, 29, 37, 41, 51, 57, 66, 69, 74, 228 | 1, 9, 14, 18, 61, 64, 73, 76, 81, 86, 103, 105 | 10, 14, 49, 52, 61, 66, 82, 84, 100 | 3, 10, 34, 37, 46, 66, 68 | 1, 6, 28, 31, 37, 55, 57 | 2, 25, 28, 34, 50, 52 |

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|--------------|----------|--|--|---|--|---------------------------------------|-------------------------------|-------------------------------|
| EQEP1_INDEX | I/O | eQEP-1 Index | 0, 9, 13, 17, 23, 31, 32, 43, 53, 59, 67, 72, 76, 80, 236, 242 | 10, 16, 20, 49, 62, 67, 79, 84, 91, 100, 102, 112, 116, 119, 121, 128 | 12, 16, 39, 50, 55, 64, 79, 81, 90, 92, 99 | 2, 12, 28, 35, 40, 49, 54, 63, 65, 75 | 8, 24, 29, 34, 40, 52, 54, 62 | 6, 22, 26, 31, 37, 47, 49, 56 |
| EQEP1_STROBE | I/O | eQEP-1 Strobe | 1, 8, 12, 16, 22, 30, 42, 52, 58, 68, 71, 75, 226 | 15, 19, 63, 66, 72, 82, 83, 94, 95, 99, 104, 111, 127 | 11, 15, 51, 54, 67, 74, 78, 83, 98 | 1, 11, 36, 39, 57, 58, 62, 67 | 7, 30, 33, 47, 51, 56 | 27, 30, 46, 51 |
| EQEP2_A | I | eQEP-2 Input A | 11, 14, 18, 24, 54, 69, 215 | 17, 47, 64, 68, 73, 87, 125 | 13, 52, 56, 68, 96 | 37, 41, 50, 79 | 31, 35, 41 | 28, 32, 38 |
| EQEP2_B | I | eQEP-2 Input B | 15, 16, 19, 25, 33, 55, 70 | 51, 65, 66, 69, 74, 88, 124 | 43, 53, 54, 57, 69, 95 | 38, 39, 42, 51, 78 | 32, 33, 42 | 29, 30, 39 |
| EQEP2_INDEX | I/O | eQEP-2 Index | 26, 29, 57, 71 | 1, 70, 81, 83 | 58, 66, 100 | 3, 43 | 1 | 2 |
| EQEP2_STROBE | I/O | eQEP-2 Strobe | 4, 27, 28, 56, 64 | 2, 56, 71, 80, 96 | 1, 59, 65, 75 | 4, 44, 59 | 2, 48 | 3, 43 |
| EQEP3_A | I | eQEP-3 Input A | 22, 25, 70, 211 | 43, 69, 74, 104 | 57, 83 | 42, 67 | 56 | 51 |
| EQEP3_B | I | eQEP-3 Input B | 9, 26, 72, 212 | 44, 70, 84, 119 | 58, 90 | 43, 75 | 62 | 56 |
| EQEP3_INDEX | I/O | eQEP-3 Index | 11, 14, 30, 69, 81, 214 | 46, 64, 73, 87, 117, 127 | 52, 68, 98 | 1, 37, 50 | 31, 41 | 28, 38 |
| EQEP3_STROBE | I/O | eQEP-3 Strobe | 10, 16, 27, 40, 71, 213 | 45, 66, 71, 83, 101, 122 | 54, 59, 80, 93 | 39, 44, 64, 76 | 33, 53, 63 | 30, 48 |
| ERRORSTS | O | Error Status Output. This signal requires an external pull-down. | 24, 28, 29, 55, 64, 73 | 1, 2, 51, 56, 68, 85 | 1, 43, 56, 100 | 3, 4, 41 | 1, 2, 35 | 2, 3, 32 |
| FSIRXA_CLK | I | FSIRX-A Input Clock | 0, 4, 13, 30, 33, 54, 57, 67, 70 | 10, 17, 62, 65, 74, 81, 96, 100, 127 | 13, 50, 53, 66, 75, 79, 98 | 1, 35, 38, 59, 63 | 29, 32, 48, 52 | 26, 29, 43, 47 |
| FSIRXA_D0 | I | FSIRX-A Primary Data Input | 3, 12, 32, 40, 44, 52, 58, 68 | 15, 63, 72, 79, 82, 97, 101, 106 | 11, 51, 64, 67, 76, 80, 85 | 36, 49, 60, 64, 69 | 30, 40, 49, 53 | 27, 37, 44, 48 |
| FSIRXA_D1 | I | FSIRX-A Optional Additional Data Input | 2, 11, 31, 41, 53, 56, 69 | 16, 64, 73, 80, 98, 103, 128 | 12, 52, 65, 77, 82, 99 | 2, 37, 61, 66 | 31, 50, 55 | 28, 45, 50 |
| FSITXA_CLK | O | FSITX-A Output Clock | 7, 10, 27, 44, 51, 78 | 14, 71, 105, 106, 114, 122 | 10, 59, 84, 85, 93 | 44, 68, 69, 76 | 57, 63 | 52 |
| FSITXA_D0 | O | FSITX-A Primary Data Output | 6, 9, 26, 45, 49, 80 | 12, 70, 110, 116, 119, 126 | 8, 58, 90, 97 | 43, 73, 75, 80 | 62, 64 | 1, 56 |
| FSITXA_D1 | O | FSITX-A Optional Additional Data Output | 5, 6, 8, 25, 46, 50, 81 | 4, 13, 69, 95, 117, 118, 126 | 9, 57, 74, 89, 97 | 6, 42, 58, 74, 80 | 47, 61, 64 | 1, 55 |
| GPIO0 | I/O | General-Purpose Input Output 0 | 0 | 100 | 79 | 63 | 52 | 47 |
| GPIO1 | I/O | General-Purpose Input Output 1 | 1 | 99 | 78 | 62 | 51 | 46 |
| GPIO2 | I/O | General-Purpose Input Output 2 | 2 | 98 | 77 | 61 | 50 | 45 |
| GPIO3 | I/O | General-Purpose Input Output 3 | 3 | 97 | 76 | 60 | 49 | 44 |
| GPIO4 | I/O | General-Purpose Input Output 4 | 4 | 96 | 75 | 59 | 48 | 43 |
| GPIO5 | I/O | General-Purpose Input Output 5 | 5 | 118 | 89 | 74 | 61 | 55 |
| GPIO6 | I/O | General-Purpose Input Output 6 | 6 | 126 | 97 | 80 | 64 | 1 |
| GPIO7 | I/O | General-Purpose Input Output 7 | 7 | 105 | 84 | 68 | 57 | 52 |
| GPIO8 | I/O | General-Purpose Input Output 8 | 8 | 95 | 74 | 58 | 47 | |
| GPIO9 | I/O | General-Purpose Input Output 9 | 9 | 119 | 90 | 75 | 62 | 56 |
| GPIO10 | I/O | General-Purpose Input Output 10 | 10 | 122 | 93 | 76 | 63 | |
| GPIO11 | I/O | General-Purpose Input Output 11 | 11 | 64 | 52 | 37 | 31 | 28 |
| GPIO12 | I/O | General-Purpose Input Output 12 | 12 | 63 | 51 | 36 | 30 | 27 |
| GPIO13 | I/O | General-Purpose Input Output 13 | 13 | 62 | 50 | 35 | 29 | 26 |
| GPIO14 | I/O | General-Purpose Input Output 14 | 14 | 125 | 96 | 79 | | |
| GPIO15 | I/O | General-Purpose Input Output 15 | 15 | 124 | 95 | 78 | | |
| GPIO16 | I/O | General-Purpose Input Output 16 | 16 | 66 | 54 | 39 | 33 | 30 |
| GPIO17 | I/O | General-Purpose Input Output 17 | 17 | 67 | 55 | 40 | 34 | 31 |
| GPIO18 | I/O | General-Purpose Input Output 18 | 18 | 87 | 68 | 50 | 41 | 38 |
| GPIO19 | I/O | General-Purpose Input Output 19 | 19 | 88 | 69 | 51 | 42 | 39 |
| GPIO20 | I/O | General-Purpose Input Output 20 | 20 | 60 | 48 | 33 | 27 | 24 |
| GPIO21 | I/O | General-Purpose Input Output 21 | 21 | 61 | 49 | 34 | 28 | 25 |
| GPIO22 | I/O | General-Purpose Input Output 22 | 22 | 104 | 83 | 67 | 56 | 51 |
| GPIO23 | I/O | General-Purpose Input Output 23 | 23 | 102 | 81 | 65 | 54 | 49 |
| GPIO24 | I/O | General-Purpose Input Output 24 | 24 | 68 | 56 | 41 | 35 | 32 |
| GPIO25 | I/O | General-Purpose Input Output 25 | 25 | 69 | 57 | 42 | | |
| GPIO26 | I/O | General-Purpose Input Output 26 | 26 | 70 | 58 | 43 | | |

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|----------------------------------|------|---------|--------|--------|-------|--------|
| GPIO27 | I/O | General-Purpose Input Output 27 | 27 | 71 | 59 | 44 | | |
| GPIO28 | I/O | General-Purpose Input Output 28 | 28 | 2 | 1 | 4 | 2 | 3 |
| GPIO29 | I/O | General-Purpose Input Output 29 | 29 | 1 | 100 | 3 | 1 | 2 |
| GPIO30 | I/O | General-Purpose Input Output 30 | 30 | 127 | 98 | 1 | | |
| GPIO31 | I/O | General-Purpose Input Output 31 | 31 | 128 | 99 | 2 | | |
| GPIO32 | I/O | General-Purpose Input Output 32 | 32 | 79 | 64 | 49 | 40 | 37 |
| GPIO33 | I/O | General-Purpose Input Output 33 | 33 | 65 | 53 | 38 | 32 | 29 |
| GPIO34 | I/O | General-Purpose Input Output 34 | 34 | 123 | 94 | 77 | | |
| GPIO35 | I/O | General-Purpose Input Output 35 | 35 | 78 | 63 | 48 | 39 | 36 |
| GPIO37 | I/O | General-Purpose Input Output 37 | 37 | 76 | 61 | 46 | 37 | 34 |
| GPIO40 | I/O | General-Purpose Input Output 40 | 40 | 101 | 80 | 64 | 53 | 48 |
| GPIO41 | I/O | General-Purpose Input Output 41 | 41 | 103 | 82 | 66 | 55 | 50 |
| GPIO42 | I/O | General-Purpose Input Output 42 | 42 | 94 | | 57 | | |
| GPIO43 | I/O | General-Purpose Input Output 43 | 43 | 91 | | 54 | | |
| GPIO44 | I/O | General-Purpose Input Output 44 | 44 | 106 | 85 | 69 | | |
| GPIO45 | I/O | General-Purpose Input Output 45 | 45 | 110 | | 73 | | |
| GPIO46 | I/O | General-Purpose Input Output 46 | 46 | 4 | | 6 | | |
| GPIO47 | I/O | General-Purpose Input Output 47 | 47 | 8 | 6 | | | |
| GPIO48 | I/O | General-Purpose Input Output 48 | 48 | 11 | 7 | | | |
| GPIO49 | I/O | General-Purpose Input Output 49 | 49 | 12 | 8 | | | |
| GPIO50 | I/O | General-Purpose Input Output 50 | 50 | 13 | 9 | | | |
| GPIO51 | I/O | General-Purpose Input Output 51 | 51 | 14 | 10 | | | |
| GPIO52 | I/O | General-Purpose Input Output 52 | 52 | 15 | 11 | | | |
| GPIO53 | I/O | General-Purpose Input Output 53 | 53 | 16 | 12 | | | |
| GPIO54 | I/O | General-Purpose Input Output 54 | 54 | 17 | 13 | | | |
| GPIO55 | I/O | General-Purpose Input Output 55 | 55 | 51 | 43 | | | |
| GPIO56 | I/O | General-Purpose Input Output 56 | 56 | 80 | 65 | | | |
| GPIO57 | I/O | General-Purpose Input Output 57 | 57 | 81 | 66 | | | |
| GPIO58 | I/O | General-Purpose Input Output 58 | 58 | 82 | 67 | | | |
| GPIO59 | I/O | General-Purpose Input Output 59 | 59 | 121 | 92 | | | |
| GPIO60 | I/O | General-Purpose Input Output 60 | 60 | 52 | 44 | | | |
| GPIO61 | I/O | General-Purpose Input Output 61 | 61 | 120 | 91 | | | |
| GPIO62 | I/O | General-Purpose Input Output 62 | 62 | 58 | 46 | 31 | | |
| GPIO63 | I/O | General-Purpose Input Output 63 | 63 | 59 | 47 | 32 | | |
| GPIO64 | I/O | General-Purpose Input Output 64 | 64 | 56 | | | | |
| GPIO65 | I/O | General-Purpose Input Output 65 | 65 | 57 | | | | |
| GPIO66 | I/O | General-Purpose Input Output 66 | 66 | 9 | | | | |
| GPIO67 | I/O | General-Purpose Input Output 67 | 67 | 10 | | | | |
| GPIO68 | I/O | General-Purpose Input Output 68 | 68 | 72 | | | | |
| GPIO69 | I/O | General-Purpose Input Output 69 | 69 | 73 | | | | |
| GPIO70 | I/O | General-Purpose Input Output 70 | 70 | 74 | | | | |
| GPIO71 | I/O | General-Purpose Input Output 71 | 71 | 83 | | | | |
| GPIO72 | I/O | General-Purpose Input Output 72 | 72 | 84 | | | | |
| GPIO73 | I/O | General-Purpose Input Output 73 | 73 | 85 | | | | |
| GPIO74 | I/O | General-Purpose Input Output 74 | 74 | 86 | | | | |
| GPIO75 | I/O | General-Purpose Input Output 75 | 75 | 111 | | | | |
| GPIO76 | I/O | General-Purpose Input Output 76 | 76 | 112 | | | | |
| GPIO77 | I/O | General-Purpose Input Output 77 | 77 | 113 | | | | |
| GPIO78 | I/O | General-Purpose Input Output 78 | 78 | 114 | | | | |
| GPIO79 | I/O | General-Purpose Input Output 79 | 79 | 115 | | | | |
| GPIO80 | I/O | General-Purpose Input Output 80 | 80 | 116 | | | | |
| GPIO81 | I/O | General-Purpose Input Output 81 | 81 | 117 | | | | |
| GPIO211 | I/O | General-Purpose Input Output 211 | 211 | 43 | | | | |
| GPIO212 | I/O | General-Purpose Input Output 212 | 212 | 44 | | | | |

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|--------------|----------|---|--|--|---|---|--------------------------------------|-----------------------------------|
| GPIO213 | I/O | General-Purpose Input Output 213 | 213 | 45 | | | | |
| GPIO214 | I/O | General-Purpose Input Output 214 | 214 | 46 | | | | |
| GPIO215 | I/O | General-Purpose Input Output 215 | 215 | 47 | | | | |
| GPIO224 | I/O | General-Purpose Input Output 224 | 224 | 21 | 17 | 13 | 9 | 7 |
| GPIO226 | I/O | General-Purpose Input Output 226 | 226 | 19 | 15 | 11 | 7 | |
| GPIO227 | I/O | General-Purpose Input Output 227 | 227 | 48 | 38 | 28 | 24 | 22 |
| GPIO228 | I/O | General-Purpose Input Output 228 | 228 | 18 | 14 | 10 | 6 | |
| GPIO230 | I/O | General-Purpose Input Output 230 | 230 | 50 | 40 | 29 | 25 | 23 |
| GPIO236 | I/O | General-Purpose Input Output 236 | 236 | 49 | 39 | 28 | 24 | 22 |
| GPIO242 | I/O | General-Purpose Input Output 242 | 242 | 20 | 16 | 12 | 8 | 6 |
| GPIO247 | I/O | General-Purpose Input Output 247 | 247 | | 42 | | | |
| GPIO253 | I/O | General-Purpose Input Output 253 | 253 | | 41 | | | |
| I2CA_SCL | I/OD | I2C-A Open-Drain Bidirectional Clock | 1, 4, 8, 9, 18, 20, 27, 33, 37, 43, 57, 65, 70 | 57, 60, 65, 71, 74, 76, 81, 87, 91, 95, 96, 99, 119 | 48, 53, 59, 61, 66, 68, 74, 75, 78, 90 | 33, 38, 44, 46, 50, 54, 58, 59, 62, 75 | 27, 32, 37, 41, 47, 48, 51, 62 | 24, 29, 34, 38, 43, 46, 56 |
| I2CA_SDA | I/OD | I2C-A Open-Drain Bidirectional Data | 0, 5, 10, 19, 21, 26, 32, 35, 42, 56, 66, 79, 230 | 9, 50, 61, 70, 78, 79, 80, 88, 94, 100, 115, 118, 122 | 40, 49, 58, 63, 64, 65, 69, 79, 89, 93 | 29, 34, 43, 48, 49, 51, 57, 63, 74, 76 | 25, 28, 39, 40, 42, 52, 61, 63 | 23, 25, 36, 37, 39, 47, 55 |
| I2CB_SCL | I/OD | I2C-B Open-Drain Bidirectional Clock | 3, 9, 15, 29, 51, 81, 227 | 1, 14, 48, 97, 117, 119, 124 | 10, 38, 76, 90, 95, 100 | 3, 28, 60, 75, 78 | 1, 24, 49, 62 | 2, 22, 44, 56 |
| I2CB_SDA | I/OD | I2C-B Open-Drain Bidirectional Data | 2, 14, 28, 34, 50, 64, 80, 230 | 2, 13, 50, 56, 98, 116, 123, 125 | 1, 9, 40, 77, 94, 96 | 4, 29, 61, 77, 79 | 2, 25, 50 | 3, 23, 45 |
| LINA_RX | I | LIN-A Receive | 9, 11, 13, 15, 19, 23, 29, 33, 35, 41, 42, 47, 49, 55, 59, 63, 67, 69, 70, 75, 226 | 1, 8, 10, 12, 19, 51, 59, 62, 64, 65, 73, 74, 78, 88, 94, 102, 103, 111, 119, 121, 124 | 6, 8, 15, 43, 47, 50, 52, 53, 63, 69, 81, 82, 90, 92, 95, 100 | 3, 11, 32, 35, 37, 38, 48, 51, 57, 65, 66, 75, 78 | 1, 7, 29, 31, 32, 39, 42, 54, 55, 62 | 2, 26, 28, 29, 36, 39, 49, 50, 56 |
| LINA_TX | O | LIN-A Transmit | 10, 12, 14, 18, 22, 24, 28, 32, 37, 40, 44, 46, 54, 58, 64, 68, 73 | 2, 4, 17, 56, 63, 68, 72, 76, 79, 82, 85, 87, 101, 104, 106, 122, 125 | 1, 13, 51, 56, 61, 64, 67, 68, 80, 83, 85, 93, 96 | 4, 6, 36, 41, 46, 49, 50, 64, 67, 69, 76, 79 | 2, 30, 35, 37, 40, 41, 53, 56, 63 | 3, 27, 32, 34, 37, 38, 48, 51 |
| MCANA_RX | I | CAN/CAN FD Receive | 0, 5, 11, 12, 21, 30, 47, 49, 51, 57, 61, 63, 66, 68, 70, 76, 79, 80, 230, 242 | 8, 9, 12, 14, 20, 50, 59, 61, 63, 64, 72, 74, 81, 100, 112, 115, 116, 118, 120, 127 | 6, 8, 10, 16, 40, 47, 49, 51, 52, 66, 79, 89, 91, 98 | 1, 12, 29, 32, 34, 36, 37, 63, 74 | 8, 25, 28, 30, 31, 52, 61 | 6, 23, 25, 27, 28, 47, 55 |
| MCANA_TX | O | CAN/CAN FD Transmit | 1, 4, 7, 13, 17, 20, 31, 46, 48, 50, 56, 60, 62, 65, 67, 72, 74, 77, 81, 224, 228 | 4, 10, 11, 13, 18, 21, 52, 57, 58, 60, 62, 67, 80, 84, 86, 96, 99, 105, 113, 117, 128 | 7, 9, 14, 17, 44, 46, 48, 50, 55, 65, 75, 78, 84, 99 | 2, 6, 10, 13, 31, 33, 35, 40, 59, 62, 68 | 6, 9, 27, 29, 34, 48, 51, 57 | 7, 24, 26, 31, 43, 46, 52 |
| MCANB_RX | I | CAN/CAN FD Receive | 3, 18, 33, 35, 53, 59, 61 | 16, 65, 78, 87, 97, 120, 121 | 12, 53, 63, 68, 76, 91, 92 | 38, 48, 50, 60 | 32, 39, 41, 49 | 29, 36, 38, 44 |
| MCANB_TX | O | CAN/CAN FD Transmit | 2, 19, 32, 37, 58 | 76, 79, 82, 88, 98 | 61, 64, 67, 69, 77 | 46, 49, 51, 61 | 37, 40, 42, 50 | 34, 37, 39, 45 |
| OUTPUTXBAR1 | O | Output X-BAR Output 1 | 2, 24, 34, 58, 73, 78, 227 | 48, 68, 82, 85, 98, 114, 123 | 38, 56, 67, 77, 94 | 28, 41, 61, 77 | 24, 35, 50 | 22, 32, 45 |
| OUTPUTXBAR2 | O | Output X-BAR Output 2 | 3, 25, 37, 54, 59, 76, 242 | 17, 20, 69, 76, 97, 112, 121 | 13, 16, 57, 61, 76, 92 | 12, 42, 46, 60 | 8, 37, 49 | 6, 34, 44 |
| OUTPUTXBAR3 | O | Output X-BAR Output 3 | 4, 5, 14, 26, 48, 55, 60, 62, 77, 224 | 11, 21, 51, 52, 58, 70, 96, 113, 118, 125 | 7, 17, 43, 44, 46, 58, 75, 89, 96 | 13, 31, 43, 59, 74, 79 | 9, 48, 61 | 7, 43, 55 |
| OUTPUTXBAR4 | O | Output X-BAR Output 4 | 6, 15, 27, 33, 49, 61, 63, 70 | 12, 59, 65, 71, 74, 120, 124, 126 | 8, 47, 53, 59, 91, 95, 97 | 32, 38, 44, 78, 80 | 32, 64 | 1, 29 |
| OUTPUTXBAR5 | O | Output X-BAR Output 5 | 7, 28, 42, 64 | 2, 56, 94, 105 | 1, 84 | 4, 57, 68 | 2, 57 | 3, 52 |
| OUTPUTXBAR6 | O | Output X-BAR Output 6 | 9, 29, 43, 81 | 1, 91, 117, 119 | 90, 100 | 3, 54, 75 | 1, 62 | 2, 56 |
| OUTPUTXBAR7 | O | Output X-BAR Output 7 | 0, 11, 16, 30, 44, 69, 71, 80 | 64, 66, 73, 83, 100, 106, 116, 127 | 52, 54, 79, 85, 98 | 1, 37, 39, 63, 69 | 31, 33, 52 | 28, 30, 47 |
| OUTPUTXBAR8 | O | Output X-BAR Output 8 | 17, 31, 45, 72 | 67, 84, 110, 128 | 55, 99 | 2, 40, 73 | 34 | 31 |
| PMBUSA_ALERT | I/OD | PMBus-A Open-Drain Bidirectional Alert Signal | 13, 19, 27, 37, 43, 45, 67 | 10, 62, 71, 76, 88, 91, 110 | 50, 59, 61, 69 | 35, 44, 46, 51, 54, 73 | 29, 37, 42 | 26, 34, 39 |
| PMBUSA_CTL | I/O | PMBus-A Control Signal - Target Input/Controller Output | 12, 18, 26, 35, 42, 44, 68 | 63, 70, 72, 78, 87, 94, 106 | 51, 58, 63, 68, 85 | 36, 43, 48, 50, 57, 69 | 30, 39, 41 | 27, 36, 38 |

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Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|---|--|---|--|---------------------------------------|-------------------------------|----------------------------|
| PMBUSA_SCL | I/OD | PMBus-A Open-Drain Bidirectional Clock | 3, 9, 15, 16, 24, 35, 41, 47, 71, 73, 79, 230 | 8, 50, 66, 68, 78, 83, 85, 97, 103, 115, 119, 124 | 6, 40, 54, 56, 63, 76, 82, 90, 95 | 29, 39, 41, 48, 60, 66, 75, 78 | 25, 33, 35, 39, 49, 55, 62 | 23, 30, 32, 36, 44, 50, 56 |
| PMBUSA_SDA | I/OD | PMBus-A Open-Drain Bidirectional Data | 2, 14, 17, 25, 32, 34, 40, 44, 46, 48, 62, 72 | 4, 11, 58, 67, 69, 79, 84, 98, 101, 106, 123, 125 | 7, 46, 55, 57, 64, 77, 80, 85, 94, 96 | 6, 31, 40, 42, 49, 61, 64, 69, 77, 79 | 34, 40, 50, 53 | 31, 37, 45, 48 |
| SCIA_RX | I | SCI-A Receive Data | 0, 3, 5, 9, 17, 25, 28, 35, 49, 63, 64, 72, 80 | 2, 12, 56, 59, 67, 69, 78, 84, 97, 100, 116, 118, 119 | 1, 8, 47, 55, 57, 63, 76, 79, 89, 90 | 4, 32, 40, 42, 48, 60, 63, 74, 75 | 2, 34, 39, 49, 52, 61, 62 | 3, 31, 36, 44, 47, 55, 56 |
| SCIA_TX | O | SCI-A Transmit Data | 1, 2, 7, 8, 16, 24, 29, 37, 48, 62, 71, 73 | 1, 11, 58, 66, 68, 76, 83, 85, 95, 98, 99, 105 | 7, 46, 54, 56, 61, 74, 77, 78, 84, 100 | 3, 31, 39, 41, 46, 58, 61, 62, 68 | 1, 33, 35, 37, 47, 50, 51, 57 | 2, 30, 32, 34, 45, 46, 52 |
| SCIB_RX | I | SCI-B Receive Data | 11, 13, 15, 19, 23, 41, 57, 67, 69 | 10, 62, 64, 73, 81, 88, 102, 103, 124 | 50, 52, 66, 69, 81, 82, 95 | 35, 37, 51, 65, 66, 78 | 29, 31, 42, 54, 55 | 26, 28, 39, 49, 50 |
| SCIB_TX | O | SCI-B Transmit Data | 9, 10, 12, 14, 18, 22, 40, 56, 68 | 63, 72, 80, 87, 101, 104, 119, 122, 125 | 51, 65, 68, 80, 83, 90, 93, 96 | 36, 50, 64, 67, 75, 76, 79 | 30, 41, 53, 56, 62, 63 | 27, 38, 48, 51, 56 |
| SCIC_RX | I | SCI-C Receive Data | 21, 33, 42, 67, 75, 81, 226 | 10, 19, 61, 65, 94, 111, 117 | 15, 49, 53 | 11, 34, 38, 57 | 7, 28, 32 | 25, 29 |
| SCIC_TX | O | SCI-C Transmit Data | 20, 43, 68, 77, 224 | 21, 60, 72, 91, 113 | 17, 48 | 13, 33, 54 | 9, 27 | 7, 24 |
| SPIA_CLK | I/O | SPI-A Clock | 3, 9, 12, 18, 56, 68, 75, 226 | 19, 63, 72, 80, 87, 97, 111, 119 | 15, 51, 65, 68, 76, 90 | 11, 36, 50, 60, 75 | 7, 30, 41, 49, 62 | 27, 38, 44, 56 |
| SPIA_PICO | I/O | SPI-A Peripheral In, Controller Out (PICO) | 2, 8, 11, 16, 54, 69, 71, 77, 224 | 17, 21, 64, 66, 73, 83, 95, 98, 113 | 13, 17, 52, 54, 74, 77 | 13, 37, 39, 58, 61 | 9, 31, 33, 47, 50 | 7, 28, 30, 45 |
| SPIA_POCI | I/O | SPI-A Peripheral Out, Controller In (POCI) | 1, 4, 10, 13, 17, 35, 55, 67, 72, 74, 228 | 10, 18, 51, 62, 67, 78, 84, 86, 96, 99, 122 | 14, 43, 50, 55, 63, 75, 78, 93 | 10, 35, 40, 48, 59, 62, 76 | 6, 29, 34, 39, 48, 51, 63 | 26, 31, 36, 43, 46 |
| SPIA_PTE | I/O | SPI-A Peripheral Transmit Enable (PTE) | 0, 5, 11, 19, 24, 37, 57, 69, 73, 76, 80, 242 | 20, 64, 68, 73, 76, 81, 85, 88, 100, 112, 116, 118 | 16, 52, 56, 61, 66, 69, 79, 89 | 12, 37, 41, 46, 51, 63, 74 | 8, 31, 35, 37, 42, 52, 61 | 6, 28, 32, 34, 39, 47, 55 |
| SPIB_CLK | I/O | SPI-B Clock | 4, 14, 22, 26, 28, 32, 52, 58, 64, 81 | 2, 15, 56, 70, 79, 82, 96, 104, 117, 125 | 1, 11, 58, 64, 67, 75, 83, 96 | 4, 43, 49, 59, 67, 79 | 2, 40, 48, 56 | 3, 37, 43, 51 |
| SPIB_PICO | I/O | SPI-B Peripheral In, Controller Out (PICO) | 7, 20, 24, 30, 40, 50, 56, 60, 65, 73 | 13, 52, 57, 60, 68, 80, 85, 101, 105, 127 | 9, 44, 48, 56, 65, 80, 84, 98 | 1, 33, 41, 64, 68 | 27, 35, 53, 57 | 24, 32, 48, 52 |
| SPIB_POCI | I/O | SPI-B Peripheral Out, Controller In (POCI) | 6, 16, 21, 25, 31, 41, 51, 57, 61, 66, 71 | 9, 14, 61, 66, 69, 81, 83, 103, 120, 126, 128 | 10, 49, 54, 57, 66, 82, 91, 97, 99 | 2, 34, 39, 42, 66, 80 | 28, 33, 55, 64 | 1, 25, 30, 50 |
| SPIB_PTE | I/O | SPI-B Peripheral Transmit Enable (PTE) | 15, 23, 27, 29, 33, 53, 59, 70 | 1, 16, 65, 71, 74, 102, 121, 124 | 12, 53, 59, 81, 92, 95, 100 | 3, 38, 44, 65, 78 | 1, 32, 54 | 2, 29, 49 |
| SYNCOUT | O | External ePWM Synchronization Pulse | 6, 52 | 15, 126 | 11, 97 | 80 | 64 | 1 |
| TDI | I | JTAG Test Data Input (TDI) - TDI is the default mux selection for the pin. The internal pullup is disabled by default. The internal pullup should be enabled or an external pullup added on the board if this pin is used as JTAG TDI to avoid a floating input. | 35 | 78 | 63 | 48 | 39 | 36 |
| TDO | O | JTAG Test Data Output (TDO) - TDO is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating; the internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. | 37 | 76 | 61 | 46 | 37 | 34 |
| USB0DM | O | USB-0 PHY differential data | 23 | 102 | 81 | 65 | 54 | 49 |
| USB0DP | O | USB-0 PHY differential data | 41 | 103 | 82 | 66 | 55 | 50 |
| X1 | I/O | Crystal oscillator input or single-ended clock input. The device initialization software must configure this pin before the crystal oscillator is enabled. To use this oscillator, a quartz crystal circuit must be connected to X1 and X2. This pin can also be used to feed a single-ended 3.3-V level clock. | 19 | 88 | 69 | 51 | 42 | 39 |
| X2 | I/O | Crystal oscillator output. | 18 | 87 | 68 | 50 | 41 | 38 |

ADVANCE INFORMATION

Table 5-3. Digital Signals (continued)

| SIGNAL NAME | PIN TYPE | DESCRIPTION | GPIO | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|---|------------|------------|--------|--------|--------|--------|
| XCLKOUT | O | External Clock Output. This pin outputs a divided-down version of a chosen clock signal from within the device. | 16, 18, 71 | 66, 83, 87 | 54, 68 | 39, 50 | 33, 41 | 30, 38 |

5.3.3 Power and Ground

Table 5-4. Power and Ground

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|---|----------------|---------------|---------------|---------------|-----------|
| VDD | | 1.2-V Digital Logic Power Pins. TI recommends placing a decoupling capacitor near each VDD pin with a minimum total capacitance of approximately 10 μ F. It is also recommended that all VDD pins be externally connected to each other when internal VREG is used. | 6, 54, 90, 108 | 4, 71, 87 | 8, 53, 71 | 4, 44, 59 | 5, 41, 53 |
| VDDA | | 3.3-V Analog Power Pins. Place a minimum 2.2- μ F decoupling capacitor on each pin. | 41 | 34 | 26 | 22 | 20 |
| VDDIO | | 3.3-V Digital I/O Power Pins. Place a minimum 0.1- μ F decoupling capacitor on each pin. | 5, 55, 89, 109 | 3, 70, 88 | 7, 52, 72 | 43, 60 | 40, 54 |
| VREGENZ | I | Internal voltage regulator enable with internal pulldown. Tie low to VSS to enable internal VREG. Tie high to VDDIO to use an external supply. | 93 | 73 | 56 | 46 | 42 |
| VSS | | Digital Ground | 7, 53, 92, 107 | 5, 45, 72, 86 | 9, 30, 55, 70 | 5, 26, 45, 58 | PAD |
| VSSA | | Analog Ground | 40 | 33 | 25 | 21 | 19 |

5.3.4 Test, JTAG, and Reset

Table 5-5. Test, JTAG, and Reset

| SIGNAL NAME | PIN TYPE | DESCRIPTION | 128 PDT | 100 PZ | 80 PNA | 64 PM | 56 RSH |
|-------------|----------|---|---------|--------|--------|-------|--------|
| TCK | I | JTAG test clock with internal pullup. | 75 | 60 | 45 | 36 | 33 |
| TMS | I/O | JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. This device does not have a TRSTn pin. An external pullup resistor (recommended 2.2 k Ω) on the TMS pin to VDDIO should be placed on the board to keep JTAG in reset during normal operation. | 77 | 62 | 47 | 38 | 35 |
| XRSn | I/OD | Device Reset (in) and Watchdog Reset (out). During a power-on condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the XRSn pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor between 2.2 k Ω and 10 k Ω should be placed between XRSn and VDDIO. If a capacitor is placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to VOL within 512 OSCCLK cycles when the watchdog reset is asserted. This pin is an open-drain output with an internal pullup. If this pin is driven by an external device, it should be done using an open-drain device. | 3 | 2 | 5 | 3 | 4 |

5.4 Pin Multiplexing

5.4.1 GPIO Muxed Pins

Table 5-6. GPIO Muxed Pins

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|-------------|--------------|---------------|--------------|---------------|--------------|--------------|--------------|------------------|------------------|---------------|------------------|------------------|----------|
| GPIO 0 | EPWM1_A | | OUTPUT_XBAR7 | SCIA_RX | I2CA_SDA | SPIA_PTE | FSIRXA_CLK | MCANA_RX | CLB_OUTP_UTXBAR8 | EQEP1_IND_EX | | EPWM3_A | |
| GPIO 1 | EPWM1_B | | | SCIA_TX | I2CA_SCL | SPIA_POCI | EQEP1_STROBE | MCANA_TX | CLB_OUTP_UTXBAR7 | EPWM10_B | | EPWM3_B | |
| GPIO 2 | EPWM2_A | | | OUTPUTXB_AR1 | PMBUSA_SDA | SPIA_PICO | SCIA_TX | FSIRXA_D1 | I2CB_SDA | EPWM10_A | MCANB_TX | EPWM4_A | |
| GPIO 3 | EPWM2_B | OUTPUTXB_AR2 | | OUTPUTXB_AR2 | PMBUSA_SCL | SPIA_CLK | SCIA_RX | FSIRXA_D0 | I2CB_SCL | | MCANB_RX | EPWM4_B | |
| GPIO 4 | EPWM3_A | I2CA_SCL | MCANA_TX | OUTPUTXB_AR3 | | SPIB_CLK | EQEP2_STROBE | FSIRXA_CLK | CLB_OUTP_UTXBAR6 | EPWM11_B | SPIA_POCI | EPWM1_A | |
| GPIO 5 | EPWM3_B | I2CA_SDA | OUTPUT_XBAR3 | MCANA_RX | | SPIA_PTE | FSITXA_D1 | CLB_OUTP_UTXBAR5 | SCIA_RX | | | EPWM1_B | |
| GPIO 6 | EPWM4_A | OUTPUTXB_AR4 | SYNCOU_T | EQEP1_A | | SPIB_POCI | FSITXA_D0 | | FSITXA_D1 | | CLB_OUTP_UTXBAR8 | EPWM2_A | |
| GPIO 7 | EPWM4_B | EPWM2_A | OUTPUT_XBAR5 | EQEP1_B | | SPIB_PICO | FSITXA_CLK | CLB_OUTP_UTXBAR2 | SCIA_TX | | MCANA_TX | EPWM2_B | |
| GPIO 8 | EPWM5_A | | ADCSOC_AO | EQEP1_STR_OBE | SCIA_TX | SPIA_PICO | I2CA_SCL | FSITXA_D1 | CLB_OUTP_UTXBAR5 | EPWM11_A | | | |
| GPIO 9 | EPWM5_B | SCIB_TX | OUTPUT_XBAR6 | EQEP1_IND_EX | SCIA_RX | SPIA_CLK | I2CA_SCL | FSITXA_D0 | LINA_RX | PMBUSA_SCL | I2CB_SCL | EQEP3_B | |
| GPIO 10 | EPWM6_A | | ADCSOC_BO | EQEP1_A | SCIB_TX | SPIA_POCI | I2CA_SDA | FSITXA_CLK | LINA_TX | EQEP3_STR_OBE | | CLB_OUTP_UTXBAR4 | |
| GPIO 11 | EPWM6_B | MCANA_RX | OUTPUT_XBAR7 | EQEP1_B | SCIB_RX | SPIA_PTE | FSIRXA_D1 | LINA_RX | EQEP2_A | SPIA_PICO | | EQEP3_IND_EX | |
| GPIO 12 | EPWM7_A | | MCANA_RX | EQEP1_STR_OBE | SCIB_TX | PMBUSA_CTL | FSIRXA_D0 | LINA_TX | SPIA_CLK | | | | |
| GPIO 13 | EPWM7_B | | MCANA_TX | EQEP1_IND_EX | SCIB_RX | PMBUSA_ALERT | FSIRXA_CLK | LINA_RX | SPIA_POCI | | | | |
| GPIO 14 | EPWM8_A | SCIB_TX | | I2CB_SDA | OUTPUT_XBAR3 | PMBUSA_SDA | SPIB_CLK | EQEP2_A | LINA_TX | EPWM3_A | CLB_OUTP_UTXBAR7 | | |
| GPIO 15 | EPWM8_B | SCIB_RX | | I2CB_SCL | OUTPUT_XBAR4 | PMBUSA_SCL | SPIB_PTE | EQEP2_B | LINA_RX | EPWM3_B | CLB_OUTP_UTXBAR6 | | |
| GPIO 16 | SPIA_PICO | | OUTPUT_XBAR7 | EPWM9_A | SCIA_TX | | EQEP1_STROBE | PMBUSA_SCL | XCLKOUT | EQEP2_B | SPIB_POCI | EQEP3_STR_OBE | |
| GPIO 17 | SPIA_POCI | | OUTPUT_XBAR8 | EPWM9_B | SCIA_RX | | EQEP1_INDEX | PMBUSA_SDA | MCANA_TX | | EPWM6_A | | |
| GPIO 18 | SPIA_CLK | SCIB_TX | MCANB_RX | EPWM6_A | I2CA_SCL | | EQEP2_A | PMBUSA_CTL | XCLKOUT | LINA_TX | | EQEP3_IND_EX | X2 |
| GPIO 19 | SPIA_PTE | SCIB_RX | MCANB_TX | EPWM6_B | I2CA_SDA | | EQEP2_B | PMBUSA_ALERT | CLB_OUTP_UTXBAR1 | LINA_RX | | | X1 |
| GPIO 20 | EQEP1_A | | | EPWM12_A | SPIB_PICO | | MCANA_TX | ADCE_EXT_MUXSEL0 | I2CA_SCL | | | SCIC_TX | |
| GPIO 21 | EQEP1_B | | | EPWM12_B | SPIB_POCI | | MCANA_RX | ADCE_EXT_MUXSEL1 | I2CA_SDA | | | SCIC_RX | |
| GPIO 22 | EQEP1_STROBE | | SCIB_TX | | SPIB_CLK | | LINA_TX | CLB_OUTP_UTXBAR1 | LINA_TX | | EPWM4_A | EQEP3_A | |
| GPIO 23 | EQEP1_INDEX | | SCIB_RX | | SPIB_PTE | | LINA_RX | CLB_OUTP_UTXBAR3 | LINA_RX | EPWM12_A | EPWM4_B | | USB0_DM |
| GPIO 24 | OUTPUT_XBAR1 | EQEP2_A | SPIA_PTE | EPWM8_A | SPIB_PICO | | LINA_TX | PMBUSA_SCL | SCIA_TX | ERRORSTS | EPWM9_A | | |
| GPIO 25 | OUTPUT_XBAR2 | EQEP2_B | | EQEP1_A | SPIB_POCI | | FSITXA_D1 | PMBUSA_SDA | SCIA_RX | EQEP3_A | | | |
| GPIO 26 | OUTPUT_XBAR3 | EQEP2_IND_EX | | OUTPUTXB_AR3 | SPIB_CLK | | FSITXA_D0 | PMBUSA_CTL | I2CA_SDA | EQEP3_B | | | |
| GPIO 27 | OUTPUT_XBAR4 | EQEP2_STR_OBE | | OUTPUTXB_AR4 | SPIB_PTE | | FSITXA_CLK | PMBUSA_ALERT | I2CA_SCL | EQEP3_STR_OBE | | | |
| GPIO 28 | SCIA_RX | | EPWM7_A | OUTPUTXB_AR5 | EQEP1_A | | EQEP2_STROBE | LINA_TX | SPIB_CLK | ERRORSTS | I2CB_SDA | | |
| GPIO 29 | SCIA_TX | | EPWM7_B | OUTPUTXB_AR6 | EQEP1_B | | EQEP2_INDEX | LINA_RX | SPIB_PTE | ERRORSTS | I2CB_SCL | | AUXCLKIN |
| GPIO 30 | | | SPIB_PICO | OUTPUTXB_AR7 | EQEP1_STROBE | | FSIRXA_CLK | MCANA_RX | EPWM1_A | EQEP3_IND_EX | | | |

Table 5-6. GPIO Muxed Pins (continued)

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|-------------|---------------|------------------|--------------|------------------|--------------|------------------|---------------|------------------|------------------|----------|------------------|---------------|---------|
| GPIO 31 | | | SPIB_PO CI | OUTPUTXB AR8 | EQEP1_I NDEX | | FSIRXA_D1 | MCANA_TX | EPWM1_B | | | | |
| GPIO 32 | I2CA_SD A | EQEP1_IND EX | SPIB_CL K | EPWM8_B | LINA_TX | | FSIRXA_D0 | MCANB_TX | PMBUSA_S DA | ADCSOCBO | | | |
| GPIO 33 | I2CA_SCL | | SPIB_PT E | OUTPUTXB AR4 | LINA_RX | | FSIRXA_CLK | MCANB_RX | EQEP2_B | ADCSOCAO | | SCIC_RX | |
| GPIO 34 | OUTPUTX BAR1 | | | | PMBUSA_SDA | | | | | | I2CB_SDA | | |
| GPIO 35 | SCIA_RX | SPIA_PO CI | I2CA_SD A | MCANB_RX | PMBUSA_SCL | LINA_RX | EQEP1_A | PMBUSA_C TL | EPWM5_B | | | TDI | |
| GPIO 37 | OUTPUTX BAR2 | SPIA_PTE | I2CA_SC L | SCIA_TX | MCANB_T X | LINA_TX | EQEP1_B | PMBUSA_A LERT | EPWM5_A | | | TDO | |
| GPIO 40 | SPIB_PIC O | | | EPWM2_B | PMBUSA_SDA | FSIRXA_D0 | SCIB_TX | EQEP1_A | LINA_TX | | CLB_OUTP UTXBAR4 | EQEP3_STR OBE | |
| GPIO 41 | EPWM7_A | | | EPWM2_A | PMBUSA_SCL | FSIRXA_D1 | SCIB_RX | EQEP1_B | LINA_RX | EPWM12_B | SPIB_PO CI | | USB0 DP |
| GPIO 42 | | LINA_RX | OUTPUT XBAR5 | PMBUSA_C TL | I2CA_SD A | SCIC_RX | | EQEP1_STR OBE | CLB_OUTP UTXBAR3 | | | | |
| GPIO 43 | | | OUTPUT XBAR6 | PMBUSA_A LERT | I2CA_SCL | SCIC_TX | PMBUSA_ALERT | EQEP1_IND EX | CLB_OUTP UTXBAR4 | | | | |
| GPIO 44 | | | OUTPUT XBAR7 | EQEP1_A | PMBUSA_SDA | FSITXA_CL K | PMBUSA_CTL | CLB_OUTP UTXBAR3 | FSIRXA_D0 | | LINA_TX | | |
| GPIO 45 | | | OUTPUT XBAR8 | | | FSITXA_D0 | PMBUSA_ALERT | CLB_OUTP UTXBAR4 | | | | | |
| GPIO 46 | | | LINA_TX | MCANA_TX | | FSITXA_D1 | PMBUSA_SDA | | | | | | |
| GPIO 47 | | | LINA_RX | MCANA_RX | | CLB_OUTP UTXBAR2 | PMBUSA_SCL | | | | | | |
| GPIO 48 | OUTPUTX BAR3 | | | MCANA_TX | SCIA_TX | | PMBUSA_SDA | | | | | | |
| GPIO 49 | OUTPUTX BAR4 | | | MCANA_RX | SCIA_RX | | LINA_RX | | | | FSITXA_D0 | | |
| GPIO 50 | EQEP1_A | | | MCANA_TX | SPIB_PIC O | | I2CB_SD A | | | | FSITXA_D1 | | |
| GPIO 51 | EQEP1_B | | | MCANA_RX | SPIB_PO CI | | I2CB_SCL | | | | FSITXA_CL K | | |
| GPIO 52 | EQEP1_S TROBE | | | CLB_OUTP UTXBAR5 | SPIB_CLK | | SYNCOU T | | | | FSIRXA_D0 | | |
| GPIO 53 | EQEP1_I NDEX | | | CLB_OUTP UTXBAR6 | SPIB_PTE | | ADCSOC AO | MCANB_RX | | | FSIRXA_D1 | | |
| GPIO 54 | SPIA_PIC O | | | EQEP2_A | OUTPUTX BAR2 | | ADCSOC BO | LINA_TX | | | FSIRXA_CL K | | |
| GPIO 55 | SPIA_PO CI | | | EQEP2_B | OUTPUTX BAR3 | | ERRORS TS | LINA_RX | | | | | |
| GPIO 56 | SPIA_CLK | CLB_OUTP UTXBAR7 | MCANA_TX | EQEP2_STR OBE | SCIB_TX | | SPIB_PIC O | I2CA_SDA | EQEP1_A | | FSIRXA_D1 | | |
| GPIO 57 | SPIA_PTE | CLB_OUTP UTXBAR8 | MCANA_RX | EQEP2_IND EX | SCIB_RX | | SPIB_PO CI | I2CA_SCL | EQEP1_B | | FSIRXA_CL K | | |
| GPIO 58 | | | | OUTPUTXB AR1 | SPIB_CLK | | LINA_TX | MCANB_TX | EQEP1_STR OBE | | FSIRXA_D0 | | |
| GPIO 59 | | | | OUTPUTXB AR2 | SPIB_PTE | | LINA_RX | MCANB_RX | EQEP1_IND EX | | | | |
| GPIO 60 | EPWM12_B | | MCANA_TX | OUTPUTXB AR3 | SPIB_PIC O | | | | | | | | |
| GPIO 61 | | | MCANA_RX | OUTPUTXB AR4 | SPIB_PO CI | | | | | | MCANB_RX | | |
| GPIO 62 | EPWM10_A | OUTPUTXB AR3 | | MCANA_TX | SCIA_TX | | PMBUSA_SDA | | | | | | |
| GPIO 63 | EPWM10_B | OUTPUTXB AR4 | | MCANA_RX | SCIA_RX | | LINA_RX | | | | | | |
| GPIO 64 | SCIA_RX | EPWM11_A | EPWM7_A | OUTPUTXB AR5 | EQEP1_A | | EQEP2_S TROBE | LINA_TX | SPIB_CLK | ERRORSTS | I2CB_SDA | | |
| GPIO 65 | EQEP1_A | EPWM11_B | | | SPIB_PIC O | | MCANA_T X | | | I2CA_SCL | | | |
| GPIO 66 | EQEP1_B | EPWM12_A | | | SPIB_PO CI | | MCANA_RX | | | I2CA_SDA | | | |

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Table 5-6. GPIO Muxed Pins (continued)

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|-------------|-------------|--------------|--------------|---------------|-----------|---------------|--------------|------------|------------------|------------------|-----------|---------------|-----|
| GPIO 67 | EPWM7_B | EPWM12_B | MCANA_TX | EQEP1_IND_EX | SCIB_RX | PMBUSA_A_LERT | FSIRXA_CLK | LINA_RX | SPIA_POCI | | | SCIC_RX | |
| GPIO 68 | EPWM7_A | EPWM3_A | MCANA_RX | EQEP1_STR_OBE | SCIB_TX | PMBUSA_C_TL | FSIRXA_D0 | LINA_TX | SPIA_CLK | | | SCIC_TX | |
| GPIO 69 | EPWM6_B | EPWM3_B | OUTPUT_XBAR7 | EQEP1_B | SCIB_RX | SPIA_PTE | FSIRXA_D1 | LINA_RX | EQEP2_A | SPIA_PICO | | EQEP3_IND_EX | |
| GPIO 70 | I2CA_SCL | | SPIB_PTE | OUTPUTXB_AR4 | LINA_RX | | FSIRXA_CLK | MCANA_RX | EQEP2_B | ADCSOAO | | EQEP3_A | |
| GPIO 71 | SPIA_PICO | EPWM4_B | OUTPUT_XBAR7 | EPWM9_A | SCIA_TX | | EQEP1_STROBE | PMBUSA_SCL | XCLKOUT | EQEP2_IND_EX | SPIB_POCI | EQEP3_STR_OBE | |
| GPIO 72 | SPIA_POCI | EPWM5_A | OUTPUT_XBAR8 | EPWM9_B | SCIA_RX | | EQEP1_INDEX | PMBUSA_SDA | MCANA_TX | | EPWM6_A | EQEP3_B | |
| GPIO 73 | OUTPUTXBAR1 | EPWM5_B | SPIA_PTE | EPWM8_A | SPIB_PICO | | LINA_TX | PMBUSA_SCL | SCIA_TX | ERRORSTS | EPWM9_A | | |
| GPIO 74 | EPWM2_B | | ADCSOAO | MCANA_TX | SPIA_POCI | | | | EQEP1_B | | | | |
| GPIO 75 | EPWM1_B | | LINA_RX | EPWM6_A | SPIA_CLK | | | | EQEP1_STR_OBE | | SCIC_RX | | |
| GPIO 76 | EPWM4_A | | | OUTPUTXB_AR2 | SPIA_PTE | | | MCANA_RX | EQEP1_IND_EX | | | | |
| GPIO 77 | EPWM1_A | | | OUTPUTXB_AR3 | SPIA_PICO | | | MCANA_TX | EQEP1_A | | SCIC_TX | | |
| GPIO 78 | | EPWM8_A | EPWM3_A | OUTPUTXB_AR1 | EPWM2_B | | FSITXA_CLK | | | | | | |
| GPIO 79 | | EPWM8_B | EPWM3_B | MCANA_RX | EPWM2_A | I2CA_SDA | PMBUSA_SCL | | | | | | |
| GPIO 80 | EPWM1_A | | OUTPUT_XBAR7 | SCIA_RX | I2CB_SDA | SPIA_PTE | FSITXA_D0 | MCANA_RX | CLB_OUTP_UTXBAR8 | EQEP1_IND_EX | | EPWM3_A | |
| GPIO 81 | EPWM1_B | OUTPUTXB_AR6 | SCIC_RX | SPIB_CLK | I2CB_SCL | | FSITXA_D1 | MCANA_TX | EQEP3_IND_EX | | | | |
| GPIO 211 | EPWM10_A | | | EQEP3_A | | | | | | | | | |
| GPIO 212 | EPWM10_B | | | EQEP3_B | | | | | | | | | |
| GPIO 213 | EPWM11_A | | | EQEP3_STR_OBE | | | | | | | | | |
| GPIO 214 | EPWM11_B | | | EQEP3_IND_EX | | | | | | | | | |
| GPIO 215 | EPWM7_B | | | EQEP2_A | | | | | | | | | |
| GPIO 224 | EPWM11_B | | | OUTPUTXB_AR3 | SPIA_PICO | | EPWM1_A | MCANA_TX | EQEP1_A | ADCE_EXT_MUXSEL3 | SCIC_TX | | |
| GPIO 226 | EPWM10_B | | LINA_RX | EPWM6_A | SPIA_CLK | | EPWM1_B | | EQEP1_STR_OBE | ADCE_EXT_MUXSEL1 | SCIC_RX | | |
| GPIO 227 | I2CB_SCL | | EPWM3_A | OUTPUTXB_AR1 | EPWM2_B | | | | | | | | |
| GPIO 228 | EPWM10_A | | ADCSOAO | MCANA_TX | SPIA_POCI | | EPWM2_B | | EQEP1_B | ADCE_EXT_MUXSEL0 | | | |
| GPIO 230 | I2CB_SDA | | EPWM3_B | MCANA_RX | EPWM2_A | I2CA_SDA | PMBUSA_SCL | | | | | | |
| GPIO 236 | EPWM7_A | | | EQEP1_IND_EX | | | EPWM12_A | | | | | | |
| GPIO 242 | EPWM11_A | | | OUTPUTXB_AR2 | SPIA_PTE | | EPWM4_A | MCANA_RX | EQEP1_IND_EX | ADCE_EXT_MUXSEL2 | | | |
| GPIO 247 | EPWM12_B | | | | | | | | | | | | |
| GPIO 253 | EPWM12_A | | | | | | | | | | | | |
| AIO208 | | | | | | | | | | | | | |
| AIO209 | | | | | | | | | | | | | |
| AIO210 | | | | | | | | | | | | | |
| AIO225 | | | | | | | | | | | | | |

Table 5-6. GPIO Muxed Pins (continued)

| 0, 4, 8, 12 | 1 | 2 | 3 | 5 | 6 | 7 | 9 | 10 | 11 | 13 | 14 | 15 | ALT |
|----------------|---|---|---|---|---|---|---|----|----|----|----|----|-----|
| AIO22 9 | | | | | | | | | | | | | |
| AIO23 1 | | | | | | | | | | | | | |
| AIO23 2 | | | | | | | | | | | | | |
| AIO23 3 | | | | | | | | | | | | | |
| AIO23 4 | | | | | | | | | | | | | |
| AIO23 5 | | | | | | | | | | | | | |
| AIO23 7 | | | | | | | | | | | | | |
| AIO23 8 | | | | | | | | | | | | | |
| AIO23 9 | | | | | | | | | | | | | |
| AIO24 0 | | | | | | | | | | | | | |
| AIO24 1 | | | | | | | | | | | | | |
| AIO24 4 | | | | | | | | | | | | | |
| AIO24 5 | | | | | | | | | | | | | |
| AIO24 8 | | | | | | | | | | | | | |
| AIO24 9 | | | | | | | | | | | | | |
| AIO25 1 | | | | | | | | | | | | | |
| AIO25 2 | | | | | | | | | | | | | |

5.4.2 Digital Inputs on ADC Pins (AIOs)

Some GPIOs are multiplexed with analog pins and only have digital input functionality. These are also referred to as AIOs. Pins with only an AIO option on this port can only function in input mode. See the device data sheet for list of AIO signals. By default, these pins function as analog pins and the GPIOs are in a high-impedance state. The GPyAMSEL register is used to configure these pins for digital or analog operation.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AIOs, cross-talk can occur with adjacent analog signals. Therefore, limit the edge rate of signals connected to AIOs if adjacent channels are being used for analog functions.

5.4.3 Digital Inputs and Outputs on ADC Pins (AGPIOs)

Some GPIOs are multiplexed with analog pins and have digital input and output functionality. These are also referred to as AGPIOs. Unlike AIOs, AGPIOs have full input and output capability.

By default, the AGPIOs are not connected and must be configured. [Table 5-7](#) shows how to configure the AGPIOs. To enable the analog functionality, set the register AGPICTRLx from analog subsystem. To enable the digital functionality, set the register GPxAMSEL from the *General-Purpose Input/Output (GPIO)* chapter.

Table 5-7. AGPIO Configuration

| AGPICTRLx.GPIOy (Default = 0) | GPxAMSEL.GPIOy (Default = 1) | Pin Connected To: | |
|----------------------------------|---------------------------------|-------------------|------------------|
| | | ADC | GPIOy |
| 0 | 0 | - | Yes |
| 0 | 1 | - ⁽¹⁾ | - ⁽¹⁾ |
| 1 | 0 | - | Yes |
| 1 | 1 | Yes | - |

(1) By default there are no signals connected to AGPIO pins. One of the other rows in the table must be chosen for pin functionality.

Note

If digital signals with sharp edges (high dv/dt) are connected to the AGPIOs, cross-talk can occur with adjacent analog signals. The user must therefore limit the edge rate of signals connected to AGPIOs, if adjacent channels are being used for analog functions.

5.4.4 GPIO Input X-BAR

The Input X-BAR is used to route signals from a GPIO to many different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts (see the *Input X-BAR* figure). The *Input X-BAR Destinations* table lists the input X-BAR destinations. For details on configuring the Input X-BAR, see the Crossbar (X-BAR) chapter of the *TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual*.

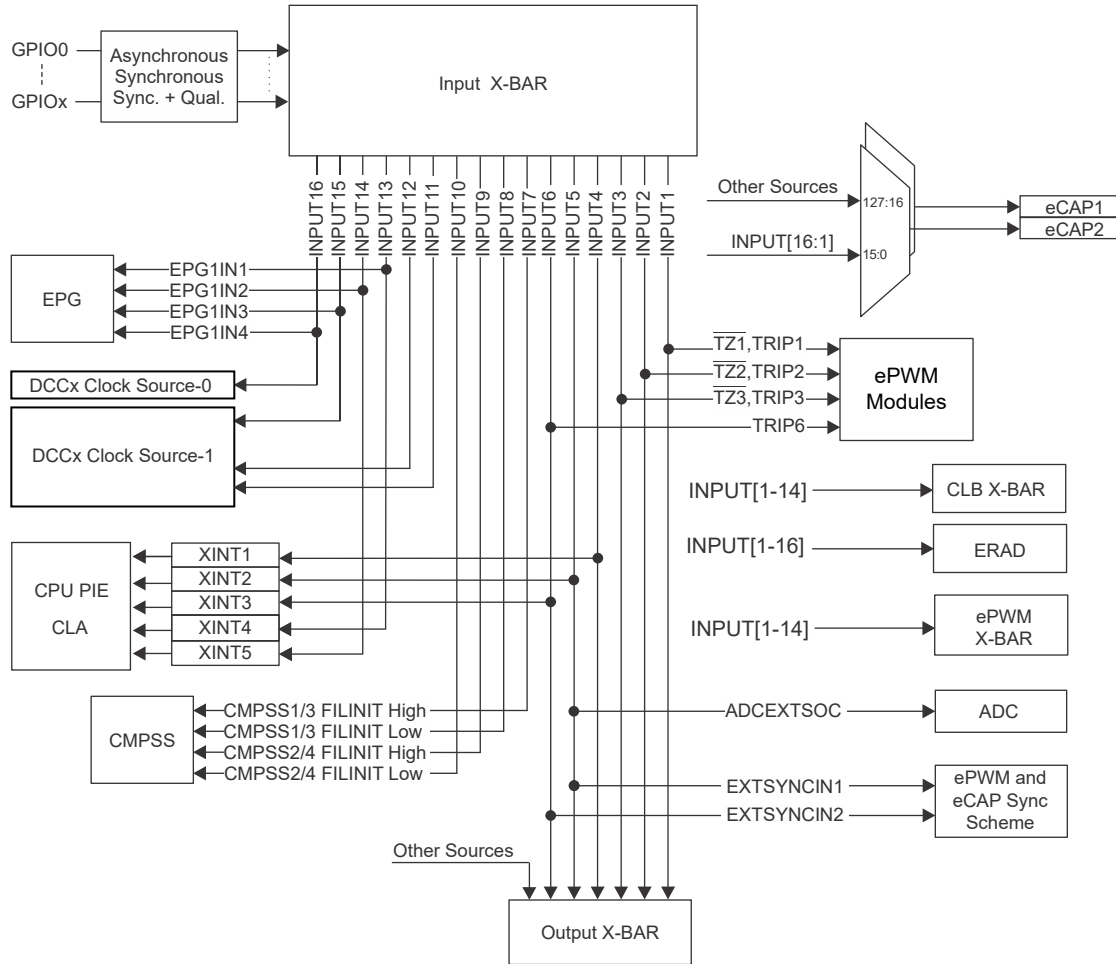


Figure 5-6. Input X-BAR

Table 5-8. Input X-BAR Destinations

| Input | ECAP | EPWM XBAR | CLB XBAR | OUTPUT XBAR | EPWM TRIP | ERAD | CPU XINT | ADC SOC | EPWM / ECAP SYNC | CMPSS | DCCx | EPG |
|------------|------|-----------|----------|-------------|------------|------|----------|-----------|------------------|-------|------|-----|
| INPUTXBAR1 | Yes | Yes | Yes | Yes | TZ1, TRIP1 | Yes | | | | | | |
| INPUTXBAR2 | Yes | Yes | Yes | Yes | TZ2, TRIP2 | Yes | | | | | | |
| INPUTXBAR3 | Yes | Yes | Yes | Yes | TZ3, TRIP3 | Yes | | | | | | |
| INPUTXBAR4 | Yes | Yes | Yes | Yes | | Yes | XINT1 | | | | | |
| INPUTXBAR5 | Yes | Yes | Yes | Yes | | Yes | XINT2 | ADCEXTSOC | EXTSYNCIN1 | | | |
| INPUTXBAR6 | Yes | Yes | Yes | Yes | TRIP6 | Yes | XINT3 | | EXTSYNCIN2 | | | |

Table 5-8. Input X-BAR Destinations (continued)

| Input | ECAP | EPWM XBAR | CLB XBAR | OUTPUT XBAR | EPWM TRIP | ERAD | CPU XINT | ADC SOC | EPWM / ECAP SYNC | CMPSS | DCCx | EPG |
|-------------|------|-----------|----------|-------------|-----------|------|----------|---------|------------------|----------------------------|------|---------|
| INPUTXBAR7 | Yes | Yes | Yes | | | Yes | | | | CMPSS1/3 EXT_FILTER_N_H | | |
| INPUTXBAR8 | Yes | Yes | Yes | | | Yes | | | | CMPSS1/3 EXT_FILTER_N_L | | |
| INPUTXBAR9 | Yes | Yes | Yes | | | Yes | | | | CMPSS2/4 EXT_FILTER_N_H | | |
| INPUTXBAR10 | Yes | Yes | Yes | | | Yes | | | | CMPSS2/4 EXT_FILTER_N_L | | |
| INPUTXBAR11 | Yes | Yes | Yes | | | Yes | | | | | CLK1 | |
| INPUTXBAR12 | Yes | Yes | Yes | | | Yes | | | | | CLK1 | |
| INPUTXBAR13 | Yes | Yes | Yes | | | Yes | XINT4 | | | | | EPGAIN1 |
| INPUTXBAR14 | Yes | Yes | Yes | | | Yes | XINT5 | | | | | EPGAIN2 |
| INPUTXBAR15 | Yes | | | | | Yes | | | | | CLK1 | EPGAIN3 |
| INPUTXBAR16 | Yes | | | | | Yes | | | | | CLK0 | EPGAIN4 |

ADVANCE INFORMATION

5.4.5 GPIO Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR

The Output X-BAR has eight outputs that can be selected on the GPIO mux as OUTPUTXBARx. The CLB X-BAR has eight outputs that are connected to the CLB global mux as AUXSIGx. The CLB Output X-BAR has eight outputs that can be selected on the GPIO mux as CLB_OUTPUTXBARx. The ePWM X-BAR has eight outputs that are connected to the TRIPx inputs of the ePWM. The sources for the Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR are shown in [Figure 5-7](#). For details on the Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR, see the Crossbar (X-BAR) chapter of the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#).

ADVANCE INFORMATION

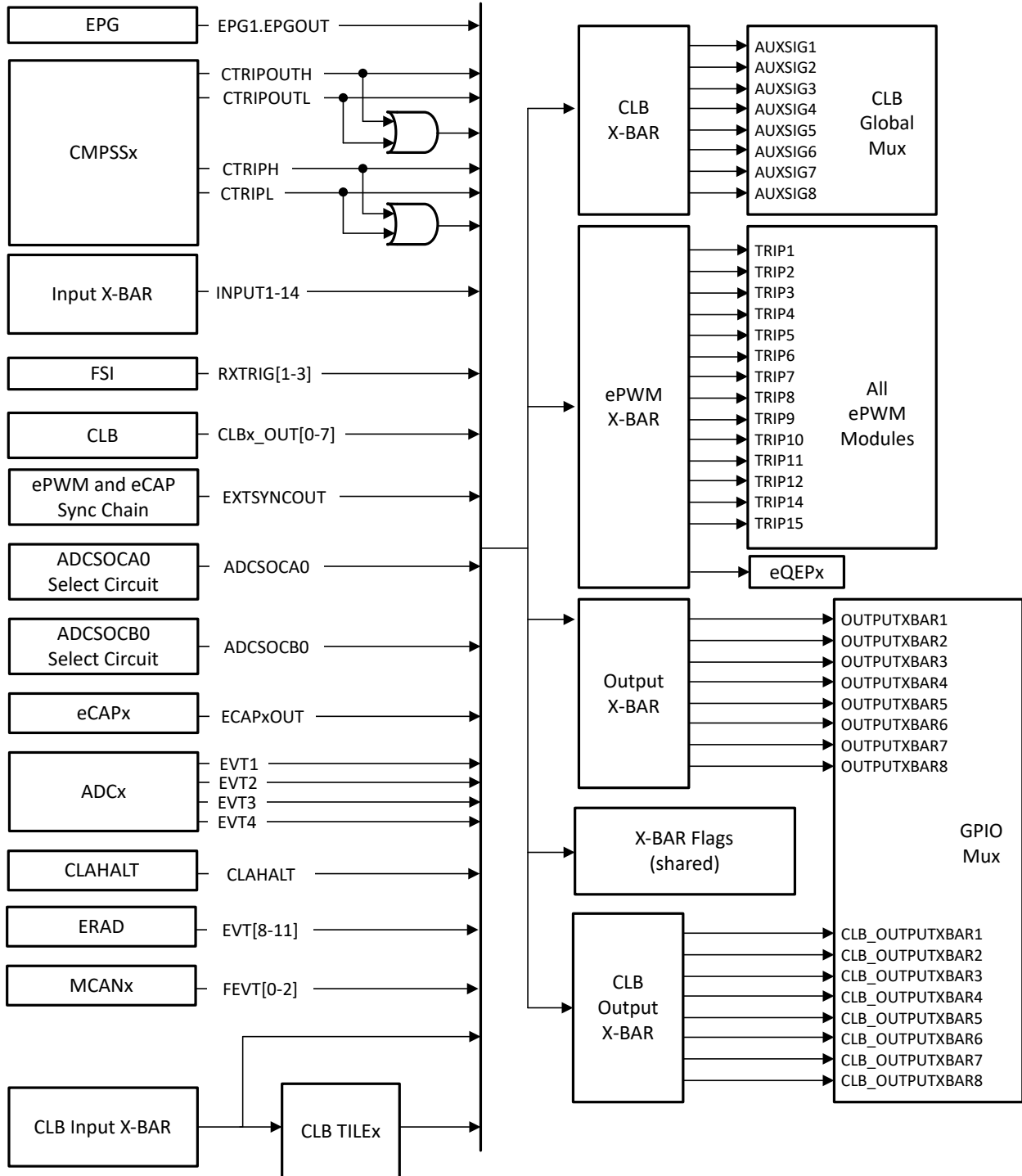


Figure 5-7. Output X-BAR, CLB X-BAR, CLB Output X-BAR, and ePWM X-BAR Sources

5.5 Pins With Internal Pullup and Pulldown

Some pins on the device have internal pullups or pulldowns. [Table 5-9](#) lists the pull direction and when it is active. The pullups on GPIO pins are disabled by default and can be enabled through software. To avoid any floating unbonded inputs, the Boot ROM will enable internal pullups on GPIO pins that are not bonded out in a particular package. Other pins noted in [Table 5-9](#) with pullups and pulldowns are always on and cannot be disabled.

Table 5-9. Pins With Internal Pullup and Pulldown

| PIN | RESET (XRSn = 0) | DEVICE BOOT | APPLICATION |
|-----------------------------|-------------------------------|--------------------------------|---------------------|
| GPIOx | Pullup disabled | Pullup disabled ⁽¹⁾ | Application defined |
| GPIO35/TDI | Pullup disabled | | Application defined |
| GPIO37/TDO | Pullup disabled | | Application defined |
| TCK | Pullup active | | |
| TMS | Pullup active | | |
| XRSn | Pullup active | | |
| Other pins (including AIOs) | No pullup or pulldown present | | |

(1) Pins not bonded out in a given package will have the internal pullups enabled by the Boot ROM.

5.6 Connections for Unused Pins

For applications that do not need to use all functions of the device, [Table 5-10](#) lists acceptable conditioning for any unused pins. When multiple options are listed in [Table 5-10](#), any option is acceptable. Pins not listed in [Table 5-10](#) must be connected according to [Section 5](#).

Table 5-10. Connections for Unused Pins

| SIGNAL NAME | ACCEPTABLE PRACTICE |
|--|--|
| ANALOG | |
| VREFHI | Tie to VDDA (applies only if ADC is not used in the application) |
| VREFLO | Tie to VSSA |
| Analog input pins with DACx_OUT | <ul style="list-style-type: none"> No Connect Tie to VSSA through 4.7-kΩ or larger resistor |
| Analog input pins (except DACx_OUT) | <ul style="list-style-type: none"> No Connect Tie to VSSA Tie to VSSA through resistor |
| Analog input pins (shared with GPIOs) ⁽¹⁾ | <ul style="list-style-type: none"> No connection (digital input mode with internal pullup enabled) No connection (digital output mode with internal pullup disabled) Pullup or pulldown resistor (any value resistor, digital input mode, and with internal pullup disabled) |
| DIGITAL | |
| GPIOx | <ul style="list-style-type: none"> No connection (input mode with internal pullup enabled) No connection (output mode with internal pullup disabled) Pullup or pulldown resistor (any value resistor, input mode, and with internal pullup disabled) |
| GPIO35/TDI | When TDI mux option is selected (default), the GPIO is in Input mode. <ul style="list-style-type: none"> Internal pullup enabled External pullup resistor |
| GPIO37/TDO | When TDO mux option is selected (default), the GPIO is in Output mode only during JTAG activity; otherwise, it is in a tri-state condition. The pin must be biased to avoid extra current on the input buffer. <ul style="list-style-type: none"> Internal pullup enabled External pullup resistor |
| TCK | <ul style="list-style-type: none"> No Connect Pullup resistor |
| TMS | Pullup resistor |
| GPIO19/X1 | Turn XTAL off and: <ul style="list-style-type: none"> Input mode with internal pullup enabled Input mode with external pullup or pulldown resistor Output mode with internal pullup disabled |
| GPIO18/X2 | Turn XTAL off and: <ul style="list-style-type: none"> Input mode with internal pullup enabled Input mode with external pullup or pulldown resistor Output mode with internal pullup disabled |

Table 5-10. Connections for Unused Pins (continued)

| SIGNAL NAME | ACCEPTABLE PRACTICE |
|-------------------------|---|
| POWER AND GROUND | |
| VDD | All VDD pins must be connected per Section 5.3 . Pins should not be used to bias any external circuits. |
| VDDA | If a dedicated analog supply is not used, tie to VDDIO. |
| VDDIO | All VDDIO pins must be connected per Section 5.3 . |
| VSS | All VSS pins must be connected to board ground. |
| VSSA | If an analog ground is not used, tie to VSS. |

- (1) AGPIO pins share analog and digital functionality. The actions here only apply if these pins are also not being used for analog functions.

6 Specifications

6.1 Absolute Maximum Ratings

over recommended operating conditions (unless otherwise noted)^{(1) (2)}

| | | MIN | MAX | UNIT |
|---|--|------|-----|------|
| Supply voltage | VDD with respect to VSS | -0.3 | 1.5 | V |
| | VDDIO with respect to VSS | -0.3 | 4.6 | |
| | VDDA with respect to VSSA | -0.3 | 4.6 | |
| Input voltage ⁽⁷⁾ | V _{IN} (3.3 V) | -0.3 | 4.6 | V |
| | V _{IN} (5.0 V) ⁽⁵⁾ | -0.3 | 6.0 | V |
| Output voltage | V _O | -0.3 | 4.6 | V |
| Input clamp current - per pin ^{(4) (6)} | I _{IK} - V _{IN} < VSS/VSSA - V _{IN} > VDDIO/VDDA | -20 | 20 | mA |
| Input clamp current - per pin: GPIO2/3/9/32 | I _{IK} - V _{IN} < VSS | -20 | | mA |
| Input clamp current - total for all inputs ^{(4) (6)} | I _{IKTOTAL} - V _{IN} < VSS/VSSA - V _{IN} > VDDIO/VDDA | -20 | 20 | mA |
| Output current | Digital output (per pin), I _{OUT} | -20 | 20 | mA |
| Operating junction temperature | T _J | -40 | 155 | °C |
| Storage temperature ⁽³⁾ | T _{stg} | -65 | 150 | °C |

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values are with respect to VSS, unless otherwise noted.
- (3) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see the [Semiconductor and IC Package Thermal Metrics Application Report](#).
- (4) Continuous clamp current per pin is ±2mA
- (5) GPIO2, GPIO3, GPIO9, GPIO32 Only
- (6) Applying a V_{IN} greater than VDDIO/VDDA or less than VSS/VSSA will turn on the ESD current clamping diode causing additional current flow to the respective supply rail. If this occurs, the current must be kept within the MIN/MAX listed to prevent permanent damage to the device.
- (7) Input clamp current must also be observed.

6.2 ESD Ratings – Commercial

| | | | VALUE | UNIT | |
|---|-------------------------|---|---|------|------|
| All F28P550Sxx devices in 128-pin PDT package | | | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 128-pin PDT: 1, 32, 33, 64, 65, 96, 97, 128 | | ±750 |
| All F28P550Sxx devices in 100-pin PZ package | | | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 100-pin PZ: 1, 25, 26, 50, 51, 75, 76, 100 | | ±750 |
| All F28P550Sxx devices in 80-pin PNA package | | | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 80-pin PNA: 1, 20, 21, 40, 41, 60, 61, 80 | | ±750 |
| All F28P550Sxx devices in 64-pin PM package | | | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64 | | ±750 |
| All F28P550Sxx devices in 56-pin RSH package | | | | | |
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V | |
| | | Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾ | All pins | | ±500 |
| | | | Corner pins on 56-pin RSH: 1, 14, 15, 28, 29, 42, 43, 56 | | ±750 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings – Automotive

| | | | VALUE | UNIT | |
|--|-------------------------|---|--|-------|---|
| All F28P559Sxx-Q1 devices in 128-pin PDT package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 128-pin PDT: 1, 32, 33, 64, 65, 96, 97, 128 | ±750 | |
| All F28P559Sxx-Q1 devices in 100-pin PZ package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 100-pin PZ: 1, 25, 26, 50, 51, 75, 76, 100 | ±750 | |
| All F28P559Sxx-Q1 devices in 80-pin PNA package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 80-pin PNA: 1, 20, 21, 40, 41, 60, 61, 80 | ±750 | |
| All F28P559Sxx-Q1 devices in 64-pin PM package | | | | | |
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | All pins | ±2000 | V |
| | | Charged device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins on 64-pin PM: 1, 16, 17, 32, 33, 48, 49, 64 | ±750 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.4 Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT | |
|---|--|---|-----|-------------|------|---|
| Device supply voltage, VDDIO and VDDA | Internal BOR enabled ⁽³⁾ | V _{BOR-VDDIO} (MAX) + V _{BOR-GB} ⁽²⁾ | | 3.3 | 3.63 | V |
| | Internal BOR disabled | 2.8 | 3.3 | 3.63 | | |
| Device supply voltage, VDD | | 1.14 | 1.2 | 1.32 | V | |
| Device ground, VSS | | | 0 | | V | |
| Analog ground, VSSA | | | 0 | | V | |
| SR _{SUPPLY} | Supply ramp rate of VDDIO, VDD, VDDA with respect to VSS. ⁽⁴⁾ | | | | | |
| V _{IN} | Digital input voltage ⁽⁶⁾ | VSS – 0.3 | | VDDIO + 0.3 | V | |
| | Digital input voltage(GPIO2, 3, 9, and 32) ⁽⁵⁾ | VSS – 0.3 | | 5.5 | V | |
| | Analog input voltage ⁽⁶⁾ | VSSA – 0.3 | | VDDA + 0.3 | V | |
| Junction temperature, T _J ⁽¹⁾ | | –40 | | 150 | °C | |
| Free-Air temperature, T _A | | –40 | | 125 | °C | |

- (1) Operation above T_J = 105°C for extended duration will reduce the lifetime of the device. See [Calculating Useful Lifetimes of Embedded Processors](#) for more information.
- (2) See the *Power Management Module (PMM)* section.
- (3) Internal BOR is enabled by default.
- (4) See the *Power Management Module Operating Conditions* table.
- (5) These pins support applied voltage prior to the device being powered
- (6) Applying a V_{IN} greater than VDDIO/VDDA or less than VSS/VSSA will turn on the ESD current clamping diode causing additional current flow to the respective supply rail. VDDIO/VDDA voltage will internally rise and could impact other electrical characteristics.

6.5 Power Consumption Summary

Current values listed in this section are representative for the test conditions given and not the absolute maximum possible. The actual device currents in an application will vary with application code and pin configurations.

6.5.1 System Current Consumption - VREG Enable - Internal Supply

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_j

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|---|--|--------|-----|-----|------|
| OPERATING MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption during operational usage | This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 92 | | mA |
| | | | 85 °C | | 105 | mA |
| | | | 125 °C | | 115 | mA |
| I_{DDA} | VDDA current consumption during operational usage | This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |
| IDLE MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Idle mode | - CPU is in IDLE mode - Flash is powered down - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 30 | | mA |
| | | | 85 °C | | 36 | mA |
| | | | 125 °C | | 48 | mA |
| I_{DDA} | VDDA current consumption while device is in Idle mode | - CPU is in IDLE mode - Flash is powered down - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |
| STANDBY MODE (PLL Enabled) | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 8 | | mA |
| | | | 85 °C | | 14 | mA |
| | | | 125 °C | | 25 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |

6.5.1 System Current Consumption - VREG Enable - Internal Supply (continued)

Over recommended operating conditions (unless otherwise noted)

 TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|---|--|--------|------|-----|------|
| STANDBY MODE (PLL Disabled) | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down - PLL is Disabled, SYSCLK & CPUCLK are gated | 30 °C | 4 | | mA |
| | | | 85 °C | | 10 | mA |
| | | | 125 °C | | 21 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |
| HALT MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while device is in Halt mode | - CPU is in HALT mode - Flash is powered down - PLL is Disabled, SYSCLK and CPUCLK are gated | 30 °C | 4 | | mA |
| | | | 85 °C | | 10 | mA |
| | | | 125 °C | | 20 | mA |
| I_{DDA} | VDDA current consumption while device is in Halt mode | - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |
| FLASH ERASE/PROGRAM | | | | | | |
| I_{DDIO} | VDDIO current consumption during Erase/Program cycle ⁽¹⁾ | - CPU is running from RAM - Flash going through continuous Program/Erase operation - PLL is enabled, SYSCLK at 120 MHz. - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low | | 91 | 128 | mA |
| I_{DDA} | VDDA current consumption during Erase/Program cycle | | | 0.1 | 8 | mA |
| RESET MODE | | | | | | |
| I_{DDIO} | VDDIO current consumption while reset is active ⁽²⁾ | Device is under Reset | 30 °C | 10 | | mA |
| | | | 85 °C | 13 | | mA |
| | | | 125 °C | 20 | | mA |
| I_{DDA} | VDDA current consumption while reset is active ⁽²⁾ | | 30 °C | 0.01 | | mA |
| | | | 85 °C | 0.01 | | mA |
| | | | 125 °C | 0.01 | | mA |

(1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.

(2) This is the current consumption while reset is active, that is, XRSn is low.

6.5.2 System Current Consumption - VREG Disable - External Supply

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|---|--|--------|-----|-----|------|
| OPERATING MODE | | | | | | |
| I_{DD} | VDD current consumption during operational usage | This is an estimation of current for a typical heavily loaded application. Actual currents will vary depending on system activity, I/O electrical loading and switching frequency. This includes Core supply current with Internal Vreg Enabled. - CPU is running from RAM - Flash is powered up - X1/X2 crystal is powered up - PLL is enabled, SYSCLK=Max Device frequency - Analog modules are powered up - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 85 | | mA |
| | | | 85 °C | | 96 | mA |
| | | | 125 °C | | 108 | mA |
| I_{DDIO} | VDDIO current consumption during operational usage | | 30 °C | 13 | | mA |
| | | | 85 °C | 17 | | mA |
| | | | 125 °C | 18 | | mA |
| I_{DDA} | VDDA current consumption during operational usage | | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |
| IDLE MODE | | | | | | |
| I_{DD} | VDD current consumption while device is in Idle mode | - CPU is in IDLE mode - Flash is powered down - PLL is Enabled, SYSCLK=Max Device Frequency, CPUCLK is gated - X1/X2 crystal is powered up - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 28 | | mA |
| | | | 85 °C | | 35 | mA |
| | | | 125 °C | | 47 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Idle mode | | 30 °C | 3 | | mA |
| | | | 85 °C | 6 | | mA |
| | | | 125 °C | 7 | | mA |
| I_{DDA} | VDDA current consumption while device is in Idle mode | | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |
| STANDBY MODE (PLL Enabled) | | | | | | |
| I_{DD} | VDD current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down - PLL is Enabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down - Analog Modules are powered down - Outputs are static without DC Load - Inputs are static high or low | 30 °C | 6 | | mA |
| | | | 85 °C | | 12 | mA |
| | | | 125 °C | | 24 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | | 30 °C | 3 | | mA |
| | | | 85 °C | 6 | | mA |
| | | | 125 °C | 7 | | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |

6.5.2 System Current Consumption - VREG Disable - External Supply (continued)

Over recommended operating conditions (unless otherwise noted)

 TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------------|---|--|--------|-----|-----|------|
| STANDBY MODE (PLL Disabled) | | | | | | |
| I_{DD} | VDD current consumption while device is in Standby mode | - CPU is in STANDBY mode - Flash is powered down - PLL is Disabled, SYSCLK & CPUCLK are gated - X1/X2 crystal is powered down | 30 °C | 3 | | mA |
| | | | 85 °C | | 8 | mA |
| | | | 125 °C | | 20 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Standby mode | - Analog Modules are powered down - Outputs are static without DC Load | 30 °C | 2 | | mA |
| | | | 85 °C | | 5 | mA |
| | | | 125 °C | | 6 | mA |
| I_{DDA} | VDDA current consumption while device is in Standby mode | - Inputs are static high or low | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |
| HALT MODE | | | | | | |
| I_{DD} | VDD current consumption while device is in Halt mode | - CPU is in HALT mode - Flash is powered down - PLL is Disabled, SYSCLK and CPUCLK are gated - X1/X2 crystal is powered down | 30 °C | 2 | | mA |
| | | | 85 °C | | 8 | mA |
| | | | 125 °C | | 20 | mA |
| I_{DDIO} | VDDIO current consumption while device is in Halt mode | - Analog Modules are powered down - Outputs are static without DC Load | 30 °C | 2 | | mA |
| | | | 85 °C | | 5 | mA |
| | | | 125 °C | | 6 | mA |
| I_{DDA} | VDDA current consumption while device is in Halt mode | - Inputs are static high or low | 30 °C | 1 | | mA |
| | | | 85 °C | | 3 | mA |
| | | | 125 °C | | 8 | mA |
| FLASH ERASE/PROGRAM | | | | | | |
| I_{DD} | VDD current consumption during Erase/Program cycle ⁽¹⁾ | - CPU is running from RAM - Flash going through continuous Program/Erase operation - PLL is enabled, SYSCLK at 100 MHz. - Peripheral clocks are turned OFF. - X1/X2 crystal is powered up - Analog is powered down - Outputs are static without DC Load - Inputs are static high or low | | 80 | 108 | mA |
| I_{DDIO} | VDDIO current consumption during Erase/Program cycle ⁽¹⁾ | | | 11 | 20 | mA |
| I_{DDA} | VDDA current consumption during Erase/Program cycle | | | 0.1 | 8 | mA |

6.5.2 System Current Consumption - VREG Disable - External Supply (continued)

Over recommended operating conditions (unless otherwise noted)

TYP : V_{nom} , Temperatures shown are T_J

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|--|-----------------------|--------|------|-----|------|
| RESET MODE | | | | | | |
| I_{DD} | VDD current consumption while reset is active ⁽²⁾ | Device is under Reset | 30 °C | 5 | | mA |
| | | | 85 °C | 8 | | mA |
| | | | 125 °C | 15 | | mA |
| I_{DDIO} | VDDIO current consumption while reset is active ⁽²⁾ | | 30 °C | 5 | | mA |
| | | | 85 °C | 5 | | mA |
| | | | 125 °C | 5 | | mA |
| I_{DDA} | VDDA current consumption while reset is active ⁽²⁾ | | 30 °C | 0.01 | | mA |
| | | | 85 °C | 0.01 | | mA |
| | | | 125 °C | 0.01 | | mA |

- (1) Brownout events during flash programming can corrupt flash data and permanently lock the device. Programming environments using alternate power sources (such as a USB programmer) must be capable of supplying the rated current for the device and other system components with sufficient margin to avoid supply brownout conditions.
- (2) This is the current consumption while reset is active, that is XRSn is low.

6.5.3 Operating Mode Test Description

The *System Current Consumption - VREG Enable - Internal Supply* table, *System Current Consumption - VREG Disable - External Supply* table, and [Section 6.5.4](#) list the current consumption values for the operational mode of the device. The operational mode provides an estimation of what an application might encounter. The test condition for these measurements has the following properties:

- Code is executing from RAM.
- FLASH is read and kept in active state.
- No external components are driven by I/O pins.
- All peripherals have clocks enabled.
- The CPU is actively executing code.
- All analog peripherals are powered up. ADCs and DACs are periodically converting.

6.5.4 Reducing Current Consumption

The F28P55x devices provide some methods to reduce the device current consumption:

- One of the two low-power modes—IDLE or STANDBY—could be entered during idle periods in the application.
- The flash module may be powered down if the code is run from RAM.
- Disable the pullups on pins that assume an output function.
- Each peripheral has an individual clock-enable bit (PCLKCRx). Reduced current consumption may be achieved by turning off the clock to any peripheral that is not used in a given application. The *Typical Current Reduction per Disabled Peripheral* table lists the typical current reduction that may be achieved by disabling the clocks using the PCLKCRx register.
- To realize the lowest VDDA current consumption in an LPM, see the Analog-to-Digital Converter (ADC) chapter of the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#) to ensure each module is powered down as well.

6.5.4.1 Typical Current Reduction per Disabled Peripheral

For peripherals with multiple instances, the current quoted is for all modules combined.

| PERIPHERAL | I _{DDIO} CURRENT REDUCTION (mA) |
|----------------------|--|
| ADC ⁽¹⁾ | 1.0 |
| CLA | 0.56 |
| CLB | 1.41 |
| CMPSS ⁽¹⁾ | 0.31 |
| CPU TIMER | 0.06 |
| GPDAC | 0.12 |
| MCAN | 1.01 |
| DCC | 0.08 |
| eCAP | 0.12 |
| ERAD | 1.56 |
| EPG | 0.32 |
| ePWM(per) | 0.95 |
| eQEP | 0.18 |
| SCI | 0.50 |
| I2C | 0.51 |
| SPI | 0.11 |
| FSI RX | 0.34 |
| FSI TX | 0.27 |
| PMBUS | 0.28 |

(1) This current represents the current drawn by the digital portion of the each module.

6.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|------------------------------|--|---|---|-----|-----------|------|----|---|
| Digital and Analog IO | | | | | | | | |
| V _{OH} | High-level output voltage | I _{OH} = I _{OH} MIN | VDDIO * 0.8 | | | V | | |
| | | I _{OH} = -100 μA | VDDIO - 0.2 | | | | | |
| V _{OL} | Low-level output voltage | I _{OL} = I _{OL} MAX | | | 0.4 | V | | |
| | | I _{OL} = 100 μA | | | 0.2 | | | |
| I _{OH} | High-level output source current for all output pins | | -4 | | | mA | | |
| I _{OL} | Low-level output sink current for all output pins | | | | 4 | mA | | |
| | Low-level output sink current for all output pins - GPIO2/3/9/32 | IO_DRVSEL:DRVSELG PIOx = 0 | | | 4 | mA | | |
| | | IO_DRVSEL:DRVSELG PIOx = 1 | | | 12 | mA | | |
| R _{OH} | High-level output impedance for all output pins | | VOH=VDDIS-0.4V | | 50 | 66 | 96 | Ω |
| R _{OL} | Low-level output impedance for all output pins | | VOL=0.4V | | 48 | 60 | 84 | Ω |
| V _{IH} | High-level input voltage | | 2.0 | | | V | | |
| | High-level input voltage - GPIO2/3/9/32 | IO_MODSEL:MODSEL GPIOx = 0 | 0.7*VDDIO | | | V | | |
| | | IO_MODSEL:MODSEL GPIOx = 1 | 1.35 | | | V | | |
| V _{IL} | Low-level input voltage | | | | 0.8 | V | | |
| | Low-level input voltage - GPIO2/3/9/32 | IO_MODSEL:MODSEL GPIOx = 0 | | | 0.3*VDDIO | V | | |
| | | IO_MODSEL:MODSEL GPIOx = 1 | | | 0.8 | V | | |
| V _{HYSTERESIS} | Input hysteresis (AIO) | | 125 | | | mV | | |
| | Input hysteresis (GPIO) | | 125 | | | | | |
| I _{PULLDOWN} | Input current | Pins with pulldown | VDDIO = 3.3 V V _{IN} = VDDIO | | 120 | μA | | |
| I _{PULLUP} | Input current | Digital inputs with pullup enabled ⁽¹⁾ | VDDIO = 3.3 V V _{IN} = 0 V | | 160 | μA | | |
| R _{PULLDOWN} | Weak pulldown resistance | | 22 | 31 | 62 | kΩ | | |
| R _{PULLUP} | Weak pullup resistance | | 19 | 29 | 54 | kΩ | | |
| | GPIO2/3/9/32 | | 20 | 31 | 65 | kΩ | | |
| I _{LEAK} | Pin leakage | Digital inputs | Pullups and outputs disabled 0 V ≤ V _{IN} ≤ VDDIO | | 0.1 | μA | | |
| | | Digital inputs (GPIO2/3/9/32 only) | | | 20 | | | |
| | | Analog pins | Analog drivers disabled 0 V ≤ V _{IN} ≤ VDDA | | 0.1 | | | |
| C _I | Input capacitance | Digital inputs | | | 2 | pF | | |
| | | Analog pins ⁽²⁾ | | | | | | |

6.6 Electrical Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|--|-----------------|-----|-----|-----|------|
| VREG and BOR | | | | | | |
| VREG, POR, BOR ⁽³⁾ | | | | | | |

- (1) See the *Pins With Internal Pullup and Pulldown* table for a list of pins with a pullup or pulldown.
- (2) The analog pins are specified separately; see the *Per-Channel Parasitic Capacitance* tables that are in the *ADC Input Model* section.
- (3) See the *Power Management Module (PMM)* section.

ADVANCE INFORMATION

6.7 Thermal Resistance Characteristics for PDT Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance | 10.6 |
| R θ_{JB} | Junction-to-board thermal resistance | 24.9 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 42.5 |
| Psi $_{JT}$ | Junction-to-package top | 0.4 |
| Psi $_{JB}$ | Junction-to-board | 24.4 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.8 Thermal Resistance Characteristics for PZ Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance | 11 |
| R θ_{JB} | Junction-to-board thermal resistance | 28.8 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 46.4 |
| Psi $_{JT}$ | Junction-to-package top | 0.4 |
| Psi $_{JB}$ | Junction-to-board | 28.2 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.9 Thermal Resistance Characteristics for PNA Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance | 14.5 |
| R θ_{JB} | Junction-to-board thermal resistance | 29.5 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 51.7 |
| Psi $_{JT}$ | Junction-to-package top | 0.5 |
| Psi $_{JB}$ | Junction-to-board | 29.4 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.10 Thermal Resistance Characteristics for PM Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance | 11.6 |
| R θ_{JB} | Junction-to-board thermal resistance | 24.9 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 45 |
| Psi $_{JT}$ | Junction-to-package top | 0.4 |
| Psi $_{JB}$ | Junction-to-board | 24.5 |

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [R θ_{JC}] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.11 Thermal Resistance Characteristics for RSH Package

| | | °C/W ⁽¹⁾ |
|------------------------------|---|---------------------|
| R θ_{JC} | Junction-to-case thermal resistance(top) | 11.6 |
| | Junction-to-case thermal resistance(bottom) | 1.2 |
| R θ_{JB} | Junction-to-board thermal resistance | 6.7 |
| R θ_{JA} (High k PCB) | Junction-to-free air thermal resistance | 23.7 |
| Psi $_{JT}$ | Junction-to-package top | 0.1 |
| Psi $_{JB}$ | Junction-to-board | 6.7 |

6.12 Thermal Design Considerations

Based on the end application design and operational profile, the I $_{DD}$ and I $_{DDIO}$ currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T $_A$) varies with the end application and product design. The critical factor that affects reliability and functionality is T $_J$, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T $_J$ within the specified limits. T $_{case}$ should be measured to estimate the operating junction temperature T $_J$. T $_{case}$ is normally measured at the center of the package top-side surface. The thermal application report [Semiconductor and IC Package Thermal Metrics](#) helps to understand the thermal metrics and definitions.

6.13 System

6.13.1 Power Management Module (PMM)

6.13.1.1 Introduction

The Power Management Module (PMM) handles all the power management functions required for device operation.

6.13.1.2 Overview

The block diagram of the PMM is shown in Figure 6-1. As can be seen, the PMM comprises of various subcomponents, which are described in the subsequent sections.

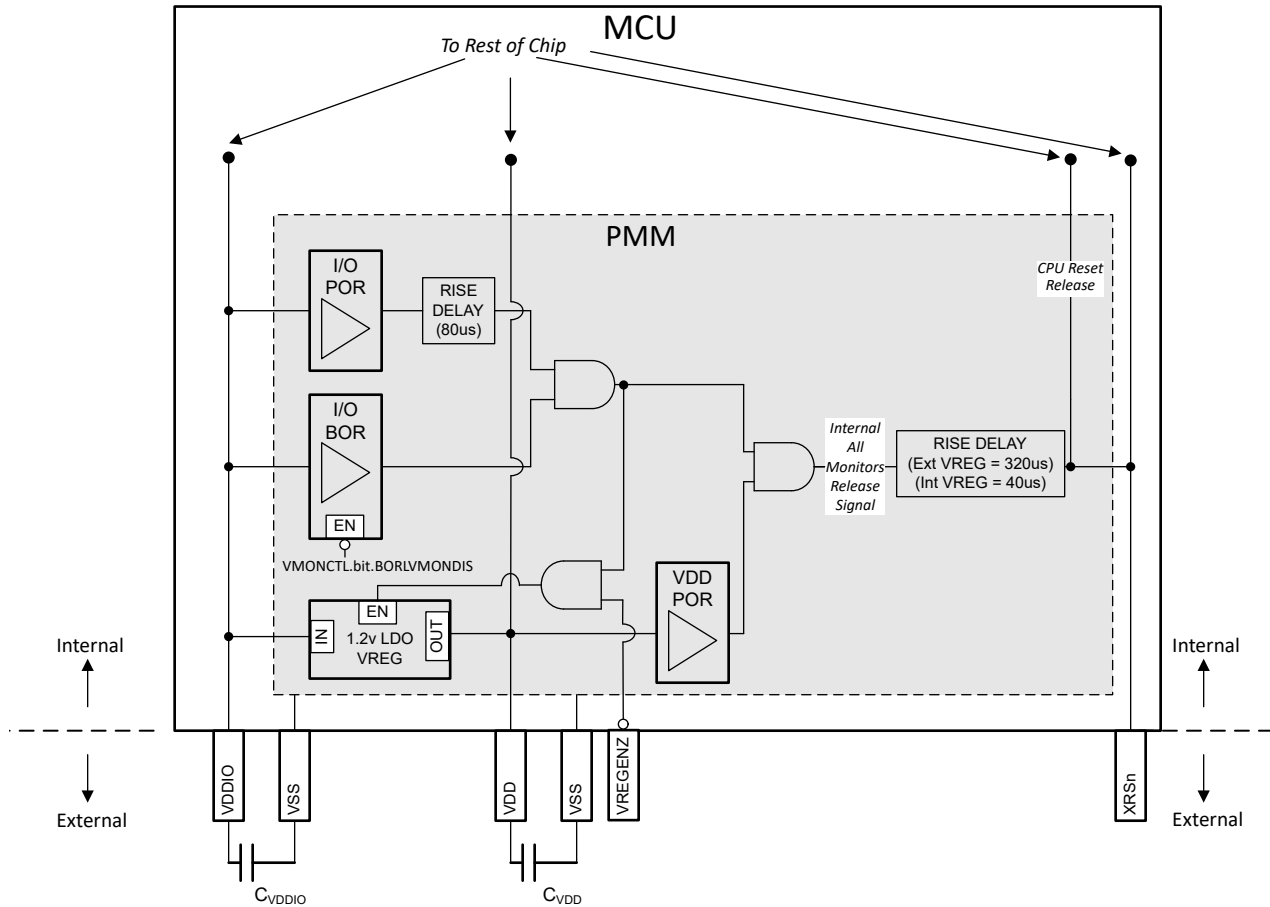


Figure 6-1. PMM Block Diagram

6.13.1.2.1 Power Rail Monitors

The PMM has voltage monitors on the supply rails that release the XRSn signal high once the voltages cross the set threshold during power up. They also function to trip the XRSn signal low if any of the voltages drop below the programmed levels. The various voltage monitors are described in subsequent sections.

Note

Not all the voltage monitors are supported for device operation in an application after boot up. In the case where a voltage monitor is not supported, an external supervisor is recommended if the device needs supply voltage monitoring while the application is running.

The three voltage monitors (I/O POR, I/O BOR, VDD POR) all have to release their respective outputs before the device begins operation (that is, XRSn goes high). However, if any of the voltage monitors trips, XRSn is driven low. The I/Os are held in high impedance when any of the voltage monitors trip.

6.13.1.2.1.1 I/O POR (Power-On Reset) Monitor

The I/O POR monitor supervises the VDDIO rail. During power up, this is the first monitor to release (that is, first to untrip) on VDDIO.

6.13.1.2.1.2 I/O BOR (Brown-Out Reset) Monitor

The I/O BOR monitor also supervises the VDDIO rail. During power up, this is the second monitor to release (that is, second to untrip) on VDDIO. This monitor has a tighter tolerance compared to the I/O POR.

Any drop in voltage below the recommended operating voltages will trip the I/O BOR and reset the device but this can be disabled by setting VMONCTL.bit.BORLVMONDIS to 1. The I/O BOR can only be disabled after the device has fully booted up. If the I/O BOR is disabled, the I/O POR will reset the device for voltage drops.

Note

The level at which the I/O POR trips is well below the minimum recommended voltage for VDDIO, and therefore should not be used for device supervision.

Figure 6-2 shows the operating region of the I/O BOR.

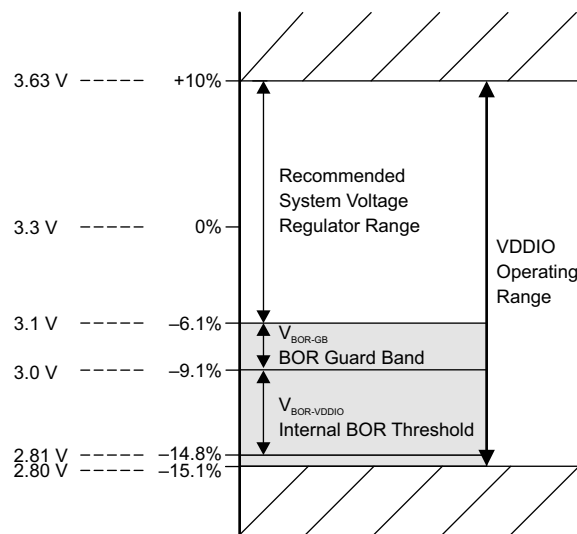


Figure 6-2. I/O BOR Operating Region

6.13.1.2.1.3 VDD POR (Power-On Reset) Monitor

The VDD POR monitor supervises the VDD rail. During power up, this monitor releases (that is, untrips) once the voltage crosses the programmed trip level on VDD.

Note

VDD POR is programmed at a level below the minimum recommended voltage for VDD, and therefore it should not be relied upon for VDD supervision if that is required in the application.

6.13.1.2.2 External Supervisor Usage

VDDIO Monitoring: The I/O BOR is supported for application use, so an external supervisor is not required to monitor the I/O rail.

VDD Monitoring:

- VDD supplied from the internal VREG: The VDD supply is derived from the VDDIO supply. The VREG is designed in such a way that a valid VDDIO supply(monitored by the IO BOR) implies a valid VDD supply.
- VDD supplied from an external supply: The VDD POR is not supported for application use. If VDD monitoring is required by the application, an external supervisor can be used to monitor the VDD rail.

Note

The use of an external supervisor with the internal VREG is not supported.If VDD monitoring is required by the application, a package with a VREGENZ pin must be used to power VDD externally.

6.13.1.2.3 Delay Blocks

The delay blocks in the path of the voltage monitors work together to delay the release time between the voltage monitors and XRSn. This is to ensure that the voltages are stable when XRSn releases. The delay blocks are only active during power up (that is, when VDDIO and VDD are ramping up).

The delay blocks contribute to the minimum slew rates specified in [Power Management Module Electrical Data and Timing](#) for the power rails.

Note

The delay numbers specified in the block diagram are typical numbers.

6.13.1.2.4 Internal 1.2-V LDO Voltage Regulator (VREG)

The internal VREG is supplied by the VDDIO rail and can generate the 1.2 V required to power the VDD pins. Although the internal VREG eliminates the need to use an external supply for VDD, decoupling capacitors are still required on the VDD pins for VREG stability and transients. See the *VDD Decoupling* section for details.

6.13.1.2.5 VREGENZ

The VREGENZ (VREG disable) pin controls the state of the internal VREG. To enable the internal VREG, connect the VREGENZ pin to a logic low voltage. For applications supplying VDD externally (external VREG), disable the internal VREG by tying the VREGENZ pin high.

Note

Not all device packages have VREGENZ pinned out. For packages without VREGENZ, external VREG mode is not supported.

6.13.1.3 External Components

6.13.1.3.1 Decoupling Capacitors

VDDIO and VDD require decoupling capacitors for correct operation. The requirements are outlined in subsequent sections.

6.13.1.3.1.1 VDDIO Decoupling

Place a minimum amount of decoupling capacitance on VDDIO. See the C_{VDDIO} parameter in [Power Management Module Electrical Data and Timing](#). The actual amount of decoupling capacitance to use is a requirement of the power supply driving VDDIO. Either of the configurations outlined below is acceptable:

- **Configuration 1:** Place a decoupling capacitor on each VDDIO pin per the C_{VDDIO} parameter.
- **Configuration 2:** Install a single decoupling capacitor that is the equivalent of $C_{VDDIO} * VDDIO$ pins.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.13.1.3.1.2 VDD Decoupling

Place a minimum amount of decoupling capacitance on VDD. See the C_{VDD} TOTAL parameter in [Power Management Module Electrical Data and Timing](#).

In external VREG mode, the actual amount of decoupling capacitance to use is a requirement of the power supply driving VDD.

Either of the configurations outlined below is acceptable:

- **Configuration 1:** Divide C_{VDD} TOTAL equally across the VDD pins. In this configuration, the VDD pins may be separated at the PCB level.
- **Configuration 2:** Install a single decoupling capacitor with value of C_{VDD} TOTAL. In this configuration, all VDD pins must be connected to each other on the PCB.

Note

Having the decoupling capacitor or capacitors close to the device pins is critical.

6.13.1.4 Power Sequencing

6.13.1.4.1 Supply Pins Ganging

Connecting all 3.3-V rails together and supplying from a single source are strongly recommended. This list includes:

- VDDIO
- VDDA

In addition, connect all power pins to avoid leaving any unconnected.

In external VREG mode, the VDD pins should be tied together and supplied from a single source.

In internal VREG mode, tying the VDD pins together is optional as long as each VDD pin has a capacitor connected to pin. See the *VDD Decoupling* section for VDD decoupling configurations.

The analog modules on the device have fairly high PSRR; therefore, in most cases, noise on VDDA will have to exceed the recommended operating conditions of the supply rails before the analog modules see performance degradation. Therefore, supplying VDDA separately typically offers minimal benefits. Nevertheless, for the purposes of noise improvement, placing a pi filter between VDDIO and VDDA is acceptable.

Note

All the supply pins per rail are tied together internally. For example, all VDDIO pins are tied together internally, all VDD pins are tied together internally, and so forth.

6.13.1.4.2 Signal Pins Power Sequence

Before powering the device, do not apply voltage larger than 0.3 V above VDDIO or 0.3 V below VSS to any digital pin and 0.3 V above VDDA or 0.3 V below VSSA to any analog pin (including VREFHI). Simply, the signal pins should only be driven after XRSn goes high, provided all the 3.3-V rails are tied together. This sequencing is still required even if VDDIO and VDDA are not tied together.

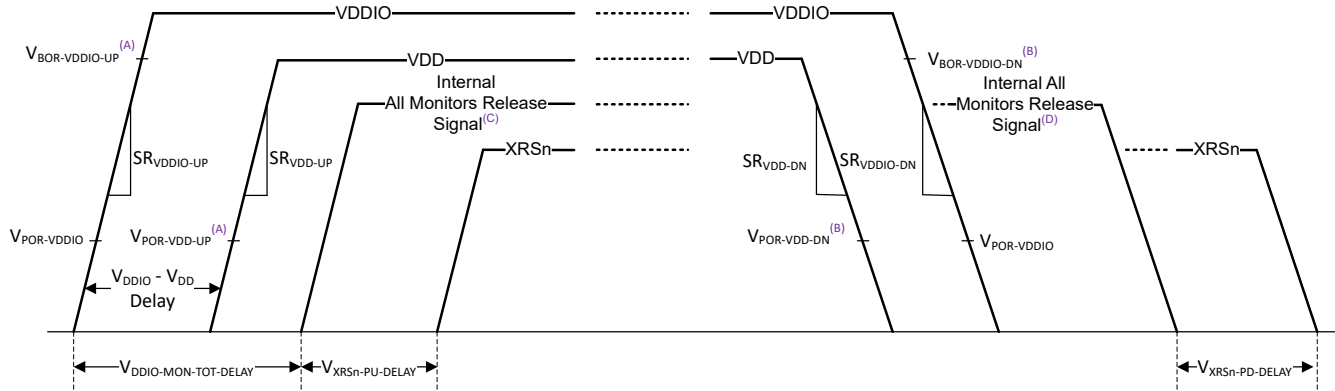
CAUTION

If the above sequence is violated, device malfunction and possibly damage can occur as current will flow through unintended parasitic paths in the device.

6.13.1.4.3 Supply Pins Power Sequence

6.13.1.4.3.1 External VREG/VDD Mode Sequence

Figure 6-3 depicts the power sequencing requirements for external VREG mode. The values for all the parameters indicated can be found in [Power Management Module Electrical Data and Timing](#).



- A. This trip point is the trip point before XRSn releases. See the *Power Management Module Characteristics* table.
- B. This trip point is the trip point after XRSn releases. See the *Power Management Module Characteristics* table.
- C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the *PMM Block Diagram*.
- D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the *PMM Block Diagram*.

Figure 6-3. External VREG Power Up Sequence

For Power Up:

1. VDDIO (that is, the 3.3-V rail) should come up first with the minimum slew rate specified.
2. VDD (that is, the 1.2-V rail) should come up next with the minimum slew rate specified.
3. The time delta between the VDDIO rail coming up and when the VDD rail can come up is also specified.
4. After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSN-PD-DELAY}$, XRSn will be released and the device starts the boot-up sequence.
5. The I/O BOR monitor has different release points during power up and power down.
6. During power up, both VDDIO and VDD rails have to be up before XRSn releases.

For Power Down:

1. There is no requirement between VDDIO and VDD on which should power down first; however, there is a minimum slew rate specification.
2. The I/O BOR monitor has different release points during power up and power down.
3. Any of the POR or BOR monitors that trips during power down will cause XRSn to go low after $V_{XRSN-PD-DELAY}$.

Note

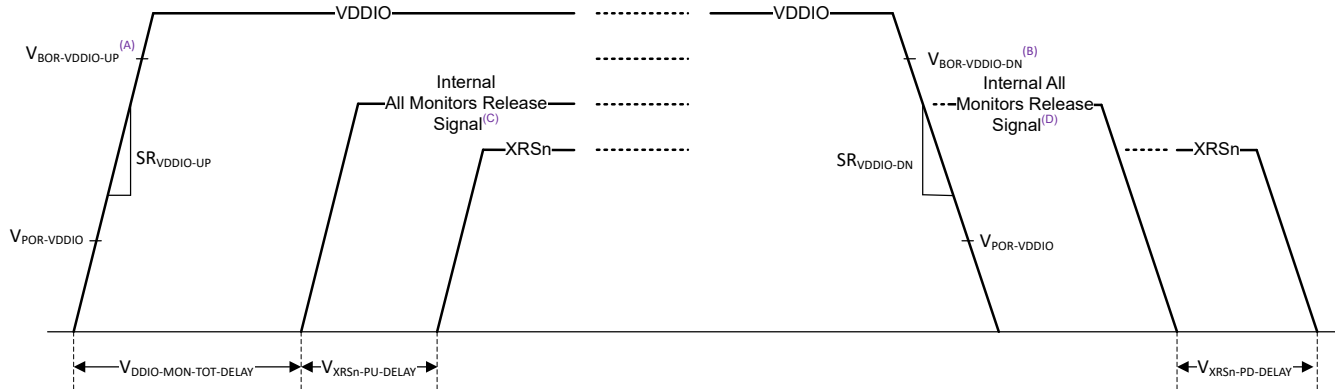
The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.13.1.4.3.2 Internal VREG/VDD Mode Sequence

Figure 6-4 depicts the power sequencing requirements for internal VREG mode. The values for all the parameters indicated can be found in [Power Management Module Electrical Data and Timing](#).



- A. This trip point is the trip point before XRSn releases. See the *Power Management Module Characteristics* table.
- B. This trip point is the trip point after XRSn releases. See the *Power Management Module Characteristics* table.
- C. During power up, the All Monitors Release Signal goes high after all POR and BOR monitors are released. See the *PMM Block Diagram*.
- D. During power down, the All Monitors Release Signal goes low if any of the POR or BOR monitors are tripped. See the *PMM Block Diagram*.

Figure 6-4. Internal VREG Power Up Sequence

- **For Power Up:**
 1. VDDIO (that is, the 3.3-V rail) should come up with the minimum slew rate specified.
 2. The Internal VREG powers up after the I/O monitors (I/O POR and I/O BOR) are released.
 3. After the times specified by $V_{DDIO-MON-TOT-DELAY}$ and $V_{XRSn-PU-DELAY}$, XRSn will be released and the device starts the boot-up sequence.
 4. The I/O BOR monitor has different release points during power up and power down.
- **For Power Down:**
 1. The only requirement on VDDIO during power down is the slew rate.
 2. The I/O BOR monitor has different release points during power up and power down.
 3. The I/O BOR tripping will cause XRSn to go low after $V_{XRSn-PD-DELAY}$ and also power down the Internal VREG.

Note

The *All Monitors Release Signal* is an internal signal.

Note

If there is an external circuit driving XRSn (for example, a supervisor), the boot-up sequence does not start until the XRSn pin is released by all internal and external sources.

6.13.1.4.3.3 Supply Sequencing Summary and Effects of Violations

The acceptable power-up sequence for the rails is summarized below. "Power up" here means the rail in question has reached the minimum recommended operating voltage.

CAUTION
 Non-acceptable sequences leads to reliability concerns and possibly damage.

For simplicity, connecting all 3.3-V rails together and following the descriptions in [Supply Pins Power Sequence](#) is recommended.

Table 6-1. External VREG Sequence Summary

| CASE | RAILS POWER-UP ORDER | | | ACCEPTABLE |
|------|----------------------|------|-----|------------|
| | VDDIO | VDDA | VDD | |
| A | 1 | 2 | 3 | Yes |
| B | 1 | 3 | 2 | Yes |
| C | 2 | 1 | 3 | - |
| D | 2 | 3 | 1 | - |
| E | 3 | 2 | 1 | - |
| F | 3 | 1 | 2 | - |
| G | 1 | 1 | 2 | Yes |
| H | 2 | 2 | 1 | - |

Table 6-2. Internal VREG Sequence Summary

| CASE | RAILS POWER-UP ORDER | | ACCEPTABLE |
|------|----------------------|------|------------|
| | VDDIO | VDDA | |
| A | 1 | 2 | Yes |
| B | 2 | 1 | - |
| C | 1 | 1 | Yes |

Note

The analog modules on the device should only be powered after VDDA has reached the minimum recommended operating voltage.

6.13.1.4.3.4 Supply Slew Rate

VDDIO has a minimum slew rate requirement. If the minimum slew rate is not met, XRSn might toggle a few times until VDDIO crosses the I/O BOR region.

Note

The toggling on XRSn has no adverse effect on the device as boot only starts once XRSn is steadily high. However if XRSn from the device is used to gate the reset signal of other ICs, then the slew rate requirement should be met to prevent this toggling.

VDD has a minimum slew rate requirement in external VREG mode. If the minimum slew rate is not met, the VDD POR may release before the VDD operational minimum voltage is met and the device may not start in a properly reset state.

6.13.1.5 Power Management Module Electrical Data and Timing

6.13.1.5.1 Power Management Module Operating Conditions

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|-----------------|-----|-----|-----|-------|
| General | | | | | | |
| C_{VDDIO} (1) (2) | VDDIO Capacitance Per Pin ⁽⁷⁾ | | 0.1 | | | uF |
| C_{VDDA} (1) (2) | VDDA Capacitance Per Pin ⁽⁷⁾ | | 2.2 | | | uF |
| SR_{VDD33} (3) | Supply Ramp Rate of 3.3V Rails (VDDIO, VDDA) | | 20 | | 100 | mV/us |
| $V_{BOR-VDDIO-GB}$ (5) | VDDIO Brown Out Reset Voltage Guardband | | | 0.1 | | V |
| External VREG | | | | | | |
| $C_{VDD\ TOTAL}$ (1) (4) | Total VDD Capacitance ⁽⁷⁾ | | 10 | | | uF |
| SR_{VDD12} (3) | Supply Ramp Rate of 1.2V Rail (VDD) | | 10 | | 100 | mV/us |
| $V_{DDIO} - V_{DD}$ Delay ⁽⁶⁾ | Ramp Delay Between VDDIO and VDD | | 0 | | | us |
| Internal VREG | | | | | | |
| $C_{VDD\ TOTAL}$ (1) (4) | Total Nominal VDD Capacitance ⁽⁷⁾ | | 10 | | 22 | uF |

- (1) A bulk capacitor should also be used. The exact value of the decoupling capacitance depends on the system voltage regulation solution that is supplying these pins.
- (2) It is recommended to tie the 3.3V rails (VDDIO, VDDA) together and supply them from a single source.
- (3) See the *Supply Slew Rate* section. Supply ramp rate faster than the maximum can trigger the on-chip ESD protection.
- (4) See the *Power Management Module (PMM)* section on possible configurations for the total decoupling capacitance.
- (5) TI recommends $V_{BOR-VDDIO-GB}$ to avoid BOR-VDDIO resets due to normal supply noise or load-transient events on the 3.3-V VDDIO system regulator. Good system regulator design and decoupling capacitance (following the system regulator specifications) are important to prevent activation of the BOR-VDDIO during normal device operation. The value of $V_{BOR-VDDIO-GB}$ is a system-level design consideration; the voltage listed here is typical for many applications.
- (6) Delay between when the 3.3-V rail ramps up and when the 1.2-V rail ramps up. See the *VREG Sequence Summary* table for the allowable supply ramp sequences.
- (7) Max capacitor tolerance should be 20%.

6.13.1.5.2 Power Management Module Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|-------------------------------|-------|-----|-------|------|
| V_{VREG} | Internal Voltage Regulator Output | | 1.152 | 1.2 | 1.248 | V |
| $V_{VREG-PU}$ | Internal Voltage Regulator Power Up Time | | | | 350 | us |
| $V_{VREG-INRUSH}$ (4) | Internal Voltage Regulator Inrush Current | | | 650 | | mA |
| $V_{POR-VDDIO}$ | VDDIO Power on Reset Voltage | Before and After XRSn Release | | 2.3 | | V |
| $V_{BOR-VDDIO-UP}$ (1) | VDDIO Brown Out Reset Voltage on Ramp Up | Before XRSn Release | | 2.7 | | V |
| $V_{BOR-VDDIO-DOWN}$ (1) | VDDIO Brown Out Reset Voltage on Ramp Down | After XRSn Release | 2.81 | | 3.0 | V |
| $V_{XRSn-PU-DELAY}$ (2) | XRSn Release Delay after Supplies are Ramped Up During Power-Up | | | 40 | | us |

6.13.1.5.2 Power Management Module Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|--|---------------------------------|-----|-----|-----|------|
| $V_{XRSn-PD-DELAY}$ (3) | XRSn Trip Delay after Supplies are Ramped Down During Power-Down | | | 2 | | us |
| $V_{DDIO-MON-TOT-DELAY}$ | Total Delays in Path of VDDIO Monitors (POR, BOR) | | | 80 | | us |
| $V_{XRSn-MON-RELEASE-DELAY}$ | XRSn Release Delay after a VDD POR Event | Supplies Within Operating Range | | 40 | | us |
| | XRSn Release Delay after a VDDIO BOR Event | | | 40 | | us |
| | XRSn Release Delay after a VDDIO POR Event | | | 120 | | us |

- (1) See the *I/O BOR Operating Region* figure.
- (2) Supplies are considered fully ramped up after they cross the minimum recommended operating conditions for the respective rail. All POR and BOR monitors need to be released before this delay takes effect.
- (3) On power down, any of the POR or BOR monitors that trips will immediately trip XRSn. This delay is the time between any of the POR, BOR monitors tripping and XRSn going low. It is variable and depends on the ramp down rate of the supply.
- (4) This is the transient current drawn on the VDDIO rail when the internal VREG turns on. Due to this, there might be some voltage drops on the VDDIO rail when the VREG turns on which could cause the VREG to ramp up in steps. There is no detriment to the device from this but the effect can be reduced if desired by using sufficient decoupling capacitors on VDDIO or picking an LDO/DC-DC that can supply this transient current.

6.13.2 Reset Timing

XRSn is the device reset pin. It functions as an input and open-drain output. The device has a built-in power-on reset (POR) and brown-out reset (BOR) monitors. During power up, the monitor circuits keep the XRSn pin low. For more details, see the *Power Management Module (PMM)* section. A watchdog or NMI watchdog reset will also drive the pin low. An external open-drain circuit may drive the pin to assert a device reset.

A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between XRSn and VDDIO. A capacitor should be placed between XRSn and VSS for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the XRSn pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Figure 6-5 shows the recommended reset circuit.

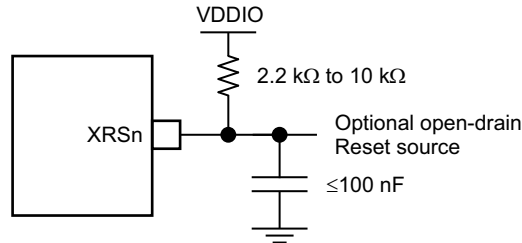


Figure 6-5. Reset Circuit

6.13.2.1 Reset Sources

The *Reset Signals* table summarizes the various reset signals and their effect on the device.

Table 6-3. Reset Signals

| Reset Source | CPU Core Reset (C28x, FPU, TMU) | Peripherals Reset | JTAG / Debug Logic Reset | IOs | XRS Output |
|------------------------|---------------------------------|-------------------|--------------------------|------|------------|
| POR | Yes | Yes | Yes | Hi-Z | Yes |
| BOR | Yes | Yes | Yes | Hi-Z | Yes |
| XRS Pin | Yes | Yes | No | Hi-Z | - |
| WDRS | Yes | Yes | No | Hi-Z | Yes |
| NMIWDRS | Yes | Yes | No | Hi-Z | Yes |
| SYSRS (Debugger Reset) | Yes | Yes | No | Hi-Z | No |
| SCCRESET | Yes | Yes | No | Hi-Z | No |
| SIMRESET. XRS | Yes | Yes | No | Hi-Z | Yes |
| SIMRESET. CPU1RS | Yes | Yes | No | Hi-Z | No |

The parameter $t_{h(\text{boot-mode})}$ must account for a reset initiated from any of these sources.

See the *Resets* section of the System Control chapter in the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#).

CAUTION

Some reset sources are internally driven by the device. Some of these sources will drive XRSn low, use this to disable any other devices driving the boot pins. The SCCRESET and debugger reset sources do not drive XRSn; therefore, the pins used for boot mode should not be actively driven by other devices in the system. The boot configuration has a provision for changing the boot pins in OTP.

6.13.2.2 Reset Electrical Data and Timing

6.13.2.2.1 Reset - XRSn - Timing Requirements

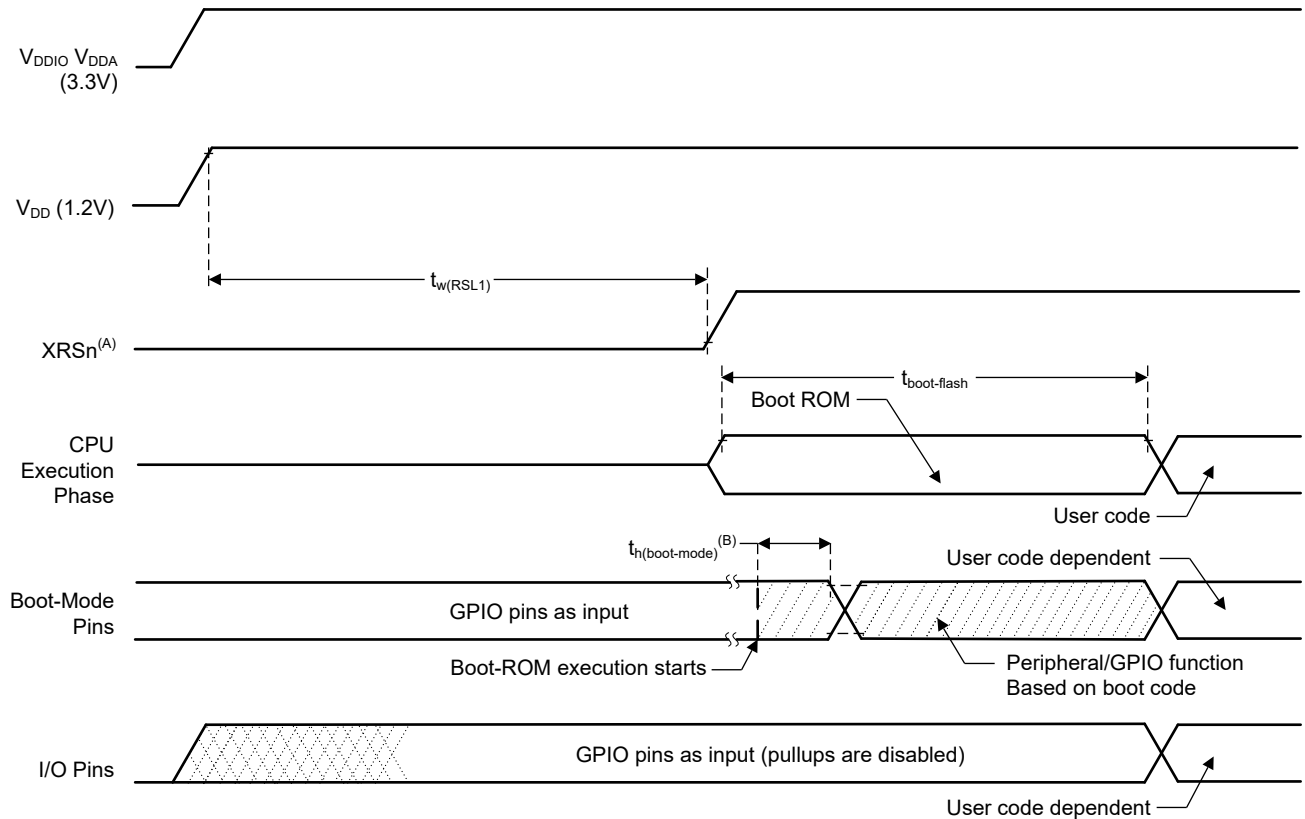
| | | MIN | MAX | UNIT |
|---------------------------|--|-----|-----|---------------|
| $t_{h(\text{boot-mode})}$ | Hold time for boot-mode pins | 1.5 | | ms |
| $t_{w(\text{RSL2})}$ | Pulse duration, XRSn low on warm reset | 3.2 | | μs |

6.13.2.2.2 Reset - XRSn - Switching Characteristics

over recommended operating conditions (unless otherwise noted)

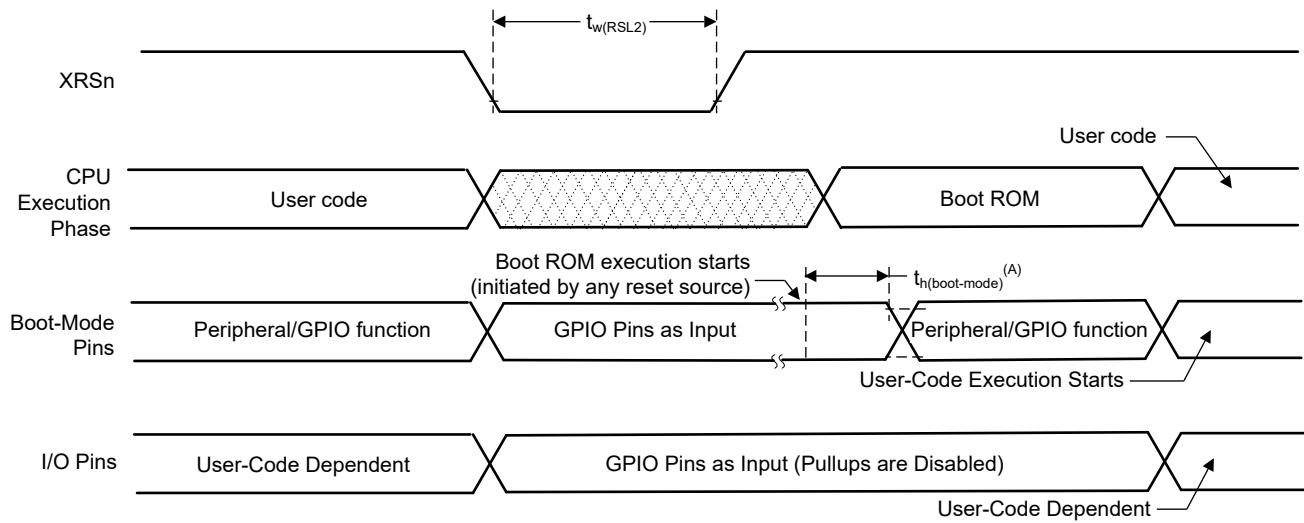
| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------------------|---|-----|-----------------------------|-----|---------------|
| $t_{w(\text{RSL1})}$ | Pulse duration, XRSn driven low by device after supplies are stable | | 100 | | μs |
| $t_{w(\text{WDRS})}$ | Pulse duration, reset pulse generated by watchdog | | $512t_{c(\text{OSCCLOCK})}$ | | cycles |
| $t_{\text{boot-flash}}$ | Boot-ROM execution time to first instruction fetch in flash | | | 1.2 | ms |

6.13.2.2.3 Reset Timing Diagrams



- The XRSn pin can be driven externally by a supervisor or an external pullup resistor, see the *Pin Attributes* table. On-chip monitors will hold this pin low until the supplies are in a valid range.
- After reset from any source (see the *Reset Sources* section), the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-6. Power-on Reset



- A. After reset from any source (see the *Reset Sources* section), the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLK speed. The SYSCLK will be based on user environment and could be with or without PLL enabled.

Figure 6-7. Warm Reset

ADVANCE INFORMATION

6.13.3 Clock Specifications

6.13.3.1 Clock Sources

Table 6-4. Possible Reference Clock Sources

| CLOCK SOURCE | DESCRIPTION |
|------------------------|---|
| INTOSC1 | Internal oscillator 1. 10-MHz internal oscillator. |
| INTOSC2 ⁽¹⁾ | Internal oscillator 2. 10-MHz internal oscillator. |
| X1 (XTAL) | External crystal or resonator connected between the X1 and X2 pins or single-ended clock connected to the X1 pin. |

(1) On reset, internal oscillator 2 (INTOSC2) is the default clock source for the PLL (OSCCLK).

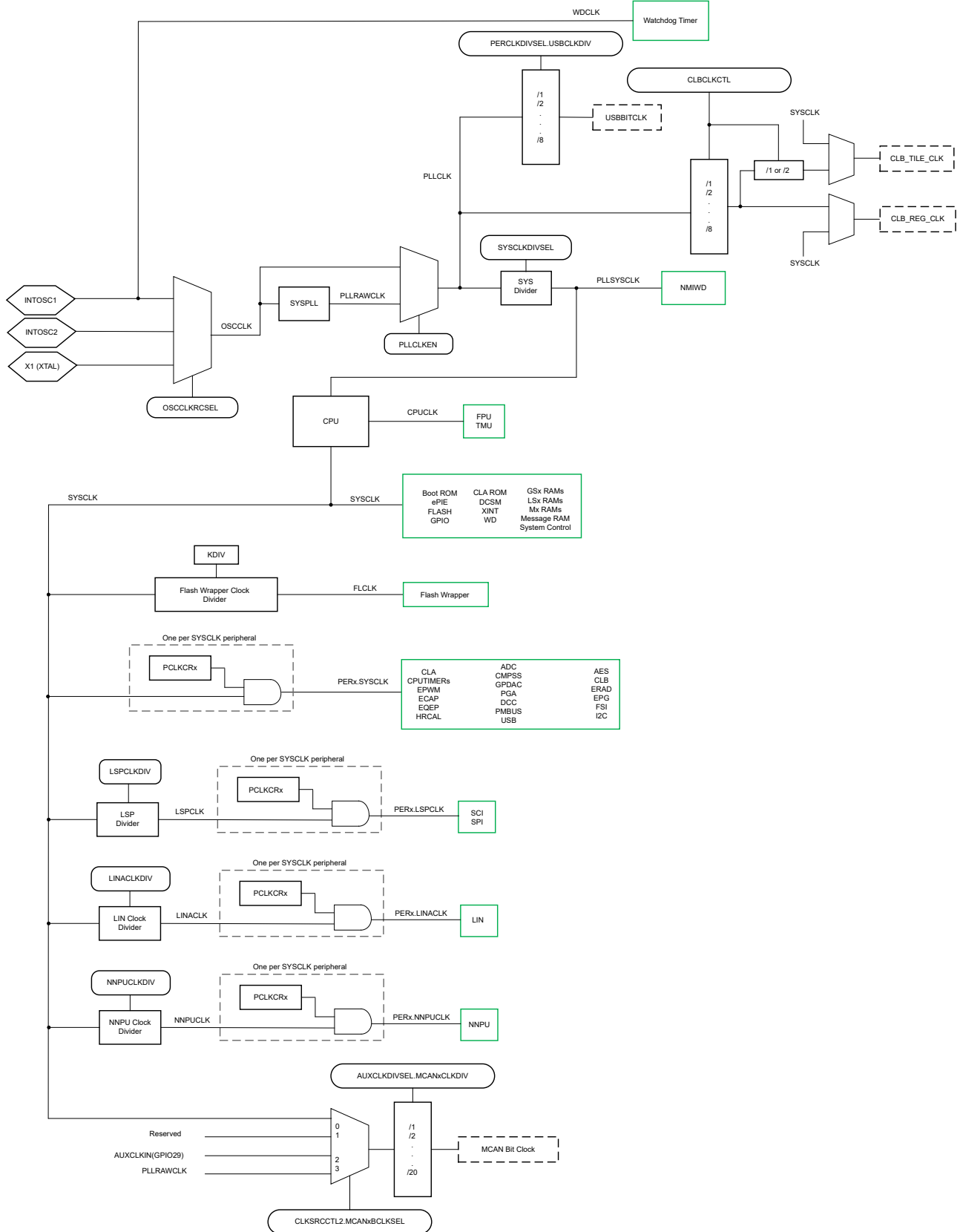


Figure 6-8. Clocking System

SYSPLL

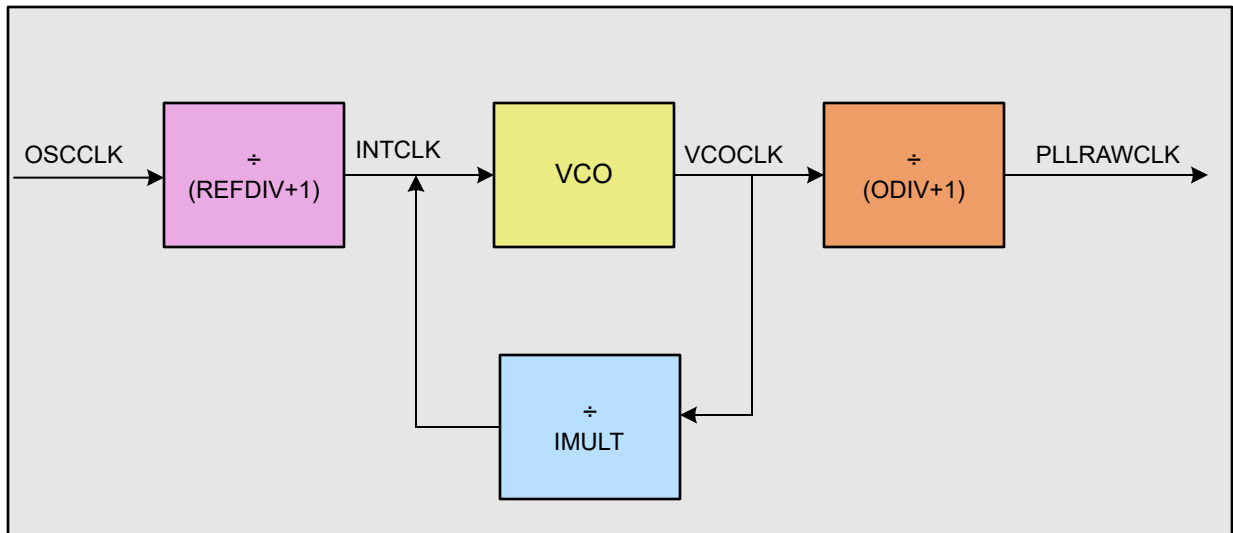


Figure 6-9. System PLL

In the *System PLL* figure,

$$f_{PLLRAWCLK} = \frac{f_{OSCCLK}}{(REFDIV + 1)} \times \frac{IMULT}{(ODIV + 1)} \quad (1)$$

6.13.3.2 Clock Frequencies, Requirements, and Characteristics

This section provides the frequencies and timing requirements of the input clocks, PLL lock times, frequencies of the internal clocks, and the frequency and switching characteristics of the output clock.

6.13.3.2.1 Input Clock Frequency and Timing Requirements, PLL Lock Times

6.13.3.2.1.1 Input Clock Frequency

| | | MIN | MAX | UNIT |
|--------------|--|-----|-----|------|
| $f_{(XTAL)}$ | Frequency, X1/X2, from external crystal or resonator | 10 | 20 | MHz |
| $f_{(X1)}$ | Frequency, X1, from external oscillator | 10 | 25 | MHz |

6.13.3.2.1.2 XTAL Oscillator Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|-------------|--------------------------------|------------------|-----|------------------|------|
| X1 V_{IL} | Valid low-level input voltage | -0.3 | | $0.3 * V_{DDIO}$ | V |
| X1 V_{IH} | Valid high-level input voltage | $0.7 * V_{DDIO}$ | | $V_{DDIO} + 0.3$ | V |

6.13.3.2.1.3 X1 Input Level Characteristics When Using an External Clock Source - Not a Crystal

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|-------------|---|------------------|------------------|------|
| X1 V_{IL} | Valid low-level input voltage (Buffer) | -0.3 | $0.3 * V_{DDIO}$ | V |
| X1 V_{IH} | Valid high-level input voltage (Buffer) | $0.7 * V_{DDIO}$ | $V_{DDIO} + 0.3$ | V |

6.13.3.2.1.4 X1 Timing Requirements

| | | MIN | MAX | UNIT |
|--------------|--|-----|-----|------|
| $t_{f(X1)}$ | Fall time, X1 | | 6 | ns |
| $t_{r(X1)}$ | Rise time, X1 | | 6 | ns |
| $t_{w(X1L)}$ | Pulse duration, X1 low as a percentage of $t_{c(X1)}$ | | 45% | 55% |
| $t_{w(X1H)}$ | Pulse duration, X1 high as a percentage of $t_{c(X1)}$ | | 45% | 55% |

6.13.3.2.1.5 AUXCLKIN Timing Requirements

| | | MIN | MAX | UNIT |
|---------------|---|-----|-----|------|
| $t_{f(AUXI)}$ | Fall time, AUXCLKIN | | 6 | ns |
| $t_{r(AUXI)}$ | Rise time, AUXCLKIN | | 6 | ns |
| $t_{w(AUXL)}$ | Pulse duration, AUXCLKIN low as a percentage of $t_{c(XCI)}$ | | 45% | 55% |
| $t_{w(AUXH)}$ | Pulse duration, AUXCLKIN high as a percentage of $t_{c(XCI)}$ | | 45% | 55% |

6.13.3.2.1.6 APLL Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | TYP | MAX | UNIT |
|----------------------------------|-----|--|-----|------|
| PLL Lock time | | | | |
| SYS PLL Lock Time ⁽¹⁾ | | $5\mu s + (1024 * (REFDIV + 1) * t_{c(OSCCLK)})$ | | us |

- (1) The PLL lock time here defines the typical time that takes for the PLL to lock once PLL is enabled (SYSPLLCTL1[PLLENA]=1). Additional time to verify the PLL clock using Dual Clock Comparator (DCC) is not accounted here. TI recommends using the latest example software from C2000Ware for initializing the PLLs. For the system PLL, see InitSysPll() or SysCtl_setClock().

6.13.3.2.1.7 XCLKOUT Switching Characteristics - PLL Bypassed or Enabled

over recommended operating conditions (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|------------------------------|---------------|---------------|------|
| $t_{f(XCO)}$ | Fall time, XCLKOUT | | 6 | ns |
| $t_{r(XCO)}$ | Rise time, XCLKOUT | | 6 | ns |
| $t_{w(XCOL)}$ | Pulse duration, XCLKOUT low | $H - 2^{(2)}$ | $H + 2^{(2)}$ | ns |
| $t_{w(XCOH)}$ | Pulse duration, XCLKOUT high | $H - 2^{(2)}$ | $H + 2^{(2)}$ | ns |
| $f_{(XCO)}$ | Frequency, XCLKOUT | | 50 | MHz |

(1) A load of 6 pF is assumed for these parameters.

(2) $H = 0.5t_{c(XCO)}$

6.13.3.2.1.8 Internal Clock Frequencies

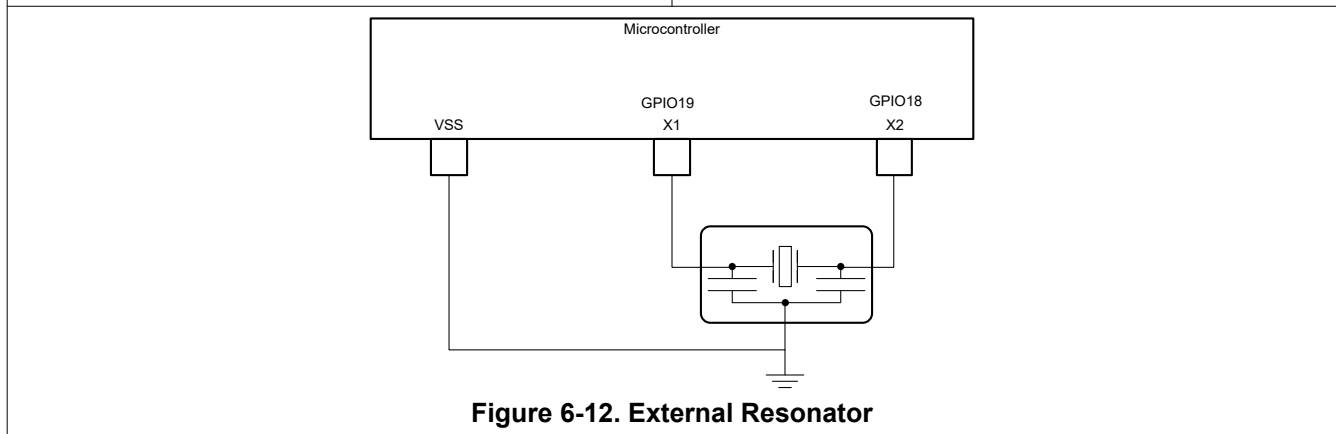
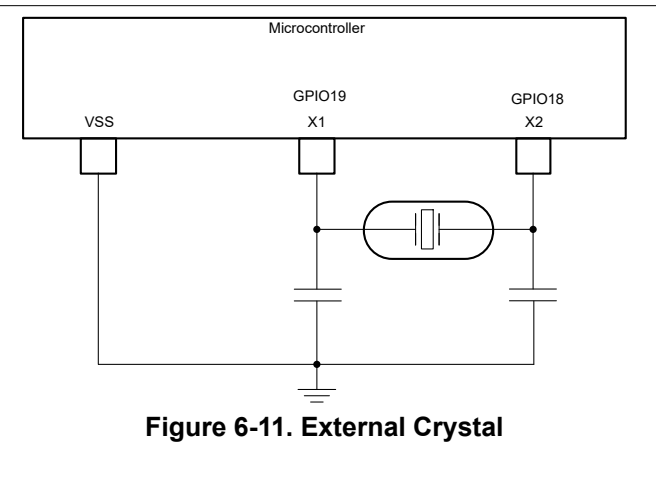
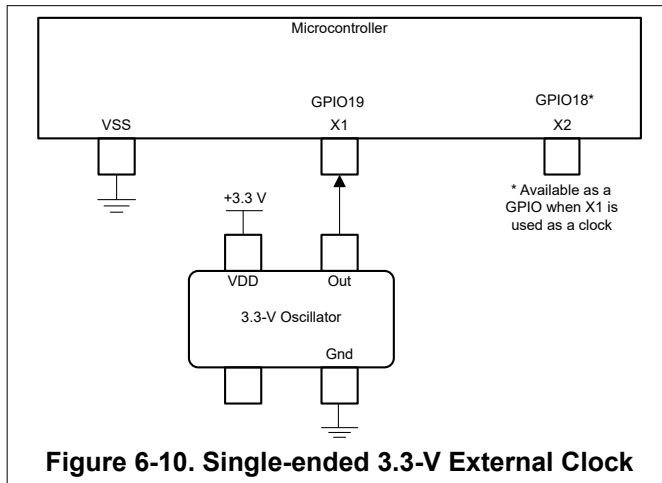
| | | MIN | NOM | MAX | UNIT |
|-------------------|--|------|----------------------|-----|------|
| $f_{(SYSCLK)}$ | Frequency, device (system) clock | 2 | | 150 | MHz |
| $t_{c(SYSCLK)}$ | Period, device (system) clock | 6.67 | | 500 | ns |
| $f_{(INTCLK)}$ | Frequency, system PLL going into VCO (after REFDIV) | 2 | | 20 | MHz |
| $f_{(VCOCLK)}$ | Frequency, system PLL VCO (before ODIV) | 220 | | 600 | MHz |
| $f_{(PLLRAWCLK)}$ | Frequency, system PLL output (before SYSCLK divider) | 6 | | 300 | MHz |
| $f_{(PLL)}$ | Frequency, PLLSYSCLK | 2 | | 150 | MHz |
| $f_{(PLL_LIMP)}$ | Frequency, PLL Limp Frequency ⁽¹⁾ | | $45/(ODIV+1)$ | | MHz |
| $f_{(LSP)}$ | Frequency, LSPCLK | 2 | | 150 | MHz |
| $t_{c(LSPCLK)}$ | Period, LSPCLK | 6.67 | | 500 | ns |
| $f_{(OSCCLK)}$ | Frequency, OSCCLK (INTOSC1 or INTOSC2 or XTAL or X1) | | See respective clock | | MHz |
| $f_{(EPWM)}$ | Frequency, EPWMCLK | | | 150 | MHz |
| $f_{(HRPWM)}$ | Frequency, HRPWMCLK | 60 | | 150 | MHz |

(1) PLL output frequency when OSCCLK is dead (Loss of OSCCLK causes PLL to Limp).

6.13.3.3 Input Clocks and PLLs

In addition to the internal 0-pin oscillators, three types of external clock sources are supported:

- A single-ended 3.3-V external clock. The clock signal should be connected to X1, as shown in [Figure 6-10](#), with the XTALCR.SE bit set to 1.
- An external crystal. The crystal should be connected across X1 and X2 with its load capacitors connected to VSS as shown in [Figure 6-11](#).
- An external resonator. The resonator should be connected across X1 and X2 with its ground connected to VSS as shown in [Figure 6-12](#).



6.13.3.4 XTAL Oscillator

6.13.3.4.1 Introduction

The crystal oscillator in this device is an embedded electrical oscillator that, when paired with a compatible quartz crystal (or a ceramic resonator), can generate the system clock required by the device.

6.13.3.4.2 Overview

The following sections describe the components of the electrical oscillator and crystal.

6.13.3.4.2.1 Electrical Oscillator

The electrical oscillator in this device is a Pierce oscillator. It is a positive feedback inverter circuit that requires a tuning circuit in order to oscillate. When this oscillator is paired with a compatible crystal, a tank circuit is formed. This tank circuit oscillates at the fundamental frequency of the crystal. On this device, the oscillator is designed to operate in parallel resonance mode due to the shunt capacitor (C0) and required load capacitors (CL). [Figure 6-13](#) illustrates the components of the electrical oscillator and the tank circuit.

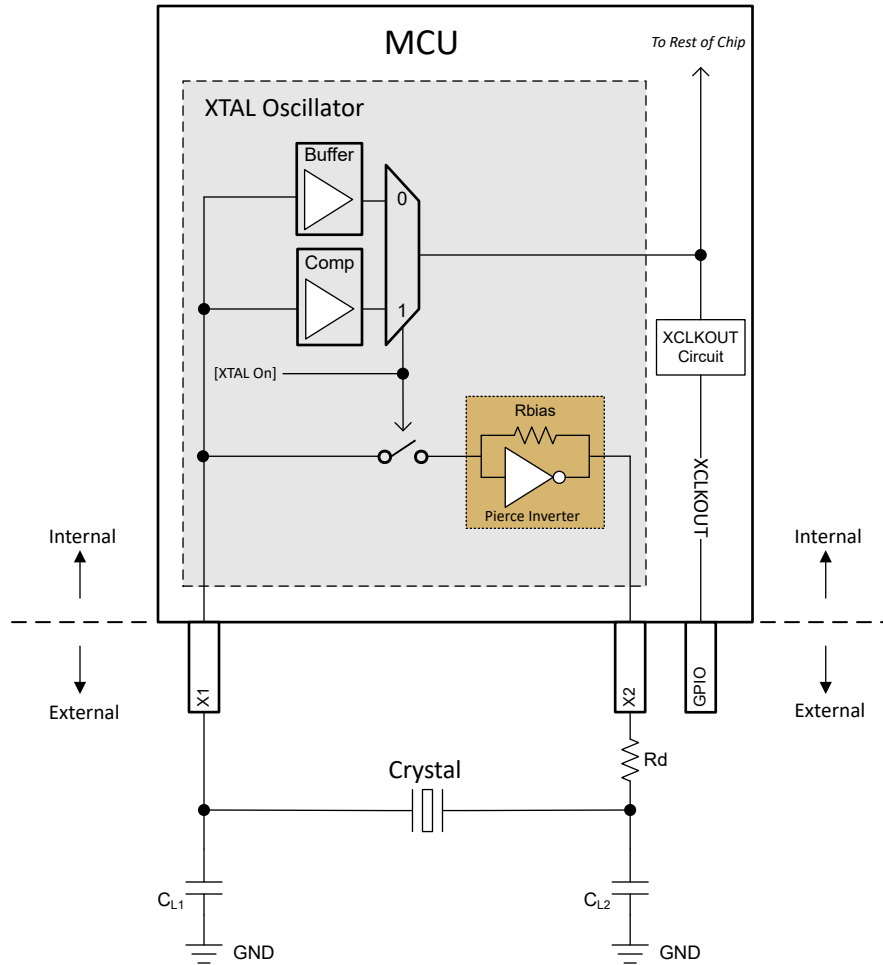


Figure 6-13. Electrical Oscillator Block Diagram

6.13.3.4.2.1.1 Modes of Operation

The electrical oscillator in this device has two modes of operation: crystal mode and single-ended mode.

6.13.3.4.2.1.1.1 Crystal Mode of Operation

In the crystal mode of operation, a quartz crystal with load capacitors has to be connected to X1 and X2.

This mode of operation is engaged when $[XTAL\ On] = 1$, which is achieved by setting $XTALCR.OSCOFF = 0$ and $XTALCR.SE = 0$. There is an internal bias resistor for the feedback loop so an external one should not be used. Adding an external bias resistor will create a parallel resistance with the internal R_{bias} , moving the bias point of operation and possibly leading to clipped waveforms, out-of-specification duty cycle, and reduction in the effective negative resistance.

In this mode of operation, the resultant clock on X1 is passed through a comparator (Comp) to the rest of the chip. The clock on X1 needs to meet the V_{IH} and V_{IL} of the comparator. See the *XTAL Oscillator Characteristics* table for the V_{IH} and V_{IL} requirements of the comparator.

6.13.3.4.2.1.1.2 Single-Ended Mode of Operation

In the single-ended mode of operation, a clock signal is connected to X1 with X2 left unconnected. A quartz crystal should not be used in this mode.

This mode is enabled when $[XTAL\ On] = 0$, which can be achieved by setting $XTALCR.OSCOFF = 1$ and $XTALCR.SE = 1$.

In this mode of operation, the clock on X1 is passed through a buffer (Buffer) to the rest of the chip. See the *X1 Input Level Characteristics When Using an External Clock Source (Not a Crystal)* table for the input requirements of the buffer.

6.13.3.4.2.1.2 XTAL Output on XCLKOUT

The output of the electrical oscillator that is fed to the rest of the chip can be brought out on XCLKOUT for observation by configuring the CLKSRCCTL3.XCLKOUTSEL and XCLKOUTDIVSEL.XCLKOUTDIV registers. See the *GPIO Muxed Pins* table for a list of GPIOs that XCLKOUT comes out on.

6.13.3.4.2.2 Quartz Crystal

Electrically, a quartz crystal can be represented by an LCR (Inductor-Capacitor-Resistor) circuit. However, unlike an LCR circuit, crystals have very high Q due to the low motional resistance and are also very underdamped. Components of the crystal are shown in [Figure 6-14](#) and explained below.

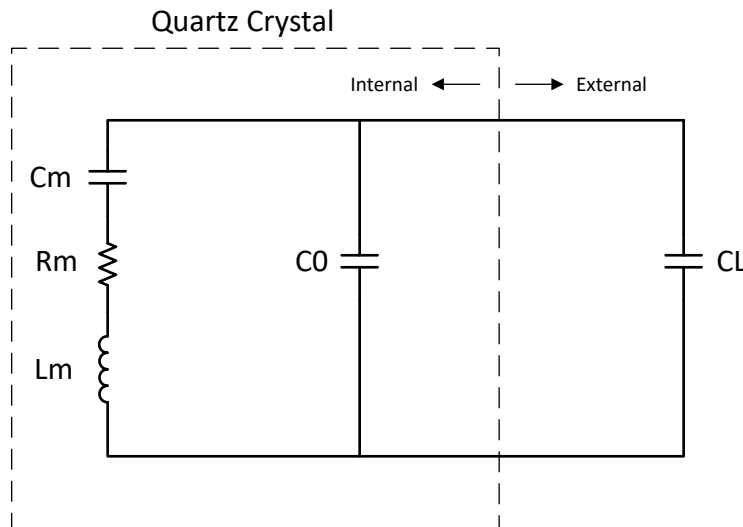


Figure 6-14. Crystal Electrical Representation

Cm (Motional capacitance): Denotes the elasticity of the crystal.

Rm (Motional resistance): Denotes the resistive losses within the crystal. This is not the ESR of the crystal but can be approximated as such depending on the values of the other crystal components.

Lm (Motional inductance): Denotes the vibrating mass of the crystal.

C0 (Shunt capacitance): The capacitance formed from the two crystal electrodes and stray package capacitance.

CL (Load capacitance): This is the effective capacitance seen by the crystal at its electrodes. It is external to the crystal. The frequency ppm specified in the crystal data sheet is usually tied to the CL parameter.

Note that most crystal manufacturers specify CL as the effective capacitance seen at the crystal pins, while some crystal manufacturers specify CL as the capacitance on just one of the crystal pins. Check with the crystal manufacturer for how the CL is specified in order to use the correct values in calculations.

From [Figure 6-13](#), CL1 and CL2 are in series; so, to find the equivalent total capacitance seen by the crystal, the capacitance series formula has to be applied which simply evaluates to $[CL1]/2$ if $CL1 = CL2$.

It is recommended that a stray PCB capacitance be added to this value. 3 pF to 5 pF are reasonable estimates, but the actual value will depend on the PCB in question.

Note that the load capacitance is a requirement of both the electrical oscillator and crystal. The value chosen has to satisfy both the electrical oscillator and the crystal.

The effect of CL on the crystal is frequency-pulling. If the effective load capacitance is lower than the target, the crystal frequency will increase and vice versa. However, the effect of frequency-pulling is usually very minimal and typically results in less than 10-ppm variation from the nominal frequency.

6.13.3.4.2.3 GPIO Modes of Operation

On this device, X1 and X2 can be used as GPIO19 and GPIO18, respectively, depending on the operating mode of the XTAL. Refer to the *External Oscillator (XTAL)* section of the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#).

6.13.3.4.3 Functional Operation

6.13.3.4.3.1 ESR – Effective Series Resistance

Effective Series Resistance is the resistive load the crystal presents to the electrical oscillator at resonance. The higher the ESR, the lower the Q, and less likely the crystal will start up or maintain oscillation. The relationship between ESR and the crystal components is indicated below.

$$ESR = R_m * \left(1 + \frac{C_0}{CL}\right)^2 \quad (2)$$

Note that ESR is not the same as motional resistance of the crystal, but can be approximated as such if the effective load capacitance is much greater than the shunt capacitance.

6.13.3.4.3.2 Rneg – Negative Resistance

Negative resistance is the impedance presented by the electrical oscillator to the crystal. It is the amount of energy the electrical oscillator must supply to the crystal to overcome the losses incurred during oscillation. Rneg depicts a circuit that provides rather than consume energy and can also be viewed as the overall gain of the circuit.

The generally accepted practice is to have Rneg > 3x ESR to 5x ESR to ensure the crystal starts up under all conditions. Note that it takes slightly more energy to start up the crystal than it does to sustain oscillation; therefore, if it can be ensured that the negative resistance requirement is met at start-up, then oscillation sustenance will not be an issue.

[Figure 6-15](#) and [Figure 6-16](#) show the variation between negative resistance and the crystal components for this device. As can be seen from the graphs, the crystal shunt capacitance (C0) and effective load capacitance (CL) greatly influence the negative resistance of the electrical oscillator. Note that these are typical graphs; so, refer to [Table 6-5](#) for minimum and maximum values for design considerations.

6.13.3.4.3.3 Start-up Time

Start-up time is an important consideration when selecting the components of the crystal circuit. As mentioned in the [Rneg – Negative Resistance](#) section, for reliable start-up across all conditions, it is recommended that the Rneg > 3x ESR to 5x ESR of the crystal.

Crystal ESR and the dampening resistor (Rd) greatly affect the start-up time. The higher the two values, the longer the crystal takes to start up. Longer start-up times are usually a sign that the crystal and components are not a correct match.

Refer to [Crystal Oscillator Specifications](#) for the typical start-up times. Note that the numbers specified here are typical numbers provided for guidance only. Actual start-up time depends heavily on the crystal in question and the external components.

6.13.3.4.3.3.1 X1/X2 Precondition

On this device, the GPIO19/18 alternate functionality on X1/X2 can be used to speed up the start-up time of the crystal if needed. This functionality is achieved by preconditioning the load capacitors CL1 and CL2 to a known state before the XTAL is turned on. See the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#) for details.

6.13.3.4.3.4 DL – Drive Level

Drive level refers to how much power is provided by the electrical oscillator and dissipated by the crystal. The maximum drive level specified in the crystal manufacturer's data sheet is usually the maximum the crystal can dissipate without damage or significant reduction in operating life. On the other hand, the drive level specified by the electrical oscillator is the maximum power it can provide. The actual power provided by the electrical oscillator is not necessarily the maximum power and depends on the crystal and board components.

For cases where the actual drive level from the electrical oscillator exceeds the maximum drive level specification of the crystal, a dampening resistor (R_d) should be installed to limit the current and reduce the power dissipated by the crystal. Note that R_d reduces the circuit gain; and therefore, the actual value to use should be evaluated to make sure all other conditions for start-up and sustained oscillation are met.

6.13.3.4.4 How to Choose a Crystal

Using [Crystal Oscillator Specifications](#) as a reference:

- Pick a crystal frequency (for example, 20 MHz).
- Check that the ESR of the crystal $\leq 50 \Omega$ per specifications for 20 MHz.
- Check that the load capacitance requirement of the crystal manufacturer is within 6 pF and 12 pF per specifications for 20 MHz.
 - As mentioned, CL_1 and CL_2 are in series; so, provided $CL_1 = CL_2$, effective load capacitance $CL = [CL_1]/2$.
 - Adding board parasitics to this results in $CL = [CL_1]/2 + C_{stray}$
- Check that the maximum drive level of the crystal ≥ 1 mW. If this requirement is not met, a dampening resistor R_d can be used. Refer to [DL – Drive Level](#) on other points to consider when using R_d .

6.13.3.4.5 Testing

It is recommended that the user have the crystal manufacturer completely characterize the crystal with their board to ensure the crystal always starts up and maintains oscillation.

Below is a brief overview of some measurements that can be performed:

Due to how sensitive the crystal circuit is to capacitance, it is recommended that scope probes not be connected to X1 and X2. If scope probes must be used to monitor X1/X2, an active probe with less than 1-pF input capacitance should be used.

Frequency

- Bring out the XTAL on XCLKOUT.
- Measure this frequency as the crystal frequency.

Negative Resistance

- Bring out the XTAL on XCLKOUT.
- Place a potentiometer in series with the crystal between the load capacitors.
- Increase the resistance of the potentiometer until the clock on XCLKOUT stops.
- This resistance plus the crystal's actual ESR is the negative resistance of the electrical oscillator.

Start-Up Time

- Turn off the XTAL.
- Bring out the XTAL on XCLKOUT.
- Turn on the XTAL and measure how long it takes the clock on XCLKOUT to stay within 45% and 55% duty cycle.

6.13.3.4.6 Common Problems and Debug Tips

Crystal Fails to Start Up

- Go through the [How to Choose a Crystal](#) section and make sure there are no violations.

Crystal Takes a Long Time to Start Up

- If a dampening resistor R_d is installed, it is too high.
- If no dampening resistor is installed, either the crystal ESR is too high or the overall circuit gain is too low due to high load capacitance.

6.13.3.4.7 Crystal Oscillator Specifications

6.13.3.4.7.1 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------|--|-----|-----|-----|------|
| Start-up time ⁽¹⁾ | f = 10 MHz | ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 4 | | ms |
| | f = 20 MHz | ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 2 | | ms |
| Crystal drive level (DL) | | | | | 1 | mW |

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.13.3.4.7.2 Crystal Equivalent Series Resistance (ESR) Requirements

For the [Crystal Equivalent Series Resistance \(ESR\) Requirements](#) table:

1. Crystal shunt capacitance (C0) should be less than or equal to 7 pF.
2. $ESR = \text{Negative Resistance}/3$

Table 6-5. Crystal Equivalent Series Resistance (ESR) Requirements

| CRYSTAL FREQUENCY (MHz) | MAXIMUM ESR (Ω) (CL1 = CL2 = 12 pF) | MAXIMUM ESR (Ω) (CL1 = CL2 = 24 pF) |
|-------------------------|---|---|
| 10 | 55 | 110 |
| 12 | 50 | 95 |
| 14 | 50 | 90 |
| 16 | 45 | 75 |
| 18 | 45 | 65 |
| 20 | 45 | 50 |

Negative Resistance vs. 10MHz Crystal

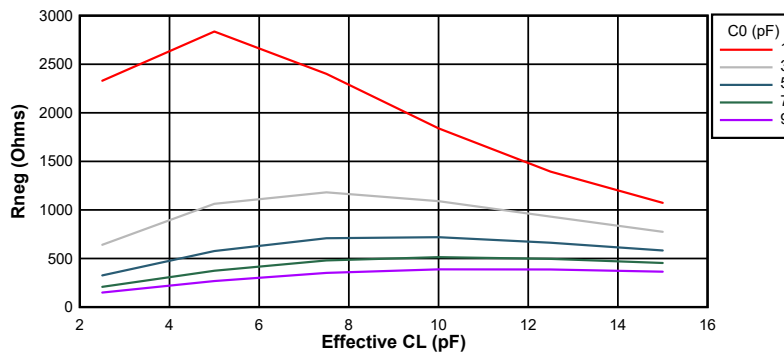


Figure 6-15. Negative Resistance Variation at 10 MHz

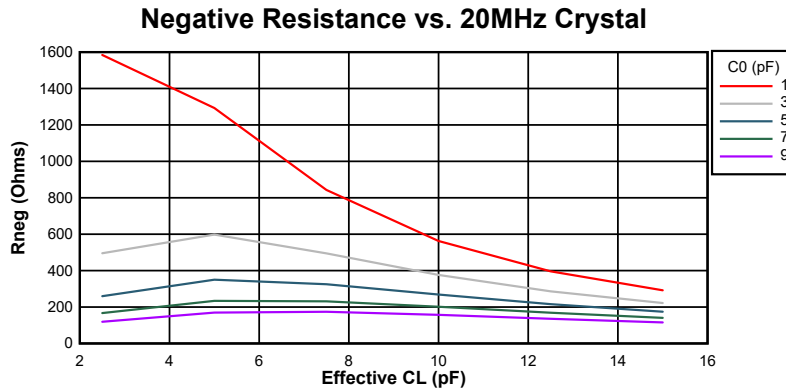


Figure 6-16. Negative Resistance Variation at 20 MHz

6.13.3.4.7.3 Crystal Oscillator Parameters

| | | MIN | MAX | UNIT |
|----------|---------------------------|-----|-----|------|
| CL1, CL2 | Load capacitance | 12 | 24 | pF |
| C0 | Crystal shunt capacitance | | 7 | pF |

6.13.3.4.7.4 Crystal Oscillator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|------------|---|-----|-----|-----|------|
| Start-up time ⁽¹⁾ | f = 10 MHz | ESR MAX = 110 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 4 | | ms |
| | f = 20 MHz | ESR MAX = 50 Ω CL1 = CL2 = 24 pF C0 = 7 pF | | 2 | | ms |
| Crystal drive level (DL) | | | | | 1 | mW |

(1) Start-up time is dependent on the crystal and tank circuit components. TI recommends that the crystal vendor characterize the application with the chosen crystal.

6.13.3.5 Internal Oscillators

To reduce production board costs and application development time, all devices contain two independent internal oscillators, referred to as INTOSC1 and INTOSC2. By default, INTOSC2 is set as the source for the system reference clock (OSCCLK) and INTOSC1 is set as the backup clock source.

Applications requiring tighter **SCI baud rate matching** can use the SCI baud tuning example (baud_tune_via_uart) available in C2000Ware.

6.13.3.5.1 INTOSC Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | PART | PACKAGE SUFFIX | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------|---|------|----------------|-------------------|--------------|-----|-------------|------|
| f _{INTOSC} | Frequency, INTOSC1 and INTOSC2 ⁽¹⁾ | All | All | -40°C to 125°C | 9.82 (-1.8%) | 10 | 10.1 (1.0%) | MHz |
| | | | | -30°C to 90°C | 9.86 (-1.4%) | 10 | 10.1 (1.0%) | |
| | | | | -10°C to 85°C | 9.9 (-1.0%) | 10 | 10.1 (1.0%) | |
| f _{INTOSC-STABILITY} | Frequency stability at room temperature | All | All | 30°C, Nominal VDD | ±0.1 | | % | |
| t _{INTOSC-ST} | Start-up and settling time | All | All | | 20 | | µs | |

- (1) INTOSC frequency may shift due to the thermal and mechanical stress of solder reflow. A post-reflow bake can restore the unit to its original data sheet performance.

6.13.4 Flash Parameters

Table 6-6 lists the minimum required Flash wait states with different clock sources and frequencies. Wait state is the value set in register FRDCNTL[RWAIT].

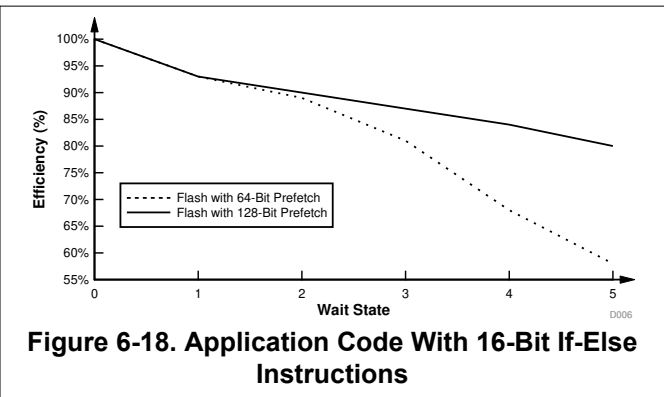
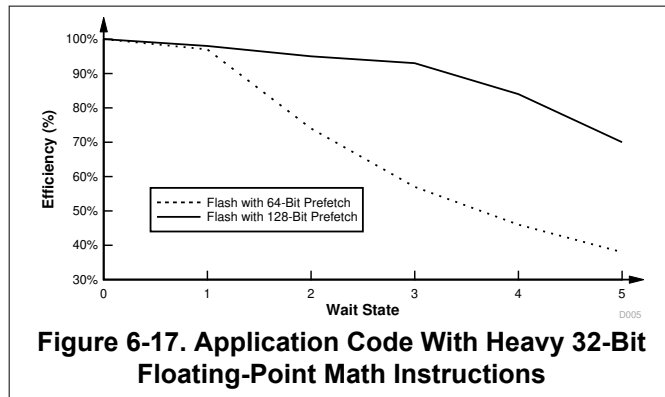
Table 6-6. Minimum Required Flash Wait States with Different Clock Sources and Frequencies

| CPUCLK (MHz) | Wait States (FRDCNTL[RWAIT] ⁽¹⁾) |
|--------------------|--|
| 120 < CPUCLK ≤ 150 | 3 |
| 80 < CPUCLK ≤ 120 | 2 |
| 0 < CPUCLK ≤ 80 | 1 |

(1) Minimum required FRDCNTL[RWAIT] is 1, RWAIT=0 is not supported.

The F28P55x devices have a 128-bit prefetch buffer that provides high flash code execution efficiency across wait states. Figure 6-17 and Figure 6-18 illustrate typical efficiency across wait-state settings compared to previous-generation devices with a 64-bit prefetch buffer. Wait-state execution efficiency with a prefetch buffer will depend on how many branches are present in application software. Two examples of linear code and if-then-else code are provided.

ADVANCE INFORMATION



Note

The Main Array flash programming must be aligned to 64-bit address boundaries and each 64-bit word may only be programmed once per write/erase cycle.

6.13.4.1 Flash Parameters

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---|-----------------------------|-----|------|--------|--------|
| Program Time ⁽¹⁾ | 128 data bits + 16 ECC bits | | 62.5 | 625 | μs |
| | 2KB (Sector) | | 8 | 80 | μs |
| Erase Time ^{(2) (3)} at < 25 cycles | 2KB (Sector) | | 15 | 55 | ms |
| | 64KB | | 17 | 61 | ms |
| | 128KB | | 18 | 66 | ms |
| | 256KB | | 21 | 78 | ms |
| Erase Time ^{(2) (3)} at 1000 cycles | 2KB (Sector) | | 25 | 130 | ms |
| | 64KB | | 28 | 143 | ms |
| | 128KB | | 30 | 157 | ms |
| | 256KB | | 35 | 183 | ms |
| Erase Time ^{(2) (3)} at 2000 cycles | 2KB (Sector) | | 30 | 221 | ms |
| | 64KB | | 33 | 243 | ms |
| | 128KB | | 36 | 265 | ms |
| | 256KB | | 42 | 310 | ms |
| Erase Time ^{(2) (3)} at 20K cycles | 2KB (Sector) | | 120 | 1003 | ms |
| | 64KB | | 132 | 1102 | ms |
| | 128KB | | 145 | 1205 | ms |
| | 256KB | | 169 | 1410 | ms |
| N_{wec} Write/Erase Cycles per Bank ⁽⁴⁾ | | | | 100000 | cycles |
| $t_{retention}$ Data retention duration at $T_J = 85^\circ\text{C}$ | | 20 | | | years |

- (1) Program time is at the maximum device frequency. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:
- Code that uses flash API to program the flash
 - Flash API itself
 - Flash data to be programmed
- In other words, the time indicated in this table is applicable after all the required code/data is available in the device RAM, ready for programming. The transfer time will significantly vary depending on the speed of the JTAG debug probe used. Program time calculation is based on programming 144 bits at a time at the specified operating frequency. Program time includes Program verify by the CPU. The program time does not degrade with write/erase (W/E) cycling, but the erase time does. Erase time includes Erase verify by the CPU and does not involve any data transfer.
- (2) Erase time includes Erase verify by the CPU.
- (3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required prior to programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.
- (4) The combined total of bank and sector write/erase cycles is limited to this number

6.13.5 RAM Specifications

All volatile memory (RAM and ROM) on the F28P55x device is 0 Wait-state for both reads and writes, meaning the memory operates at the same speed as SYSCLK. [Table 6-7](#), [Table 6-8](#), and [Table 6-9](#) summarize the characteristics of the different RAM instances on the device.

Table 6-7. RAM Parameters – F28P55xSJ

| RAM TYPE | SIZE | FETCH TIME ⁽¹⁾ (CYCLES) | READ TIME ⁽¹⁾ (CYCLES) | STORE TIME (CYCLES) | BUS WIDTH | NUMBER OF BUSES AVAILABLE | NUMBER OF WAIT STATES | BURST ACCESS |
|------------------------|------|---------------------------------------|--------------------------------------|------------------------|------------|---------------------------|-----------------------|--------------|
| LS RAM | 64KB | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| M0 | 2KB | 2 | 2 | 1 | 16/32 bits | 1 | 0 | No |
| M1 | 2KB | 2 | 2 | 1 | 16/32 bits | 1 | 0 | No |
| GS RAM | 64KB | 2 | 2 | 1 | 16/32 bits | 3 | 0 | No |
| CLA-to-CPU Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| CPU-to-CLA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| CLA-to-DMA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 3 | 0 | No |
| DMA-to-CLA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 3 | 0 | No |

(1) Without arbitration between read/write/fetch. Access completes in 2 cycles; otherwise, arbitration priority (Write/Read/Fetch) is followed.

Table 6-8. RAM Parameters – F28P55xSG

| RAM TYPE | SIZE | FETCH TIME ⁽¹⁾ (CYCLES) | READ TIME ⁽¹⁾ (CYCLES) | STORE TIME (CYCLES) | BUS WIDTH | NUMBER OF BUSES AVAILABLE | NUMBER OF WAIT STATES | BURST ACCESS |
|------------------------|------|---------------------------------------|--------------------------------------|------------------------|------------|---------------------------|-----------------------|--------------|
| LS RAM | 64KB | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| M0 | 2KB | 2 | 2 | 1 | 16/32 bits | 1 | 0 | No |
| M1 | 2KB | 2 | 2 | 1 | 16/32 bits | 1 | 0 | No |
| GS RAM | 32KB | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| CLA-to-CPU Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| CPU-to-CLA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| CLA-to-DMA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 3 | 0 | No |
| DMA-to-CLA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 3 | 0 | No |

(1) Without arbitration between read/write/fetch. Access completes in 2 cycles; otherwise, arbitration priority (Write/Read/Fetch) is followed.

Table 6-9. RAM Parameters – F28P55xSD

| RAM TYPE | SIZE | FETCH TIME ⁽¹⁾ (CYCLES) | READ TIME ⁽¹⁾ (CYCLES) | STORE TIME (CYCLES) | BUS WIDTH | NUMBER OF BUSES AVAILABLE | NUMBER OF WAIT STATES | BURST ACCESS |
|------------------------|------|---------------------------------------|--------------------------------------|------------------------|------------|---------------------------|-----------------------|--------------|
| LS RAM | 32KB | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| M0 | 2KB | 2 | 2 | 1 | 16/32 bits | 1 | 0 | No |
| M1 | 2KB | 2 | 2 | 1 | 16/32 bits | 1 | 0 | No |
| GS RAM | 32KB | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| CLA-to-CPU Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| CPU-to-CLA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |
| CLA-to-DMA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 3 | 0 | No |
| DMA-to-CLA Message RAM | 256B | 2 | 2 | 1 | 16/32 bits | 3 | 0 | No |

(1) Without arbitration between read/write/fetch. Access completes in 2 cycles; otherwise, arbitration priority (Write/Read/Fetch) is followed.

6.13.6 ROM Specifications

All volatile memory (RAM and ROM) on the F28P55x device is 0 Wait-state for both reads and writes, meaning the memory operates at the same speed as SYSCLK. [Table 6-10](#) summarizes the aspects of the ROM instances on the device.

Table 6-10. ROM Parameters – F28P55xSJ, F28P55xSG, and F28P55xSD

| ROM TYPE | SIZE | FETCH TIME ⁽¹⁾ (CYCLES) | READ TIME ⁽¹⁾ (CYCLES) | STORE TIME (CYCLES) | BUS WIDTH | NUMBER OF BUSES AVAILABLE | NUMBER OF WAIT STATES | BURST ACCESS |
|-----------------------|------|---------------------------------------|--------------------------------------|------------------------|------------|---------------------------|-----------------------|--------------|
| Boot ROM + Secure ROM | 96KB | 2 | 2 | 1 | 16/32 bits | 1 | 0 | No |
| CLA Data ROM | 8KB | 2 | 2 | 1 | 16/32 bits | 2 | 0 | No |

(1) Without arbitration between read/write/fetch. Access completes in 2 cycles; otherwise, arbitration priority (Write/Read/Fetch) is followed.

6.13.7 Emulation/JTAG

The JTAG (IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture) port has four dedicated pins: TMS, TDI, TDO, and TCK. The cJTAG (IEEE Standard 1149.7-2009 for Reduced-Pin and Enhanced-Functionality Test Access Port and Boundary-Scan Architecture) port is a compact JTAG interface requiring only two pins (TMS and TCK), which allows other device functionality to be muxed to the traditional GPIO35 (TDI) and GPIO37 (TDO) pins.

Typically, no buffers are needed on the JTAG signals when the distance between the MCU target and the JTAG header is smaller than 6 inches (15.24 cm), and no other devices are present on the JTAG chain. Otherwise, each signal should be buffered. Additionally, for most JTAG debug probe operations at 10 MHz, no series resistors are needed on the JTAG signals. However, if high emulation speeds are expected (35 MHz or so), 22- Ω resistors should be placed in series on each JTAG signal.

The PD (Power Detect) pin of the JTAG debug probe header should be connected to the board's 3.3-V supply. Header GND pins should be connected to board ground. TDIS (Cable Disconnect Sense) should also be connected to board ground. The JTAG clock should be looped from the header TCK output pin back to the RTCK input pin of the header (to sense clock continuity by the JTAG debug probe). This MCU does not support the EMU0 and EMU1 signals that are present on 14-pin and 20-pin emulation headers. These signals should always be pulled up at the emulation header through a pair of board pullup resistors ranging from 2.2 k Ω to 4.7 k Ω (depending on the drive strength of the debugger ports). Typically, a 2.2-k Ω value is used.

Header pin $\overline{\text{RESET}}$ is an open-drain output from the JTAG debug probe header that enables board components to be reset through JTAG debug probe commands (available only through the 20-pin header). [Figure 6-19](#) shows how the 14-pin JTAG header connects to the MCU's JTAG port signals. [Figure 6-20](#) shows how to connect to the 20-pin JTAG header. The 20-pin JTAG header pins EMU2, EMU3, and EMU4 are not used and should be grounded.

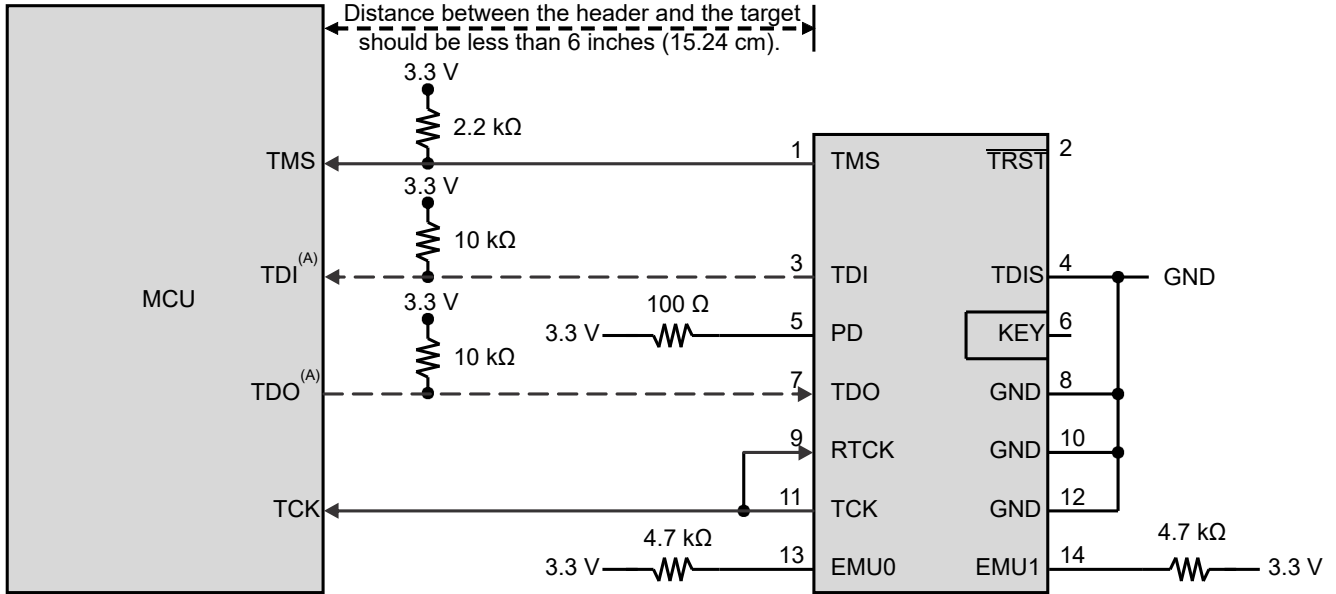
For more information about hardware breakpoints and watchpoints, see [Hardware Breakpoints and Watchpoints in CCS for C2000 devices](#).

For more information about JTAG emulation, see the [XDS Target Connection Guide](#).

Note

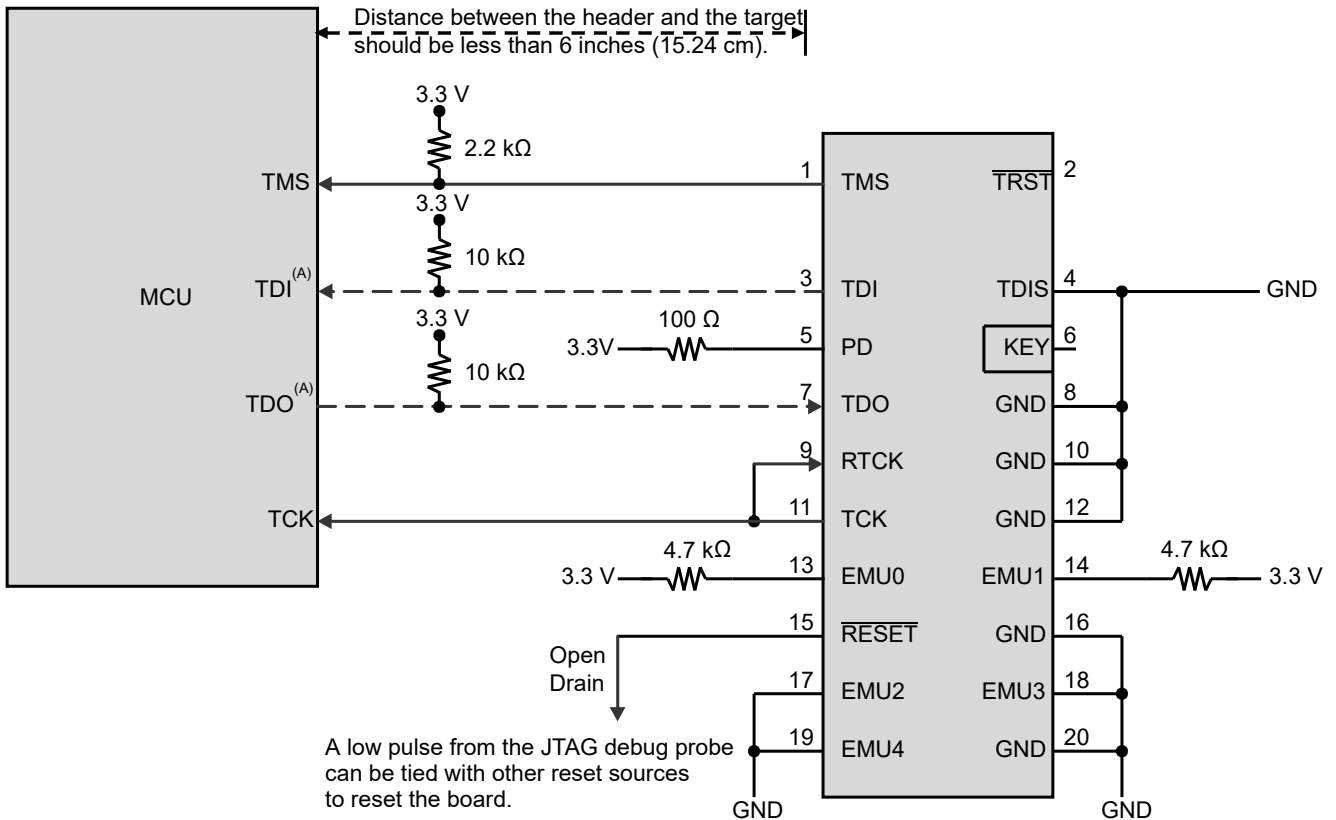
JTAG Test Data Input (TDI) is the default mux selection for the pin. The internal pullup is disabled by default. If this pin is used as JTAG TDI, the internal pullup should be enabled or an external pullup added on the board to avoid a floating input. In the cJTAG option, this pin can be used as GPIO.

JTAG Test Data Output (TDO) is the default mux selection for the pin. The internal pullup is disabled by default. The TDO function will be in a tri-state condition when there is no JTAG activity, leaving this pin floating. The internal pullup should be enabled or an external pullup added on the board to avoid a floating GPIO input. In the cJTAG option, this pin can be used as GPIO.



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-19. Connecting to the 14-Pin JTAG Header



A. TDI and TDO connections are not required for cJTAG option and these pins can be used as GPIOs instead.

Figure 6-20. Connecting to the 20-Pin JTAG Header

ADVANCE INFORMATION

6.13.7.1 JTAG Electrical Data and Timing

6.13.7.1.1 JTAG Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|---------------------------|--|-------|-----|------|
| 1 | $t_c(\text{TCK})$ | Cycle time, TCK | 66.66 | | ns |
| 1a | $t_w(\text{TCKH})$ | Pulse duration, TCK high (40% of t_c) | 26.66 | | ns |
| 1b | $t_w(\text{TCKL})$ | Pulse duration, TCK low (40% of t_c) | 26.66 | | ns |
| 3 | $t_{su}(\text{TDI-TCKH})$ | Input setup time, TDI valid to TCK high | 7 | | ns |
| | $t_{su}(\text{TMS-TCKH})$ | Input setup time, TMS valid to TCK high | 7 | | |
| 4 | $t_h(\text{TCKH-TDI})$ | Input hold time, TDI valid from TCK high | 7 | | ns |
| | $t_h(\text{TCKH-TMS})$ | Input hold time, TMS valid from TCK high | 7 | | |

6.13.7.1.2 JTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|------------------------|-----|-----|------|
| 2 | $t_d(\text{TCKL-TDO})$ | 6 | 20 | ns |

6.13.7.1.3 JTAG Timing Diagram

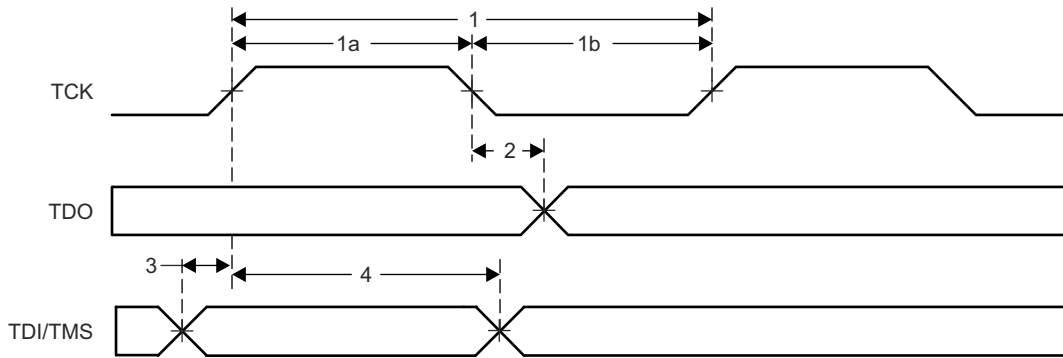


Figure 6-21. JTAG Timing

6.13.7.2 cJTAG Electrical Data and Timing

6.13.7.2.1 cJTAG Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|---------------------------|--|-----|-----|------|
| 1 | $t_c(\text{TCK})$ | Cycle time, TCK | 100 | | ns |
| 1a | $t_w(\text{TCKH})$ | Pulse duration, TCK high (40% of t_c) | 40 | | ns |
| 1b | $t_w(\text{TCKL})$ | Pulse duration, TCK low (40% of t_c) | 40 | | ns |
| 3 | $t_{su}(\text{TMS-TCKH})$ | Input setup time, TMS valid to TCK high | 7 | | ns |
| | $t_{su}(\text{TMS-TCKL})$ | Input setup time, TMS valid to TCK low | 7 | | ns |
| 4 | $t_h(\text{TCKH-TMS})$ | Input hold time, TMS valid from TCK high | 2 | | ns |
| | $t_h(\text{TCKL-TMS})$ | Input hold time, TMS valid from TCK low | 2 | | ns |

6.13.7.2.2 cJTAG Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | MIN | MAX | UNIT |
|-----|----------------------------|-----|-----|------|
| 2 | $t_d(\text{TCKL-TMS})$ | 6 | 20 | ns |
| 5 | $t_{dis}(\text{TCKH-TMS})$ | | 20 | ns |

6.13.7.2.3 cJTAG Timing Diagram

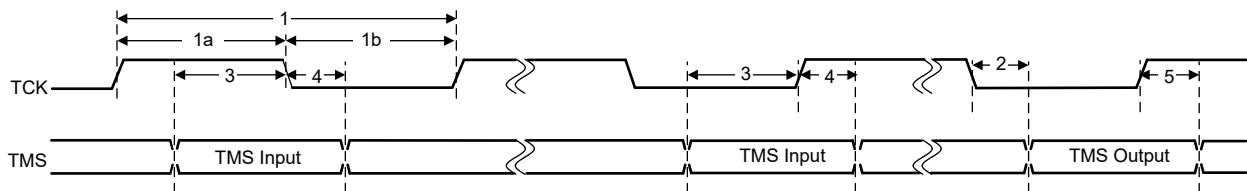


Figure 6-22. cJTAG Timing

6.13.8 GPIO Electrical Data and Timing

The peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. On reset, GPIO pins are configured as inputs. For specific inputs, the user can also select the number of input qualification cycles to filter unwanted noise glitches.

The GPIO module contains an Output X-BAR which allows an assortment of internal signals to be routed to a GPIO in the GPIO mux positions denoted as OUTPUTXBARx. The GPIO module also contains an Input X-BAR which is used to route signals from any GPIO input to different IP blocks such as the ADCs, eCAPs, ePWMs, and external interrupts. For more details, see the X-BAR chapter in the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#).

6.13.8.1 GPIO – Output Timing

6.13.8.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | | MIN | MAX | UNIT |
|--------------|---------------------------------------|----------------------------|-----|------------------|------|
| $t_{r(GPO)}$ | Rise time, GPIO switching low to high | All GPIOs | | 6 ⁽¹⁾ | ns |
| $t_{f(GPO)}$ | Fall time, GPIO switching high to low | All GPIOs | | 6 ⁽¹⁾ | ns |
| f_{rGPO} | Toggling frequency, GPIO pins | All GPIOs not listed below | | 50 | MHz |
| | | GPIO 2, 3, 9, and 32 | | 40 | |
| | | GPIO 23 and 41 | | 25 | |

(1) Rise time and fall time vary with load. These values assume a 6-pF load.

6.13.8.1.2 General-Purpose Output Timing Diagram

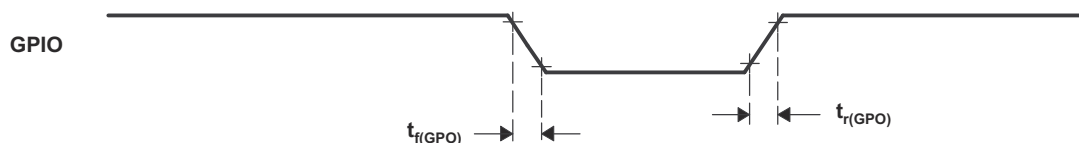


Figure 6-23. General-Purpose Output Timing

6.13.8.2 GPIO – Input Timing

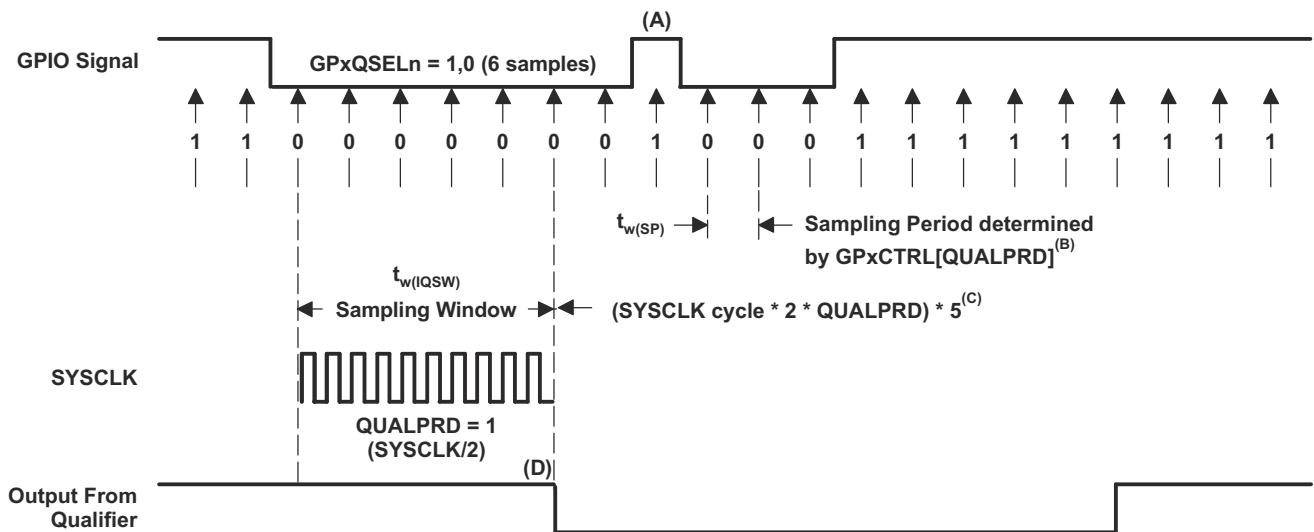
6.13.8.2.1 General-Purpose Input Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------------|---------------------------------|----------------------|--|-----|--------|
| $t_{w(SP)}$ | Sampling period | QUALPRD = 0 | $1t_{c(SYSCLK)}$ | | cycles |
| | | QUALPRD \neq 0 | $2t_{c(SYSCLK)} * QUALPRD$ | | cycles |
| $t_{w(IQSW)}$ | Input qualifier sampling window | | $t_{w(SP)} * (n^{(1)} - 1)$ | | cycles |
| $t_{w(GPI)}^{(2)}$ | Pulse duration, GPIO low/high | Synchronous mode | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCLK)}$ | | cycles |

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.

(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active low signal and V_{IH} to V_{IH} for an active high signal.

6.13.8.2.2 Sampling Mode



- A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. It can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is 1 SYSCLK cycle. For any other value "n", the qualification sampling period is 2n SYSCLK cycles (that is, at every 2n SYSCLK cycles, the GPIO pin will be sampled).
- B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
- C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
- D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLK cycles or greater. In other words, the inputs should be stable for $(5 \times QUALPRD \times 2)$ SYSCLK cycles. This would ensure 5 sampling periods for detection to occur. Because external signals are driven asynchronously, a 13-SYSCLK-wide pulse ensures reliable recognition.

Figure 6-24. Sampling Mode

6.13.8.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLK.

Sampling frequency = $\text{SYSCLK} / (2 \times \text{QUALPRD})$, if $\text{QUALPRD} \neq 0$

Sampling frequency = SYSCLK , if $\text{QUALPRD} = 0$

Sampling period = $\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}$, if $\text{QUALPRD} \neq 0$

In the previous equations, SYSCLK cycle indicates the time period of SYSCLK.

Sampling period = SYSCLK cycle , if $\text{QUALPRD} = 0$

In a given sampling window, either 3 or 6 samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using 3 samples

Sampling window width = $(\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}) \times 2$, if $\text{QUALPRD} \neq 0$

Sampling window width = $(\text{SYSCLK cycle}) \times 2$, if $\text{QUALPRD} = 0$

Case 2:

Qualification using 6 samples

Sampling window width = $(\text{SYSCLK cycle} \times 2 \times \text{QUALPRD}) \times 5$, if $\text{QUALPRD} \neq 0$

Sampling window width = $(\text{SYSCLK cycle}) \times 5$, if $\text{QUALPRD} = 0$

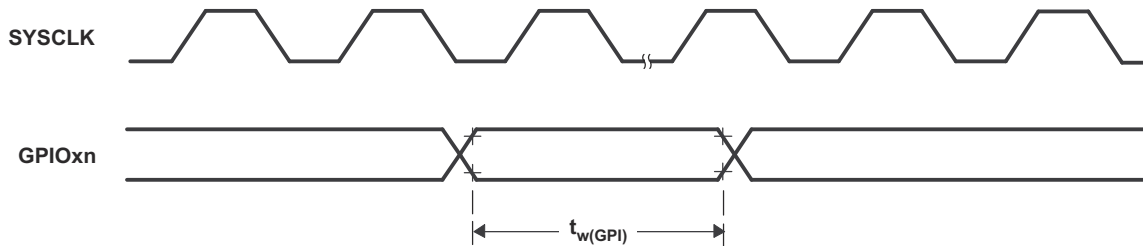


Figure 6-25. General-Purpose Input Timing

6.13.9 Interrupts

The C28x CPU has fourteen peripheral interrupt lines. Two of them (INT13 and INT14) are connected directly to CPU timers 1 and 2, respectively. The remaining twelve are connected to peripheral interrupt signals through the enhanced Peripheral Interrupt Expansion (ePIE) module. The ePIE multiplexes up to sixteen peripheral interrupts into each CPU interrupt line. It also expands the vector table to allow each interrupt to have its own ISR. This allows the CPU to support a large number of peripherals.

An interrupt path is divided into three stages—the peripheral, the ePIE, and the CPU. Each stage has its own enable and flag registers. This system allows the CPU to handle one interrupt while others are pending, implement and prioritize nested interrupts in software, and disable interrupts during certain critical tasks.

Figure 6-26 shows the interrupt architecture for this device.

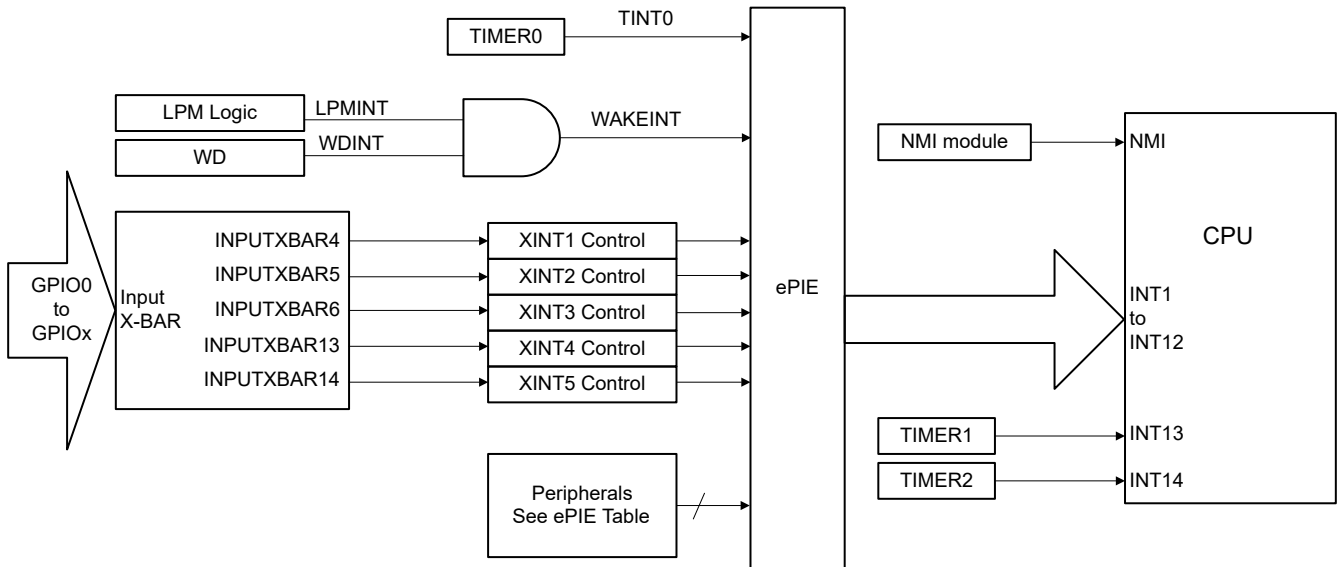


Figure 6-26. Device Interrupt Architecture

6.13.9.1 External Interrupt (XINT) Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.13.9.1.1 External Interrupt Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------|------------------------------------|----------------|---|-----|--------|
| $t_{w(INT)}$ | Pulse duration, INT input low/high | Synchronous | $2t_{c(SYSCCLK)}$ | | cycles |
| | | With qualifier | $t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SYSCCLK)}$ | | cycles |

6.13.9.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|--------------|---|----------------------------------|--|--------|
| $t_{d(INT)}$ | Delay time, INT low/high to interrupt-vector fetch ⁽¹⁾ | $t_{w(IQSW)} + 14t_{c(SYSCCLK)}$ | $t_{w(IQSW)} + t_{w(SP)} + 14t_{c(SYSCCLK)}$ | cycles |

(1) This assumes that the ISR is in a single-cycle memory.

6.13.9.1.3 External Interrupt Timing

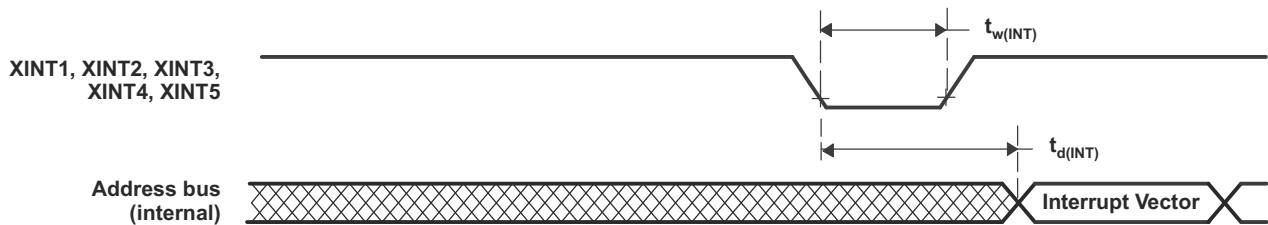


Figure 6-27. External Interrupt Timing

6.13.10 Low-Power Modes

This device has HALT, IDLE and STANDBY as clock-gating low-power modes.

Further details, as well as the entry and exit procedure, for all of the low-power modes can be found in the *Low-Power Modes* section of the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#).

6.13.10.1 Clock-Gating Low-Power Modes

IDLE and HALT modes on this device are similar to those on other C28x devices. [Table 6-11](#) describes the effect on the system when any of the clock-gating low-power modes are entered.

Table 6-11. Effect of Clock-Gating Low-Power Modes on the Device

| MODULES/ CLOCK DOMAIN | IDLE | STANDBY | HALT |
|---|---------|---------|--|
| SYSCLK | Active | Gated | Gated |
| CPUCLK | Gated | Gated | Gated |
| Clock to modules connected to PERx.SYSCLK | Active | Gated | Gated |
| WDCLK | Active | Active | Gated if CLKSRCCTL1.WDHALTI = 0 |
| PLL | Powered | Powered | Software must power down PLL before entering HALT. |
| INTOSC1 | Powered | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| INTOSC2 | Powered | Powered | Powered down if CLKSRCCTL1.WDHALTI = 0 |
| Flash ⁽¹⁾ | Powered | Powered | Powered |
| XTAL ⁽²⁾ | Powered | Powered | Powered |

- (1) The Flash module is not powered down by hardware in any LPM. It may be powered down using software if required by the application.
- (2) The XTAL is not powered down by hardware in any LPM. It may be powered down by software setting the XTALCR.OSCOFF bit to 1. This can be done at any time during the application if the XTAL is not required.

6.13.10.2 Low-Power Mode Wake-up Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.13.10.2.1 IDLE Mode Timing Requirements

| | | | MIN | MAX | UNIT |
|---------------|---|-------------------------|--------------------------------|-----|--------|
| $t_{w(WAKE)}$ | Pulse duration, external wake-up signal | Without input qualifier | $2t_{c(SYSCLK)}$ | | cycles |
| | | With input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |

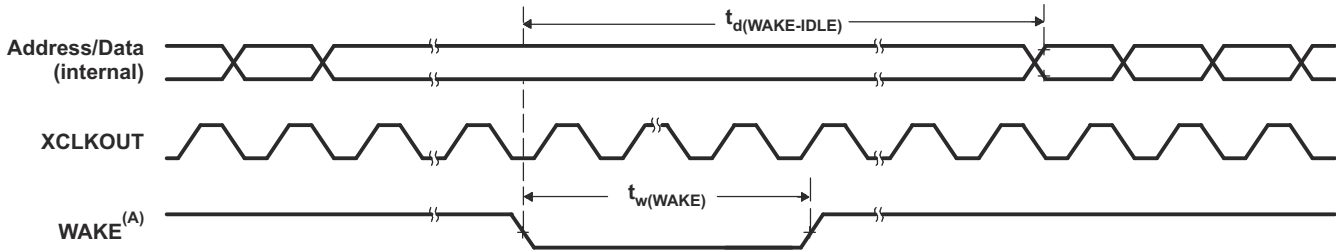
6.13.10.2.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|---|---------------------------|-------------------------|---------------------------------|--------|
| $t_{d(WAKE-IDLE)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ | From Flash (active state) | Without input qualifier | $40t_{c(SYSCLK)}$ | cycles |
| | | | With input qualifier | $40t_{c(SYSCLK)} + t_{w(WAKE)}$ | cycles |
| | | From RAM | Without input qualifier | $25t_{c(SYSCLK)}$ | cycles |
| | | | With input qualifier | $25t_{c(SYSCLK)} + t_{w(WAKE)}$ | cycles |

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

6.13.10.2.3 IDLE Entry and Exit Timing Diagram



A. WAKE can be any enabled interrupt, \overline{WDINT} or XRSn. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

Figure 6-28. IDLE Entry and Exit Timing Diagram

6.13.10.2.4 STANDBY Mode Timing Requirements

| | | | MIN | MAX | UNIT |
|-------------------|---|---|-----------------------------------|-----|--------|
| $t_{w(WAKE-INT)}$ | Pulse duration, external wake-up signal | QUALSTDBY = 0 $2t_{c(OSCCLK)}$ | $3t_{c(OSCCLK)}$ | | cycles |
| | | QUALSTDBY > 0 $(2 + QUALSTDBY)t_{c(OSCCLK)}$ ⁽¹⁾ | $(2 + QUALSTDBY) * t_{c(OSCCLK)}$ | | |

(1) QUALSTDBY is a 6-bit field in the LPMCR register.

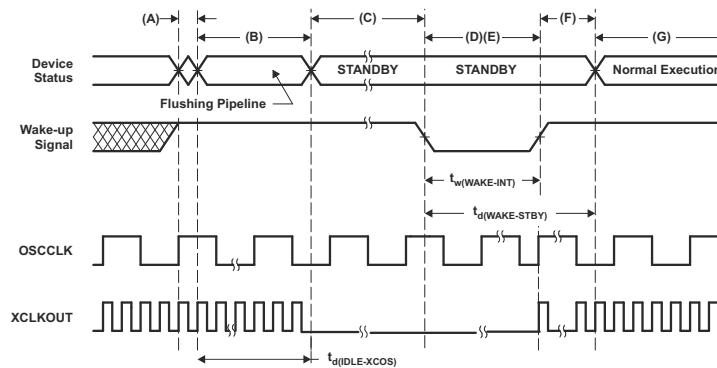
6.13.10.2.5 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|---|--|--|--------|
| $t_{d(IDLE-XCOS)}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $16t_{c(INTOSC1)}$ | cycles |
| $t_{d(WAKE-STBY)}$ | Delay time, external wake signal to program execution resume ⁽¹⁾ | Wakeup from flash (Flash module in active state) | $175t_{c(SYSCCLK)} + t_{w(WAKE-INT)}$ | cycles |
| $t_{d(WAKE-STBY)}$ | | Wakeup from RAM | $3t_{c(OSC)} + 15t_{c(SYSCCLK)} + t_{w(WAKE-INT)}$ | cycles |

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.

6.13.10.2.6 STANDBY Entry and Exit Timing Diagram



- IDLE instruction is executed to put the device into STANDBY mode.
- The LPM block responds to the STANDBY signal, SYSCCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
- Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- The external wake-up signal is driven active.
- The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
- After a latency period, the STANDBY mode is exited.
- Normal execution resumes. The device will respond to the interrupt (if enabled).

Figure 6-29. STANDBY Entry and Exit Timing Diagram

6.13.10.2.7 HALT Mode Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------------|---|--|-----|--------|
| $t_{w(\text{WAKE-GPIO})}$ | Pulse duration, GPIO wake-up signal ⁽¹⁾ | $t_{\text{oscst}} + 2t_{c(\text{OSCCLK})}$ | | cycles |
| $t_{w(\text{WAKE-XRS})}$ | Pulse duration, $\overline{\text{XRS}}$ wake-up signal ⁽¹⁾ | $t_{\text{oscst}} + 8t_{c(\text{OSCCLK})}$ | | cycles |

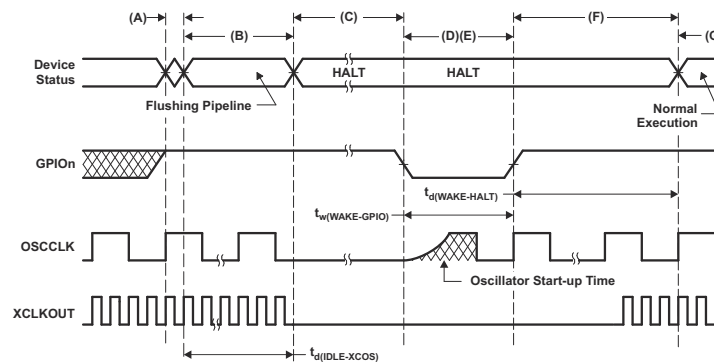
(1) For applications using X1/X2 for OSCCLK, the user must characterize their specific oscillator start-up time as it is dependent on circuit/layout external to the device. See the *Crystal Oscillator (XTAL)* section for more information. For applications using INTOSC1 or INTOSC2 for OSCCLK, see the *Internal Oscillators* section for t_{oscst} . Oscillator start-up time does not apply to applications using a single-ended crystal on the X1 pin, as it is powered externally to the device.

6.13.10.2.8 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|---------------------------|---|-----|---------------------------|--------|
| $t_{d(\text{IDLE-XCOS})}$ | Delay time, IDLE instruction executed to XCLKOUT stop | | $16t_{c(\text{INTOSC1})}$ | cycles |
| $t_{d(\text{WAKE-HALT})}$ | Delay time, external wake signal end to CPU1 program execution resume | | | cycles |
| | Wakeup from Flash - Flash module in active state | | $75t_{c(\text{OSCCLK})}$ | |
| | Wakeup from RAM | | $75t_{c(\text{OSCCLK})}$ | |

6.13.10.2.9 HALT Entry and Exit Timing Diagram



- A. IDLE instruction is executed to put the device into HALT mode.
- B. The LPM block responds to the HALT signal, SYSCLK is held for a maximum 16 INTOSC1 clock cycles before being turned off. This delay enables the CPU pipeline and any other pending operations to flush properly.
- C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes very little power. It is possible to keep the internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT MODE. This is done by writing 1 to CLKSRCCTL1.WDHALTI. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
- D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low noise environment before entering and during HALT mode.
- E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
- F. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after some latency. The HALT mode is now exited.
- G. Normal operation resumes.
- H. The user must relock the PLL upon HALT wakeup to ensure a stable PLL lock.

Figure 6-30. HALT Entry and Exit Timing Diagram

6.14 Analog Peripherals

The analog subsystem module is described in this section.

The analog modules on this device include the Analog-to-Digital Converter (ADC), temperature sensor, Comparator Subsystem (CMPSS), Programmable Gain Amplifier (PGA), and buffered Digital-to-Analog Converter (DAC).

The analog subsystem has the following features:

- Flexible voltage references
 - The ADCs are referenced to VREFH_{ix} and VSSA pins
 - VREFH_{ix} pin voltage can be driven in externally or can be generated by an internal bandgap voltage reference
 - The internal voltage reference range can be selected to be 0 V to 3.3 V or 0 V to 2.5 V
 - The buffered DACs are referenced to VREFH_{ix} and VSSA
 - The comparator DACs are referenced to VDDA and VSSA
- Flexible pin usage
 - Buffered DAC outputs, comparator subsystem inputs, and digital inputs (AIOs)/outputs (AGPIOs) are multiplexed with ADC inputs
 - Internal connection to V_{REFLO} on all ADCs for offset self-calibration

6.14.1 Block Diagram

The following analog subsystem block diagrams show the connections between the different integrated analog modules to the device pins. These pins fall into two categories: analog module inputs/outputs and reference pins.

The reference pins, VREFHI and VREFLO, can be used to supply an external voltage reference to the associated ADCs. VREFHI can also be used to supply the voltage reference to buffered DAC. The choice of reference is configurable per module for each CMPSS or buffered DAC; the selection is made using the module's configuration registers.

Some analog pins support digital functionality through muxed AIOs and AGPIOs. AIOs only support digital input functionality, while AGPIOs support full digital input and output functionality.

The following notes apply to all packages:

- Not all analog pins are available on all devices. See the device data manual to determine which pins are available.
- See the device data manual to determine the allowable voltage range for VREFHI and VREFLO.
- An external capacitor is required on the VREFHI pins. See the device data manual for the specific value required.

Figure 6-31 shows the Analog Subsystem Block Diagram for the 128-/80-pin TQFP, the 64-pin LQFP, and the 56-pin VQFN.

Figure 6-32 shows the Analog Subsystem Block Diagram for the 100-pin LQFP.

Figure 6-33 shows the general overview of the analog group connections.

The analog pins and internal connections are given in [Analog Pins and Internal Connections](#). [Analog Signal Descriptions](#) lists descriptions of analog signals.

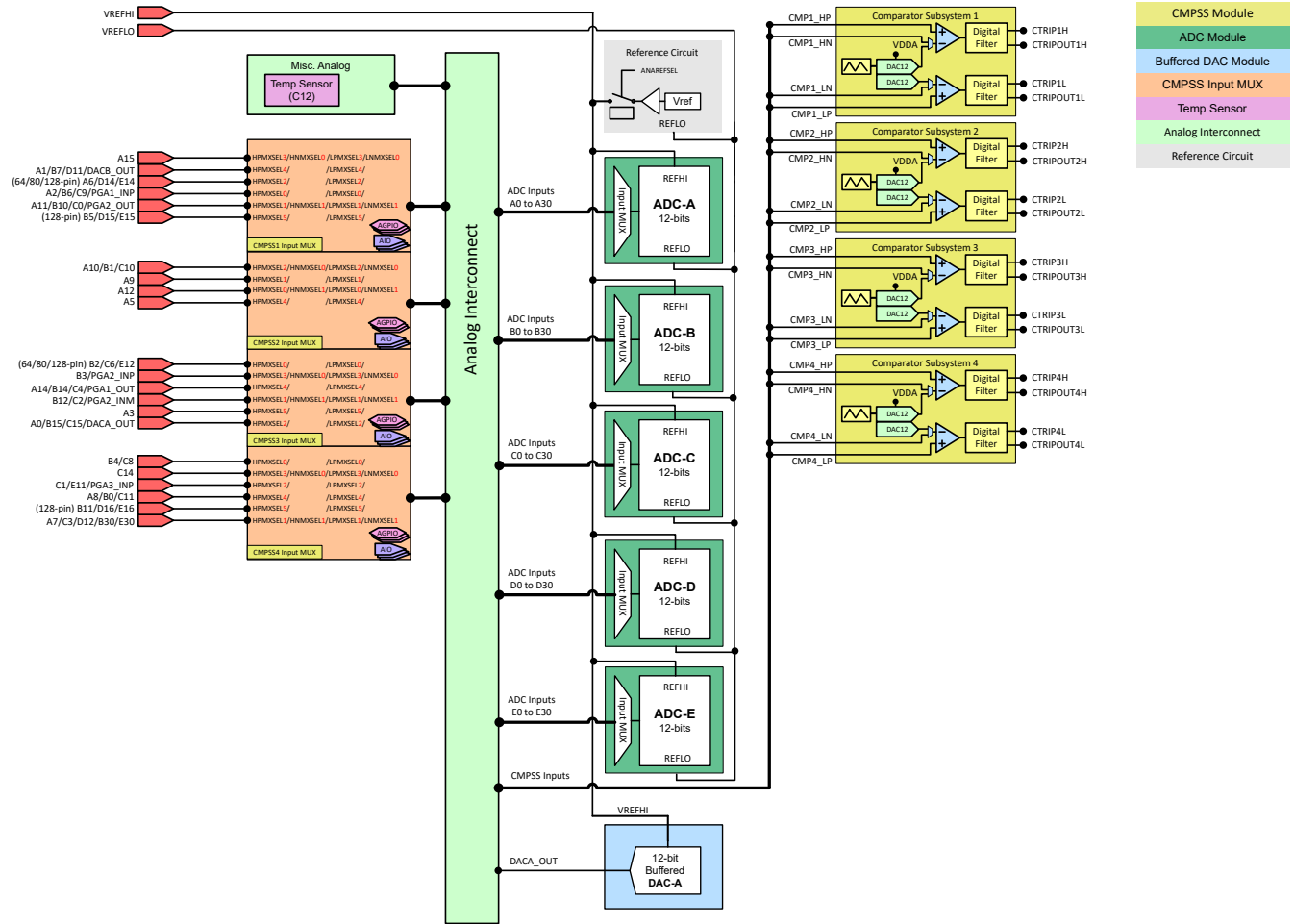


Figure 6-31. Analog Subsystem Block Diagram (128-/80-/64-/56-Pin Packages)

ADVANCE INFORMATION

ADVANCE INFORMATION

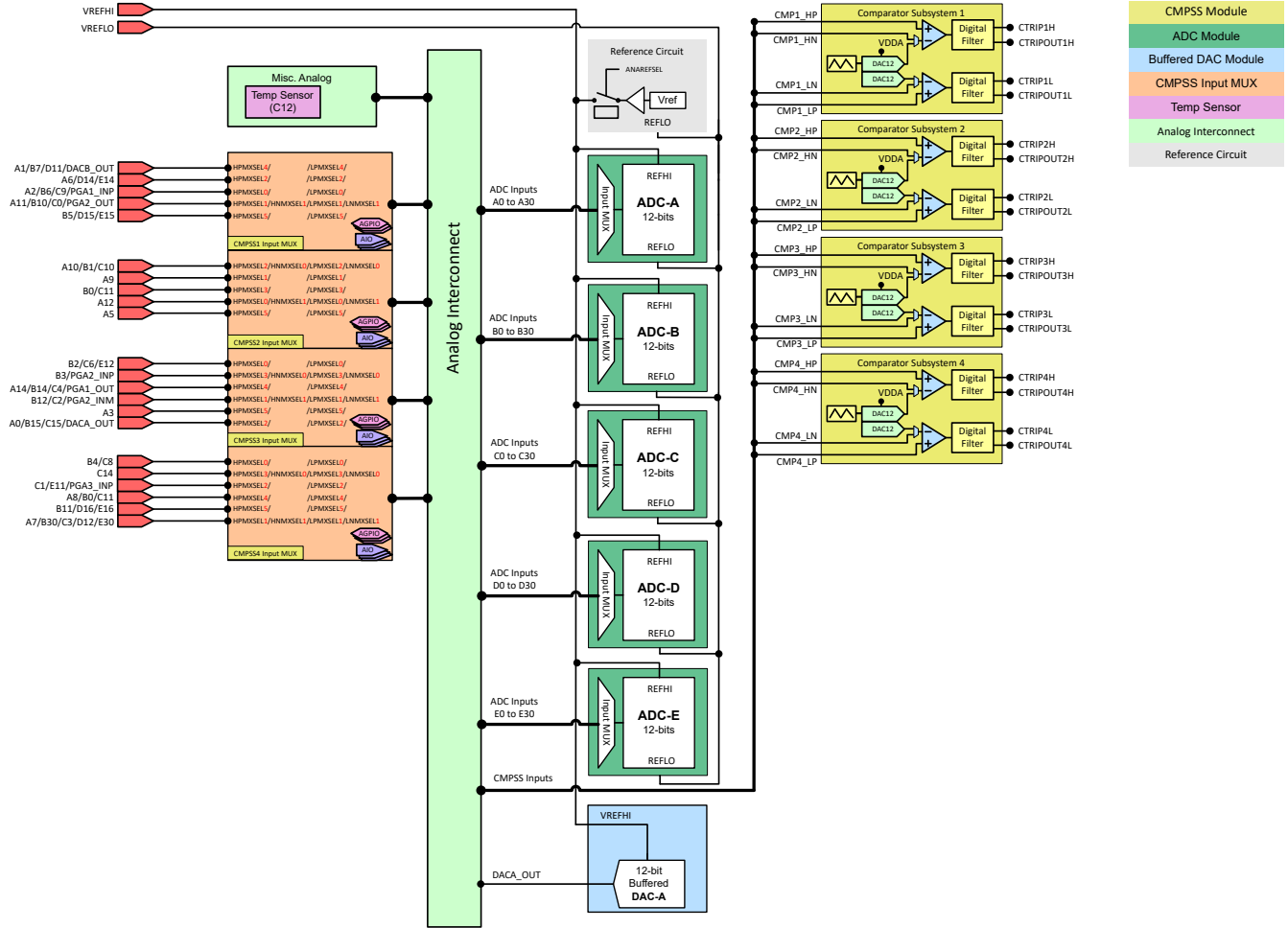


Figure 6-32. Analog Subsystem Block Diagram (100-Pin Package)

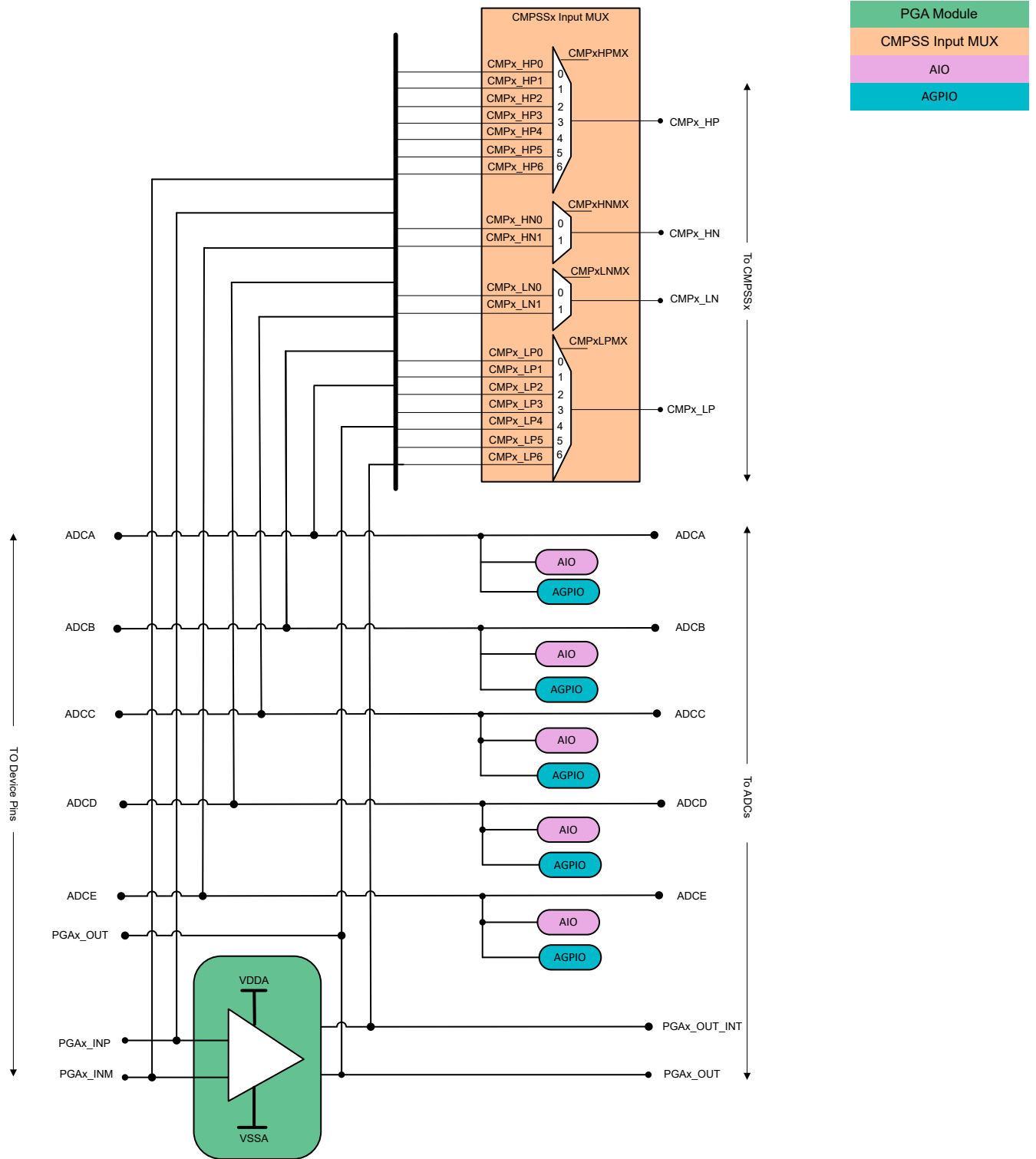


Figure 6-33. Analog Group Connections

ADVANCE INFORMATION

Input connections to the CMPSS modules are selectable through a programmable input mux. Figure 6-33 demonstrates the connection between the input MUX of CMPSS modules, PGA modules, and ADC modules. Table 6-12 shows the mapping of ADC input signals and PGA input and output signals to CMPSS mux inputs.

- To configure the CMPx_HP input mux for CMPSSx, write to the CMPxHPMXSEL field in the CMPHPMXSEL analog subsystem register.
- To configure the CMPx_HN input mux for CMPSSx, write to the CMPxHNMXSEL field in the CMPHNMXSEL analog subsystem register.
- To configure the CMPx_LP input mux for CMPSSx, write to the CMPxLPMXSEL field in the CMPLPMXSEL analog subsystem register.
- To configure the CMPx_LN input mux for CMPSSx, write to the CMPxLNMXSEL field in the CMPLNMXSEL analog subsystem register.

Table 6-12. CMPSS Input Mux Options

| CMPSSx Input MUX | CMP1 | CMP2 | CMP3 | CMP4 |
|------------------|-----------------------------|------------------------|------------------------|------------------------------|
| HP0 | A2, B6, C9, PGA1_INP | A4, B8 | B2, C6, E12 | B4, C8 |
| HP1 | A11, B10, C0, PGA2_OUT | A12 | B12, C2, PGA2_INM | A7, C3, D12, B30, E30, |
| HP2 | A6, D14, E14 ⁽³⁾ | A9 | A0, B15, C15, DACA_OUT | C1, E11, PGA3_INP |
| HP3 | A15 ⁽²⁾ | A10, B1, C10 | B3, PGA2_INP | C14 |
| | | B0, C11 ⁽¹⁾ | | |
| HP4 | A1, B7, D11, DACB_OUT | | A14, B14, C4, PGA1_OUT | A8 |
| | | | | B0, C11 ⁽²⁾ |
| HP5 | B5, D15, E15 ⁽⁴⁾ | A5 ⁽¹⁾ | A3 | B11, D16, E16 ⁽⁴⁾ |
| HP6 | PGA1_OUT_INT | PGA3_OUT_INT | PGA2_OUT_INT | |
| HP7 | | TEMP SENSOR | | |
| HN0 | A15 ⁽²⁾ | A10, B1, C10 | B3, PGA2_INP | C14 |
| HN1 | A11, B10, C0, PGA2_OUT | A12 | B12, C2, PGA2_INM | A7, B30, C3, D12, E30 |
| LP0 | A2, B6, C9, PGA1_INP | A4, B8 | B2, C6, E12 | B4, C8 |
| LP1 | A11, B10, C0, PGA2_OUT | A12 | B12, C2, PGA2_INM | A7, B30, C3, D12, E30 |
| LP2 | A6, D14, E14 ⁽³⁾ | A9 | A0, B15, C15, DACA_OUT | C1, E11, PGA3_INP |
| LP3 | A15 ⁽²⁾ | A10, B1, C10 | B3, PGA2_INP | C14 |
| | | B0, C11 ⁽¹⁾ | | |
| LP4 | A1, B7, D11, DACB_OUT | | A14, B14, C4, PGA1_OUT | A8 |
| | | | | B0, C11 ⁽²⁾ |
| LP5 | B5, D15, E15 ⁽⁴⁾ | A5 ⁽¹⁾ | A3 | B11, D16, E16 ⁽⁴⁾ |
| LP6 | PGA1_OUT_INT | PGA3_OUT_INT | PGA2_OUT_INT | |
| LN0 | A15 | A10, B1, C10 | B3, PGA2_INP | C14 |
| LN1 | A11, B10, C0, PGA2_OUT | A12 | B12, C2, PGA2_INM | A7, C3, D12, B30, E30 |

- (1) These MUX options are available only on 100 QFP package.
 (2) This MUX option is available only on 56 QFN, 64 QFP, 80 QFP, and 128 QFP packages.
 (3) This MUX option is available only on 64 QFP, 80 QFP, 100 QFP, and 128 QFP packages.
 (4) This MUX option is available only on 100 QFP and 128 QFP packages.

6.14.2 Analog Pins and Internal Connections

Table 6-13. Analog Pins and Internal Connections

| Pin Name | Pins/Package | | | | | ADC | | | | | DAC | PGA | Comparator Subsystem (MUX) | | | | AIO Input/ AGPIO |
|-----------------------|--------------|------------|-----------|-----------|-----------|-----|-----|-----|----------|-----|-------------|----------|----------------------------|---------------------|---------------------|---------------------|---------------------|
| | 128 QFP | 100 QFP | 80 QFP | 64 QFP | 56 QFN | A | B | C | D | E | | | High Positive | High Negative | Low Positive | Low Negative | |
| VREFHI | 31 32 | 24 25 | 20 | 16 | 14 | - | - | - | D20 | E20 | | | | | | | |
| VREFLO | 33 34 | 26 27 | 21 | 17 | 15 | A13 | B13 | C13 | D13 | E13 | | | | | | | |
| Analog Group 1 | | | | | | | | | | | CMP1 | | | | | | |
| A6/D14/E14 | 18 | 14 | 10 | 6 | - | A6 | - | - | D14 | E14 | | | CMP1 (HPMXSEL=2) | - | CMP1 (LPMXSEL=2) | - | AGPIO228 (3) |
| A2/B6/C9/PGA1_INP | 21 | 17 | 13 | 9 | 7 | A2 | B6 | C9 | - | - | | PGA1_INP | CMP1 (HPMXSEL=0) | - | CMP1 (LPMXSEL=0) | - | AGPIO224 (3) |
| A15 | 22 | - | 14 | 10 | 8 | A15 | - | - | - | - | | | CMP1 (HPMXSEL=3) | CMP1 (HNMXSEL=0) | CMP1 (LPMXSEL=3) | CMP1 (LNMXSEL=0) | AGPIO233 (3) |
| B9/C7/PGA1_INM | | 18 | | | | - | B9 | C7 | - | - | PGA1_INM | | | | | | |
| A11/B10/C0/PGA2_OUT | 27 | 20 | 16 | 12 | 10 | A11 | B10 | C0 | - | - | | PGA2_OUT | CMP1 (HPMXSEL=1) | CMP1 (HNMXSEL=1) | CMP1 (LPMXSEL=1) | CMP1 (LNMXSEL=1) | AIO237 |
| A1/B7/D11/DACB_OUT | 29 | 22 | 18 | 14 | 12 | A1 | B7 | - | D11 | - | DACB_OUT | | CMP1 (HPMXSEL=4) | - | CMP1 (LPMXSEL=4) | - | AIO232 |
| B5/D15/E15 | 38 | 32 | - | - | - | - | B5 | - | D15 | E15 | | | - | - | CMP1 (LPMXSEL=5) | - | AIO252 |
| PGA3_OUT | | 24 | 20 | 18 | - | - | - | - | PGA3_OUT | | | | | | | | |
| Analog Group 2 | | | | | | | | | | | CMP2 | | | | | | |
| A4/B8 | 42 | 36 | 27 | 23 | 21 | A4 | B8 | - | - | - | | | CMP2 (HPMXSEL=0) | - | CMP2 (LPMXSEL=0) | - | AIO225 |
| A12 | 35 | 28 | 22 | 18 | 16 | A12 | - | - | - | - | | | CMP2 (HPMXSEL=1) | - | CMP2 (LPMXSEL=1) | - | AIO238 |
| A9 | 48 | 38 | 28 | 24 | 22 | A9 | - | - | - | - | | | CMP2 (HPMXSEL=2) | - | CMP2 (LPMXSEL=2) | - | AGPIO227 (3) |
| A10/B1/C10 | 50 | 40 | 29 | 25 | 23 | A10 | B1 | C10 | - | - | | | CMP2 (HPMXSEL=3) | CMP2 (HNMXSEL=0) | CMP2 (LPMXSEL=3) | CMP2 (LNMXSEL=0) | AGPIO230 (3) |
| B0/C11 | - | 41 | - | - | - | - | B0 | C11 | | | | | CMP2 (HPMXSEL=3) | - | CMP2 (LPMXSEL=3) | - | AGPIO231 (3) |
| A5 | 28 | - | 17 | 13 | 11 | A5 | - | - | - | - | | | CMP2 (HPMXSEL=5) | - | CMP2 (LPMXSEL=5) | - | AIO249 |
| | - | 35 | - | - | - | | | | | | | | | | | | |
| Analog Group 3 | | | | | | | | | | | CMP3 | | | | | | |
| B2/C6/E12 | 19 | 15 | 11 | 7 | - | - | B2 | C6 | - | E12 | | | CMP3 (HPMXSEL=0) | - | CMP3 (LPMXSEL=0) | - | AGPIO226 (3) |
| B12/C2/PGA2_INM | 28 | 21 | 17 | 13 | 11 | - | B12 | C2 | - | - | | PGA2_INM | CMP3 (HPMXSEL=1) | CMP3 (HNMXSEL=1) | CMP3 (LPMXSEL=1) | CMP3 (LNMXSEL=1) | AIO244 |

Table 6-13. Analog Pins and Internal Connections (continued)

| Pin Name | Pins/Package | | | | | ADC | | | | | DAC | PGA | Comparator Subsystem (MUX) | | | | AIO Input/ AGPIO |
|-----------------------------|-------------------|-------------------|-----------|-----------|-----------|-----|-----|-----|-----|-----|----------|------------------|----------------------------|---------------------|---------------------|---------------------|---------------------|
| | 128 QFP | 100 QFP | 80 QFP | 64 QFP | 56 QFN | A | B | C | D | E | | | High Positive | High Negative | Low Positive | Low Negative | |
| A0/B15/C15/DACA_OUT | 30 | 23 | 19 | 15 | 13 | A0 | B15 | C15 | - | - | DACA_OUT | | CMP3 (HPMXSEL=2) | - | CMP3 (LPMXSEL=2) | - | AIO231 |
| B3/PGA2_INP | 20 | 16 | 12 | 8 | 6 | - | B3 | - | - | - | | PGA2_INP | CMP3 (HPMXSEL=3) | CMP3 (HNMXSEL=0) | CMP3 (LPMXSEL=3) | CMP3 (LNMXSEL=0) | AGPIO242 (3) |
| C5 | | 28 | | | | | C5 | | | | | | | | | | |
| A14/B14/C4/PGA1_OUT | 26 | 19 | 15 | 11 | 9 | A14 | B14 | C4 | - | - | | PGA1_OUT | CMP3 (HPMXSEL=4) | - | CMP3 (LPMXSEL=4) | - | AIO239 |
| A3 | 20 | - | 12 | 8 | 6 | A3 | - | - | - | - | | | CMP3 (HPMXSEL=5) | - | CMP3 (LPMXSEL=5) | - | |
| | - | 18 | - | - | - | | | | | | | | | | | | |
| Analog Group 4 | | | | | | | | | | | | CMP4 | | | | | |
| B4/C8 | 49 | 39 | 28 | 24 | 22 | - | B4 | C8 | - | - | | | CMP4 (HPMXSEL=0) | - | CMP4 (LPMXSEL=0) | - | AGPIO236 (3) |
| C1/E11/PGA3_INP | 35 | 29 | 22 | 18 | 16 | - | - | C1 | - | E11 | | PGA3_INP | CMP4 (HPMXSEL=2) | - | CMP4 (LPMXSEL=2) | - | - |
| C14 | 42 | 42 | 27 | 23 | 21 | - | - | C14 | - | - | | | CMP4 (HPMXSEL=3) | CMP4 (HNMXSEL=0) | CMP4 (LPMXSEL=3) | CMP4 (LNMXSEL=0) | AGPIO247 (3) |
| B0/C11 | 39 | - | 24 | 20 | 18 | - | B0 | C11 | - | - | | | CMP4 (HPMXSEL=4) | - | CMP4 (LPMXSEL=4) | - | AIO241 |
| A8 | - | 37 | - | - | - | A8 | - | - | - | - | | | CMP4 (HPMXSEL=4) | - | CMP4 (LPMXSEL=4) | - | AIO240 |
| B11/D16/E16 | 36 | 30 | - | - | - | - | B11 | - | D16 | E16 | | | CMP4 (HPMXSEL=5) | - | CMP4 (LPMXSEL=5) | - | AIO251 |
| PGA3_INM | 36 ⁽¹⁾ | 30 ⁽¹⁾ | 23 | 19 | 17 | - | - | - | - | - | | PGA3_INM | | | | | |
| A7/B30/C3/D12/E30 | 37 | 31 | | | | A7 | B30 | C3 | D12 | E30 | | | | CMP4 (HPMXSEL=1) | CMP4 (HNMXSEL=1) | CMP4 (LPMXSEL=1) | CMP4 (LNMXSEL=1) |
| Other Analog | | | | | | | | | | | | | | | | | |
| TempSensor ⁽²⁾ | | | | | | - | - | C12 | - | - | | | CMP2 (HPMXSEL=7) | - | - | - | - |
| PGA1_OUT_INT ⁽²⁾ | | | | | | A21 | B21 | - | - | - | | PGA1_OUT_I NT | CMP1 (HPMXSEL=6) | - | CMP1 (LPMXSEL=6) | - | - |
| PGA2_OUT_INT ⁽²⁾ | | | | | | - | B22 | C21 | - | - | | PGA2_OUT_I NT | CMP3 (HPMXSEL=6) | - | CMP3 (LPMXSEL=6) | - | - |
| PGA3_OUT_INT ⁽²⁾ | | | | | | A22 | - | C22 | - | - | | PGA3_OUT_I NT | CMP2 (HPMXSEL=6) | - | CMP2 (LPMXSEL=6) | - | - |

- (1) Signal is bonded together with another signal as a single pin on this package.
- (2) Internal connection only; does not come to a device pin.
- (3) Only on 100 QFP package, AGPIO 247 is available.

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Note

The GPIOs on the analog pins support full digital input and output functionality and are referred to as AGPIOs. By default, the AGPIOs are unconnected; that is, the analog and digital functions are both disabled. For configuration details, see the *Digital Inputs and Outputs on ADC Pins (AGPIOs)* section.

6.14.3 Analog Signal Descriptions

Table 6-14. Analog Signal Descriptions

| Signal Name | Description |
|-----------------|---|
| AIOx | Digital input on ADC pin |
| AGPIOx | Digital input/output pin with ADC functionality |
| ADCINAx, Ax | ADC A Input |
| ADCINBx, Bx | ADC B Input |
| ADCINCx, Cx | ADC C Input |
| ADCINDx, Dx | ADC D Input |
| ADCINEx, Ex | ADC E Input |
| CMPx_HP | Comparator subsystem high comparator positive input |
| CMPx_HN | Comparator subsystem high comparator negative input |
| CMPx_LP | Comparator subsystem low comparator positive input |
| CMPx_LN | Comparator subsystem low comparator negative input |
| DACA_OUT | Buffered DAC Output |
| DACB_OUT | CMPSS1 DAC Output |
| PGAx_INP | PGA module non-inverting pin |
| PGAx_INM | PGA module inverting pin |
| PGAx_OUT | PGA module output |
| PGAx_OUT_INT | PGA module internal output connected to CMPSS and ADC modules |
| TEMP SENSOR, TS | Internal temperature sensor |

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6.14.4 Analog-to-Digital Converter (ADC)

The ADC module described here is a successive approximation (SAR) style ADC with resolution of 12 bits. This section refers to the analog circuits of the converter as the “core,” and includes the channel-select MUX, the sample-and-hold (S/H) circuit, the successive approximation circuits, voltage reference circuits, and other analog support circuits. The digital circuits of the converter are referred to as the “wrapper” and include logic for programmable conversions, result registers, interfaces to analog circuits, interfaces to the peripheral buses, post-processing circuits, and interfaces to other on-chip modules.

Each ADC module consists of a single sample-and-hold (S/H) circuit. The ADC module is designed to be duplicated multiple times on the same chip, allowing simultaneous sampling or independent operation of multiple ADCs. The ADC wrapper is start-of-conversion (SOC)-based (see the *SOC Principle of Operation* section of the Analog-to-Digital Converter (ADC) chapter in the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#)).

Each ADC has the following features:

- Resolution of 12 bits
- Ratiometric external reference set by VREFHI/VREFLO
- Selectable internal reference of 2.5 V or 3.3 V
- Single-ended signal mode
- Input multiplexer with up to 32 channels
- 16 configurable SOCs
- 16 individually addressable result registers
- External analog input mux selection per SOC, up to 4 bits
- Sample cap reset feature for memory crosstalk mitigation
- Multiple trigger sources
 - Software immediate start
 - All ePWMs: ADCSOC A or B
 - GPIO XINT2
 - CPU Timers 0/1/2
 - ADCINT1/2
 - ECAP events in capture mode (CEVT1, CEVT2, CEVT3, and CEVT4) and APWM mode (period match, compare match, or both).
 - Global software trigger for multiple ADCs
- Four flexible PIE interrupts
- Burst-mode triggering option
- Hardware oversampling mode up to 128x, with configurable trigger spread delay
- Hardware undersampling mode
- Trigger phase delay function
- Four post-processing blocks, each with:
 - Saturating offset calibration
 - Error from setpoint calculation
 - High, low, and zero-crossing compare, with interrupt and ePWM trip capability
 - Configurable digital filter for high/low/zero-crossing compare
 - Trigger-to-sample delay capture
 - Absolute value calculation
 - 24-bit accumulation register for oversampling, with configurable binary shift
 - Minimum/maximum calculation for outlier rejection

Note

Not every channel can be pinned out from all ADCs. See the *Pin Configuration and Functions* section to determine which channels are available.

The block diagram for the ADC core and ADC wrapper are shown in Figure 6-34.

ADVANCE INFORMATION

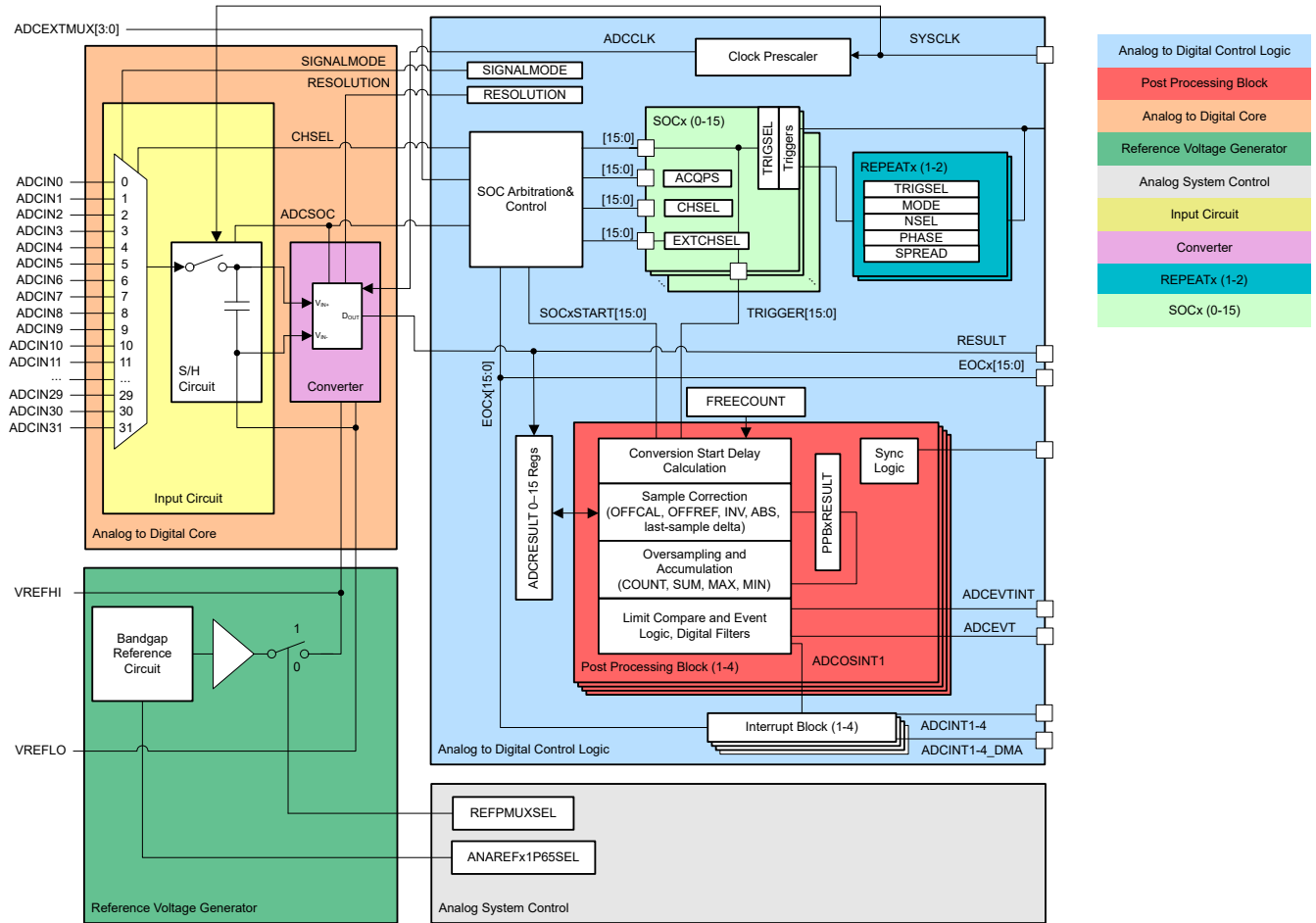


Figure 6-34. ADC Module Block Diagram

6.14.4.1 ADC Configurability

Some ADC configurations are individually controlled by the SOCs, while others are globally controlled per ADC module. Table 6-15 summarizes the basic ADC options and their level of configurability.

Table 6-15. ADC Options and Configuration Levels

| OPTIONS | CONFIGURABILITY |
|-----------------------------|--|
| Clock | Per module ⁽¹⁾ |
| Resolution | Not configurable (12-bit resolution only) |
| Signal mode | Not configurable (single-ended signal mode only) |
| Reference voltage source | Either external or internal for all modules |
| Trigger source | Per SOC ⁽¹⁾ |
| Converted channel | Per SOC |
| Acquisition window duration | Per SOC ⁽¹⁾ |
| EOC location | Per module |
| Burst mode | Per module ⁽¹⁾ |

(1) Writing these values differently to different ADC modules could cause the ADCs to operate asynchronously. For guidance on when the ADCs are operating synchronously or asynchronously, see the *Ensuring Synchronous Operation* section of the Analog-to-Digital Converter (ADC) chapter in the *TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual*.

6.14.4.1.1 Signal Mode

The ADC supports single-ended signaling. The input voltage to the converter is sampled through a single pin (ADCINx), referenced to VREFLO.

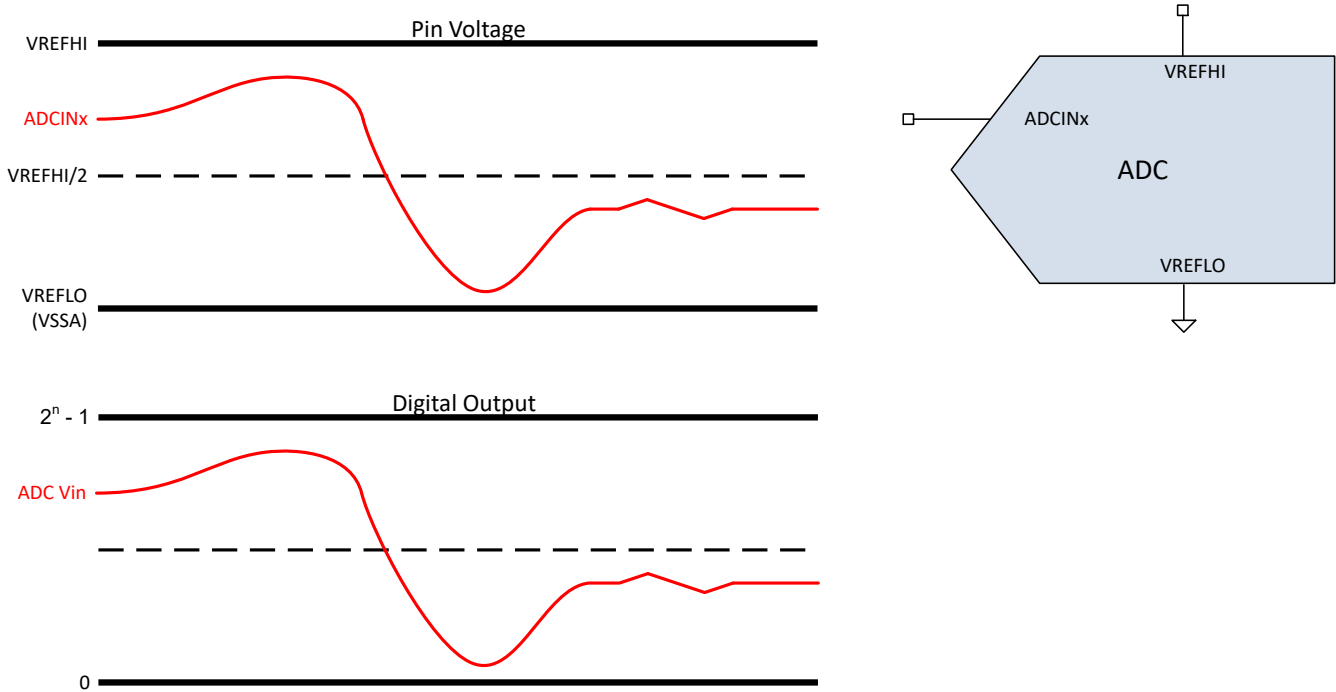


Figure 6-35. Single-ended Signaling Mode

6.14.4.2 ADC Electrical Data and Timing

Note

The ADC inputs should be kept below $V_{DDA} + 0.3$ V. If an ADC input goes above this level, ADC disturbances to other channels may occur by two mechanisms:

- ADC input overvoltage will overdrive the CMPSS mux, disturbing all other channels which share a common CMPSS mux. This disturbance will be continuous regardless of if the overvoltage input is sampled by the ADC
- When the ADC samples the overvoltage ADC input, V_{REFHI} will be pulled up to a higher level. This will disturb subsequent ADC conversions on any channel until the V_{REF} stabilizes

Note

The V_{REFHI} pin must be kept below $V_{DDA} + 0.3$ V to ensure proper functional operation. If the V_{REFHI} pin exceeds this level, a blocking circuit may activate, and the internal value of V_{REFHI} may float to 0 V internally, giving improper ADC conversion.

6.14.4.2.1 ADC Operating Conditions

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------------|-------------|--------------|-------------|------|
| ADCCLK (derived from PERx.SYSCLK) | | 5 | | 75 | MHz |
| Sample rate | 150-MHz SYSCLK | | | 3.9 | MSPS |
| Sample window duration (set by ACQPS and PERx.SYSCLK) ⁽¹⁾ | With 50 Ω or less R_S | 67 | | | ns |
| V_{REFHI} | External Reference | 1.55 | 1.65 or 2.50 | V_{DDA} | V |
| | Internal Reference = 3.3V Range | | 1.65 | | V |
| | Internal Reference = 2.5V Range | | 2.50 | | V |
| V_{REFLO} | | V_{SSA} | | V_{SSA} | V |
| $V_{REFHI} - V_{REFLO}$ | | 2.4 | | V_{DDA} | V |
| Conversion range | Internal Reference = 3.3 V Range | 0 | | 3.3 | V |
| Conversion range | Internal Reference = 2.5 V Range | 0 | | 2.5 | V |
| Conversion range | External Reference | V_{REFLO} | | V_{REFHI} | V |
| Conversion range | Analog Supply as Reference | V_{SSA} | | V_{DDA} | V |

(1) The sample window must also be at least as long as 1 ADCCLK cycle for correct ADC operation.

(2) In internal reference mode, the reference voltage is driven out of the V_{REFHI} pin by the device. The user should not drive a voltage into the pin in this mode.

6.14.4.2.2 ADC Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-----|------|---------|
| General | | | | | |
| ADCCLK Conversion Cycles | 150-MHz SYSCLK | | | 14 | ADCCLKs |
| Power Up Time | External Reference mode | | | 500 | μ s |
| | Internal Reference mode | | | 5000 | μ s |
| | Internal Reference mode, when switching between 2.5-V range and 3.3-V range. | | | 5000 | μ s |
| V_{REFHI} input current ⁽¹⁾ | | | 40 | | μ A |
| Internal Reference Capacitor Value ⁽²⁾ | | 2.2 | | | μ F |

6.14.4.2.2 ADC Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|---------------|-----|------|
| External Reference Capacitor Value ⁽²⁾ | | 2.2 | | | μF |
| DC Characteristics | | | | | |
| Gain Error | Internal reference | -45 | | 45 | LSB |
| | External reference | -5 | ±3 | 5 | |
| Offset Error | | -5 | ±1 | 5 | LSB |
| Channel-to-Channel Gain Error ⁽⁴⁾ | | | 2 | | LSB |
| Channel-to-Channel Offset Error ⁽⁴⁾ | | | 2 | | LSB |
| ADC-to-ADC Gain Error ⁽⁵⁾ | Identical VREFHI and VREFLO for all ADCs | | 4 | | LSB |
| ADC-to-ADC Offset Error ⁽⁵⁾ | Identical VREFHI and VREFLO for all ADCs | | 2 | | LSB |
| DNL Error | | >-1 | ±0.5 | 1 | LSB |
| INL Error | | -2 | ±1.5 | 2 | LSB |
| ADC-to-ADC Isolation | VREFHI = 2.5 V, synchronous ADCs | -1 | | 1 | LSBs |
| AC Characteristics | | | | | |
| SNR ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 | | 69.2 | | dB |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC | | TBD | | |
| THD ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz | | -83 | | dB |
| SFDR ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz | | 79.2 | | dB |
| SINAD ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1 | | 68.5 | | dB |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from INTOSC | | 60.0 | | |
| ENOB ⁽³⁾ | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, Single ADC | | 11.2 | | bits |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, synchronous ADCs | | TBD | | |
| | VREFHI = 2.5 V, fin = 100 kHz, SYSCLK from X1, asynchronous ADCs | | Not Supported | | |
| PSRR | VDD = 1.2-V DC + 100mV DC up to Sine at 1 kHz | | 60 | | dB |
| | VDD = 1.2-V DC + 100 mV DC up to Sine at 300 kHz | | 57 | | |
| | VDDA = 3.3-V DC + 200 mV DC up to Sine at 1 kHz | | 60 | | |
| | VDDA = 3.3-V DC + 200 mV Sine at 900 kHz | | 57 | | |

- (1) Load current on VREFHI increases when ADC input is greater than VDDA. This causes inaccurate conversions.
- (2) A ceramic capacitor with package size of 0805 or smaller is preferred. Up to ±20% tolerance is acceptable.
- (3) IO activity is minimized on pins adjacent to ADC input and VREFHI pins as part of best practices to reduce capacitive coupling and crosstalk.
- (4) Variation across all channels belonging to the same ADC module.
- (5) Worst case variation compared to other ADC modules.

6.14.4.2.3 ADC INL and DNL

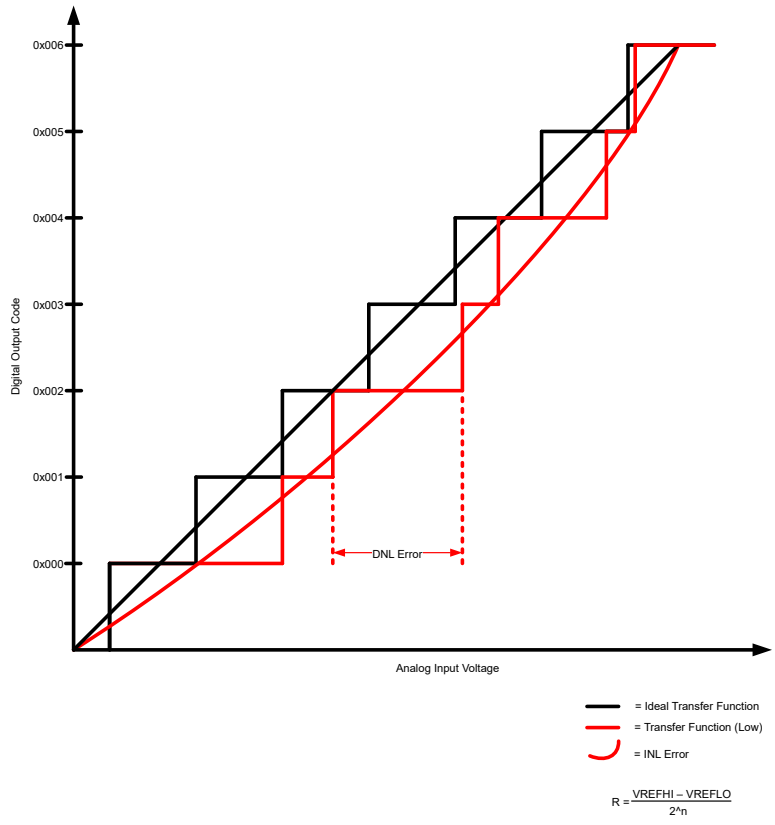


Figure 6-36. ADC INL and DNL

6.14.4.2.4 ADC Input Model

Table 6-16. Input Model Parameters

| | DESCRIPTION | REFERENCE MODE | VALUE |
|-----------------|-----------------------------|--|------------------------------|
| C _p | Parasitic input capacitance | All | See Table 6-17 to Table 6-21 |
| R _{on} | Sampling switch resistance | External Reference, 2.5-V Internal Reference | 1000 Ω |
| | | 3.3-V Internal Reference | 1700 Ω |
| C _h | Sampling capacitor | External Reference, 2.5-V Internal Reference | 4 pF |
| | | 3.3-V Internal Reference | 2.5 pF |
| R _s | Nominal source impedance | All | 50 Ω |

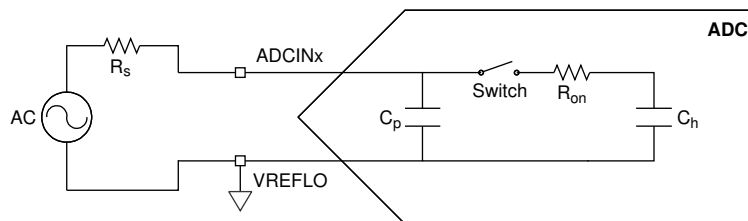


Figure 6-37. Input Model

This input model should be used with actual signal source impedance to determine the acquisition window duration. For more information, see the *Choosing an Acquisition Window Duration* section of the Analog-

to-Digital Converter (ADC) chapter in the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#). For recommendations on improving ADC input circuits, see the [ADC Input Circuit Evaluation for C2000 MCUs](#) Application Report.

Table 6-17. Per-Channel Parasitic Capacitance for 128-Pin QFP

| ADC CHANNEL | C _p (pF) | |
|------------------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0, B15, C15, DACA_OUT | 1.7 | 3.2 |
| A1, B7, D11, DACB_OUT, REFHI | 1.5 | 3.0 |
| A2, B6, C9, PGA1_INP | 1.7 | 3.2 |
| A3 | 5.4 | 6.9 |
| A4, B8, REFLO | 1.2 | 2.7 |
| A5 | 2.2 | 3.7 |
| A6, D14, E14 | 0.2 | 1.7 |
| A7, C3, D12, B30, E30 | 0.9 | 2.4 |
| A8, B0, C11 | 0.5 | 2.0 |
| A9 | 0.2 | 1.7 |
| A10, B1, C10 | 0.2 | 1.7 |
| A11, B10, C0,PGA2_OUT | 1.1 | 2.6 |
| A12 | 1.1 | 2.6 |
| A14, B14, C4, PGA1_OUT | 1.0 | 2.5 |
| A15 | 0.5 | 2.0 |
| A16, B16, C16 | 0.2 | 0.2 |
| A17,B17,C17 | 0.2 | 0.2 |
| A18,B18,C18 | 0.2 | 0.2 |
| A19,B19,C19 | 0.2 | 0.2 |
| A20,B20,C20 | 0.2 | 0.2 |
| B2, C6, E12 | 0.2 | 1.7 |
| B3, PGA2_INP | 0.2 | 1.7 |
| B4, C8 | 0.2 | 1.7 |
| B5, D15, E15 | 0.5 | 2.0 |
| B9, C7, PGA1_INM | 1.8 | 1.8 |
| B11, D16, E16 | 5.0 | 6.5 |
| B12, C2, PGA2_INM | 1.0 | 2.5 |
| C1,E11,PGA3_INP | 0.7 | 2.2 |
| C5 | 5.4 | 5.4 |
| C14 | 4.9 | 6.4 |
| D0,E0,A24 | 0.2 | 0.2 |
| D1,E1,B24 | 0.2 | 0.2 |
| D2,E2,C24 | 0.2 | 0.2 |
| D3,E3,A25 | 0.2 | 0.2 |
| D4,E4,B25 | 0.2 | 0.2 |

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Table 6-17. Per-Channel Parasitic Capacitance for 128-Pin QFP (continued)

| ADC CHANNEL | C _p (pF) | |
|-------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| D5,E5,C25 | 5.0 | 5.0 |
| D6,E6,A26 | 5.0 | 5.0 |
| D7,E7,B26 | 5.0 | 5.0 |
| D8, E8, C26 | 0.2 | 0.2 |
| D9,E9, A27 | 0.2 | 0.2 |
| D10,E10,B27 | 0.2 | 0.2 |
| D18,E18,C27 | 0.2 | 0.2 |
| D19,E19,A28 | 0.2 | 0.2 |

Table 6-18. Per-Channel Parasitic Capacitance for 100-Pin QFP

| ADC CHANNEL | C _p (pF) | |
|------------------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0, B15, C15, DACA_OUT | 1.7 | 3.2 |
| A1, B7, D11, DACB_OUT, REFHI | 1.5 | 3.0 |
| A2, B6, C9, PGA1_INP | 1.7 | 3.2 |
| A3 | 5.4 | 6.9 |
| A4, B8, REFLO | 1.2 | 2.7 |
| A5 | 2.2 | 3.7 |
| A6, D14, E14 | 0.2 | 1.7 |
| A7, C3, D12, B30, E30 | 0.9 | 2.4 |
| A8, B0, C11 | 0.5 | 2.0 |
| A9 | 0.2 | 1.7 |
| A10, B1, C10 | 0.2 | 1.7 |
| A11, B10, C0, PGA2_OUT | 1.1 | 2.6 |
| A12 | 1.1 | 2.6 |
| A14, B14, C4, PGA1_OUT | 1.0 | 2.5 |
| A16/B16/C16 | 0.2 | 0.2 |
| A17,B17,C17 | 0.2 | 0.2 |
| A18,B18,C18 | 0.2 | 0.2 |
| A19,B19,C19 | 0.2 | 0.2 |
| A20,B20,C20 | 0.2 | 0.2 |
| B2, C6, E12 | 0.2 | 1.7 |
| B3, PGA2_INP | 0.2 | 1.7 |
| B4, C8 | 0.2 | 1.7 |
| B5, D15, E15 | 0.5 | 2.0 |
| B9, C7, PGA1_INM | 1.8 | 1.8 |
| B11, D16, E16 | 5.0 | 6.5 |
| B12, C2, PGA2_INM | 1.0 | 2.5 |
| C1,E11,PGA3_INP | 0.7 | 2.2 |

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Table 6-18. Per-Channel Parasitic Capacitance for 100-Pin QFP (continued)

| ADC CHANNEL | C _p (pF) | |
|-------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| C5 | 5.4 | 5.4 |
| C14 | 4.9 | 6.4 |
| D0,E0,A24 | 0.2 | 0.2 |
| D1,E1,B24 | 0.2 | 0.2 |
| D2,E2,C24 | 0.2 | 0.2 |
| D3,E3,A25 | 0.2 | 0.2 |
| D4,E4,B25 | 0.2 | 0.2 |

Table 6-19. Per-Channel Parasitic Capacitance for 80-Pin QFP

| ADC CHANNEL | C _p (pF) | |
|------------------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0, B15, C15, DACA_OUT | 1.7 | 3.2 |
| A1, B7, D11, DACB_OUT, REFHI | 1.5 | 3.0 |
| A2, B6, C9, PGA1_INP | 1.7 | 3.2 |
| A3 | 5.4 | 6.9 |
| A4, B8, REFLO | 1.2 | 2.7 |
| A5 | 2.2 | 3.7 |
| A6, D14, E14 | 0.2 | 1.7 |
| A7, C3, D12, B30,E30 | 0.9 | 2.4 |
| A8, B0, C11 | 0.5 | 2.0 |
| A9 | 0.2 | 1.7 |
| A10, B1, C10 | 0.2 | 1.7 |
| A11, B10, C0,PGA2_OUT | 1.1 | 2.6 |
| A12 | 1.1 | 2.6 |
| A14, B14, C4, PGA1_OUT | 1.0 | 2.5 |
| A15 | 0.5 | 2.0 |
| A16/B16/C16 | 0.2 | 0.2 |
| A17,B17,C17 | 0.2 | 0.2 |
| A18,B18,C18 | 0.2 | 0.2 |
| A19,B19,C19 | 0.2 | 0.2 |
| A20,B20,C20 | 0.2 | 0.2 |
| B2, C6, E12 | 0.2 | 1.7 |
| B3, PGA2_INP | 0.2 | 1.7 |
| B4, C8 | 0.2 | 1.7 |
| B9, C7, PGA1_INM | 1.8 | 1.8 |
| B12, C2, PGA2_INM | 1.0 | 2.5 |
| C1,E11,PGA3_INP | 0.7 | 2.2 |
| C5 | 5.4 | 5.4 |
| C14 | 4.9 | 6.4 |

Table 6-19. Per-Channel Parasitic Capacitance for 80-Pin QFP (continued)

| ADC CHANNEL | C _p (pF) | |
|-------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| D0,E0,A24 | 0.2 | 0.2 |
| D1,E1,B24 | 0.2 | 0.2 |
| D2,E2,C24 | 0.2 | 0.2 |
| D3,E3,A25 | 0.2 | 0.2 |
| D4,E4,B25 | 0.2 | 0.2 |

Table 6-20. Per-Channel Parasitic Capacitance for 64-Pin QFP

| ADC CHANNEL | C _p (pF) | |
|------------------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0, B15, C15, DACA_OUT | 1.7 | 3.2 |
| A1, B7, D11, DACB_OUT, REFHI | 1.5 | 3.0 |
| A2, B6, C9, PGA1_INP | 1.7 | 3.2 |
| A3 | 5.4 | 6.9 |
| A4, B8, REFLO | 1.2 | 2.7 |
| A5 | 2.2 | 3.7 |
| A6, D14, E14 | 0.2 | 1.7 |
| A7, C3, D12, B30, E30 | 0.9 | 2.4 |
| A8, B0, C11 | 0.5 | 2.0 |
| A9 | 0.2 | 1.7 |
| A10, B1, C10 | 0.2 | 1.7 |
| A11, B10, C0,PGA2_OUT | 1.1 | 2.6 |
| A12 | 1.1 | 2.6 |
| A14, B14, C4, PGA1_OUT | 1.0 | 2.5 |
| A15 | 0.5 | 2.0 |
| A16, B16, C16 | 0.2 | 0.2 |
| A17,B17,C17 | 0.2 | 0.2 |
| A18,B18,C18 | 0.2 | 0.2 |
| A19,B19,C19 | 0.2 | 0.2 |
| A20,B20,C20 | 0.2 | 0.2 |
| B2, C6, E12 | 0.2 | 1.7 |
| B3, PGA2_INP | 0.2 | 1.7 |
| B4, C8 | 0.2 | 1.7 |
| B9, C7, PGA1_INM | 1.8 | 1.8 |
| B12, C2, PGA2_INM | 1.0 | 2.5 |
| C1,E11,PGA3_INP | 0.7 | 2.2 |
| C5 | 5.4 | 5.4 |
| C14 | 4.9 | 6.4 |
| D0,E0,A24 | 0.2 | 0.2 |
| D1,E1,B24 | 0.2 | 0.2 |

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Table 6-20. Per-Channel Parasitic Capacitance for 64-Pin QFP (continued)

| ADC CHANNEL | C _p (pF) | |
|-------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| D2,E2,C24 | 0.2 | 0.2 |
| D3,E3,A25 | 0.2 | 0.2 |
| D4,E4,B25 | 0.2 | 0.2 |

Table 6-21. Per-Channel Parasitic Capacitance for 56-Pin QFN

| ADC CHANNEL | C _p (pF) | |
|------------------------------|---------------------|--------------------|
| | COMPARATOR DISABLED | COMPARATOR ENABLED |
| A0, B15, C15, DACA_OUT | 1.7 | 3.2 |
| A1, B7, D11, DACB_OUT, REFHI | 1.5 | 3.0 |
| A2, B6, C9, PGA1_INP | 1.7 | 3.2 |
| A3 | 5.4 | 6.9 |
| A4, B8, REFLO | 1.2 | 2.7 |
| A5 | 2.2 | 3.7 |
| A7, C3, D12, B30,E30 | 0.9 | 2.4 |
| A8, B0, C11 | 0.5 | 2.0 |
| A9 | 0.2 | 1.7 |
| A10, B1, C10 | 0.2 | 1.7 |
| A11, B10, C0,PGA2_OUT | 1.1 | 2.6 |
| A12 | 1.1 | 2.6 |
| A14, B14, C4, PGA1_OUT | 1.0 | 2.5 |
| A15 | 0.5 | 2.0 |
| A16,B16,C16 | 0.2 | 0.2 |
| A17,B17,C17 | 0.2 | 0.2 |
| A18,B18,C18 | 0.2 | 0.2 |
| A19,B19,C19 | 0.2 | 0.2 |
| A20,B20,C20 | 0.2 | 0.2 |
| B3, PGA2_INP | 0.2 | 1.7 |
| B4, C8 | 0.2 | 1.7 |
| B9, C7, PGA1_INM | 1.8 | 1.8 |
| B12, C2, PGA2_INM | 1.0 | 2.5 |
| C1,E11,PGA3_INP | 0.7 | 2.2 |
| C5 | 5.4 | 5.4 |
| C14 | 4.9 | 6.4 |
| D0,E0,A24 | 0.2 | 0.2 |
| D1,E1,B24 | 0.2 | 0.2 |
| D2,E2,C24 | 0.2 | 0.2 |
| D3,E3,A25 | 0.2 | 0.2 |
| D4,E4,B25 | 0.2 | 0.2 |

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6.14.4.2.5 ADC Timing Diagrams

The following diagrams show the ADC conversion timings for two SOC0s given the following assumptions:

- SOC0 and SOC1 are configured to use the same trigger.
- No other SOC0s are converting or pending when the trigger occurs.
- The round-robin pointer is in a state that causes SOC0 to convert first.
- ADCINTSEL is configured to set an ADCINT flag upon end of conversion for SOC0 (whether this flag propagates through to the CPU to cause an interrupt is determined by the configurations in the PIE module).

Table 6-22 lists the descriptions of the ADC timing parameters. Table 6-23 and Table 6-24 list the ADC timings.

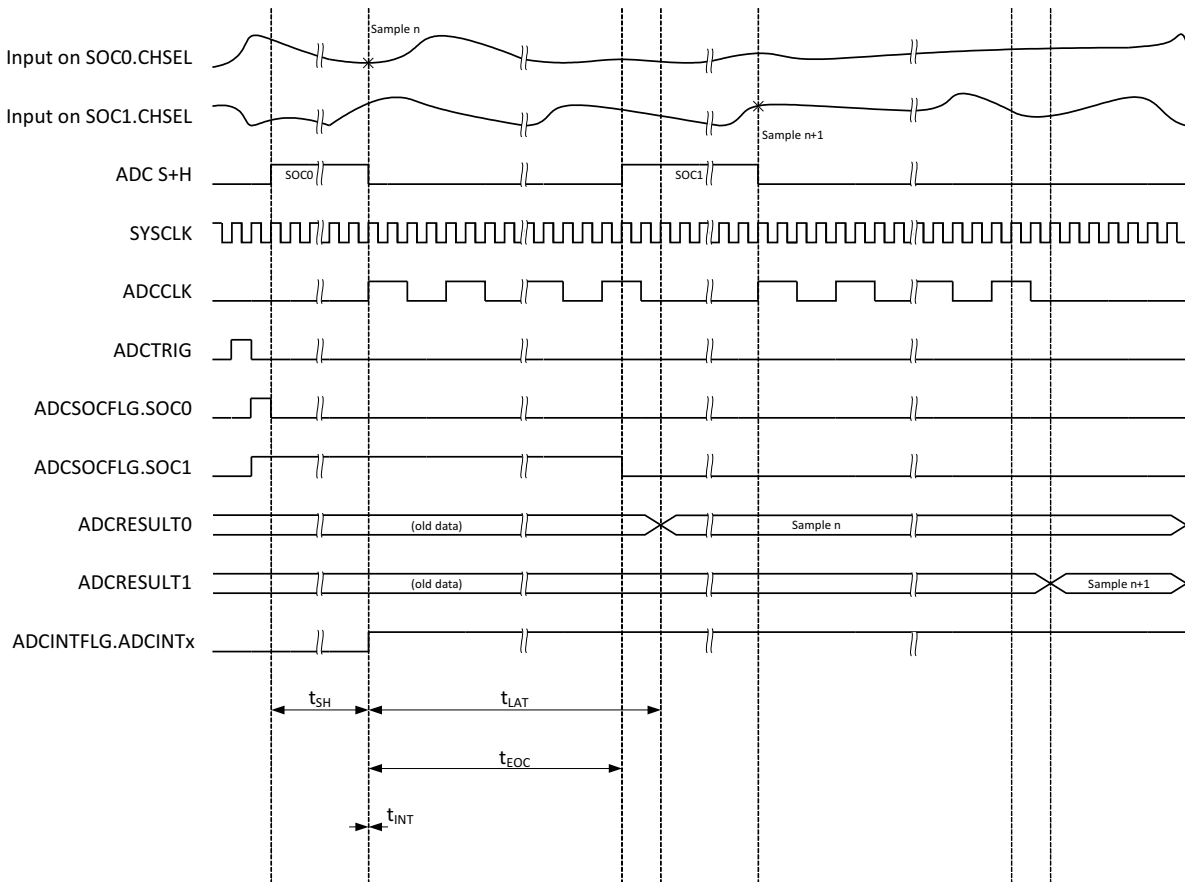


Figure 6-38. ADC Timings for 12-bit Mode in Early Interrupt Mode

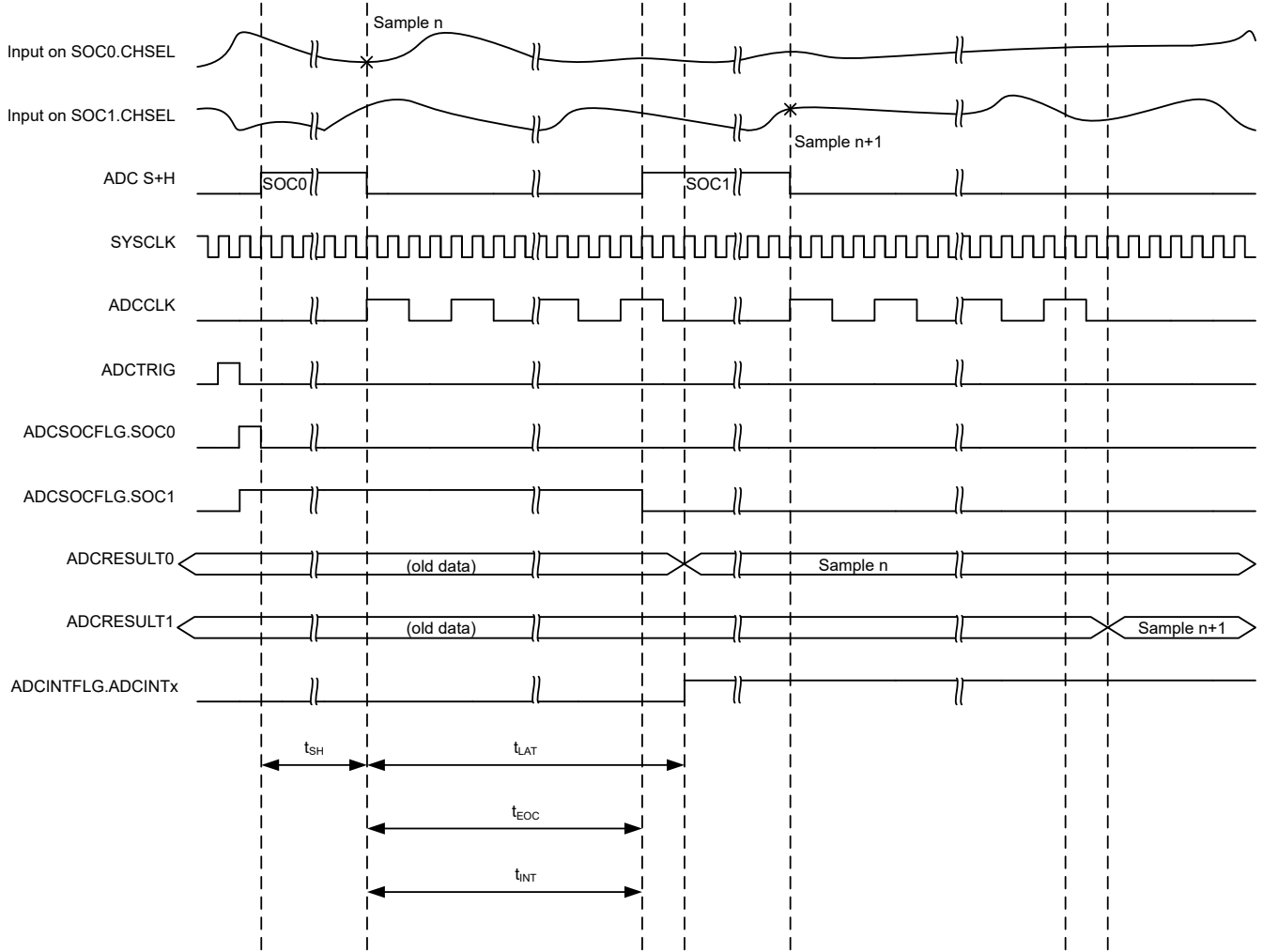


Figure 6-39. ADC Timings for 12-bit Mode in Late Interrupt Mode

Table 6-22. ADC Timing Parameter Descriptions

| PARAMETER | DESCRIPTION |
|-----------|---|
| t_{SH} | <p>The duration of the S+H window.</p> <p>At the end of this window, the value on the S+H capacitor becomes the voltage to be converted into a digital value. The duration is given by $(ACQPS + 1)$ SYSCLK cycles. ACQPS can be configured individually for each SOC, so t_{SH} is not necessarily the same for different SOCs.</p> <p>Note: The value on the S+H capacitor is captured approximately 5 ns before the end of the S+H window regardless of device clock settings.</p> |
| t_{LAT} | <p>The time from the end of the S+H window until the ADC results latch in the ADCRESULTx register.</p> <p>If the ADCRESULTx register is read before this time, the previous conversion results are returned.</p> |
| t_{EOC} | <p>The time from the end of the S+H window until the S+H window for the next ADC conversion can begin. The subsequent sample can start before the conversion results are latched.</p> |
| t_{INT} | <p>The time from the end of the S+H window until an ADCINT flag is set (if configured).</p> <p>If the INTPULSEPOS bit in the ADCCTL1 register is set, t_{INT} coincides with the end of conversion (EOC) signal.</p> <p>If the INTPULSEPOS bit is 0, t_{INT} coincides with the end of the S+H window. If t_{INT} triggers a read of the ADC result register (directly through DMA or indirectly by triggering an ISR that reads the result), care must be taken to make sure the read occurs after the results latch (otherwise, the previous results are read).</p> <p>If the INTPULSEPOS bit is 0, and the OFFSET field in the ADCINTCYCLE register is not 0, then there is a delay of OFFSET SYSCLK cycles before the ADCINT flag is set. This delay can be used to enter the ISR or trigger the DMA exactly when the sample is ready.</p> |
| t_{DMA} | <p>The time from the end of the S+H window until a DMA read of the ADC conversion result is triggered, when ADCCTL1.TDMAEN = 1.</p> <p>If TDMAEN is set to 0, then the DMA trigger occurs at T_{INT}. In certain conditions, the ADCINT flag can be set before the ADCRESULT value is latched. To make sure that the DMA read occurs after the ADCRESULT value has been latched, write 1 to ADCCTL1.TDMAEN to enable DMA timings.</p> |

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Table 6-23. ADC Timings in 12-bit Mode with SAMPCAPRESETSEL = 0

| ADCCLK Prescale | | SYSCLK Cycles | | | | |
|------------------|----------------|------------------|------------------|---|-------------------------|------------------|
| ADCCTL2.PRESCALE | Prescale Ratio | t _{Eoc} | t _{LAT} | t _{INT} (Early) ⁽¹⁾ | t _{INT} (Late) | t _{DMA} |
| 0 | 1 | 15 | 20 | 1 | 15 | 20 |
| 2 | 2 | 30 | 35 | 1 | 30 | 35 |
| 3 | 2.5 | 38 | 46 | 1 | 38 | 46 |
| 4 | 3 | 45 | 50 | 1 | 45 | 50 |
| 5 | 3.5 | 53 | 58 | 1 | 53 | 58 |
| 6 | 4 | 60 | 65 | 1 | 60 | 65 |
| 7 | 4.5 | 68 | 73 | 1 | 68 | 73 |
| 8 | 5 | 75 | 80 | 1 | 75 | 80 |
| 9 | 5.5 | 83 | 88 | 1 | 83 | 88 |
| 10 | 6 | 90 | 95 | 1 | 90 | 95 |
| 11 | 6.5 | 98 | 103 | 1 | 98 | 103 |
| 12 | 7 | 105 | 110 | 1 | 105 | 110 |
| 13 | 7.5 | 113 | 118 | 1 | 113 | 118 |
| 14 | 8 | 120 | 125 | 1 | 120 | 125 |
| 15 | 8.5 | 128 | 133 | 1 | 128 | 133 |

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

Table 6-24. ADC Timings in 12-bit Mode with SAMPCAPRESETSEL = 1

| ADCCLK Prescale | | SYSCLK Cycles | | | | |
|------------------|----------------|------------------|------------------|---|-------------------------|------------------|
| ADCCTL2.PRESCALE | Prescale Ratio | t _{Eoc} | t _{LAT} | t _{INT} (Early) ⁽¹⁾ | t _{INT} (Late) | t _{DMA} |
| 0 | 1 | 14 | 19 | 1 | 14 | 19 |
| 2 | 2 | 28 | 33 | 1 | 28 | 33 |
| 3 | 2.5 | 35 | 40 | 1 | 35 | 40 |
| 4 | 3 | 42 | 47 | 1 | 42 | 47 |
| 5 | 3.5 | 49 | 54 | 1 | 49 | 54 |
| 6 | 4 | 56 | 61 | 1 | 56 | 61 |
| 7 | 4.5 | 63 | 68 | 1 | 63 | 68 |
| 8 | 5 | 70 | 75 | 1 | 70 | 75 |
| 9 | 5.5 | 77 | 82 | 1 | 77 | 82 |
| 10 | 6 | 84 | 89 | 1 | 84 | 89 |
| 11 | 6.5 | 91 | 96 | 1 | 91 | 96 |
| 12 | 7 | 98 | 103 | 1 | 98 | 103 |
| 13 | 7.5 | 105 | 110 | 1 | 105 | 110 |
| 14 | 8 | 112 | 117 | 1 | 112 | 117 |
| 15 | 8.5 | 119 | 124 | 1 | 119 | 124 |

(1) By default, t_{INT} occurs one SYSCLK cycle after the S+H window if INTPULSEPOS is 0. This can be changed by writing to the OFFSET field in the ADCINTCYCLE register.

6.14.5 Temperature Sensor

6.14.5.1 Temperature Sensor Electrical Data and Timing

The temperature sensor can be used to measure the device junction temperature. The temperature sensor is sampled through an internal connection to the ADC and translated into a temperature through TI-provided software. When sampling the temperature sensor, the ADC must meet the acquisition time in the *Temperature Sensor Characteristics* table.

6.14.5.1.1 Temperature Sensor Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------|--|--------------------|-----|----------|-----|--------------------|
| T_{acc} | Temperature Accuracy | External reference | | ± 15 | | $^{\circ}\text{C}$ |
| $t_{startup}$ | Start-up time (TSNSCTL[ENABLE] to sampling temperature sensor) | | | 500 | | μs |
| t_{acq} | ADC acquisition time | | 450 | | | ns |

6.14.6 Comparator Subsystem (CMPSS)

The Comparator Subsystem (CMPSS) consists of analog comparators and supporting circuits that are useful for power applications such as peak current mode control, switched-mode power supply, power factor correction, voltage trip monitoring, and so forth.

The comparator subsystem is built around a number of modules. Each subsystem contains two comparators, two reference 12-bit DACs, and two digital filters. The subsystem also includes two ramp generators. The ramp generators ramp up and down. Comparators are denoted "H" or "L" within each module where "H" and "L" represent high and low, respectively. Each comparator generates a digital output which indicates whether the voltage on the positive input is greater than the voltage on the negative input. The positive input of the comparator is driven from an external pin (see the *Analog Subsystem* chapter of the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#) for mux options available to the CMPSS). The negative input can be driven by an external pin or by the programmable reference 12-bit DAC. Each comparator output passes through a programmable digital filter that can remove spurious trip signals. An unfiltered output is also available if filtering is not required. Two ramp generator circuits are optionally available to control the reference 12-bit DAC values for the high and low comparators in the subsystem. The DAC along with a wrapper can be used to generate a ramp which is used for slope compensation in Peak Current Mode Control (PCMC) and other applications.

Each CMPSS includes:

- Two analog comparators
- Two independently programmable reference 12-bit DACs
- Dual decrementing/incrementing ramp generators
- Two digital filters with max filter clock prescale of 2^{24}
- Ability to synchronize submodules with EPWMSYNCPER
- Ability to extend clear signal with EPWMBLANK
- Ability to synchronize output with SYSCLK
- Ability to latch output
- Ability to invert output
- Option to use hysteresis on the input
- Option for negative input of comparator to be driven by an external signal or by the reference DAC
- Option for positive input of comparator to be driven by an external signal or by the PGA
- Option to use the low comparator DAC output, CMPx_DACL, on an external pin (select instances only, mutually exclusive with use of compare functionality)
- External connection to CMPSS filters
- Supports connection with ePWM for diode emulation
- Ramp generator prescaler
- Wake-up from standby and halt LPM (Low Power Modes) triggered by CMPSS trip outputs

6.14.6.1 CMPx_DACL

Some CMPSS module instances have support for DAC output buffered to a pin. This CMPx_DACL output from the CMPSS module uses the low-side DAC of the CMPSS module specified. When using DAC output from a CMPSS instance, all other CMPSS module features for that instance are unavailable.

For CMPx_DACL instances available for a particular device, please see the DAC column of the *Analog Pins and Internal Connections* table.

See the *Buffered Output from CMPx_DACL Electrical Characteristics* section for DAC output capabilities.

6.14.6.2 CMPSS Connectivity Diagram

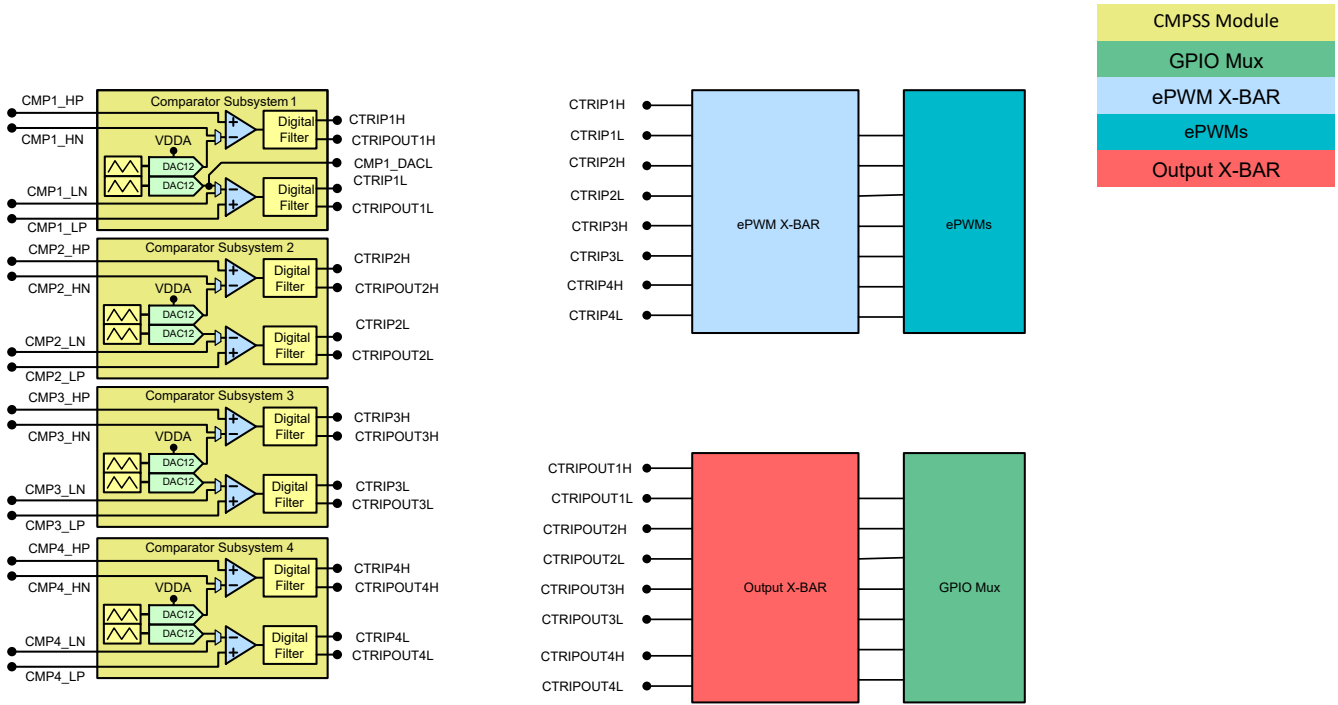


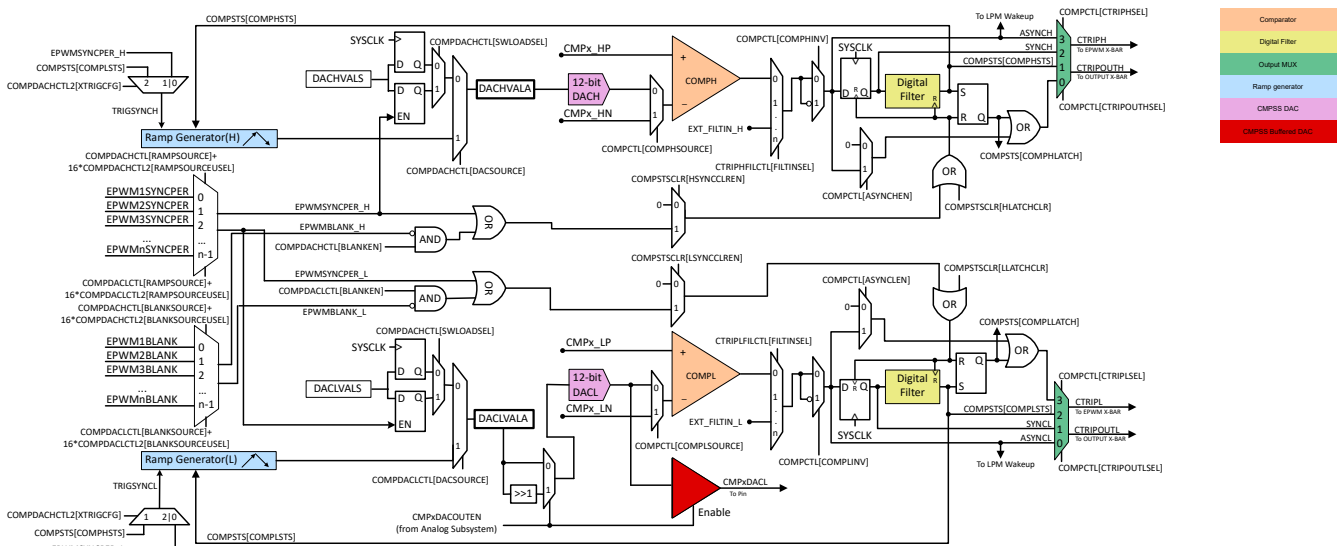
Figure 6-40. CMPSS Connectivity

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6.14.6.3 Block Diagram

The block diagram for the CMPSS is shown in Figure 6-41.

- CTRIPx(x= "H" or "L") signals are connected to the ePWM X-BAR for ePWM trip response. See the *Enhanced Pulse Width Modulator (ePWM)* chapter of the for more details on the ePWM X-BAR mux configuration.
- CTRIPxOUTx(x= "H" or "L") signals are connected to the Output X-BAR for external signaling. See the *General-Purpose Input/Output (GPIO)* chapter of the for more details on the Output X-BAR mux configuration.



- CMPxDACL only exists for the CMPSS 1 module on this device.
- Enabling the DACL to a pin disables all other functionality: DACH, both COMP, the Ramp Generator, and the digital filters.

Figure 6-41. CMPSS Module Block Diagram

Each reference 12-bit DAC can be configured to drive a reference voltage into the negative input of the respective comparator. Some CMPSS instances also allow the low DAC output to be routed to a pin to act as an external DAC. In this case, all other CMPSS module functionality is not useable, including the high DAC, both comparators, ramp generation, and the digital filters. The reference 12-bit DAC is illustrated in Figure 6-42.

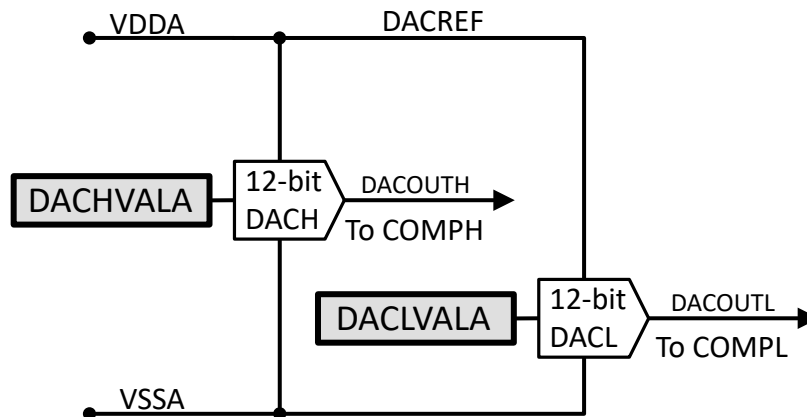


Figure 6-42. Reference DAC Block Diagram

6.14.6.4 CMPSS Electrical Data and Timing

6.14.6.4.1 CMPSS Comparator Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|------------------------------|--|-----|-----|------|------|
| TPU | Power-up time | | | | 500 | μs |
| Comparator input (CMPINxx) range | | | 0 | | VDDA | V |
| Input referred offset error | | Low common mode, inverting input set to 50mV | -20 | | 20 | mV |
| Hysteresis ⁽¹⁾ | 1x | | 4 | 12 | 20 | LSB |
| | 2x | | 17 | 24 | 33 | |
| | 3x | | 25 | 36 | 50 | |
| | 4x | | 30 | 48 | 67 | |
| Response time (delay from CMPINx input change to output on ePWM X-BAR or Output X-BAR) | Step response | | | 21 | 60 | ns |
| | Ramp response (1.65V/μs) | | | 26 | | |
| | Ramp response (8.25mV/μs) | | | 30 | | ns |
| PSRR | Power Supply Rejection Ratio | Up to 250 kHz | | 46 | | dB |
| CMRR | Common Mode Rejection Ratio | | 40 | | | dB |

(1) The CMPSS DAC is used as the reference to determine how much hysteresis to apply. Therefore, hysteresis will scale with the CMPSS DAC reference voltage. Hysteresis is available for all comparator input source configurations.

CMPSS Comparator Input Referred Offset and Hysteresis

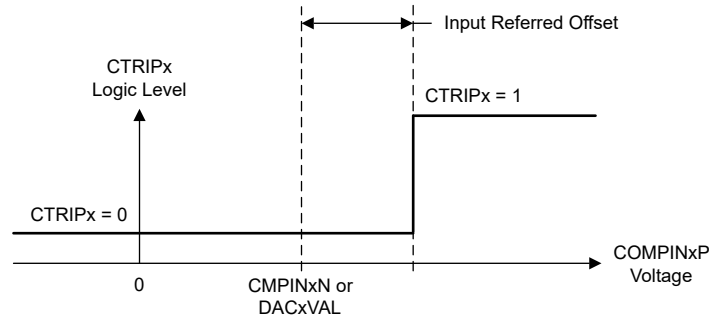


Figure 6-43. CMPSS Comparator Input Referred Offset

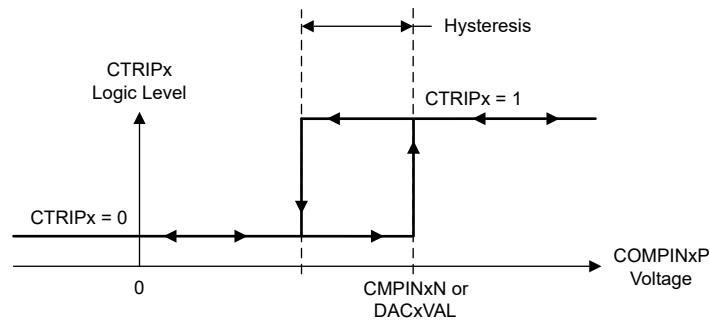


Figure 6-44. CMPSS Comparator Hysteresis

6.14.6.4.2 CMPSS DAC Static Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|------|-----|------|----------|
| CMPSS DAC output range | Internal reference | 0 | | VDDA | V |
| Static offset error ⁽¹⁾ | | -25 | | 25 | mV |
| Static gain error ⁽¹⁾ | | -2 | | 2 | % of FSR |
| Static DNL | Endpoint corrected | >-1 | | 4 | LSB |
| Static INL | Endpoint corrected | -16 | | 16 | LSB |
| Settling time | Settling to 1LSB after full-scale output change | | | 1 | μs |
| Resolution | | | 12 | | bits |
| CMPSS DAC output disturbance ⁽²⁾ | Error induced by comparator trip or CMPSS DAC code change within the same CMPSS module | -100 | | 100 | LSB |
| CMPSS DAC disturbance time ⁽²⁾ | | | | 200 | ns |

- (1) Includes comparator input referred errors.
- (2) Disturbance error may be present on the CMPSS DAC output for a certain amount of time after a comparator trip.

6.14.6.4.3 CMPSS Illustrative Graphs

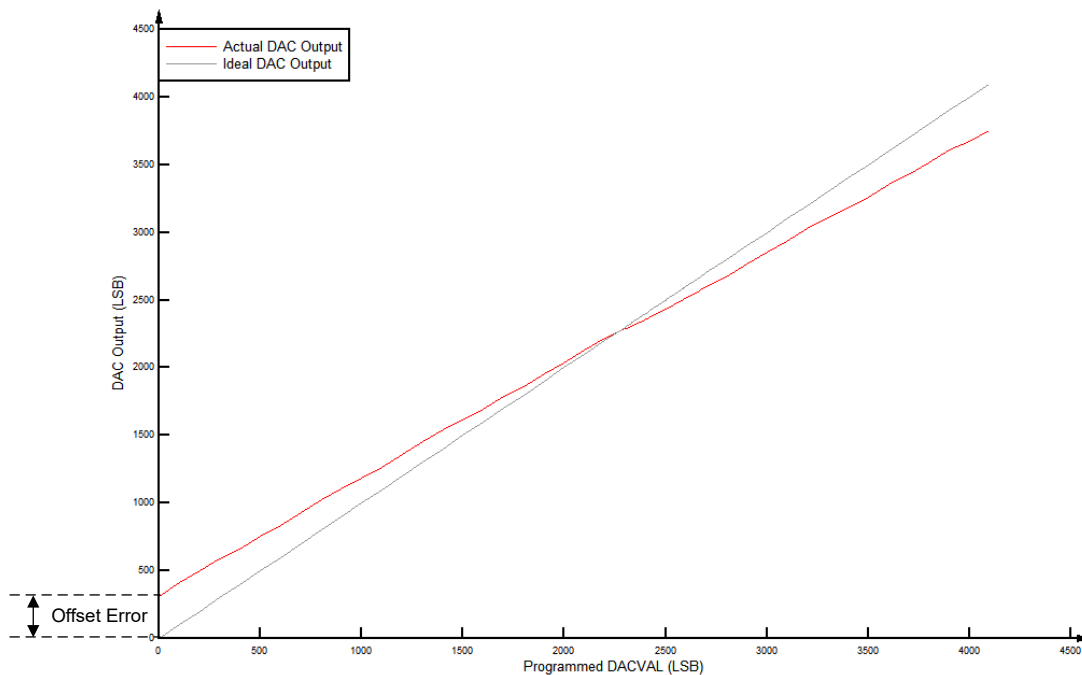


Figure 6-45. CMPSS DAC Static Offset

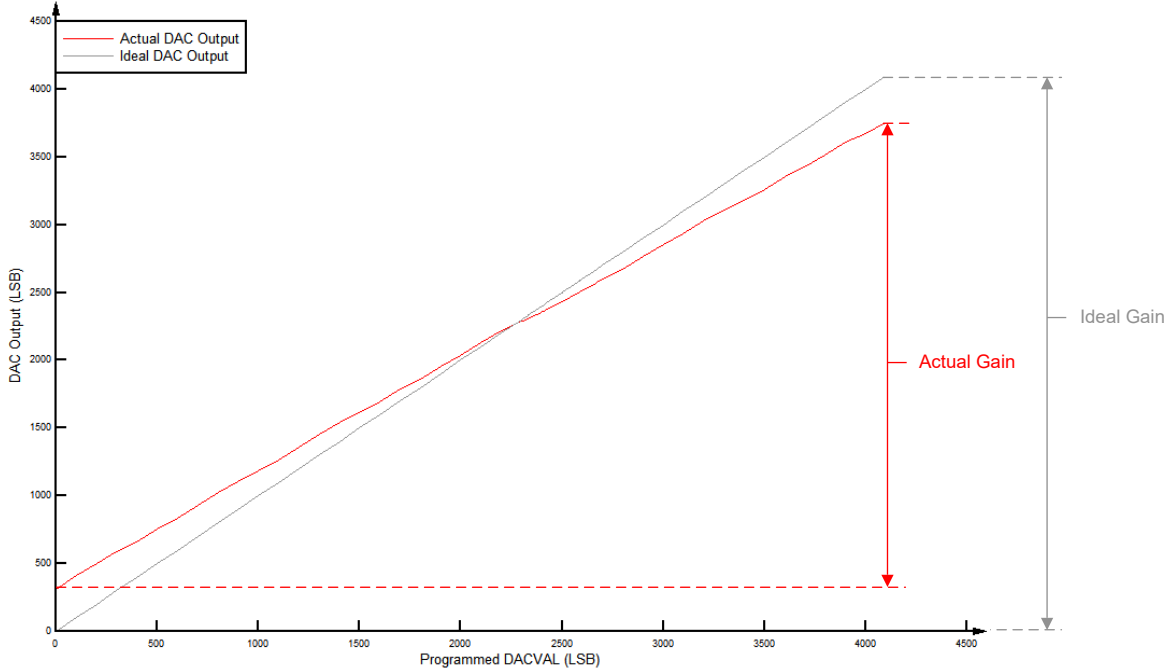


Figure 6-46. CMPSS DAC Static Gain

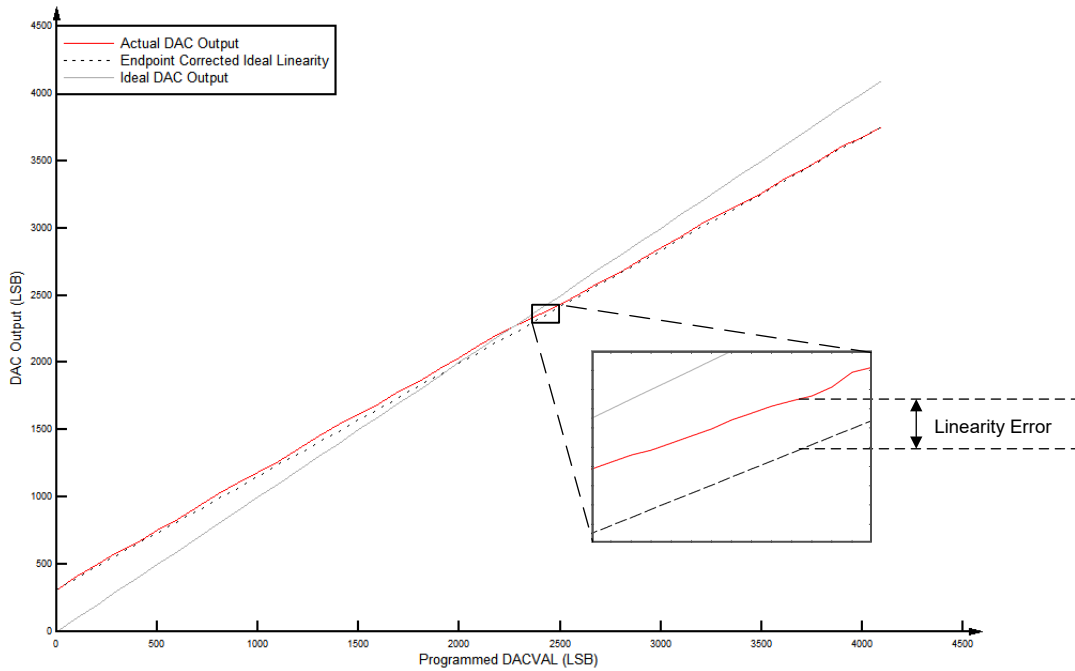


Figure 6-47. CMPSS DAC Static Linearity

6.14.6.4.4 Buffered Output from CMPx_DACL Operating Conditions
 over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|-------------------------------|-----|-----|-----|------|
| R _L | Resistive Load ⁽²⁾ | 5 | | | kΩ |
| C _L | Capacitive Load | | | 100 | pF |

6.14.6.4.4 Buffered Output from CMPx_DACL Operating Conditions (continued)

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|---|-----------------------|-----|------------|------------|------|
| V _{OUT} | Valid Output Voltage Range ⁽³⁾ | R _L = 5 kΩ | 0.3 | | VDDA – 0.3 | V |
| | | R _L = 1 kΩ | 0.6 | | VDDA – 0.6 | V |
| Reference Voltage ⁽⁴⁾ | | VREFHI | 2.4 | 2.5 or 3.0 | VDDA | V |

- (1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
- (2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
- (3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
- (4) For best PSRR performance, VREFHI should be less than VDDA.

6.14.6.4.5 Buffered Output from CMPx_DACL Electrical Characteristics

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|------|-------|-----|--------------|
| General | | | | | | |
| Resolution ⁽⁴⁾ | | | | 12 | | bits |
| Load Regulation | | | –1 | | 1 | mV/V |
| Glitch Energy | | | | 1.5 | | V-ns |
| Voltage Output Settling Time Full-Scale | | Settling to 2 LSBs after 0.3V-to-3V transition | | | 2 | μs |
| Voltage Output Settling Time 1/4 th Full-Scale | | Settling to 2 LSBs after 0.3V-to-0.75V transition | | | 1.6 | μs |
| Voltage Output Slew Rate | | Slew rate from 0.3V-to-3V transition | 2.8 | | 4.5 | V/μs |
| Load Transient Settling Time | | 5-kΩ Load | | | 328 | ns |
| TPU | Power Up Time | Bandgap Not Enabled | | | 500 | μs |
| DC Characteristics | | | | | | |
| Offset | Offset Error | | –100 | | 100 | mV |
| Gain | Gain Error ⁽²⁾ | | –1.5 | | 1.5 | % of FSR |
| DNL | Differential Non Linearity ⁽⁴⁾ | Endpoint corrected | –2 | | 2 | LSB (12-bit) |
| INL | Integral Non Linearity | Endpoint corrected | –7 | | 7 | LSB (12-bit) |
| AC Characteristics | | | | | | |
| Output Noise | | Integrated noise from 100 Hz to 100 kHz | | 600 | | μVrms |
| | | Noise density at 10 kHz | | 800 | | nVrms/√Hz |
| SNR | Signal to Noise Ratio | 1 kHz, 200 KSPS | | 64 | | dB |
| THD | Total Harmonic Distortion | 1 kHz, 200 KSPS | | –64.2 | | dB |
| SFDR | Spurious Free Dynamic Range | 1 kHz, 200 KSPS | | 66 | | dB |
| SINAD | Signal to Noise and Distortion Ratio | 1 kHz, 200 KSPS | | 61.7 | | dB |
| PSRR | Power Supply Rejection Ratio ⁽³⁾ | DC | | 70 | | dB |
| | | 100 kHz | | 30 | | dB |

- (1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
- (2) Gain error is calculated for linear output range.
- (3) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.
- (4) 11-bit effective (monotonic response).

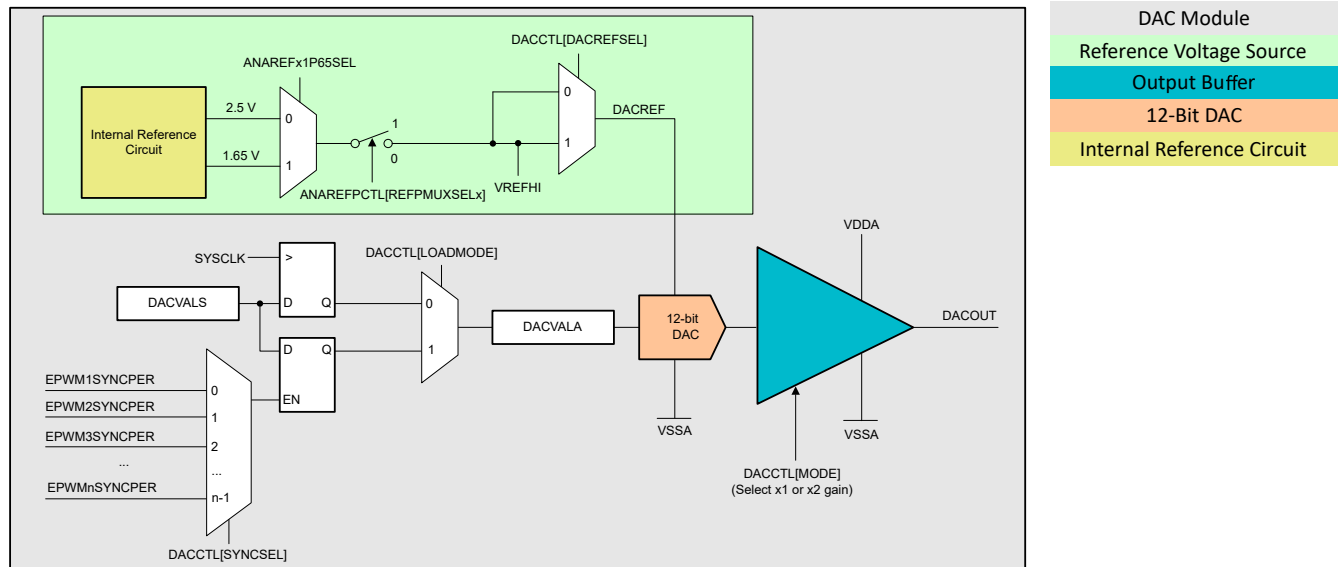
6.14.7 Buffered Digital-to-Analog Converter (DAC)

The buffered DAC module consists of an internal 12-bit DAC and an analog output buffer that can drive an external load. For driving even higher loads than typical, a trade-off can be made between load size and output voltage swing. For the load conditions of the buffered DAC, see the *Buffered DAC Electrical Data and Timing* section. The buffered DAC is a general-purpose DAC that can be used to generate a DC voltage or AC waveforms such as sine waves, square waves, triangle waves and so forth. Software writes to the DAC value register can take effect immediately or can be synchronized with EPWMSYNCO events.

Each buffered DAC has the following features:

- 12-bit resolution
- Selectable reference voltage source
- x1 and x2 gain modes when using internal VREFHI
- Ability to synchronize with EPWMSYNCPER

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A. VDAC is not available for this device; so, VREFHI and VSSA are the reference voltages.

Figure 6-48. DAC Module Block Diagram

6.14.7.1 Buffered DAC Electrical Data and Timing

6.14.7.1.1 Buffered DAC Operating Conditions

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------------|---|-----------------------|-----|------------|------------|------|
| R _L | Resistive Load ⁽²⁾ | | 5 | | | kΩ |
| C _L | Capacitive Load | | | | 100 | pF |
| V _{OUT} | Valid Output Voltage Range ⁽³⁾ | R _L = 5 kΩ | 0.3 | | VDDA – 0.3 | V |
| | | R _L = 1 kΩ | 0.6 | | VDDA – 0.6 | V |
| Reference Voltage ⁽⁴⁾ | | VREFHI | 2.4 | 2.5 or 3.0 | VDDA | V |

- (1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
- (2) DAC can drive a minimum resistive load of 1 kΩ, but the output range will be limited.
- (3) This is the linear output range of the DAC. The DAC can generate voltages outside this range, but the output voltage will not be linear due to the buffer.
- (4) For best PSRR performance, VREFHI should be less than VDDA.

6.14.7.1.2 Buffered DAC Electrical Characteristics

over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|------|-------|------|-----------|
| General | | | | | | |
| Resolution | | | | 12 | | bits |
| Load Regulation | | | –1 | | 1 | mV/V |
| Glitch Energy | | | | 1.5 | | V-ns |
| Voltage Output Settling Time Full-Scale | | Settling to 2 LSBs after 0.3V-to-3V transition | | | 2 | μs |
| Voltage Output Settling Time 1/4 th Full-Scale | | Settling to 2 LSBs after 0.3V-to-0.75V transition | | | 1.6 | μs |
| Voltage Output Slew Rate | | Slew rate from 0.3V-to-3V transition | 2.8 | | 4.5 | V/μs |
| Load Transient Settling Time | | 5-kΩ Load | | | 328 | ns |
| | | 1-kΩ Load | | | 557 | ns |
| Reference Input Resistance ⁽²⁾ | | VREFHI | 160 | 200 | 240 | kΩ |
| TPU | Power Up Time | External Reference mode | | | 500 | μs |
| | | Internal Reference mode | | | 5000 | μs |
| DC Characteristics | | | | | | |
| Offset | Offset Error | Midpoint | –10 | | 10 | mV |
| Gain | Gain Error ⁽³⁾ | | –2.5 | | 2.5 | % of FSR |
| DNL | Differential Non Linearity ⁽⁴⁾ | Endpoint corrected | –1 | ±0.4 | 1 | LSB |
| INL | Integral Non Linearity | Endpoint corrected | –5 | ±2 | 5 | LSB |
| AC Characteristics | | | | | | |
| Output Noise | | Integrated noise from 100 Hz to 100 kHz | | 600 | | μVrms |
| | | Noise density at 10 kHz | | 800 | | nVrms/√Hz |
| SNR | Signal to Noise Ratio | 1 kHz, 200 KSPS | | 64 | | dB |
| THD | Total Harmonic Distortion | 1 kHz, 200 KSPS | | –64.2 | | dB |
| SFDR | Spurious Free Dynamic Range | 1 kHz, 200 KSPS | | 66 | | dB |
| SINAD | Signal to Noise and Distortion Ratio | 1 kHz, 200 KSPS | | 61.7 | | dB |

6.14.7.1.2 Buffered DAC Electrical Characteristics (continued)

 over recommended operating conditions (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|---|-----------------|-----|-----|-----|------|
| PSRR | Power Supply Rejection Ratio ⁽⁵⁾ | DC | | 70 | | dB |
| | | 100 kHz | | 30 | | dB |

- (1) Typical values are measured with VREFHI = 3.3 V and VREFLO = 0 V, unless otherwise noted. Minimum and maximum values are tested or characterized with VREFHI = 2.5 V and VREFLO = 0 V.
- (2) Per active Buffered DAC module.
- (3) Gain error is calculated for linear output range.
- (4) The DAC output is monotonic.
- (5) VREFHI = 3.2 V, VDDA = 3.3 V DC + 100 mV Sine.

6.14.8.1 PGA Electrical Data and Timing

6.14.8.1.1 PGA Operating Conditions

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|-----------------|------------|-----|------------|------|
| PGA Output Range ⁽¹⁾ | | VSSA+0.025 | | VDDA-0.025 | V |
| Cap Load on PGA Out | | | 40 | | pF |

(1) This is the linear output range of the PGA. The PGA can output voltages outside this range, but the voltages will not be linear.

6.14.8.1.2 PGA Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|-----|------------------------------|-----|------------|
| General | | | | | |
| Min ADC S+H (No Filter; All Gain Settings; Single ADC Driven) | Settling within ± 1 ADC LSB Accuracy | | 400 | | ns |
| Min ADC S+H (No Filter; All Gain Settings; Two ADC Driven) | Settling within ± 1 ADC LSB Accuracy | | 450 | | ns |
| Min ADC S+H (With Filter; All Gain Settings) | Settling within ± 1 ADC LSB Accuracy | | 450 ⁽⁵⁾ | | ns |
| Gain Settings | | | 1 | | |
| | | | 2, 4, 8, 16, 32, 64 | | |
| | | | -1, -3, -7, -15, -31, -63 | | |
| Input Bias Current | | | 2 | | nA |
| Short Circuit Current | | | 41 | | mA |
| Full Scale Step Response (No Filter) | Settling within ± 1 ADC LSB Accuracy | | 450 | | ns |
| Settling Time | Gain Switching | | 10 | | μ s |
| Slew Rate | Naked OPA Mode | | 10.9 | | V/ μ s |
| Slew Rate | Gain = 1 | | 10 | | V/ μ s |
| | Gain = 2/-1 | | 21 | | V/ μ s |
| | Gain = 4/-3 | | 39 | | V/ μ s |
| | Gain = 8/-7 | | 56 | | V/ μ s |
| | Gain = 16/-15 | | 46 | | V/ μ s |
| | Gain = 32/-31 | | 29 | | V/ μ s |
| | Gain = 64/-63 | | 25 | | V/ μ s |
| R _{ia} | Gain = 1 | | 256 | | k Ω |
| | Gain = 2/-1 | | 16 | | k Ω |
| | Gain = 4/-3 | | 8 | | k Ω |
| | Gain = 8/-7 | | 8 | | k Ω |
| | Gain = 16/-15 | | 8 | | k Ω |
| | Gain = 32/-31 | | 8 | | k Ω |
| | Gain = 64/-63 | | 4 | | k Ω |

6.14.8.1.2 PGA Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|---------------------------|-----|---------|-----|-------------|
| R _{ib} | Gain = 1 | | 0 | | kΩ |
| | Gain = 2/-1 | | 16 | | kΩ |
| | Gain = 4/-3 | | 24 | | kΩ |
| | Gain = 8/-7 | | 56 | | kΩ |
| | Gain = 16/-15 | | 128 | | kΩ |
| | Gain = 32/-31 | | 248 | | kΩ |
| | Gain = 64/-63 | | 252 | | kΩ |
| Filter Resistor Targets | R _{FILT} = 800 Ω | | 800 | | Ω |
| | R _{FILT} = 400 Ω | | 400 | | Ω |
| | R _{FILT} = 200 Ω | | 200 | | Ω |
| | R _{FILT} = 100 Ω | | 100 | | Ω |
| | R _{FILT} = 50 Ω | | 50 | | Ω |
| Gain Bandwidth Product | Gain=1 | | 7 | | MHz |
| Gain Bandwidth Product | Gain=1 | | 7 | | MHz |
| Closed Loop -3bd BW | Gain=1 | | 15 | | MHz |
| | Gain=2/-1 | | 13.7 | | MHz |
| | Gain=4/-3 | | 10.5 | | MHz |
| | Gain=8/-7 | | 9.5 | | MHz |
| | Gain=16/-15 | | 5.8 | | MHz |
| | Gain=32/-31 | | 3.8 | | MHz |
| | Gain=64/-63 | | 3.25 | | MHz |
| | DC Characteristics | | | | |
| Gain Error ⁽¹⁾ | Gain = 1 | | +/-0.18 | | % |
| Gain Error ⁽¹⁾ | Gain = 2, -1 | | +/-0.37 | | % |
| Gain Error ⁽¹⁾ | Gain = 4, -3 | | +/-0.6 | | % |
| Gain Error ⁽¹⁾ | Gain = 8, -7 | | +/-0.73 | | % |
| Gain Error ⁽¹⁾ | Gain = 16, -15 | | +/-0.81 | | % |
| Gain Error ⁽¹⁾ | Gain = 32, -31 | | +/-1.0 | | % |
| Gain Error ⁽¹⁾ | Gain = 64, -63 | | +/-1.82 | | % |
| Offset Error ⁽²⁾ | Input Referred | | +/-1.0 | | mV |
| Offset Temp Coefficient | Input Referred | | ±3.0 | | μV/C |
| Offset Error - Chopped | | | +/-0.8 | | mV |
| Offset Temp Coefficient - Chopped | | | 0.3 | | μV/C |
| DC Code Spread | | | 2.5 | | 12b LSB |
| AC Characteristics | | | | | |
| Bandwidth ⁽³⁾ | All Gain Modes | | 7 | | MHz |
| THD ⁽⁴⁾ | DC | | -78 | | dB |
| | Up to 100 kHz | | -70 | | dB |
| CMRR | DC | | -60 | | dB |
| | Up to 100 kHz | | -50 | | dB |
| PSRR ⁽⁴⁾ | DC | | -75 | | dB |
| | Up to 100 kHz | | -50 | | dB |
| Noise PSD ⁽⁴⁾ | 1 kHz | | 200 | | nV/sqrt(Hz) |

6.14.8.1.2 PGA Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|-----------------|-----|-----|-----|------|
| Integrated Noise (Input Referred) ⁽⁴⁾ | 3 Hz to 30 MHz | | 100 | | μV |

- (1) Includes ADC gain error.
- (2) Includes ADC offset error.
- (3) 3dB bandwidth.
- (4) Performance of PGA alone.
- (5) Step response time (max) = 450ns + 7.6*R_{filt}* C_{filt}

6.15 Control Peripherals

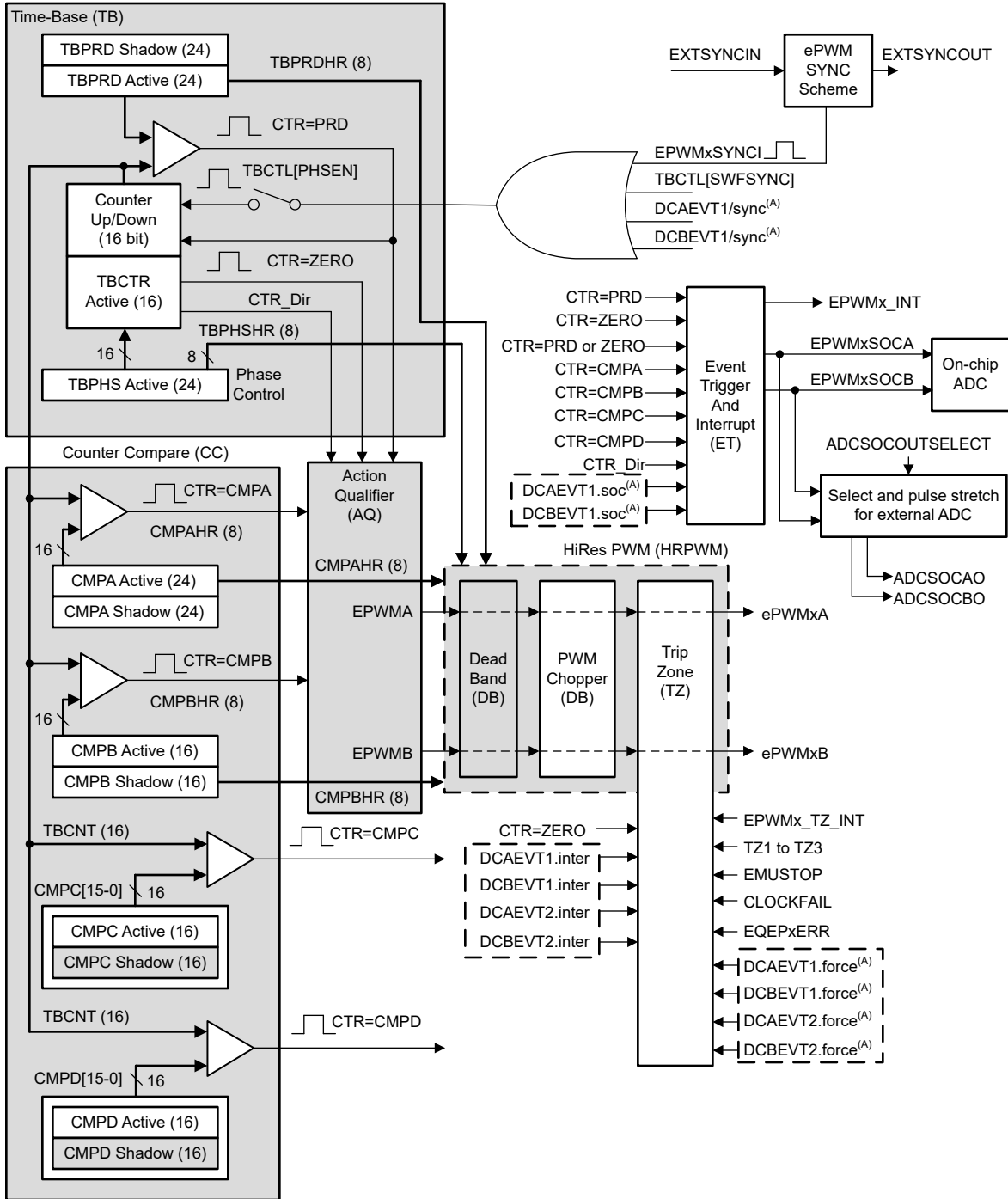
6.15.1 Enhanced Pulse Width Modulator (ePWM)

The ePWM peripheral is a key element in controlling many of the power electronic systems found in both commercial and industrial equipment. The ePWM type-4 module is able to generate complex pulse width waveforms with minimal CPU overhead by building the peripheral up from smaller modules with separate resources that can operate together to form a system. Some of the highlights of the ePWM type-4 module include complex waveform generation, dead-band generation, a flexible synchronization scheme, advanced trip-zone functionality, and global register reload capabilities.

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules.

[Figure 6-50](#) shows the ePWM module. [Figure 6-51](#) shows the ePWM trip input connectivity.

ADVANCE INFORMATION



A. These events are generated by the ePWM digital compare (DC) submodule based on the levels of the TRIPIN inputs.

Figure 6-50. ePWM Submodules and Critical Internal Signal Interconnects

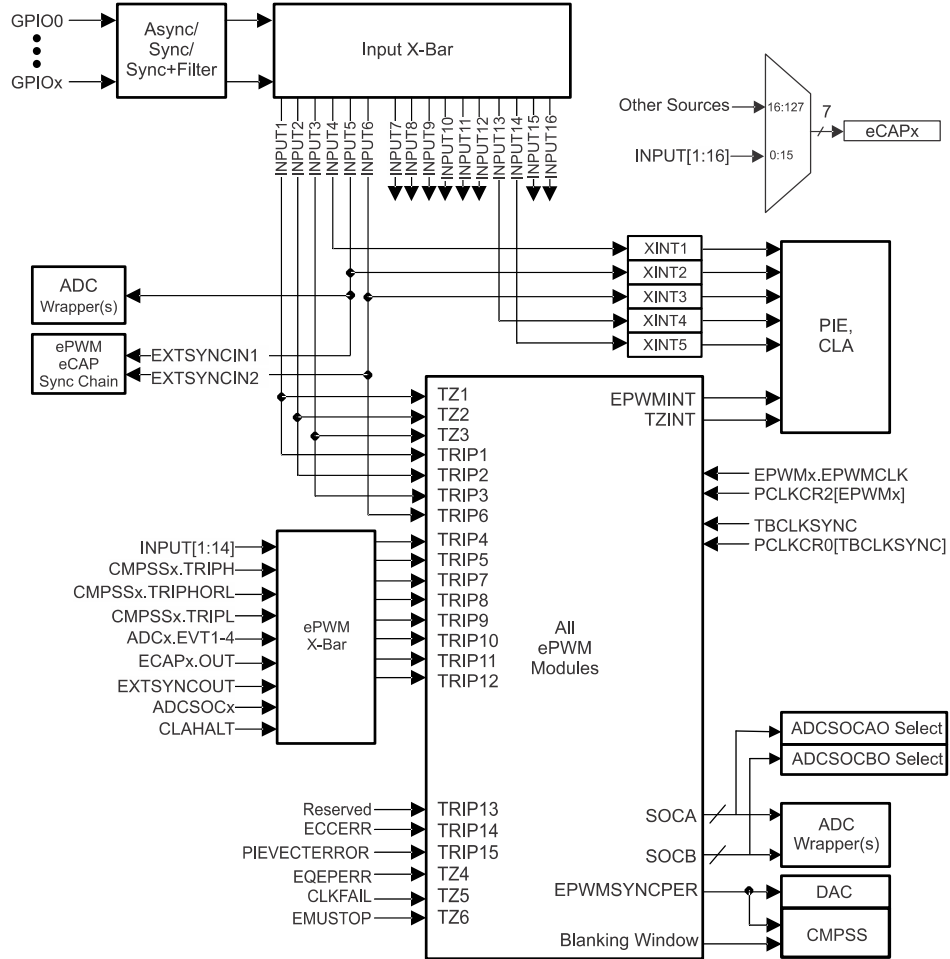


Figure 6-51. ePWM Trip Input Connectivity

ADVANCE INFORMATION

6.15.1.1 Control Peripherals Synchronization

The ePWM and eCAP synchronization scheme on the device provides flexibility in partitioning the ePWM and eCAP modules and allows localized synchronization within the modules. Figure 6-52 shows the synchronization scheme.

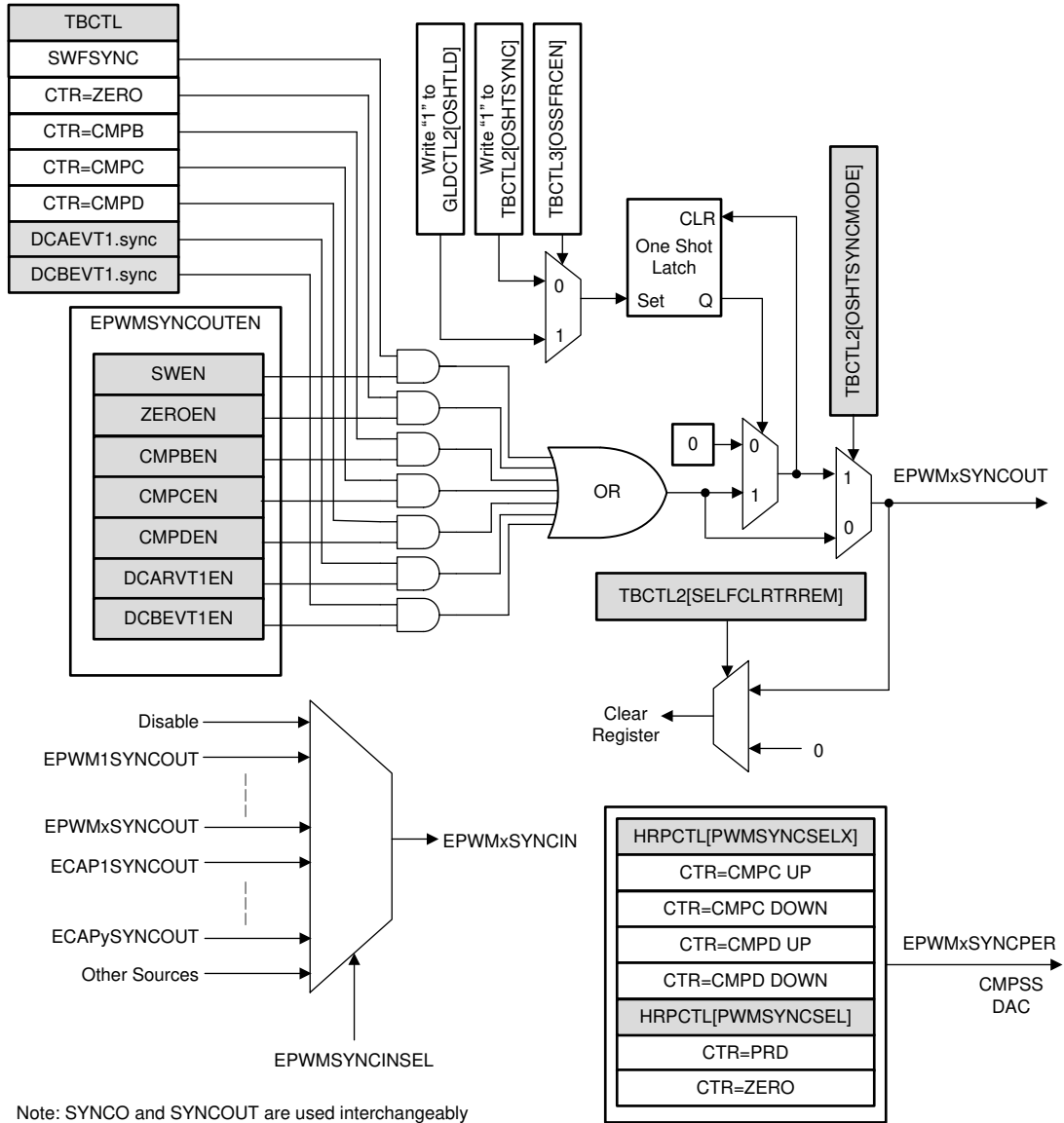


Figure 6-52. Synchronization Chain Architecture

6.15.1.2 ePWM Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.15.1.2.1 ePWM Timing Requirements

| | | | MIN | MAX | UNIT |
|------------------------|------------------------|----------------------|---|-----|--------|
| $t_{w(\text{SYNCIN})}$ | Sync input pulse width | Asynchronous | $2t_{c(\text{EPWMCLK})}$ | | cycles |
| | | Synchronous | $2t_{c(\text{EPWMCLK})}$ | | |
| | | With input qualifier | $1t_{c(\text{EPWMCLK})} + t_{w(\text{IQSW})}$ | | |

6.15.1.2.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|--------------------------|--|-------------------------|-----|--------|
| $t_{w(\text{PWM})}$ | Pulse duration, PWMx output high/low | 20 | | ns |
| $t_{w(\text{SYNCOUT})}$ | Sync output pulse width | $8t_{c(\text{SYSCLK})}$ | | cycles |
| $t_{d(\text{TZ-PWM})}$ | Delay time, trip input active to PWM forced high | | 25 | ns |
| | Delay time, trip input active to PWM forced low | | | |
| | Delay time, trip input active to PWM Hi-Z | | | |

(1) 20-pF load on pin.

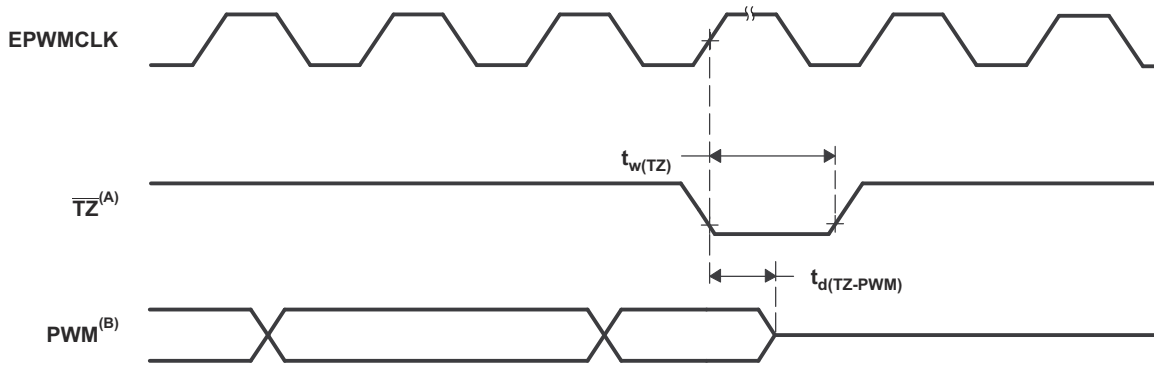
6.15.1.2.3 Trip-Zone Input Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.15.1.2.3.1 Trip-Zone Input Timing Requirements

| | | | MIN | MAX | UNIT |
|--------------------|---|----------------------|---|-----|--------|
| $t_{w(\text{TZ})}$ | Pulse duration, $\overline{\text{TZx}}$ input low | Asynchronous | $1t_{c(\text{EPWMCLK})}$ | | cycles |
| | | Synchronous | $2t_{c(\text{EPWMCLK})}$ | | cycles |
| | | With input qualifier | $1t_{c(\text{EPWMCLK})} + t_{w(\text{IQSW})}$ | | cycles |

6.15.1.2.3.2 PWM Hi-Z Characteristics Timing Diagram



A. TZ: TZ1, TZ2, TZ3, TRIP1–TRIP12

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after TZ is taken high depends on the PWM recovery software.

Figure 6-53. PWM Hi-Z Characteristics

6.15.2 High-Resolution Pulse Width Modulator (HRPWM)

The HRPWM combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module, there are two HR outputs:

- HR Duty and Deadband control on Channel A
- HR Duty and Deadband control on Channel B

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A, B, phase, period and deadband registers of the ePWM module.

6.15.2.1 HRPWM Electrical Data and Timing

6.15.2.1.1 High-Resolution PWM Characteristics

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|-----|-----|-----|------|
| Micro Edge Positioning (MEP) step size ⁽¹⁾ | | 150 | 310 | ps |

- (1) The MEP step size will be largest at high temperature and minimum voltage on V_{DD} . MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage. Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO functions in end applications. SFO functions help to estimate the number of MEP steps per SYSCLK period dynamically while the HRPWM is in operation.

6.15.3 External ADC Start-of-Conversion Electrical Data and Timing

6.15.3.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | MIN | MAX | UNIT |
|--|-------------------|-----|--------|
| $t_{w(ADCSOCL)}$ Pulse duration, $\overline{ADCSOCxO}$ low | $32t_{c(SYSCLK)}$ | | cycles |

6.15.3.2 $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing Diagram

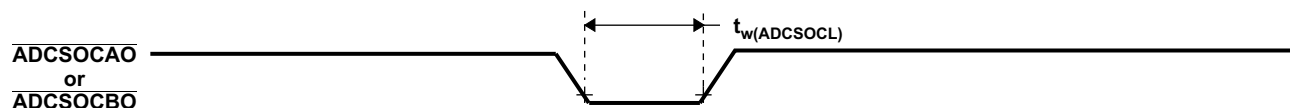


Figure 6-54. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

6.15.4 Enhanced Capture (eCAP)

The features of the eCAP module include:

- Speed measurements of rotating machinery (for example, toothed sprockets sensed by way of Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors

The eCAP module features described in this chapter include:

- 4-event time-stamp registers (each 32 bits)
- Edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt on either of the four events
- Single-shot capture of up to four event time-stamps
- Continuous mode capture of time stamps in a four-deep circular buffer
- Absolute time-stamp capture
- Difference (Delta) mode time-stamp capture
- When not used in capture mode, the eCAP module can be configured as a single-channel PWM output

The capture functionality of the Type 1 eCAP is enhanced from the Type 0 eCAP with the following added features:

- Event filter reset bit
 - Writing a 1 to ECCTL2[CTRFILTRESET] clears the event filter, the modulo counter, and any pending interrupts flags. Resetting the bit is useful for initialization and debug.
- Modulo counter status bits
 - The modulo counter (ECCTL2 [MODCNRSTS]) indicates which capture register is loaded next. In the Type 0 eCAP, to know the current state of the modulo counter was not possible
- DMA trigger source
 - eCAPxDMA was added as a DMA trigger. CEVT[1-4] can be configured as the source for eCAPxDMA.
- Input multiplexer
 - ECCTL0 [INPUTSEL] selects one of 128 input signals, which are detailed in the Configuring Device Pins for the eCAP section of the Enhanced Capture (eCAP) chapter in the .
- EALLOW protection
 - EALLOW protection was added to critical registers. To maintain software compatibility with Type-0, configure DEV_CFG_REGS.ECAPTYPE to make these registers unprotected.

The capture functionality of the Type 2 eCAP is enhanced from the Type 1 eCAP with the following added features:

- Added ECAPxSYNCINSEL register
 - ECAPxSYNCINSEL register is added for each eCAP to select an external SYNCIN. Every eCAP can have a separate SYNCIN signal.

6.15.4.1 eCAP Block Diagram

ADVANCE INFORMATION

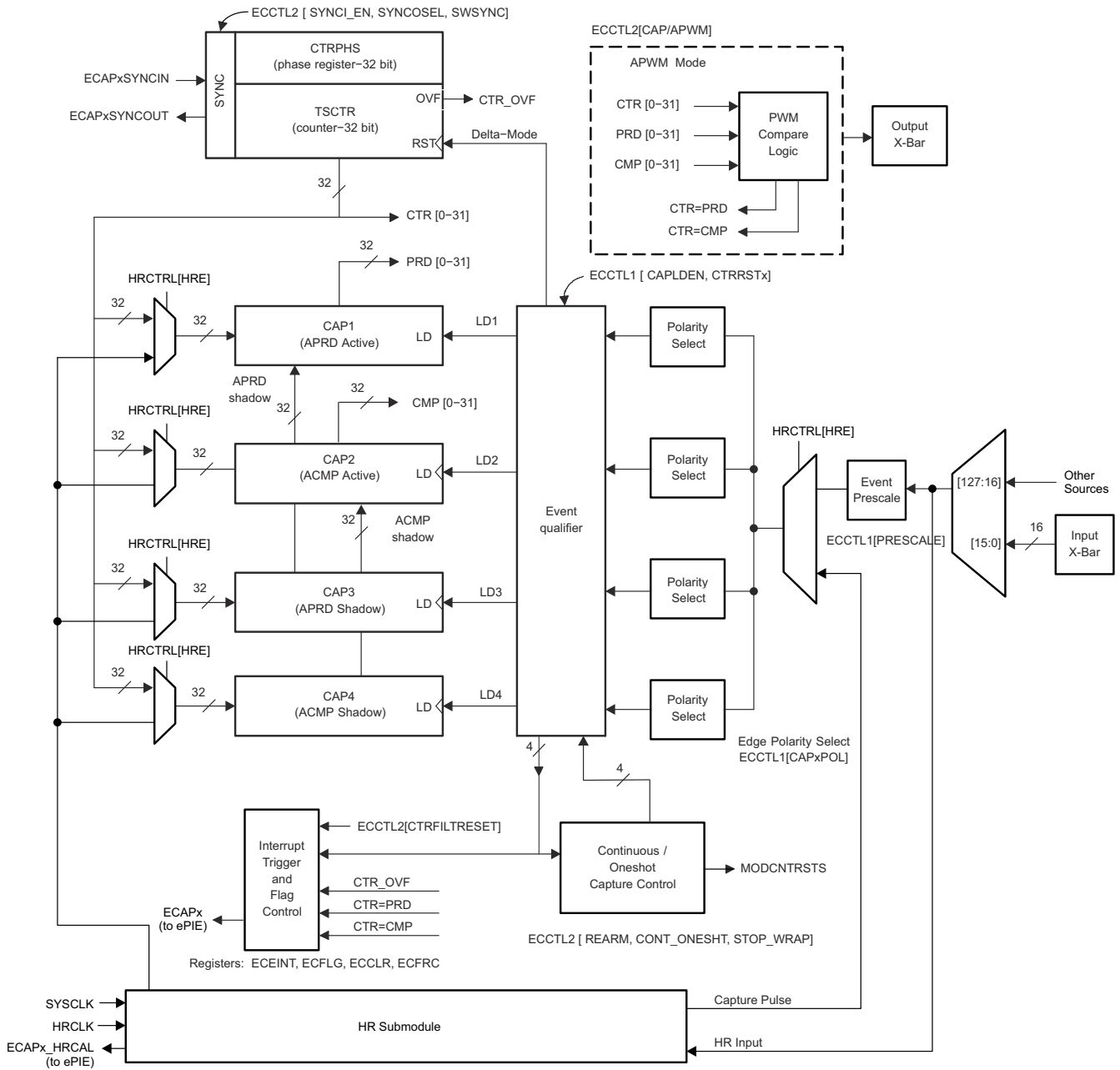


Figure 6-55. eCAP Block Diagram

6.15.4.2 eCAP Synchronization

The eCAP modules can be synchronized with each other by selecting a common SYNCIN source. SYNCIN source for eCAP can be either software sync-in or external sync-in. The external sync-in signal can come from EPWM, eCAP, or X-Bar. The SYNC signal is defined by the selection in the ECAPxSYNCINSEL[SEL] bit for ECAPx as shown in Figure 6-56.

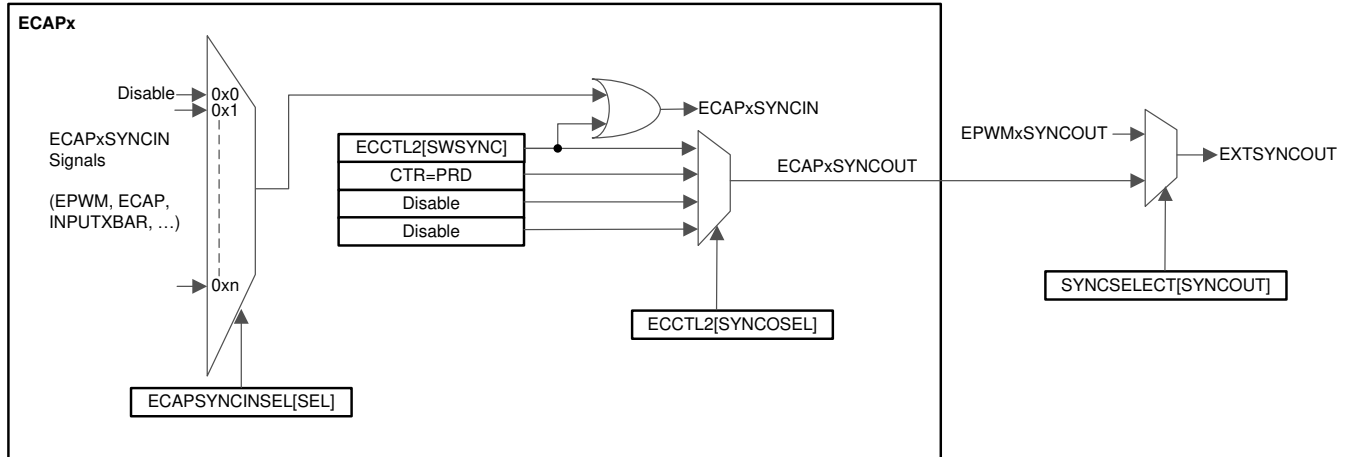


Figure 6-56. eCAP Synchronization Scheme

6.15.4.3 eCAP Electrical Data and Timing

6.15.4.3.1 eCAP Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|--------------|---------------------------|----------------------|--------------------------------|-----|-----|------|
| $t_{w(CAP)}$ | Capture input pulse width | Asynchronous | $2t_{c(SYSCLK)}$ | | | ns |
| | | Synchronous | $2t_{c(SYSCLK)}$ | | | |
| | | With input qualifier | $1t_{c(SYSCLK)} + t_{w_IQSW}$ | | | |

6.15.4.3.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|---------------|---------------------------------------|-----|-----|-----|------|
| $t_{w(APWM)}$ | Pulse duration, APWMx output high/low | 20 | | | ns |

6.15.5 Enhanced Quadrature Encoder Pulse (eQEP)

The eQEP module on this device is Type-2. The eQEP interfaces directly with linear or rotary incremental encoders to obtain position, direction, and speed information from rotating machines used in high-performance motion and position control systems.

The eQEP peripheral contains the following major functional units (see Figure 6-57):

- Programmable input qualification for each pin (part of the GPIO MUX)
- Quadrature decoder unit (QDU)
- Position counter and control unit for position measurement (PCCU)
- Quadrature edge-capture unit for low-speed measurement (QCAP)
- Unit time base for speed/frequency measurement (UTIME)
- Watchdog timer for detecting stalls (QWDOG)
- Quadrature Mode Adapter (QMA)

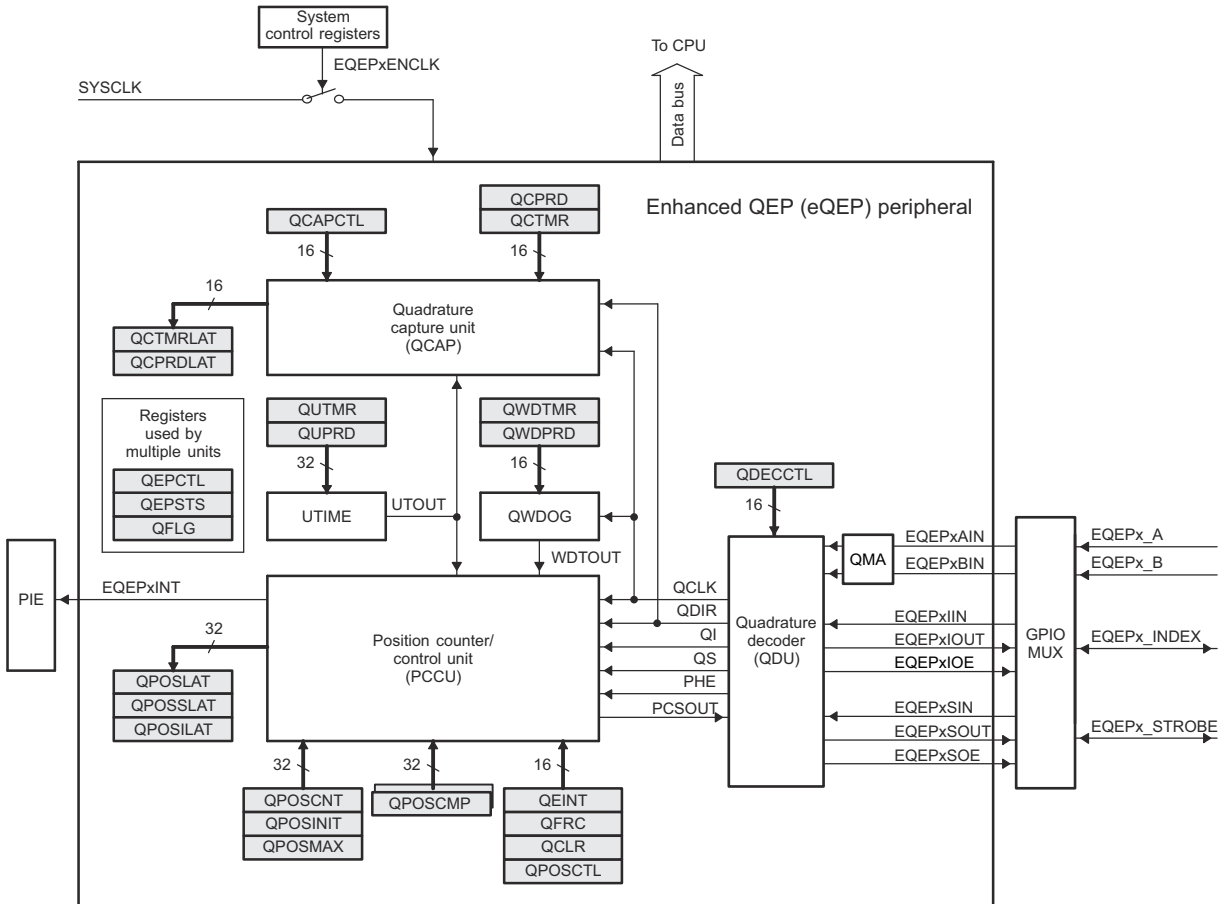


Figure 6-57. eQEP Block Diagram

ADVANCE INFORMATION

6.15.5.1 eQEP Electrical Data and Timing

For an explanation of the input qualifier parameters, see the *General-Purpose Input Timing Requirements* table.

6.15.5.1.1 eQEP Timing Requirements

| | | | MIN | MAX | UNIT |
|-----------------|---------------------------|----------------------------------|-----------------------------------|-----|--------|
| $t_{w(QEPP)}$ | QEP input period | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2[1t_{c(SYSCLK)} + t_{w(IQSW)}]$ | | |
| $t_{w(INDEXH)}$ | QEP Index Input High time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(INDEXL)}$ | QEP Index Input Low time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(STROBH)}$ | QEP Strobe High time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |
| $t_{w(STROBL)}$ | QEP Strobe Input Low time | Synchronous ⁽¹⁾ | $2t_{c(SYSCLK)}$ | | cycles |
| | | Synchronous with input qualifier | $2t_{c(SYSCLK)} + t_{w(IQSW)}$ | | |

(1) The GPIO GPxQSELn Asynchronous mode should not be used for eQEP module input pins.

6.15.5.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | MIN | MAX | UNIT |
|------------------------|--|-----|------------------|--------|
| $t_{d(CNTR)_{xin}}$ | Delay time, external clock to counter increment | | $5t_{c(SYSCLK)}$ | cycles |
| $t_{d(PCS-OUT)_{QEP}}$ | Delay time, QEP input edge to position compare sync output | | $7t_{c(SYSCLK)}$ | cycles |

6.16 Communications Peripherals

6.16.1 Modular Controller Area Network (MCAN)

The Controller Area Network (CAN) is a serial communications protocol that efficiently supports distributed real-time control with a high level of reliability. CAN has high immunity to electrical interference and the ability to detect various type of errors. In CAN, many short messages are broadcast to the entire network, which provides data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with flexible data-rate) protocols. The CAN FD feature allows higher throughput and increased payload per data frame. Classic CAN and CAN FD devices may coexist on the same network without any conflict provided that partial network transceivers, which can detect and ignore CAN FD without generating bus errors, are used by the classic CAN devices. The MCAN module is compliant to ISO 11898-1:2015.

Note

The availability of the CAN FD feature is dependent on the device's part number. Refer to the device data sheet for more information.

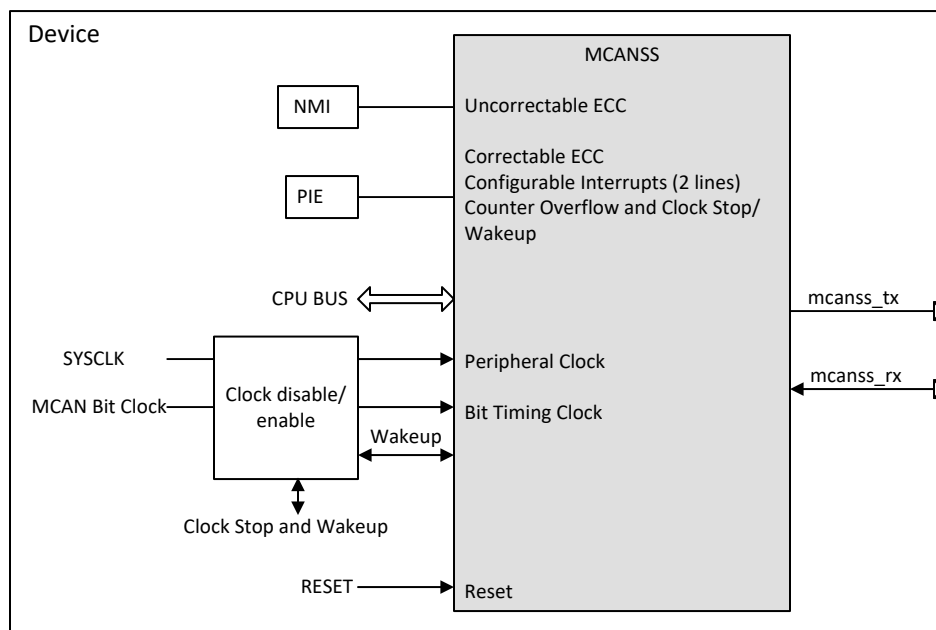


Figure 6-58. MCAN Module Overview

The MCAN module implements the following features:

- Conforms with CAN Protocol 2.0 A, B and ISO 11898-1:2015
- Full CAN FD support (up to 64 data bytes)
- AUTOSAR and SAE J1939 support
- Flexible Message RAM allocation (maximum configuration below is for a device with 4352 32-bit word message RAM)
 - Up to 32 dedicated transmit buffers
 - Configurable transmit FIFO, up to 32 elements
 - Configurable transmit queue, up to 32 elements
 - Configurable transmit Event FIFO, up to 32 elements
 - Up to 64 dedicated receive buffers
 - Two configurable receive FIFOs, up to 64 elements each
 - Up to 128 filter elements
- Loop-back mode for self-test

- Maskable interrupt (two configurable interrupt lines, correctable ECC, counter overflow and clock stop/wakeup)
- Non-maskable interrupt (uncorrectable ECC)
- Two clock domains (CAN clock/host clock)
- ECC check for Message RAM
- Clock stop and wake-up support
- Timestamp counter

Non-supported features:

- Host bus firewall
- Clock calibration
- Debug over CAN

6.16.2 Inter-Integrated Circuit (I2C)

The I2C module has the following features:

- Compliance with the NXP Semiconductors I²C-bus specification (version 2.1):
 - Support for 8-bit format transfers
 - 7-bit and 10-bit addressing modes
 - General call
 - START byte mode
 - Support for multiple controller-transmitters and target-receivers
 - Support for multiple target-transmitters and controller-receivers
 - Combined controller transmit/receive and receive/transmit mode
 - Data transfer rate from 10Kbps up to 400Kbps (Fast-mode)
- Supports voltage thresholds compatible to:
 - SMBus 3.0 and below
 - PMBus 1.3 and below
- One 16-byte receive FIFO and one 16-byte transmit FIFO
- Supports two ePIE interrupts
 - I2Cx interrupt – Any of the below conditions can be configured to generate an I2Cx interrupt:
 - Transmit Ready
 - Receive Ready
 - Register-Access Ready
 - No-Acknowledgment
 - Arbitration-Lost
 - Stop Condition Detected
 - Addressed-as-Target
 - I2Cx_FIFO interrupts:
 - Transmit FIFO interrupt
 - Receive FIFO interrupt
- Module enable and disable capability
- Free data format mode

Figure 6-59 shows how the I2C peripheral module interfaces within the device.

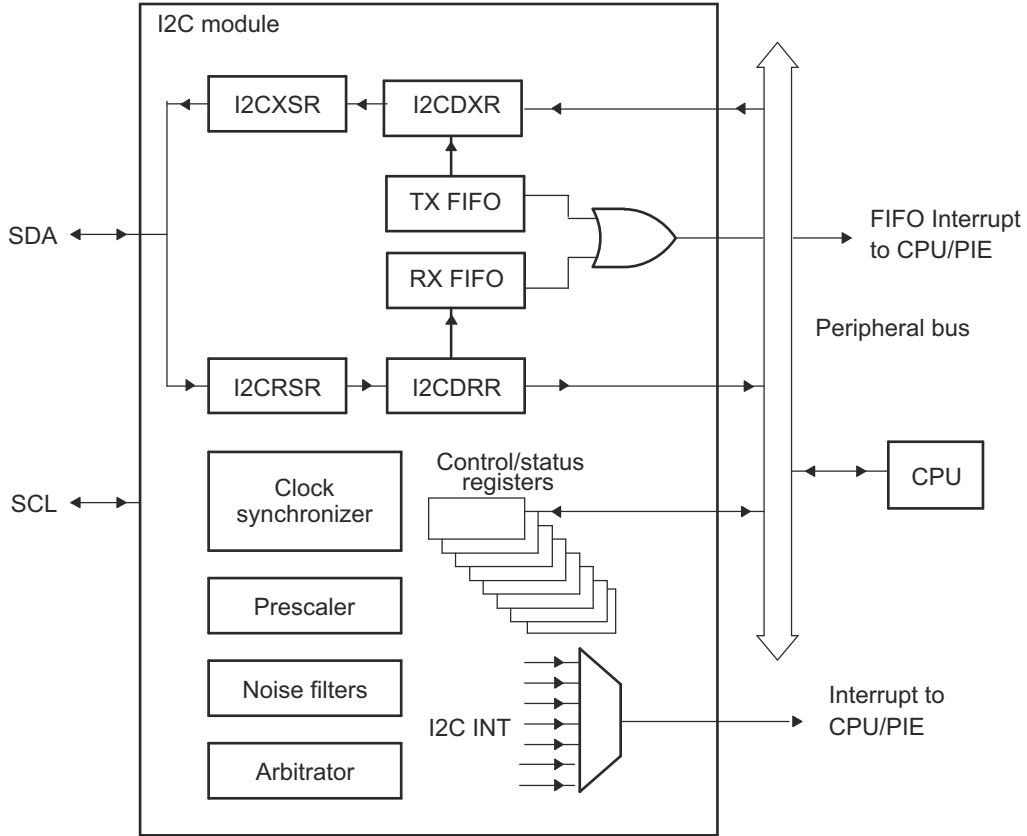


Figure 6-59. I2C Peripheral Module Interfaces

ADVANCE INFORMATION

6.16.2.1 I2C Electrical Data and Timing

Note

To meet all of the I2C protocol timing specifications, the I2C module clock must be configured in the range from 7 MHz to 12 MHz.

A pullup resistor must be chosen to meet the I2C standard timings. In most circumstances, 2.2 kΩ of total bus resistance to VDDIO is sufficient. For evaluating pullup resistor values for a particular design, see the [I2C Bus Pullup Resistor Calculation](#) Application Report.

6.16.2.1.1 I2C Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|----------------------|-------------------------------|--|------|------|------|
| Standard mode | | | | | |
| T0 | f_{mod} | I2C module frequency | 7 | 12 | MHz |
| T1 | $t_{\text{h(SDA-SCL)START}}$ | Hold time, START condition, SCL fall delay after SDA fall | 4.0 | | μs |
| T2 | $t_{\text{su(SCL-SDA)START}}$ | Setup time, Repeated START, SCL rise before SDA fall delay | 4.0 | | μs |
| T3 | $t_{\text{h(SCL-DAT)}}$ | Hold time, data after SCL fall | 0 | | μs |
| T4 | $t_{\text{su(DAT-SCL)}}$ | Setup time, data before SCL rise | 250 | | ns |
| T5 | $t_{\text{r(SDA)}}$ | Rise time, SDA | | 1000 | ns |
| T6 | $t_{\text{r(SCL)}}$ | Rise time, SCL | | 1000 | ns |
| T7 | $t_{\text{f(SDA)}}$ | Fall time, SDA | | 300 | ns |
| T8 | $t_{\text{f(SCL)}}$ | Fall time, SCL | | 300 | ns |
| T9 | $t_{\text{su(SCL-SDA)STOP}}$ | Setup time, STOP condition, SCL rise before SDA rise delay | 4.0 | | μs |
| T10 | $t_{\text{w(SP)}}$ | Pulse duration of spikes that will be suppressed by filter | 0 | 50 | ns |
| T11 | C_{b} | capacitance load on each bus line | | 400 | pF |
| Fast mode | | | | | |
| T0 | f_{mod} | I2C module frequency | 7 | 12 | MHz |
| T1 | $t_{\text{h(SDA-SCL)START}}$ | Hold time, START condition, SCL fall delay after SDA fall | 0.6 | | μs |
| T2 | $t_{\text{su(SCL-SDA)START}}$ | Setup time, Repeated START, SCL rise before SDA fall delay | 0.6 | | μs |
| T3 | $t_{\text{h(SCL-DAT)}}$ | Hold time, data after SCL fall | 0 | | μs |
| T4 | $t_{\text{su(DAT-SCL)}}$ | Setup time, data before SCL rise | 100 | | ns |
| T5 | $t_{\text{r(SDA)}}$ | Rise time, SDA | 20 | 300 | ns |
| T6 | $t_{\text{r(SCL)}}$ | Rise time, SCL | 20 | 300 | ns |
| T7 | $t_{\text{f(SDA)}}$ | Fall time, SDA | 11.4 | 300 | ns |
| T8 | $t_{\text{f(SCL)}}$ | Fall time, SCL | 11.4 | 300 | ns |
| T9 | $t_{\text{su(SCL-SDA)STOP}}$ | Setup time, STOP condition, SCL rise before SDA rise delay | 0.6 | | μs |
| T10 | $t_{\text{w(SP)}}$ | Pulse duration of spikes that will be suppressed by filter | 0 | 50 | ns |
| T11 | C_{b} | capacitance load on each bus line | | 400 | pF |

6.16.2.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|----------------------|------------------|---|-----------------------------------|------|------------|
| Standard mode | | | | | |
| S1 | f_{SCL} | SCL clock frequency | 0 | 100 | kHz |
| S2 | T_{SCL} | SCL clock period | 10 | | μs |
| S3 | $t_{w(SCLL)}$ | Pulse duration, SCL clock low | 4.7 | | μs |
| S4 | $t_{w(SCLH)}$ | Pulse duration, SCL clock high | 4.0 | | μs |
| S5 | t_{BUF} | Bus free time between STOP and START conditions | 4.7 | | μs |
| S6 | $t_{v(SCL-DAT)}$ | Valid time, data after SCL fall | | 3.45 | μs |
| S7 | $t_{v(SCL-ACK)}$ | Valid time, Acknowledge after SCL fall | | 3.45 | μs |
| S8 | I_I | Input current on pins | $0.1 V_{bus} < V_i < 0.9 V_{bus}$ | -10 | 10 μA |
| Fast mode | | | | | |
| S1 | f_{SCL} | SCL clock frequency | 0 | 400 | kHz |
| S2 | T_{SCL} | SCL clock period | 2.5 | | μs |
| S3 | $t_{w(SCLL)}$ | Pulse duration, SCL clock low | 1.3 | | μs |
| S4 | $t_{w(SCLH)}$ | Pulse duration, SCL clock high | 0.6 | | μs |
| S5 | t_{BUF} | Bus free time between STOP and START conditions | 1.3 | | μs |
| S6 | $t_{v(SCL-DAT)}$ | Valid time, data after SCL fall | | 0.9 | μs |
| S7 | $t_{v(SCL-ACK)}$ | Valid time, Acknowledge after SCL fall | | 0.9 | μs |
| S8 | I_I | Input current on pins | $0.1 V_{bus} < V_i < 0.9 V_{bus}$ | -10 | 10 μA |

6.16.2.1.3 I2C Timing Diagram

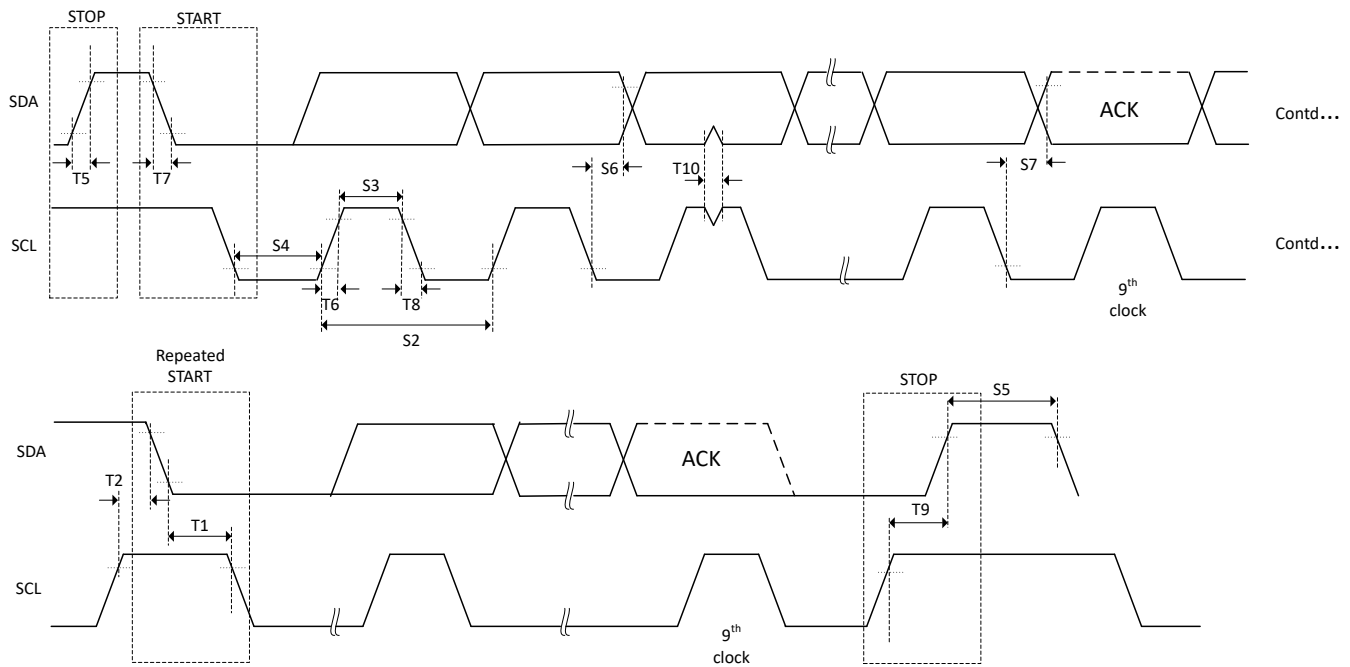


Figure 6-60. I2C Timing Diagram

6.16.3 Power Management Bus (PMBus) Interface

The PMBus module has the following features:

- Compliance with the SMI Forum PMBus Specification (Part I v1.0 and Part II v1.1)
- Supports voltage thresholds compatible to:
 - PMBus 1.3 and below
 - SMBus 3.0 and below
- Support for controller and target
- Support for I2C mode
- Support for three speeds:
 - Standard Mode: Up to 100 kHz
 - Fast Mode: 400 kHz
 - Fast Plus Mode: 1MHz
- Packet error checking
- CONTROL and ALERT signals
- Clock high and low time-outs
- Four-byte transmit and receive buffers
- One maskable interrupt, which can be generated by several conditions:
 - Receive data ready
 - Transmit buffer empty
 - Target address received
 - End of message
 - ALERT input asserted
 - Clock low time-out
 - Clock high time-out
 - Bus free

Note

Please see the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#) to determine which pins support Fast Plus Mode as well as full SMBUS3.0 and PMBUS1.3 specifications

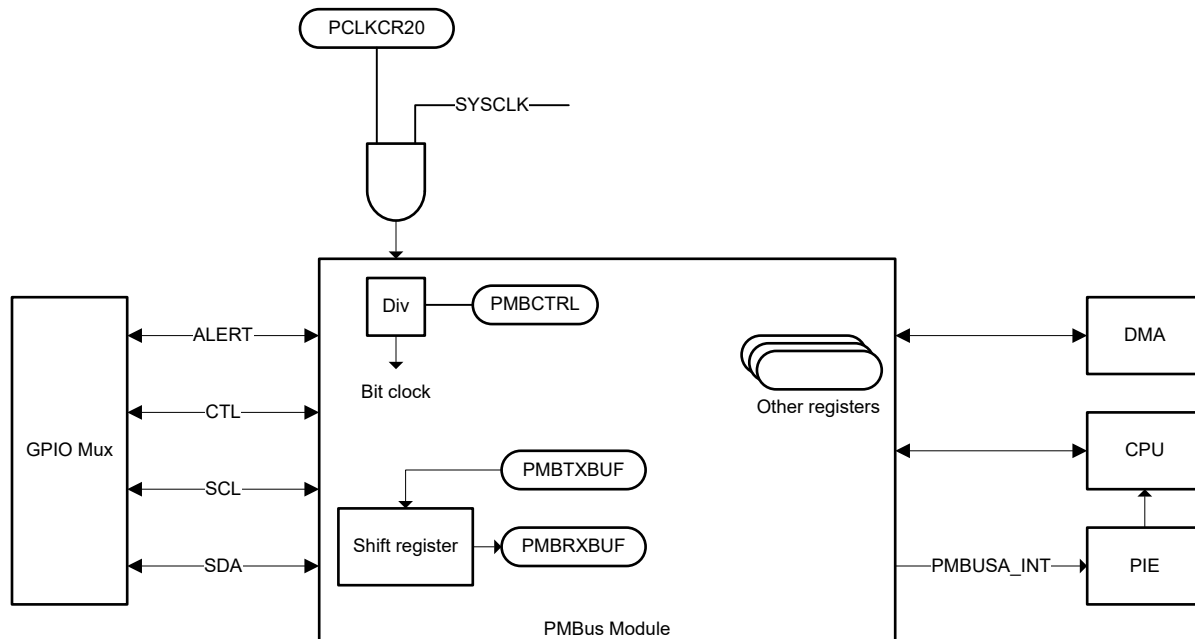


Figure 6-61. PMBus Block Diagram

6.16.3.1 PMBus Electrical Data and Timing

6.16.3.1.1 PMBus Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|--|-----|-------|-----|------|
| V _{IL} | Valid low-level input voltage | | | | 0.8 | V |
| V _{IH} | Valid high-level input voltage | | 2.1 | VDDIO | | V |
| V _{OL} | Low-level output voltage | At I _{pullup} = 4 mA | | | 0.4 | V |
| I _{OL} | Low-level output current | V _{OL} ≤ 0.4 V | 4 | | | mA |
| t _{SP} | Pulse width of spikes that must be suppressed by the input filter | | 0 | | 50 | ns |
| I _i | Input leakage current on each pin | 0.1 V _{bus} < V _i < 0.9 V _{bus} | -10 | | 10 | μA |
| C _i | Capacitance on each pin | | | | 10 | pF |

6.16.3.1.2 PMBus Fast Plus Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|--------------------------|------|-----|---------------------|------|
| F _{mod} | PMBus Module Clock Frequency ⁽²⁾ | | 20 | | 25 | MHz |
| f _{SCL} | SCL clock frequency | 3.3V Nominal Bus Voltage | 10 | | 1000 ⁽³⁾ | kHz |
| | | 5.0V Nominal Bus Voltage | 10 | | 1000 ⁽⁴⁾ | |
| t _{BUF} | Bus free time between STOP and START conditions | | 0.5 | | | μs |
| t _{HD;STA} | START condition hold time -- SDA fall to SCL fall delay | | 0.26 | | | μs |
| t _{SU;STA} | Repeated START setup time -- SCL rise to SDA fall delay | | 0.26 | | | μs |
| t _{SU;STO} | STOP condition setup time -- SCL rise to SDA rise delay | | 0.26 | | | μs |
| t _{HD;DAT} | Data hold time after SCL fall | | 300 | | | ns |
| | Data hold time after SCL fall PMBCTRL_ZH_EN = 1 ⁽¹⁾ | | 0 | | | ns |
| t _{SU;DAT} | Data setup time before SCL rise | | 50 | | | ns |
| t _{Timeout} | Clock low time-out | | 25 | | 35 | ms |
| t _{LOW} | Low period of the SCL clock | | 0.5 | | | μs |
| t _{HIGH} | High period of the SCL clock | | 0.26 | | 50 | μs |
| t _{LOW;SEXT} | Cumulative clock low extend time (target device) | From START to STOP | | | 25 | ms |
| t _{LOW;MEXT} | Cumulative clock low extend time (controller device) | Within each byte | | | 10 | ms |
| t _r | Rise time of SDA and SCL | 5% to 95% | 20 | | 120 | ns |
| t _f | Fall time of SDA and SCL | 95% to 5% | 20 | | 120 | ns |

- (1) This bit must be set to enable 0ns hold time/SMBUS3.0 Compliance
- (2) If the max clock is used all below timings will be met with the default register configurations for the PMBUS
- (3) Due to max IO drive strength of 12mA, 1MHz SCL clock is only valid for bus capacitances up to 520pF
- (4) Due to max IO drive strength of 12mA, 1MHz SCL clock is only valid for bus capacitances up to 330pF

6.16.3.1.3 PMBus Fast Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------|--|--------------------|---------------------|-----|-----|---------|
| F_{mod} | PMBus Module Clock Frequency ⁽²⁾ | | $f_{(SYSCLK)} / 32$ | | 10 | MHz |
| f_{SCL} | SCL clock frequency | | 10 | | 400 | kHz |
| t_{BUF} | Bus free time between STOP and START conditions | | 1.3 | | | μ s |
| $t_{HD;STA}$ | START condition hold time -- SDA fall to SCL fall delay | | 0.6 | | | μ s |
| $t_{SU;STA}$ | Repeated START setup time -- SCL rise to SDA fall delay | | 0.6 | | | μ s |
| $t_{SU;STO}$ | STOP condition setup time -- SCL rise to SDA rise delay | | 0.6 | | | μ s |
| $t_{HD;DAT}$ | Data hold time after SCL fall | | 300 | | | ns |
| | Data hold time after SCL fall PMBCTRL_INC_1[ZH+EN] = 1 ⁽¹⁾ | | 0 | | | ns |
| $t_{SU;DAT}$ | Data setup time before SCL rise | | 100 | | | ns |
| $t_{Timeout}$ | Clock low time-out | | 25 | | 35 | ms |
| t_{LOW} | Low period of the SCL clock | | 1.3 | | | μ s |
| t_{HIGH} | High period of the SCL clock | | 0.6 | | 50 | μ s |
| $t_{LOW;SEXT}$ | Cumulative clock low extend time (target device) | From START to STOP | | | 25 | ms |
| $t_{LOW;MEXT}$ | Cumulative clock low extend time (controller device) | Within each byte | | | 10 | ms |
| t_r | Rise time of SDA and SCL | 5% to 95% | 20 | | 300 | ns |
| t_f | Fall time of SDA and SCL | 95% to 5% | 20 | | 300 | ns |

(1) This bit must be set to enable 0ns hold time/SMBUS3.0 Compliance

(2) If the max clock is used all below timings will be met with the default register configurations for the PMBUS

6.16.3.1.4 PMBus Standard Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|--|--------------------|-------------------------------|-----|------|------|
| F _{mod} | PMBus Module Clock Frequency ⁽²⁾ | | f _(SYSCLK) / 32 | | 10 | MHz |
| f _{SCL} | SCL clock frequency | | 10 | | 100 | kHz |
| t _{BUF} | Bus free time between STOP and START conditions | | 4.7 | | | μs |
| t _{HD;STA} | START condition hold time -- SDA fall to SCL fall delay | | 4 | | | μs |
| t _{SU;STA} | Repeated START setup time -- SCL rise to SDA fall delay | | 4.7 | | | μs |
| t _{SU;STO} | STOP condition setup time -- SCL rise to SDA rise delay | | 4 | | | μs |
| t _{HD;DAT} | Data hold time after SCL fall | | 300 | | | ns |
| | Data hold time after SCL fall PMBCTRL_INC_1[ZH+EN] = 1 ⁽¹⁾ | | 0 | | | ns |
| t _{SU;DAT} | Data setup time before SCL rise | | 250 | | | ns |
| t _{Timeout} | Clock low time-out | | 25 | | 35 | ms |
| t _{LOW} | Low period of the SCL clock | | 4.7 | | | μs |
| t _{HIGH} | High period of the SCL clock | | 4 | | 50 | μs |
| t _{LOW;SEXT} | Cumulative clock low extend time (target device) | From START to STOP | | | 25 | ms |
| t _{LOW;MEXT} | Cumulative clock low extend time (controller device) | Within each byte | | | 10 | ms |
| t _r | Rise time of SDA and SCL | | | | 1000 | ns |
| t _f | Fall time of SDA and SCL | | | | 300 | ns |

(1) This bit must be set to enable 0ns hold time/SMBUS3.0 Compliance

(2) If the max clock is used all below timings will be met with the default register configurations for the PMBUS

6.16.4 Serial Communications Interface (SCI)

The SCI is a 2-wire asynchronous serial port, commonly known as a UART. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format

The SCI receiver and transmitter each have a 16-level-deep FIFO for reducing servicing overhead, and each has its own separate enable and interrupt bits. Both can be operated independently for half-duplex communication, or simultaneously for full-duplex communication. To specify data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to different speeds through a 16-bit baud-select register.

Features of the SCI module include:

- Two external pins:
 - SCITXD: SCI transmit-output pin
 - SCIRXD: SCI receive-input pin
 - Baud rate programmable to 64K different rates
- Data-word format
 - 1 start bit
 - Data-word length programmable from 1 to 8 bits
 - Optional even/odd/no parity bit
 - 1 or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
 - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
 - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ format
- Auto baud-detect hardware logic
- 16-level transmit and receive FIFO

Note

All registers in this module are 8-bit registers. When a register is accessed, the register data is in the lower byte (bits 7–0), and the upper byte (bits 15–8) is read as zeros. Writing to the upper byte has no effect.

Figure 6-62 shows the SCI block diagram.

6.16.5 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a high-speed synchronous serial input and output (I/O) port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmed bit-transfer rate. The SPI is normally used for communications between the MCU controller and external peripherals or another controller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and analog-to-digital converters (ADCs). Multidevice communications are supported by the controller or peripheral operation of the SPI. The port supports a 16-level, receive and transmit FIFO for reducing CPU servicing overhead.

The SPI module features include:

- SPIPOCI: SPI peripheral-output/controller-input pin
- SPIPICO: SPI peripheral-input/controller-output pin
- SPIPTE: SPI peripheral transmit-enable pin
- SPICLK: SPI serial-clock pin
- Two operational modes: Controller and Peripheral
- Baud rate: 125 different programmable rates. The maximum baud rate that can be employed is limited by the maximum speed of the I/O buffers used on the SPI pins.
- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
 - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
 - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
 - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithm
- 16-level transmit/receive FIFO
- DMA support
- High-speed mode
- Delayed transmit control
- 3-wire SPI mode
- SPIPTE inversion for digital audio interface receive mode on devices with two SPI modules

Figure 6-63 shows the SPI CPU interfaces.

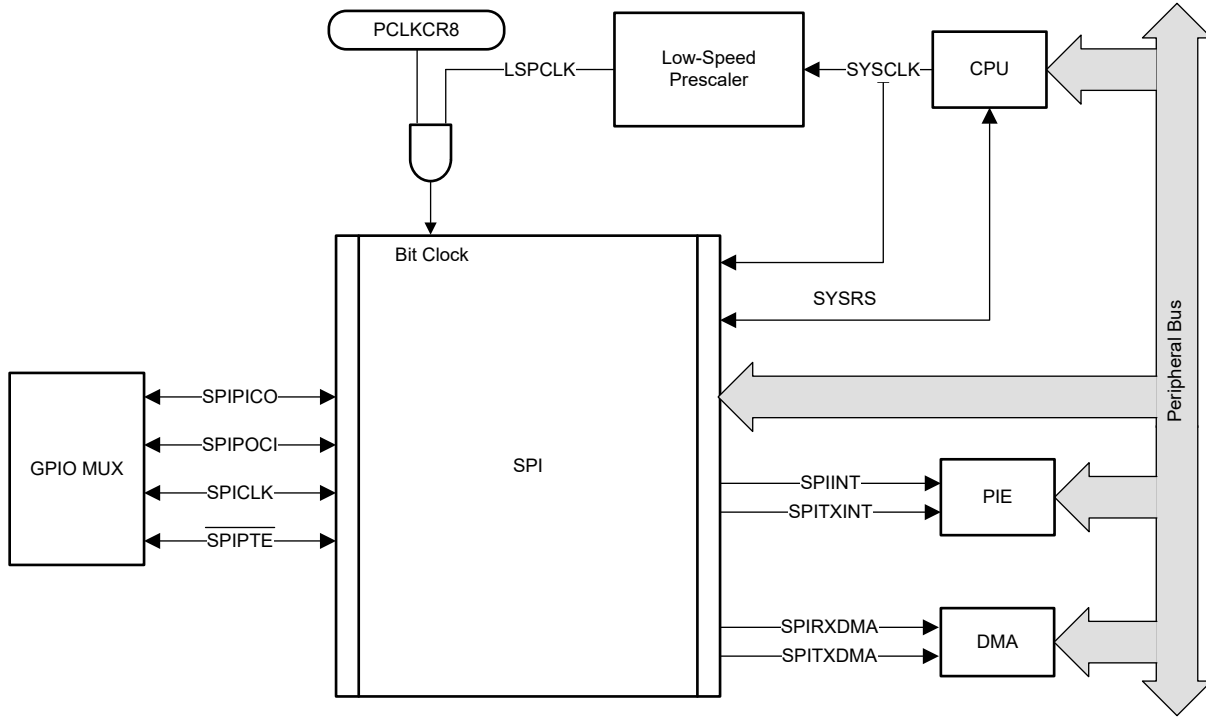


Figure 6-63. SPI CPU Interface

ADVANCE INFORMATION

6.16.5.1 SPI Controller Mode Timings

The following section contains the SPI Controller Mode Timings.

Note

All timing parameters for SPI High-Speed Mode assume a load capacitance of 5 pF on SPICLK, SPIPICO, and SPIPOCI.

6.16.5.1.1 SPI Controller Mode Timing Requirements

| NO. | PARAMETER ⁽²⁾ | | (BRR + 1) ⁽¹⁾ | MIN | MAX | UNIT |
|------------------------|--------------------------|---|--------------------------|------|-----|------|
| High-Speed Mode | | | | | | |
| 8 | $t_{su(POCI)M}$ | Setup time, SPIPOCI valid before SPICLK | Even, Odd | 0.7 | | ns |
| 8 | $t_{su(POCI)M}$ | Setup time, SPIPOCI valid before SPICLK(when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even, Odd | 1.5 | | ns |
| 8 | $t_{su(POCI)M}$ | Setup time, SPIPOCI valid before SPICLK(when used on pin muxed with USB - GPIO23, or 41) | Even, Odd | 1.5 | | ns |
| 9 | $t_{h(POCI)M}$ | Hold time, SPIPOCI valid after SPICLK | Even, Odd | 6.5 | | ns |
| Normal Mode | | | | | | |
| 8 | $t_{su(POCI)M}$ | Setup time, SPIPOCI valid before SPICLK | Even, Odd | 15 | | ns |
| 8 | $t_{su(POCI)M}$ | Setup time, SPIPOCI valid before SPICLK(when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even, Odd | 16.5 | | ns |
| 9 | $t_{h(POCI)M}$ | Hold time, SPIPOCI valid after SPICLK | Even, Odd | 0 | | ns |

- (1) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.
 (2) GPIOs 2, 3, 9, 23, 32, or 41 do not support full High-Speed Mode(37.5MHz) SPI operation

6.16.5.1.2 SPI Controller Mode Switching Characteristics - Clock Phase 0

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER (1) (2) (4) | (BRR + 1) ⁽³⁾ | MIN | MAX | UNIT | |
|------------------------|-----------------------|---|-----------|---|------|----|
| General | | | | | | |
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ $128t_{c(LSPCLK)}$ | ns | |
| | | | Odd | $5t_{c(LSPCLK)}$ $127t_{c(LSPCLK)}$ | | |
| 2 | $t_{w(SPC1)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ $0.5t_{c(SPC)M} + 1$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ $0.5t_{c(SPC)M} + 1$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | | |
| 23 | $t_{d(SPC)M}$ | Delay time, $\overline{SPIPT\bar{E}}$ active to SPICLK | Even | $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$ $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$ | ns | |
| | | | Odd | $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$ $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$ | | |
| 23 | $t_{d(SPC)M}$ | Delay time, $\overline{SPIPT\bar{E}}$ active to SPICLK (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even | $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 4$ $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$ | ns | |
| | | | Odd | $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 4$ $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 3$ | | |
| 23 | $t_{d(SPC)M}$ | Delay time, $\overline{SPIPT\bar{E}}$ active to SPICLK (when used on pin muxed with USB - GPIO23 or GPIO41) | Even | $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$ $1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} + 5.5$ | ns | |
| | | | Odd | $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} - 3$ $1.5t_{c(SPC)M} - 4t_{c(SYSCLK)} + 5.5$ | | |
| 24 | $t_{v(STE)M}$ | Valid time, SPICLK to $\overline{SPIPT\bar{E}}$ inactive | Even | $0.5t_{c(SPC)M} - 3$ $0.5t_{c(SPC)M} + 3$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | | |
| 24 | $t_{v(STE)M}$ | Valid time, SPICLK to $\overline{SPIPT\bar{E}}$ inactive (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even | $0.5t_{c(SPC)M} - 4$ $0.5t_{c(SPC)M} + 3$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 4$ $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 3$ | | |
| 24 | $t_{v(STE)M}$ | Valid time, SPICLK to $\overline{SPIPT\bar{E}}$ inactive (when used on pin muxed with USB - GPIO23 or GPIO41) | Even | $0.5t_{c(SPC)M} - 3$ $0.5t_{c(SPC)M} + 5.5$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 5.5$ | | |
| High-Speed Mode | | | | | | |
| 4 | $t_{d(PICO)M}$ | Delay time, SPICLK to SPIPICO valid | Even, Odd | | 1 | ns |
| 4 | $t_{d(PICO)M}$ | Delay time, SPICLK to SPIPICO valid (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even, Odd | | 2 | ns |
| 5 | $t_{v(PICO)M}$ | Valid time, SPIPICO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| 5 | $t_{v(PICO)M}$ | Valid time, SPIPICO valid after SPICLK (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even | $0.5t_{c(SPC)M} - 4.5$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 4.5$ | | |
| Normal Mode | | | | | | |
| 4 | $t_{d(PICO)M}$ | Delay time, SPICLK to SPIPICO valid | Even, Odd | | 2 | ns |
| 5 | $t_{v(PICO)M}$ | Valid time, SPIPICO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |

6.16.5.1.2 SPI Controller Mode Switching Characteristics - Clock Phase 0 (continued)

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ ⁽²⁾ ⁽⁴⁾ | | (BRR + 1) ⁽³⁾ | MIN | MAX | UNIT |
|-----|--|---|--------------------------|---|-----|------|
| 5 | $t_{V(PICO)M}$ | Valid time, SPIPICO valid after SPICLK (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even | 0.5 $t_{c(SPC)M}$ – 4.5 | | ns |
| | | | Odd | 0.5 $t_{c(SPC)M}$ – 0.5 $t_{c(LSPCLK)}$ – 4.5 | | |

(1) 10-pF load on pin for High-Speed Mode.

(2) 20-pF load on pin for Normal Mode.

(3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.

(4) GPIOs 2, 3, 9, 23, 32, or 41 do not support full High-Speed Mode(37.5MHz) SPI operation

6.16.5.1.3 SPI Controller Mode Switching Characteristics - Clock Phase 1

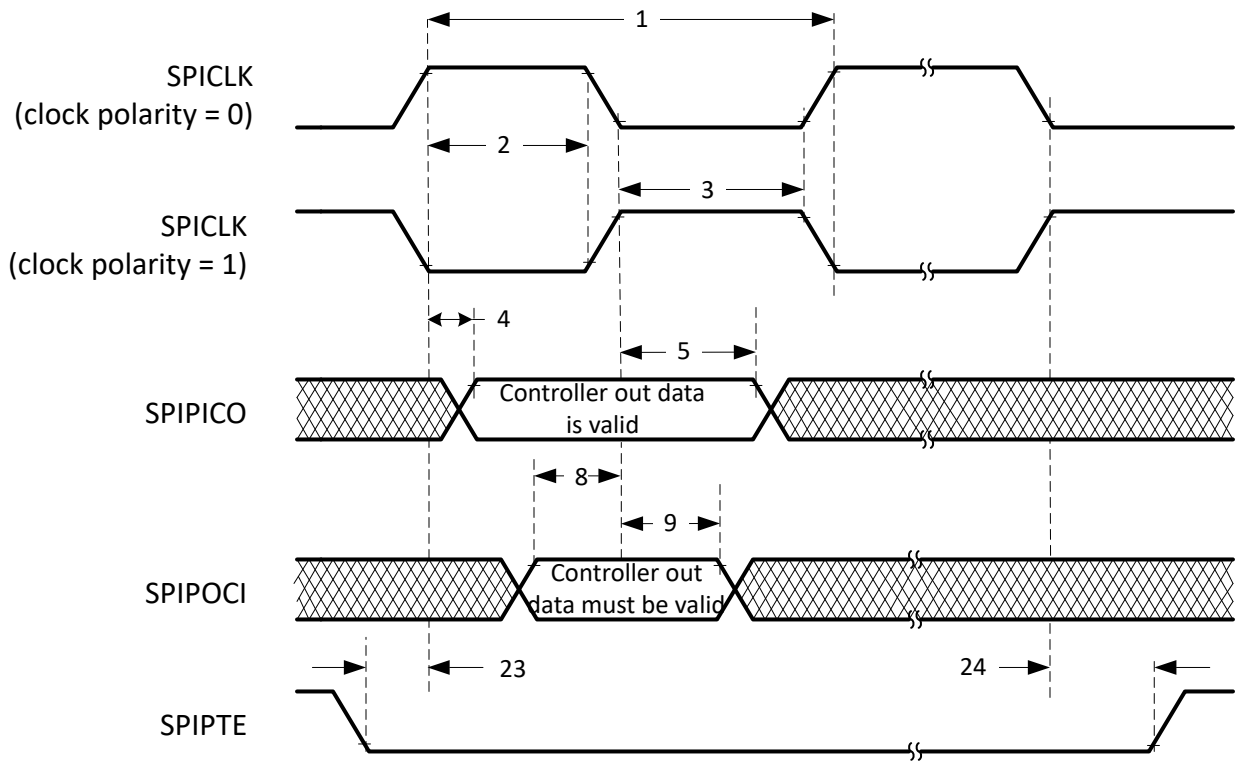
over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ^{(1) (2) (4)} | (BRR + 1) ⁽³⁾ | MIN | MAX | UNIT | |
|------------------------|----------------------------------|--|-----------|---|---|----|
| General | | | | | | |
| 1 | $t_{c(SPC)M}$ | Cycle time, SPICLK | Even | $4t_{c(LSPCLK)}$ | $128t_{c(LSPCLK)}$ | ns |
| | | | Odd | $5t_{c(LSPCLK)}$ | $127t_{c(LSPCLK)}$ | |
| 2 | $t_{w(SPCH)M}$ | Pulse duration, SPICLK, first pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 1$ | |
| 3 | $t_{w(SPC2)M}$ | Pulse duration, SPICLK, second pulse | Even | $0.5t_{c(SPC)M} - 1$ | $0.5t_{c(SPC)M} + 1$ | ns |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 1$ | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 1$ | |
| 23 | $t_{d(SPC)M}$ | Delay time, \overline{SPIPTE} valid to SPICLK | Even, Odd | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$ | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$ | ns |
| 23 | $t_{d(SPC)M}$ | Delay time, \overline{SPIPTE} valid to SPICLK (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even, Odd | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 4$ | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 3$ | ns |
| 23 | $t_{d(SPC)M}$ | Delay time, \overline{SPIPTE} valid to SPICLK (when used on pin muxed with USB - GPIO23 or GPIO41) | Even, Odd | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 3$ | $2t_{c(SPC)M} - 3t_{c(SYSCLK)} + 5.5$ | ns |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to \overline{SPIPTE} invalid | Even | -3 | 3 | ns |
| | | | Odd | -3 | 3 | |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to \overline{SPIPTE} invalid (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even | -4 | 3 | ns |
| | | | Odd | -4 | 3 | |
| 24 | $t_{d(STE)M}$ | Delay time, SPICLK to \overline{SPIPTE} invalid (when used on pin muxed with USB - GPIO23 or GPIO41) | Even | -3 | 5.5 | ns |
| | | | Odd | -3 | 5.5 | |
| High-Speed Mode | | | | | | |
| 4 | $t_{d(PICO)M}$ | Delay time, SPIPICO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 2$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$ | | |
| 4 | $t_{d(PICO)M}$ | Delay time, SPIPICO valid to SPICLK (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even | $0.5t_{c(SPC)M} - 3$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 3$ | | |
| 5 | $t_{v(PICO)M}$ | Valid time, SPIPICO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| 5 | $t_{v(PICO)M}$ | Valid time, SPIPICO valid after SPICLK (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even | $0.5t_{c(SPC)M} - 4.5$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 4.5$ | | |
| Normal Mode | | | | | | |
| 4 | $t_{d(PICO)M}$ | Delay time, SPIPICO valid to SPICLK | Even | $0.5t_{c(SPC)M} - 2$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 2$ | | |
| 5 | $t_{v(PICO)M}$ | Valid time, SPIPICO valid after SPICLK | Even | $0.5t_{c(SPC)M} - 3$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 3$ | | |
| 5 | $t_{v(PICO)M}$ | Valid time, SPIPICO valid after SPICLK (when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | Even | $0.5t_{c(SPC)M} - 4.5$ | ns | |
| | | | Odd | $0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 4.5$ | | |

- (1) 10-pF load on pin for High-Speed Mode.
- (2) 20-pF load on pin for Normal Mode.
- (3) The (BRR + 1) condition is Even when (SPIBRR + 1) is even or SPIBRR is 0 or 2. It is Odd when (SPIBRR + 1) is odd and SPIBRR is greater than 3.
- (4) GPIOs 2, 3, 9, 23, 32, or 41 do not support full High-Speed Mode(37.5MHz) SPI operation

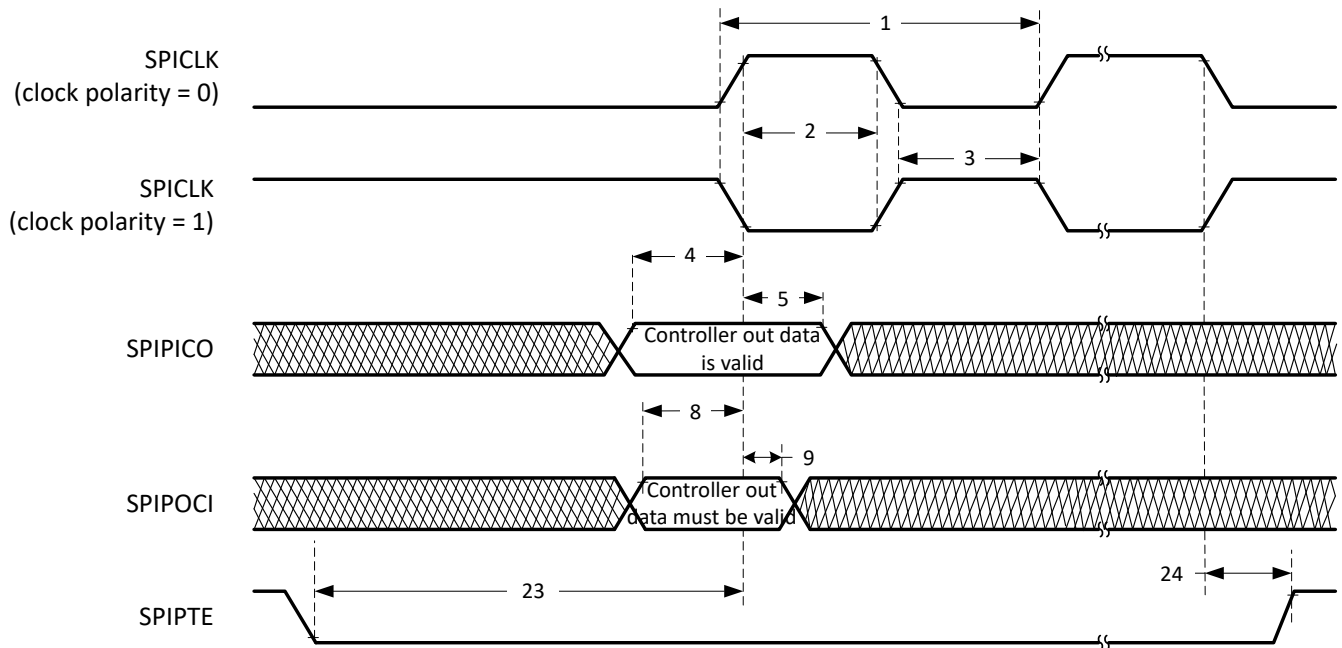
ADVANCE INFORMATION

6.16.5.1.4 SPI Controller Mode Timing Diagrams



- A. On the trailing end of the word, $\overline{\text{SPIPTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-64. SPI Controller Mode External Timing (Clock Phase = 0)



- A. On the trailing end of the word, $\overline{\text{SPIPTE}}$ will go inactive except between back-to-back transmit words in both FIFO and non-FIFO modes.

Figure 6-65. SPI Controller Mode External Timing (Clock Phase = 1)

6.16.5.2 SPI Peripheral Mode Timings

The following section contains the SPI Peripheral Mode Timings.

6.16.5.2.1 SPI Peripheral Mode Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|-----------------|--|-----------------------|-----|------|
| 12 | $t_{c(SPC)}S$ | Cycle time, SPICLK | $4t_{c(SYSCLK)}$ | | ns |
| 13 | $t_{w(SPC1)}S$ | Pulse duration, SPICLK, first pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 14 | $t_{w(SPC2)}S$ | Pulse duration, SPICLK, second pulse | $2t_{c(SYSCLK)} - 1$ | | ns |
| 19 | $t_{su(PICO)}S$ | Setup time, SPIPICO valid before SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 20 | $t_{h(PICO)}S$ | Hold time, SPIPICO valid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |
| 25 | $t_{su(STE)}S$ | Setup time, SPIPTE valid before SPICLK (Clock Phase = 0) | $2t_{c(SYSCLK)} + 15$ | | ns |
| | | Setup time, SPIPTE valid before SPICLK (Clock Phase = 1) | $2t_{c(SYSCLK)} + 15$ | | ns |
| 26 | $t_{h(STE)}S$ | Hold time, SPIPTE invalid after SPICLK | $1.5t_{c(SYSCLK)}$ | | ns |

6.16.5.2.2 SPI Peripheral Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|-----|--------------------------|--|-----|------|------|
| 15 | $t_{d(POCI)}S$ | Delay time, SPICLK to SPIPOCI valid (non-high speed mode) | | 17 | ns |
| 15 | $t_{d(POCI)}S$ | Delay time, SPICLK to SPIPOCI valid (high-speed mode) | | 12.5 | ns |
| | | Delay time, SPICLK to SPIPOCI valid (high-speed mode)(when used on pins muxed with PMBUS - GPIO2, 3, 9, or 32) | | 14 | ns |
| | | Delay time, SPICLK to SPIPOCI valid (high-speed mode)(when used on pins muxed with USB - GPIO23 or 41) | | 16.7 | ns |
| 16 | $t_{v(POCI)}S$ | Valid time, SPIPOCI valid after SPICLK | 0 | | ns |

(1) 20-pF load on pin.

6.16.5.2.3 SPI Peripheral Mode Timing Diagrams

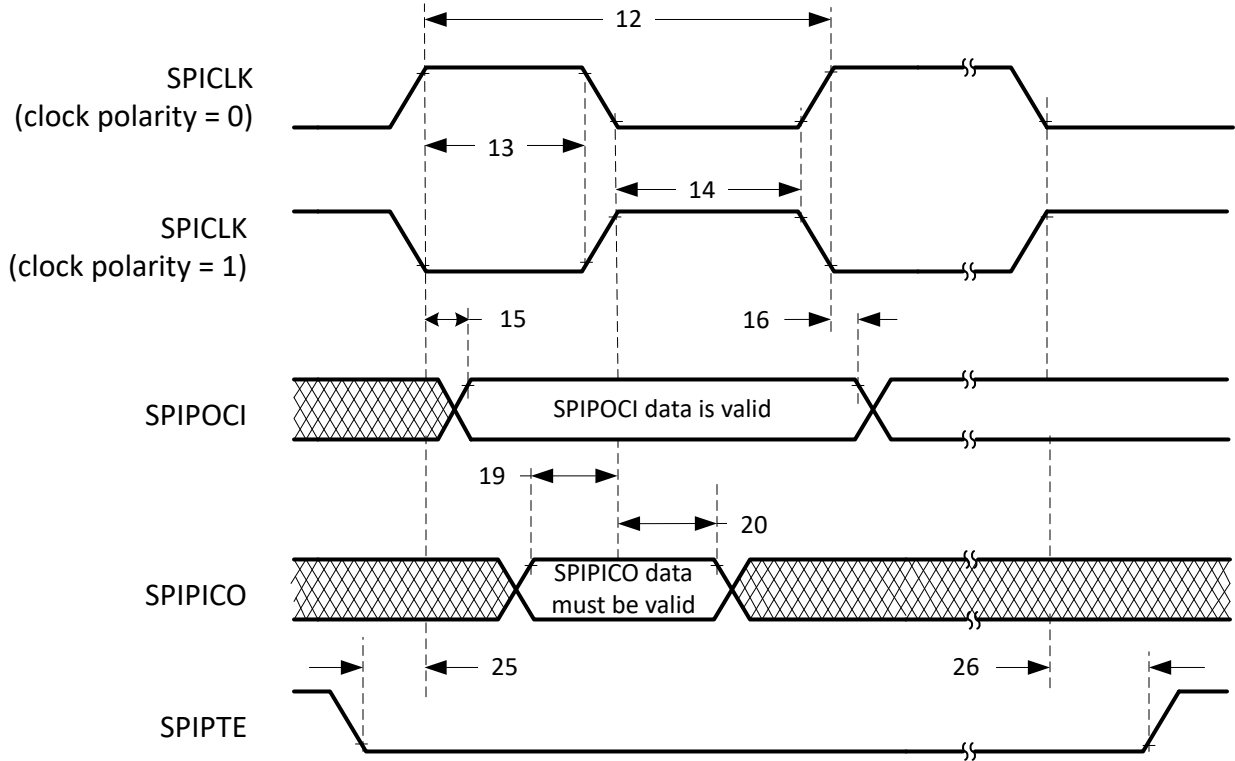


Figure 6-66. SPI Peripheral Mode External Timing (Clock Phase = 0)

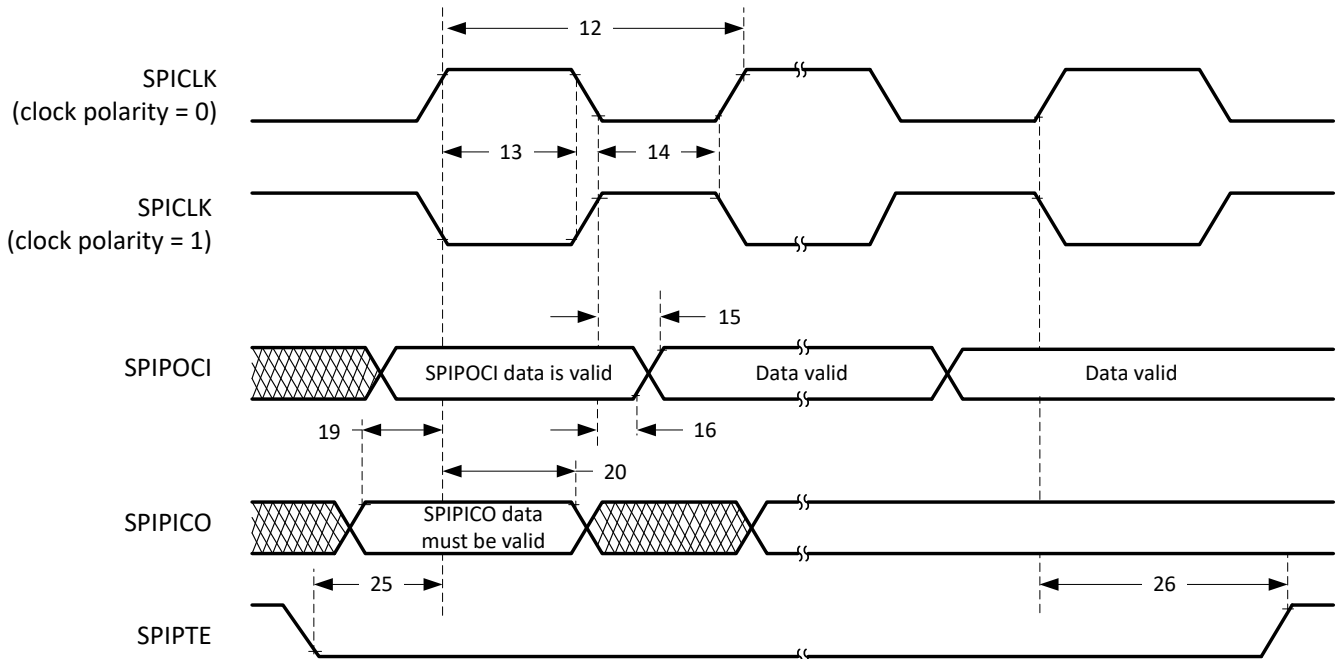


Figure 6-67. SPI Peripheral Mode External Timing (Clock Phase = 1)

6.16.6 Local Interconnect Network (LIN)

This device contains one Local Interconnect Network (LIN) module. The LIN module adheres to the LIN 2.1 standard as defined by the *LIN Specification Package Revision 2.1*. The LIN is a low-cost serial interface designed for applications where the CAN protocol may be too expensive to implement, such as small subnetworks for cabin comfort functions like interior lighting or window control in an automotive application.

The LIN standard is based on the SCI (UART) serial data link format. The communication concept is single-commander and multiple-responder with a message identification for multicast transmission between any network nodes.

The LIN module can be programmed to work either as an SCI or as a LIN as the core of the module is an SCI. The hardware features of the SCI are augmented to achieve LIN compatibility. The SCI module is a universal asynchronous receiver-transmitter (UART) that implements the standard non-return-to-zero format.

Though the registers are common for LIN and SCI, the register descriptions have notes to identify the register/bit usage in different modes. Because of this, code written for this module cannot be directly ported to the stand-alone SCI module and vice versa.

The LIN module has the following features:

- Compatibility with LIN 1.3, 2.0 and 2.1 protocols
- Configurable baud rate up to 20 kbps (as per LIN 2.1 protocol)
- Two external pins: LINRX and LINTX
- Multibuffered receive and transmit units
- Identification masks for message filtering
- Automatic commander header generation
 - Programmable synchronization break field
 - Synchronization field
 - Identifier field
- Responder automatic synchronization
 - Synchronization break detection
 - Optional baud rate update
 - Synchronization validation
- 2³¹ programmable transmission rates with 7 fractional bits
- Wakeup on LINRX dominant level from transceiver
- Automatic wake-up support
 - Wakeup signal generation
 - Expiration times on wakeup signals
- Automatic bus idle detection
- Error detection
 - Bit error
 - Bus error
 - No-response error
 - Checksum error
 - Synchronization field error
 - Parity error
- Capability to use direct memory access (DMA) for transmit and receive data
- Two interrupt lines with priority encoding for:
 - Receive
 - Transmit
 - ID, error, and status
- Support for LIN 2.0 checksum
- Enhanced synchronizer finite state machine (FSM) support for frame processing
- Enhanced handling of extended frames
- Enhanced baud rate generator

- Update wakeup/go to sleep

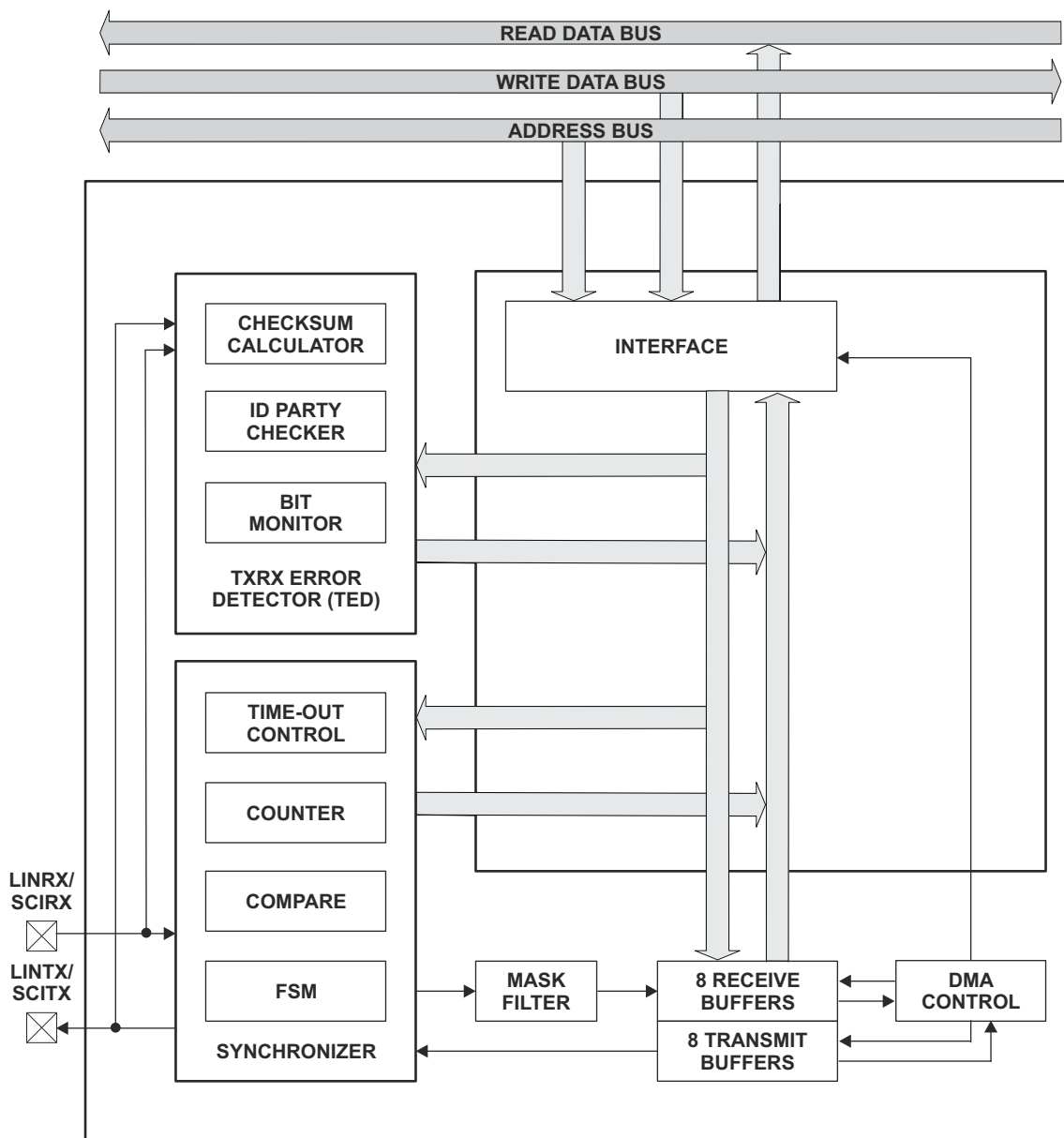


Figure 6-68. LIN Block Diagram

ADVANCE INFORMATION

6.16.7 Fast Serial Interface (FSI)

The Fast Serial Interface (FSI) module is a serial communication peripheral capable of reliable and robust high-speed communications. The FSI is designed to ensure data robustness across many system conditions such as chip-to-chip as well as board-to-board across an isolation barrier. Payload integrity checks such as CRC, start- and end-of-frame patterns, and user-defined tags, are encoded before transmit and then verified after receipt without additional CPU interaction. Line breaks can be detected using periodic transmissions, all managed and monitored by hardware. The FSI is also tightly integrated with other control peripherals on the device. To ensure that the latest sensor data or control parameters are available, frames can be transmitted on every control loop period. An integrated skew-compensation block has been added on the receiver to handle skew that may occur between the clock and data signals due to a variety of factors, including trace-length mismatch and skews induced by an isolation chip. With embedded data robustness checks, data-link integrity checks, skew compensation, and integration with control peripherals, the FSI can enable high-speed, robust communication in any system. These and many other features of the FSI follow.

The FSI module includes the following features:

- Independent transmitter and receiver cores
- Source-synchronous transmission
- Dual data rate (DDR)
- One or two data lines
- Programmable data length
- Skew adjustment block to compensate for board and system delay mismatches
- Frame error detection
- Programmable frame tagging for message filtering
- Hardware ping to detect line breaks during communication (ping watchdog)
- Two interrupts per FSI core
- Externally triggered frame generation
- Hardware- or software-calculated CRC
- Embedded ECC computation module
- Register write protection
- DMA support
- SPI compatibility mode (limited features available)

Operating the FSI at maximum speed (60 MHz) at dual data rate (120Mbps) may require the integrated skew compensation block to be configured according to the specific operating conditions on a case-by-case basis. The [Fast Serial Interface \(FSI\) Skew Compensation](#) Application Report provides example software on how to configure and set up the integrated skew compensation block on the Fast Serial Interface.

The FSI consists of independent transmitter (FSITX) and receiver (FSIRX) cores. The FSITX and FSIRX cores are configured and operated independently. The features available on the FSITX and FSIRX are described in the [FSI Transmitter](#) section and the [FSI Receiver](#) section of the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#), respectively.

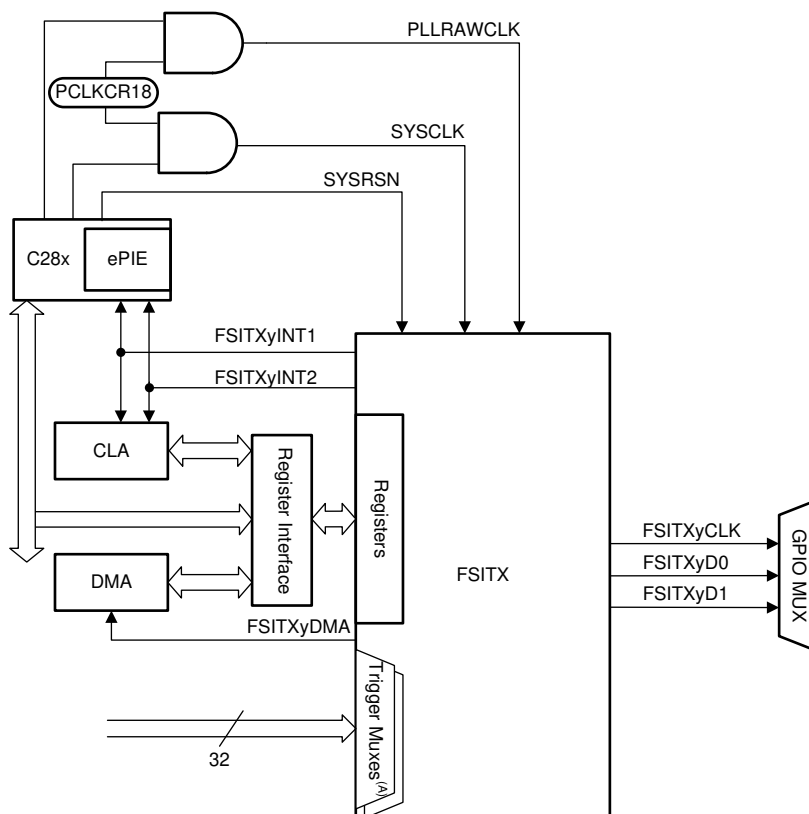
6.16.7.1 FSI Transmitter

The FSI transmitter module handles the framing of data, CRC generation, signal generation of TXCLK, TXD0, and TXD1, as well as interrupt generation. The operation of the transmitter core is controlled and configured through programmable control registers. The transmitter control registers let the CPU (or the CLA) program, control, and monitor the operation of the FSI transmitter. The transmit data buffer is accessible by the CPU, CLA, and the DMA.

The transmitter has the following features:

- Automated ping frame generation
- Externally triggered ping frames
- Externally triggered data frames
- Software-configurable frame lengths
- 16-word data buffer
- Data buffer underrun and overrun detection
- Hardware-generated CRC on data bits
- Software ECC calculation on select data
- DMA support
- CLA task triggering

Figure 6-69 shows the FSITX CPU interface. Figure 6-70 shows the high-level block diagram of the FSITX. Not all data paths and internal connections are shown. This diagram provides a high-level overview of the internal modules present in the FSITX.



A. The signals connected to the trigger muxes are described in the *External Frame Trigger Mux* section of the Fast Serial Interface (FSI) chapter in the *TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual*.

Figure 6-69. FSITX CPU Interface

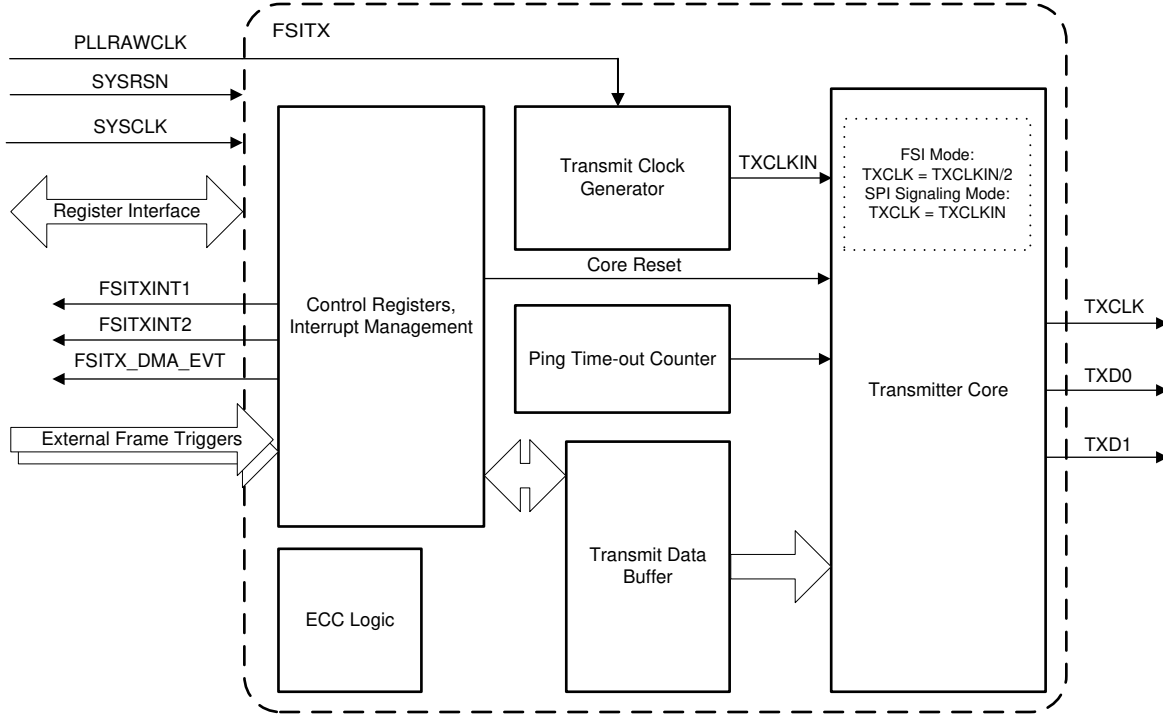


Figure 6-70. FSITX Block Diagram

6.16.7.1.1 FSITX Electrical Data and Timing

6.16.7.1.1.1 FSITX Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ | MIN | MAX | UNIT |
|-----|-----------------------------|-------------------------------|---------------------------------|------|
| 1 | $t_c(\text{TXCLK})$ | | 16.67 | ns |
| 1 | $t_c(\text{TXCLK})$ | | 26.67 | ns |
| 2 | $t_w(\text{TXCLK})$ | $(0.5t_c(\text{TXCLK})) - 1$ | $(0.5t_c(\text{TXCLK})) + 1$ | ns |
| 3 | $t_d(\text{TXCLK-TXD})$ | $(0.25t_c(\text{TXCLK})) - 2$ | $(0.25t_c(\text{TXCLK})) + 2$ | ns |
| 3 | $t_d(\text{TXCLK-TXD})$ | $(0.25t_c(\text{TXCLK})) - 2$ | $(0.25t_c(\text{TXCLK})) + 2.5$ | ns |
| 4 | $t_d(\text{TXCLK})$ | 9.4 | 30 | ns |
| 5 | $t_d(\text{TXD0})$ | 9.4 | 30 | ns |
| 6 | $t_d(\text{TXD1})$ | 9.4 | 30 | ns |
| 7 | $t_d(\text{DELAY_ELEMENT})$ | 0.29 | 1 | ns |

(1) 10-pF load on pin.

6.16.7.1.1.2 FSITX Timings

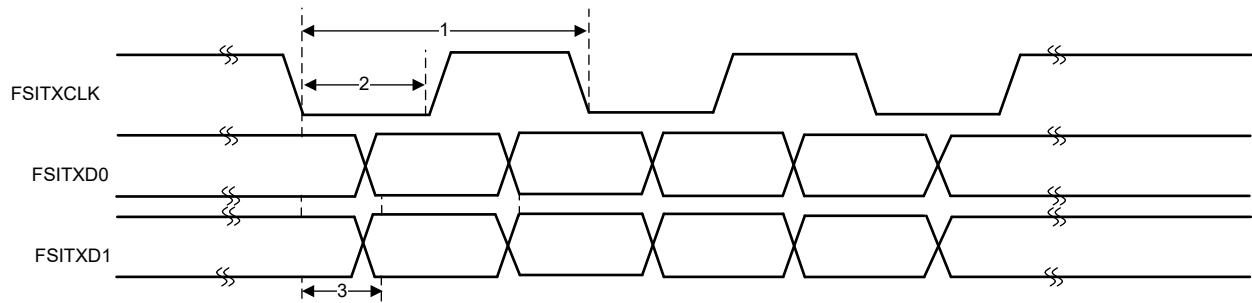


Figure 6-71. FSITX Timings

6.16.7.2 FSI Receiver

The receiver module interfaces to the FSI clock (RXCLK), and data lines (RXD0 and RXD1) after they pass through an optional programmable delay line. The receiver core handles the data framing, CRC computation, and frame-related error checking. The receiver bit clock and state machine are run by the RXCLK input, which is asynchronous to the device system clock.

The receiver control registers let the CPU program (or the CLA), control, and monitor the operation of the FSIRX. The receive data buffer is accessible by the CPU, CLA, and the DMA.

The receiver core has the following features:

- 16-word data buffer
- Multiple supported frame types
- Ping frame watchdog
- Frame watchdog
- CRC calculation and comparison in hardware
- ECC detection
- Programmable delay line control on incoming signals
- DMA support
- SPI compatibility mode
- CLA task triggering

Figure 6-72 shows the FSIRX CPU interface. Figure 6-73 provides a high-level overview of the internal modules present in the FSIRX. Not all data paths and internal connections are shown.

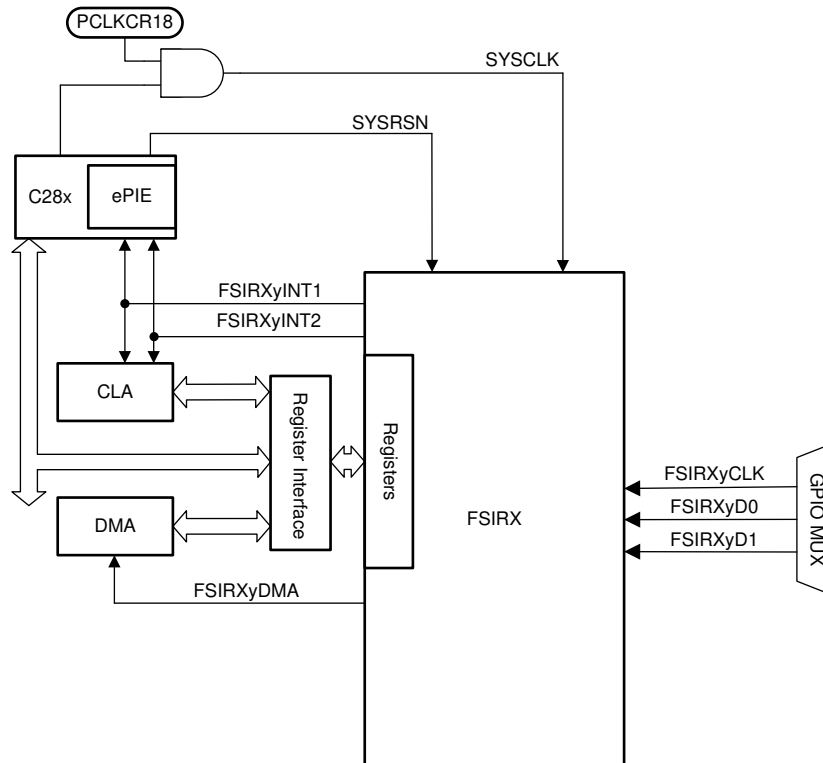


Figure 6-72. FSIRX CPU Interface

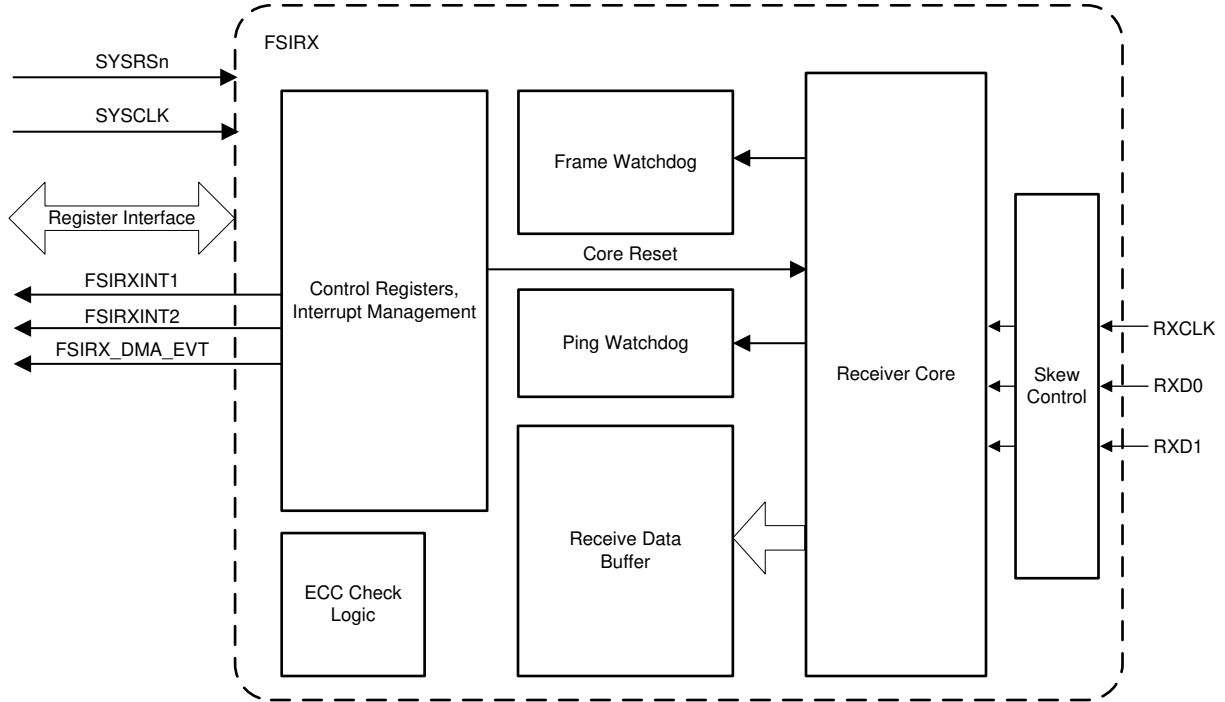


Figure 6-73. FSIRX Block Diagram

6.16.7.2.1 FSIRX Electrical Data and Timing

6.16.7.2.1.1 FSIRX Timing Requirements

| NO. | | | MIN | MAX | UNIT |
|-----|----------------------------|--|-------------------------|-------------------------|------|
| 1 | $t_c(\text{RXCLK})$ | Cycle time, RXCLK | | 16.67 | ns |
| 1 | $t_c(\text{RXCLK})$ | Cycle time, RXCLK(when any FSI signal is used on pins muxed with PMBUS - GPIO2, 3, 9, or 32) | | 26.67 | ns |
| 2 | $t_w(\text{RXCLK})$ | Pulse width, RXCLK low or RXCLK high. | $0.35t_c(\text{RXCLK})$ | $0.65t_c(\text{RXCLK})$ | ns |
| 3 | $t_{su}(\text{RXCLK-RXD})$ | Setup time with respect to RXCLK, applies to both edges of the clock | 1.7 | | ns |
| 3 | $t_{su}(\text{RXCLK-RXD})$ | Setup time with respect to RXCLK, applies to both edges of the clock(when used on pin muxed with PMBUS - GPIO2, 3, 9, or 32) | 2.6 | | ns |
| 4 | $t_h(\text{RXCLK-RXD})$ | Hold time with respect to RXCLK, applies to both edges of the clock | 2 | | ns |

6.16.7.2.1.2 FSIRX Switching Characteristics

| NO. | PARAMETER ⁽¹⁾ | MIN | MAX | UNIT | |
|------|-------------------------------------|--|------|------|----|
| 1 | $t_d(\text{RXCLK})$ | RXCLK delay compensation at RX_DLYLINE_CTRL[RXCLK_DLY]=31 | 9.7 | 30 | ns |
| 2 | $t_d(\text{RXD0})$ | RXD0 delay compensation at RX_DLYLINE_CTRL[RXD0_DLY]=31 | 9.7 | 30 | ns |
| 3 | $t_d(\text{RXD1})$ | RXD1 delay compensation at RX_DLYLINE_CTRL[RXD1_DLY]=31 | 9.7 | 30 | ns |
| 4 | $t_d(\text{DELAY_ELEMENT})$ | Incremental delay of each delay line element for RXCLK, RXD0, and RXD1 | 0.29 | 1 | ns |
| TDM1 | $t_{skew}(\text{TDM_CLK-TDM}_{Dx})$ | Delay skew introduced between RXCLK-TDM_CLK delay and RXDx-TDM_Dx delays | -3 | 3 | ns |
| TDM1 | $t_d(\text{RXCLK-TDM}_{CLK})$ | Delay time, RXCLK input to TDM_CLK output | 2 | 14.5 | ns |

6.16.7.2.1.2 FSIRX Switching Characteristics (continued)

| NO. | PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|------|--------------------------|---------------------------------------|-----|------|------|
| TDM2 | $t_{d(RXD0-TXD0)}$ | Delay time, RXD0 input to TXD0 output | 2 | 14.5 | ns |
| TDM3 | $t_{d(RXD1-TXD1)}$ | Delay time, RXD1 input to TXD1 output | 2 | 14.5 | ns |

(1) 10-pF load on pin.

6.16.7.2.1.3 FSIRX Timings

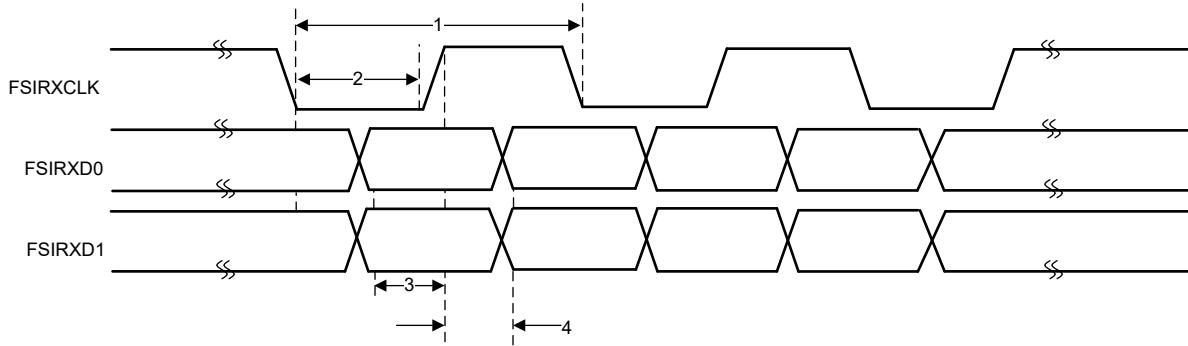


Figure 6-74. FSIRX Timings

6.16.7.3 FSI SPI Compatibility Mode

The FSI supports a SPI compatibility mode to enable communication with programmable SPI devices. In this mode, the FSI transmits its data in the same manner as a SPI in a single clock configuration mode. While the FSI is able to physically interface with a SPI in this mode, the external device must be able to encode and decode an FSI frame to communicate successfully. This is because the FSI transmits all SPI frame phases with the exception of the preamble and postamble. The FSI provides the same data validation and frame checking as if it was in standard FSI mode, allowing for more robust communication without consuming CPU cycles. The external SPI is required to send all relevant information and can access standard FSI features such as the ping frame watchdog on the FSIRX, frame tagging, or custom CRC values. The list of features of SPI compatibility mode follows:

- Data will transmit on rising edge and receive on falling edge of the clock.
- Only 16-bit word size is supported.
- TXD1 will be driven like an active-low chip-select signal. The signal will be low for the duration of the full frame transmission.
- No receiver chip-select input is required. RXD1 is not used. Data is shifted into the receiver on every active clock edge.
- No preamble or postamble clocks will be transmitted. All signals return to the idle state after the frame phase is finished.
- It is not possible to transmit in the SPI peripheral configuration because the FSI TXCLK cannot take an external clock source.

6.16.7.3.1 FSITX SPI Signaling Mode Electrical Data and Timing

Special timings are not required for the FSIRX in SPI signaling mode. FSIRX timings listed in the *FSIRX Timing Requirements* table are applicable in SPI compatibility mode. Setup and Hold times are only valid on the falling edge of FSIRXCLK because this is the active edge in SPI signaling mode.

6.16.7.3.1.1 FSITX SPI Signaling Mode Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

| NO. | PARAMETER ⁽¹⁾ | | MIN | MAX | UNIT |
|-----|--------------------------|--|-------------------------|-------------------------|------|
| 1 | $t_{c(TXCLK)}$ | Cycle time, TXCLK | | 16.67 | ns |
| 1 | $t_{c(TXCLK)}$ | Cycle time, TXCLK(when any FSI signal is used on pins muxed with PMBUS - GPIO2, 3, 9, or 32) | | 26.67 | ns |
| 2 | $t_{w(TXCLK)}$ | Pulse width, TXCLK low or TXCLK high | $(0.5t_{c(TXCLK)}) - 1$ | $(0.5t_{c(TXCLK)}) + 1$ | ns |
| 3 | $t_{d(TXCLKH-TXD0)}$ | Delay time, TXD0 valid after TXCLK high | | 3 | ns |
| 4 | $t_{d(TXD1-TXCLK)}$ | Delay time, TXCLK high after TXD1 low | $t_{w(TXCLK)} - 3$ | | ns |
| 5 | $t_{d(TXCLK-TXD1)}$ | Delay time, TXD1 high after TXCLK low | $t_{w(TXCLK)}$ | | ns |

(1) 10-pF load on pin

6.16.7.3.1.2 FSITX SPI Signaling Mode Timings

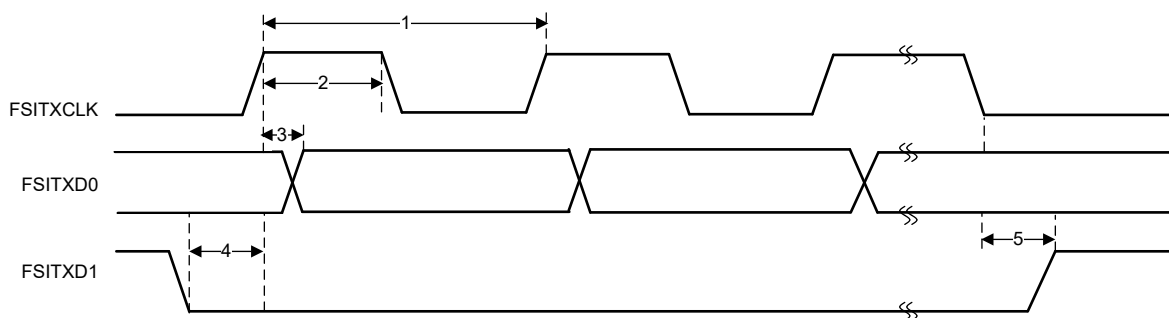


Figure 6-75. FSITX SPI Signaling Mode Timings

6.16.8 Universal Serial Bus (USB)

The USB controller operates as a full-speed or low-speed function controller during point-to-point communications with USB host or device functions.

The USB module has the following features:

- USB 2.0 full-speed and low-speed operation
- Integrated PHY
- Three transfer types: control, interrupt, and bulk
- 32 endpoints
 - One dedicated control IN endpoint and one dedicated control OUT endpoint
 - 15 configurable IN endpoints and 15 configurable OUT endpoints
- 4KB of dedicated endpoint memory

Figure 6-76 shows the USB block diagram.

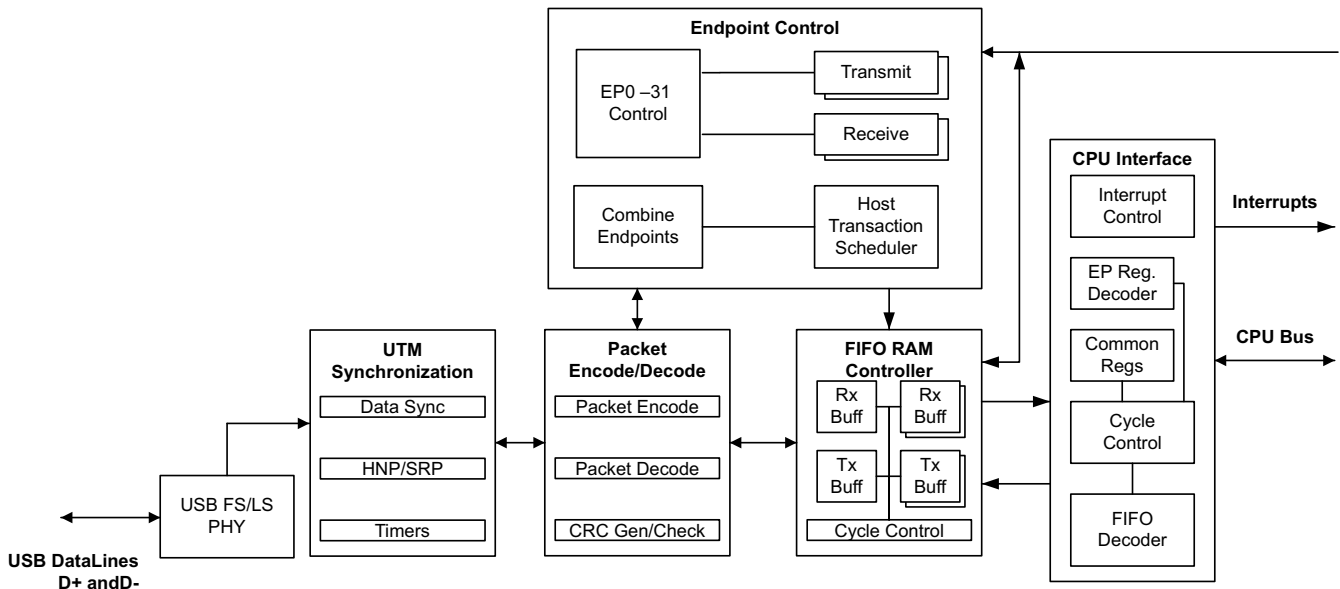


Figure 6-76. USB Block Diagram

Note

The accuracy of the on-chip zero-pin oscillator (see the *INTOSC Characteristics* section) will not meet the accuracy requirements of the USB protocol. An external clock source must be used for applications using USB. For applications using the USB boot mode, see the *Boot ROM and Peripheral Booting* section for clock frequency requirements.

6.16.8.1 USB Electrical Data and Timing

6.16.8.1.1 USB Input Ports DP and DM Timing Requirements

| | | MIN | MAX | UNIT |
|-----------------|--------------------------------------|-----|-----|------|
| V(CM) | Differential input common mode range | 0.8 | 2.5 | V |
| Z(IN) | Input impedance | 300 | | kΩ |
| VCRS | Crossover voltage | 1.3 | 2.0 | V |
| V _{IL} | Static SE input logic-low level | 0.8 | | V |
| V _{IH} | Static SE input logic-high level | | 2.0 | V |
| VDI | Differential input voltage | | 0.2 | V |

6.16.8.1.2 USB Output Ports DP and DM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|-----------------|---------------------|--|-----|-----|------|
| V _{OH} | D+, D– single-ended | USB 2.0 load conditions | 2.8 | 3.6 | V |
| V _{OL} | D+, D– single-ended | USB 2.0 load conditions | 0 | 0.3 | V |
| Z(DRV) | D+, D– impedance | | 28 | 44 | Ω |
| t _r | Rise time | Full speed, differential, C _L = 50 pF, 10%/90%, Rpu on D+ | 4 | 20 | ns |
| t _f | Fall time | Full speed, differential, C _L = 50 pF, 10%/90%, Rpu on D+ | 4 | 20 | ns |

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The TMS320F28P55x (F28P55x) is a member of the C2000™ real-time microcontroller family of scalable, ultra-low latency devices designed for efficiency in power electronics, including but not limited to: high power density, high switching frequencies, and supporting the use of GaN and SiC technologies.

These include such applications as:

- [Industrial motor drives](#)
- Motor control
 - [Traction inverter motor control](#)
 - [HVAC motor control](#)
 - [Mobile robot motor control](#)
- Solar inverters
 - [Central inverter](#)
 - [Micro inverter](#)
 - [String inverter](#)
- [Digital power](#)
- [Electrical vehicles and transportation](#)
- [EV charging infrastructure](#)

The [real-time control subsystem](#) is based on TI's 32-bit C28x DSP core, which provides 150 MIPS of signal-processing performance in each core for floating- or fixed-point code running from either on-chip flash or SRAM. The C28x CPU is further boosted by the [Trigonometric Math Unit \(TMU\)](#) and [VCRC \(Cyclical Redundancy Check\) extended instruction sets](#), speeding up common algorithms key to real-time control systems. Extended instruction sets enable IEEE double-precision 32-bit floating-point math. Finally, the [Control Law Accelerator \(CLA\)](#) enables an additional 150 MIPS per core of independent processing ability.

To allow fast context switching from existing to new firmware, hardware enhancements for Live Firmware Update (LFU) have been added to F28P55x.

High-performance analog blocks are tightly integrated with the processing and control units to provide optimal real-time signal chain performance. The Analog-to-Digital Converter (ADC) has been enhanced with up to 39 analog channels, 22 of which have general-purpose input/output (GPIO) capability. Implementation of oversampling is greatly simplified with hardware improvement. For safety-critical ADC conversions, a hardware redundancy checker has been added that provides the ability to compare ADC conversion results from multiple ADC modules for consistency without additional CPU cycles. Three Programmable Gain Amplifiers (PGAs) are present, supporting unity gain as well as up to 64x of non-inverting gain. Twenty-four frequency-independent PWMs, 16 with high-resolution capability, enable control of multiple power stages, from 3-phase inverters to advanced multilevel power topologies.

The inclusion of the Configurable Logic Block (CLB) allows the user to add [custom logic](#) and potentially [integrate FPGA-like functions](#) into the C2000 real-time MCU.

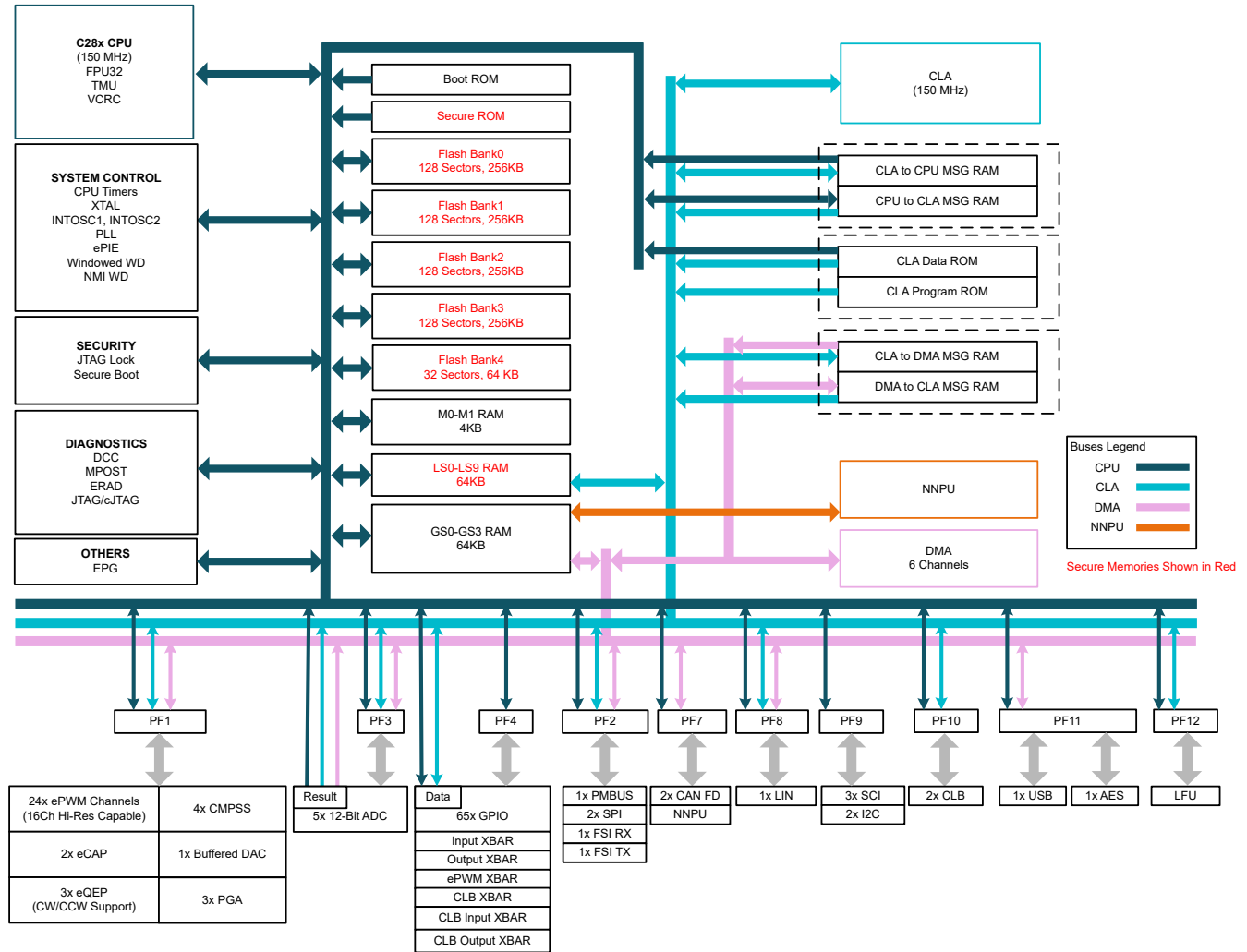
Industry-standard protocols like CAN FD and USB 2.0 are available on this device. The [Fast Serial Interface \(FSI\)](#) enables up to 200 Mbps of robust communications across an isolation boundary. Enhancements have been made to the PMBUS module to support Fast Plus mode.

Want to learn more about features that make C2000 MCUs the right choice for your real-time control system? Check out [The Essential Guide for Developing With C2000™ Real-Time Microcontrollers](#) and visit the [C2000™ real-time control MCUs](#) page.

7.2 Functional Block Diagram

Figure 7-1 shows the CPU system and associated peripherals.

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- A. The internal DAC from one of the CMPSS modules can be configured as an output DAC.
- B. The LIN module can also be used as a SCI module.

Figure 7-1. Functional Block Diagram

7.3 Memory

7.3.1 Memory Map

The *Memory Map* table describes the memory map. See the *Memory Controller Module* section of the System Control chapter in the *TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual*.

Table 7-1. Memory Map

| MEMORY | SIZE (x16) | START ADDRESS | END ADDRESS | CPU1.DMA ACCESS | CPU1.CLA1 DATA ACCESS | CPU1.CLA1 PROGRAM ACCESS | ECC/Parity | SECURITY | PART NUMBER |
|--------------------|------------|---------------|-------------|-----------------|-----------------------|--------------------------|------------|----------|---|
| M0 RAM | 1024 | 0x0000_0000 | 0x0000_03FF | - | - | - | ECC | - | All |
| M1 RAM | 1024 | 0x0000_0400 | 0x0000_07FF | - | - | - | ECC | - | All |
| PIE Vector Table | 512 | 0x0000_0D00 | 0x0000_0EFF | - | - | - | Parity | - | All |
| CLAtoCPU MSG RAM | 128 | 0x0000_1480 | 0x0000_14FF | - | YES | - | Parity | - | All |
| CPUtoCLA MSG RAM | 128 | 0x0000_1500 | 0x0000_157F | - | YES | - | Parity | - | All |
| CLAtoDMA MSG RAM | 128 | 0x0000_1680 | 0x0000_16FF | YES | YES | - | Parity | - | All |
| DMAtoCLA MSG RAM | 128 | 0x0000_1700 | 0x0000_177F | YES | YES | - | Parity | - | All |
| LS8 RAM - CLA Prog | 8192 | 0x0000_4000 | 0x0000_5FFF | - | - | YES | Parity | YES | F28P559SJ9-Q1, F28P550SJ9, F28P559SG9-Q1, F28P550SG9, F28P550SG8, F28P559SG8-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| LS9 RAM - CLA Prog | 8192 | 0x0000_6000 | 0x0000_7FFF | - | - | YES | Parity | YES | F28P559SJ9-Q1, F28P550SJ9, F28P559SG9-Q1, F28P550SG9, F28P550SG8, F28P559SG8-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| LS0 RAM | 2048 | 0x0000_8000 | 0x0000_87FF | - | YES | YES | Parity | YES | All |
| LS1 RAM | 2048 | 0x0000_8800 | 0x0000_8FFF | - | YES | YES | Parity | YES | All |
| LS2 RAM | 2048 | 0x0000_9000 | 0x0000_97FF | - | YES | YES | Parity | YES | All |
| LS3 RAM | 2048 | 0x0000_9800 | 0x0000_9FFF | - | YES | YES | Parity | YES | All |
| LS4 RAM | 2048 | 0x0000_A000 | 0x0000_A7FF | - | YES | YES | Parity | YES | All |
| LS5 RAM | 2048 | 0x0000_A800 | 0x0000_AFFF | - | YES | YES | Parity | YES | All |
| LS6 RAM | 2048 | 0x0000_B000 | 0x0000_B7FF | - | YES | YES | Parity | YES | All |
| LS7 RAM | 2048 | 0x0000_B800 | 0x0000_BFFF | - | YES | YES | Parity | YES | All |
| GS0 RAM | 8192 | 0x0000_C000 | 0x0000_DFFF | YES | - | - | Parity | - | All |
| GS1 RAM | 8192 | 0x0000_E000 | 0x0000_FFFF | YES | - | - | Parity | - | All |
| CLA Data ROM | 4096 | 0x0000_F000 | 0x0000_FFFF | - | YES | - | Parity | - | F28P559SJ9-Q1, F28P550SJ9, F28P559SG9-Q1, F28P550SG9, F28P550SG8, F28P559SG8-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| GS2 RAM | 8192 | 0x0001_0000 | 0x0001_1FFF | YES | - | - | Parity | - | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ2-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| GS3 RAM | 8192 | 0x0001_2000 | 0x0001_3FFF | YES | - | - | Parity | - | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ2-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| LS8 RAM - CPU | 8192 | 0x0001_4000 | 0x0001_5FFF | - | - | - | Parity | YES | F28P559SJ9-Q1, F28P550SJ9, F28P559SG9-Q1, F28P550SG9, F28P559SG8-Q1, F28P559SJ2-Q1, F28P550SG8, F28P559SJ6-Q1, F28P550SJ6 |

Table 7-1. Memory Map (continued)

| MEMORY | SIZE (x16) | START ADDRESS | END ADDRESS | CPU1.DMA ACCESS | CPU1.CLA1 DATA ACCESS | CPU1.CLA1 PROGRAM ACCESS | ECC/Parity | SECURITY | PART NUMBER |
|-------------------------------------|------------|---------------|-------------|-----------------|-----------------------|--------------------------|------------|----------|---|
| LS9 RAM - CPU | 8192 | 0x0001_6000 | 0x0001_7FFF | - | - | - | Parity | YES | F28P559SJ9-Q1,F28P550SJ9,F28P559SG9-Q1,F28P550SG9,F28P559SG8-Q1,F28P559SG2-Q1,F28P559SJ2-Q1,F28P550SG8,F28P559SJ6-Q1,F28P550SJ6 |
| USB RAM | 2048 | 0x0004_1000 | 0x0004_17FF | YES | - | - | - | - | F28P559SJ9-Q1,F28P550SJ9,F28P559SG9-Q1,F28P550SG9,F28P559SJ6-Q1,F28P550SJ6 |
| MCANA Message RAM (CPU Access mode) | 2048 | 0x0005_8000 | 0x0005_87FF | YES | - | - | ECC | - | All |
| MCANA Message RAM (Peripheral mode) | 4096 | 0x0005_8000 | 0x0005_8FFF | YES | - | - | ECC | - | All |
| MCANB Message RAM (Peripheral mode) | 4096 | 0x0005_A000 | 0x0005_AFFF | YES | - | - | ECC | - | All |
| MCANB Message RAM (CPU Access mode) | 2048 | 0x0005_A000 | 0x0005_A7FF | YES | - | - | ECC | - | All |
| TI OTP Bank 0 | 1536 | 0x0007_2000 | 0x0007_25FF | - | - | - | ECC | - | All |
| UID_REGS | 6 | 0x0007_2172 | 0x0007_2177 | - | - | - | ECC | - | All |
| TI OTP Bank 1 | 1536 | 0x0007_3000 | 0x0007_35FF | - | - | - | ECC | - | F28P559SJ9-Q1,F28P550SJ9,F28P559SJ2-Q1,F28P559SJ6-Q1,F28P550SJ6 |
| TI OTP Bank 2 | 1536 | 0x0007_4000 | 0x0007_45FF | - | - | - | ECC | - | All |
| TI OTP Bank 3 | 1536 | 0x0007_5000 | 0x0007_55FF | - | - | - | ECC | - | F28P559SJ9-Q1,F28P550SJ9,F28P559SJ2-Q1,F28P559SJ6-Q1,F28P550SJ6 |
| TI OTP Bank 4 | 1536 | 0x0007_6000 | 0x0007_65FF | - | - | - | ECC | - | F28P559SJ9-Q1,F28P550SJ9,F28P559SJ2-Q1,F28P559SJ6-Q1,F28P550SJ6,F28P559SG9-Q1,F28P550SG9 |
| DCSM BANK0 Z1 OTP | 512 | 0x0007_8000 | 0x0007_81FF | - | - | - | ECC | YES | All |
| DCSM BANK0 Z2 OTP | 512 | 0x0007_8200 | 0x0007_83FF | - | - | - | ECC | YES | All |
| User OTP Bank 1 | 1024 | 0x0007_8800 | 0x0007_8BFF | - | - | - | ECC | - | F28P559SJ9-Q1,F28P550SJ9,F28P559SJ2-Q1,F28P559SJ6-Q1,F28P550SJ6 |
| User OTP Bank 2 | 1024 | 0x0007_9000 | 0x0007_93FF | - | - | - | ECC | - | All |
| User OTP Bank 3 | 1024 | 0x0007_9800 | 0x0007_9BFF | - | - | - | ECC | - | F28P559SJ9-Q1,F28P550SJ9,F28P559SJ2-Q1,F28P559SJ6-Q1,F28P550SJ6 |
| User OTP Bank 4 | 1024 | 0x0007_A000 | 0x0007_A3FF | - | - | - | ECC | - | F28P559SG9-Q1,F28P550SG9 |
| Flash Bank 0 | 131072 | 0x0008_0000 | 0x0009_FFFF | - | - | - | ECC | YES | All |

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Table 7-1. Memory Map (continued)

| MEMORY | SIZE (x16) | START ADDRESS | END ADDRESS | CPU1.DMA ACCESS | CPU1.CLA1 DATA ACCESS | CPU1.CLA1 PROGRAM ACCESS | ECC/Parity | SECURITY | PART NUMBER |
|---------------------------|------------|---------------|-------------|-----------------|-----------------------|--------------------------|------------|----------|--|
| Flash Bank 1 | 131072 | 0x000A_0000 | 0x000B_FFFF | - | - | - | ECC | YES | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ2-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| Flash Bank 2 | 131072 | 0x000C_0000 | 0x000D_FFFF | - | - | - | ECC | YES | All |
| Flash Bank 3 | 131072 | 0x000E_0000 | 0x000F_FFFF | - | - | - | ECC | YES | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ2-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| Flash Bank 4 | 32768 | 0x0010_0000 | 0x0010_7FFF | - | - | - | ECC | YES | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ2-Q1, F28P559SJ6-Q1, F28P550SJ6, F28P559SG9-Q1, F28P550SG9 |
| Z1-SecureBoot Functions | 3072 | 0x003F_4000 | 0x003F_4BFF | - | - | - | Parity | YES | All |
| Z1-Safe Functions | 1536 | 0x003F_4C00 | 0x003F_51FF | - | - | - | Parity | YES | All |
| Z2-Safe Functions | 1536 | 0x003F_5600 | 0x003F_5BFF | - | - | - | Parity | YES | All |
| CPU STL | 9216 | 0x003F_5C00 | 0x003F_7FFF | - | - | - | Parity | - | All |
| Boot ROM | 32768 | 0x003F_8000 | 0x003F_FFFF | - | - | - | Parity | - | All |
| PIE Vector Table Swap | 512 | 0x0100_0900 | 0x0100_0AFF | - | - | - | Parity | - | All |
| CLA Data ROM (CPU Mapped) | 4096 | 0x0100_1000 | 0x0100_1FFF | - | - | - | Parity | - | F28P559SJ9-Q1, F28P550SJ9, F28P559SG9-Q1, F28P550SG9, F28P550SG8, F28P559SG8-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| TI OTP Bank 0 ECC | 192 | 0x0107_0400 | 0x0107_04BF | - | - | - | - | - | All |
| TI OTP Bank 1 ECC | 192 | 0x0107_0600 | 0x0107_06BF | - | - | - | - | - | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ2-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| TI OTP Bank 2 ECC | 192 | 0x0107_0800 | 0x0107_08BF | - | - | - | - | - | All |
| TI OTP Bank 3 ECC | 192 | 0x0107_0A00 | 0x0107_0ABF | - | - | - | - | - | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ2-Q1, F28P559SJ6-Q1, F28P550SJ6 |
| TI OTP Bank 4 ECC | 192 | 0x0107_0C00 | 0x0107_0CBF | - | - | - | - | - | F28P559SJ9-Q1, F28P550SJ9, F28P559SJ2-Q1, F28P559SJ6-Q1, F28P550SJ6, F28P559SG9-Q1, F28P550SG9 |

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7.3.1.1 Dedicated RAM (Mx RAM)

The CPU subsystem has two dedicated ECC-capable RAM blocks: M0 and M1. These memories are small nonsecure blocks that are tightly coupled with the CPU (that is, only the CPU has access to them).

7.3.1.2 Local Shared RAM (LSx RAM)

Local shared RAMs (LSx RAMs) are accessible to the CPU and CLA. All LSx RAM blocks have parity. These memories are secure and have CPU access protection (CPU write/CPU fetch).

7.3.1.3 Global Shared RAM (GSx RAM)

Global shared RAMs (GSx RAMs) are accessible from the CPU and DMA. The CPU and DMA have full read and write access to these memories. All GSx RAM blocks have parity. The GSx RAMs have access protection (CPU write/CPU fetch/DMA write/HIC write).

7.3.1.4 Message RAM

There are two types of message RAMs on this device that can be used to share between CPU, CLA and DMA. CLA-CPU message RAM shares data between the CLA and CPU while the CLA-DMA message RAM shares data between the CLA and DMA.

7.3.2 Control Law Accelerator (CLA) Memory Map

Table 7-2 shows the CLA data ROM memory map.

Table 7-2. CLA Data ROM Memory Map

| MEMORY | START ADDRESS | LENGTH |
|-------------------|---------------|--------|
| FFT Tables (Load) | 0x0100 1070 | 0x0800 |
| Data (Load) | 0x0100 1870 | 0x078A |
| Version (Load) | 0x0100 1FFA | 0x0006 |
| FFT Tables (Run) | 0x0000 F070 | 0x0800 |
| Data (Run) | 0x0000 F870 | 0x078A |
| Version (Run) | 0x0000 FFFA | 0x0006 |

7.3.3 Flash Memory Map

On the F28P55x devices, five flash banks (1084KB) are available. 4 banks are 256KB and the 5th bank is 64KB in size. Flash operations (erase and program) are performed at the bank level. Code cannot be executed from the same bank as an operation is being performed. Code can be allocated in a different flash bank, SRAM, or ROM while these operations are in progress. The *Addresses of Flash Sectors* table lists the addresses of flash sectors available for each part number.

7.3.3.1 Addresses of Flash Sectors

Table 7-3. Flash Memory Map

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|-----------------------|--------------------------------------|-----------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| OTP Sectors | | | | | | | |
| All F28P55x | TI OTP Bank 0 (Unsecure) | 1520 x 16 | 0x0007 2000 | 0x0007 25EF | 190 x 16 | 0x0107 0400 | 0x0107 04BD |
| | TI OTP Bank 0 (Secure) | 16 x 16 | 0x0007 25F0 | 0x0007 25FF | 2 x 16 | 0x0107 04BE | 0x0107 04BE |
| | TI OTP Bank 2 | 1536 x 16 | 0x0007 4000 | 0x0007 45FF | 192 x 16 | 0x0107 0800 | 0x0107 08BF |
| F28P55xSJx | TI OTP Bank 1 | 1536 x 16 | 0x0007 3000 | 0x0007 35FF | 192 x 16 | 0x0107 0600 | 0x0107 06BF |
| | TI OTP Bank 3 | 1536 x 16 | 0x0007 5000 | 0x0007 55FF | 192 x 16 | 0x0107 0A00 | 0x0107 0ABF |
| | TI OTP Bank 4 | 1536 x 16 | 0x0007 6000 | 0x0007 65FF | 192 x 16 | 0x0107 0C00 | 0x0107 0CBF |
| All F28P55x | User configurable DCSM Z1 OTP Bank 0 | 512 x 16 | 0x0007 8000 | 0x0007 81FF | 64 x 16 | 0x0107 1000 | 0x0107 103F |
| | User configurable DCSM Z2 OTP Bank 0 | 512 x 16 | 0x0007 8200 | 0x0007 83FF | 64 x 16 | 0x0107 1040 | 0x0107 107F |
| | User configurable OTP Bank 2 | 1K x 16 | 0x0007 9000 | 0x0007 93FF | 128 x 16 | 0x0107 1100 | 0x0107 117F |
| F28P55xSJx | User configurable OTP Bank 1 | 1K x 16 | 0x0007 8800 | 0x0007 8BFF | 128 x 16 | 0x0107 1080 | 0x0107 10FF |
| | User configurable OTP Bank 3 | 1K x 16 | 0x0007 9800 | 0x0007 9BFF | 128 x 16 | 0x0107 1180 | 0x0107 11FF |
| | User configurable OTP Bank 4 | 1K x 16 | 0x0007 A000 | 0x0007 A3FF | 128 x 16 | 0x0107 1200 | 0x0107 127F |
| Bank 0 Sectors | | | | | | | |
| All | Sector 0 | 1K x 16 | 0x0008 0000 | 0x0008 03FF | 128 x 16 | 0x0108 0000 | 0x0108 007F |
| | Sector 1 | 1K x 16 | 0x0008 0400 | 0x0008 07FF | 128 x 16 | 0x0108 0080 | 0x0108 00FF |
| | Sector 2 | 1K x 16 | 0x000800800 | 0x0008 0BFF | 128 x 16 | 0x0108 0100 | 0x0108 017F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 29 | 1K x 16 | 0x0008 7400 | 0x0008 77FF | 128 x 16 | 0x0108 0E80 | 0x0108 0EFF |
| | Sector 30 | 1K x 16 | 0x0008 7800 | 0x0008 7BFF | 128 x 16 | 0x0108 0F00 | 0x0108 0F7F |
| | Sector 31 | 1K x 16 | 0x0008 7C00 | 0x0008 7FFF | 128 x 16 | 0x0108 0F80 | 0x0108 0FFF |

Table 7-3. Flash Memory Map (continued)

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|--|------------|---------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| F28P55xSJx, F28P55xSGx, F28P55xSDx | Sector 32 | 1K x 16 | 0x0008 8000 | 0x0008 83FF | 512 x 16 | 0x0108 1000 | 0x0108 107F |
| | Sector 33 | 1K x 16 | 0x0008 8400 | 0x0008 87FF | 512 x 16 | 0x0108 1080 | 0x0108 10FF |
| | Sector 34 | 1K x 16 | 0x0008 8800 | 0x0008 8BFF | 512 x 16 | 0x0108 1100 | 0x0108 117F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 61 | 1K x 16 | 0x0008 F400 | 0x0008 F7FF | 512 x 16 | 0x0108 1E80 | 0x0108 1EFF |
| | Sector 62 | 1K x 16 | 0x0008 F800 | 0x0008 FBFF | 512 x 16 | 0x0108 1F00 | 0x0108 1F7F |
| | Sector 63 | 1K x 16 | 0x0008 FC00 | 0x0008 FFFF | 512 x 16 | 0x0108 1F80 | 0x0108 1FFF |
| F28P55xSJx, F28P55xSGx | Sector 64 | 1K x 16 | 0x0009 0000 | 0x0009 03FF | 512 x 16 | 0x0108 2000 | 0x0108 207F |
| | Sector 65 | 1K x 16 | 0x0009 0400 | 0x0009 07FF | 512 x 16 | 0x0108 2080 | 0x0108 20FF |
| | Sector 66 | 1K x 16 | 0x0009 0800 | 0x0009 0BFF | 512 x 16 | 0x0108 2100 | 0x0108 217F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 93 | 1K x 16 | 0x0009 7400 | 0x0009 77FF | 512 x 16 | 0x0108 2E80 | 0x0108 2EFF |
| | Sector 94 | 1K x 16 | 0x0009 7800 | 0x0009 7BFF | 512 x 16 | 0x0108 2F00 | 0x0108 2F7F |
| | Sector 95 | 1K x 16 | 0x0009 7C00 | 0x0009 7FFF | 512 x 16 | 0x0108 2F80 | 0x0108 2FFF |
| F28P55xSJx | Sector 96 | 1K x 16 | 0x0009 8000 | 0x0009 83FF | 512 x 16 | 0x0108 3000 | 0x0108 307F |
| | Sector 97 | 1K x 16 | 0x0009 8400 | 0x0009 87FF | 512 x 16 | 0x0108 3080 | 0x0108 30FF |
| | Sector 98 | 1K x 16 | 0x0009 8800 | 0x0009 8BFF | 512 x 16 | 0x0108 3100 | 0x0108 317F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 125 | 1K x 16 | 0x0009 F400 | 0x0009 F7FF | 512 x 16 | 0x0108 3E80 | 0x0108 3EFF |
| | Sector 126 | 1K x 16 | 0x0009 F800 | 0x0009 FBFF | 512 x 16 | 0x0108 3F00 | 0x0108 3F7F |
| | Sector 127 | 1K x 16 | 0x0009 FC00 | 0x0009 FFFF | 512 x 16 | 0x0108 3F80 | 0x0108 3FFF |
| Bank 1 Sectors | | | | | | | |
| F28P55xSJx only | Sector 0 | 1K x 16 | 0x000A 0000 | 0x000A 03FF | 128 x 16 | 0x0108 4000 | 0x0108 407F |
| | Sector 1 | 1K x 16 | 0x000A 0400 | 0x000A 07FF | 128 x 16 | 0x0108 4080 | 0x0108 40FF |
| | Sector 2 | 1K x 16 | 0x000A 0800 | 0x000A 0BFF | 128 x 16 | 0x0108 4100 | 0x0108 417F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 125 | 1K x 16 | 0x000B F400 | 0x000B F7FF | 128 x 16 | 0x0108 7E80 | 0x0108 7EFF |
| | Sector 126 | 1K x 16 | 0x000B F800 | 0x000B FBFF | 128 x 16 | 0x0108 7F00 | 0x0108 7F7F |
| | Sector 127 | 1K x 16 | 0x000B FC00 | 0x000B FFFF | 128 x 16 | 0x0108 7F80 | 0x0108 7FFF |
| Bank 2 Sectors | | | | | | | |
| All | Sector 0 | 1K x 16 | 0x000C 0000 | 0x000C 03FF | 128 x 16 | 0x0108 0000 | 0x0108 007F |
| | Sector 1 | 1K x 16 | 0x000C 0400 | 0x000C 07FF | 128 x 16 | 0x0108 0080 | 0x0108 00FF |
| | Sector 2 | 1K x 16 | 0x000C 0800 | 0x000C 0BFF | 128 x 16 | 0x0108 0100 | 0x0108 017F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 29 | 1K x 16 | 0x000C 7400 | 0x000C 77FF | 128 x 16 | 0x0108 0E80 | 0x0108 0EFF |
| | Sector 30 | 1K x 16 | 0x000C 7800 | 0x000C 7BFF | 128 x 16 | 0x0108 0F00 | 0x0108 0F7F |
| | Sector 31 | 1K x 16 | 0x000C 7C00 | 0x000C 7FFF | 128 x 16 | 0x0108 0F80 | 0x0108 0FFF |
| F28P55xSJx, F28P55xSGx, F28P55xSDx | Sector 32 | 1K x 16 | 0x000C 8000 | 0x000C 83FF | 512 x 16 | 0x0108 1000 | 0x0108 107F |
| | Sector 33 | 1K x 16 | 0x000C 8400 | 0x000C 87FF | 512 x 16 | 0x0108 1080 | 0x0108 10FF |
| | Sector 34 | 1K x 16 | 0x000C 8800 | 0x000C 8BFF | 512 x 16 | 0x0108 1100 | 0x0108 117F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 61 | 1K x 16 | 0x000C F400 | 0x000C F7FF | 512 x 16 | 0x0108 1E80 | 0x0108 1EFF |
| | Sector 62 | 1K x 16 | 0x000C F800 | 0x000C FBFF | 512 x 16 | 0x0108 1F00 | 0x0108 1F7F |
| | Sector 63 | 1K x 16 | 0x000C FC00 | 0x000C FFFF | 512 x 16 | 0x0108 1F80 | 0x0108 1FFF |

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Table 7-3. Flash Memory Map (continued)

| PART NUMBER | SECTOR | ADDRESS | | | ECC ADDRESS | | |
|---------------------------|------------|---------|-------------|-------------|-------------|-------------|-------------|
| | | SIZE | START | END | SIZE | START | END |
| F28P55xSJx, F28P55xSGx | Sector 64 | 1K x 16 | 0x000D 0000 | 0x000D 03FF | 512 x 16 | 0x0108 2000 | 0x0108 207F |
| | Sector 65 | 1K x 16 | 0x000D 0400 | 0x000D 07FF | 512 x 16 | 0x0108 2080 | 0x0108 20FF |
| | Sector 66 | 1K x 16 | 0x000D 0800 | 0x000D 0BFF | 512 x 16 | 0x0108 2100 | 0x0108 217F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 93 | 1K x 16 | 0x000D 7400 | 0x000D77FF | 512 x 16 | 0x0108 2E80 | 0x0108 2EFF |
| | Sector 94 | 1K x 16 | 0x000D 7800 | 0x000D 7BFF | 512 x 16 | 0x0108 2F00 | 0x0108 2F7F |
| | Sector 95 | 1K x 16 | 0x000D 7C00 | 0x000D 7FFF | 512 x 16 | 0x0108 2F80 | 0x0108 2FFF |
| F28P55xSJx | Sector 96 | 1K x 16 | 0x000D 8000 | 0x000D 83FF | 512 x 16 | 0x0108 3000 | 0x0108 307F |
| | Sector 97 | 1K x 16 | 0x000D 8400 | 0x000D 87FF | 512 x 16 | 0x0108 3080 | 0x0108 30FF |
| | Sector 98 | 1K x 16 | 0x000D 8800 | 0x000D 8BFF | 512 x 16 | 0x0108 3100 | 0x0108 317F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 125 | 1K x 16 | 0x000D F400 | 0x000D F7FF | 512 x 16 | 0x0108 3E80 | 0x0108 3EFF |
| | Sector 126 | 1K x 16 | 0x000D F800 | 0x000D FBFF | 512 x 16 | 0x0108 3F00 | 0x0108 3F7F |
| | Sector 127 | 1K x 16 | 0x000D FC00 | 0x000D FFFF | 512 x 16 | 0x0108 3F80 | 0x0108 3FFF |
| Bank 3 Sectors | | | | | | | |
| F28P55xSJx only | Sector 0 | 1K x 16 | 0x000E 0000 | 0x000E 03FF | 128 x 16 | 0x0108 C000 | 0x0108 C07F |
| | Sector 1 | 1K x 16 | 0x000E 0400 | 0x000E 07FF | 128 x 16 | 0x0108 C080 | 0x0108 C0FF |
| | Sector 2 | 1K x 16 | 0x000E 0800 | 0x000E 0BFF | 128 x 16 | 0x0108 C100 | 0x0108 C17F |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 125 | 1K x 16 | 0x000F F400 | 0x000F F7FF | 128 x 16 | 0x0108 FE80 | 0x0108 FEFF |
| | Sector 126 | 1K x 16 | 0x000F F800 | 0x000F FBFF | 128 x 16 | 0x0108 FF00 | 0x0108 FF7F |
| | Sector 127 | 1K x 16 | 0x000F FC00 | 0x000F FFFF | 128 x 16 | 0x0108 FF80 | 0x0108 FFFF |
| Bank 4 Sectors | | | | | | | |
| F28P55xSJx only | Sector 0 | 1K x 16 | 0x0010 0000 | 0x0010 03FF | 128 x 16 | 0x0109 0000 | 0x0109 007F |
| | Sector 1 | 1K x 16 | 0x0010 0400 | 0x0010 07FF | 128 x 16 | 0x0109 0080 | 0x0190 00FF |
| | Sector 2 | 1K x 16 | 0x0010 0800 | 0x0010 0BFF | 128 x 16 | 0x0109 0100 | 0x0109 0180 |
| | ... | ... | ... | ... | ... | ... | ... |
| | Sector 29 | 1K x 16 | 0x0010 7400 | 0x0010 77FF | 128 x 16 | 0x0109 0E80 | 0x0109 0EFF |
| | Sector 30 | 1K x 16 | 0x0010 7800 | 0x0010 7BFF | 128 x 16 | 0x0109 0F00 | 0x0109 0F7F |
| | Sector 31 | 1K x 16 | 0x0010 7C00 | 0x0010 7FFF | 128 x 16 | 0x0109 0F80 | 0x0109 0FFF |

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7.3.4 Peripheral Registers Memory Map

Table 7-4. Peripheral Registers Memory Map

| Structure | DriverLib Name | Base Address | CPU1 | CPU1.DMA | CPU1.CLA1 | Pipeline Protected |
|---------------------------------|--------------------------|--------------|------|----------|-----------|--------------------|
| Peripheral Frame 0 (PF0) | | | | | | |
| CPUTIMER_REGS | CPUTIMER0_BASE | 0x0000_0C00 | YES | - | - | - |
| CLA_ONLY_REGS | CLA1_ONLY_BASE | 0x0000_0C00 | - | - | YES | - |
| CPUTIMER_REGS | CPUTIMER1_BASE | 0x0000_0C08 | YES | - | - | - |
| CPUTIMER_REGS | CPUTIMER2_BASE | 0x0000_0C10 | YES | - | - | - |
| PIE_CTRL_REGS | PIECTRL_BASE | 0x0000_0CE0 | YES | - | - | - |
| CLA_SOFTINT_REGS | CLA1_SOFTINT_BASE | 0x0000_0CE0 | - | - | YES | - |
| PIE_VECT_TABLE | PIEVECTTABLE_BASE | 0x0000_0D00 | YES | - | - | - |
| DMA_REGS | DMA_BASE | 0x0000_1000 | YES | - | - | - |
| DMA_CH_REGS | DMA_CH1_BASE | 0x0000_1020 | YES | - | - | - |
| DMA_CH_REGS | DMA_CH2_BASE | 0x0000_1040 | YES | - | - | - |
| DMA_CH_REGS | DMA_CH3_BASE | 0x0000_1060 | YES | - | - | - |
| DMA_CH_REGS | DMA_CH4_BASE | 0x0000_1080 | YES | - | - | - |
| DMA_CH_REGS | DMA_CH5_BASE | 0x0000_10A0 | YES | - | - | - |
| DMA_CH_REGS | DMA_CH6_BASE | 0x0000_10C0 | YES | - | - | - |
| CLA_REGS | CLA1_BASE | 0x0000_1400 | YES | - | - | - |
| ADC_RESULT_REGS | ADCARESET_BASE | 0x0000_1800 | YES | YES | YES | - |
| ADC_RESULT_REGS | ADCBRESULT_BASE | 0x0000_1880 | YES | YES | YES | - |
| ADC_RESULT_REGS | ADCCRESULT_BASE | 0x0000_1900 | YES | YES | YES | - |
| ADC_RESULT_REGS | ADCDRESULT_BASE | 0x0000_1980 | YES | YES | YES | - |
| ADC_RESULT_REGS | ADCERESULT_BASE | 0x0000_1A00 | YES | YES | YES | - |
| PCTRACE_BUFFER_REGS | ERAD_PCTRACE_BUFFER_BASE | 0x0005_FE00 | YES | - | - | YES |
| UID_REGS | UID_BASE | 0x0007_2172 | YES | - | - | - |
| DCSM_Z1_OTP | DCSM_Z1OTP_BASE | 0x0007_8000 | YES | - | - | - |
| DCSM_Z2_OTP | DCSM_Z2OTP_BASE | 0x0007_8200 | YES | - | - | - |
| Peripheral Frame 1 (PF1) | | | | | | |
| EPWM_REGS | EPWM1_BASE | 0x0000_4000 | YES | YES | YES | YES |
| EPWM_REGS | EPWM2_BASE | 0x0000_4100 | YES | YES | YES | YES |
| EPWM_REGS | EPWM3_BASE | 0x0000_4200 | YES | YES | YES | YES |
| EPWM_REGS | EPWM4_BASE | 0x0000_4300 | YES | YES | YES | YES |
| EPWM_REGS | EPWM5_BASE | 0x0000_4400 | YES | YES | YES | YES |
| EPWM_REGS | EPWM6_BASE | 0x0000_4500 | YES | YES | YES | YES |
| EPWM_REGS | EPWM7_BASE | 0x0000_4600 | YES | YES | YES | YES |
| EPWM_REGS | EPWM8_BASE | 0x0000_4700 | YES | YES | YES | YES |

ADVANCE INFORMATION

Table 7-4. Peripheral Registers Memory Map (continued)

| Structure | DriverLib Name | Base Address | CPU1 | CPU1.DMA | CPU1.CLA1 | Pipeline Protected |
|---------------------------------|-------------------|--------------|------|----------|-----------|--------------------|
| EPWM_REGS | EPWM9_BASE | 0x0000_4800 | YES | YES | YES | YES |
| EPWM_REGS | EPWM10_BASE | 0x0000_4900 | YES | YES | YES | YES |
| EPWM_REGS | EPWM11_BASE | 0x0000_4A00 | YES | YES | YES | YES |
| EPWM_REGS | EPWM12_BASE | 0x0000_4B00 | YES | YES | YES | YES |
| EQEP_REGS | EQEP1_BASE | 0x0000_5100 | YES | YES | YES | YES |
| EQEP_REGS | EQEP2_BASE | 0x0000_5140 | YES | YES | YES | YES |
| EQEP_REGS | EQEP3_BASE | 0x0000_5180 | YES | YES | YES | YES |
| ECAP_REGS | ECAP1_BASE | 0x0000_5200 | YES | YES | YES | YES |
| ECAP_REGS | ECAP2_BASE | 0x0000_5240 | YES | YES | YES | YES |
| CMPSS_REGS | CMPSS1_BASE | 0x0000_5500 | YES | YES | YES | YES |
| CMPSS_REGS | CMPSS2_BASE | 0x0000_5540 | YES | YES | YES | YES |
| CMPSS_REGS | CMPSS3_BASE | 0x0000_5580 | YES | YES | YES | YES |
| CMPSS_REGS | CMPSS4_BASE | 0x0000_55C0 | YES | YES | YES | YES |
| PGA_REGS | PGA1_BASE | 0x0000_5B00 | YES | YES | YES | YES |
| PGA_REGS | PGA2_BASE | 0x0000_5B10 | YES | YES | YES | YES |
| PGA_REGS | PGA3_BASE | 0x0000_5B20 | YES | YES | YES | YES |
| DAC_REGS | DACA_BASE | 0x0000_5C00 | YES | YES | YES | YES |
| Peripheral Frame 2 (PF2) | | | | | | |
| SPI_REGS | SPIA_BASE | 0x0000_6100 | YES | YES | YES | YES |
| SPI_REGS | SPIB_BASE | 0x0000_6110 | YES | YES | YES | YES |
| PMBUS_REGS | PMBUSA_BASE | 0x0000_6400 | YES | YES | YES | YES |
| FSI_TX_REGS | FSITXA_BASE | 0x0000_6600 | YES | YES | YES | YES |
| FSI_RX_REGS | FSIRXA_BASE | 0x0000_6680 | YES | YES | YES | YES |
| Peripheral Frame 3 (PF3) | | | | | | |
| ADC_REGS | ADCC_BASE | 0x0000_6A00 | YES | - | YES | YES |
| ADC_REGS | ADCD_BASE | 0x0000_6C00 | YES | - | YES | YES |
| ADC_REGS | ADCE_BASE | 0x0000_6E00 | YES | - | YES | YES |
| ADC_REGS | ADCA_BASE | 0x0000_7400 | YES | - | YES | YES |
| ADC_REGS | ADCB_BASE | 0x0000_7600 | YES | - | YES | YES |
| Peripheral Frame 4 (PF4) | | | | | | |
| INPUT_XBAR_REGS | INPUTXBAR_BASE | 0x0000_7900 | YES | - | - | YES |
| XBAR_REGS | XBAR_BASE | 0x0000_7920 | YES | - | - | YES |
| SYNC_SOC_REGS | SYNCSOC_BASE | 0x0000_7940 | YES | - | - | YES |
| INPUT_XBAR_REGS | CLBINPUTXBAR_BASE | 0x0000_7960 | YES | - | - | YES |
| DMA_CLA_SRC_SEL_REGS | DMACLASRCSEL_BASE | 0x0000_7980 | YES | - | - | YES |

Table 7-4. Peripheral Registers Memory Map (continued)

| Structure | DriverLib Name | Base Address | CPU1 | CPU1.DMA | CPU1.CLA1 | Pipeline Protected |
|---------------------------------|----------------------|--------------|------|----------|-----------|--------------------|
| EPWM_XBAR_REGS | EPWMXBAR_BASE | 0x0000_7A00 | YES | - | - | YES |
| CLB_XBAR_REGS | CLBXBAR_BASE | 0x0000_7A40 | YES | - | - | YES |
| OUTPUT_XBAR_REGS | OUTPUTXBAR_BASE | 0x0000_7A80 | YES | - | - | YES |
| OUTPUT_XBAR_REGS | CLBOUTPUTXBAR_BASE | 0x0000_7BC0 | YES | - | - | YES |
| GPIO_CTRL_REGS | GPIOCTRL_BASE | 0x0000_7C00 | YES | - | - | YES |
| GPIO_DATA_REGS | GPIODATA_BASE | 0x0000_7F00 | YES | - | YES | YES |
| GPIO_DATA_READ_REGS | GPIODATAREAD_BASE | 0x0000_7F80 | YES | - | YES | YES |
| DEV_CFG_REGS | DEVCFG_BASE | 0x0005_D000 | YES | - | - | YES |
| CLK_CFG_REGS | CLKCFG_BASE | 0x0005_D200 | YES | - | - | YES |
| CPU_SYS_REGS | CPUSYS_BASE | 0x0005_D300 | YES | - | - | YES |
| SYS_STATUS_REGS | SYSSTAT_BASE | 0x0005_D400 | YES | - | - | YES |
| PERIPH_AC_REGS | PERIPHAC_BASE | 0x0005_D500 | YES | - | - | YES |
| ANALOG_SUBSYS_REGS | ANALOGSUBSYS_BASE | 0x0005_D700 | YES | - | - | YES |
| Peripheral Frame 6 (PF6) | | | | | | |
| ERAD_GLOBAL_REGS | ERAD_GLOBAL_BASE | 0x0005_E800 | YES | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP1_BASE | 0x0005_E900 | YES | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP2_BASE | 0x0005_E908 | YES | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP3_BASE | 0x0005_E910 | YES | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP4_BASE | 0x0005_E918 | YES | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP5_BASE | 0x0005_E920 | YES | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP6_BASE | 0x0005_E928 | YES | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP7_BASE | 0x0005_E930 | YES | - | - | YES |
| ERAD_HWBP_REGS | ERAD_HWBP8_BASE | 0x0005_E938 | YES | - | - | YES |
| ERAD_COUNTER_REGS | ERAD_COUNTER1_BASE | 0x0005_E980 | YES | - | - | YES |
| ERAD_COUNTER_REGS | ERAD_COUNTER2_BASE | 0x0005_E990 | YES | - | - | YES |
| ERAD_COUNTER_REGS | ERAD_COUNTER3_BASE | 0x0005_E9A0 | YES | - | - | YES |
| ERAD_COUNTER_REGS | ERAD_COUNTER4_BASE | 0x0005_E9B0 | YES | - | - | YES |
| ERAD_CRC_GLOBAL_REGS | ERAD_CRC_GLOBAL_BASE | 0x0005_EA00 | YES | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC1_BASE | 0x0005_EA10 | YES | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC2_BASE | 0x0005_EA20 | YES | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC3_BASE | 0x0005_EA30 | YES | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC4_BASE | 0x0005_EA40 | YES | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC5_BASE | 0x0005_EA50 | YES | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC6_BASE | 0x0005_EA60 | YES | - | - | YES |
| ERAD_CRC_REGS | ERAD_CRC7_BASE | 0x0005_EA70 | YES | - | - | YES |

Table 7-4. Peripheral Registers Memory Map (continued)

| Structure | DriverLib Name | Base Address | CPU1 | CPU1.DMA | CPU1.CLA1 | Pipeline Protected |
|---------------------------------|-----------------------|--------------|------|----------|-----------|--------------------|
| ERAD_CRC_REGS | ERAD_CRC8_BASE | 0x0005_EA80 | YES | - | - | YES |
| PCTRACE_REGS | ERAD_PCTRACE_BASE | 0x0005_EAD0 | YES | - | - | YES |
| EPG_REGS | EPG1_BASE | 0x0005_EC00 | YES | - | - | YES |
| EPG_MUX_REGS | EPG1MUX_BASE | 0x0005_ECD0 | YES | - | - | YES |
| DCSM_Z1_REGS | DCSM_Z1_BASE | 0x0005_F000 | YES | - | - | YES |
| DCSM_Z2_REGS | DCSM_Z2_BASE | 0x0005_F080 | YES | - | - | YES |
| DCSM_COMMON_REGS | DCSMCOMMON_BASE | 0x0005_F0C0 | YES | - | - | YES |
| MEM_CFG_REGS | MEMCFG_BASE | 0x0005_F400 | YES | - | - | YES |
| ACCESS_PROTECTION_REGS | ACCESSPROTECTION_BASE | 0x0005_F500 | YES | - | - | YES |
| MEMORY_ERROR_REGS | MEMORYERROR_BASE | 0x0005_F540 | YES | - | - | YES |
| TEST_ERROR_REGS | TESTERROR_BASE | 0x0005_F590 | YES | - | - | YES |
| FLASH_CTRL_REGS | FLASH0CTRL_BASE | 0x0005_F800 | YES | - | - | YES |
| FLASH_ECC_REGS | FLASH0ECC_BASE | 0x0005_FB00 | YES | - | - | YES |
| Peripheral Frame 7 (PF7) | | | | | | |
| NNPU_EXT_EVT_REGS | NNPU_EXTEVT_BASE | 0x0005_4000 | YES | - | - | YES |
| NNPU_EXT_GPRCM_REGS | NNPU_EXTGPRCM_BASE | 0x0005_400A | YES | - | - | YES |
| NNPU_IPSTANDARD_REGS | NNPU_IPSTANDARD_BASE | 0x0005_4020 | YES | - | - | YES |
| NNPU_IPSPECIFIC_REGS | NNPU_IPSPECIFIC_BASE | 0x0005_4100 | YES | - | - | YES |
| NNPU_DATA_REGS | NNPU_DATA_BASE | 0x0005_4700 | YES | - | - | YES |
| NNPU_ACC_REGS | NNPU_ACC_BASE | 0x0005_4C00 | YES | - | - | YES |
| NNPU_INSTRUCTION_REGS | NNPU_INSTRUCTION_BASE | 0x0005_5000 | YES | - | - | YES |
| NNPU_RFDATA_REGS | NNPU_RFDATA_BASE | 0x0005_5800 | YES | - | - | YES |
| MCANSS_REGS | MCANASS_BASE | 0x0005_9400 | YES | - | - | YES |
| MCAN_REGS | MCANA_BASE | 0x0005_9600 | YES | - | - | YES |
| MCAN_ERROR_REGS | MCANA_ERROR_BASE | 0x0005_9800 | YES | - | - | YES |
| MCANSS_REGS | MCANBSS_BASE | 0x0005_B400 | YES | - | - | YES |
| MCAN_REGS | MCANB_BASE | 0x0005_B600 | YES | - | - | YES |
| MCAN_ERROR_REGS | MCANB_ERROR_BASE | 0x0005_B800 | YES | - | - | YES |
| DCC_REGS | DCC0_BASE | 0x0005_E700 | YES | - | - | YES |
| DCC_REGS | DCC1_BASE | 0x0005_E740 | YES | - | - | YES |
| Peripheral Frame 8 (PF8) | | | | | | |
| LIN_REGS | LINA_BASE | 0x0000_6800 | YES | YES | YES | YES |
| Peripheral Frame 9 (PF9) | | | | | | |
| WD_REGS | WD_BASE | 0x0000_7000 | YES | - | - | YES |
| NMI_INTRUPT_REGS | NMI_BASE | 0x0000_7060 | YES | - | - | YES |

Table 7-4. Peripheral Registers Memory Map (continued)

| Structure | DriverLib Name | Base Address | CPU1 | CPU1.DMA | CPU1.CLA1 | Pipeline Protected |
|-----------------------------------|---------------------|--------------|------|----------|-----------|--------------------|
| XINT_REGS | XINT_BASE | 0x0000_7070 | YES | - | - | YES |
| SCI_REGS | SCIA_BASE | 0x0000_7200 | YES | - | - | YES |
| SCI_REGS | SCIB_BASE | 0x0000_7210 | YES | - | - | YES |
| SCI_REGS | SCIC_BASE | 0x0000_7220 | YES | - | - | YES |
| I2C_REGS | I2CA_BASE | 0x0000_7300 | YES | - | - | YES |
| I2C_REGS | I2CB_BASE | 0x0000_7340 | YES | - | - | YES |
| Peripheral Frame 10 (PF10) | | | | | | |
| CLB_LOGIC_CONFIG_REGS | CLB1_LOGICCFG_BASE | 0x0000_3000 | YES | - | YES | YES |
| CLB_LOGIC_CONTROL_REGS | CLB1_LOGICCTRL_BASE | 0x0000_3100 | YES | - | YES | YES |
| CLB_DATA_EXCHANGE_REGS | CLB1_DATAEXCH_BASE | 0x0000_3180 | YES | - | YES | YES |
| CLB_LOGIC_CONFIG_REGS | CLB2_LOGICCFG_BASE | 0x0000_3400 | YES | - | YES | YES |
| CLB_LOGIC_CONTROL_REGS | CLB2_LOGICCTRL_BASE | 0x0000_3500 | YES | - | YES | YES |
| CLB_DATA_EXCHANGE_REGS | CLB2_DATAEXCH_BASE | 0x0000_3580 | YES | - | YES | YES |
| Peripheral Frame 11 (PF11) | | | | | | |
| USB_REGS | USBA_BASE | 0x0004_0000 | YES | YES | - | YES |
| AES_REGS | AESA_BASE | 0x0004_2000 | YES | YES | - | YES |
| AES_SS_REGS | AESA_SS_BASE | 0x0004_2C00 | YES | YES | - | YES |
| Peripheral Frame 12 (PF12) | | | | | | |
| LFU_REGS | LFU_BASE | 0x0000_7FE0 | YES | - | YES | YES |

ADVANCE INFORMATION

7.4 Identification

Table 7-5 lists the Device Identification Registers. Additional information on these device identification registers can be found in the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#). See the register descriptions of PARTIDH and PARTIDL for identification of production status (TMX or TMS) and other device information.

Table 7-5. Device Identification Registers

| NAME | ADDRESS | SIZE (x16) | DESCRIPTION | | | | | | | | |
|-------------------|--|------------|---|---|----------------|--------------------|---|-------------------|--|-------------|---|
| PARTIDL | 0x0005 D008 | 2 | <table border="0"> <tr> <td style="text-align: center;"><i>Bits</i></td> <td style="text-align: center;"><i>Options</i></td> </tr> <tr> <td>14-13 INSTASPIN</td> <td>1 = InstaSPIN-FOC 2 = NONE 3 = NONE</td> </tr> <tr> <td>10-8 PIN_COUNT</td> <td>0 = 56 pin (QFN) 1 = 64 pin (QFP) 2 = 80 pin (QFP) 3 = 100 pin (QFP) 4 = 128 pin (QFP)</td> </tr> <tr> <td>7-6 QUAL</td> <td>0 = Engineering Sample (TMX) 1 = Pilot Production (TMP) 2 = Fully Qualified (TMS)</td> </tr> </table> | <i>Bits</i> | <i>Options</i> | 14-13 INSTASPIN | 1 = InstaSPIN-FOC 2 = NONE 3 = NONE | 10-8 PIN_COUNT | 0 = 56 pin (QFN) 1 = 64 pin (QFP) 2 = 80 pin (QFP) 3 = 100 pin (QFP) 4 = 128 pin (QFP) | 7-6 QUAL | 0 = Engineering Sample (TMX) 1 = Pilot Production (TMP) 2 = Fully Qualified (TMS) |
| | | | <i>Bits</i> | <i>Options</i> | | | | | | | |
| | | | 14-13 INSTASPIN | 1 = InstaSPIN-FOC 2 = NONE 3 = NONE | | | | | | | |
| 10-8 PIN_COUNT | 0 = 56 pin (QFN) 1 = 64 pin (QFP) 2 = 80 pin (QFP) 3 = 100 pin (QFP) 4 = 128 pin (QFP) | | | | | | | | | | |
| 7-6 QUAL | 0 = Engineering Sample (TMX) 1 = Pilot Production (TMP) 2 = Fully Qualified (TMS) | | | | | | | | | | |
| PARTIDH | 0x0005 D00A | 2 | Device part identification number | | | | | | | | |
| | | | TMS320F28P55xSJ9 | 0x09FF 0500 | | | | | | | |
| | | | TMS320F28P55xSJ6 | 0x09FC 0500 | | | | | | | |
| | | | TMS320F28P55xSJ2 | 0x09F8 0500 | | | | | | | |
| | | | TMS320F28P55xSG9 | 0x09F5 0500 | | | | | | | |
| | | | TMS320F28P55xSG8 | 0x09F4 0500 | | | | | | | |
| | | | TMS320F28P55xSG2 | 0x09EE 0500 | | | | | | | |
| TMS320F28P55xSD7 | 0x09E9 0500 | | | | | | | | | | |
| REVID | 0x0005 D00C | 2 | Silicon revision number Revision 0 0x0000 0001 | | | | | | | | |
| UID_UNIQUE | 0x0007 2172 | 4 | Unique identification number. This number is different on each individual device with the same PARTIDH. This unique number can be used as a serial number in the application. This number is present only on TMS devices. | | | | | | | | |

7.5 Bus Architecture – Peripheral Connectivity

The *Peripheral Connectivity* table lists a broad view of the peripheral and configuration register accessibility from each bus controller.

Table 7-6. Peripheral Connectivity

| PERIPHERAL | DMA | CLA | C28 |
|------------------------------------|-----|-----|-----|
| SYSTEM PERIPHERALS | | | |
| CPU Timers | | | Y |
| ERAD | | | Y |
| GPIO Data | | Y | Y |
| GPIO Pin Mapping and Configuration | | | Y |
| XBAR Configuration | | | Y |
| System Configuration | | | Y |
| AES | Y | | Y |
| EPG | | | Y |
| LFU | | Y | Y |
| DCC | | | Y |
| MEMORY | | | |
| M0/M1 | | | Y |
| LSx | | Y | Y |
| GSx | Y | | Y |
| ROM | | | Y |
| FLASH | | | Y |
| CONTROL PERIPHERALS | | | |
| ePWM/HRPWM | Y | Y | Y |
| eCAP | Y | Y | Y |
| eQEP ⁽¹⁾ | Y | Y | Y |
| CLB | | Y | Y |
| ANALOG PERIPHERALS | | | |
| CMPSS ⁽¹⁾ | Y | Y | Y |
| DAC ⁽¹⁾ | Y | Y | Y |
| ADC Configuration | | Y | Y |
| ADC Results ⁽¹⁾ | Y | Y | Y |
| PGA ⁽¹⁾ | Y | Y | Y |
| COMMUNICATION PERIPHERALS | | | |
| MCAN(CAN-FD) ⁽¹⁾ | Y | | Y |
| FSITX/FSIRX | Y | Y | Y |
| I2C | | | Y |
| LIN | Y | Y | Y |
| PMBus | Y | Y | Y |
| SCI | | | Y |
| SPI | Y | Y | Y |
| USB ⁽¹⁾ | Y | | Y |

(1) These modules are accessible from DMA but cannot trigger a DMA transfer.

7.6 C28x Processor

The CPU is a 32-bit fixed-point processor. This device draws from the best features of digital signal processing; reduced instruction set computing (RISC); and microcontroller architectures, firmware, and tool sets.

The CPU features include a modified Harvard architecture and circular addressing. The RISC features are single-cycle instruction execution, register-to-register operations, and modified Harvard architecture. The microcontroller features include ease of use through an intuitive instruction set, byte packing and unpacking, and bit manipulation. The modified Harvard architecture of the CPU enables instruction and data fetches to be performed in parallel. The CPU can read instructions and data while it writes data simultaneously to maintain the single-cycle instruction operation across the pipeline. The CPU does this over six separate address/data buses.

For more information on CPU architecture and instruction set, see the [TMS320C28x CPU and Instruction Set Reference Guide](#).

7.6.1 Floating-Point Unit (FPU)

The C28x plus floating-point (C28x+FPU) processor extends the capabilities of the C28x fixed-point CPU by adding registers and instructions to support IEEE single-precision floating-point operations.

Devices with the C28x+FPU include the standard C28x register set plus an additional set of floating-point unit registers. The additional floating-point unit registers are the following:

- Eight floating-point result registers, RnH (where n = 0–7)
- Floating-point Status Register (STF)
- Repeat Block Register (RB)

All of the floating-point registers, except the RB, are shadowed. This shadowing can be used in high-priority interrupts for fast context save and restore of the floating-point registers.

For more information on the C28x Floating Point Unit (FPU), see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.6.2 Trigonometric Math Unit (TMU)

The trigonometric math unit (TMU) extends the capabilities of a C28x+FPU by adding instructions and leveraging existing FPU instructions to speed up the execution of common trigonometric and arithmetic operations listed in [Table 7-7](#).

Table 7-7. TMU Supported Instructions

| Instructions | C Equivalent Operation | Pipeline Cycles |
|-------------------------|--|-----------------|
| MPY2PIF32 RaH,RbH | $a = b * 2\pi$ | 2/3 |
| DIV2PIF32 RaH,RbH | $a = b / 2\pi$ | 2/3 |
| DIVF32 RaH,RbH,RcH | $a = b/c$ | 5 |
| SQRTF32 RaH,RbH | $a = \text{sqrt}(b)$ | 5 |
| SINPUF32 RaH,RbH | $a = \sin(b*2\pi)$ | 4 |
| COSPUF32 RaH,RbH | $a = \cos(b*2\pi)$ | 4 |
| ATANPUF32 RaH,RbH | $a = \text{atan}(b)/2\pi$ | 4 |
| QUADF32 RaH,RbH,RcH,RdH | Operation to assist in calculating ATANPU2 | 5 |

Exponent instruction IEXP2F32 and logarithmic instruction LOG2F32 have been added to support computation of floating-point power function for the nonlinear proportional integral derivative control (NLPID) component of the C2000 Digital Control Library. These two added instructions reduce the power function calculations from a typical of 300 cycles using library emulation to less than 10 cycles.

No changes have been made to existing instructions, pipeline, or memory bus architecture. All TMU instructions use the existing FPU register set (R0H to R7H) to carry out the operations.

For more information, see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.6.3 VCRC Unit

Cyclic redundancy check (CRC) algorithms provide a straightforward method for verifying data integrity over large data blocks, communication packets, or code sections. The C28x+VCRC can perform 8-bit, 16-bit, 24-bit, and 32-bit CRCs. For example, the VCRC can compute the CRC for a block length of 10 bytes in 10 cycles. A CRC result register contains the current CRC, which is updated whenever a CRC instruction is executed.

The following are the CRC polynomials used by the CRC calculation logic of the VCRC:

- CRC8 polynomial = 0x07
- CRC16 polynomial 1 = 0x8005
- CRC16 polynomial 2 = 0x1021
- CRC24 polynomial = 0x5d6dcb
- CRC32 polynomial 1 = 0x04c11db7
- CRC32 polynomial 2 = 0x1edc6f41

This module can calculate CRCs for a byte of data in a single cycle. The CRC calculation for CRC8, CRC16, CRC24, and CRC32 is done byte-wise (instead of computing on a complete 16-bit or 32-bit data read by the C28x core) to match the byte-wise computation requirement mandated by various standards.

The VCRC Unit also allows the user to provide the size (1b-32b) and value of any polynomial to fit custom CRC requirements. The CRC execution time increases to three cycles when using a custom polynomial.

For more information on the Cyclic Redundancy Check (VCRC) instruction sets, see the [TMS320C28x Extended Instruction Sets Technical Reference Manual](#).

7.7 Control Law Accelerator (CLA)

The CLA Type-2 is an independent, fully programmable, 32-bit floating-point math processor that brings concurrent control-loop execution to the C28x family. The low interrupt-latency of the CLA allows it to read ADC samples "just-in-time." This significantly reduces the ADC sample to output delay to enable faster system response and higher MHz control loops. By using the CLA to service time-critical control loops, the main CPU is free to perform other system tasks such as communications and diagnostics.

The control law accelerator extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Using the CLA for time-critical tasks frees up the main CPU to perform other system and communication functions concurrently.

The following is a list of major features of the CLA:

- C compilers are available for CLA software development
- Clocked at the same rate as the main CPU (SYSCLKOUT).
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU.
 - Complete bus architecture:
 - Program Address Bus (PAB) and Program Data Bus (PDB)
 - Data Read Address Bus (DRAB), Data Read Data Bus (DRDB), Data Write Address Bus (DWAB), and Data Write Data Bus (DWDB)
 - Independent 8-stage pipeline.
 - 16-bit program counter (MPC)
 - Four 32-bit result registers (MR0 to MR3)
 - Two 16-bit auxiliary registers (MAR0, MAR1)
 - Status register (MSTF)
- Instruction set includes:
 - IEEE single-precision (32-bit) floating-point math operations
 - Floating-point math with parallel load or store
 - Floating-point multiply with parallel add or subtract
 - 1/X and 1/sqrt(X) estimations
 - Data type conversions
 - Conditional branch and call
 - Data load/store operations
- The CLA program code can consist of up to eight tasks or interrupt service routines, or seven tasks and a main background task.
 - The start address of each task is specified by the MVECT registers.
 - No limit on task size as long as the tasks fit within the configurable CLA program memory space.
 - One task is serviced at a time until its completion. There is no nesting of tasks.
 - Upon task completion a task-specific interrupt is flagged within the PIE.
 - When a task finishes the next highest-priority pending task is automatically started.
 - The Type-2 CLA can have a main task that runs continuously in the background, while other high-priority events trigger a foreground task.
- Task trigger mechanisms:
 - C28x CPU through the IACK instruction
 - Task1 to Task8: up to 256 possible trigger sources from peripherals connected to the shared bus on which the CLA assumes secondary ownership.
 - Task8 can be set to be the background task, while Tasks 1 to 7 take peripheral triggers.
- Memory and Shared Peripherals:
 - Two dedicated message RAMs for communication between the CLA and the main CPU.
 - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.
 - Two dedicated message RAMs for communication between the CLA and the DMA

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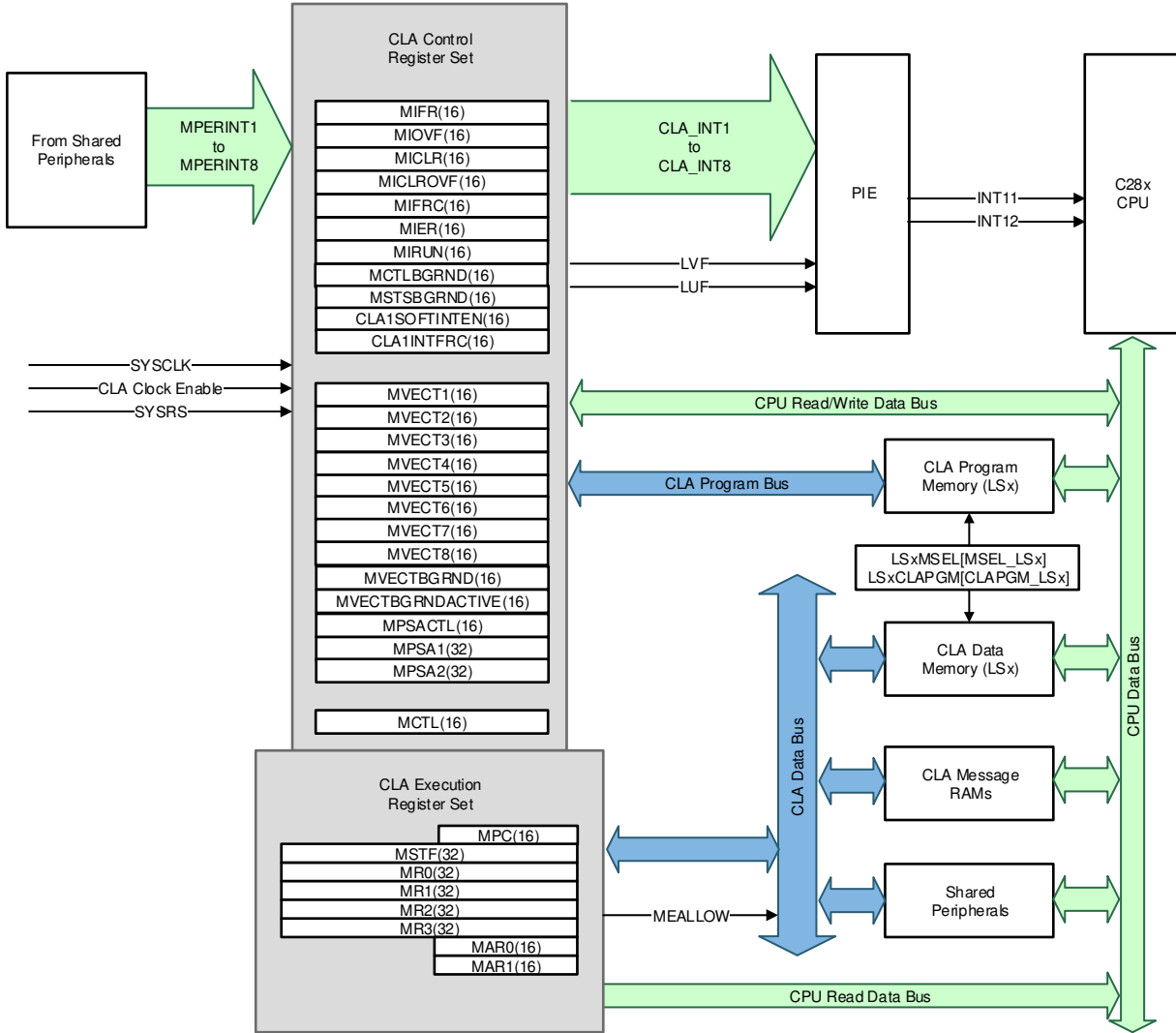


Figure 7-2. CLA Block Diagram

7.8 Embedded Real-Time Analysis and Diagnostic (ERAD)

The ERAD module enhances the debug and system-analysis capabilities of the device. The debug and system-analysis enhancements provided by the ERAD module is done outside of the CPU. The ERAD module consists of the Enhanced Bus Comparator units and the System Event Counter units. The Enhanced Bus Comparator units are used to generate hardware breakpoints, hardware watch points, and other output events. The System Event Counter units are used to analyze and profile the system. The ERAD module is accessible by the debugger and by the application software, which significantly increases the debug capabilities of many real-time systems, especially in situations where debuggers are not connected. In the TMS320F28P55x devices, the ERAD module contains eight Enhanced Bus Comparator units (which increases the number of Hardware breakpoints from two to ten) and four Benchmark System Event Counter units.

7.9 Direct Memory Access (DMA)

The DMA module provides a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Additionally, the DMA has the capability to orthogonally rearrange the data as it is transferred as well as “ping-pong” data between buffers. These features are useful for structuring data into blocks for optimal CPU processing. Figure 7-3 shows a device-level block diagram of the DMA.

DMA features include:

- Six channels with independent PIE interrupts
- Peripheral interrupt trigger sources
 - ADC interrupts and EVT signals
 - External Interrupts
 - ePWM SOC signals
 - CPU timers
 - eCAP
 - SPI transmit and receive
 - LIN transmit and receive
- Data sources and destinations:
 - GSx RAM
 - ADC result registers
 - Control peripheral registers (ePWM, eQEP, eCAP)
 - SPI, LIN, CAN, and PMBus registers
 - USB
 - PGA control registers
- Word Size: 16-bit or 32-bit (SPI limited to 16-bit)
- Throughput: Four cycles per word without arbitration

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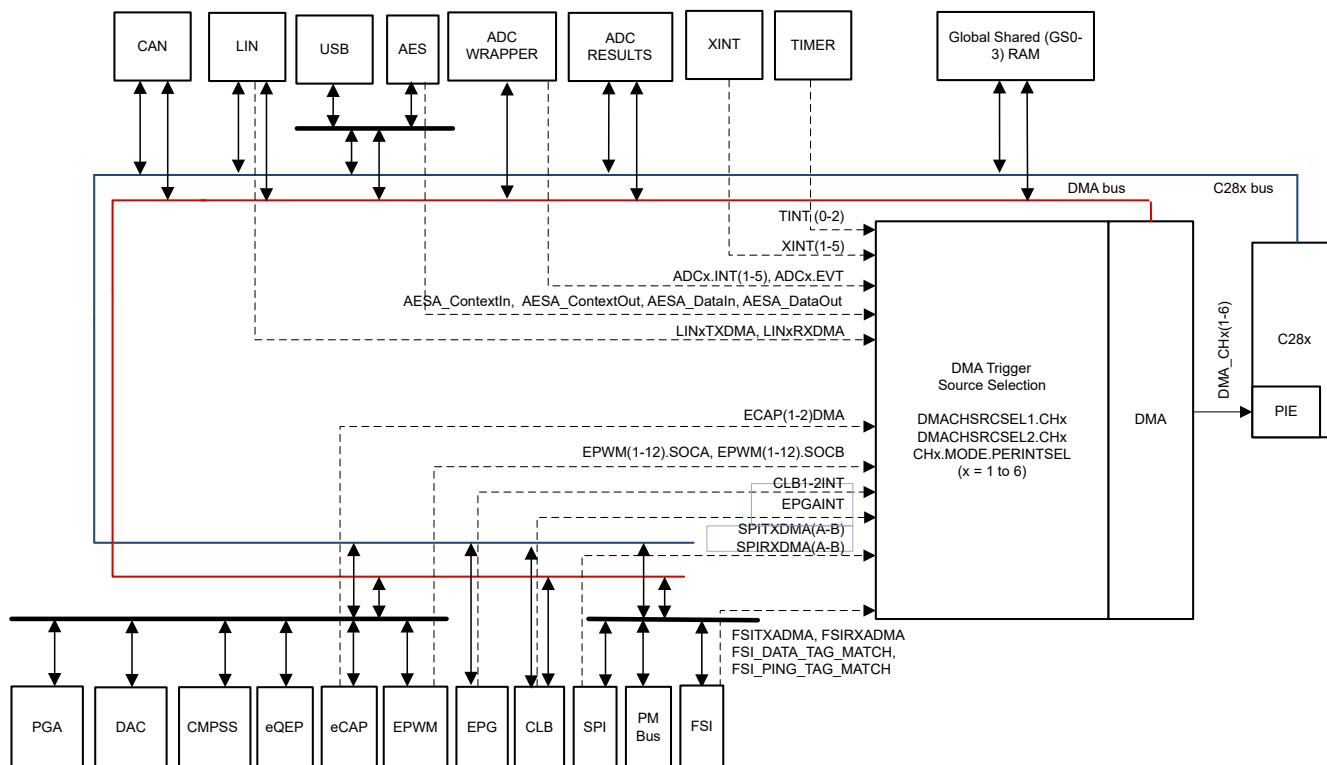


Figure 7-3. DMA Block Diagram

7.10 Device Boot Modes

This section explains the default boot modes, as well as all the available boot modes supported on this device. The boot ROM uses the boot mode select, general-purpose input/output (GPIO) pins to determine the boot mode configuration.

Table 7-8 shows the boot mode options available for selection by the default boot mode select pins. Users have the option to program the device to customize the boot modes selectable in the boot-up table as well as the boot mode select pin GPIOs used.

All the peripheral boot modes that are supported use the first instance of the peripheral module (SCIA, SPIA, I2CA, CANA, and so forth). Whenever these boot modes are referred to in this chapter, such as SCI boot, it is actually referring to the first module instance, which means the SCI boot on the SCIA port. The same applies to the other peripheral boots.

See the *Reset - XRSn - Switching Characteristics* table and the *Power-on Reset* figure for $t_{boot-flash}$, the boot ROM execution time to first instruction fetch in flash.

Table 7-8. Device Default Boot Modes

| BOOT MODE | GPIO24 (DEFAULT BOOT MODE SELECT PIN 1) | GPIO32 (DEFAULT BOOT MODE SELECT PIN 0) |
|--------------------------------|--|--|
| Parallel IO | 0 | 0 |
| SCI / Wait Boot ⁽¹⁾ | 0 | 1 |
| CAN(MCAN-NONFD) | 1 | 0 |
| Flash(USB) ⁽²⁾ | 1 | 1 |

- (1) SCI boot mode can be used as a wait boot mode as long as SCI continues to wait for an 'A' or 'a' during the SCI autobaud lock process.
- (2) If the default flash entry address is not programmed, the boot mode will switch to USB Boot for those devices that include the USB peripheral. On devices without a USB, the action will be to enter the ITRAP ISR if the default flash entry address is not programmed. The switch to USB boot is only supported for the default flash entry address option and not all entry address options.

7.10.1 Device Boot Configurations

This section details what boot configurations are available and how to configure them. This device supports from 0 boot mode select pins up to 3 boot mode select pins as well as from 1 configured boot mode up to 8 configured boot modes.

To change and configure the device from the default settings to custom settings for your application, use the following process:

1. Determine all the various ways you want application to be able to boot. (For example: Primary boot option of Flash boot for your main application, secondary boot option of CAN boot for firmware updates, tertiary boot option of SCI boot for debugging, etc)
2. Based on the number of boot modes needed, determine how many boot mode select pins (BMSPs) are required to select between your selected boot modes. (For example: 2 BMSPs are required to select between 3 boot mode options)
3. Assign the required BMSPs to a physical GPIO pin. (For example, BMSP0 to GPIO10, BMSP1 to GPIO51, and BMSP2 left as default which is disabled). Refer to [Section 7.10.1.1](#) for all the details on performing these configurations.
4. Assign the determined boot mode definitions to indexes in your custom boot table that correlate to the decoded value of the BMSPs. For example, BOOTDEF0=Boot to Flash, BOOTDEF1=CAN Boot, BOOTDEF2=SCI Boot; all other BOOTDEFx are left as default/nothing). Refer to [Section 7.10.1.2](#) for all the details on setting up and configuring the custom boot mode table.

Additionally, the *Boot Mode Example Use Cases* section of the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#) provides some example use cases on how to configure the BMSPs and custom boot tables.

Note

The CAN boot mode turns on the XTAL. Be sure an XTAL is installed in the application before using CAN boot mode.

7.10.1.1 Configuring Boot Mode Pins

This section explains how the boot mode select pins can be customized by the user, by programming the BOOTPIN-CONFIG location (refer to [Table 7-9](#)) in the user-configurable dual-zone security module (DCSM) OTP. The location in the DCSM OTP is Z1-OTP-BOOTPIN-CONFIG or Z2-OTP-BOOTPIN-CONFIG. When debugging, EMU-BOOTPIN-CONFIG is the emulation equivalent of Z1-OTP-BOOTPIN-CONFIG/Z2-OTP-BOOTPIN-CONFIG, and can be programmed to experiment with different boot modes without writing to OTP. The device can be programmed to use 0, 1, 2, or 3 boot mode select pins as needed.

Note

When using Z2-OTP-BOOTPIN-CONFIG, the configurations programmed in this location will take priority over the configurations in Z1-OTP-BOOTPIN-CONFIG. It is recommended to use Z1-OTP-BOOTPIN-CONFIG first and then if OTP configurations need to be altered, switch to using Z2-OTP-BOOTPIN-CONFIG.

Table 7-9. BOOTPIN-CONFIG Bit Fields

| BIT | NAME | DESCRIPTION |
|-------|--------------------------------|--|
| 31:24 | Key | Write 0x5A to these 8-bits to indicate the bits in this register are valid |
| 23:16 | Boot Mode Select Pin 2 (BMSP2) | Refer to BMSP0 description except for BMSP2 |
| 15:8 | Boot Mode Select Pin 1 (BMSP1) | Refer to BMSP0 description except for BMSP1 |
| 7:0 | Boot Mode Select Pin 0 (BMSP0) | Set to the GPIO pin to be used during boot (up to 255): - 0x0 = GPIO0 - 0x01 = GPIO1 - and so on Writing 0xFF disables BMSP0 and this pin is no longer used to select the boot mode. |

The following GPIOs cannot be used as a BMSP. If selected for a particular BMSP, the boot ROM automatically selects the factory default GPIO (the factory default for BMSP2 is 0xFF, which disables the BMSP).

- GPIO 20 and GPIO 21
- GPIO 36 and GPIO 38
- GPIO 62 to GPIO 223

Table 7-10. Standalone Boot Mode Select Pin Decoding

| BOOTPIN_CONFIG KEY | BMSP0 | BMSP1 | BMSP2 | REALIZED BOOT MODE |
|--------------------|--------------|--------------|--|--|
| != 0x5A | Don't Care | Don't Care | Don't Care | Boot as defined by the factory default BMSPs |
| = 0x5A | 0xFF | 0xFF | 0xFF | Boot as defined in the boot table for boot mode 0 (All BMSPs disabled) |
| | Valid GPIO | 0xFF | 0xFF | Boot as defined by the value of BMSP0 (BMSP1 and BMSP2 disabled) |
| | 0xFF | Valid GPIO | 0xFF | Boot as defined by the value of BMSP1 (BMSP0 and BMSP2 disabled) |
| | 0xFF | 0xFF | Valid GPIO | Boot as defined by the value of BMSP2 (BMSP0 and BMSP1 disabled) |
| | Valid GPIO | Valid GPIO | 0xFF | Boot as defined by the values of BMSP0 and BMSP1 (BMSP2 disabled) |
| | Valid GPIO | 0xFF | Valid GPIO | Boot as defined by the values of BMSP0 and BMSP2 (BMSP1 disabled) |
| | 0xFF | Valid GPIO | Valid GPIO | Boot as defined by the values of BMSP1 and BMSP2 (BMSP0 disabled) |
| | Valid GPIO | Valid GPIO | Valid GPIO | Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| | Invalid GPIO | Valid GPIO | Valid GPIO | BMSP0 is reset to the factory default BMSP0 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| | Valid GPIO | Invalid GPIO | Valid GPIO | BMSP1 is reset to the factory default BMSP1 GPIO Boot as defined by the values of BMSP0, BMSP1, and BMSP2 |
| Valid GPIO | Valid GPIO | Invalid GPIO | BMSP2 is reset to the factory default state, which is disabled Boot as defined by the values of BMSP0 and BMSP1 | |

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Note

When decoding the boot mode, BMSP0 is the least-significant-bit and BMSP2 is the most-significant-bit of the boot table index value. It is recommended when disabling BMSPs to start with disabling BMSP2. For example, in an instance when only using BMSP2 (BMSP1 and BMSP0 are disabled), then only the boot table indexes of 0 and 4 will be selectable. In the instance when using only BMSP0, then the selectable boot table indexes are 0 and 1.

7.10.1.2 Configuring Boot Mode Table Options

This section explains how to configure the boot definition table, BOOTDEF, for the device and the associated boot options. The 64-bit location is located in user-configurable DCSM OTP in the Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations. When debugging, EMU-BOOTDEF-LOW and EMU-BOOTDEF-HIGH are the emulation equivalents of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH, and can be programmed to experiment with different boot mode options without writing to OTP. The range of customization to the boot definition table depends on how many boot mode select pins (BMSP) are being used. For example, 0 BMSPs equals to 1 table entry, 1 BMSP equals to 2 table entries, 2 BMSPs equals to 4 table entries, and 3 BMSPs equals to 8 table entries. Refer to the [TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#) for examples on how to set up the BOOTPIN_CONFIG and BOOTDEF values.

Note

The locations Z2-OTP-BOOTDEF-LOW and Z2-OTP-BOOTDEF-HIGH will be used instead of Z1-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH locations when Z2-OTP-BOOTPIN-CONFIG is configured. Refer to [Configuring Boot Mode Pins](#) for more details on BOOTPIN_CONFIG usage.

Table 7-11. BOOTDEF Bit Fields

| BOOTDEF NAME | BYTE POSITION | NAME | DESCRIPTION |
|--------------|---------------|------------------------|---|
| BOOT_DEF0 | 7:0 | BOOT_DEF0 Mode/Options | Set the boot mode for index 0 of the boot table. Different boot modes and their options can include, for example, a boot mode that uses different GPIOs for a specific bootloader or a different flash entry point address. Any unsupported boot mode will cause the device to either go to wait boot or boot to flash. Refer to GPIO Assignments for valid BOOTDEF values to set in the table. |
| BOOT_DEF1 | 15:8 | BOOT_DEF1 Mode/Options | Refer to BOOT_DEF0 description |
| BOOT_DEF2 | 23:16 | BOOT_DEF2 Mode/Options | |
| BOOT_DEF3 | 31:24 | BOOT_DEF3 Mode/Options | |
| BOOT_DEF4 | 39:32 | BOOT_DEF4 Mode/Options | |
| BOOT_DEF5 | 47:40 | BOOT_DEF5 Mode/Options | |
| BOOT_DEF6 | 55:48 | BOOT_DEF6 Mode/Options | |
| BOOT_DEF7 | 63:56 | BOOT_DEF7 Mode/Options | |

7.10.2 GPIO Assignments

This section details the GPIOs and boot option values used for boot mode set in the BOOT_DEF memory location located at Z1-OTP-BOOTDEF-LOW/ Z2-OTP-BOOTDEF-LOW and Z1-OTP-BOOTDEF-HIGH/ Z2-OTP-BOOTDEF-HIGH. Refer to [Configuring Boot Mode Table Options](#) on how to configure BOOT_DEF. When selecting a boot mode option, make sure to verify that the necessary pins are available in the pin mux options for the specific device package being used.

Table 7-12. SCI Boot Options

| OPTION | BOOTDEF VALUE | SCITXDA GPIO | SCIRXDA GPIO |
|-------------|---------------|--------------|--------------|
| 0 (default) | 0x01 | GPIO29 | GPIO28 |
| 1 | 0x21 | GPIO16 | GPIO17 |
| 2 | 0x41 | GPIO8 | GPIO9 |
| 3 | 0x61 | GPIO2 | GPIO3 |
| 4 | 0x81 | GPIO16 | GPIO3 |

Table 7-13. MCAN Boot Options

| OPTION | BOOTDEF VALUE | CANTXA GPIO | CANRXA GPIO |
|-------------|---------------|-------------|-------------|
| 0 (default) | 0x08 | GPIO4 | GPIO5 |
| 1 | 0x28 | GPIO1 | GPIO0 |
| 2 | 0x48 | GPIO13 | GPIO12 |

Table 7-14. CAN(MCAN in non-FD mode) Boot Options

| OPTION | BOOTDEF VALUE | CANTXA GPIO | CANRXA GPIO |
|-------------|---------------|-------------|-------------|
| 0 (default) | 0x02 | GPIO4 | GPIO5 |
| 1 | 0x22 | GPIO1 | GPIO0 |
| 2 | 0x42 | GPIO13 | GPIO12 |

Table 7-15. I2C Boot Options

| OPTION | BOOTDEF VALUE | SDAA GPIO | SCLA GPIO |
|--------|---------------|-----------|-----------|
| 0 | 0x07 | GPIO0 | GPIO1 |
| 1 | 0x27 | GPIO32 | GPIO33 |
| 2 | 0x47 | GPIO5 | GPIO4 |

Table 7-16. RAM Boot Options

| OPTION | BOOTDEF VALUE | RAM ENTRY POINT (ADDRESS) |
|--------|---------------|---------------------------|
| 0 | 0x05 | 0x0000 0000 |

Table 7-17. Flash/Secure Flash Boot Options

| OPTION | BOOTDEF VALUE | FLASH ENTRY POINT (ADDRESS) | FLASH SECTOR |
|-------------|---------------|-----------------------------|-------------------|
| 0 (default) | 0x03 | 0x0008 0000 | Bank0 Sector 0 |
| 1 | 0x23 | 0x0008 8000 | Bank 0 Sector 32 |
| 2 | 0x43 | 0x000C 0000 | Bank 2 Sector 0 |
| 3 | 0x63 | 0x000C 8000 | Bank 2, Sector 32 |
| 4 | 0x83 | 0x0010 0000 | Bank 4, Sector 0 |

Table 7-18. LFU Flash Boot Options

| OPTION | BOOTDEF VALUE | FLASH ENTRY POINT (ADDRESS) | BANK |
|-------------|---------------|-----------------------------|-------|
| 0 (default) | 0x0B | 0x0008 0000 | Bank0 |
| | | 0x000C 0000 | Bank2 |
| 1 | 0x2B | 0x0008 8000 | Bank0 |
| | | 0x000C 8000 | Bank2 |

Table 7-19. Wait Boot Options

| OPTION | BOOTDEF VALUE | WATCHDOG |
|--------|---------------|----------|
| 0 | 0x04 | Enabled |
| 1 | 0x24 | Disabled |

Table 7-20. SPI Boot Options

| OPTION | BOOTDEF VALUE | SPIPCOA | SPIPOCIA | SPICLKA | SPISPTE |
|--------|---------------|---------|----------|---------|---------|
| 0 | 0x06 | GPIO2 | GPIO1 | GPIO3 | GPIO5 |
| 1 | 0x26 | GPIO16 | GPIO1 | GPIO3 | GPIO0 |
| 2 | 0x46 | GPIO8 | GPIO10 | GPIO9 | GPIO11 |
| 3 | 0x66 | GPIO8 | GPIO17 | GPIO9 | GPIO11 |

Table 7-21. Parallel Boot Options

| OPTION | BOOTDEF VALUE | D0-D7 GPIO | 28x(DSP) CONTROL GPIO | HOST CONTROL GPIO |
|-------------|---------------|------------|-----------------------|-------------------|
| 0 (default) | 0x00 | D0 - GPIO0 | GPIO16 | GPIO29 |
| | | D1 - GPIO1 | | |
| | | D2 - GPIO2 | | |
| | | D3 - GPIO3 | | |
| | | D4 - GPIO4 | | |
| | | D5 - GPIO5 | | |
| | | D6 - GPIO6 | | |
| | | D7 - GPIO7 | | |
| 1 | 0x20 | D0 - GPIO0 | GPIO12 | GPIO13 |
| | | D1 - GPIO1 | | |
| | | D2 - GPIO2 | | |
| | | D3 - GPIO3 | | |
| | | D4 - GPIO4 | | |
| | | D5 - GPIO5 | | |
| | | D6 - GPIO6 | | |
| | | D7 - GPIO7 | | |

Table 7-22. USB Boot Options

| OPTION | BOOTDEF VALUE | USB0 DM | USB0 DP |
|-------------|---------------|---------|---------|
| 0 (default) | 0x09 | GPIO23 | GPIO41 |

7.11 Security

Security features are enforced by the Dual Code Security Module (DCSM). The primary layer of defense is securing the boundary of the chip, which should always be enabled. Additionally, the Dual Zone Security feature is available to support code partitioning.

7.11.1 Securing the Boundary of the Chip

The following two features, along with authentication in the firmware update code, should be used to help to prevent unauthorized code from running on the device.

7.11.1.1 JTAGLOCK

Enabling the JTAGLOCK feature in the USER OTP disables JTAG access (for example, debug probe) to resources on the device.

7.11.1.2 Zero-pin Boot

Enabling the Zero-pin Boot option along with Flash Boot in the USER OTP blocks all pin-based external bootloader options (for example, SCI, CAN, Parallel).

7.11.2 Dual-Zone Security

The dual-zone security mechanism offers protection for two zones: Zone 1 (Z1) and Zone 2 (Z2). The security implementation for both zones is identical. Each zone has its own dedicated secure resource (OTP memory and secure ROM) and allocated secure resource (LSx RAM and flash sectors).

7.11.3 Disclaimer

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

IN NO EVENT SHALL TI BE LIABLE FOR ANY CONSEQUENTIAL, SPECIAL, INDIRECT, INCIDENTAL, OR PUNITIVE DAMAGES, HOWEVER CAUSED, ARISING IN ANY WAY OUT OF YOUR USE OF THE CSM OR THIS DEVICE, WHETHER OR NOT TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. EXCLUDED DAMAGES INCLUDE, BUT ARE NOT LIMITED TO LOSS OF DATA, LOSS OF GOODWILL, LOSS OF USE OR INTERRUPTION OF BUSINESS OR OTHER ECONOMIC LOSS.

7.12 Watchdog

The watchdog module is the same as the one on previous TMS320C2000™ microcontrollers, but with an optional lower limit on the time between software resets of the counter. This windowed countdown is disabled by default, so the watchdog is fully backward-compatible.

The watchdog generates either a reset or an interrupt. It is clocked from the internal oscillator with a selectable frequency divider.

Figure 7-4 shows the various functional blocks within the watchdog module.

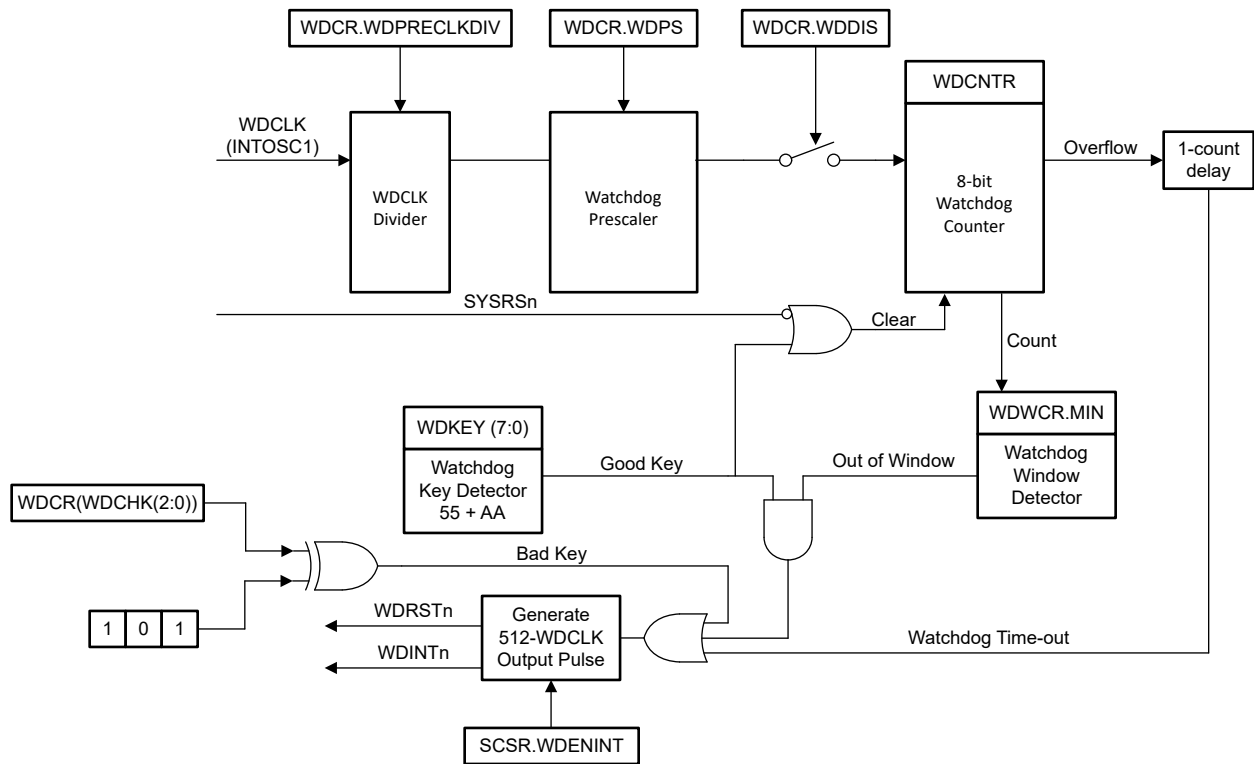


Figure 7-4. Windowed Watchdog

7.13 C28x Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presetable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register that generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and is connected to INT13 of the CPU. CPU-Timer 2 is reserved for TI-RTOS. It is connected to INT14 of the CPU. If TI-RTOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLK (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTOSC2)
- X1 (XTAL)

7.14 Dual-Clock Comparator (DCC)

The DCC module is used for evaluating and monitoring the clock input based on a second clock, which can be a more accurate and reliable version. This instrumentation is used to detect faults in clock source or clock structures, thereby enhancing the system's safety metrics.

7.14.1 Features

The DCC has the following features:

- Allows the application to ensure that a fixed ratio is maintained between frequencies of two clock signals.
- Supports the definition of a programmable tolerance window in terms of the number of reference clock cycles.
- Supports continuous monitoring without requiring application intervention.
- Supports a single-sequence mode for spot measurements.
- Allows the selection of a clock source for each of the counters, resulting in several specific use cases.

7.14.2 Mapping of DCCx Clock Source Inputs

Table 7-23. DCCx Clock Source0 Table

| DCCxCLKSRC0[3:0] | CLOCK NAME |
|------------------|-------------------------------------|
| 0x0 | XTAL/X1 |
| 0x1 | INTOSC1 |
| 0x2 | INTOSC2 |
| 0x4 | TCK |
| 0x5 | CPU1.SYSCLK |
| 0x8 | AUXCLKIN |
| 0xC | INPUT XBAR (Output16 of input-xbar) |
| others | Reserved |

Table 7-24. DCCx Clock Source1 Table

| DCCxCLKSRC1[4:0] | CLOCK NAME |
|------------------|---|
| 0x0 | PLLRAWCLK |
| 0x2 | INTOSC1 |
| 0x3 | INTOSC2 |
| 0x6 | CPU1.SYSCLK |
| 0x9 | Input XBAR (Output15 of the input-xbar) |
| 0xA | AUXCLKIN |
| 0xB | EPWMCLK |
| 0xC | LSPCLK |
| 0xD | ADCCLK |
| 0xE | WDCLK |
| 0xF | CAN0BITCLK |
| others | Reserved |

7.15 Configurable Logic Block (CLB)

The C2000 configurable logic block (CLB) is a collection of blocks that can be interconnected using software to implement custom digital logic functions or enhance existing on-chip peripherals. The CLB is able to enhance existing peripherals through a set of crossbar interconnections, which provide a high level of connectivity to existing control peripherals such as enhanced pulse width modulators (ePWM), enhanced capture modules (eCAP), and enhanced quadrature encoder pulse modules (eQEP). The crossbars also allow the CLB to be connected to external GPIO pins. In this way, the CLB can be configured to interact with device peripherals to perform small logical functions such as comparators, or to implement custom serial data exchange protocols. Through the CLB, functions that would otherwise be accomplished using external logic devices can now be implemented inside the MCU.

The CLB peripheral is configured through the CLB tool. For more information on the CLB tool, available examples, application reports and users guide, please refer to the following location in your [C2000Ware for C2000 MCUs](#) package (C2000Ware_2_00_00_03 and higher):

- [C2000WARE_INSTALL_LOCATION\utilities\clb_tool\clb_syscfg\doc](#)
- [CLB Tool User's Guide](#)
- [Designing With the C2000™ Configurable Logic Block \(CLB\) Application Report](#)
- [How to Migrate Custom Logic From an FPGA/CPLD to C2000™ Microcontrollers Application Report](#)

The CLB module and its interconnections are shown in [Figure 7-5](#).

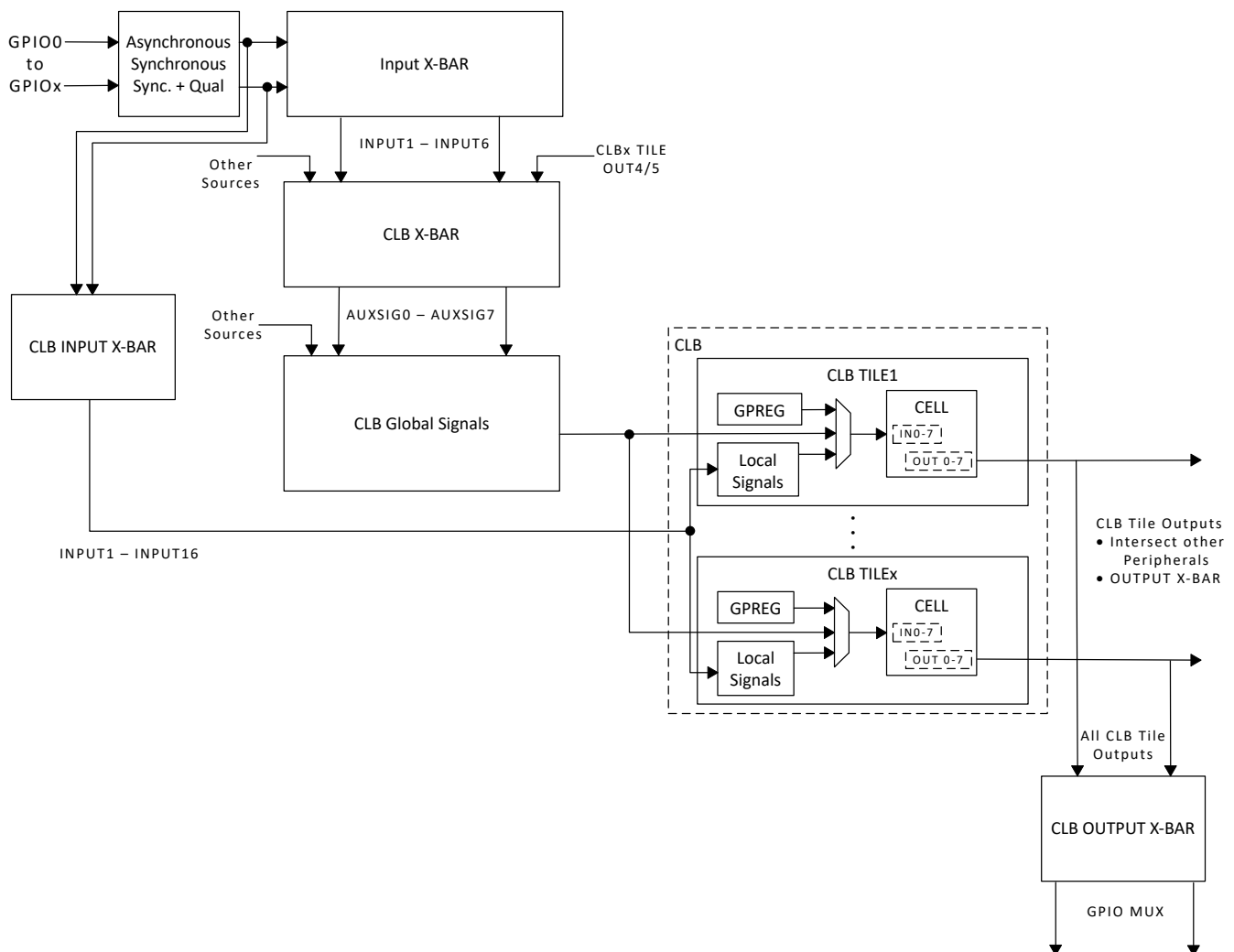


Figure 7-5. GPIO to CLB Tile Connections

Absolute encoder protocol interfaces are now provided as [Position Manager](#) solutions in the C2000Ware MotorControl SDK. Configuration files, application programmer interface (API), and use examples for such solutions are provided with [C2000Ware MotorControl SDK](#). In some solutions, the TI-configured CLB is used with other on-chip resources, such as the SPI port or the C28x CPU, to perform more complex functionality.

8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

The [Hardware Design Guide for F2800x C2000™ Real-Time MCU Series Application Note](#) is an essential guide for hardware developers using C2000 devices, and helps to streamline the design process while mitigating the potential for faulty designs. Key topics discussed include: power requirements; general-purpose input/output (GPIO) connections; analog inputs and ADC; clocking generation and requirements; and JTAG debugging among many others.

8.1 TI Reference Design

The TI Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all reference designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

Search and download TI reference designs at [Select TI reference designs](#).

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MCU devices and support tools. Each TMS320™ MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS320F28P559SJ-Q1**). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMX and TMDX) through fully qualified production devices and tools (TMS and TMDS).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

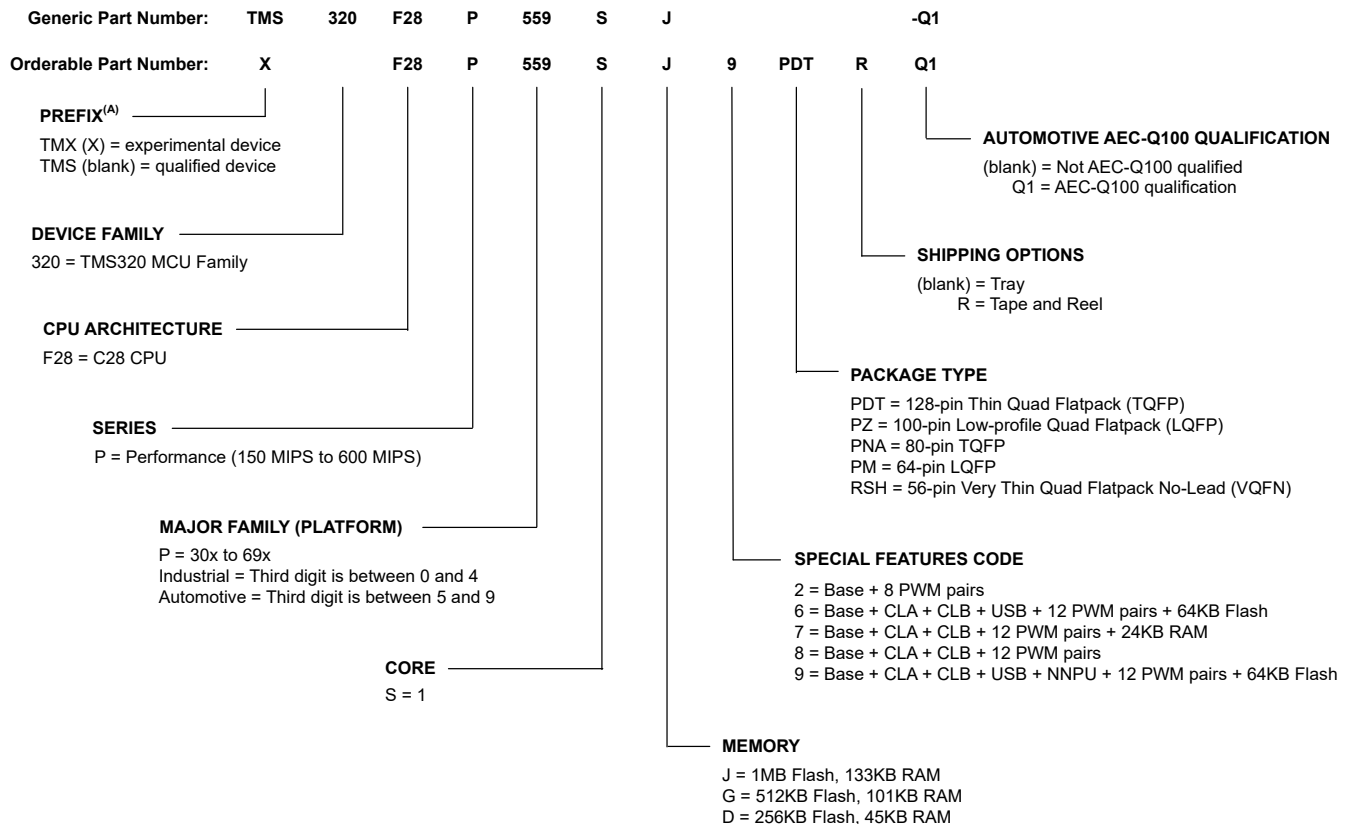
"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZ).

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.



A. Prefix X is used in orderable part numbers.

Figure 9-1. Device Nomenclature

9.2 Markings

Figure 9-2, Figure 9-3, Figure 9-4, Figure 9-5, Figure 9-6, Figure 9-7, Figure 9-8, and Figure 9-9 show the package symbolization. Table 9-1 lists the silicon revision codes.

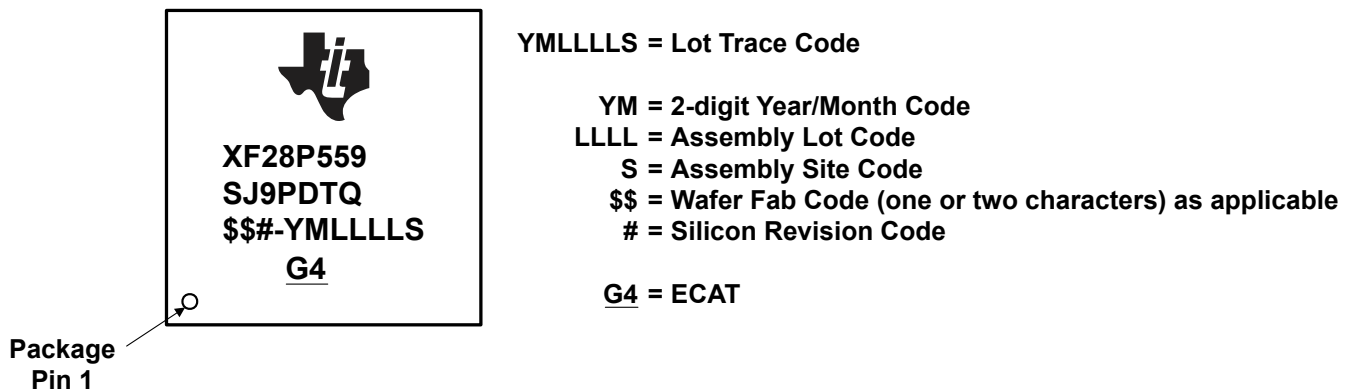
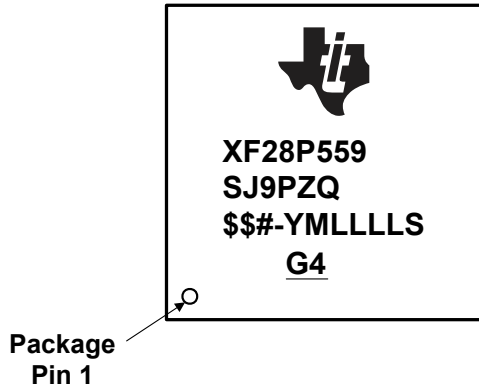


Figure 9-2. Package Symbolization for PDT Package – Automotive

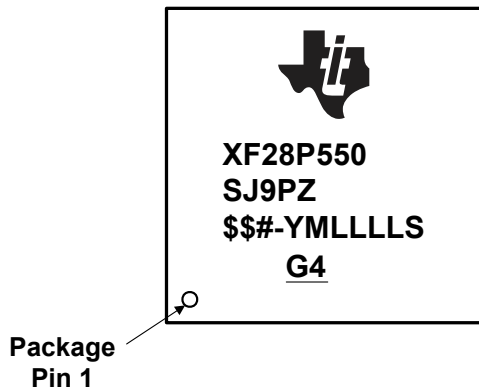


YMLLLLS = Lot Trace Code

- YM = 2-digit Year/Month Code**
- LLLL = Assembly Lot Code**
- S = Assembly Site Code**
- \$\$ = Wafer Fab Code (one or two characters) as applicable**
- # = Silicon Revision Code**

G4 = ECAT

Figure 9-3. Package Symbolization for PZ Package – Automotive

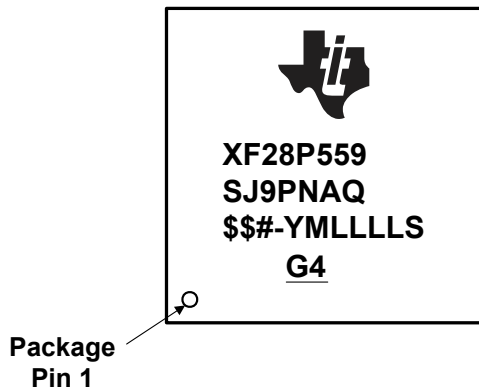


YMLLLLS = Lot Trace Code

- YM = 2-digit Year/Month Code**
- LLLL = Assembly Lot Code**
- S = Assembly Site Code**
- \$\$ = Wafer Fab Code (one or two characters) as applicable**
- # = Silicon Revision Code**

G4 = ECAT

Figure 9-4. Package Symbolization for PZ Package – Non-Automotive



YMLLLLS = Lot Trace Code

- YM = 2-digit Year/Month Code**
- LLLL = Assembly Lot Code**
- S = Assembly Site Code**
- \$\$ = Wafer Fab Code (one or two characters) as applicable**
- # = Silicon Revision Code**

G4 = ECAT

Figure 9-5. Package Symbolization for PNA Package – Automotive

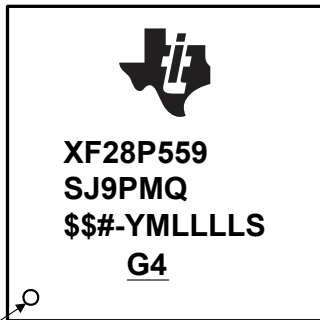


YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
\$\$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = ECAT

Figure 9-6. Package Symbolization for PNA Package – Non-Automotive

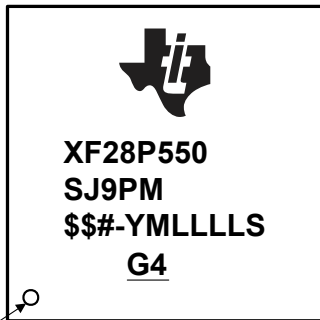


YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
\$\$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = ECAT

Figure 9-7. Package Symbolization for PM Package – Automotive



YMLLLLS = Lot Trace Code

YM = 2-digit Year/Month Code
LLLL = Assembly Lot Code
S = Assembly Site Code
\$\$ = Wafer Fab Code (one or two characters) as applicable
= Silicon Revision Code

G4 = ECAT

Figure 9-8. Package Symbolization for PM Package – Non-Automotive

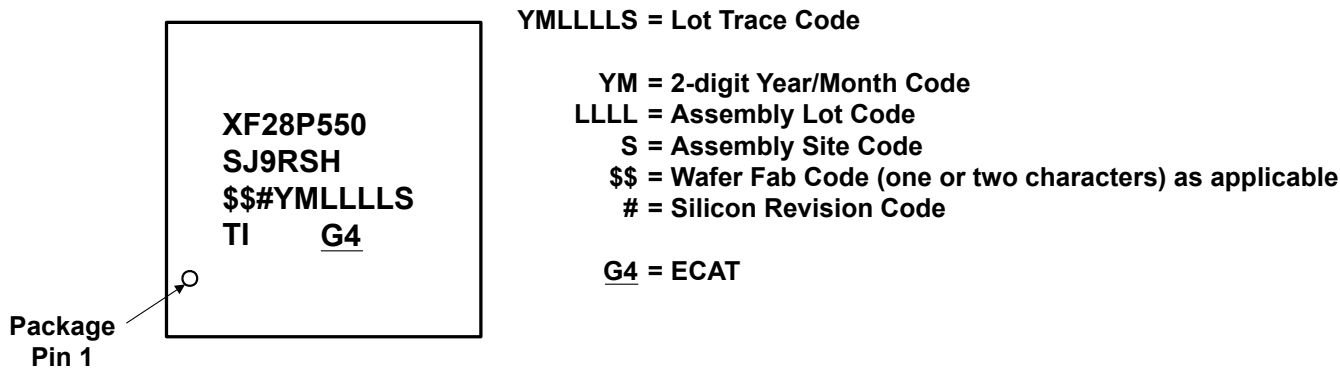


Figure 9-9. Package Symbolization for RSH Package – Non-Automotive

Table 9-1. Revision Identification

| SILICON REVISION CODE | SILICON REVISION | REVID ⁽¹⁾ ADDRESS: 0x5D00C | COMMENTS |
|-----------------------|------------------|--|--|
| Blank | 0 | 0x0000 0000 | This silicon revision is available as TMX. |

(1) Silicon Revision ID

9.3 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions follow. To view all available tools and software for C2000™ real-time control MCUs, visit the [C2000 real-time control MCUs – Design & development](#) page.

Development Tools

[TI Resource Explorer](#)

To enhance your experience, be sure to check out the TI Resource Explorer to browse examples, libraries, and documentation for your applications.

Software Tools

[C2000Ware for C2000 MCUs](#)

C2000Ware for C2000™ MCUs is a cohesive set of software and documentation created to minimize development time. It includes device-specific drivers, libraries, and peripheral examples.

[DigitalPower SDK](#)

DigitalPower SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based digital power system development time targeted for various AC-DC, DC-DC and DC-AC power supply applications. The software includes firmware that runs on C2000 digital power evaluation modules (EVMs) and TI designs (TIDs), which are targeted for solar, telecom, server, electric vehicle chargers and industrial power delivery applications. DigitalPower SDK provides all the needed resources at every stage of development and evaluation in a digital power applications.

[MotorControl SDK](#)

MotorControl SDK is a cohesive set of software infrastructure, tools, and documentation designed to minimize C2000 MCU-based motor control system development time targeted for various three-phase motor control applications. The software includes firmware that runs on C2000 motor control evaluation modules (EVMs) and TI designs (TIDs), which are targeted for industrial drive and other motor control, MotorControl SDK provides all the needed resources at every stage of development and evaluation for high-performance motor control applications.

[Code Composer Studio™ integrated development environment \(IDE\)](#)

Code Composer Studio is an integrated development environment (IDE) for TI's microcontrollers and processors. It comprises a suite of tools used to develop and debug embedded applications. Code Composer Studio is available for download across Windows®, Linux® and macOS® desktops. It can also be used in

the cloud by visiting <https://dev.ti.com>. Code Composer Studio includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler and many other features. The intuitive IDE takes you through each step of the application development flow. Familiar tools and interfaces make getting started faster than ever before. The desktop version of Code Composer Studio combines the advantages of the Eclipse software framework with advanced capabilities from TI resulting in a compelling feature-rich environment. The cloud-based Code Composer Studio leverages the Theia application framework enabling development in the cloud without needing to download and install large amounts of software.

[SysConfig System configuration tool](#)

SysConfig is a comprehensive collection of graphical utilities for configuring pins, peripherals, radios, subsystems, and other components. SysConfig helps you manage, expose and resolve conflicts visually so that you have more time to create differentiated applications. The tool's output includes C header and code files that can be used with software development kit (SDK) examples or used to configure custom software. The SysConfig tool automatically selects the pinmux settings that satisfy the entered requirements. The SysConfig tool is delivered integrated in CCS, as a standalone installer, or can be used via the dev.ti.com cloud tools portal. For more information about the SysConfig system configuration tool, visit the [System configuration tool](#) page.

[C2000 Third-party search tool](#)

TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

[UniFlash Standalone Flash Tool](#)

UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

Models

Various models are available for download from the product Design & development pages. These models include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the *Design tools & simulation* section of the *Design & development* page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the [C2000™ real-time control MCUs – Support & training](#) site.

9.4 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral follows.

Note

TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.

Errata

[TMS320F28P55x Real-Time MCUs Silicon Errata](#) describes known advisories on silicon and provides workarounds.

Technical Reference Manual

[TMS320F28P55x Real-Time Microcontrollers Technical Reference Manual](#) details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the F28P55x real-time microcontrollers.

CPU User's Guides

[TMS320C28x CPU and Instruction Set Reference Guide](#) describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This Reference Guide also describes emulation features available on these DSPs.

[TMS320C28x Extended Instruction Sets Technical Reference Manual](#) describes the architecture, pipeline, and instruction set of the TMU, VCU-II, and FPU accelerators.

Peripheral Guides

[C2000 Real-Time Control Peripherals Reference Guide](#) describes the peripheral reference guides of the 28x DSPs.

Tools Guides

[TMS320C28x Assembly Language Tools v22.6.0.LTS User's Guide](#) describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

[TMS320C28x Optimizing C/C++ Compiler v22.6.0.LTS User's Guide](#) describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

The [SMT & packaging application notes](#) website lists documentation on TI's surface mount technology (SMT) and application notes on a variety of packaging-related topics.

[Semiconductor Packing Methodology](#) describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

[Calculating Useful Lifetimes of Embedded Processors](#) provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

[An Introduction to IBIS \(I/O Buffer Information Specification\) Modeling](#) discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures, and future trends.

[Serial Flash Programming of C2000™ Microcontrollers](#) discusses using a flash kernel and ROM loaders for serial programming a device.

[The Essential Guide for Developing With C2000™ Real-Time Microcontrollers](#) provides a deeper look into the components that differentiate the C2000 Microcontroller Unit (MCU) as it pertains to Real-Time Control Systems.

9.5 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

9.6 Trademarks

C2000™, TMS320C2000™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments. Windows® is a registered trademark of Microsoft Corporation. Linux® is a registered trademark of Linus Torvalds. macOS® is a registered trademark of Apple Inc. All trademarks are the property of their respective owners.

9.7 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.8 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

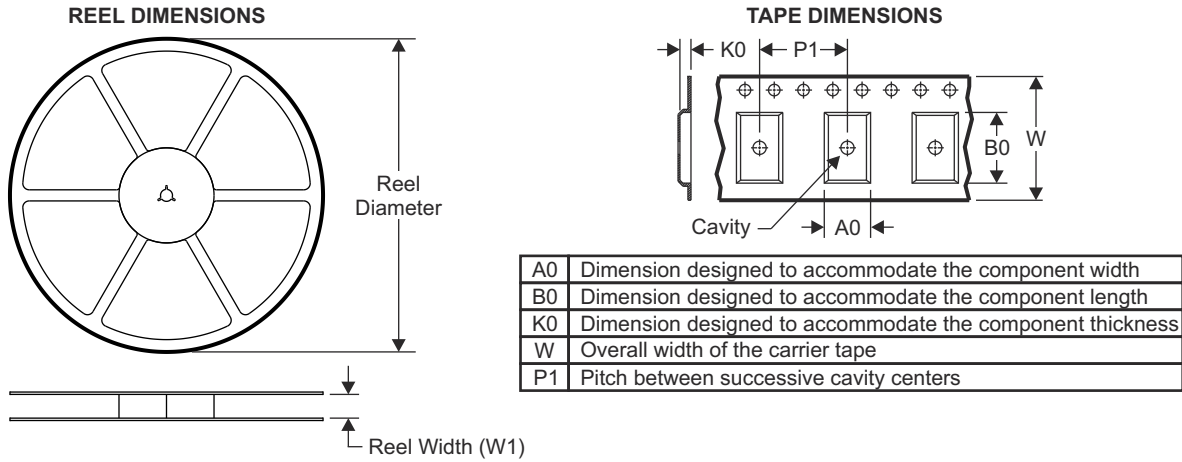
10 Revision History

| DATE | REVISION | NOTES |
|------------|----------|--|
| April 2024 | * | <p>Initial Release</p> <p>TI is transitioning to use more inclusive terminology. Some language may be different than what you would expect to see for certain technology areas.</p> <p>For SPI, all instances of legacy terminology have been changed to controller and peripheral. All instances of legacy pin names have been changed to: POCI (Peripheral OUT Controller IN); PICO (Peripheral IN Controller OUT); and CS (Chip Select).</p> <p>For the I2C Bus Interface, all instances of legacy terminology have been changed to controller and target.</p> <p>For the CAN and LIN Interface/BUS, all instances of legacy terminology have been changed to commander and responder.</p> <p>For the EtherCAT Controller, all instances of legacy terminology have been changed to MainDevice (or MDevice) and SubordinateDevice (or SubDevice).</p> |

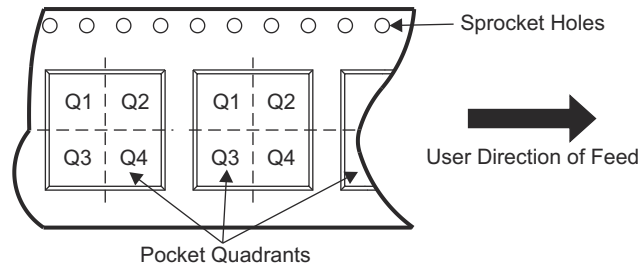
11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

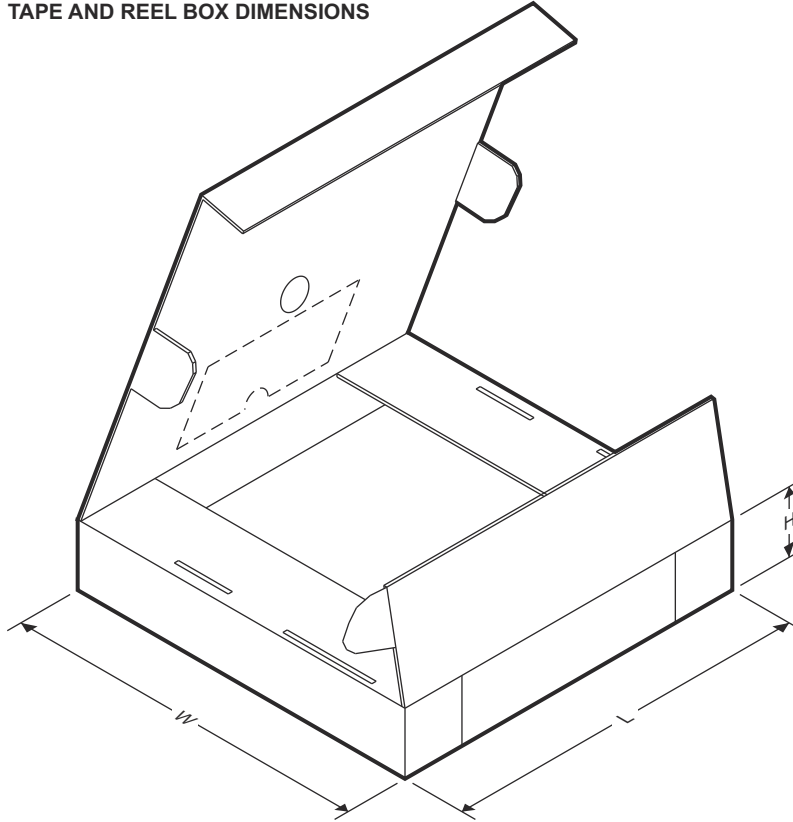


All dimensions are nominal.

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| XF28P550SJ6RSHR | VQFN | RSH | 56 | 4000 | 330.0 | 16.4 | 7.3 | 7.3 | 1.1 | 12.0 | 16.0 | Q2 |
| XF28P559SJ6PMRQ1 | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| XF28P550SJ6PMR | LQFP | PM | 64 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| XF28P550SJ6PNARQ1 | TQFP | PNA | 80 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| XF28P550SJ6PNAR | TQFP | PNA | 80 | 1000 | 330.0 | 24.4 | 13.0 | 13.0 | 2.1 | 16.0 | 24.0 | Q2 |
| XF28P550SJ6PZRQ1 | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| XF28P550SJ6PZR | LQFP | PZ | 100 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| XF28P559SJ6PDTRQ1 | TQFP | PDT | 128 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |
| XF28P550SJ6PDTR | TQFP | PDT | 128 | 1000 | 330.0 | 32.4 | 16.9 | 16.9 | 2.0 | 24.0 | 32.0 | Q2 |

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS

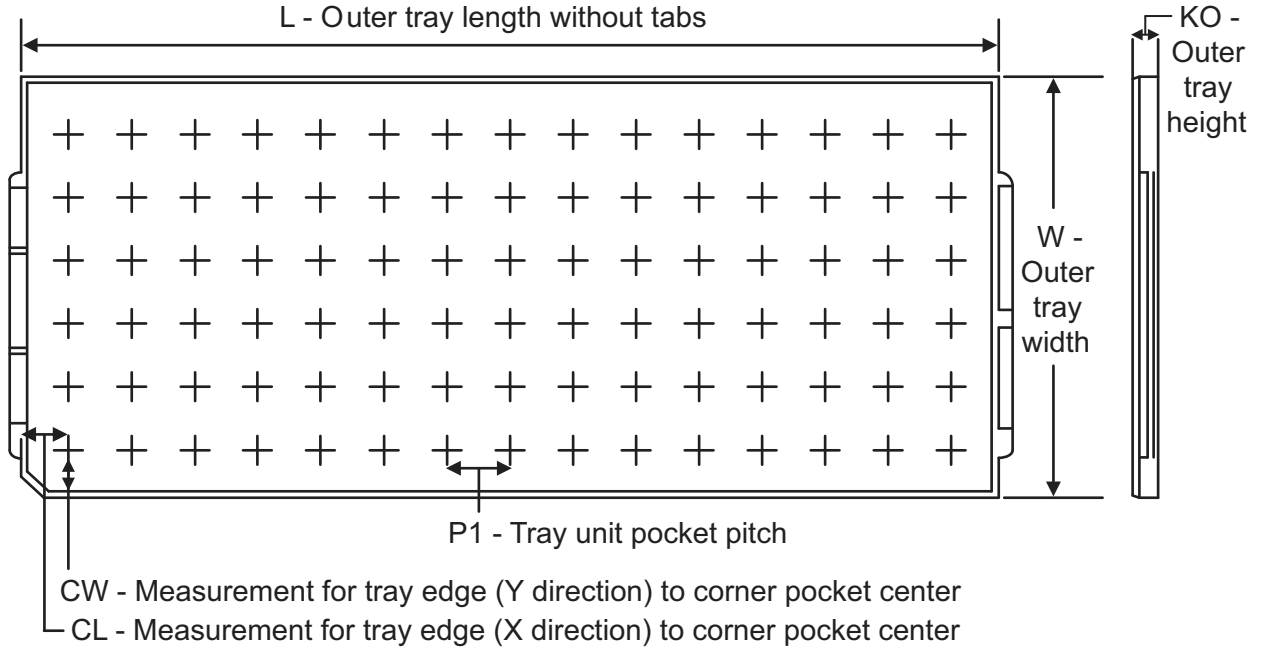


All dimensions are nominal.

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| XF28P550SJ6RSHR | VQFN | RSH | 56 | 4000 | 367.0 | 367.0 | 35.0 |
| XF28P559SJ6PMRQ1 | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| XF28P550SJ6PMR | LQFP | PM | 64 | 1000 | 336.6 | 336.6 | 41.3 |
| XF28P559SJ6PNARQ1 | TQFP | PNA | 80 | 1000 | 336.6 | 336.6 | 41.3 |
| XF28P550SJ6PNAR | TQFP | PNA | 80 | 1000 | 336.6 | 336.6 | 41.3 |
| XF28P559SJ6PZRQ1 | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| XF28P550SJ6PZR | LQFP | PZ | 100 | 1000 | 367.0 | 367.0 | 55.0 |
| XF28P559SJ6PDTRQ1 | TQFP | PDT | 128 | 1000 | 367.0 | 367.0 | 55.0 |
| XF28P550SJ6PDTR | TQFP | PDT | 128 | 1000 | 367.0 | 367.0 | 55.0 |

ADVANCE INFORMATION

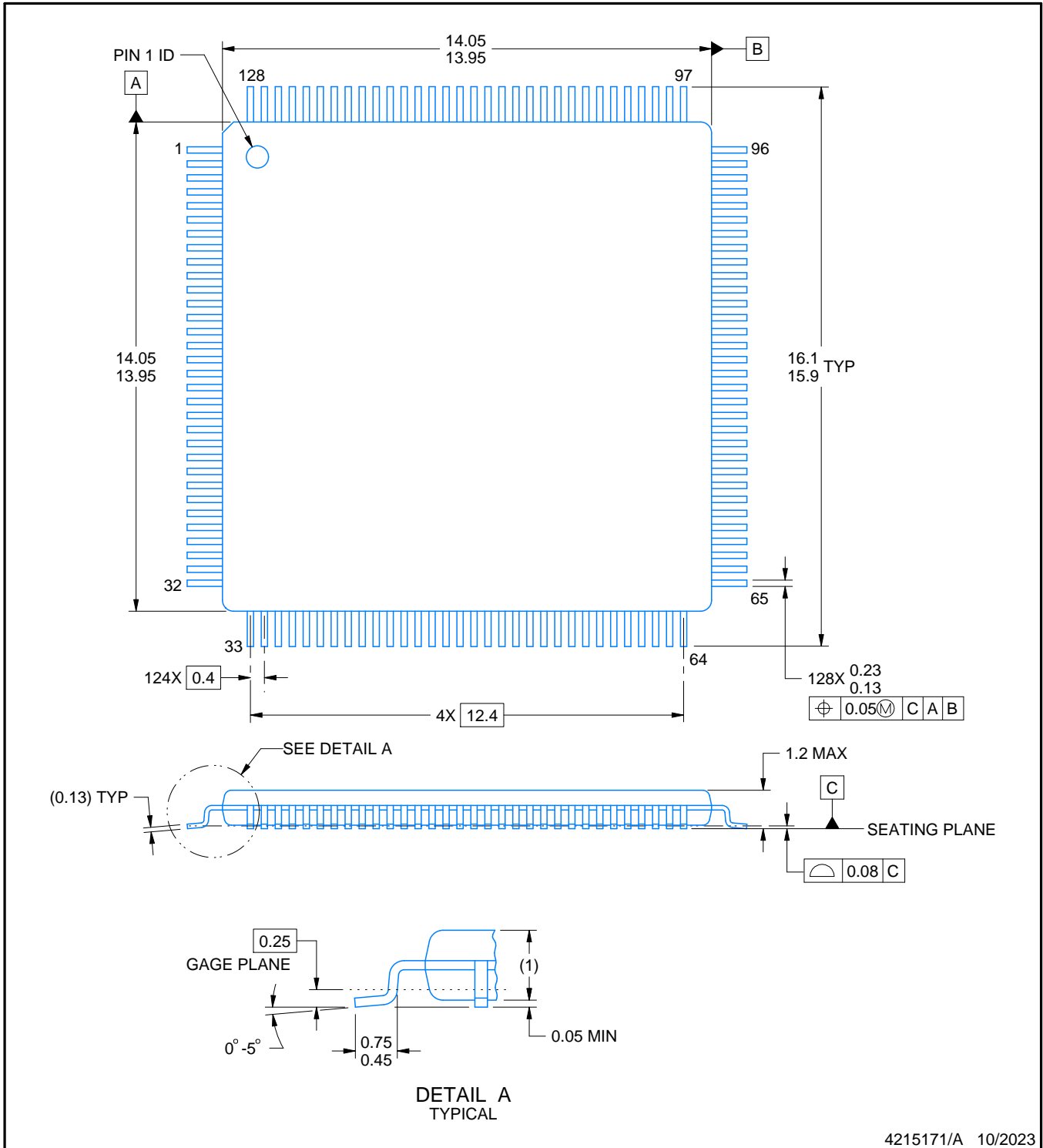
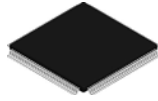
TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

All dimensions are nominal.

| Device | Package Type | Package Name | Pins | SPQ | Unit Array Matrix | Max Temp. (Deg C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|------------------|--------------|--------------|------|-----|-------------------|-------------------|--------|--------|---------|---------|---------|---------|
| XF28P550SJ9PDT | TQFP | PDT | 128 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XF28P559SJ9PDTQ1 | TQFP | PDT | 128 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 15.4 | 20.3 | 21 |
| XF28P550SJ9PZ | LQFP | PZ | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |
| XF28P559SJ9PZQ1 | LQFP | PZ | 100 | 90 | 6 x 15 | 150 | 315 | 135.9 | 7620 | 20.3 | 15.4 | 15.4 |
| XF28P550SJ9PNA | TQFP | PNA | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| XF28P559SJ9PNAQ1 | TQFP | PNA | 80 | 119 | 7 x 17 | 150 | 315 | 135.9 | 7620 | 17.9 | 14.3 | 13.95 |
| XF28P550SJ9PM | LQFP | PM | 64 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| XF28P559SJ9PMQ1 | LQFP | PM | 64 | 160 | 8 x 20 | 150 | 315 | 135.9 | 7620 | 15.2 | 13.1 | 13 |
| XF28P550SJ9RSH | VQFN | RSH | 56 | 260 | 10 x 26 | 150 | 315 | 135.9 | 7620 | 11.8 | 10 | 10.35 |



NOTES:

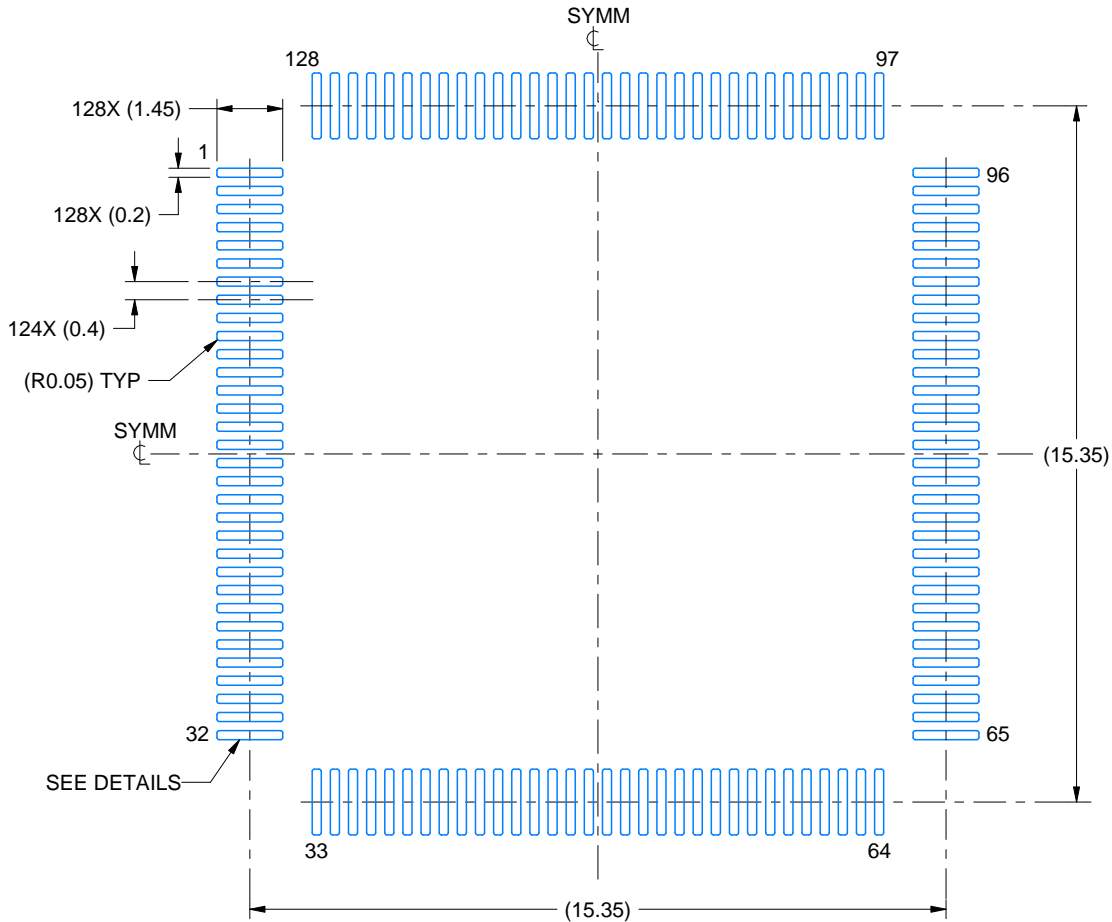
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

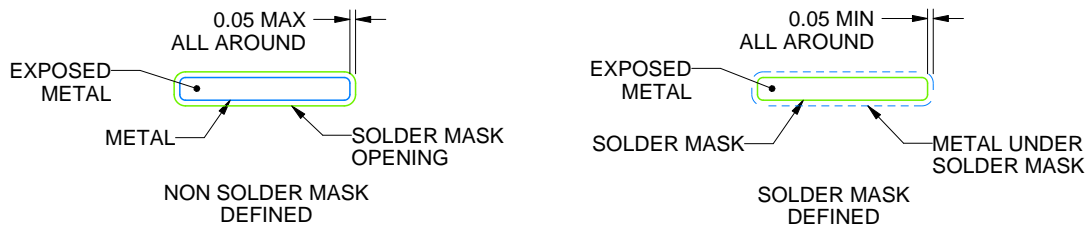
PDT0128A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

4215171/A 10/2023

NOTES: (continued)

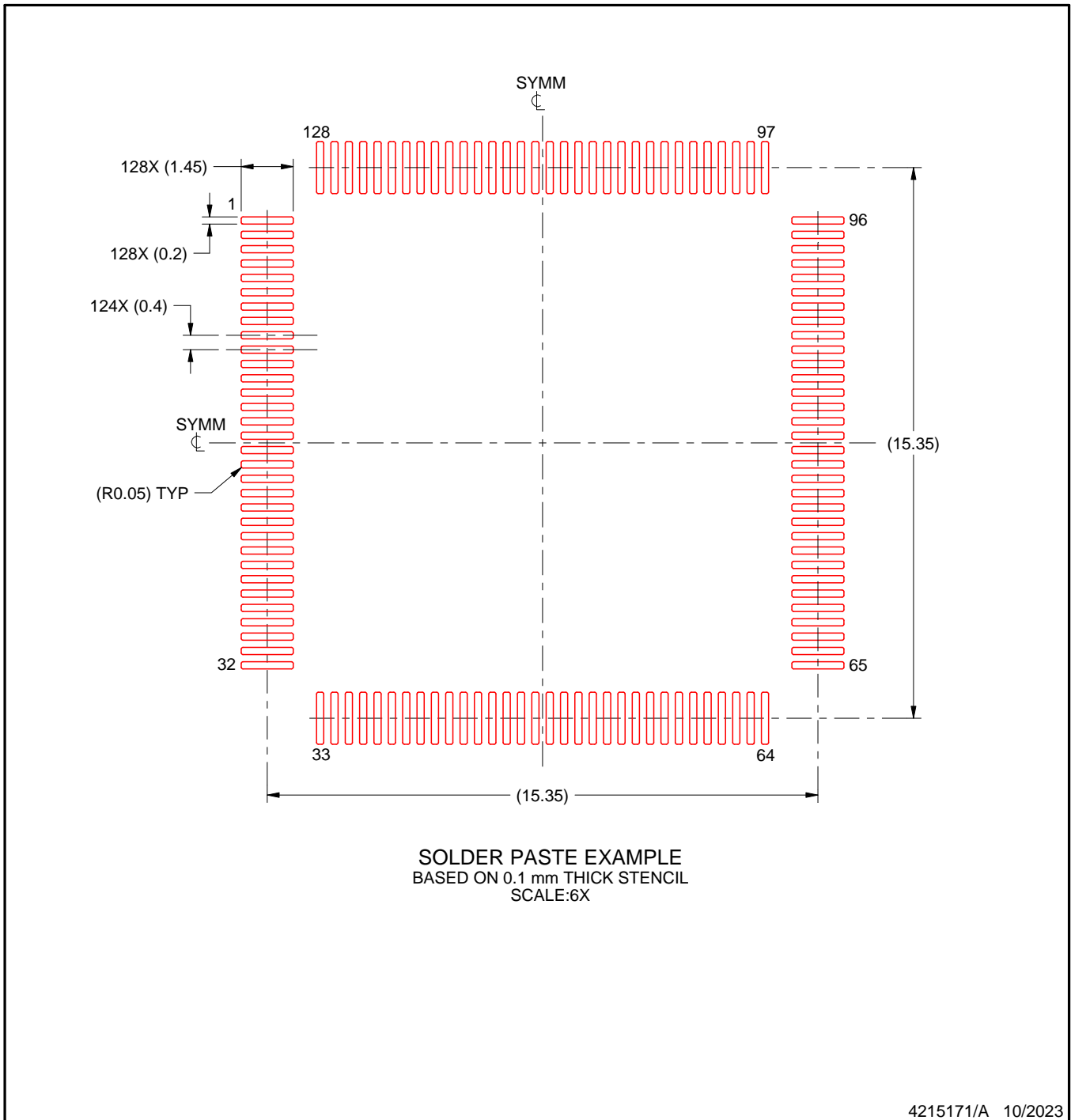
3. Publication IPC-7351 may have alternate designs.
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
5. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PDT0128A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PZ (S-PQFP-G100)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

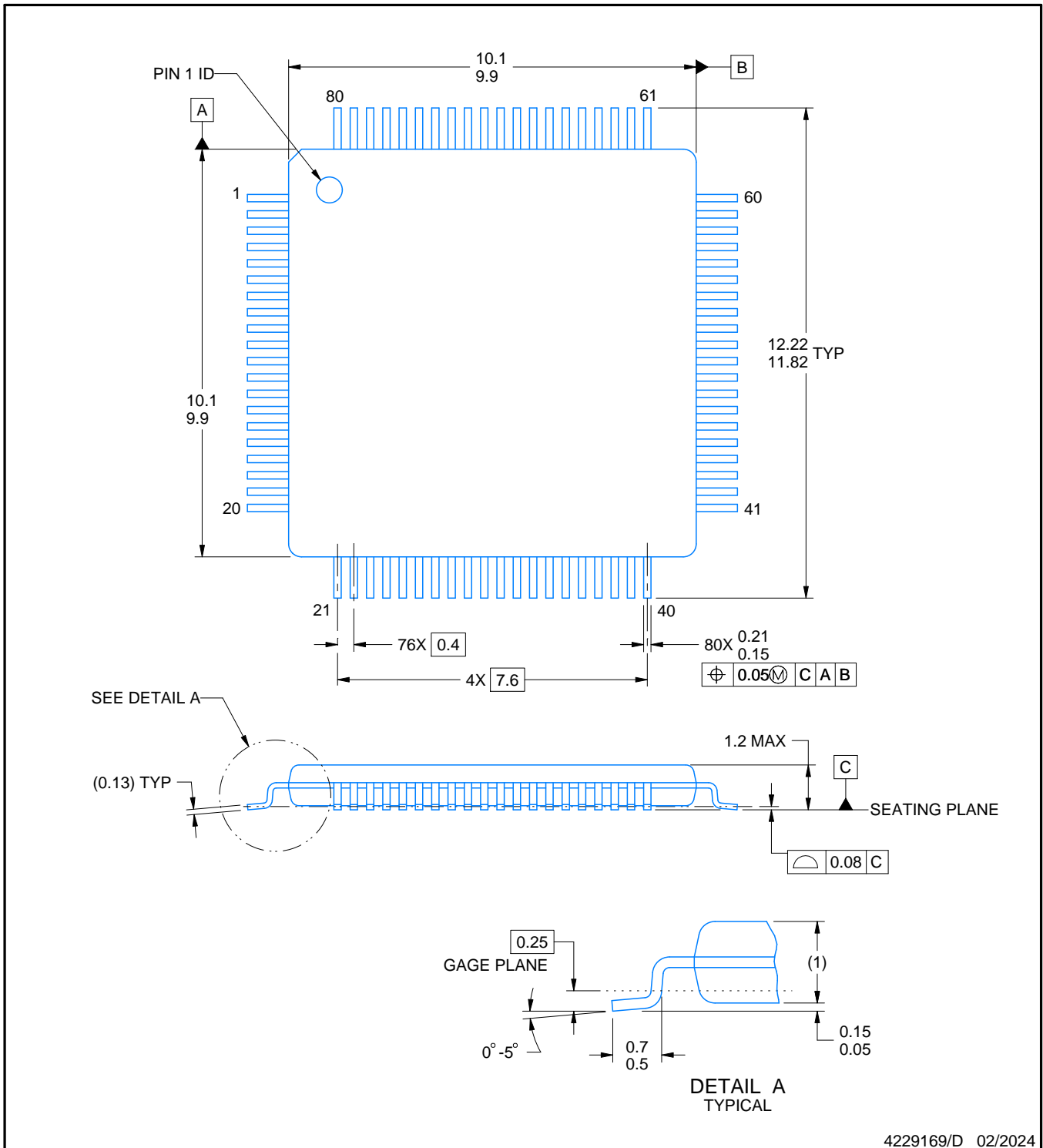
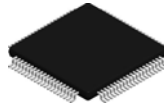
PZ (S-PQFP-G100)

PLASTIC QUAD FLAT PACK



NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4229169/D 02/2024

NOTES:

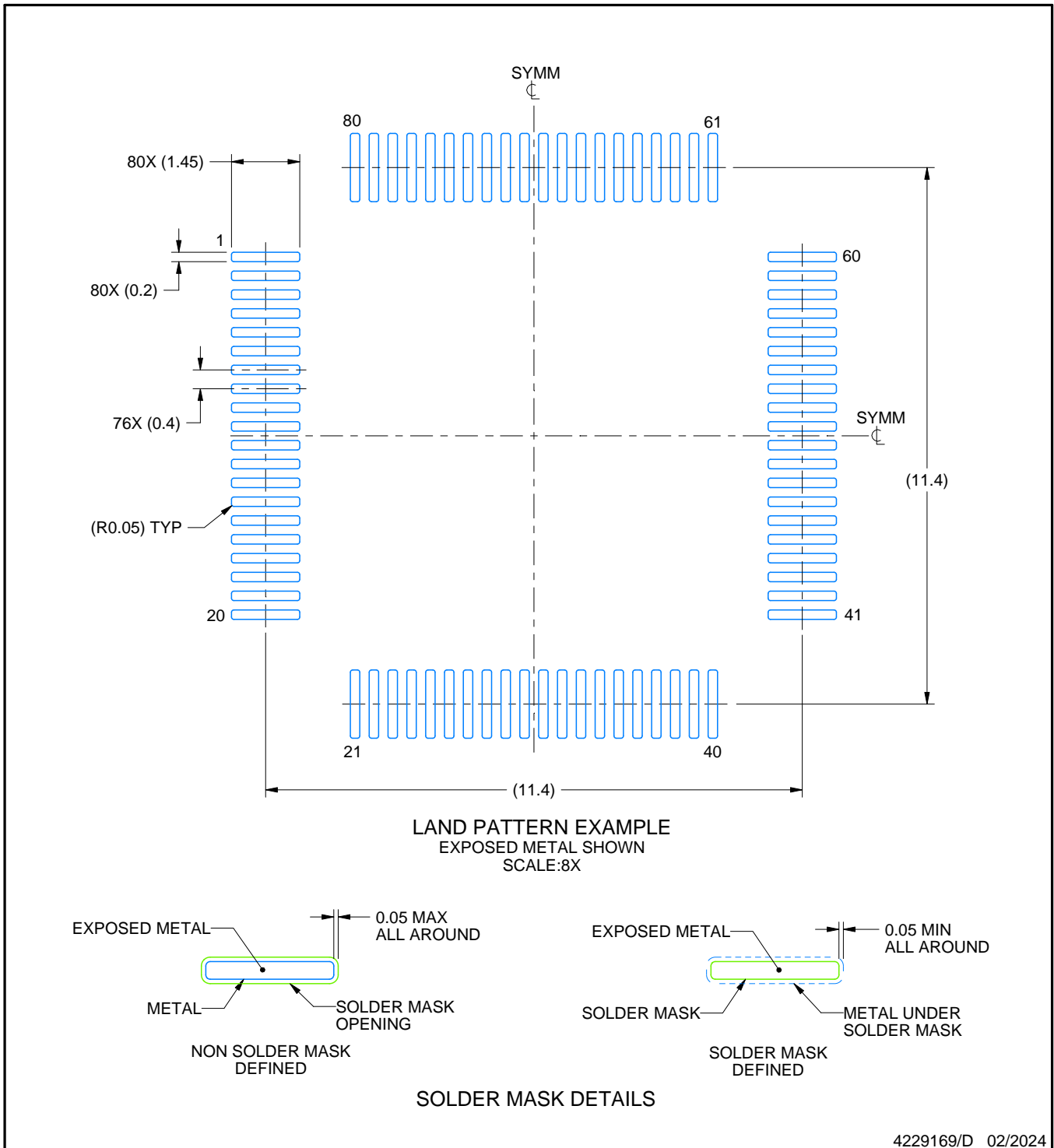
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PNA0080A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

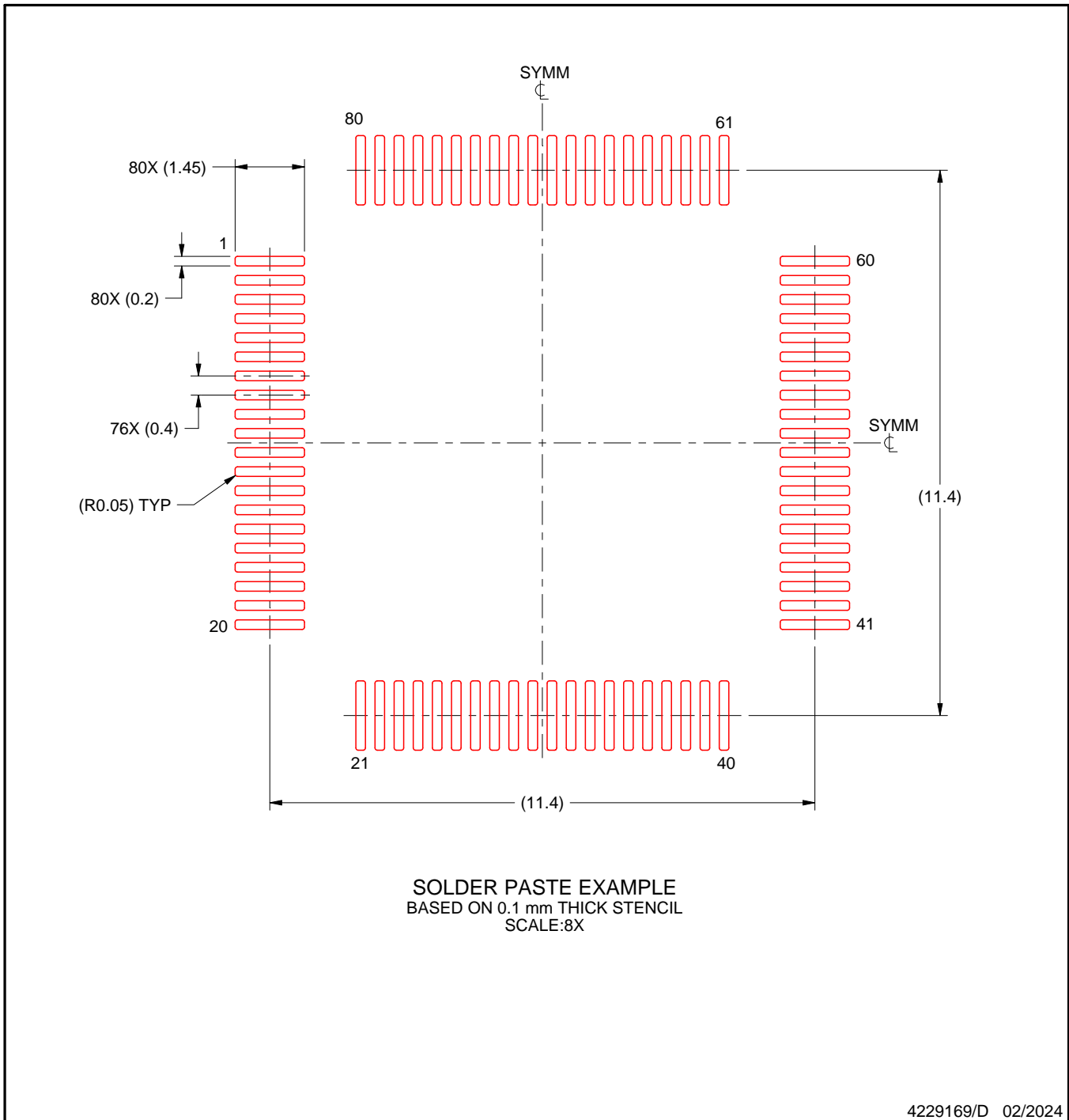
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PNA0080A

TQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PM0064A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.

EXAMPLE BOARD LAYOUT

PM0064A

LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).

EXAMPLE STENCIL DESIGN

PM0064A

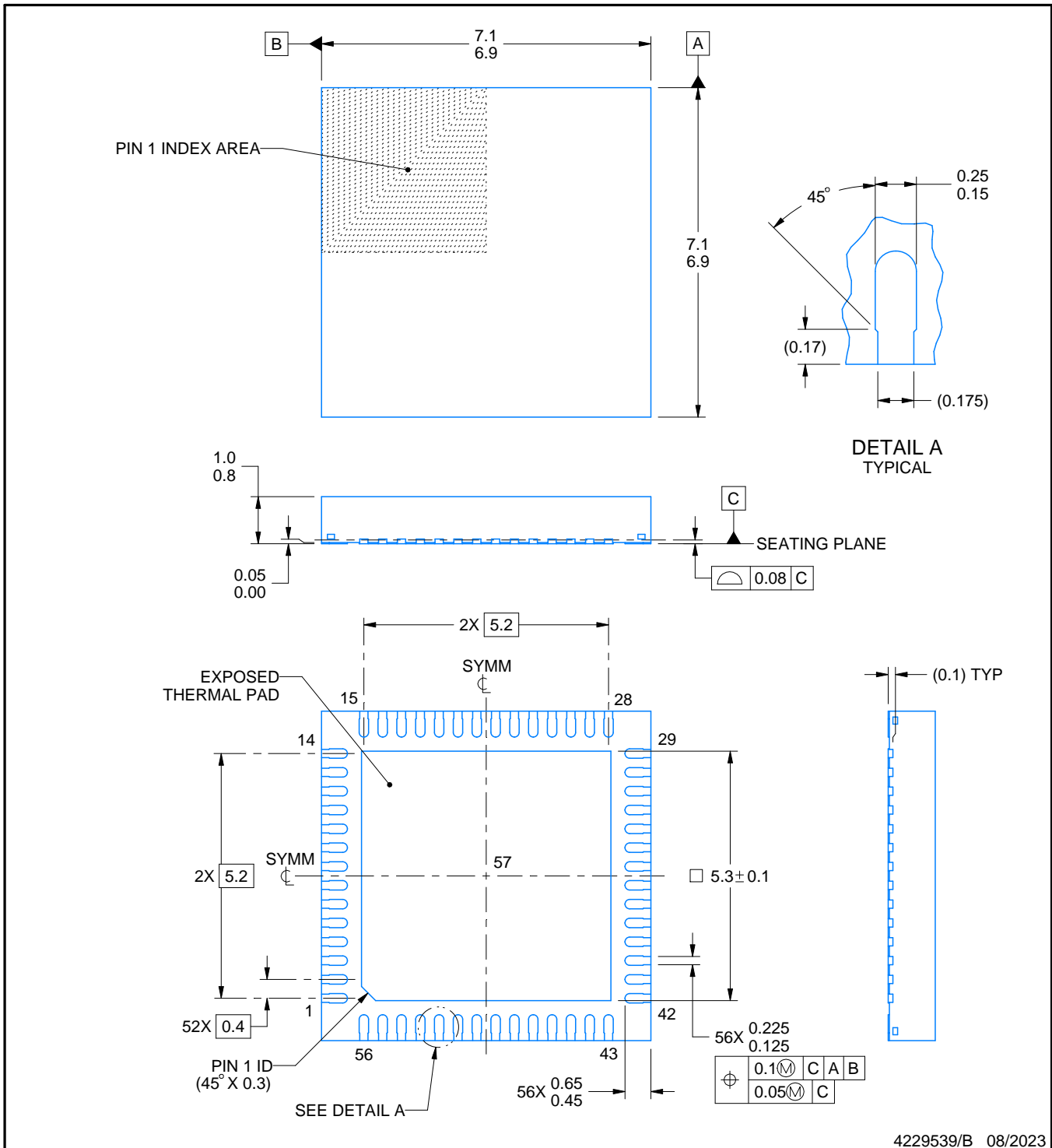
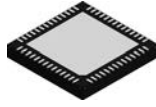
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4229539/B 08/2023

NOTES:

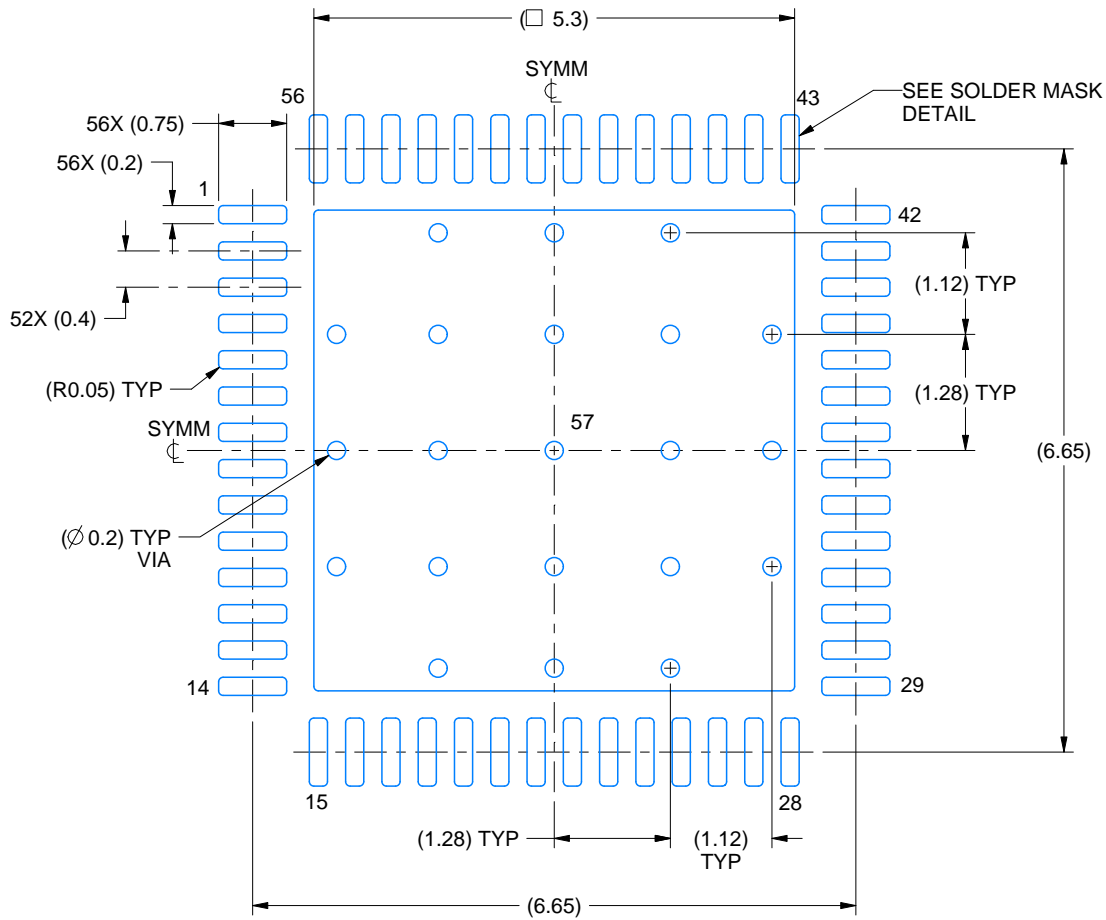
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

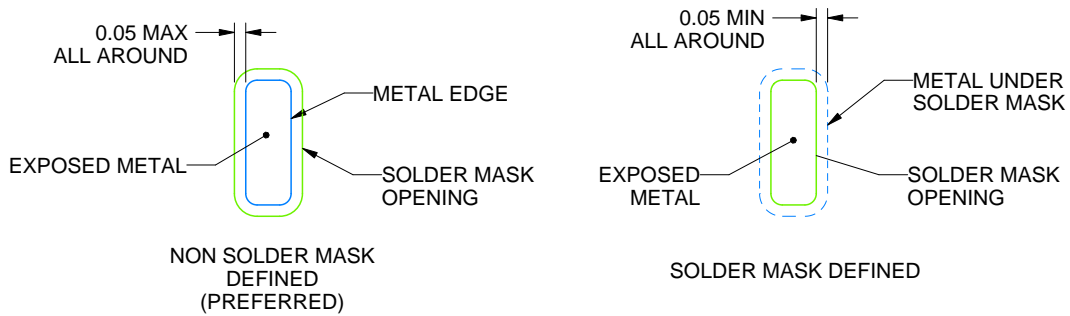
RSH0056G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X



SOLDER MASK DETAILS

4229539/B 08/2023

NOTES: (continued)

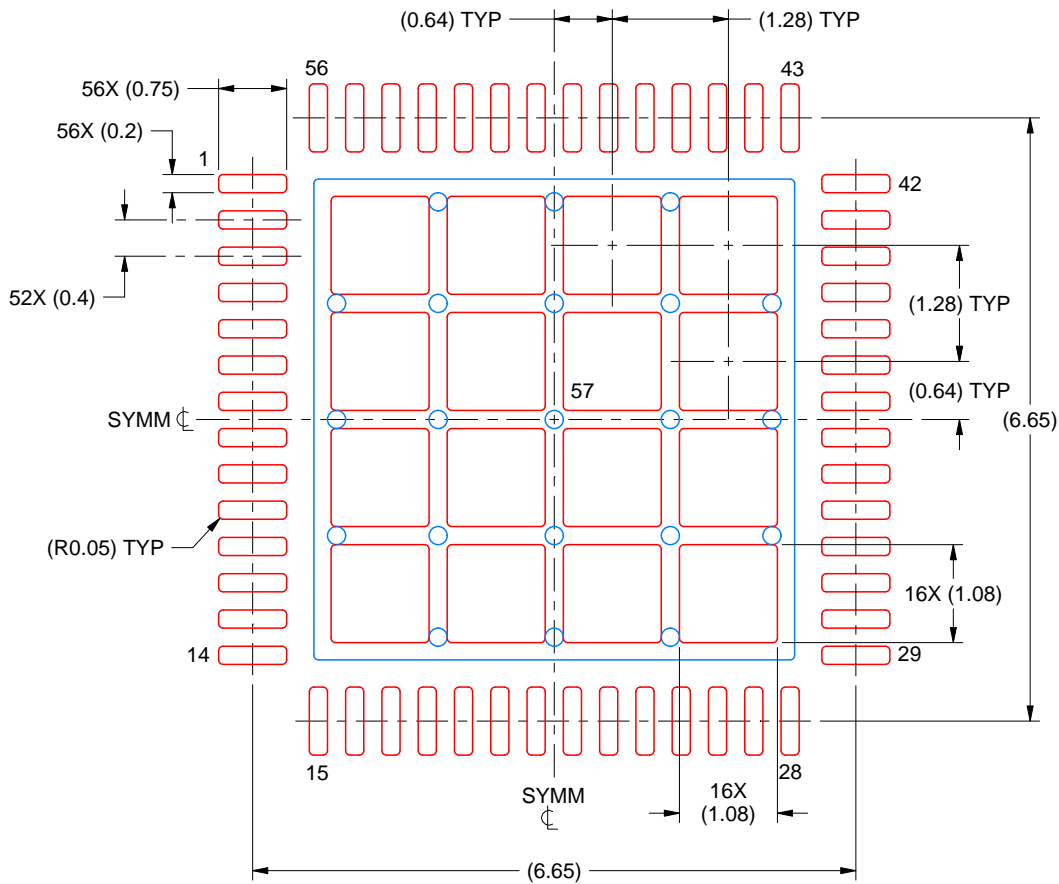
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSH0056G

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.100 MM THICK STENCIL
 SCALE: 12X

EXPOSED PAD 57
 66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4229539/B 08/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| XF28P550SJ9PDT | ACTIVE | TQFP | PDT | 128 | 90 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| XF28P550SJ9PM | ACTIVE | LQFP | PM | 64 | 160 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| XF28P550SJ9PNA | ACTIVE | TQFP | PNA | 80 | 160 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| XF28P550SJ9PZ | ACTIVE | LQFP | PZ | 100 | 90 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| XF28P550SJ9RSH | ACTIVE | VQFN | RSH | 56 | 3000 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| XF28P559SJ9PDTQ1 | ACTIVE | TQFP | PDT | 128 | 90 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| XF28P559SJ9PMQ1 | ACTIVE | TQFP | PTF | 128 | 160 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| XF28P559SJ9PNAQ1 | ACTIVE | TQFP | PNA | 80 | 160 | TBD | Call TI | Call TI | -40 to 150 | | Samples |
| XF28P559SJ9PZQ1 | ACTIVE | LQFP | PZ | 100 | 90 | TBD | Call TI | Call TI | -40 to 150 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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